A 10-dB Small-Signal Graphene FET Amplifier

M.A. Andersson, O. Habibpour, J. Vukusic and J. Stake

We report on the realisation of a graphene FET microwave amplifier operating at 1 GHz, exhibiting a small-signal power gain of 10 dB and a noise figure of 6.4 dB. The amplifier utilises a matching inductor on the gate yielding a return loss of 20 dB. The design is optimised for maximum gain and the optimum noise figure is extracted by noise modelling and predicted to be close to 1 dB for the intrinsic graphene FET at this frequency. The presented results complement existing graphene FET applications and are promising for future graphene microwave circuits.

Introduction: Solid-state transistor amplifiers are today fundamental components in any microwave and millimeter wave receiver system, with field effect transistors operating well into the terahertz range [1]. Recently discovered graphene is certainly an interesting candidate in this context, with its superior carrier mobilities of 100,000 cm^2/Vs and saturation velocity of $4{\cdot}10^7$ cm/s [2]. However, applications of graphene FETs (G-FETs) have so far been limited to frequency multipliers [3], mixers [4] and voltage amplifiers [5]. Despite a record $f_{max} = 35$ GHz, there is only one reported graphene microwave transistor with small-signal power gain when loaded with 50 Ω, for which $|S_{21}|^2 = 2$ dB was achieved [6]. Due to the low gain, there has been no possibility of performing an accurate noise figure measurement. As a result, no study has been conducted on the noise performance of G-FETs at microwave frequencies.

In this letter we demonstrate for the first time a G-FET microwave amplifier matched to 50 Ω utilising an inductor on the gate (Fig. 1), operating with 10 dB small-signal power gain at 1 GHz. The substantial gain improvement enables the first noise figure report of a G-FET amplifier, 6.4 ± 0.4 dB at 1 GHz. Finally, employing the noise model in [7], the extrinsic and intrinsic minimum noise figures of the G-FET are predicted to be approximately 3.3 dB and 1.0 dB, respectively, at 1 GHz.

G-FET Fabrication and Characterisation: The G-FET device design takes it starting point in the expression $|S_{21}| \approx \frac{2Z_0 g_{m,ex}}{Z_0 g_{d,ex}+1}$. In this expression $g_{m,ex} = \frac{\partial I_{ds}}{\partial V_{gs}}$ and $g_{d,ex} = \frac{\partial I_{ds}}{\partial V_{ds}}$ represent the extrinsic transconductance and extrinsic output conductance, respectively, as calculated from the measured DC characteristics of the transistor. To achieve $|S_{21}| > 1$ typically $g_{m,ex} > 15$ mS is required, in combination with $R_{ds,ex} = 1/g_{d,ex} = 100\ \Omega$, corresponding to the weak current saturation in G-FETs.

In order to have a better understanding of the device amplifying behavior based on its size and carrier transport parameters, DC simulations were carried out by utilising the large signal model proposed in [8]. At a drain voltage of $|V_{ds}| \approx 1$ V the important properties to have a sufficiently high $g_{m,ex}$ are mobilities on the order of 2000 cm^2/Vs and a gate capacitance per area $C_{ox} = 0.5\ F/cm^2$. Additionally, a relatively wide device is required, wherefore $W = 60\ \mu m$ was chosen. The channel length was kept at $L_g = 1\ \mu m$, for efficient gate modulation with the still high contact resistances in G-FETs. Subsequently, a simulation was conducted to verify the small-signal behavior to be satisfactory, especially $|S_{21}| > 1$.

The fabrication of the G-FET was performed on single-layer graphene on SiO_2 produced by micromechanical exfoliation. E-beam lithography was used to pattern the drain and source contacts, together with the extended, outer ground plane of the coplanar waveguide (CPW) lines. The metallisation consists of 1 nm Ti, 15 nm Pd and 60 nm Au by e-gun evaporation and lift-off. The gate oxide is 8 nm Al_2O_3 formed by three steps of 2 nm e-gun evaporated Al naturally oxidised on a hot-plate. Similarly, the gate, pads and inner CPW line for the inductor were patterned with e-beam lithography. At 1 GHz the electrical length of the CPW line connecting the inductor and the G-FET is estimated to be only a few degrees, and is thus negligible. Important for the noise properties of a FET is a low gate resistance [9], R_g, which is achieved by increasing the metal thickness to 500 nm.

The device transfer characteristics at $V_{ds} = -1.25$V, Fig. 2*a*, exhibits asymmetry with higher contact resistance on the electron branch, due to hole doping of the channel from the contacts. The optimum bias is thus at the gate voltage of maximum gm of the hole branch. Under this operation, the G-FET exhibits a maximum $g_m = 22$ mS, and from the output characteristics of Fig. 2*b*, $R_{ds} = 1/g_d \approx 100\ \Omega$. The associated gate leakage, $I_g \approx 10$ pA, is beneficial to have a minimum level of shot noise [9]. Finally, the extracted mobility is $\mu = 2000\ cm^2/Vs$ and the gate capacitance is $C_{ox} = 0.5\ \mu F/cm^2$. Further, S-parameters of the G-FET were measured on-wafer at 50 Ω utilising an Agilent E8361A PNA, together with the standard TRL calibration technique. The S-parameters presented in Fig. 2*c* are measured at $V_{ds} = -1.25$ V in the frequency range from 10 MHz to 10 GHz for the bare, unmatched G-FET. Without de-embedding, the device has an $f_T = 5$ GHz and an $f_{max} = 7$ GHz and, since $|S_{21}| > 1$ to 3.3 GHz, there is power gain also at 50 Ω.

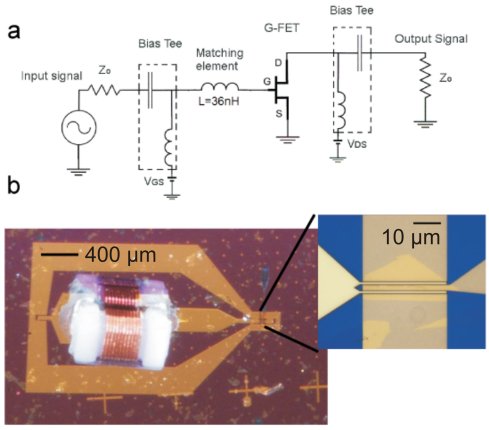

Fig. 1 *(a) Schematic of the G-FET amplifier including the external bias tees (b) Photo of the fabricated amplifier, with an inset showing the G-FET itself*

Amplifier Design and Characterisation: The final amplifier design was based on the measured G-FET S-parameters shown in Fig. 2*c*. The error of a unilateral gain design, about 1 dB, was considered unacceptable. Instead, the procedure is illustrated in Fig. 2*d*, which displays several available power gain, G_A, circles at the design frequency 1 GHz, with $G_{max} \approx 10$ dB at $\Gamma_{M,s} = 0.9\angle 29\,^\circ$. Clearly, a single series inductor is enough to match the input and enhance the gain substantially compared to a 50 Ω system. This simplifies the circuitry and has the advantage of easy DC bias. The chosen source reflection coefficient, $\Gamma_s = 0.9\angle 23\,^\circ$, corresponding to a series $L = 36$ nH, is also included. As a consequence, the predicted available power gain, including the inductor tolerance of 5 %, is close to the optimum value, with $G_A = 9 \pm 0.5$ dB. In order to achieve the same transducer power gain, G_T, the output must be conjugately matched, according to $\Gamma_L = (\Gamma_{out})^* = 0.3\angle 54\,^\circ$. Retaining the output connected to 50 Ω, though, the theoretically achieved value of the transducer power gain is $G_T \approx G_A - 0.5$ dB. Weighing the added complexity with additional lumped components to the gain improvement, the drain is kept at 50 Ω. A schematic drawing of the complete amplifier is given in Fig. 1*a*. Finally, a standard surface mount inductor (Coilcraft 0402CS), with a specified $Q \approx 44$ at 1 GHz corresponding to $R_{series} = 5\ \Omega$, was soldered on the input port. The design frequency is well below the resonance frequency of the inductor ($f_{res} > 2$ GHz). In Fig. 1*b* a photo of the fabricated amplifier is shown, with an inset of the G-FET.

The matched amplifier S-parameters were measured at $V_{ds} = -1.25$ V in the frequency range from 10 MHz to 1.5 GHz. The resulting input and output match are $|S_{11}| < -10$ dB, Fig. 3*a*, and $|S_{22}| < -8$ dB at the design frequency. For the input, this is clearly attributed to the matching network. Most importantly, Fig. 3*b* presents the gain of the tuned amplifier to be $G_T = 9.7$ dB at 1 GHz. This is slightly more than the designed value, since the fabricated amplifier has a Γ_s closer to $\Gamma_{M,s}$. Moreover, the overall maximum gain is $G_T = 10.4$ dB at 950 MHz. Also, the amplifier shows good reverse isolation, with $|S_{12}| < -20$ dB. Finally, the stability parameters are calculated with the stability factor $K > 1$ and the stability measure $b > 0$ meaning the amplifier is stable for all frequencies.

In addition, the noise figure of the tuned amplifier was measured at room temperature, at the same bias point, using an Agilent N8975A noise figure analyser and the uncertainty assessed according to [10]. It is plotted in Fig. 3*b*, together with a model fit utilising the Pospieszalski one temperature model [7] in combination with the direct extraction technique described in [11]. The frequency independent model temperature, T_d of R_{ds} given in Fig. 2*c*, represents the intrinsic channel noise. It was extracted using a least square fit to the most accurately measured noise figures from 500 MHz to 1.2 GHz where $G_T > 5$ dB. The small-signal model in Fig. 3*c* for the bare

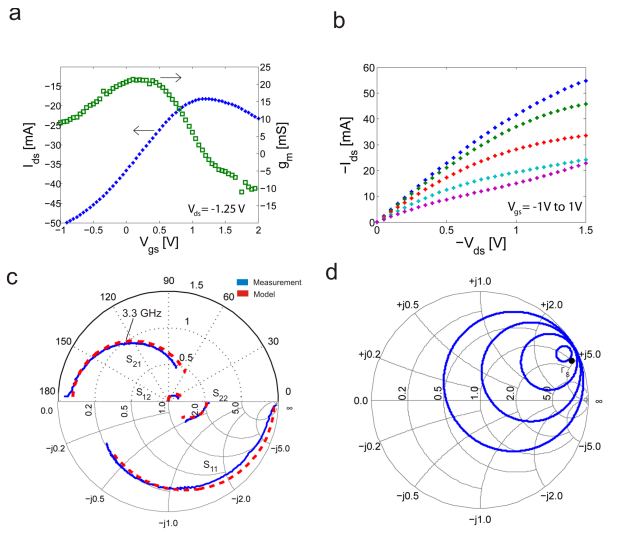

Fig. 2 *(a) Transfer characteristics and transconductance at $V_{ds} = -1.25$ V*
(b) Output characteristics at $V_{gs} = -1$ V (top) to $V_{gs} = 1$ V (bottom)
(c) S-parameters of bare G-FET from 10 MHz to 10 GHz at $V_{ds} = -1.25$ V
(d) G_A circles at 1 GHz from 0.1 dB to 9.1 dB in steps of 3 dB

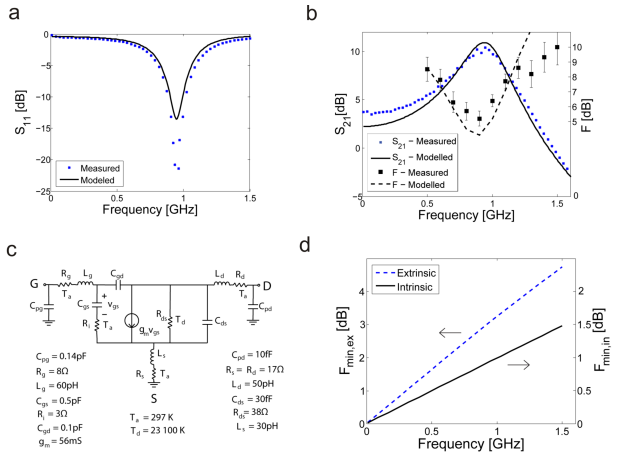

Fig. 3 *(a) Measured and modelled return loss, S_{11}, of the tuned amplifier*
(b) Measured and modelled gain and noise figure of the tuned amplifier
(c) Small-signal and noise parameters for the bare G-FET, including parasitics
(d) Modelled F_{min} of the G-FET amplifier from 10 MHz to 1.5 GHz, if tuned to the optimum source impedance at each frequency

G-FET was extracted according to [8] with resulting S-parameters in Fig. 2*c*. Particularly at 1 GHz, the noise figure is 6.4 ± 0.4 dB.

Importantly, low-noise and high gain designs in general require different Γ_s [9]. Thus, the best possible noise performance in tuning the G-FET amplifier was estimated with the noise model. The calculated minimum extrinsic noise figures are presented in Fig. 3*d*, especially $F_{min,ex} = 3.3$ dB at 1 GHz. Also, the predicted achievable intrinsic noise figures of the G-FET, in minimising the parasitic resistances, are included in Fig. 3*d*, particularly $F_{min,in} = 1$ dB at 1 GHz. To reach the performance of HEMTs with $F_{min} < 1$ dB [12], G-FETs thus need further improvement.

Conclusion: The first G-FET amplifier matched to 50 Ω at microwave frequencies has been reported, which allowed for a substantial gain improvement compared to previous work. Noise modelling techniques were utilised to estimate the minimum noise figure of the G-FET itself.

Acknowledgment: This work has been supported by the Swedish Foundation of Strategic Research.

M. Andersson, O. Habibpour, J. Vukusic and J. Stake (*Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96 Göteborg, Sweden*)

E-mail: andmic@chalmers.se

References

1 Samoska, L.A.: 'An Overview of Solid-State Integrated Circuit Amplifiers in the Submillimeter-Wave and THz Regime', *IEEE Transactions on Terahertz Science and Technology*, 2011, **1**, (1), pp. 9-24
2 Schwierz, F.: 'Graphene transistors', *Nature Nanotechnology*, 2010, **5**, (7), pp. 487-496
3 Wang, H., Hsu, A., Wu, J., Kong, J. and Palacios, T.: 'Graphene Frequency Multipliers', *IEEE Electron Device Letters*, 2009, **30**, (5), pp. 547-549
4 Habibpour, O., Cherednichenko, S., Vukusic, J., Yhland, K. and Stake, J.: 'A Subharmonic Graphene FET Mixer', *IEEE Electron Device Letters*, 2012, **33**, (1), pp. 71-73
5 Han, S.-J., Jenkins, K.A., Valdes-Garcia, A., Franklin, A.D., Bol, A.A. and Haensch, W.: 'High-Frequency Graphene Voltage Amplifier', *Nano Letters*, 2011, **11**, pp. 3690-3693
6 Wu, Y.Q., Farmer, D.B., Valdes-Garcia, A., Zhu, W.J., Jenkins, K.A., Dimitrakopoulos, C., Avouris, Ph. and Lin, Y.-M.: 'Record High RF Performance for Epitaxial Graphene Transistors', *Tech. Dig. IEDM*, 2011, pp. 528-530
7 Pospieszalski, M.W.: 'Modeling of Noise Parameters of MESFET's and MODFET's and Their Frequency and Temperature Dependence', *IEEE Transactions on Microwave Theory and Techniques*, 1989, **37**, (9), pp. 1340-1350
8 Habibpour, O., Vukusic, J. and Stake, J.: 'A Large Signal Graphene FET Model', *IEEE Transactions on Electron Devices*, 2012, **59**, (4)
9 Maas, S.A.: Noise in Linear and Nonlinear Circuits, 2005, Artech House
10 'Noise Figure Measurement Accuracy - The Y-Factor Method,' *Agilent Application Note*, 57-2.
11 Garcia, M., Stenarson, J., Yhland, K., Zirath, H. and Angelov, I.: 'A New Extraction Method for the Two-Parameter FET Temperature Noise Model', *IEEE Transactions on Microwave Theory and Techniques*, 1998, **46**, (11), pp. 1679-1685
12 Schleeh, J., Alestig, G., Halonen, J., Malmros, A., Nilsson, B., Nilsson, P.A., Starski, J.P., Wadefalk, N., Zirath, H. and Grahn, J.: 'Ultralow-Power Cryogenic InP HEMT With Minimum Noise Temperature of 1 K at 6 GHz', *IEEE Electron Device Letters*, 2012, **33**