A Large Signal Graphene FET Model

Omid Habibpour, *Student Member, IEEE,* Josip Vukusic, Jan Stake, *Senior Member, IEEE*

***Abstract*—We propose a semiempirical graphene field effect transistor (G-FET) model for analysis and design of G-FET based circuits. The model describes the current-voltage characteristic for a G-FET over a wide range of operating conditions. The gate bias dependence of the output power spectrum is studied and compared with simulated values. A good agreement between the simulated and the experimental power spectrum up to the 3rd harmonic is demonstrated which confirms the model validity. Moreover, S-parameter measurements essentially coincide with the results obtained from the simulation. The model contains a small set of fitting parameters which can straightforwardly be extracted from S-parameters and DC measurements. The developed extraction method gives a more accurate estimation of the drain and source contact resistances compared to other approaches. As a design example, we use a harmonic-balance load-pull approach to extract optimum embedding impedances for a subharmonic G-FET mixer.**

***Index Terms*—Graphene, Microwave FETs, semiconductor device modeling, subharmonic mixer, harmonic balance analysis.**

I. Introduction

GRAPHENE field effect transistors (G-FETs) are now approaching millimeter wave operation. G-FETs with intrinsic cutoff frequency (f_T) of more than 100 GHz have been demonstrated [1], [2]. Several circuits including frequency doublers [3], [4], fundamental frequency mixers [5], [6] and a subharmonic frequency mixer [7] based on G-FETs have been presented at microwaves frequencies. Moreover, a wafer-scale graphene MMIC mixer has been demonstrated [8]. Hence, in the near future, system-level graphene integrated circuits are a possible reality. Consequently, there is a demand for a device model that can predict a G-FET's behavior based on its basic transport parameters and can be implemented in standard circuit simulator programs.

Device models can be divided into two major groups: physical models and empirical models. Physical models are important in the early stages of device development and they provide better understanding of the device behavior based on its carrier transport parameters. Several physical models for G-FETs have been demonstrated [9], [10], [11], [12]. However, since the physical models are based on device physics, they are usually too intricate for circuit level modeling. They are neither fast nor easily implemented for use in circuit design tools. Empirical (semiempirical) models can provide acceptable accuracy with less calculation time and they can be implemented in standard Electronic Design Automation (EDA) tools. Recently several models for G-FETs have been proposed [13], [14], [15]. These models can describe the current-voltage characteristics. However, they utilize the same carrier mobility for electrons and holes, and the same contact resistance independent of the carrier type in the channel. Due to the substrate effect, the carrier mobility differs for electrons and holes [7], [16]. Moreover, because of the charge transfer between graphene and metal contacts, G-FETs generally experience different contact resistances depending on the carrier type in the channel [18]. Consequently, there is an asymmetry in the transfer characteristic of G-FETs, especially for short gate-length devices. The above models cannot predict this phenomenon. Lately, an empirical model for a short-channel Si MOSFET has been used to model G-FETs [17]. It allows the calculations of I-V characteristics. Nevertheless, the model uses the same carrier mobility for both electrons and holes. Up to now, all the proposed models are only validated by DC measurements. RF characterization methods, especially power spectrum analysis, reveals more details about the model accuracy and this validation method is missing in the all previous proposed models.

In this paper we utilize the semiempirical square-root charge-voltage relation and present an analytical model for G-FETs [19]. This model is derived for a single layer zero-bandgap graphene and it can accept different electron and hole mobilities. The model reflects the inherent symmetry of the intrinsic G-FETs and, is similar to the model developed for HEMTs and MOSFETs [20]. Moreover, it can take into account the asymmetric contact resistance for the n-type and p-type channel. The model has only a few fitting parameters and the parameter extraction is performed by means of both S-parameters and DC data. It is experimentally verified for a G-FET under both DC and RF operation. The RF verification includes S-parameters and power spectrum measurements. The results agree well with the model. Furthermore, as a design example, load-pull harmonic balance simulation is performed to extract optimum embedding impedances for a subharmonic G-FET mixer [7].

II. Device Model

A. Intrinsic Device

The object of this work is to develop a closed-form large signal analytical model for the G-FET, which can be utilized in EDA tools for designing and analyzing G-FET circuits.

Since the intrinsic device of the equivalent circuit (Fig. 1) has three terminals, gate, drain, and source, it is possible to express the drain current, I_{ds} as a function of any two voltages between these terminals. We select V_{gs} and V_{gd} as independent variables because of the symmetric structure of the G-FETs and since the drain and source are interchangeable. In order to distinguish between intrinsic and extrinsic voltages, capital letters are used for the latter case, i.e V_{GS}.

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The authors are with the Terahertz and Millimetre Wave Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96 Göteborg, Sweden (e-mail: omid.habibpour@chalmers.se).

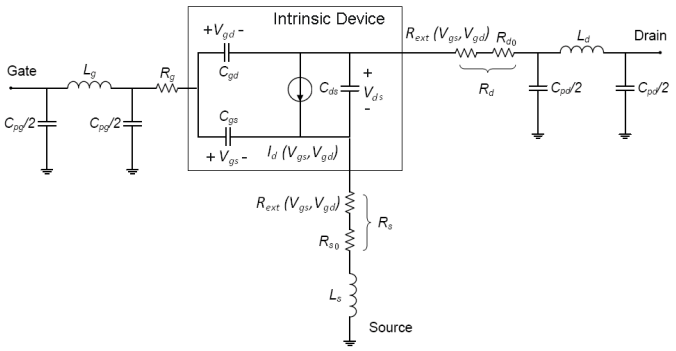

Fig. 1. Large signal model of a G-FET. C_{pg}, C_{pd}, L_g, L_d and L_s are pad parasitic capacitances and inductances. R_g is the gate resistances and, R_s and R_d are the source and drain resistances including contact and access resistances.

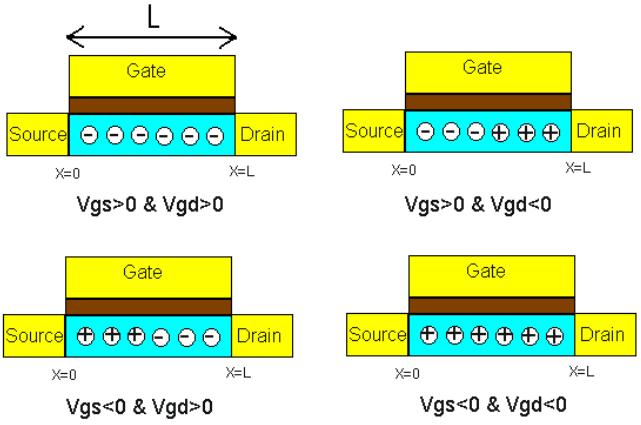

Fig. 2. Majority carrier type in a G-FET channel at 4 different V_{gs}- V_{gd} plane quadrants.

The type of majority carriers in the G-FET channel can be determined depending on which quadrant of the $V_{gs} - V_{gd}$ plane the device bias is : the carriers are electrons for ($V_{gs} > 0$, $V_{gd} > 0$), both electrons (near the source) and holes (near the drain) for ($V_{gs} > 0$, $V_{gd} < 0$), both electrons (near the drain) and holes for (near the source) ($V_{gs} < 0$, $V_{gd} > 0$), and holes for ($V_{gs} < 0$, $V_{gd} < 0$) (see Fig.2 for illustration). The current in the channel can be expressed as

$$I_{ds} = q\frac{W}{L}\int_0^L n(x)v_{drift}(x)\,\mathrm{d}x \tag{1}$$

where $n(x)$, $v_{drift}(x)$, L and W are the carrier density, the carrier velocity, the channel length and the channel width respectively. The carrier density $n(x)$, should be equal to the thermally generated carriers, n_{th} ($8\times10^{10}cm^{-2}$ at T = 300 K) for disorder-free graphene layer at zero gate voltage. However, the measured data shows that the carrier concentration at zero gate voltage is higher than n_{th} [19]. This is due to the charge impurities located at the graphene/dielectric interface or inside the dielectric, generating extra carriers (electrons or holes) in graphene layer [21]. This effect is modeled in [19] by the following semi-empirical charge-voltage relation,

$$n(x) = \sqrt{n_0^2 + (C\times V(x)/q)^2} \tag{2}$$

where n_0 is the residual carrier density due to disorder and thermal excitation. This is the minimum charge concentration of the graphene layer and $C = (C_{gs} + C_{gd})/(LW)$ is the gate capacitance per area. The total gate capacitance consists of the gate oxide capacitance, C_{ox} in series with the graphene quantum capacitance, C_q. In this model, since $C_q \gg C_{ox}$, the effect of C_q is ignored. This is valid except for ultra thin gate dielectrics [24]. We note that above equation reduces to the familiar $n(x) = C\times V(x)/q$ at high gate voltage, and to $n = n_0$ at zero gate voltage.

Moreover, the carrier drift velocity is approximated by the following velocity saturation model [22], [23].

$$v_{drift}(x) = \frac{\mu E(x)}{\sqrt[m]{1 + (\frac{\mu|E(x)|}{v_{sat}})^m}} \tag{3}$$

where v_{sat} is the saturation velocity of the carrier, μ is the carrier mobility and m is a fitting parameter. The v_{sat} depends on carrier concentration in this model with $v_{sat}(n) = v_F\beta/\sqrt{n}$ where $v_F = 10^8\ cm/s$ and β relates to the optical phonon wavelength of the dominant scattering phonon and for graphene on SiO_2 $\beta = 4\times10^5 cm^{-1}$[13]. The above expression is valid for $n > 1.1\times10^{11}cm^{-2}$ [23] where the minimum value of n is n_0. To the best of the authors knowledge the minimum reported value of n_0 is $2.2\times10^{11}cm^{-2}$ [19] in supported and top gated graphene. With this range of n_0, $v_{sat} < v_F$, although generally the quoted values of n_0 are significantly higher. We also assume a constant carrier mobility for electrons and holes (μ_e and μ_h).

In the first quadrant($V_{gs} > 0$, $V_{gd} > 0$)

$$I_{ds} = q\frac{W}{L}\int_0^L n(x)\frac{\mu E(x)}{\sqrt[m]{1 + (\frac{\mu|E(x)|}{v_{sat}(n(x))})^m}}\,\mathrm{d}x \tag{4}$$

knowing that $dV = E(x)dx$

$$I_{ds} = q\frac{W}{L}\int_{V_{gd}}^{V_{gs}} \frac{\mu n(V)}{\sqrt[m]{1 + (\frac{\mu|E(V)|}{v_{sat}(V)})^m}}\,\mathrm{d}V \tag{5}$$

For simplicity, the velocity saturation value at the average gate voltage is used in the above expression $\overline{v}_{sat} = v_F\beta/\sqrt[4]{n_0^2 + (C(V_{gs}+V_{gd})/2q)^2}$ and also $|E(V)|$ is approximated by $|V_{gs} - V_{gd}|/L$ and

$$I_{ds1} = \frac{\mu_e}{\sqrt[m]{1 + (\frac{\mu_e|V_{gs}-V_{gd}|}{L\overline{v}_{sat}})^m}}\frac{W}{L}(V_{gs}\sqrt{Q_0^2 + (CV_{gs})^2} - V_{gd}\sqrt{Q_0^2 + (CV_{gd})^2} + q^2/C\ln\frac{\sqrt{Q_0^2 + (CV_{gs})^2} + CV_{gs}}{\sqrt{Q_0^2 + (CV_{gd})^2} + CV_{gd}}) \tag{6}$$

where Q_0 ($q\times n_0$) is the residual charge density. In order to simplify the equation notation, the following unitless function

is defined:

$$f(x,y) = x\sqrt{1+x^2} - y\sqrt{1+y^2} + \ln\frac{\sqrt{1+x^2}+x}{\sqrt{1+y^2}+y} \tag{7}$$

and defining $\bar{V}_{gs} = V_{gs}/V_0$ and $\bar{V}_{gd} = V_{gd}/V_0$ where $V_0 = Q_0/C$ and therefore,

$$I_{ds1} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1+(\frac{\mu_e|V_{gs}-V_{gd}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}f(\bar{V}_{gs},\bar{V}_{gd}) \tag{8}$$

In the second quadrant ($V_{gs} > 0$, $V_{gd} < 0$) there is a point in the channel ($x = L_1$) where the voltage is the same as the gate voltage. At this point, the type of majority carriers changes from electrons to holes.

$$I_{ds} = \frac{W}{L}\left(\int_0^{L_1} e\times n(x) v_{drift,e}\,\mathrm{d}x + \int_{L_1}^{L} e\times n(x) v_{drift,h}\,\mathrm{d}x\right) \tag{9}$$

after integration we have

$$I_{ds2} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1+(\frac{\mu_e|V_{gs}-V_{gd}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}f(\bar{V}_{gs},0) + \frac{\mu_h V_0 Q_0}{\sqrt[m]{1+(\frac{\mu_h|V_{gs}-V_{gd}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}f(0,\bar{V}_{gd}) \tag{10}$$

In the third quadrant ($V_{gs} < 0$, $V_{gd} > 0$) using the same procedure as before

$$I_{ds3} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1+(\frac{\mu_h|V_{gs}-V_{gd}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}f(\bar{V}_{gs},0) + \frac{\mu_e V_0 Q_0}{\sqrt[m]{1+(\frac{\mu_e|V_{gs}-V_{gd}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}f(0,\bar{V}_{gd}) \tag{11}$$

and finally for the forth quadrant ($V_{gs} < 0$, $V_{gd} < 0$) we have

$$I_{ds4} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1+(\frac{\mu_h|V_{gs}-V_{gd}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}f(\bar{V}_{gs},\bar{V}_{gd}) \tag{12}$$

The above equations describe I_{ds} based on the V_{gd} and V_{gs} in different quadrants. We combine the above equations and write the I_{ds} for all bias conditions as

$$I_{ds} = I_{ds1}\Theta(V_{gs})\Theta(V_{gd}) + I_{ds2}\Theta(V_{gs})\Theta(-V_{gd}) \; I_{ds3}\Theta(-V_{gs})\Theta(V_{gd}) + I_{ds4}\Theta(-V_{gs})\Theta(-V_{gd}) \tag{13}$$

where $\Theta(x)$ is the step function. Fig. 3 shows a contour plot of the drain current of a G-FET based on intrinsic V_{gs} and V_{gd} with μ_e = 2000 cm^2/Vs, μ_h = 2400 cm^2/Vs, $n_0 = 6\times 10^{11} cm^{-2}$, $L = 1\mu m$ and $m = 1$.

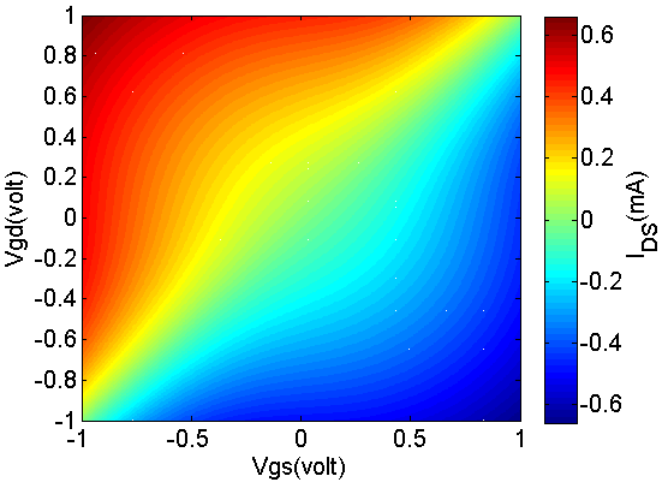

Fig. 3. Contour plot of drain current ($I_{ds}(mA/\mu m)$) of a G-FET versus the intrinsic V_{gs} and V_{gd}. μ_e = 2000 cm^2/Vs, μ_h = 2400 cm^2/Vs, $n_0 = 6\times 10^{11} cm^{-2}$, $L = 1\mu m$

In the above expressions we assume that there is no unintentional charging (doping) in the channel, i.e. $V_{Dirac} = 0$ at low drain voltages ($V_{ds} \ll 1$). Hence, in order to include this effect above equation should be modified by putting $V_{gs} - V_{Dirac}$ and $V_{gd} - V_{Dirac}$ instead of V_{gs} and V_{gd} respectively.

The convergence of some simulation techniques such as harmonic-balance and transient analysis, requires continuous first- and second-order derivatives [25]. Consequently, the model should have continuous high-order derivatives. Since $f(x,y)$ has high-order partial derivatives ($\frac{\partial^n f(x,y)}{\partial x^n}, \frac{\partial^n f(x,y)}{\partial y^n}$), by replacing $\Theta(x)$ with a smooth analytic function in equation 13, I_{ds} will have high order continuous derivatives. For that reason, $\Theta(x) \simeq U(x) = (1 + tanh(x/V_1))/2$ where V_1 is a fitting parameter.

Finally, from above equations the transconductance $g_m = dI_d/dV_{gs}|_{V_{ds}=const}$ of the intrinsic device can be approximated in the different quadrants as,

$$g_{m1,4} = \frac{2\mu_{e,h}}{\sqrt[m]{1+(\frac{\mu_{e,h}|V_{ds}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}C\left(\sqrt{V_0^2+V_{gs}^2} - \sqrt{V_0^2+(V_{gs}-V_{ds})^2}\right) \tag{14}$$

$$g_{m2,3} = \frac{2\mu_{e,h}}{\sqrt[m]{1+(\frac{\mu_{e,h}|V_{ds}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}C\sqrt{V_0^2+V_{gs}^2} - \frac{2\mu_{h,e}}{\sqrt[m]{1+(\frac{\mu_{h,e}|V_{ds}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}C\sqrt{V_0^2+(V_{gs}-V_{ds})^2} \tag{15}$$

From above equations, $g_{m,Max} = \frac{2\mu_{e,h}}{\sqrt[m]{1+(\frac{\mu_{e,h}|V_{ds}|}{L\bar{v}_{sat}})^m}}\frac{W}{L}C|V_{ds}|$ and for high carrier mobility, $g_{m,Max} \simeq 2\bar{v}_{sat}WC$. It should be noted that this value is obtained from the intrinsic part (without including parasitic drain and source resistances) and therefore it is an upper limit of the G-FET transconductance.

B. Drain and Source Resistance Model

Measurement data [18], [26] shows that there is a difference in the conductivity of G-FETs depending on whether the majority carriers in the G-FET channel are electrons ($V_{gs} > 0$, $V_{gd} > 0$) or holes ($V_{gs} < 0$, $V_{gd} < 0$). This effect mainly comes from the charge transfer between the graphene and the metal contact. The charge type can be electrons or holes depending on the work function of the deposited metal [27]. When the carrier type of the G-FET channel is the opposite of the charge in the metal-graphene contact, a p-n barrier is formed and adds an extra resistance [28]. For submicron gate-length G-FETs, this phenomenon dominates the whole channel resistance [2], [26]. Therefore including this term is necessary for G-FET modeling. In order to model this effect we add a carrier dependent term to the drain and source resistors,

$$R_s = R_{s0} + R_{ext}(V_{gs}, V_{gd}) \tag{16}$$

$$R_d = R_{d0} + R_{ext}(V_{gs}, V_{gd}) \tag{17}$$

$$R_{ext}(V_{gs}, V_{gd}) = \frac{1 + tanh(V_{gs}/V_2)}{2} \frac{1 + tanh(V_{gd}/V_2)}{2} \times R_{exto}$$

In the above expression when the majority carriers in the G-FET channel are electrons, an extra resistance, R_{exto} appears in the drain and source resistances and V_2 is a fitting parameter. Since the metal-graphene contact scales with the contact width rather than the contact area [28] and the drain and source have the same contact width, we can assume R_{s0}=R_{d0}=R_0.

Since in the large area graphene there is no bandgap, the contact resistance becomes more critical as the gate length decreases. The main effect than can be seen in very short gate-length (L_g < 100-150 nm) G-FETs, is that by changing the gate voltage, the current variation for n- (p-) channel becomes much smaller than the current variation for p- (n-) channel [29], [2]. In other words G-FET behaves like a unipolar FET. A high value of R_{exto} can be used for modelling the above effect. Also in [30] it has been shown that the saturation velocity is almost independent of the gate-length while the carrier mobility generally decreases when reducing the gate-length.

III. Parameter Extraction

Device parameters are extracted from both DC and S-parameters measurements. The measured S-parameters are used in order to extract the extrinsic parasitic elements as well as intrinsic capacitors (Fig. 1). For parasitic elements, S-parameters of the open and short structures are needed. In conventional FETs, the open and short structures are obtained by biasing the device under the forward-biased gate and pinched off respectively (V_{DS} = 0, cold-FET technique) [31], [32]. However, the G-FET channel can not be pinched off. Consequently, the method must be modified for the G-FET. As described in [2], 'open' and 'short' structures with identical layouts, excluding graphene are used to deembed the parasitic elements and calculate the intrinsic elements by $Y_{intrinsic} = ((Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}$. However, since the 'open' and 'short' structures do not include graphene in channel, the parasitic drain and source resistances achieved by this method do not include the contact and access resistances. These resistances are the main contributions to the parasitic resistances and as a result, this method underestimates the contact resistances. For example in [2] the extracted drain and source resistances for graphene of about 3 μm width are 13.9 Ω (42 $\Omega.\mu m$) and 2.4 Ω (7 $\Omega.\mu m$) respectively. These values are more than an order of magnitude lower than the lowest reported contact resistance for a single layer graphene at room temperature (500 $\Omega.\mu m$) [28]. Consequently we modify the the method as follows:

1. Open and short structures with identical layouts, excluding the graphene are used to extract $L_s, L_g, L_d, C_{pg}, C_{pd}$ and R_g.
2. For extraction of R_d and R_s (R_0 and R_{ext}), the drain is biased at a low voltage. At low drain voltage ($|V_{ds}/V_{gd}|$,$|V_{ds}/V_{gs}| \ll 1$) equation 8 and 12 can be written as $I_{DS} = \mu_e(W/L)Q_0\sqrt{1 + (V_{gs}/V_0)^2}V_{ds}$ and $I_{DS} = \mu_h(W/L)Q_0\sqrt{1 + (V_{gs}/V_0)^2}V_{ds}$ respectively and as a result, the drain to source resistance becomes

$$R_{DS} = 2R_0 + 2R_{exto} + \frac{\alpha_{\mu_e}}{\sqrt{1 + (V_{gs}/V_0)^2}} \tag{18}$$

for $V_{gs} \gg V_{Dirac}$ and

$$R_{DS} = 2R_0 + \frac{\alpha_{\mu_h}}{\sqrt{1 + (V_{gs}/V_0)^2}} \tag{19}$$

for $V_{gs} \ll V_{Dirac}$ where $\alpha_{\mu_{e,h}} = L/(W\mu_{e,h}Q_0)$. By fitting the R_{ds} profile with above equations R_d and R_s (R_0 and R_{exto}) as well as $\alpha_{\mu_{e,h}}$ and V_0 can be extracted.

3. The capacitors of the intrinsic device can be obtained by biasing the gate voltage of the G-FET at the minimum conductivity ($V_{GS} = V_{Dirac}$) and measuring the S-parameters. Since the device is biased at V_{Dirac}, the transconductance, g_m becomes zero. The parasitic elements obtained from the previous sections can be deembedded [33] and the remaining small signal model is depicted in Fig. 4. It can be shown that

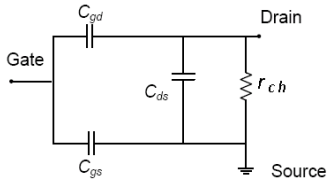

Fig. 4. Small signal model after deembedding the parasitic elements at $V_{GS} = V_{Dirac}$.

$$C_{gd} = -Y_{12}/j\omega, C_{gs} = (Y_{11} + Y_{12})/j\omega, \tag{20}$$

$$C_{ds} = Im(Y_{22} + Y_{12})/\omega \tag{21}$$

where Y is the admittance matrix of the structure in Fig. 4.

4. The rest of the parameters are calculated as follow:

$$C = (C_{gs} + C_{gd})/(LW) \tag{22}$$

$$Q_0 = CV_0 \tag{23}$$

$$\mu_{e,h} = L/(W\alpha_{\mu_{e,h}}Q_0) \tag{24}$$

TABLE I
MODEL PARAMETERS

Element	value
C_{gs}	25 fF
C_{gd}	22 fF
C_{ds}	48 fF
C_{pd}	18 fF
C_{pg}	20 fF
L_s	31 pH
L_d	43 pH

Element	value
L_g	75 pH
R_g	12 Ω
R_o	28 Ω
R_{exto}	5 Ω
μ_e	2000 cm^2/Vs
μ_h	2400 cm^2/Vs
V_0	0.41 V

IV. Results

The model has been implemented in a circuit simulation software (ADS) and verified by the experimental DC and RF characterization of a G-FET. The G-FET fabrication process is the same as the method described in [7]. By the method described in the previous section, the model's parameters have been extracted and presented in table I (W_{ch} = 20μm and L_{ch} = 1μm) with fitting parameters of m = 1, V_1 = 1/3 V and V_2 = 1/4 V.

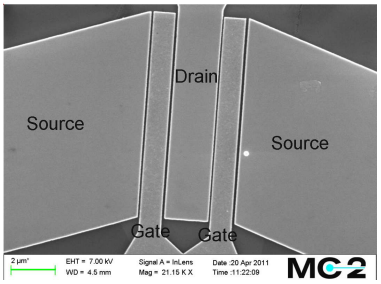

Fig. 5. SEM image of the G-FET, L_g = 1μm , W_g = 20μm.

The measured G-FET drain-source resistance versus the fitted model is shown in Fig. 6. The transconductance and $I_{DS} - V_{DS}$ characteristic curves at different V_{GS} are depicted in figures 7 and 8 respectively. As can be seen the model is in good agreement with the measurement. For the $I_{DS} - V_{DS}$ characterization, a pulsed I-V measurement was used to avoid the self heating effect at high drain voltages [34]. The simulated voltage range has been extended beyond the experiment range in order to show the formation of p-n junction along the channel. For example at $V_{GS} - V_{Dirac}$ = 2 V, when V_{DS} reaches 2 V a p-n junction starts to form.

Moreover, measured and modeled S-parameters are shown in Fig. 9. The measurement is performed from 1 GHz to 30 GHz with an Agilent PNA with on-wafer probing. As described in the previous section, for extracting the capacitors of the intrinsic device, S-parameters of the G-FET biased at V_{GS} = V_{Dirac} are needed. At this bias point, g_m = 0, and consequently S_{12} = S_{21}. Therefore, V_{Dirac} can be found by tuning the gate voltage until S_{12} and S_{21} completely coincide. For example for V_{DS} = 0.1 and 0.5 V in this device, we have V_{Dirac} = 1 and 1.22 V respectively (Fig. 9 a,b). Fig. 9 c,d show the measured and modeled S-parameters for the maximum g_m with V_{DS} = 0.1 and 0.5 V.

In order to investigate the model accuracy more in detail, a power spectrum analysis is performed. This is done by

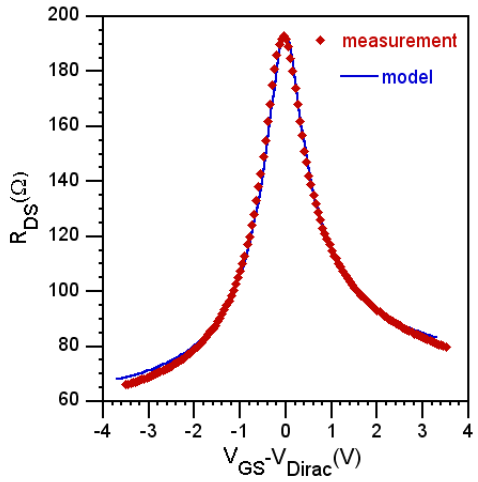

Fig. 6. Fitted data (solid line) versus measured data (♦) for the drain-source resistance (V_{Dirac} = 1 V, V_{DS} = 0.1 V).

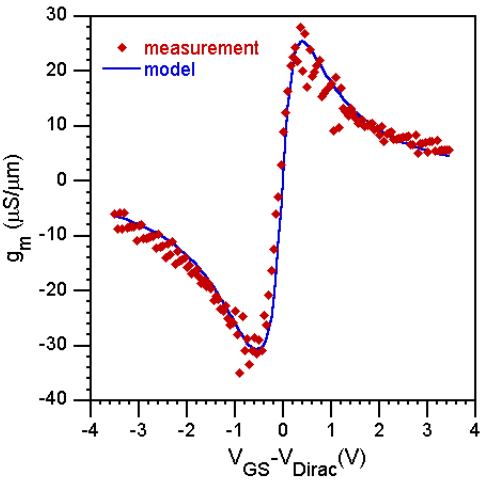

Fig. 7. Model (solid line) versus measured data (♦) for the transconductance (V_{Dirac} = 1 V, V_{DS} = 0.1 V).

sweeping the gate bias voltage and superimposing a low frequency (10 MHz) signal to the gate, and measuring the power spectrum at the drain. Harmonic balance analysis is used to simulate the power spectrum using the model. Fig. 10 demonstrates a good agreement between the simulated and measured power spectrum up to the third harmonic. Also, as can be seen from the first harmonic, there is no power gain in this G-FET.

V. Design Example

Here, we show how the model can be used for designing and analyzing a G-FET based circuit. Fig. 11 shows the circuit schematic of a subharmonic resistive G-FET mixer [7]. The input-signal frequencies are 2 GHz (f_{RF}) and 1.01 GHz (f_{LO}) and the desired output-signal frequency ($f_{IF} = |f_{RF} - 2 \times f_{LO}|$) is 20 MHz. By running a harmonic balance load-pull simulation, the optimum RF and IF embedding impedances for a given LO power, P_{LO} can be found. Fig. 12 depicts contour plots showing simulated conversion loss (CL) for RF and IF

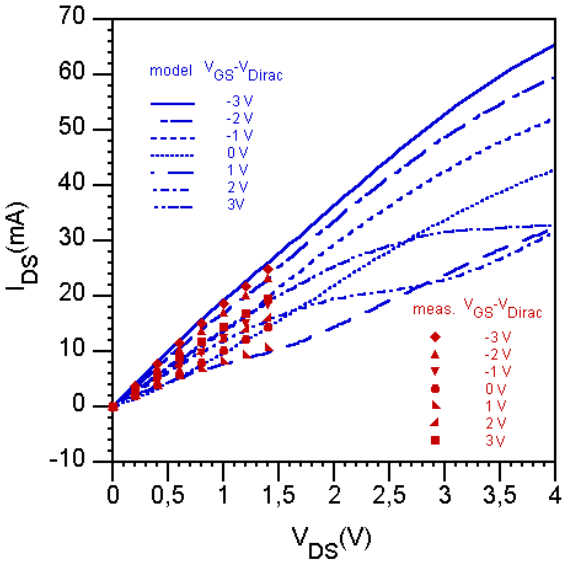

Fig. 8. Model (solid line) versus measured data (⧫) for $I_{DS} - V_{DS}$ characteristic curves at $V_{GS} - V_{Dirac}$ =-3 to 3 volts. The measurement is based on the pulsed-IV method.

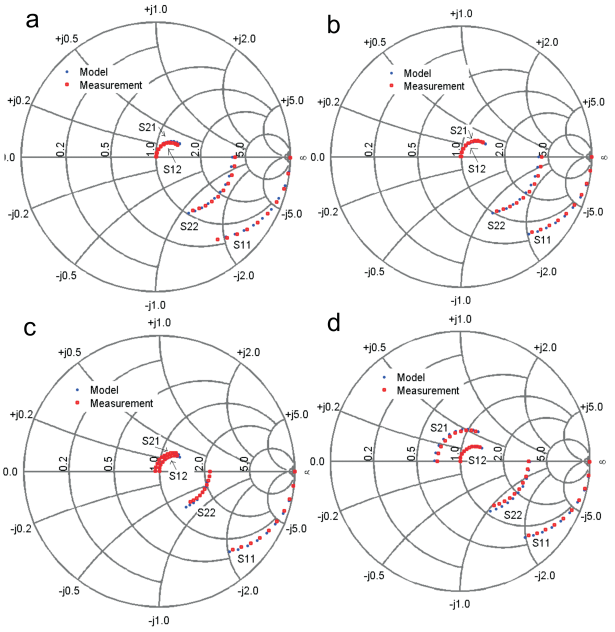

Fig. 9. S-parameters Model (•) versus measurement (○), a) V_{GS} = 1 V , V_{DS} = 0.1 V, g_m = 0, b) V_{GS} = 1.22 V , V_{DS} = 0.5 V, g_m = 0 c) V_{GS} = 1.5 V , V_{DS} = 0.1 V, g_m = 27 $\mu S/\mu m$, d) V_{GS} = 1.75 V , V_{DS} = 0.5 V, g_m = 137 $\mu S/\mu m$

impedance levels at P_{LO} = 15 dBm. The plot is achieved by the following steps. First, the global optimum embedding impedances are estimated by sweeping one impedance (e.g. Z_{RF}) in the Γ-plane while keeping the other impedance (e.g. Z_{IF}) at Z_0 = 50 Ω. Then, $Z_{RF,opt}$ ($Z_{IF,opt}$) is obtained by sweeping Z_{RF} (Z_{IF}) in the Γ-plane with Z_{IF} (Z_{RF}) kept at the estimated global optimum value. Fig. 13 shows $Z_{RF,opt}$, $Z_{IF,opt}$, the simulated and measured mixer CL versus P_{LO}. There is a good agreement between the measured and simulated CL. The optimum impedances are located near the

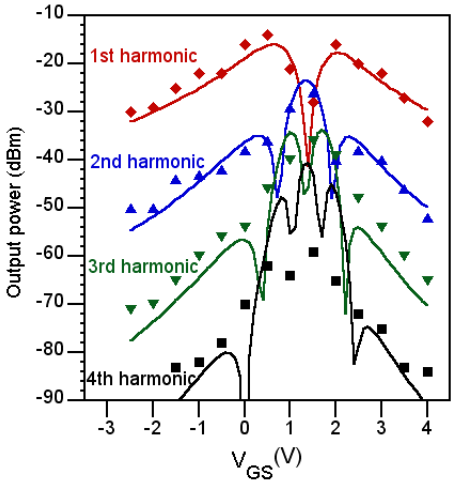

Fig. 10. Model (solid line) and measured power spectrum. f_{in} = 10 MHz, P_{in} = 0 dBm, V_{DS} = 0.5 V.

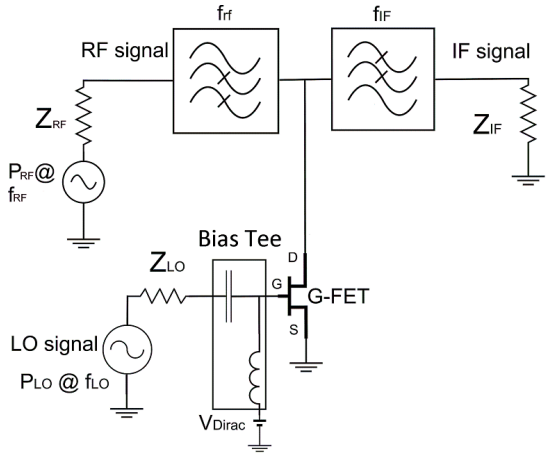

Fig. 11. A subharmonic G-FET mixer circuit [7].

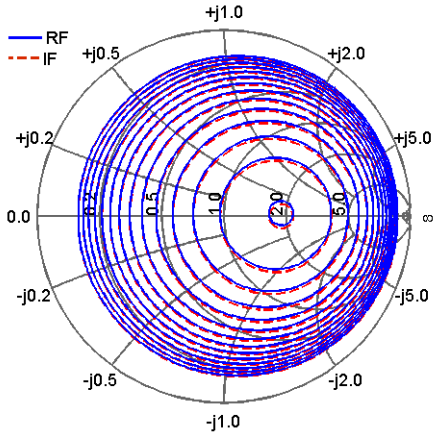

Fig. 12. Simulated CL contour plots for RF and IF embedding impedances. The inner contour is for 22.8 dB CL and the outer contour is for 30 dB CL (0.5-dB step), P_{LO} = 15 dBm and, Z_{LO} and all other mixing terms are terminated with Z_0 (V_{GS} = V_{Dirac} = 1 V).

real axis of the Γ-plane, therefore the real values are plotted. The optimum RF and IF embedding impedances essentially

coincide and it is due to the low RF frequency. It can be seen that by using the optimum embedding impedances at low P_{LO} levels, a lower CL can be reached. Also, it is seen that at high P_{LO}, the CL starts to increase. This is because at high P_{LO}, the time duration of 'off state' becomes much shorter than that of 'on state'. In conventional subharmonic FET mixers, the device can be biased such that the time duration of the 'on state' and 'off state' becomes close together, and consequently the mixer CL monotonically decreases by increasing P_{LO} and saturates [35], [36]. The demonstrated mixer exhibits a high CL which is attributed to the low on-off current ratio ($\simeq$ 3) of the G-FET. Further simulation shows that by utilizing a G-FET with a on-off ratio of 10-20 in the mixer, a CL of 15-17 dB is achievable [37]. A higher on-off ratio can be obtained by reducing the contact resistance levels as well as creating a bandgap in the G-FET channel [38].

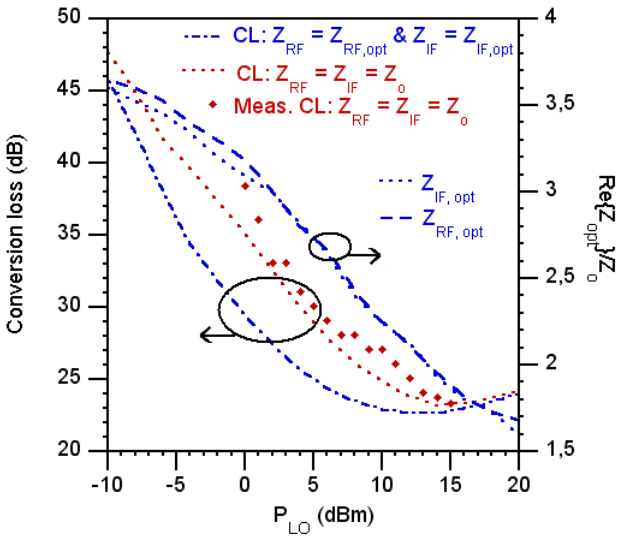

Fig. 13. Simulated and measured CL, as well as the optimum embedding impedances versus P_{LO} (Z_{LO} = Z_0). The measured data is compensated for filter losses and the device parameters are the same as those in table I (V_{GS} = V_{Dirac} = 1 V).

VI. Conclusion

We have proposed and evaluated a closed form large signal model for the G-FETs. The model is semiempirical and is derived for a single layer zero-bandgap graphene. The model accepts different carrier mobilities for electrons and holes and it can predict the asymmetric transfer characteristic of a G-FET. Using a semiempirical approach reduces the complexity of the calculations and enables us to have an analytical model suitable for circuit-level simulations. The model has few fitting parameters which can straightforwardly be extracted using a novel method. This new extraction method gives a more accurate estimation of the drain and source contact resistances than previously reported methods. The model is experimentally verified at DC and RF. The DC measurements agree well with the model and also the power spectrum analysis shows good agreement up to the 3rd order. As a practical example for the model, a harmonic-balance load pull analysis is performed to extract the optimum embedding impedances of a G-FET subharmonic mixer. In this case the measured and simulated mixer CL are compared, and the simulated result follows the measured data. This example shows how the model can be used to analyse and design G-FET circuits. For future model development, the effect of self-heating should be considered. Moreover, for ultra-thin gate dielectrics, where the effect of the graphene quantum capacitance is no longer negligible, the model should be modified.

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Omid Habibpour (S'08) received the B.S degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2002 and the M.S. degree in electrical engineering from Amirkabir University of technology, Tehran, Iran, in 2004.

He is currently working toward the Ph.D. degree in graphene electronics with the Terahertz and Millimetre Wave Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden.

Josip Vukusic received the diploma and Ph.D. degree in photonics from Chalmers University of Technology, Göteborg, Sweden, in 1997 and 2003, respectively.

Since 2004, he has been with the Terahertz and Millimetre Wave Laboratory working on terahertz (THz) technology. His is currently involved in modeling, fabrication, and characterization of frequency multipliers and photomixers for THz generation.

Jan Stake (S'95- M'00 - SM'06) was born in Uddevalla, Sweden, in 1971. He received the M.Sc. degree in electrical engineering and the Ph.D. degree in microwave electronics from Chalmers University of Technology, Göteborg, Sweden, in 1994 and 1999, respectively.

In 1997 he was a Research Assistant at the University of Virginia, Charlottesville, USA. From 1999 to 2001, he was a Research Fellow in the millimetre wave group at the Rutherford Appleton Laboratory, UK. He then joined Saab Combitech Systems AB as a Senior RF/microwave Engineer until 2003. From 2000 to 2006, he held different academic positions at Chalmers and was also Head of the Nanofabrication Laboratory at MC2 between 2003 and 2006. During the summer 2007, he was a Visiting Professor in the Submillimeter Wave Advanced Technology (SWAT) group at Caltech/JPL, Pasadena, USA. He is currently Professor and Head of the Terahertz and Millimetre Wave Laboratory at the department of Microtechnology and Nanoscience (MC2), Chalmers, Gteborg, Sweden. His research involves sources and detectors for terahertz frequencies, high frequency semiconductor devices, graphene electronics, terahertz measurement techniques and applications. He is also co-founder of Wasa Millimeter Wave AB.

Prof. Stake serves as Topical Editor for the IEEE Transactions on Terahertz Science ad Technology.