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High Efficiency Radio Frequency Pulse Width Modulation of Class-E Power Amplifiers

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***Abstract*—A new switch mode power amplifier (SMPA) topology particularly suitable for energy efficient amplification of radio frequency pulse width modulation (RF-PWM) signals is derived. It is analytically shown that high efficiency can be maintained over a wide power dynamic range if the imaginary part of the Class-E load impedance is varied along with the duty cycle (pulse width). Using the theory developed, an explicit design procedure is presented that allows practical realization of the proposed topology from the circuit and component specifications. Following the design procedure, and using in-house (Chalmers University) SiC varactor diodes to implement the tunable imaginary load impedance, a 2 GHz 10 W peak output power GaN HEMT circuit demonstrator is realized. RF-PWM input signals for characterization of the prototype PA is generated with a dedicated 65 nm CMOS modulator. The measurements show that a drain efficiency $> 70\%$ can be obtained over an 6.5 dB dynamic range, which verifies the theory presented and demonstrates the feasibility of the proposed PA topology.**

***Index Terms*—Class-E, high efficiency, power amplifiers, pulse width modulation, RF-PWM.**

I. Introduction

THE radio frequency pulse width modulation (RF-PWM) concept was first proposed by Besslich in [1] for linear amplification with highly efficient switch mode power amplifiers (SMPA). The main principle of RF-PWM is to vary the duty cycle (pulse width) of a square wave at each RF period according to the envelope of the signal. The phase information is in this case represented by the timing of the pulses. The resulting pulse train is amplified with an SMPA and a reconstruction filter is used after the PA to remove the spurious products. The spurious products caused by the switched operation occur in the vicinity of the harmonics of the carrier and can therefore easily be removed with a low loss filter [2], [3], [4]. The transmitter architecture is shown in Fig. 1.

A challenge associated with RF-PWM architecture is that conventional SMPAs (e.g. Class-E, Class-D) suffer from severe switching losses when they are used to amplify RF-PWM signals. Thus, in spite of its high potential, no competitive efficiency results have been presented with that architecture so far. Tom *et al.* [5] studied the efficiency performance of RF-PWM driven Class-E PAs. Although the simulated peak efficiency of the (almost) ideal Class-E is 80%, the average efficiency is 45% with an 8 dB peak to average power ratio (PAPR) Rayleigh distributed envelope signal. It is concluded that the main loss source is caused by non-zero voltage switching, in other words by capacitive losses ($0.5CV^2$) at the switching instances due to dynamic duty cycles. In [6], an RF-PWM transmitter is implemented in 65 nm CMOS technology and measurement results are presented. The drain efficiency of the SMPA (Class-E) is 38% at the peak output power, while it decreases to 12% at 10 dB back-off with a nearly constant slope. Wagh *et al.* [7] constructed a prototype 100 MHz pHEMT Class-D PA and studied the performance with RF-PWM signals as the input. The Class-D PA provides 60% of peak efficiency at 50% duty cycle. The efficiency however decreases to 48% at 25% duty cycle. The measured output power dynamic range with the mentioned duty cycle range is 3 dB.

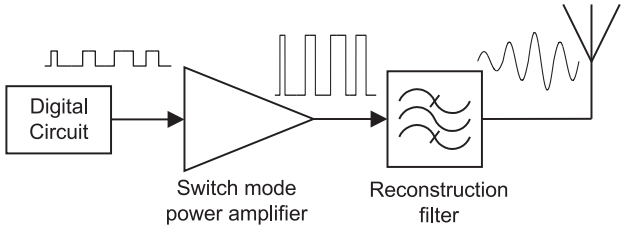

Fig. 1. Block diagram of RF pulse width modulation based transmitter architecture

Clearly, novel SMPA topologies must be studied in order to successfully utilize the potential of the RF-PWM architecture for high efficiency linear amplification of modulated signals. In this paper we derive a new PA topology that is suitable for efficient amplification of RF-PWM signals. It will be analytically derived that a Class-E PA with tunable imaginary load impedance can provide sub-optimal Class-E operation versus the duty cycle. RF-PWM of such a PA will therefore not suffer from any severe switching losses and consequently provide high average efficiency with realistic, modulated signals.

A systematic design procedure is a very convenient tool for hardware development. Using the theory developed, we therefore outline an explicit, non-iterative, design procedure that allows realization of the proposed PA from the circuit and component specifications. Following the design procedure, a circuit demonstrator is implemented to verify the theory and

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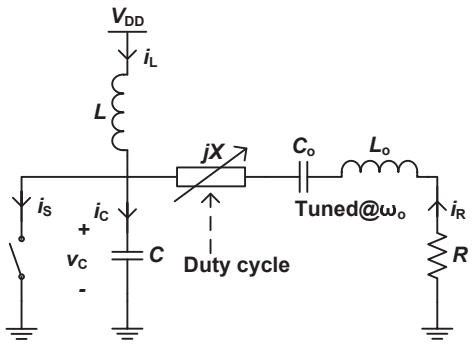


Fig. 2. Class-E power amplifier with tunable X for high efficiency RF pulse width modulation.

the feasibility of the PA topology.

The outline of the paper is as follows. In Section II the suggested PA topology and its operation principles are introduced. Section III treats the theory behind the operation. In Section IV the design procedure is outlined. In Section V design of the circuit demonstrator is treated and the measurement results are presented in Section VI. Finally, the most important findings are summarized in Section VII.

II. Efficient RF Pulse Width Modulated Class-E PA

A Class-E PA is a single ended SMPA, see Fig. 2, where the load network is designed to satisfy two switching conditions:

$$v_C\left(\frac{2\pi}{\omega_0}\right) = 0, \tag{1}$$

$$\frac{dv_C(t)}{dt}\Big|_{t=\frac{2\pi}{\omega_0}} = 0 \tag{2}$$

where $v_C(t)$ is the voltage across the capacitor C shown in Fig. 2. The condition given in (1) is named zero voltage switching (ZVS) and the condition given in (2) is named zero voltage derivative switching (ZVDS). The first condition is required to prevent losses due to discharge of the capacitor C at off-to-on switching instances, while the latter is meant to avoid high current through an unsaturated transistor during the off-to-on transitions [8].

The components of the Class-E are optimized at a fixed duty cycle. If the duty cycle is varied from the nominal value, the switching conditions are violated and the losses increase. A possible way to preserve the switching conditions is therefore to have electronically tunable components in the load network. Singhal $et\ al.$ [9] analytically proved that ZVS and ZVDS switching conditions can be preserved if the $\{C, R\}$ components of a parallel circuit Class-E[1] PA are modulated along with the duty cycle. For Class-E PAs, both switching conditions (1) and (2) can actually be preserved if two of the reactive components of the Class-E, $\{C, X\}$ or $\{L, X\}$, are re-optimized as the duty cycle is varied. This property can easily be seen by studying the design equations of Class-E PAs, e.g. the ones given in [10]. However, in a practical implementation it is highly desirable to have only one tunable component in the load network for minimized complexity. The options are therefore to vary either L, C or X. Tunable inductors are not practical, which immediately excludes L. Tuning of the capacitance C is not practical neither, since the tuning range will be limited by the output capacitance of the transistor. X is therefore selected as the tunable element. Moreover, having a tunable component in series with the tuned filter seen in Fig. 2 may also help for frequency re-configurability, since it allows the filter center frequency to be tuned.

As will be proved in Section IV, it is only possible to preserve one of the Class-E switching conditions (1) and (2) when there is one variable component in the load network. Earlier publications clearly prove the importance of the ZVS condition (1) over the ZVDS condition (2) for low switching losses [11], [12]. Therefore we prefer to preserve the ZVS condition. This mode of operation is called sub-optimum Class-E[2] and the corresponding design equations for this mode are required in order to calculate the X values versus duty cycle.

Raab derived the design equations for sub-optimum Class-E PAs with an RF-choke at the power supply at arbitrary duty cycle in [11]. However, the Class-E with RF-choke results in a lower maximum operating frequency and has a much lower design flexibility compared to the Class-E with finite feed inductance [10]. Later, Acar $et\ al.$ derived the design equations for sub-optimum Class-E PAs with finite feed only at 50% duty cycle in [12]. In this work, however, we derive the design equations for sub-optimum Class-E PAs with finite feed at arbitrary duty cycle. The results will be used as a basis for the circuit design procedure in Section IV.

III. Theory

In this section the design equations for sub-optimum Class-E PAs at arbitrary duty cycle will be derived. First, the definitions and assumptions made in the circuit analysis are given.

A. Definitions and Assumptions

The switching conditions of the sub-optimum Class-E can be defined as [12]:

$$v_C\left(\frac{2\pi}{\omega_0}\right) = 0, \tag{3}$$

$$\frac{dv_C(t)}{dt}\Big|_{t=\frac{2\pi}{\omega_0}} = k\omega_o V_{DD} \tag{4}$$

where $k\omega_o V_{DD}$ is equal to the slope of $v_C(t)$ at off-to-on switching instances. Notice that $k = 0$ corresponds to conventional Class-E operation. However, for sub-optimum Class-E PAs, k is a free design variable and can be any real number.

A number of assumptions is made in the circuit analysis:

- The switch is loss-less with zero on resistance and infinite off resistance.

[1]The schematic of parallel circuit Class-E is the same as the schematic given in Fig. 2 except that X is replaced with a short circuit.

[2]Term *variable-slope* Class-E PA is also used in the literature for this mode, e.g. in [12].

- The loaded quality factor ($Q_L = \omega_o L_o/R$) of the tuned filter is high enough, such that the current through the load is a pure sinusoid at the carrier frequency.
- The only power dissipation in the circuit occurs in the load resistance R, the DC power is therefore converted to RF power with 100% efficiency.

We define the switch function as

$$S = \begin{cases} \text{on} & 0 < t \leq d\frac{2\pi}{\omega_0} \\ \text{off} & d\frac{2\pi}{\omega_0} < t \leq \frac{2\pi}{\omega_0} \end{cases}$$

e.g. $d = 1$ corresponds to 100% duty cycle.

B. Circuit Analysis

1) On state of the switch: In the time interval $0 < t < d\frac{2\pi}{\omega_o}$ the switch is on, therefore $i_C = 0$ and $v_C = 0$. The switch current will then be given by

$$i_S(t) = i_L(t) + i_R(t) \tag{5}$$

where, according to the sinusoidal load current assumption, we define $i_R(t)$ as

$$i_R(t) = I_R \sin(\omega_o t + \phi). \tag{6}$$

The current $i_L(t)$ in (5) is given by

$$i_L(t) = \frac{1}{L}\int_0^t V_{DD} d\tau + i_L(0) = \frac{V_{DD}}{L}t + i_L(0) \tag{7}$$

and $i_L(0)$ is known from the boundary condition given in (4) as

$$i_L(0) = i_C(0) - i_S(0) = C\omega_o V_{DD} k - I_R \sin\phi. \tag{8}$$

Substituting (7) into (5) yields

$$i_S(t) = \frac{V_{DD}}{L}t + C\omega_o V_{DD} k - I_R \sin\phi + I_R \sin(\omega_o t + \phi). \tag{9}$$

2) Off state of the switch: In the time interval $d\frac{2\pi}{\omega_o} < t < \frac{2\pi}{\omega_o}$ the switch is off and the currents through L and R will combine into C as

$$\begin{aligned} i_C(t) &= i_L(t) + i_R(t) \\ &= \frac{1}{L}\int_{\frac{d2\pi}{\omega_o}}^{t} \big(V_{DD} - v_C(t)\big)dt + i_L(d\frac{2\pi}{\omega_o}) + i_R(t). \end{aligned} \tag{10}$$

By taking the time-derivative of (10), the following second order linear non-homogenous differential equation is obtained:

$$LC\frac{d^2 v_C(t)}{dt^2} + v_C(t) - V_{DD} - \omega_o L I_R \cos(\omega_o t + \phi) = 0. \tag{11}$$

Solution of (11) follows as

$$\begin{aligned} v_C(t) =& C_1 \cos(q\omega_o t) + C_2 \sin(q\omega_o t) + V_{DD} \\ &+ V_{DD}\frac{q^2}{q^2-1}\rho\cos(\omega_o t + \phi) \end{aligned} \tag{12}$$

where

$$q = 1/(\omega_o\sqrt{LC}), \tag{13}$$

$$\rho = \omega_o L I_R / V_{DD}. \tag{14}$$

TABLE I
ELEMENTS OF THE DESIGN SET K

$K_L = \frac{\omega_o L}{R}$,	$K_C = \omega_o C R$,	$K_X = \frac{X}{R}$,	$K_P = \frac{P_{out} R}{V_{DD}^2}$

Two boundary conditions are required to solve for the coefficients C_1 and C_2. These can be found by examining $v_C(t)$ and $i_L(t)$ at the on-to-off switching instances, which yields:

$$\begin{aligned} v_C\left(d\frac{2\pi}{\omega_o}\right) &= 0, \\ i_C\left(d\frac{2\pi}{\omega_o}\right) &= i_L\left(d\frac{2\pi}{\omega_o}\right) + I_R \sin(d2\pi + \phi). \end{aligned}$$

The resulting expressions for C_1 and C_2 are given in the Appendix.

The expression for $v_C(t)$ must also satisfy the switching conditions given in (3) and (4) for proper operation of the circuit. Substitution of the switching conditions in (12), yields two relations for ρ, ϕ, d, q and k, which can be arranged as:

$$a_1(d,q,k) + \rho\big(b_1(d,q,k)\cos\phi + c_1(d,q,k)\sin\phi\big) = 0 \tag{15}$$

$$a_2(d,q,k) + \rho\big(b_2(d,q,k)\cos\phi + c_2(d,q,k)\sin\phi\big) = 0 \tag{16}$$

where the expressions for $\{a_{1,2}(d,q,k),\ b_{1,2}(d,q,k),\ c_{1,2}(d,q,k)\}$ are given in the Appendix. It is important to note that these functions are only dependent on (d,q,k).

Next, the circuit design equations will be derived using the relations in (15) and (16).

C. Derivation of the Design Equations

The derivation of the design equations will be made using a design-set, $K = \{K_L, K_C, K_X, K_P\}$, which was first defined in [12]. The elements of K are related to the circuit element values using the expressions in Table I. The elements of K will be derived in terms of (d,q,k), hence, depending on the selected combination of (d,q,k), infinitely many sub-optimum Class-E circuit realizations can be found using K. By definition, d can take any value in the range [0,1], q can be any real positive number and k can be any real number.

The derivation of $\{K_L, K_C, K_P, K_X\}$ is straightforward as follows.

K_L: This element can be derived from the following relation, which is based on the fact that the DC power is converted into RF power with 100% efficiency:

$$I_o V_{DD} = \frac{I_R^2}{2}R \tag{17}$$

where I_o is the average current through the DC voltage source. This can be written as

$$\begin{aligned} I_0 &= \frac{\omega_o}{2\pi}\int_0^{2\pi/\omega_o} i_S(t)dt \\ &= \frac{V_{DD}\Big(\pi d\big(\pi d + \frac{k}{q^2} - \rho\sin(\phi)\big) + \rho\sin(\pi d)\sin(\pi d + \phi)\Big)}{\pi L \omega_o}. \end{aligned} \tag{18}$$

Substitution of (18) into (17) yields

$$K_L = \frac{\frac{\pi}{2}\rho^2}{\pi d\big(\pi d + \frac{k}{q^2} - \rho\sin(\phi)\big) + \rho\sin(\pi d)\sin(\pi d + \phi)}. \quad (19)$$

If ρ and ϕ are solved in terms of (d, q, k) from (15) and (16), the derivation of $K_L(d, q, k)$ is completed, where the solutions follow as

$$\rho = \frac{a_1(d,q,k)\sqrt{m^2+1}}{b_1(d,q,k) + c_1(d,q,k)m}, \quad (20)$$

$$\phi = \arctan(m) \quad (21)$$

where ϕ is in the same quadrant as the point $(-1, -m)$ and

$$m = \frac{a_1(d,q,k)b_2(d,q,k) - a_2(d,q,k)b_1(d,q,k)}{a_2(d,q,k)c_1(d,q,k) - a_1(d,q,k)c_2(d,q,k)}.$$

K_C: Derivation of K_C is straightforward and follows from the definition of q, as

$$K_C(d,q,k) = \frac{1}{q^2 K_L(d,q,k)} \quad (22)$$

K_X: The expression for K_X can be derived using two quadrature Fourier components of $v_C(t)$, as

$$K_X(d,q,k) = \frac{V_X}{V_R} \quad (23)$$

where

$$V_R = \frac{\omega_o}{\pi}\int_0^{2\pi/\omega_o} v_C(t)\sin(\omega_o t + \phi)dt,$$

$$V_X = \frac{\omega_o}{\pi}\int_0^{2\pi/\omega_o} v_C(t)\cos(\omega_o t + \phi)dt.$$

Expressions for V_R and V_X are given in the Appendix, where both of them are dependent only on (d, q, k).

K_P: This element can easily be derived by substituting $I_R = \sqrt{2P_{out}/R}$ into (14), as

$$K_P(d,q,k) = \frac{\rho^2}{2K_L(d,q,k)^2}. \quad (24)$$

All the elements of $K(d, q, k)$ now have been derived. Next, a circuit design procedure is outlined based on the derived design set.

IV. Systematic Design Procedure

In this section we present an explicit, non-iterative design procedure for the design of a variable duty-cycle sub-optimum Class-E PA, based on the design-set K derived in the preceding section.

As discussed in Section II, only X is a tunable component in the topology. If C and L are constant, the design variable k has a relation to the duty cycle d, i.e. $k = k(d)$. The design equations then follow as

$$C = \frac{1}{\omega_o R}K_C\big(d, q, k(d)\big), \quad (25)$$

$$L = \frac{1}{q^2\omega_o^2 C}, \quad (26)$$

$$X(d) = RK_X\big(d, q, k(d)\big), \quad (27)$$

$$P_{out}(d) = \frac{V_{DD}^2}{R}K_P\big(d, q, k(d)\big). \quad (28)$$

Once the free design variables $\big(q, k(d)\big)$ and the load resistance R are determined, all the remaining circuit element values can be calculated.

A. Circuit Optimization

The variables $\big(q, k(d)\big)$ and R will be optimized to meet the following design considerations:

- The resulting maximum value of the switch current (i_{max}) must be equal to the maximum current capability of the transistor (I_{max}) in order to utilize the device fully.
- The capacitance C will be set equal to the transistor output capacitance (C_{out}). This will result in a low loss load network and minimum circuit complexity. Furthermore, C is limiting the maximum operating frequency of the amplifier. We therefore do not want to increase C above the value of the output capacitance of the transistor
- The X-variation should be limited to the tuning factor ($\Delta X = X_{max}/X_{min}$) of the varactors used.

These design considerations can mathematically be expressed as:

$$\frac{R}{V_{DD}}i_{max}\big(d_u, q, k(d_u)\big) - \frac{I_{max}}{V_{DD}}R = 0, \quad (29)$$

$$\frac{V_{DD}}{R}\frac{K_C\big(d_u, q, k(d_u)\big)}{i_{max}\big(d_u, q, k(d_u)\big)} - \omega_o C_{out}\frac{V_{DD}}{I_{max}} = 0, \quad (30)$$

$$\frac{K_X\big(d_l, q, k(d_l)\big)}{K_X\big(d_u, q, k(d_u)\big)} - \Delta X = 0 \quad (31)$$

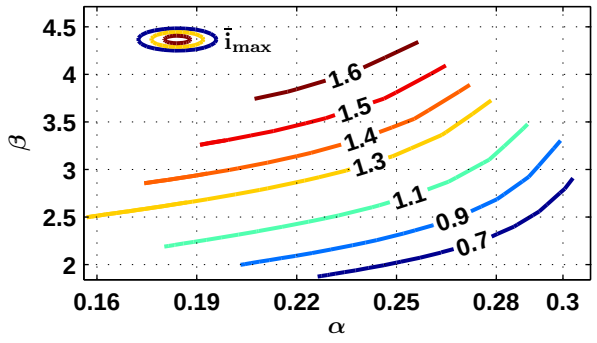
where d_l and d_u represent the lower and upper limits of $d \in [d_l, d_u]$ and the unknown $k(d_l)$ is related to $(q, k(d_u))$ via the following equality based on (25):

$$K_C\big(d_l, q, k(d_l)\big) = K_C\big(d_u, q, k(d_u)\big). \quad (32)$$

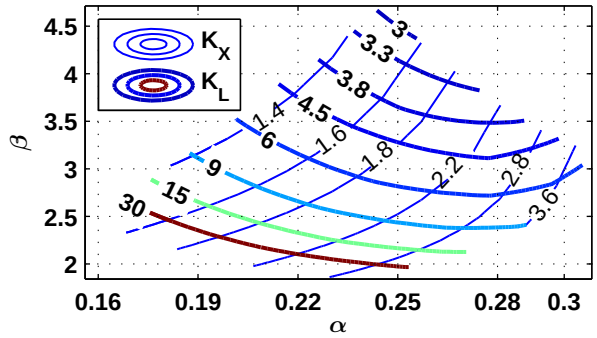
For convenience the first terms in (29)-(31) will be noted as $\bar{i}_{max}\big(q, k(d_u)\big)$, $\alpha\big(q, k(d_u)\big)$ and $\beta\big(q, k(d_u)\big)$, respectively.

The free design variables $\big(q, k(d_u)\big)$ and R can numerically be solved from (29)-(31) if the transistor and varactor specifications are known. All circuit elements are then known through (25)-(27).

In order to have an easy to use design procedure, we have generated contour plots of $\bar{i}_{max}\big(q, k(d_u)\big)$, $K_X\big(d_u, q, k(d_u)\big)$ and $K_L\big(d, q, k(d)\big)$ versus $\{\alpha\big(q, k(d_u)\big), \beta\big(q, k(d_u)\big)\}$ over $q \in [0, 1]$ and $k(d_u) \in [-1.5, -0.5]$, see Fig. 3. These plots contain all information required for practical circuit design for a given duty cycle range $d \in [d_l, d_u]$. The plots presented here have therefore been generated with $d_u = 0.5$, corresponding to maximum Class-E transistor utilization [11]. The lower limit



(a)



(b)

Fig. 3. Plots for the circuit optimization, all versus $\{\alpha(q,k(d_u)),\beta(q,k(d_u))\}$: (a) Normalized maximum switch current, $\bar{i}_{max}(q,k(d_u))$ in (29). (b) $K_X(d_u,q,k(d_u))$ and $K_L(d,q,k(d))$.

d_l is set to 0.3 and set by the minimum pulse width of the available RF-PWM generator used in the prototype transmitter in Section V.

Next, the calculation of the circuit element values are described step by step.

B. Design Steps

1) Drain Bias: The maximum value of the drain voltage (v_{max}) is bounded to $[3.2, 3.3]V_{DD}$ for the $(q,k(d_u))$ ranges used here. The V_{DD} can consequently be formulated as $V_{DD} = 0.3V_{BR}$ with a very slight error, where V_{BR} is the drain to source breakdown voltage of the transistor.

2) Load Resistance: By using given I_{max}, C_{out} and ΔX specifications, α and β may be calculated using (30) and (31), respectively. Fig. 3a then gives the corresponding value of $\bar{i}_{max}$. The load resistance may then be calculated using (29).

3) Reactive Circuit Elements: $K_X(d_u,q,k(d_u))$ and $K_L(d,q,k(d))$ are obtained from Fig. 3b. $X(d_u)$ and L may then be calculated using the expressions in Table I. Finally, $X(d_l)$ is given by $X(d_l) = \beta(q,k(d_u))X(d_u)$.

Implementation of the steps above quantifies all circuit elements of the circuit in Fig. 2. Although the $X(d)$ will only be known at d_l and d_u, it will have a rather linear dependence within the d range.

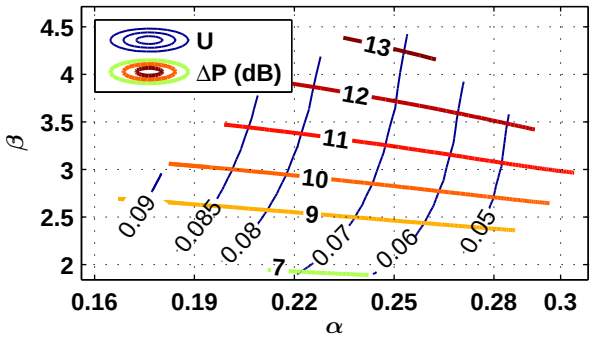


Fig. 4. Performance figure of merits: Transistor utilization factor, $U(q,k(d_u))$ and power dynamic range, $\Delta P(q,k(d_u))$ versus $\{\alpha(q,k(d_u)),\beta(q,k(d_u))\}$.

C. Performance Figure of Merits

Clearly, the peak output power (P_{peak}) achieved from a certain transistor is a performance indicator for a PA design. The transistor utilization factor at d_u, $U(q,k(d_u))$, is plotted in Fig. 4, which is enough to determine P_{peak}:

$$P_{peak} = U(q,k(d_u))I_{max}V_{BR}. \tag{33}$$

Another performance indicator is the achieved power dynamic range with $d \in [d_l, d_u]$, which follow as:

$$\Delta P(q,k(d_u)) = \frac{K_P(d_u,q,k_{d_u})}{K_P(d_l,q,k_{d_l})}. \tag{34}$$

$\Delta P(q,k(d_u))$ is plotted in Fig. 4 using $d_l = 0.3$ and $d_u = 0.5$. Observe that ΔP increases with $\beta(q,k(d_u))$, which is equal to the large-signal tuning factor of the varactor diode. This proves that the achievable power dynamic range is not only dependent on d range with this topology but also dependent on the characteristics of the varactor diode used.

An explicit, non-iterative design procedure has been developed so far. In the next section, the procedure will be applied in a practical design.

V. Prototype Transmitter Design

In this section a prototype 2 GHz RF-PWM transmitter is designed and manufactured. RF-PWM signals are generated with a modulator implemented in a commercial 65 nm CMOS technology. The RF-PWM signals are amplified with a tunable imaginary load impedance GaN HEMT (*Cree* CGH60015DE) Class-E PA. The high power tunable load network is facilitated using in-house high breakdown voltage SiC varactors [13].

A. RF Pulse Width Modulator

A single stage inverter circuit implemented in a commercial 65 nm CMOS process is used as modulator. The schematic of the modulator is shown in Fig. 5. The inverter generates variable duty cycle signals by varying the PMOS and NMOS transistor gate bias voltages, V_{gP} and V_{gN} respectively [14], [15]. The modulator use extended drain MOS (EDMOS) transistors which have breakdown voltage of 10 V [16]. The modulator can therefore provide the required voltage swing to

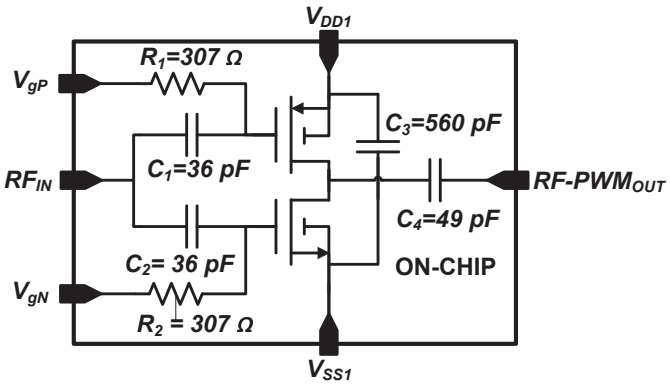


Fig. 5. Schematic of the CMOS RF pulse width modulator.

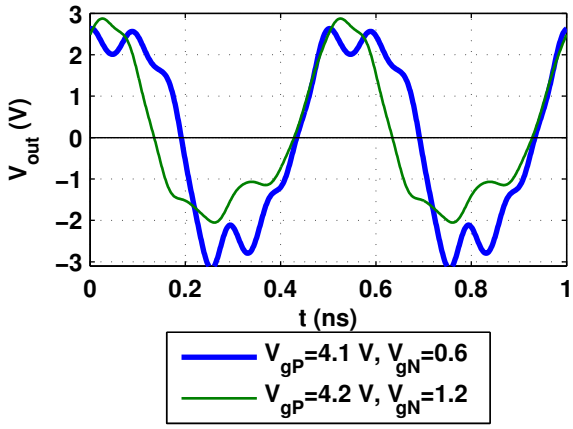


Fig. 6. The measured time domain output waveforms of the RF pulse width modulator.

switch the GaN transistor between on and off states. Typically 5 V of peak-to-peak voltage swing is sufficient to drive the GaN between on and off.

An active load-pull setup is used to test the performance of the modulator under realistic loading conditions at 2 GHz [17]. The input capacitance of the GaN HEMT ($C_{gs} = 5$ pF), is emulated as the load to the modulator for the fundamental frequency (ω_o) and the second harmonic frequency ($2\omega_o$). Higher order harmonics are not controlled and terminated with approximately 50 Ω. The measured time domain waveforms are shown in Fig. 6. The measurement results show that the duty cycle can be varied approximately from 50% to 30% by an appropriate control of the V_{gP} and V_{gN} CMOS voltages. The voltage swing is above 5 V and slightly below 5 V for 50% and 30% duty cycles, respectively.

In the transmitter, the RF input port of the modulator, RF_{in} in Fig. 5, is directly connected to an RF synthesizer with no input matching in between. The output of the modulator is connected to the gate of the GaN HEMT using very short bond wires, see Fig. 7. This ensures that square shaped signals can be generated across the gate of the GaN at RF frequencies. The output of the modulator is DC decoupled which allows the gate of the GaN HEMT to be biased near its pinch off voltage at -3 V. The biasing is implemented with an L-C network connected to the gate of the GaN HEMT with a relatively

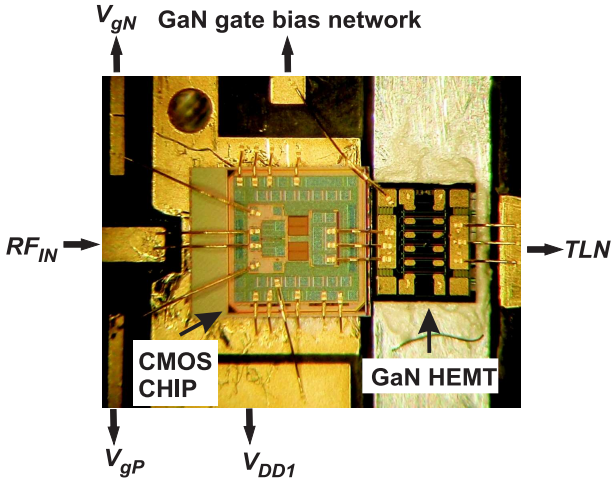


Fig. 7. CMOS RF pulse width modulator and GaN HEMT line up. Drain terminal of the GaN HEMT is connected to a tunable load network (TLN).

TABLE II
SUMMARY OF THE CIRCUIT DESIGN.

$V_{DD} = 30$ V	$R = 21\Omega$	$L = 9$ nH
$C = 1.2$ pF	$X(50\%) = 34\ \Omega$	$X(30\%) = 101\ \Omega$
$P_{peak} = 15$ W	DR = 10 dB	

long bond wire. The GaN HEMT device functions as the active switch in the tunable imaginary load impedance Class-E stage, which is subject of the following section.

B. Tunable Imaginary Load Impedance Class-E PA

The design of the PA shown in Fig. 2 requires the ideal component values and the drain bias, $\{L, C, R, X(d), V_{DD}\}$ to be calculated. The component values are easily calculated via the design procedure outlined in Section IV using the specifications of the transistor and the varactor diode. The junction capacitance and the series resistance of the SiC varactor, C_j and R_s respectively, are plotted versus bias in Fig. 8. Considering the possible high RF voltage swing across the varactors, the useable impedance tuning factor is taken as $\Delta X = 3$. The transistor specifications are: $I_{max} = 2$ A, $V_{BR} = 100$ V and $C_{out} = 1.2$ pF.

The final design values, which are found by implementing the design procedure outlined in Section IV.B, are summarized in Table II. The designed circuit is simulated via the harmonic balance method using a switch with finite on/off resistances and an ideal tunable capacitor. The resulting switch waveforms are shown in Fig. 9. Observe that the switch voltage, $v_C(t)$, is always zero at off-to-on switching instances. Thus, ideal efficiency of the sub-optimum Class-E (100%) is preserved for a duty cycle range of 30%-50%. This range yields a power dynamic range of $\Delta P = 10$ dB.

Next step is the implementation of the designed load network with realistic components. The load network of the Class-E is realized by providing the required drain impedances at the carrier frequency and at harmonics of the carrier with a transmission-line based network [8]. Simulations show that the

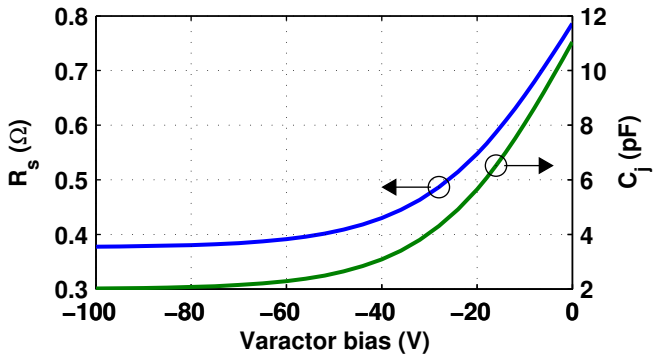


Fig. 8. Intrinsic series resistance (R_s) and junction capacitance (C_j) of the SiC varactor die versus the bias voltage.

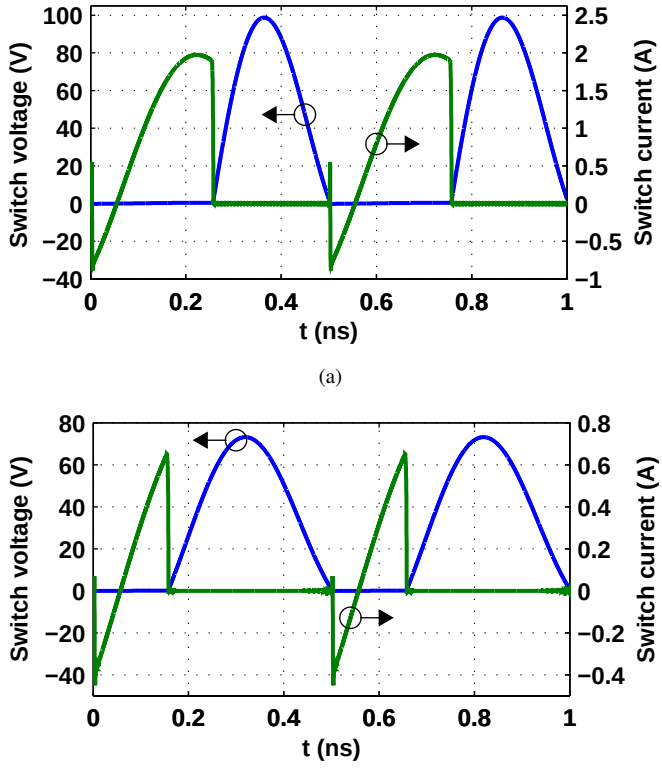


Fig. 9. Simulated switch waveforms: (a) The duty cycle is 50% and $X = 34\ \Omega$ (b) The duty cycle is 30% and $X = 101\ \Omega$.

fundamental (ω_o) and the second ($2\omega_o$) harmonic impedances have the strongest influence on the performance in terms of efficiency and output power. Higher order ($3\omega_o$, $4\omega_o$, ...) harmonic impedances do not effect the performance considerably, which is also known theoretically [18]. The required drain impedances are provided only for the fundamental and the second harmonic with the load network, which is shown in Fig. 10.

The load network is implemented on 20 mil thick Duroid 5870 ($Rogers\ Corp.$) substrate. The required C value is equal to the output capacitance of the GaN HEMT, thus provided by the device itself. The high Q tuned filter in the load network of Class-E PA implies that the load impedance at $2\omega_o$, (Z_2 in Fig. 10), must be equal to $j2\omega_o L$. TL_2 is equivalent to a short circuit at $2\omega_o$ and TL_1 transforms the short circuit to $j2\omega_o L$. Two anti-series connected SiC varactors are used for impedance tuning [13]. The electrical lengths and the characteristic impedances of the transmission lines $TL_3 - TL_8$ are engineered to ensure that the load impedance at ω_o (Z_1 in Fig. 10) is equal to a parallel connection of impedances $R + jX(d)$ and $j\omega_o L$, as desired (see Fig. 2). The GaN HEMT drain bias network is implemented with a radial stub and a quarter wavelength transmission line. The same topology is also used to bias the varactors. The DC grounds for the varactors are provided via the short circuited stubs TL_4 and TL_7.

C. Cut-Ready Simulation Results

In this section cut-ready simulation results of the transmitter are presented. All simulations use an in-house model for the GaN HEMT die. The model is optimized for switch mode operation and has been verified to give high accuracy for SMPA simulations [19]. A large signal model of the SiC varactor die was developed using multi-bias S-parameter measurements calibrated to the die reference plane. The measured time domain output waveforms of the modulator circuit, see Fig. 6, are directly used as the input drive signal for the Class-E PA during the simulations.

The simulated large signal load impedances at ω_o and $2\omega_o$, Z_1 and Z_2 respectively, are plotted versus varactor control voltage (V_c), see Fig. 11. Note that, Z_1 is equivalent to a parallel connection of impedances $R + jX(d)$ and $j\omega_o L$. The real and imaginary parts of Z_1 are therefore expected to vary according to the design equations, i.e. $Z_1(50\%) = 13 + j28.4\ \Omega$ and $Z_1(30\%) = 6.5 + j56.6\ \Omega$ at 2 GHz, see Table II. After the design optimization $Z_1(50\%) = 14.1 + j25.1\ \Omega$ and $Z_1(30\%) = 12.3 + j48.5\ \Omega$. The discrepancy between the theoretical and the implemented load impedance values is mainly due to non-ideal switching behavior of the transistor, i.e. the non-zero on resistance value and non-zero switching durations, and the non-linear behavior of the device parasitic capacitances. The simulated second harmonic impedance, Z_2, is constant versus the duty cycle as assumed in the theoretical derivation. The Z_2 after the design optimization is equal to $1 + j144\ \Omega$ at 2 GHz while the calculated value from Table II is $j226\ \Omega$.

The simulated drain waveforms are shown in Fig. 12 for the peak output power level and at 7 dB back off. Observe that voltage and current overlap is fairly low for both cases. The simulated drain efficiency is shown in Fig. 13. The efficiency results agree well with the theory, showing that the drain efficiency remains fairly constant at its peak value when the duty cycle and X are modulated simultaneously to control the output power. The simulated drain efficiency is higher than 74% over a 7 dB of dynamic range at 2 GHz carrier frequency. The overall transmitter efficiency simulation results are not included here since no model was available for the modulator circuit. The measured overall transmitter efficiency results are, however, presented in the following section.

Finally, the manufactured modulator board, the GaN HEMT die and the tunable load network are mounted on an aluminium

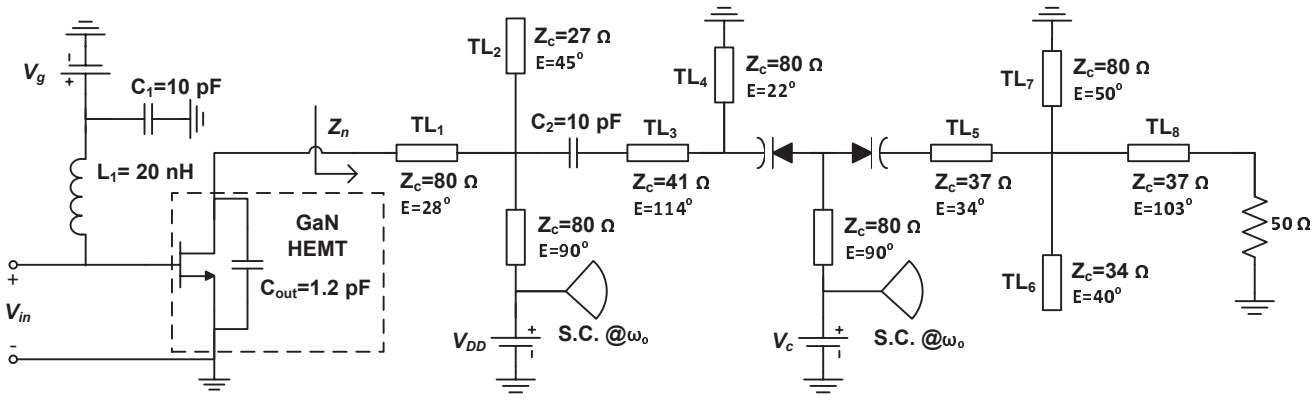


Fig. 10. Class-E PA with electronically tunable load network. Z_n denotes the impedance seen from the indicated reference plane at $n\omega_o$, where n is the harmonic index. The electrical lengths of the transmission lines (E) are specified at 2 GHz.

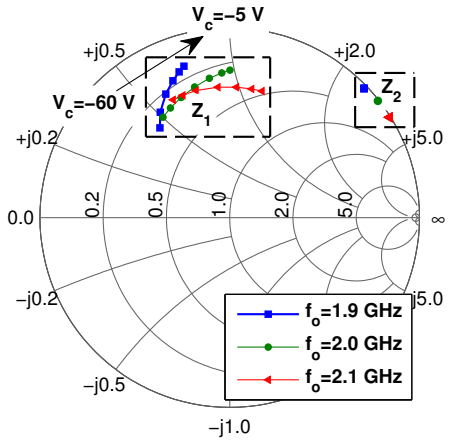


Fig. 11. Simulated large signal load impedance for variable varactor bias voltage at the fundamental frequency (ω_o) and the second harmonic frequency ($2\omega_o$), Z_1 and Z_2 respectively. The varactor control voltage is varied from -60 V to -5 V.

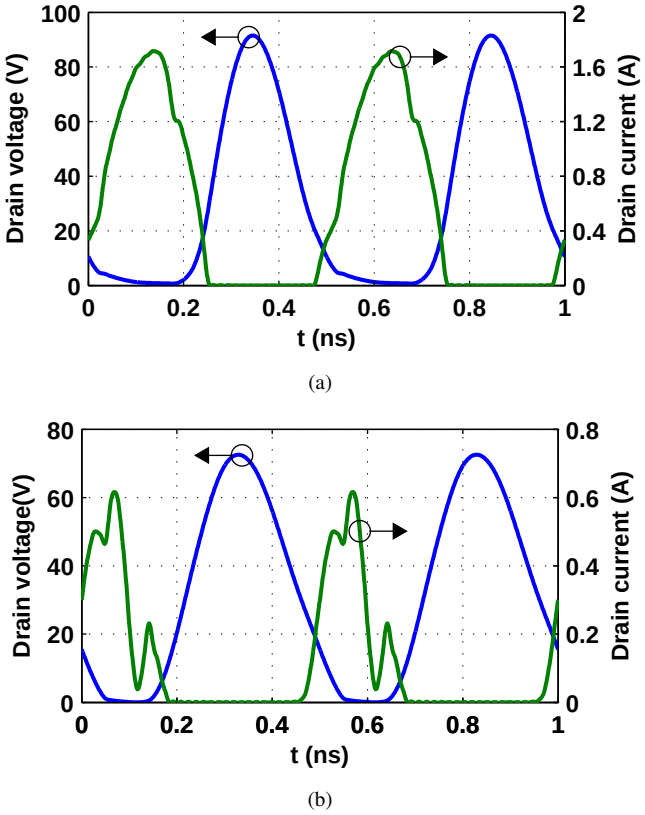


Fig. 12. Simulated drain waveforms from the cut-ready Class-E PA, $V_{DD} = 30$ V, $V_g = -3$ V and $f_o = 2$ GHz : (a) Peak power, 13 W and (b) 7 dB output power back-off

fixture which is also used for overall grounding. A photograph of the prototype transmitter is shown in Fig. 14 (see Fig. 7 for a close up of the CMOS and GaN interconnect).

VI. Experimental Result

In this section static measurement results of the manufactured transmitter are presented. The drain efficiency of the Class-E stage (η) and the overall transmitter efficiency (η_{tot}) are both measured. The efficiency definitions follow as [20]

$$\eta = \frac{P_{out}}{P_{DC1}} \tag{35}$$

$$\eta_{tot} = \frac{P_{out}}{P_{DC1} + P_{DC2} + P_A} \tag{36}$$

where P_{DC1} and P_{DC2} are the DC powers drawn by the Class-E stage and the modulator stages, respectively. P_A is the available RF power from the RF synthesizer applied to the modulator input.

The CMOS drain bias, V_{DD1}, is set to 5 V. The breakdown voltage of the varactors were slightly lower than the expected value. The drain bias of the GaN HEMT, V_{DD}, is therefore decreased from 30 V to 25 V for safe operation of the varactors during the measurements. The gate bias of the GaN HEMT, V_g, is set to -3 V. The duty cycle is controlled by varying the gate bias of the NMOS and PMOS transistors in the modulator circuit, V_{gN} and V_{gP} respectively, see Fig. 5. A look up table is constructed by recording the efficiency from the static measurements by sweeping the V_{gN} and the V_{gP} at each varactor control voltage, V_c. This way the optimum combination of the duty cycle and the load impedance corresponding to the

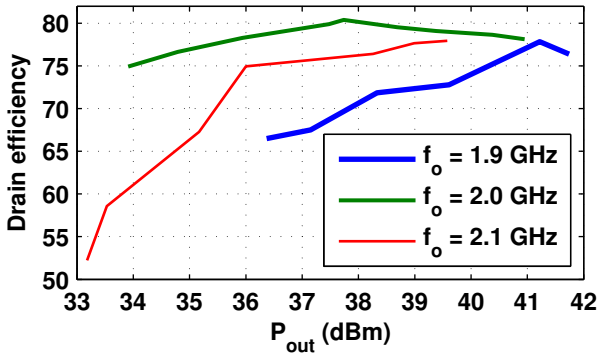


Fig. 13. Simulated drain efficiency, η, of the GaN HEMT Class-E stage versus the output power, P_{out}, $V_{DD} = 30$ V, $V_g = -2.5$ V.

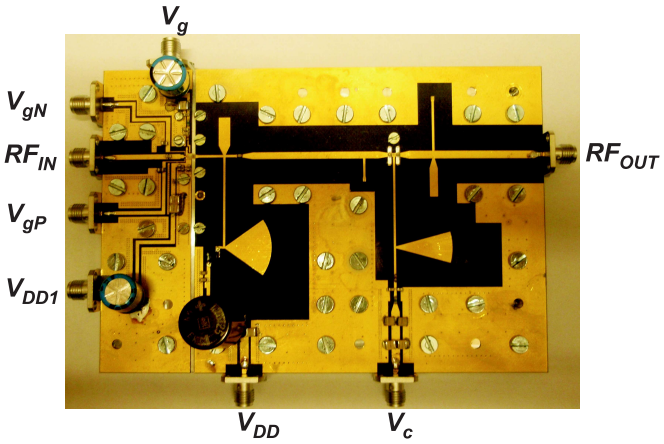


Fig. 14. Photograph of the fabricated prototype transmitter. Size: 13.5x9 cm.

best η_{tot} can be identified at each output power level. It is observed that V_{gN} can be kept constant at 1.0 V for the best η_{tot}. The optimal combination of V_c and V_{gP} versus the P_{out} are shown in Fig. 15, which is divided into two regions: RF-PWM and linear operation regions. In the RF-PWM region, the output power is controlled by varying the duty cycle and the load impedance simultaneously with a constant RF input power to the CMOS modulator, $P_A = 24.5$ dBm. In the linear operation region, the control signals are kept constant and P_A is swept below 24.5 dBm to control the output power. The corresponding input/ouput power relationship is shown in Fig. 16.

For the final application the baseband control signals will be varied dynamically. The V_c can be generated by amplifying the output signal from a digital to analog converter (DAC) with an high speed operational amplifier [21]. Note that negligible power is needed to control the varactor and gate bias voltages.

The efficiency measurement results versus output power using the optimum varactor and driver bias combination are shown in Fig. 17. The measured η is above 70% and η_{tot} is above 55% over the RF-PWM operation region corresponding to a dynamic range of 6.5 dB. The measured η and the dynamic range results well agree with the simulation results presented in Fig. 13. The good agreement is attributed to accuracy of the

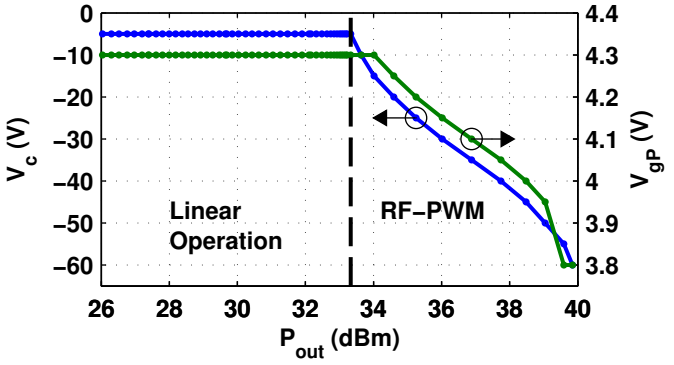


Fig. 15. The optimal varactor and duty cycle control voltages, V_c and V_{gP}, respectively, versus the output power, P_{out}, at 2 GHz carrier frequency.

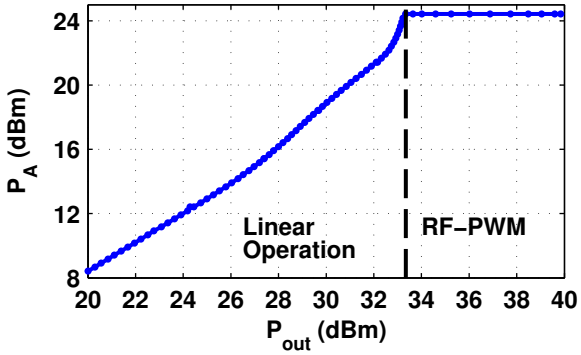


Fig. 16. The available input power from the RF synthesizer, P_A, versus the output power, P_{out}. The carrier frequency is 2 GHz.

GaN HEMT and the varactor models, as well as the careful mounting methods used.

The efficiency is also measured with constant V_c to observe the performance when the load impedance tuning disabled, representing traditional RF-PWM of the Class E PA, see Fig. 18. For that case, η drops to $< 41\%$ at less than 5 dB back-off thus proving that very significant efficiency improvement is achieved with the proposed PA topology.

It is important to mention that the η_{tot} results can be improved substantially by implementing a matching network

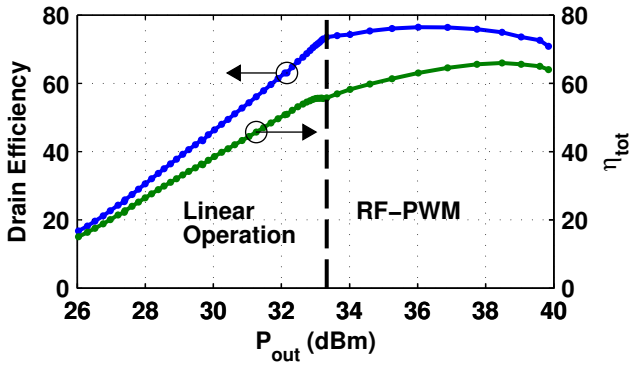


Fig. 17. The measured drain efficiency of the Class-E stage, η, and the overall transmitter efficiency, η_{tot}, versus the output power, P_{out}, at 2 GHz carrier frequency.

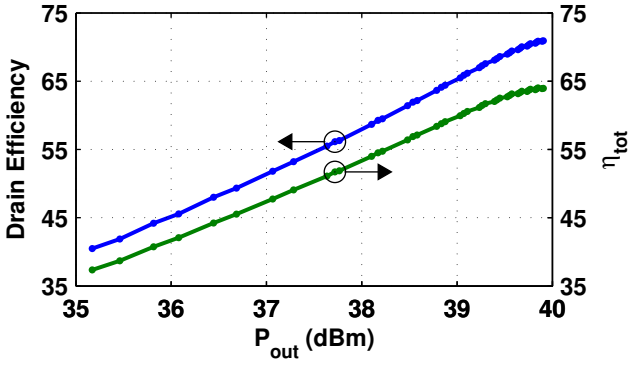


Fig. 18. The measured drain efficiency and the overall transmitter efficiency (η_{tot}) with a constant varactor voltage, $V_c = -60$ V, corresponding to RF-PWM of conventional Class-E. The carrier frequency is 2 GHz.

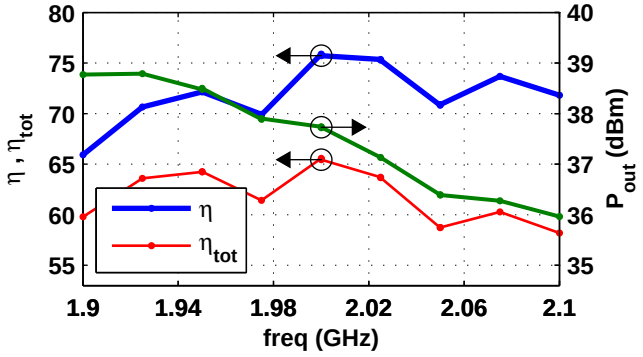
between the modulator input and the RF synthesizer. The load-pull measurements of the modulator have shown that the delivered RF power to the CMOS chip is approximately 6.5 dB lower than the available power used for the measurements, i.e. 19 dBm.

The frequency response of the transmitter is measured at two different power levels, at approximately 2 dB and 6 dB below the peak power using the V_c/V_{gP} combination optimized at 2 GHz. Frequency sweep at the peak power is avoided to prevent any breakdown in the active components due to possible increase in the output power versus the frequency. The results are shown in Fig. 19 indicating that high efficiency operation is maintained over 200 MHz bandwidth, specifically at 2 dB back-off $\eta > 65$ and 6 dB back-off $\eta > 50\%$ across the bandwidth. It is important to mention that the frequency response is related to the back-off level, meaning that the bandwidth performance at the peak output power will probably be even better than the presented results.

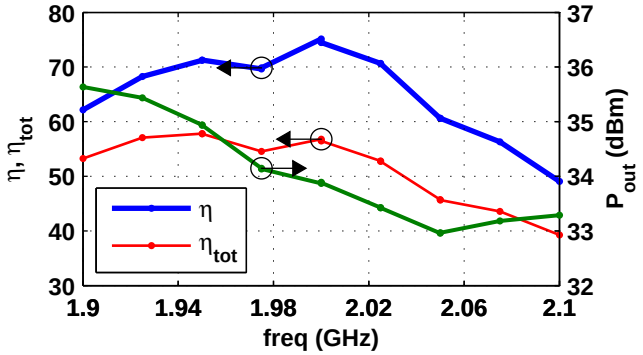
The static characterization results show that the proposed method can provide high efficiency over a wide range of output power levels. The linearity of the transmitter remains to be studied still. The earlier works [21], [22], [23] however show that digital pre-distortion (DPD) of the input signal can be a robust solution for linearization of the transmitter presented. In work [22], a mixed mode out-phasing/Class-B transmitter with a similar input/output power relationship to the one shown in Fig. 16 is linearized with a constellation mapping based DPD algorithm. In works [21], [23], it has been proven that DPD can also remove the residual non-linearities caused by the varactor diodes in the load network for dynamic load modulation architecture. Although the required techniques are already in the literature, a linearity study still requires extensive experiments, analyzes and discussions. Dynamic characterization with modulated signals is therefore not included in the scope of this publication and is subject of future work.

VII. Conclusion

In this paper a novel SMPA topology, Class-E PA with electronically tunable imaginary load impedance, is derived



(a)



(b)

Fig. 19. The measured drain efficiency, η, the overall transmitter efficiency, η_{tot}, and output power, P_{out}, versus the frequency. (a) $V_c = -40$ V and $V_{gP} = 4.05$ V corresponding to 2 dB back-off level at 2 GHz carrier frequency. (b) $V_c = -10$ V and $V_{gP} = 4.2$ V corresponding to 6 dB back-off level at 2 GHz.

particularly to be used in RF-PWM transmitters. It is theoretically proven that such PA topology can provide sub-optimal Class-E operation for variable duty cycles. Thus, in contrast to the existing SMPAs, it does not suffer from switching losses as the duty cycle is varied from the nominal value. Consequently, RF-PWM of the proposed PA can provide an average efficiency that is very close to the peak efficiency for realistic, modulated signals. In this respect, the presented work is pioneering and opening the way for realization of highly efficient RF-PWM transmitters.

The theory is accompanied by a straightforward systematic design procedure, which allows easy design of high performance circuits from given transistor and varactor specifications. A prototype 2 GHz RF-PWM transmitter is manufactured for experimental verification of the theory and the design procedure. A very good agreement is achieved between the theory and the measurement results. The measured drain efficiency of the Class-E stage is higher than 70% and the overall transmitter efficiency is higher than 55% over a 6.5 dB of output power dynamic range proving the feasibility of the proposed PA topology.

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APPENDIX

In this section, various expressions used in the circuit analysis in Section III are presented.

A. The switch voltage

The switch voltage, $v_C(t)$, for the time interval $d\frac{2\pi}{\omega_o} < t < \frac{2\pi}{\omega_o}$ was derived as

$$\begin{aligned} v_C(t) =& C_1\cos(q\omega_o t) + C_2\sin(q\omega_o t) + V_{DD} \\ &+ V_{DD}\frac{q^2}{q^2-1}\rho\cos(\omega_o t+\phi) \end{aligned}$$

where the coefficient C_1 and C_2 follow from the boundary conditions at on-to-off transition, $v_c\left(d\frac{2\pi}{\omega_o}\right) = 0$ and $i_C\left(d\frac{2\pi}{\omega_o}\right) = i_L\left(d\frac{2\pi}{\omega_o}\right) + I_R\sin\left(d2\pi+\phi\right)$, as

$$\begin{aligned} C_1 =& \frac{V_{DD}}{q(q^2-1)}\Big[\sin(2\pi dq)\Big(-q^4\rho\sin(2\pi d+\phi) \\ &- (q^2-1)\big(2\pi dq^2+k-q^2\rho\sin(\phi)\big)\Big) \\ &- q\cos(2\pi dq)\big(q^2\rho\cos(2\pi d+\phi)+q^2-1\big)\Big], \end{aligned}$$

$$\begin{aligned} C_2 =& \frac{V_{DD}}{q(q^2-1)}\Big[\cos(2\pi dq)\Big((q^2-1)\big(2\pi dq^2+k \\ &- q^2\rho\sin(\phi)\big)+q^4\rho\sin(2\pi d+\phi)\Big) \\ &- q\sin(2\pi dq)\big(q^2\rho\cos(2\pi d+\phi)+q^2-1\big)\Big]. \end{aligned}$$

B. Expressions for ρ and ϕ

Variables ϕ and ρ were solved in terms of design variables (d,q,k). The solutions were given in terms of coefficients $(a_{1,2},b_{1,2},c_{1,2})$, which follow as

$$a_1 = 1 - \frac{(2\pi dq^2+k)\sin\big(2\pi q(d-1)\big)}{q} - \cos\big(2\pi q(d-1)\big),$$

$$\begin{aligned} b_1 =& \frac{q^2}{2}\left[\frac{\cos\Big(2\pi\big(q(d-1)+d\big)\Big)}{q+1} - \frac{\cos\Big(2\pi\big(q(1-d)+d\big)\Big)}{q-1}\right. \\ &\left.+\frac{2}{q^2-1}\right], \end{aligned}$$

$$\begin{aligned} c_1 =& \frac{q^2}{2}\left[\frac{\sin\Big(2\pi\big(q(1-d)+d\big)\Big)}{q-1} - \frac{\sin\Big(2\pi\big(q(d-1)+d\big)\Big)}{q+1}\right] \\ &+ q\sin\big(2\pi q(d-1)\big), \end{aligned}$$

$$a_2 = \frac{(2\pi dq^2+k)\cos\big(2\pi q(d-1)\big) - q\sin\big(2\pi q(d-1)\big) - k}{q^2},$$

$$\begin{aligned} b_2 =& \frac{q}{2}\left[\frac{\sin\Big(2\pi\big(q(d-1)+d\big)\Big)}{q+1} + \frac{\sin\Big(2\pi\big(q(1-d)+d\big)\Big)}{q-1}\right], \end{aligned}$$

$$\begin{aligned} c_2 =& \frac{q}{2}\left[\frac{\cos\Big(2\pi\big(q(d-1)+d\big)\Big)}{q+1} + \frac{\cos\Big(2\pi\big(q(1-d)+d\big)\Big)}{q-1}\right] \\ &- \cos\big(2\pi q(d-1)\big) - \frac{1}{q^2-1}. \end{aligned}$$

C. Expression for K_X

An analytical expression for $K_X(d,q,k)$ was derived in Section III in the form of

$$K_X(d,q,k) = \frac{V_X}{V_R}$$

where V_X and V_R follow as

$$\begin{aligned} V_R =& \frac{1}{4\pi(q^2-1)}\Big[-4\cos(2\pi d+\phi)\big(C_2\sin(2\pi dq) \\ &+ C_1\cos(2\pi dq) - V_{DD}(q^2-1)\big) \\ &+ q\Big(4\sin(2\pi d+\phi)\big(C_2\cos(2\pi dq) - C_1\sin(2\pi dq)\big) \\ &+ qV_{DD}\rho\cos\big(2(2\pi d+\phi)\big)\Big) + 4\cos(\phi)\big(C_2\sin(2\pi q) \\ &+ C_1\cos(2\pi q) - V_{DD}(q^2-1)\big) \\ &- q\Big(4\sin(\phi)\big(C_2\cos(2\pi q) - C_1\sin(2\pi q)\big) \\ &+ qV_{DD}\rho\cos(2\phi)\Big)\Big], \end{aligned}$$

$$\begin{aligned} V_X =& \frac{1}{\pi(q^2-1)}\Big[C_2\sin(2\pi d+\phi)\sin(2\pi dq) \\ &+ q\cos(2\pi d+\phi)\big(C_2\cos(2\pi dq) \\ &- C_1\sin(2\pi dq)\big) + C_1\sin(2\pi d+\phi)\cos(2\pi dq) \\ &- C_2\sin(\phi)\sin(2\pi q) + q\cos(\phi)\big(C_1\sin(2\pi q) \\ &- C_2\cos(2\pi q)\big) - C_1\sin(\phi)\cos(2\pi q) \\ &- V_{DD}\Big(\frac{q^2}{4}\rho\Big(\sin\big(2(2\pi d+\phi)\big) \\ &- \sin(2\phi)\Big) + q^2\sin(2\pi d+\phi) - \sin(2\pi d+\phi) \\ &+ \pi(d-1)q^2\rho - (q^2-1)\sin(\phi)\Big)\Big]. \end{aligned}$$

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