(Article begins on next page)

InGaAs/InAlAs/AlAs Heterostructure Barrier Varactors on Silicon Substrate

M. Hadi Tavakoli Dastjerdi, *Student Member, IEEE,* Anke Sanz-Velasco, Josip Vukusic, Erik L. Kollberg, *Fellow, IEEE*, Mahdad Sadeghi, and Jan Stake, *Senior Member, IEEE*

***Abstract*—We present the results of a study on epitaxial transfer of InP-based heterostructure barrier varactor materials onto silicon substrate employing the low temperature plasma activated bonding technique. Test diodes fabricated on the bonded samples exhibit symmetric electrical characteristics, over the temperature range of 25˚C to 165˚C, and show no degradation compared to previously reported InP-based diodes. Moreover, the onset temperature for de-bonding, the effective barrier height extracted from the measured data, and the maximum voltage of the heterostructure barrier varactors for a current density of 100 A/cm^2, were extracted to be 260˚C, 0.56 eV and 10.5 V, respectively.**

***Index Terms*—Millimeter wave devices, wafer bonding, integrated circuits, III-V semiconductors, epitaxial transfer.**

I. Introduction

Terahertz (THz) electronics provides a technology platform for a variety of applications ranging from radio astronomy to biomedical imaging and wireless communications. This technology is largely based on high frequency devices that out of necessity have been fabricated from high mobility III-V semiconductors [1]. Unfortunately, further progress is hampered due to the difficulty to realize fundamental sources in this frequency region. A possibility is to use nonlinear devices and generate high frequency harmonics from a lower frequency pump. The Heterostructure Barrier Varactor (HBV) [2] is one such device that has a symmetric/antisymmetric electrical characteristic and thus does not require DC-bias. Another benefit of the HBV is its inherent high voltage handling capability, which requires excellent thermal management. Thermal issues become even more pronounced at higher frequencies since size constraints together with reduced efficiency increases the heat dissipation density.

Even though the III-V material systems are optimal for the epitaxy when targeting extreme THz frequencies, there are some limitations concerning its native substrates. When addressing issues such as thermal management, integration, machining/processing and fundamental electromagnetic properties, other substrate materials might be better suited. By transferring the active layer structure of the device onto substrates with superior properties the overall device performance, integration and functionality can be significantly improved [3].

To address the mentioned drawbacks with the native III-V substrate, there have been different reports on substrate transfer efforts for the HBV. Epitaxial transfer of the InP-based HBVs onto copper has been reported [4] reducing the electrical and thermal spreading resistance although modern planar HBV topologies require a non-conducting substrate. Transferring the epitaxial structure onto quartz ($\varepsilon_r \approx 3.9$) [5] and borosilicate glass ($\varepsilon_r \approx 4.5$) [6] have been reported in order to decrease the dielectric constant of the substrate resulting in less parasitic capacitance. On the issue of improving device thermal management, measurement results of the hybrid, AlN based [7, 8] flip-chipped HBV circuits have yielded dramatic improvements in power handling ability and conversion efficiency. This is due to the high thermal conductivity of AlN (~170 W/m·K) compared to InP (~70 W/m·K) [9, 10].

In this letter we demonstrate high quality epitaxial transfer of InP-based HBVs onto silicon substrate utilizing the low temperature plasma activated bonding [11] technique as the two material systems are thermally mismatched. This direct bonding approach was preferred over adhesive bonding [3, 12] techniques due to the ambiguous long time behavior and difficulties with thermal treatment of the adhesive materials. Silicon has several advantages over an InP substrate. Besides having almost two times higher thermal conductivity it is also less brittle and has the whole mature microelectromechanical systems (MEMS) toolbox at its disposal. This enables a high level of heterogeneous device integration with micromachined THz waveguides and antennas [13]. Our results show no degradation of the electrical characteristics of the fabricated test diodes compared to those of the InP-based diodes.

II. Device Fabrication

The HBV layer structure [6], Chalmers MBE2052, was grown on a 2–in diameter InP substrate using Molecular Beam Epitaxy (MBE) in an EPI 930 MBE-system at about 500 ˚C. Barrier layers consist of 50 Å $In_{0.53}Ga_{0.47}As$, 50 Å $In_{0.52}Al_{0.48}As$, 30 Å AlAs, 50 Å $In_{0.52}Al_{0.48}As$ and 50 Å $In_{0.53}Ga_{0.47}As$. Fig. 1 shows the schematic of the layer structure on the target substrate.

The (100) silicon wafer used in this experiment was a 2-in diameter, N-doped wafer with a thickness of 290 µm. The wafer was initially cleaned in NH_4OH: H_2O_2: H_2O 1:5:20

Manuscript received October 4, 2010. This research was supported in part by the Swedish Research Council (VR) under Grant No. 2008-5395, and in part by Swedish Governmental Agency of Innovation Systems (VINNOVA) under Grant No. 2007-02955.

The authors are with the Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96 Göteborg, Sweden (e-mail: hadi.tavakoli@ieee.org).

solution at 60˚C for 10 min, known as Standard Clean 1, to remove the organic contaminants and then was dipped in 2% HF solution for 30 s in order to remove the native silicon oxide layer at the surface. A 30 s oxygen plasma treatment was performed on the wafers in the Oxford Plasmalab System 100 after initial cleaning of the chamber. An oxygen flow of 20 sccm with 40 mTorr pressure at forward power of 15 W and ICP power of 800 W was set for this step. Following a short dip of the silicon wafer in water, the wafer was blow dried with N_2 and the two surfaces were immediately put in contact and were transferred to the substrate bonder, MicroTec Suss SB6, where 1000 mbar of tool pressure was applied on the wafers at close to the room temperature for about 4 h. The bonding quality was then inspected using an infrared light source to detect the bonded and unbounded regions, i.e. voids, where Newton`s rings could be observed. After optical inspection, the InP substrate was etched away in an HCL: H_2O 5:1 solution for 1 h.

After the epitaxial transfer, the wafer was diced into samples of 8 mm × 8 mm dimensions. Diode mesas with areas of 3600 μm^2 were fabricated by standard photolithography and wet etching. A second photolithography step was performed to e-beam evaporate the non-alloyed Ti/Pd/Au contacts on top of the created mesas. Due to the thermal mismatch of the bonded materials, avoiding high temperature annealed contacts is preferred. Before the actual contact deposition, the samples were treated by a 10 min long UV-ozone followed by a 20 s ammonium hydroxide dip after which the samples were blow dried by N_2.

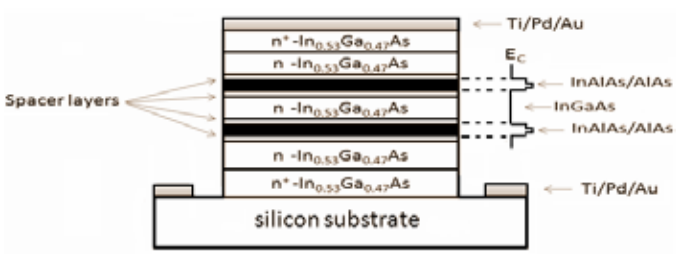

Fig. 1. Schematic of the layer structure of the two-barrier HBV diode and the corresponding conduction energy band diagram (figure not to scale).

III. Results

The infrared image taken from the bonded wafers is shown in Fig. 2(a). Few unbonded regions are observed mostly close to the edges where the Newton`s rings are visible. The side image of the layer structure of the bonded material and the interface between the highly doped $In_{0.52}Ga_{0.48}As$ and silicon can be seen from the SEM image in Fig. 2(b). In order to find out the maximum allowed temperature before de-bonding, the samples were annealed for 1 min from 200˚C to 300˚C and it was found that de-bonding onset temperature is about 260˚C. Beyond this temperature the samples would be irreversibly damaged.

The current-voltage characteristics of the fabricated diodes were measured with a Keithley 4200 semiconductor characterization system at different temperatures from RT up to 165˚C, see Fig 3. Fig 4 shows the differential capacitance-voltage (C-V) characteristics of the fabricated diodes on silicon substrate together with InP based diodes with a similar intrinsic HBV layer specification, Chalmers MBE2049 [6], measured at room temperature with a HP4284A LCR meter. For the 2-barrier device measured at RT, a breakdown voltage of about 10.5 V was observed. The maximum voltage, here defined as the voltage resulting in a current density of 100 A/cm^2, drops from ca 10.5 V at RT down to 6.8 V at 165˚C. A zero-biased differential capacitance of about 1.3 fF/μm^2 and a minimum differential conductance $(dI/dV)|_{v=0}$ of 0.12 pS/μm^2 were measured. The measured parameters are all comparable to previously reported data for the similar active layer structures on InP substrate [8, 14, 15].

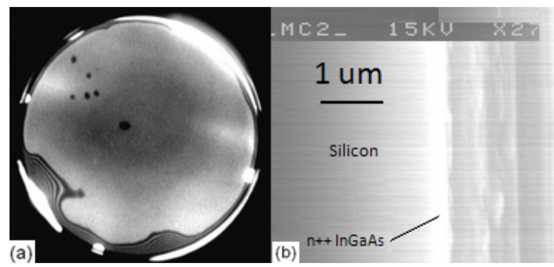

Fig. 2. (a) IR-image of the bonded wafers, (b) SEM image of the bond interface $In_{0.53}Ga_{0.47}As$ / Si.

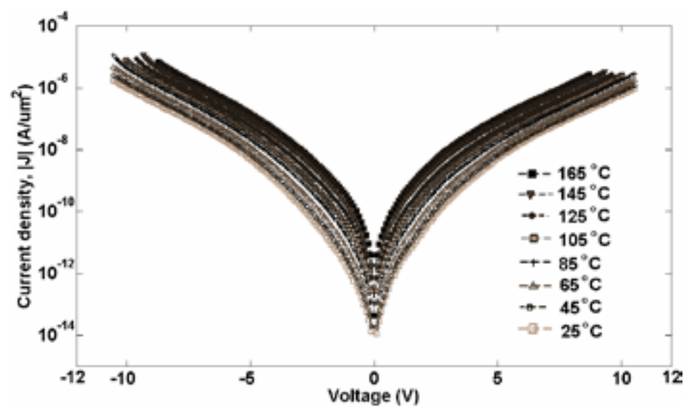

Fig. 3. Measured current density versus applied voltage at different temperatures.

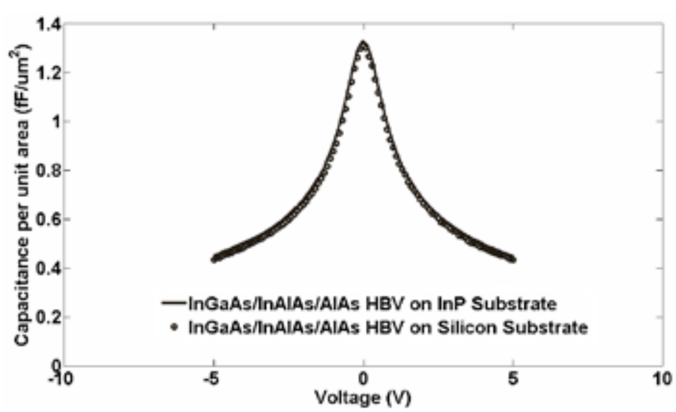

Fig. 4. Differential capacitance per unit area versus applied voltage for the fabricated HBV diodes on silicon substrate and InP based diodes with a similar intrinsic HBV layer specification. Both samples were measured at room temperature.

The effective barrier height, ϕ_b, of the pseudomorphic

$In_{0.52}Al_{0.48}As/AlAs/In_{0.52}Al_{0.48}As$ barrier structure can be estimated by analyzing the minimum differential conductance, G_{min}, versus temperature. For a small external bias and relatively thick barriers, say >10 nm, thermionic emission across the barrier will start to dominate over tunneling current [14] at moderate to high temperatures. If the effect of field emission and tunneling are neglected, the current is mainly limited by thermionic emission as described by Richardson's law:

$$J = A^* T^2 e^{-\frac{\phi_b(V)}{KT}} \qquad (1)$$

where A^* is the modified Richardson constant and ϕ_b is the bias dependent barrier height [16]. Hence, the differential conductance at zero bias can be expressed as:

$$G_{\min} = A\left.\frac{\partial J}{\partial V}\right|_{V=0} = A\frac{A^*}{k}\frac{\partial \phi_b(0)}{\partial V} T e^{-\frac{\phi_b(0)}{KT}} . \qquad (2)$$

An Arrhenius plot of the measured minimum conductance, $\ln(G_{min}/T)$ versus $1000/T$, is shown in Fig. 5. The measurements indicate that thermionic emission starts to dominate above ca 350K, whereas tunneling of carriers is more important at room temperature.

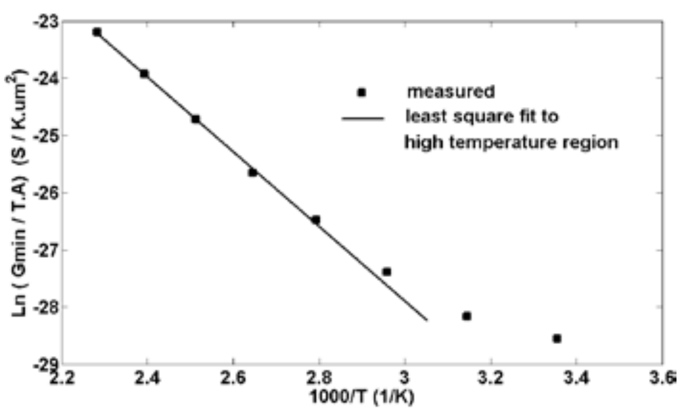

Fig. 5. Arrhenius plot of ln(G/T) versus 1000/T, (at V_{bias}=0 Volt).

The effective barrier height at zero bias of the device, ϕ_b, was estimated to be 0.56 eV, by applying a least square fit of (2) for the high temperature region (asymptote). The data are comparable with reported results for HBVs on InP [14, 15] and also close to the expected conduction band offset, ΔE_c, of 0.65eV [17].

IV. Conclusions

We have successfully demonstrated a direct bonding technique for transferring InGaAs/InAlAs/AlAs HBVs onto silicon substrates without any use of adhesives. The low temperature plasma activated bonding method resulted in a mechanically and thermally stable structure and no degradation was observed in electrical characteristics over normal operating temperatures. The epitaxial transfer technique is promising for future integrated terahertz circuits, where high-speed III-V devices can be combined with silicon based electronics as well as advanced micromachined THz-circuits.

References

[1] T. W. Crowe, W. L. Bishop, D. W. Porterfield, J. L. Hesler, and R. M. Weikle, "Opening the Terahertz window with integrated diode circuits," *IEEE Journal of Solid-State Circuits,* vol. 40, pp. 2104-2110, Oct. 2005.

[2] E. L. Kollberg and A. Rydberg, "Quantum-barrier-varactor diode for high-efficiency millimetre-wave multipliers," *Electronics Letters,* vol. 25, pp. 1696-1698, 1989.

[3] S. M. Marazita, W. Bishop, J. Hesler, K. Hui, W. E. Bowen, and T. Crowe, "Integrated GaAs Schottky mixers by spin-on-dielectric wafer bonding," *IEEE Transaction on Electron Devices,* vol. 46, pp. 1152-1157, Jun. 2000.

[4] L. Dillner, W. Strupinski, S. Hollung, C. Mann, J. Stake, M. Beardsley, and E. L. Kollberg, "Frequency Multiplier Measurements on Heterostructure Barrier Varactors on a Copper Substrate," *IEEE Electron Device Letters,* vol. 21, pp. 206-208, May. 2000.

[5] S. Arscott, P. Mounaix, and D. Lippens, "Substrate transfer process for InP-based hetersotructure barrier varactor devices," *Journal of Vacuum Science and Technology B,* vol. 18, pp. 150-155, Jan. 2000.

[6] M. H. Tavakoli Dastjerdi, A. Sanz-Velasco, J. Vukusic, and J. Stake, "Transfer of InP-based HBV epitaxy onto borosilicate glass substrate by anodic bonding," *Electronics Letters,* vol. 46, pp. 1013-1014, Jul. 2010.

[7] Q. Xiao, J. L. Hesler, T. W. Crowe, I. Robert M. Weikle, and Y. Duan, "High Efficiency Heterostructure-Barrier-Varactor Frequency Triplers Using AlN Substrates," in *IMS 2005*, Long Beach, CA, 2005.

[8] J. Vukusic, T. Bryllert, T. A. Emadi, M. Sadeghi, and J. Stake, "A 0.2-W heterostructure barrier varactor frequency tripler at 113 GHz," *IEEE Electron Device Letters,* vol. 28, pp. 340-342, May. 2007.

[9] M. Ingvarson, B. Alderman, A. Ø. Olsen, J. Vukusic, and J. Stake, "Thermal constraint for heterostructure barrier varactor diodes," *IEEE Electron Device Letters,* vol. 25, pp. 713-715, Nov. 2004.

[10] J. Stake, L. Dillner, S. H. Jones, C. M. Mann, J. Thornton, J. R. Jones, W. L. Bishop, and E. L. Kollberg, "Effects of self-heating on planar heterostructure barrier varactor diodes," *IEEE Transactions on Electron Devices,* vol. 45, pp. 2298-2303, Nov. 1998.

[11] D. Pasquariello and K. Hjort, "Plasma-assisted InP-to-Si low temperature wafer bonding," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 8, pp. 118-131, Jan./Feb. 2002.

[12] F. Niklaus, G. Stemme, J. Q. Lu, and R. J. Gutmann, "Adhesive wafer bonding," *J. Appl. Phys.,* vol. 99, Feb. 2006.

[13] C. Jung, C. Lee, B. Thomas, G. Chattopadhyay, A. Peralta, R. Lin, J. Gill, and I. Mehdi, "Silicon Micromachining Technology for THz applications," presented at the *35th International Conference on Infrared, Millimeter and THz Waves*, Rome, Italy, 2010.

[14] T. A. Emadi, T. Bryllert, M. Sadeghi, J. Vukusic, and J. Stake, "Optimum barrier thickness study for the InGaAs/InAlAs/AlAs heterostructure barrier varactor diodes," *Applied Physics Letters,* vol. 90, pp. 012108-3, Jan. 2007.

[15] R. Havart, E. Lheurette, O. Vanbésien, P. Mounaix, F. Mollot, and D. Lippens, "Step-like heterostructure barrier varactor," *IEEE Transactions on Electron Devices,* vol. 45, pp. 2291-2297, Nov. 1998.

[16] H. Hjelmgren, J. East, and E. L. Kollberg, "Thermionic emission Current in a single barrier varactor," in *Third International Symposium on Space Terahertz Technology*, pp. 110-114, 1992.

[17] T. Inata, S. Muto, Y. Nakata, S. Sasa, T. Fujii, and S. Higamizu, "A Pseudomorphic In0.53Ga0.47As/AlAs Resonant Tunneling Barrier with a Peak-to-Valley Current Ratio of 14 at Room Temperature," *Jpn. J. Appl. Phys.,* vol. 26, pp. L1332-L1334, Aug. 1987.