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Design and Implementation of FOX Radar Interface using Gbit Ethernet

Master of Science Thesis

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Abstract

The object of this thesis project was to design and implement an external radar interface to the Saab Systems radar extractor FOX. The radar extractor runs on a standard PC and the radar interface used today is a full length PCI card, thus limiting the minimum size of the PC. In addition as the radar interface needs to be located close to the radar to avoid cable losses, the FOX PC is often located in a narrow inaccessible space. Therefore a design of a new external radar interface gives the possibility to use a FOX PC with very small form factor.

The best solution found for the communication between the FOX PC and the external radar interface was Gbit Ethernet over cat-5e cables. This interface also enables the FOX PC to be moved up to 100 meter away from the external radar interface.

The design of the Fox external Radar Interface (FRI) is constituted of two parts, an Ethernet connectivity part and a radar interface part. The Ethernet part is designed using a PowerPC processor board with Gbit Ethernet ports whereas the radar interface part is a custom build circuit board with circuits for digitalization of the radar signals. In between the two parts an FPGA circuit is placed and used for high speed data processing.

The Design of the FOX external radar interface is completed but as the implementation has been delayed so no functional prototype was constructed during this thesis project.

Abbreviations

ACP	Azimuth Counter Pulse
ADC	Analogue to Digital Converter
ARP	Azimuth Reset Pulse
FRI	Fox external Radar Interface
FPGA	Field Programmable Gate Array
IDE	Integrated Development Environment
IP	Intellectual Property
MAC	Media Access Controller
PHY	Ethernet Physical Interface
PLD	Programmable Logic Device
PRF	Pulse Repetition Frequency (Frequency at witch a pulse radar transmits pulses)
RIC	Radar Interface Card
UDP/IP	User Datagram Protocol over the Internet Protocol

Acknowledgements

Many thanks, to my supervisor Jakob Sönnerstam who has successfully guided me through my thesis project and to all my colleagues at Saab Systems in Göteborg.

Special thanks to my dear girlfriend Sarah who has been most understanding and helpful proofreading my thesis report.

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1. Introduction

This is a report of my thesis work that was carried out at Saab Systems Security Solutions ATM Göteborg during the summer and autumn 2006.

1.1. Saab Systems Security Solutions, ATM

Saab Systems Security Solutions Air Traffic Management (ATM) formally AerotechTelub is a part of the SAAB group which is one of the worlds leading high-tech companies. The company has its main operations in defence, aviation, space and civil security. The ATM business units' main focuses are management software and systems for civil and military air traffic. ATM Göteborg has approximately 20 employees and is located in the Saab Space building in Kallebäck.

1.2. Problem Description

ATM has developed the FOX radar extractor. FOX is a flexible, high-performance, cost-effective radar extractor. It can be connected to many types of radar stations, presentation devices, and processing systems. The application of FOX includes e.g. marine radar stations for naval surveillance, within aviation surveillance systems and for surface movement radars. FOX is designed as a software product, running in a standard PC environment under the operating system Windows NT/2000/XP. Input of raw radar is done via a plug-in circuit board for the PCI-bus.

Since future radar systems require smaller and more easily maintained components, the full size PCI radar interface board used today limit the size and flexibility of the PC running FOX.

The FOX computer is preferably located close to the radar since the radar video is easily degraded if transmitted over long distances. This is not always a problem, but if the radar is located in a tower or somewhere else where space is scarce, there might be a problem when the system needs support/service. So preferably the FOX computer should be able to be moved away from the radar and an external radar interface should be used as shown in Figure 1.1. In addition, it is desired that the FOX system should be a cost-effective system so a cheaper more flexible solution for the radar interface is desired.

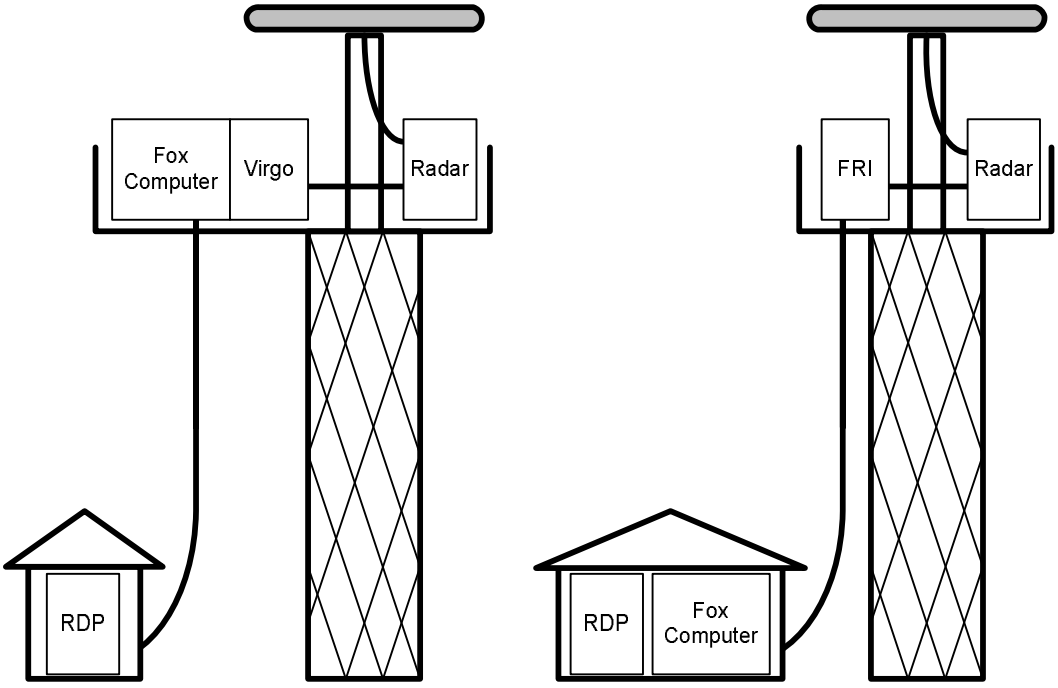

Figure 1.1 Left; Radar system design used today where the FOX computer uses an internal radar interface card so the FOX computer has to be located relatively close to the radar. Right; Design using an FOX external Radar Interface FRI which makes the placement of the FOX computer more flexible.

1.3. Thesis Description

The thesis project is to design and construct an external radar interface. The interface should be able to receive and digitalize radar video signals and decode azimuth signals. The radar interface shall also communicate with a PC using a standard communication interface like USB, Firewire or Ethernet. The receiver of the radar data is Saab Systems radar extractor FOX, which extracts plots and targets from the received radar video.

The project involves both hardware construction and software programming.

2. Radar System Theory

There are many types of radars, where the pulse radar is the simplest and probably most used type. The basic operation of a typical pulse radar may be described using Figure 2.1. (Skolnik, M. I. 1981) and (Kingsley, S., Quegan, S. 1999)

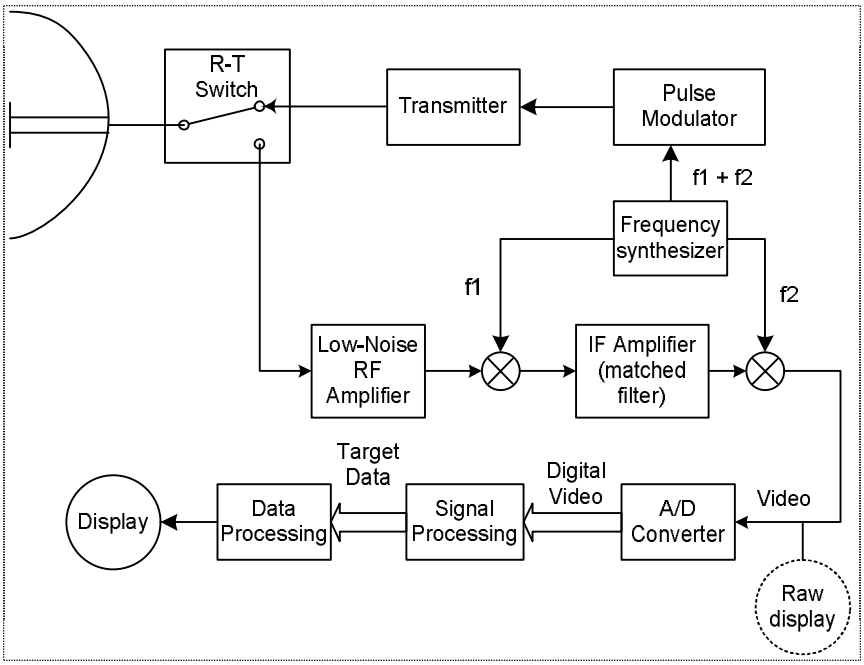

Figure 2.1 A description of a pulse radar system with a super heterodyne receiver. Radar video from the receiver is digitalized. Targets are found and followed in the Signal processing stage. Target identification, trajectory prediction etc. is done in the data processing. Then the relevant information is presented on a display.

In this description the carrier frequency, at which the radar transmits is generated by the frequency synthesizer and the shape and frequency of the pulse is modulated on to the carrier frequency in the pulse modulator. The pulsed signal is then fed into the transmitter where the signal is amplified. Thereafter the amplified radar pulse is fed in to the antenna through the receiver transmitter switch or duplexer. When the radar pulse is transmitted, the duplexer is “switches” to receiving mode and the radar then listens for echoes of the transmitted pulse.

The radar receiver in this description is of the super heterodyne type, where the first stage after the duplexer is a low noise amplifier. The signal is then down converted using a mixer to a lower intermediate frequency (IF), which is then amplified and decoded. The signal is down mixed again to a base band or video signal. A typical radar video signal is shown in Figure 2.2, where the transmitted pulse and three target echoes are illustrated. The transmitted pulse is seen since there are often some power leakages in the duplexer.

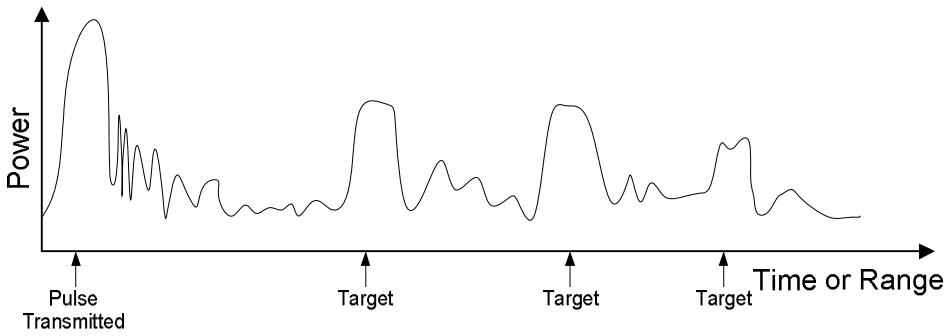

Figure 2.2 A typical radar video signal, were the transmitted pulse and three target are seen.

This video can with the use of azimuth information be visualized in a polar display with the range and azimuth displayed as radius and angle coordinates, whereas the power is displayed as intensity.

The radar video signal is then sampled and converted to a digital video signal. From this digital video targets can be detected. When combining these new targets with old targets, the real targets can be identified and clutter and interference can be removed, this signal processor stage is also called extractor.

The azimuth information is generated mechanically from the radar antenna and it is given by the Azimuth Counter Pulse (ACP) and Azimuth Reset Pulse (ARP) signals. The ACP signal send out a known number of pulses during one revolution and the ARP signal send out a single pulse when the radar points north.

The standard pulse radar interface also transmits a synchronization pulse signal that is triggered when a radar pulse is transmitted. This Synchronization pulse is used as reference when measuring distances to targets found in the radar video.

The range of a radar is not only determined by the transmit power and receiver sensitivity, but also determined by the frequency at which the radar transmit radar pulses Pulse Repetition Frequency (PRF) and sweep time, the time of one revolution. If the PRF is too high, the radio waves do not have the time to do a round trip from the radar to the target and back before the next pulse is transmitted. In addition, there could be difficulties determine the range to the target as the echo might be registered as an echo of the next radar pulse. This can be seen in Figure 2.3 where (a) shows where the target are physically located relative to the radar and (b) shows received echoes if target exceeds the pulse repetition period. There are several methods to distinguish this multiple time around echoes form the unambiguous echoes. One method is to colour or label each pulse in some way so they can be distinguished from its closes neighbours. One other way is to let the PRF fluctuate and combine several pulses to sort out the echoes that does not fluctuate with the PRF seen in Figure 2.3(c).

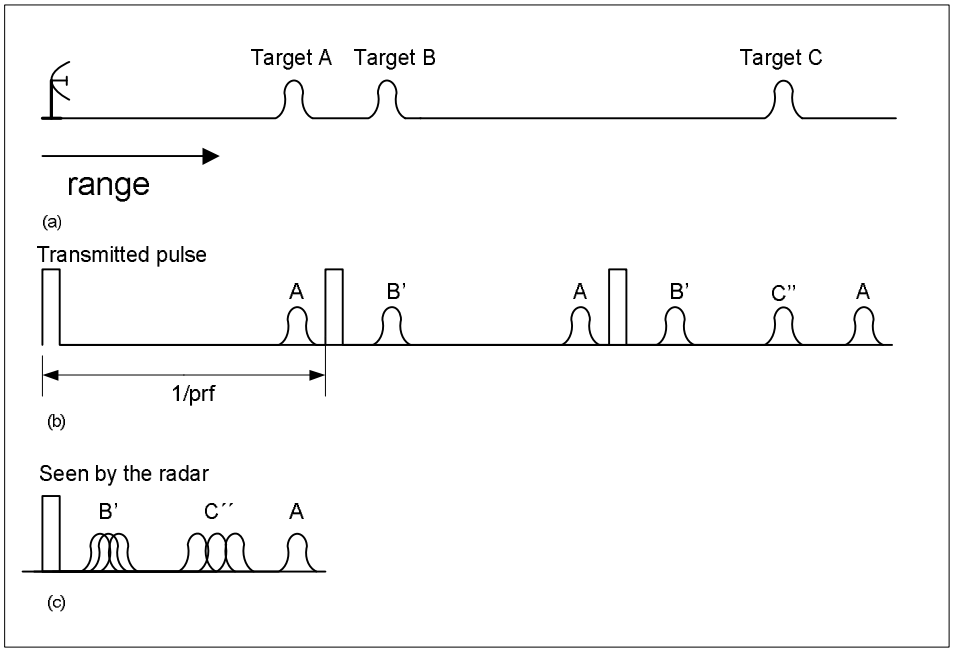

Figure 2.3 A problem that can occur when the PRF of the radar and the sweep time are poorly configured. (a) The geographical orientation of the radar and the three targets. (b) The radar video where multiple time around targets can B' and C''. (c) radar video with a fluctuating PRF only the non multiplier time around target is stationary.

If the sweep time is too short the radar antenna will point in different direction when the radar echo is received. This can also be used to reduce the multiple time-around echoes, so the sweep time and PRF of radars are closely linked together.

3. System Design

3.1. Specification

The full specification of the FOX external Radar Interface, FRI can be found in Appendix A

Summary of the FRI specification

Function

The External Radar Interface shall be able to receive a radar video signal and transmit a digitalised version of the video to the extractor. It should also be able to receive and decode azimuth signals and transmit the data to the extractor.

The Radar Interface

- One 75 Ω BNC connectors for the Radar Video with signal levels of 0-5V.
- One 75 Ω BNC connectors for the Synchronisation pulse.
- One 9 pin D-type connector for the two azimuth signals on differential pairs that follow the RS-422A standard.

FOX interfaces

- Communication with the extractor shall use a standard high speed communication interface like USB, Firewire or Ethernet.
- A C++ program module shall be implemented to complement FOX with the new radar interface.

Signal Processing

- The radar video shall be digitalized using an ADC with a variable sampling frequency up too and preferably higher than 50 MHz. The resolution of the sampled data shall be at least 8 bits.
- The synchronisation pulse shall be time stamped using a 1 MHz timer.
- Decoding of the azimuth pulse signals.
- The data throughput should be such that the system can handle a PRF of 12 kHz or 4096 samples per radar pulse.

3.2. Preliminary Work

The first task was to decide which of the three preferred interfaces that should be used for the FRI to radar extractor communication.

The first criterion that the interface had to fulfil was the data throughput. The maximum data generation rate depends on the sampling frequency, the sample resolution and on the sampling time. By not sampling the radar video constantly the interference between two radar pulses are reduced. Se Figure 3.1.

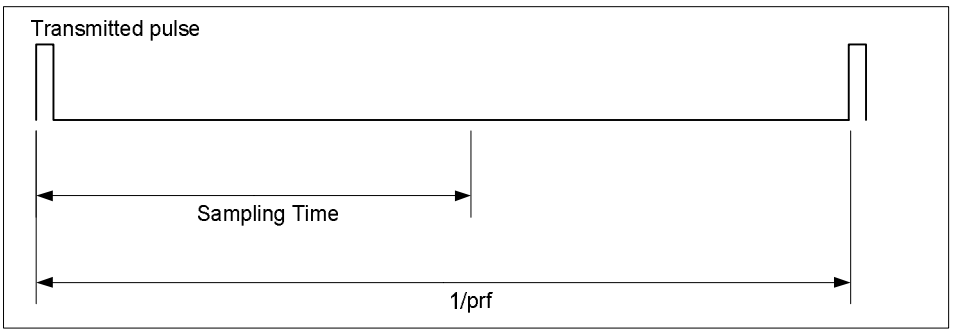

Figure 3.1 The received radar signal is in this case sampled during the first half between two radar pulses.

The maximum data generation was obviously when using the maximum sampling frequency and the longest radar pulse sampling time.
When using an ADC resolution of 8 bits, a sampling frequency of 50MHz and a sampling time of half the pulse repetition time the equation (3.1) give a maximum data generation of 24 Mibyte/s. This rate could probably be reduced using data compression.

$$ADC_{\text{Res.}} \cdot f_s \cdot \tau_s = DataRate \qquad \textbf{(3.1)}$$

Where τ_s = Sampling time relative to the pulse repetition time.

USB

The maximum data rate specified for the USB interface is 480 Mbit/s which is roughly 55 Mibyte/s and the maximum cable length is 5 meters (usb.org, 2006).

IEEE 1394 Firewire

The newest Firewire standard IEEE 1394b support data rates up to 3.2 Gbit/s. But the available products used today ether use the older IEEE 1394a standard with data rates up to 400 Mbit/s and a maximum cable length of 4.5 meters, or they use the IEEE 1394b standard at 100 Mbit/s which support cables up to 100 meters (IEEE 1394b, 2002).

Ethernet

The 1000Base-T Ethernet uses standard CAT-5e cables and has a maximum bit rate of 1Gbit/s for cables up to 100 meters. (IEEE 802.3, 2005)

All the three interfaces can support the data throughput needed for the FOX communication. The data rate is therefore not a limiting factor, but since radar towers can be tens of meters high, a standard that support cable length over 30 meters is preferred. This excludes the USB interface and the Firewire IEEE 1394a standard. The Firewire interface using the newer 1394b standard for long distances is rarely used today and it uses special cables, thus this solution is excluded. The Gbit Ethernet using standard CAT-5e cables is more or less a standard on new high end PCs today and it is also frequently supported on embedded processors. As a consequence a solution using Gbit Ethernet over standard CAT-5e cables was selected.

3.3. Design

Ethernet Communication

The first priority task in the design process was to find a solution for the Ethernet communication, since that was deemed to be the most challenging part of the design.

Ethernet occupies the two lowest layers of the Open Systems Interconnection Model, OSI; the physical layer and the data link layer which are illustrated in Figure 3.2.

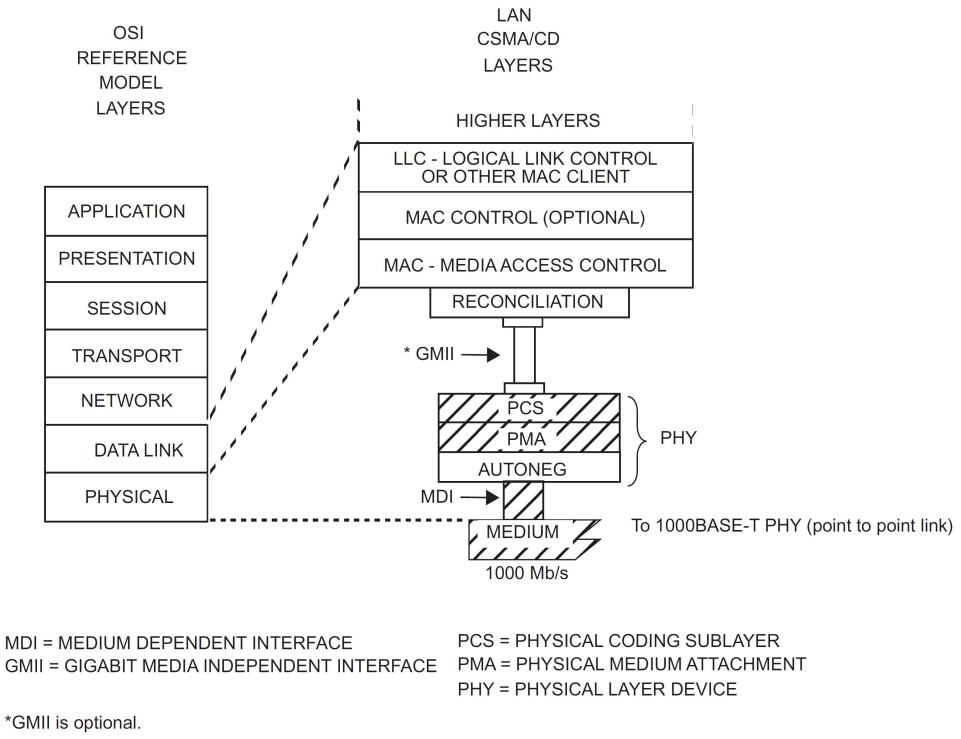

Figure 3.2 Type 1000BASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model (IEEE 802.3, 2005).

To design an Ethernet capable system it must consist of a PHY-unit that supply the physical interface to the medium. The PHY modulate and demodulate the analogue signal that is transmitted onto and received from the medium. The next mandatory unit is the MAC Medium Access Controller, this unit organises the communication over the medium. Since 1000BASE-T Ethernet is basically a point to point communication protocol, an extra protocol layer is needed.

Several Ethernet physical design solutions were considered either using a processor based or using a FPGA based solution.

Two main Ethernet solutions using processors were considered. One solution involved a DSP with a PCI bus connected Ethernet Controller with MAC and PHY, whereas the other solution involved a PowerPC processor with build in Ethernet MAC and an external PHY.

The FPGA solution used an IP block implementation of the Ethernet MAC and an external PHY. The three Ethernet solutions are illustrated in Figure 3.3.

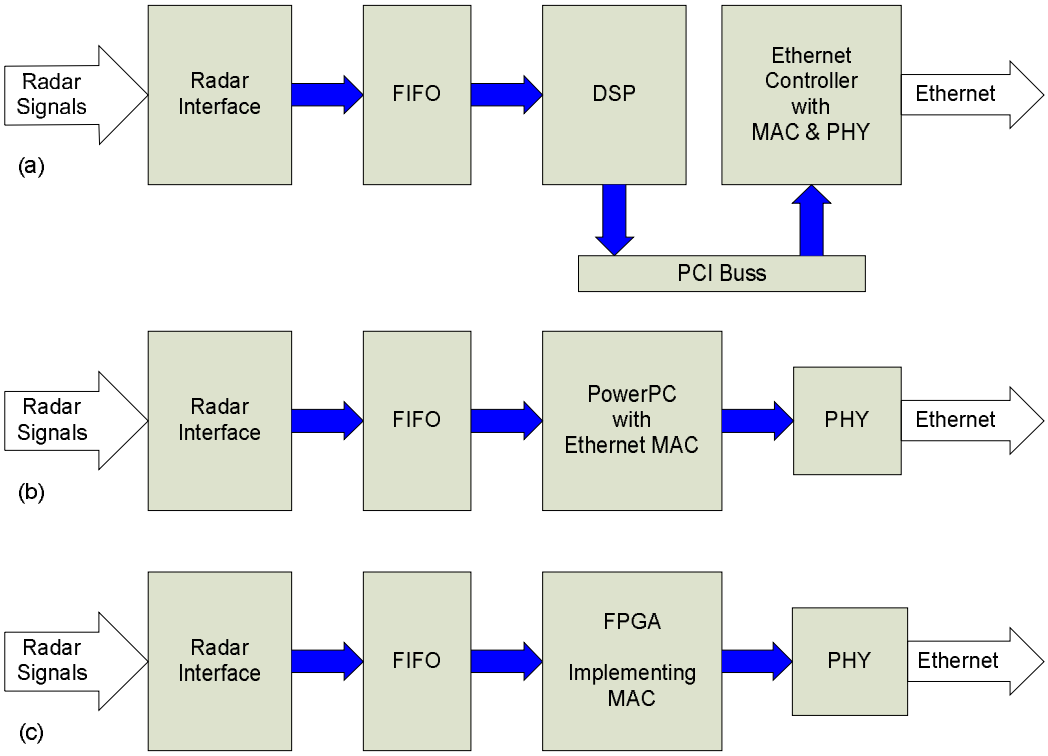

Figure 3.3 Three investigated solutions for Gbit Ethernet communication.

Since all three solutions required a large electrical design-effort, hence a lot of time, a complete Gbit Ethernet solution was desired.

For the network layer the IP protocol will be used and for the transport layer the User Datagram Protocol (UDP) will be used as it is simple and resource friendly and there is no need for absolute reliability.

A suitable processor board was found that used a Freescale Power Quick II Pro processor (Freescale, 2006) with a complete Gbit Ethernet interface. The name of this board is Rattler 8347 (Analogue & Micro Ltd, 2006) and will be referred to as Rattler in this thesis report. The board came with GNU development tools and operating system. As this board dose not have the ability to interface directly using the specified radar interface, a Radar Interface Card, RIC had to be added to the design. A bonus with the rattler board is the small FPGA used for the configurable expansion connector, which will make a flexible connection to the radar interface card.

3.3.1. Rattler Board

The specification of the PowerPC board.

- Freescale MPC8347 processor with 400 MHz core speed
- 128 MB DDR RAM
- 32 MB program Flash Memory
- 2x 10/100/1000 Base Ethernet ports
- 1x 32-bit PCI port
- 140 pin configurable expansion port
- 2x RS-232 serial ports
- 2x USB 2.0 ports

The configurable expansion port uses a Lattice FPGA for signal routing, which gives a large flexibility in how signals are connected on the expansion port. The signals routed from the processor to the FPGA are some digital IO ports and the Local Bus Controller (LBC). The FPGA is configured from the processor using a boot loader function. The board is powered by a 3.3 DC power supply and consume around 2A and the power can either be connected to the board via a standard DC port or it can be connected though the expansion port.

The board comes with GNU development tools and eCos and Linux operating systems which both include a full TCP/IP stack for Ethernet communication. The eCos is a highly configurable open source real-time operation system that is intended for embedded applications.

To facilitate the development, the board had the Redboot boot loader installed at delivery. This boot loader support downloading of embedded applications using a serial or Ethernet interfaces, and it is controlled using serial terminal interface.

3.3.2. Rattler FPGA

The FRI system requires that some digital functions have to be implemented in hardware because they have special need for speed and timing and software is too slow and unresponsive. These digital functions can either be implemented using dedicated digital circuits and/or they can be combined into a Programmable Logic Device (PLD).

For all the digital functions, a PLD implementation was selected as it makes a much smaller and neater electrical design. The PLD will also work as an interface between the ADC and the processor, but since the data generation rate at the ADC is high, a buffer is needed to offload the processor. The best solution is therefore to use some sort of dual clocked FIFO memory.

During the design process the target device for the programmable logic changed and the FIFO functionality moved inside the PLD. The first intended target device was an Altera CPLD (Complex PLD). The program was developed using the Altera Quartus II Web Edition IDE, and written using VHDL as description language. This solution was based on the usage of an external FIFO memory, but since fast FIFO circuits where found to be quite expensive, the target device was changed from the CPLD device to an Altera Cyclone II FPGA device with build in memory. The migration from the CPLD to the FPGA was simple and the implementation of a FIFO block was easily done using an IP block supplied with the Quartus development software.

When further data on the Rattler board was received it was discovered that the above solution could fit in the Rattler FPGA (Lattice EC FPGA), which is a smaller but similar variant of Altera FPGA. The only drawback found was the development tool for the Lattice FPGA ispLEVER which is not as good as the Altera Quartus tool. It lacks simulation tools and it has a very complex and non user-friendly interface.

It was decided to use this Lattice FPGA solution and the migration of the FPGA program to ispLEVER was easily done and a Lattice specific IP block was used for the FIFO memory.

3.3.3. Radar Interface Card

After the decision to use the rattler FPGA almost all digital functions where moved to the rattler board. Thus the functionality that remains to be done on the Radar Interface Card, RIC, is the radar connector interface, signal adaptation and conversion. The basic description of the radar interface card can be seen in Figure 3.4.

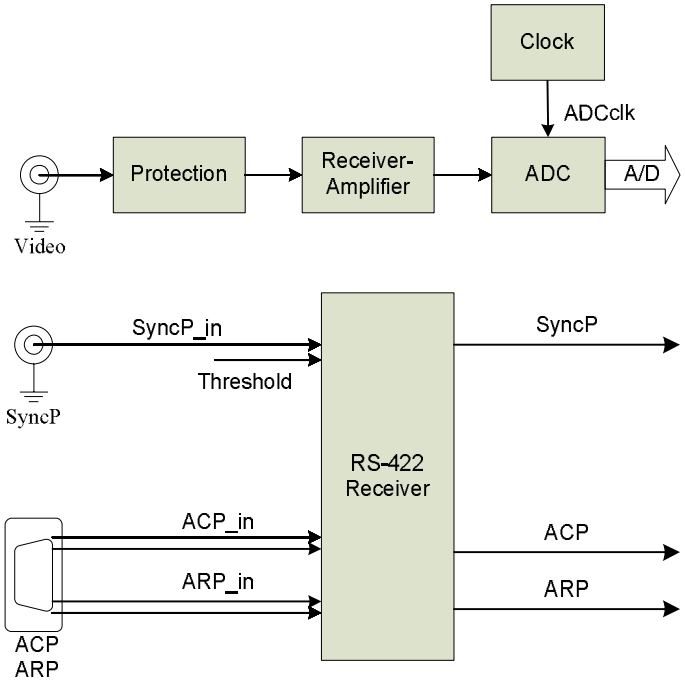

Figure 3.4 A block diagram description of the RIC.

The radar video will be connected to the board using a BNC connector and to protect the amplifier stage from ESD a protection circuit will be used. Then to maximise the ADC's dynamic range a programmable receiver amplifier stage will adjust the radar video gain and offset. The ADC used will be able to sample the signal at 10 bits resolution and with frequencies up to 105 MHz, and the ADC clock will be generated by a programmable clock synthesizer that can generate a clock signal over the entire frequency range of the ADC.

The azimuth signals are differential digital signals and they will be connected to the RIC using a standard 9-pin D-type connector. The two differential signals will be received and transformed to single ended signals using a standard RS-422 receiver circuit with build in ESD protection.

The Synchronisation signal will be connected using a BNC connector. The synchronisation signal needs to be compared to a threshold voltage then this will generate the digital signal. The same RS-422 receiver circuit as used for the azimuth signals will be used since it basically is a Schmitt trigger circuit with a threshold input. Although the hysteresis of the receiver is only 45mV, but it can be compensated for using a “digital hysteresis” function in the FPGA. Since the RS-422 circuit has a lot of ESD protection no extra protection is needed.

The radar interface card will also be a power supply card, it will generate the voltages needed for the card itself and it will also supply the rattler board.

4. System Construction

A functional division between the two cards is found in Figure 4.1.

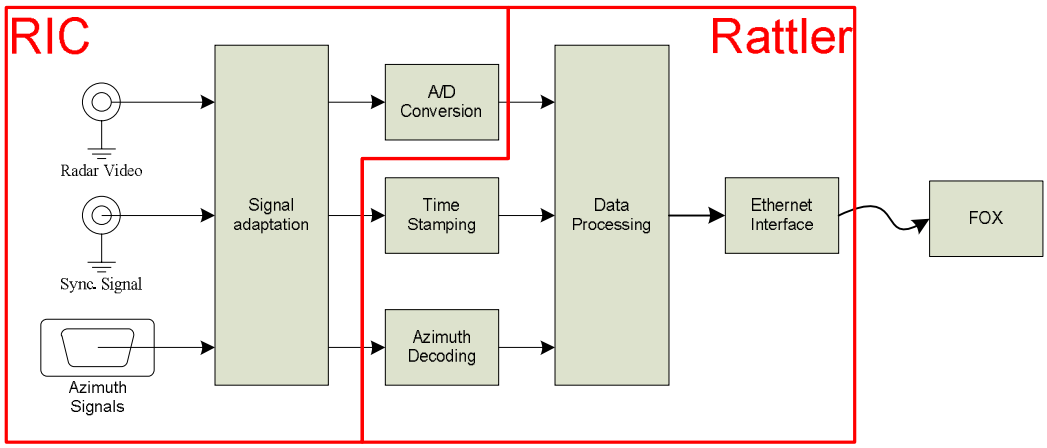

Figure 4.1 The physical distribution of functional blocks between the rattler board and RIC of the FIR system.

4.1. Rattler Card

4.1.1. PowerPC Program

The task of the PowerPC program is to control the FRI and to communicate with the FOX. The control task is to program the FPGA, the DAC as well as the Clock synthesizer. The communication task is to receive configuration information from the FOX and to transmit the digital radar data and status information to the FOX.

The PowerPC compiler supplied with the rattler board run on Linux or on Windows using the Cygwin environment. The eCos operating system is configured with the “net template” that enables the Ethernet capability of the board.

When the eCos was build, simple test programs where written to verify the operating system. The program and operating system was easily downloaded to the processor using the TFTP protocol.

To test the Local Bus Controller (LBC) communication with the FPGA, severak test programs were written. This program read and writes to the memory mapped address that is connected to the FPGA.

4.1.2. Rattler FPGA

The FPGA program was designed and implemented in four modules represented as VHDL entities. The modules are CTB (Counter Timer Block), DSG (Data Sequence Generator), FIFO-memory and SBI (System Bus Interface). A block diagram of the different modules and input/output signals can be seen in Figure 4.2.

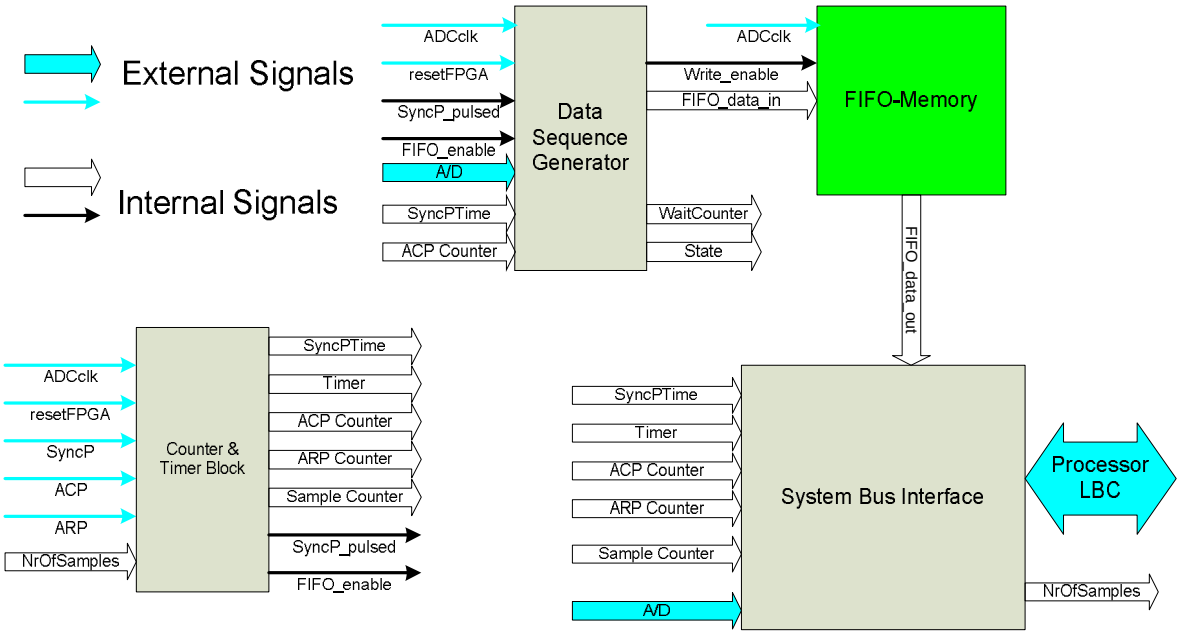

Figure 4.2 Block diagram of the rattler FPGA VHDL program.

The first module is **CTB**. This module is implemented using two architectures; one for the counter and timers and one sub-architecture for the digital hysteresis. The CTB is described in Figure 4.3 and different components in the figure are numbered and thoroughly described in the following text.

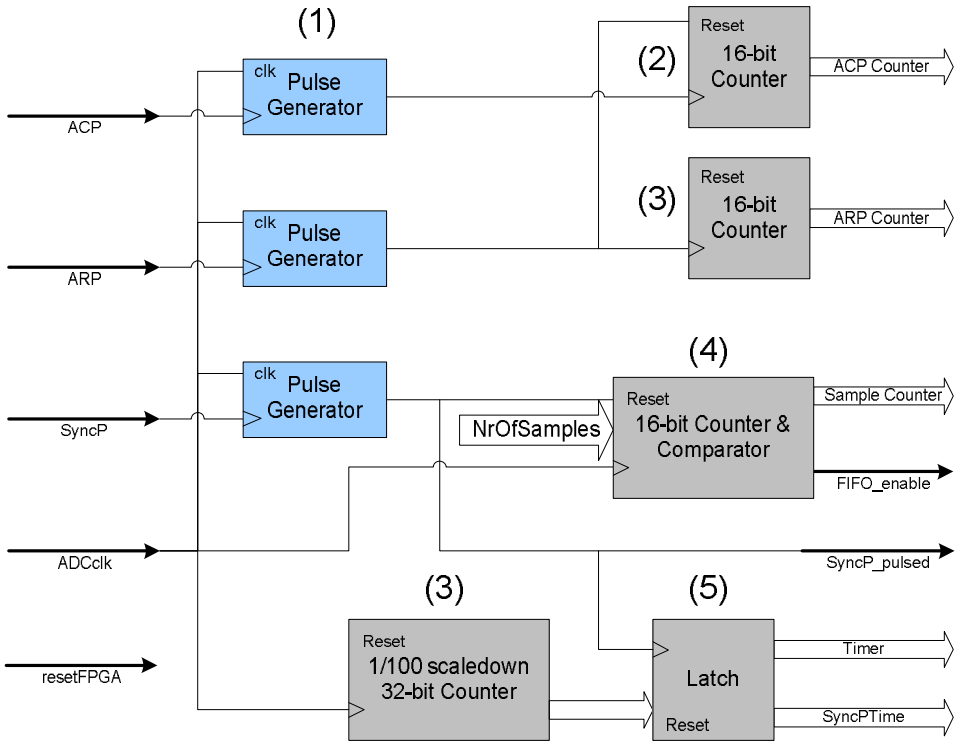

Figure 4.3 Block diagram of the CTB, the resetFPGA signal reset all counters.

1. The **PulseGenerator** sub architecture implement the “digital hysteresis” function that is used on the ARP, ACP and SyncP signals. The previous radar interface used a similar solution with the RS-422 receiver and it had occasional problems with counters triggered several times on a single noisy pulse. The extra digital hysteresis is designed so that it triggers on the rising edge of the input signal and generate a single clock cycle pulse. Then the pulse generator circuit wait until the input signal has gone low and stable for a number of ADCclk cycles before it can be triggered again. Signals that have passed though the “digital hysteresis” circuit get the name extension “_pulsed”.

2. The **ACP_count** process counts of the number of ACP pulses received since the last ARP pulse. It is implemented as a 16-bit counter that is trigged by the *ACP_pulsed* signal and is reset by the *ARP_pulsed* signal and the *reset* signals.

3. The **ARP_count** process keep count of the number of ARP pulses received and it is used for debugging purposes. It is implemented as a 16-bit counter that trigged by the *ARP_pulsed* signal and is reset by the *reset* signal.

4. The **time_count** process generate the timer data used for time stamping of the Synchronisation pulse, it is basically a scale down count of the ADCclk signal. The process uses two counters; an internal scale down counter as well as a time counter. The scale down counter is increased on rising edge on the *ADCclk* signal and when the counter reaches 100 the counter is zeroed and the time counter is increased one count. The scale down counter is an integer counter with range from 0 to 99 and the time counter is 32-bit long. The resolution of the counter is 1 Mhz and will overflow every 1h and 10 minutes when the ADCclk is running at 100 Mhz.

5. The **Sample_Counter** process counts the number of samples sampled by the ADC since the last received Synchronisation pulse. When the count is larger than the value of the NrOfSamples signal it will notify the DSG module to stop adding more ADC samples to the FIFO. The sample counter is a 16-bit counter that triggers on the ADCclk signal.

6. The **Time_latch** process stores the current timer counter value when the Synchronisation pulse is received.

The second module is the **DSG.** This module arranges SyncPTimer, azimuth and ADC data into a radar pulse data sequence and store that data sequence into the FIFO memory. The radar pulse data sequence is a format in which data from a single radar pulse is organized and it is illustrated in Figure 4.4.

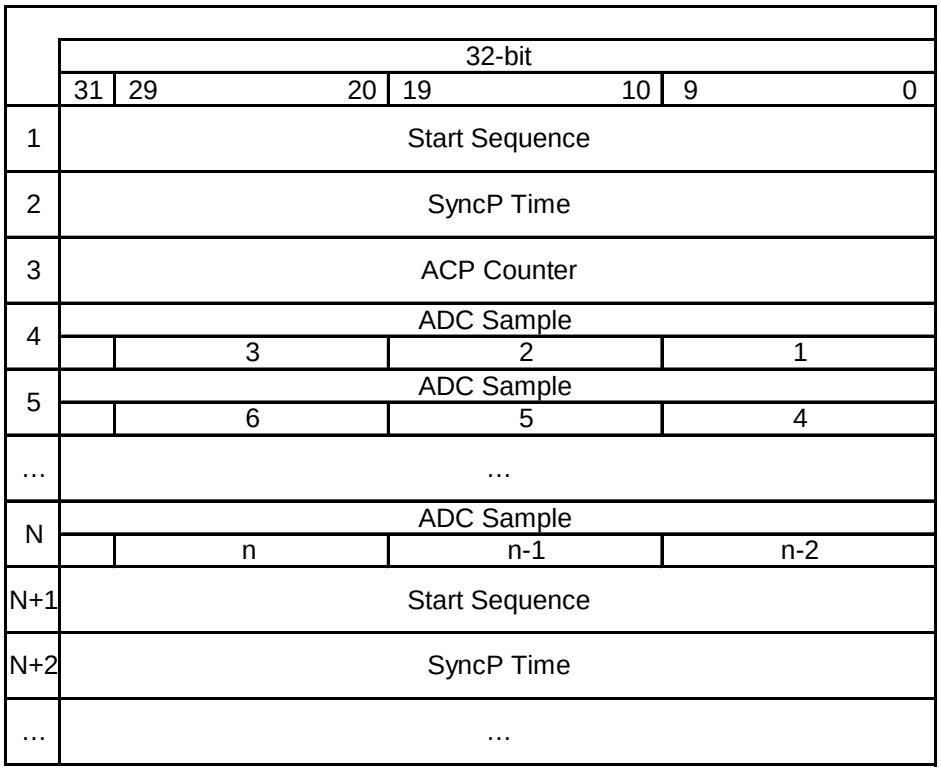

Figure 4.4 Illustration of the radar pulse data format in which data is sorted to the FIFO memory and transferred to Processor memory.

The module is constructed as a state machine with seven states which is written using a two-process architecture design pattern. The state machine shown in Figure 4.5

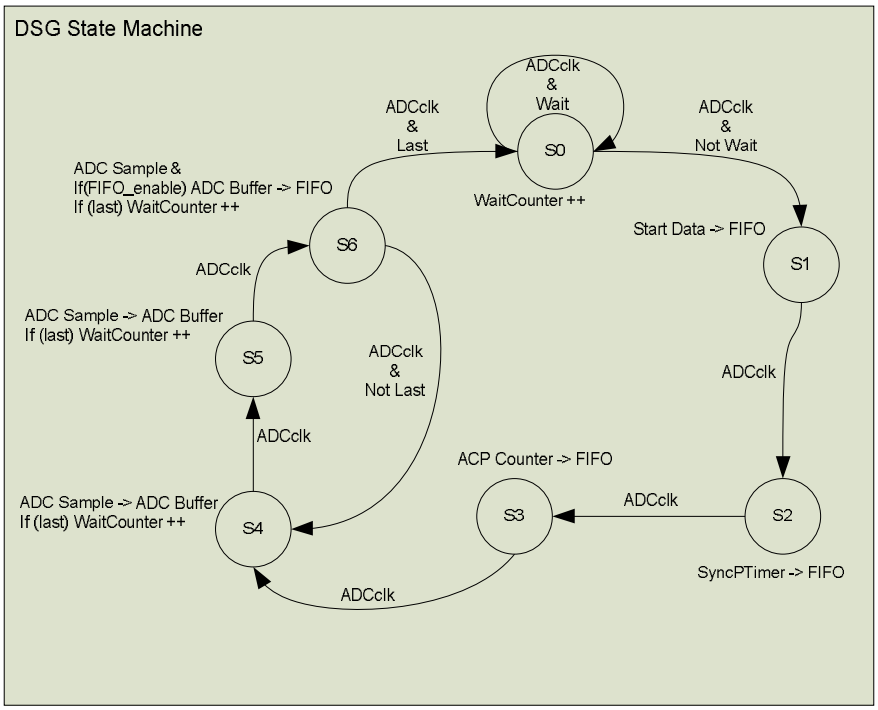

Figure 4.5 A description of the DSG State machine. Where state 1-3 writes the start sequence and state 4-6 writes ADC data to the FIFO, state 0 is a wait state.

The S0 wait state compensate for the pipeline delay introduced by the ADC. Then State S1 to S3 writes the start sequence, the Synchronisation pulse time and the ACP counter data to the FIFO. State S4 to S6, where three ADC samples are combined and written to the FIFO memory, are then repeated until the FIFO memory is ether disabled or if a new Synchronisation pulse is received.

The third module is the **FIFO-memory**. It is a dual clock FIFO IP module supplied with the Lattice development tool, ispLEVER. The FIFO is made as large as the FPGA can support. Hence the FIFO is made 32-bit wide and 2^{11} deep which makes it possible to store $3*2^{11} = 6144$ radar video samples (minus 9 samples per radar pulse which are lost due to the first three words in the radar pulse data format).

The fourth module is the **SBI**. This module is a modification of a VHDL file that came with the rattler card. The SBI act as a memory module to the LBC interface, the memory addresses is connected to internal FPGA signals and registers.

4.2. Radar Interface Card

The radar interface card (RIC) is an analogue piggyback card for the rattler module. The RIC is connected to the rattler board's expansion port. In addition to the physical radar interface, the RIC card functions as a power supply both to the RIC card and to the rattler board.

The description of the radar interface card is divided into four functional areas; the radar video, the synchronisation signal, the azimuth signals and the power supply. A full schematic of the electrical design of RIC is found in Appendix B.

Radar Video

The radar video signal path begins at the radar video BNC connector and end with the digital output of the ADC converter. The signal path is divided into 8 parts as illustrated in Figure 4.6 and each part is numbered and described in the text below.

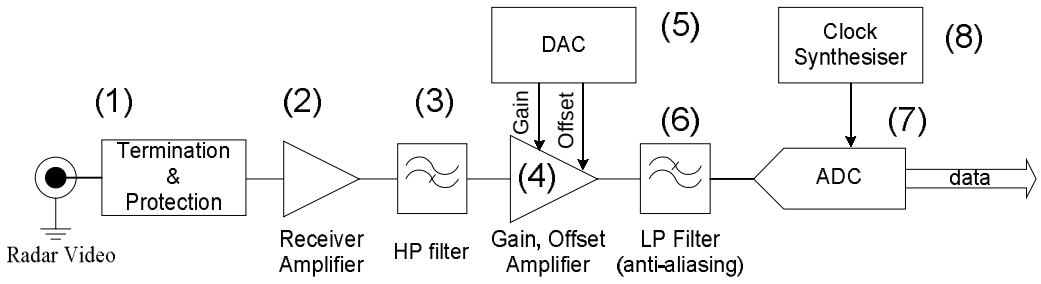

Figure 4.6 A illustration of the radar video path each numbered part is described in more detail below

1. The radar video is terminated using a 75 Ohm resistor. The input is protected using an ESD-protection diode that sinks both positive and negative over-voltages to ground.

2. The receiver amplifier is an Analog Devices Low cost 270 MHz Differential Receiver Amplifier[1]. It is used as a buffer amplifier with a 0 dB gain since the grounding design changed slightly. It would probably be removed from the design if the tests indicate that it is not needed.

3. The High pass filter is at this point not used since the optional high pass filter never was used on the old PCI radar receiver card. But in the design there is a space for a CR (Capacitor Resistor) high pass filter if it is considered to be needed.

[1] The Amplifier used has model number AD8130 (Analog Devices 2006)

4. The Gain Offset Amplifier is an Analog Devices 250 Mhz 4-Quadrant Multiplier circuit[1]. It is a very useful circuit that has the basic function of equation (4.1)

$$W = (X_1 - X_2) \times (Y_1 - Y_2) + Z \quad \textbf{(4.1)}$$

Where X and Y are differential inputs.
Z is a single ended input.
W is the output.

5. The Gain and Offset voltages are generated by the Analog Devices quad voltage output, 10-bit DAC[2]. The device output voltages are programmed from the PowerPC processor using an I^2C interface. The DAC also generate the threshold voltage for the synchronisation pulse.

6. As an anti-aliasing filter a RC filter is used with the cut off frequency around 50 MHz, that should be the absolute maximum frequency of the input signal. As the input noise of the system is unknown a RC filter is used. But a filter with better attenuation can be implemented later if needed.

7. The ADC is an Analog Devices 10-bit 105MSPS A/D Converter[3]. The device is configured for single ended input according to the reference design found in the data sheet.

8. The ADC clock generator is a Serially Programmable clock source from Integrated Circuit Systems ICS[4]. It can generate frequencies up to 200 Mhz thus covering the entire ADC frequency range, but since a input is an 10 Mhz crystal, the device will work best between 10 and 200 Mhz. It is programmed from the PowerPC processor using a three wire serial interface.

Synchronisation Pulse signal

The synchronisation pulse signal is connected to the RIC using a BNC connector and terminated using a 75 Ohm resistor. The input is also connected to the positive input of the MAX3096 RS-422 receiver, which is used as threshold detector. The DAC generated threshold signal is connected to the negative input of the RS-422 receiver. The output of the receiver is then routed to the rattler board.

[1] The Multiplier circuit used has model number AD835 (Analog Devices 2006)

[2] The DAC used has model number AD5315 (Analog Devices 2006)

[3] The ADC used has the model number AD9215 (Analog Devices 2006)

[4] The Clock generator used has model number ICS307M-02 (IDT 2006)

Azimuth signals

The two differential azimuth signals is connected to the circuit board using a 4-pin list connector and the signal is terminated using a 120 Ohm resistor and connected to the RS-422 receiver.

Power Supply

The power supply generates four voltages, the +5V, -5V, 3.3V and the 3V. All four voltages are generated from a single 5V DC supply. Table 4.1 shows a simple power budget with the stated power consumption of the different circuits, a safety margin of 2 is added to the stated consumption.

Table 4.1 Power budget calculated using the component's typical consumption together with a safety margin

Power Budget					
	Components	**Voltage [V]**	**Consumption [mA]**	**Margin**	**Demand [mA]**
	10bit 105 Msps ADC	3	55		
Sum 3V			**55**	**2**	**110**
	MULTIPLIER IC	5	25		
	Diff Receiver	5	11		
Sum +-5V			**36**	**2**	**72**
	DAC	3,3	20		
	Clock Synthesizer	3,3	30		
	RS-422	3,3	10		
	Rattler Board	3,3	1300		
Sum 3,3V			**1360**	**2**	**2720**

The 3V and the 3.3V are generated using voltage regulators[1] and the dual 5V is generated using a switched Traco 1W DC/DC converter[2].

[1] The regulators are the Torex XC6201 for the 3V and the National Semiconductor LP3876 for the 3,3V.

[2] The DC/DC converter is the Traco TSM0505D.

4.2.1. PCB

The first part of the PCB design is deciding the component footprints. If the footprint was not included in the Edwin database a new footprint was drawn using the recommended dimensions for the specific footprint. Since the rattler board and the RIC shall stack nice together, the RIC dimensions are decided to be the same as the rattler board's dimensions. The number of components and their complexity is quite small. In addition the board is decided to have four copper layers; the component layer, the ground layer, the power layer and the soldering layer. There is a lot of space for component placing, thus all components except the two rattler board connectors are placed on the component side of the board.

The ground plane is designed using a star-ground topography where four ground planes are connected together in a single connection point. This will minimize the noise transferred from noisy circuits to the sensitive analogue circuits.

The decoupling capacitors are placed as close to their component as possible and routed to the ground plain with as short leads as possible.

The digital output from the ADC is routed via 120 ohms resistors to minimize the current from the driving stage of the ADC, which is done according to the recommendations from the ADC data sheet. The complete PCB design is found in Appendix C

Grounding and Shielding

The FRI system is going to be placed in an EMI rich environment, thus the system needs to be well shielded. The electric fields can easily be shielded away by enclosing the system in a conduction shell, like a Faradays cage. If shielded cables are used and their shield is tightly connected to the shell the shield remains intact. A schematic description of the shield is illustrated in Figure 4.7. The ground inside the FRI box will be distributed from the RIC card to the chassis and rattler board.

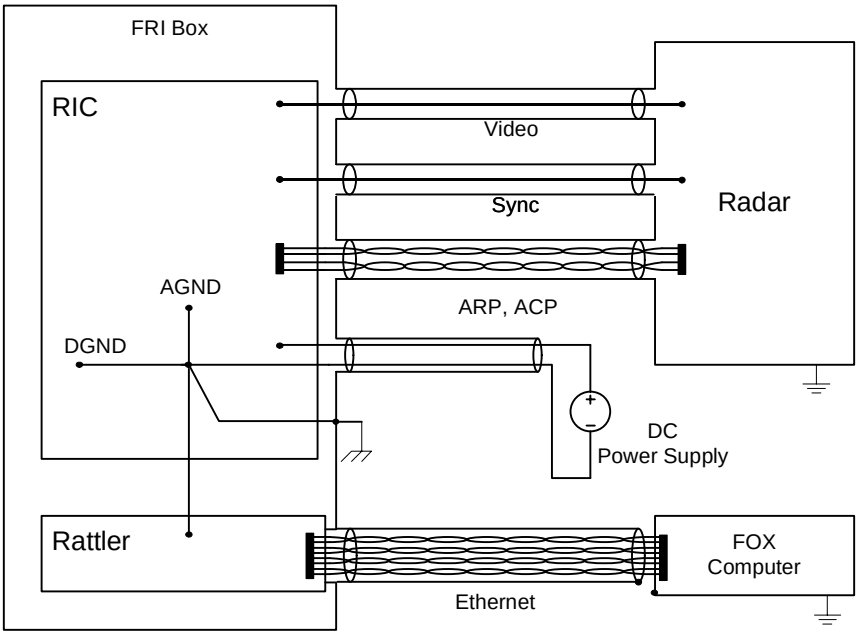

Figure 4.7 Ground and Shielding description of the FRI system, where a conducting shell around the FRI system can be seen.

4.3. Tests

4.3.1. MPC8347 Program

The PowerPC processor program is far from completed, but probably the most significant parts have been tested i.e. the operating system eCos. No benchmarking tests and hard real-time performance tests have been preformed on eCos. Up to this point only some functional tests verifying its functionality with several processes running in parallel have been run. The Ethernet capabilities where also tested to se if Ethernet communication over TCP/IP worked. Due to lack of time no Ethernet benchmarking tests have been done.

The three wire interface to the clock generator and the I^2C interface to the DAC on the RIC have not been implemented and tested because the RIC has not been manufactured yet.

4.3.2. Rattler FPGA

To verify the functionality of the FPGA program several tests and simulations have been preformed. All of the functionality could not be tested, this mainly because the development tool ispLEVER Starter did not include any simulation tools. Instead it relied entirely on "ModelSim" for simulations and since the evaluation version of "ModelSim" that was used did not work with ispLEVER, the design was only partially simulated. Functional Simulation could be performed on all modules except for the FIFO module. However, no timing simulation could be performed due to the incompatibility described above. Using the ispLEVER timing test, the requirement of a 100 MHz clock cycle was satisfied even for the most critical path of the FPGA.

CTB simulation

The block is simulated as a standalone module. The simulation data is generated in a ModelSim script file and then feed into the module inputs. The generated data is such that the functionality of the CTB block could be confirmed.

DSG simulation.

The input to the DSG was generated using arbitrary input data to test the transition between the different states in the state machine and the timing of the output signals.

A weakness found in the DSG is that when a synchronisation pulse is received in any of the state s1 s2 s3 there will be ADC data losses. However, this can only happen if two synchronisation pulses are received within 6 clock cycles, which should not happen and in such a case also should be prevented by the "digital hysteresis" function. Additionally, there are some uncertainness about the timing of the data output and the FIFO input, but since no timing simulations could be carried out this has to be tested further.

SBI Test.

The SBI interface which was delivered with the rattler board was believed to work optimally. In this perspective only the new function was tested using the processor as testbench.

A problem was found with the FIFO read functionality; several data words were missed when reading from the FIFO memory. This problem was derived from how the communication between the SBI and the processor LBC worked. The LBC and SBI are configured to wait a couple of clock cycles when reading from and writing to the SBI. Hence, more data was clocked out from the FIFO since it was clocked directly by the LBC clock. To solve this problem a non-optimal solution was used to clock out new data from the FIFO memory. This alternative solution uses two memory addresses and when both these addresses are read from, a new FIFO data is clocked out. As the time was scarce a modification of the SBI that did not require the “wait clock cycles” was not done. However as this is a time critical point of the system a modification is required.

4.3.3. Radar interface Card

The radar interface card has not yet been tested because the manufacturing of the card has been delayed. The card is designed to be easily tested. The signal path of the radar video is divided into five stages with zero ohm resistors in-between, thus making it possible to test the construction one stage at the time. There are also zero ohm resistors from the power supply, so each stage of the power can be controlled and tested. All signals of interest also have test pads thus making signal measurements easy.

4.4. FRI Costs

The cost of the FRI prototype system is presented in Table 4.2 and the component cost is calculated from the single unit price. Since the Manufacturing and assembly of the circuit board is not complete the price is not known. All costs will be dramatically reduced if the FRI system will be serially produced.

Table 4.2 FRI prototype system costs, not including the RIC prototype circuit board and assembly

RIC components	640
Circuit Board + Assembly	?
Rattler Board	6300
Sum	**6940**

5. Conclusions

The conclusion of the thesis project is that it is possible to use an external radar interface to the FOX system. The best communication solution between the external radar interface and the FOX computer is Gbit Ethernet, which will give a long range over standard cables with a widely spread technology.

The time plan that was drawn up in the beginning of the project did not hold because the design phase took more time than expected, and because extended time spend on finding a manufacturer and manufacturing the RIC circuit board.
The main reason for the design phase delays was that it took longer than expected to research and decide which components that should be used, but also since a lot of excess time where spend on finding a suitable CAD software and learning it.

The goal of this thesis project was to design and construct a working prototype of the FRI system. But since the time of this project has run out, all the goals the project cannot be completed. Therefore to complete the FRI system further work is needed and that is declared in the next section “further work”.

6. Further work

Rattler board

The PowerPC program remains to be implemented likewise the design and implementation of the rattler to FOX communication protocol at which data will be transmitted over the UDP/IP network. The SBI to LBC communication need to be optimized in order to increase data through put.

Additional tests on the FPGA program are necessary since the simulations were not completely satisfactory. To be able to test the FPGA program further, a test module that connects to the expansion port of the rattler board could be used. This module would generate the required signals using a computer parallel port, thus making the input fully controllable. Although this can not be done at full speed, it will be possible to demonstrate the functionality of the FPGA program including the FIFO memory.

Radar interface card

The radar interface card remains to be manufactured and tested.

FOX

The FRI interface program module needs to be designed and implemented in FOX.

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Appendix A

Specification

Tj-ställe/Utgivare
L/SAF, Jakob Sönnerstam

Datum
2006-05-29

Mottagare

Tj-ställe/Fastställd

Informationsklass
Intern

SRS
Extern radarinsamlingsenhet

Examensarbete

Innehållsförteckning

Versionshistorik

Version	Datum	Beskrivning
0.1	2006-05-29	Diskussionsunderlag
0.2	2006-06-08	Enligt möte, Carl Jakobsson
0.5	2006-06-30	Uppdaterad, Carl Jakobsson

Referenser

1. Beskrivning av examensarbete – Mobil A/D-omvandlare, Mattias Liljenberg, Saab AB, 2006.

Förkortningar

Begrepp	Förklaring
ACP	Bäringspuls
ARP	Norrpuls
PRF	Pulsrepetitionsfrekvens

1 Inledning

1.1 Identifiering

Denna specifikation definierar den externa radarinsamlingsenheten.

1.2 Översikt

Den externa radarinsamlingsenheten utformas för att användas som datainsamlingsenhet till radarextraktorn FOX. Arbetet sker inom ramen för ett examensarbete vid Chalmers tekniska högskola, institutionen för Signaler och System.

2 Funktionskrav

2.1 Dataöverföring

§ 2.1.1 Varje puls skall tidsstämplas med en 1MHz 32 bitars räknare.

§ 2.1.2 Varje puls skall riktningsstämplas med en ACP 16 bitars räknare.

§ 2.1.3 ARP pulserna skall räknas i en 16 bitars räknare som skall kunna avläsas från FOX för felsöknings ändamål.

§ 2.1.4 Radarinsamlingsenheten skall överföra data till radarextraktorn FOX via Gigabit Ethernet.

2.2 Signalbehandling

§ 2.2.1 Radarinsamlingsenheten skall sampla råradarvideo med en samplingsfrekvens på 50+ MHz och med en upplösning på 8-10 bitar.

§ 2.2.2 Radarinsamlingsenheten skall ha tillräcklig kapacitet för en PRF på 12 kHz.

§ 2.2.3 Radarinsamlingsenheten skall ha kapacitet för att ta emot upp till 4096 bäringspulser per antennvarv vid rotationshastigheter på upp till 60 varv/min.

§ 2.2.4 Radarinsamlingsenheten skall ha en låg brusnivå.

§ 2.2.5 Radarinsamlingsenheten bör ha funktion för variabel samplingsfrekvens. Funktionen skall säkerställa att toppar i mottagen video registreras.

§ 2.2.6 Radarinsamlingsenheten bör ha logik för att kunna avgöra om synkroniseringspuls och bäringspulser ligger inom angivna gränser samt funktion för att sätta dessa gränser.

§ 2.2.7 Radarinsamlingsenheten bör ha funktion för att ställa in känsligheten för bäringssignalerna.

2.3 Övrigt

§ 2.3.1 Hårdvaran skall ha ett läsbart unikt serienummer.

§ 2.3.2 Hårdvaran bör kunna övervaka och rapportera fel på insignaler.

3 Gränsytekrav

3.1 Gränsyta mot radar

§ 3.1.1 Radarinsamlingsenheten skall ha två BNC-anslutningar för inkoppling av rådararvideo och synkroniseringspuls samt en D-sub-anslutning för bäringspulser.

§ 3.1.2 Radarinsamlingsenhetens anslutningar skall ha följande karakteristik.

Signal	Information	Signalkarakteristik
Råvideo	Råradarvideo	5V, 75 Ω
Synkpuls	Synkroniseringspuls	1,3V_{TH}, 75 Ω
ARP	Norrpuls	RS422A, 120 Ω
ACP	Bäringsräknare	RS422A, 120 Ω

3.2 Gränsyta mot FOX

§ 3.2.2 Data från radarinsamlingsenheten skall göras tillgänglig för FOX via en modul.

4 Konstruktionskrav

§ 4.1 Modul till radarextraktorn FOX skall skrivas i C++.

5 Dokumentationskrav

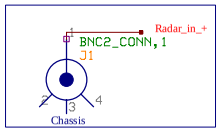
§ 5.1 Utvecklingsarbetet skall redovisas i en teknisk rapport, författad på ett sätt som uppfyller kraven för en examensarbetsrapport vid Chalmers tekniska högskola, Institutionen för Signaler och System.

6 Leveranskrav

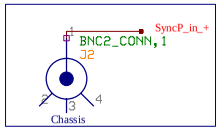
§ 6.1 Radarinsamlingsenheten skall levereras den 13 oktober 2006.

Appendix B

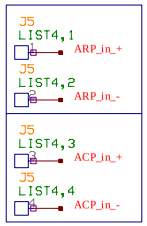
Schematics



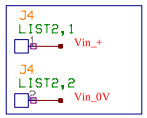
BNC Radar in



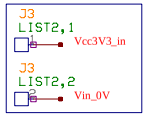
BNC SyncP in



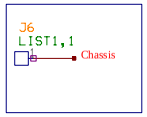
D-Sub ARP & ACP in



Power Connector 12-20V

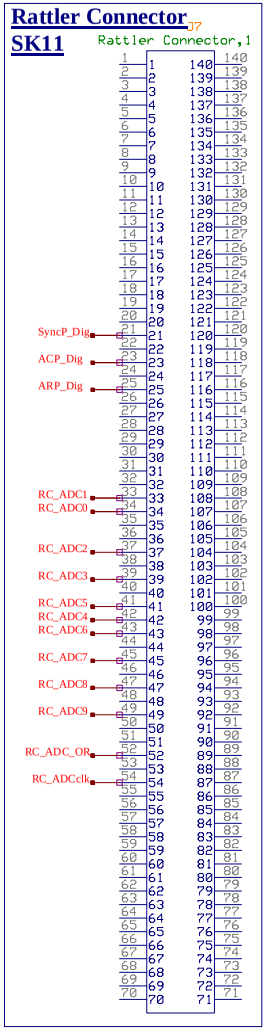


Power Connector 3,3V to Rattler

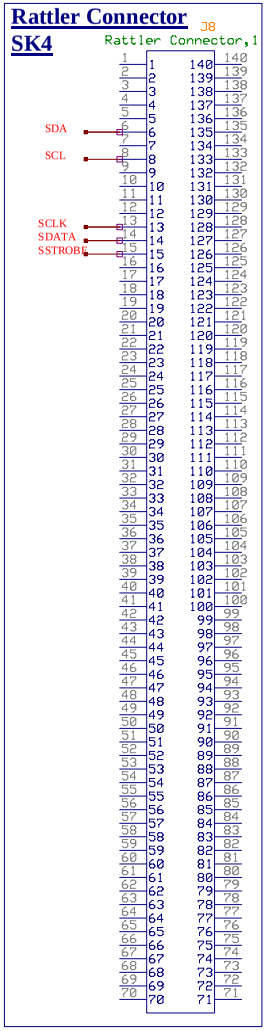


Chassis Ground Connector

Rattler Connector SK11



Rattler Connector SK4



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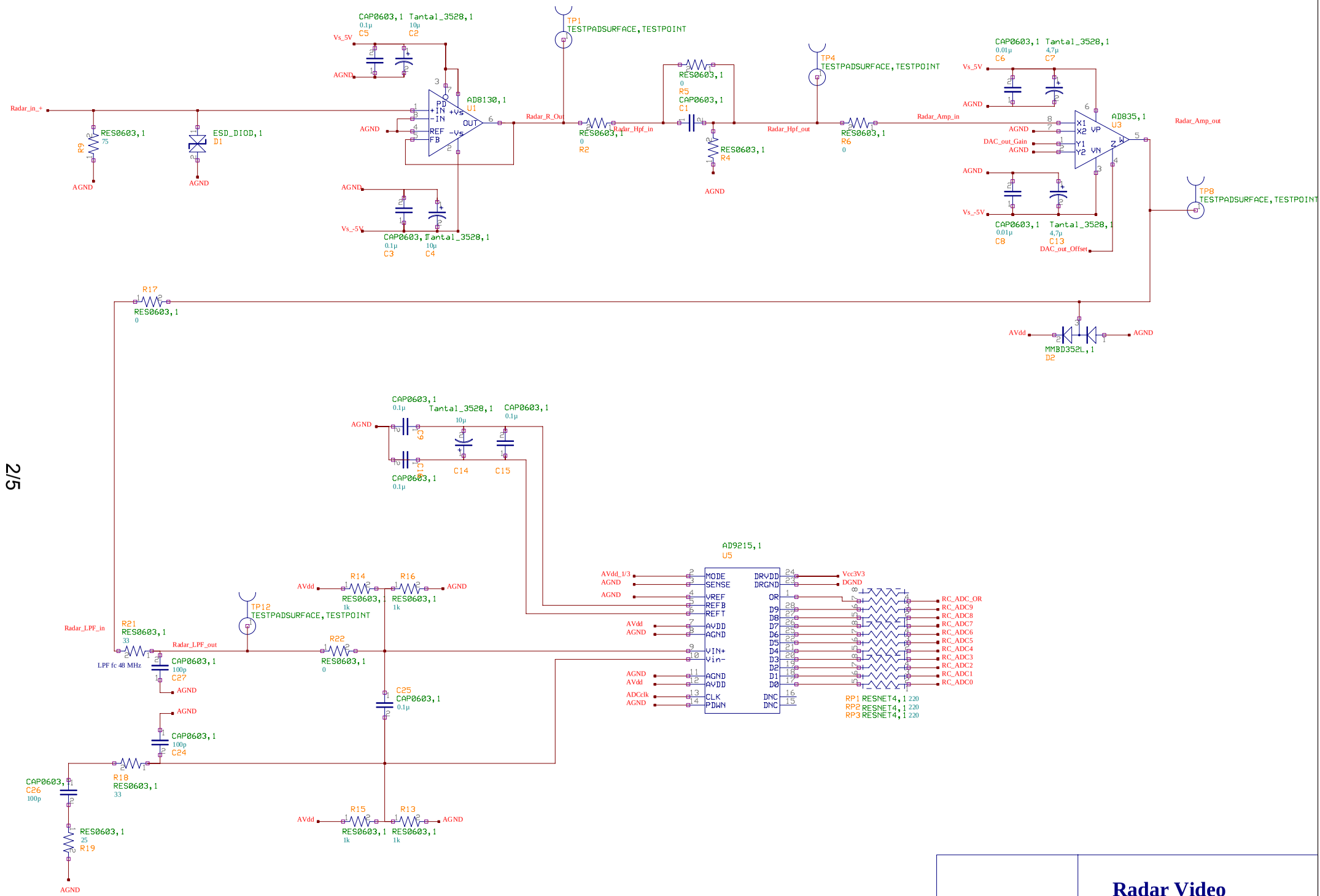
Main Page

Date : 2006-10-05

By: Carl Jakobsson



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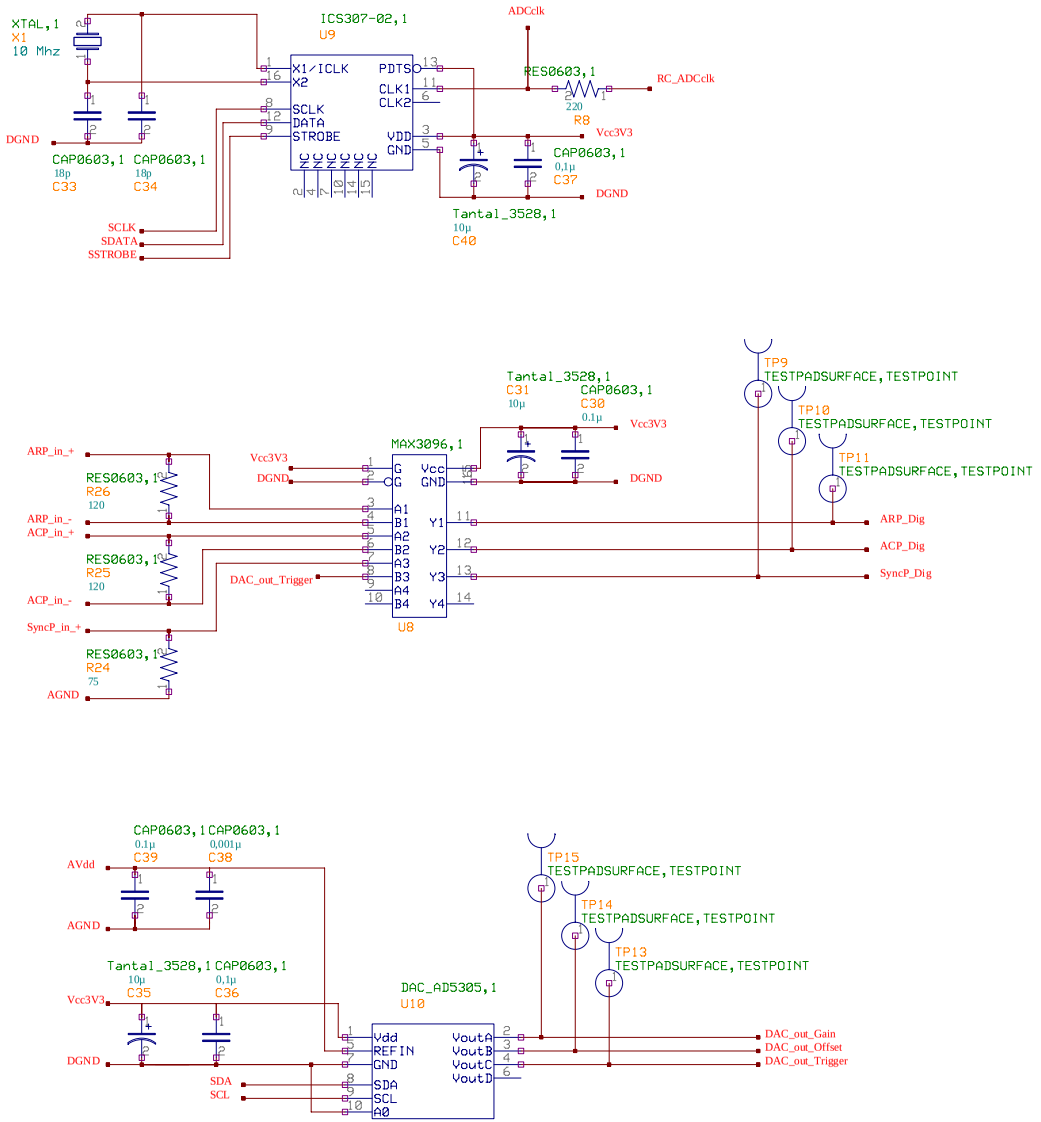
By: Carl Jakobsson	**Page 2/4**



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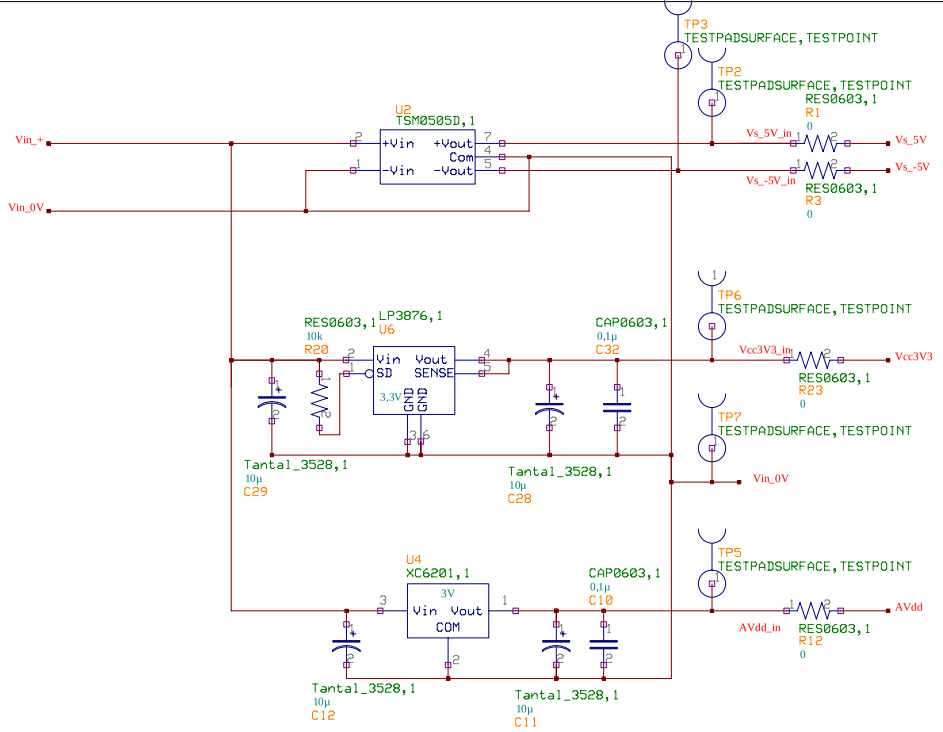
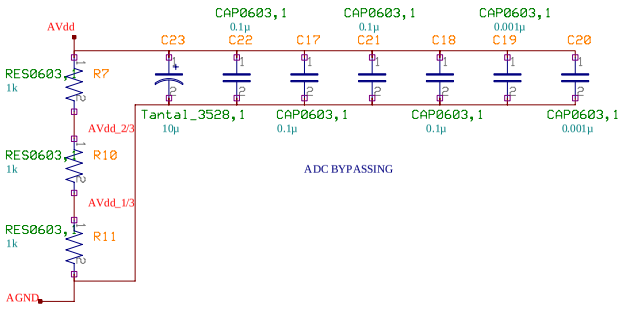
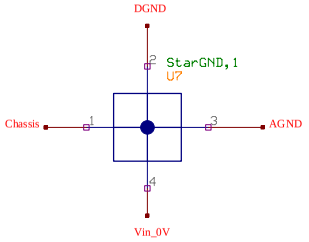
Date : 2006-10-05	
By: Carl Jakobsson	**Page 3/4**







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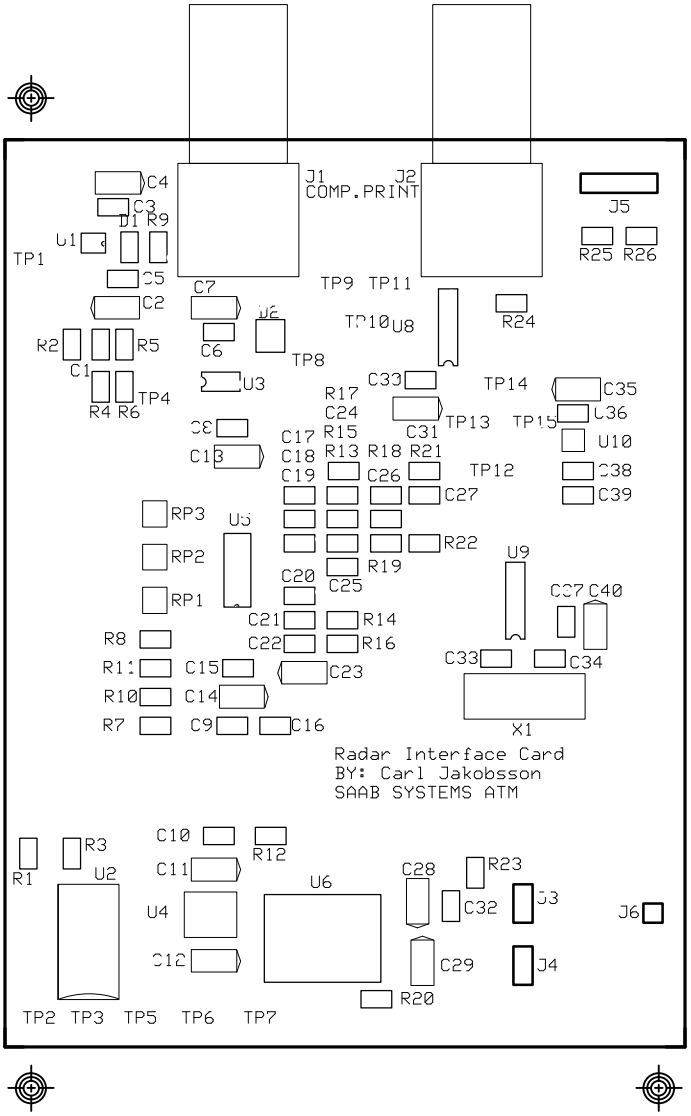
By: Carl Jakobsson	**Page 4/4**

Appendix C

PCB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J2
J5
C4
C3
D1
R9
U1
TP1
C5
C7
C2
U7
TP9
TP11
TP10
U8
R24
R25
R26
R2
R5
C6
TP8
C1
U3
C33
TP14
C35
R4
R6
TP4
R17
C24
TP13
TP15
U36
C31
U10
C17
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C18
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R21
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C26
TP12
C38
C27
C39
RP3
U5
RP2
R22
U9
R19
C20
C25
RP1
C21
R14
C37
C40
C22
R16
R8
C33
C34
R11
C15
C23
R10
C14
R7
C9
C16
X1
Radar Interface Card
BY: Carl Jakobsson
SAAB SYSTEMS ATM
C10
R12
R3
R1
U2
C11
U6
C28
R23
U4
C32
J3
J6
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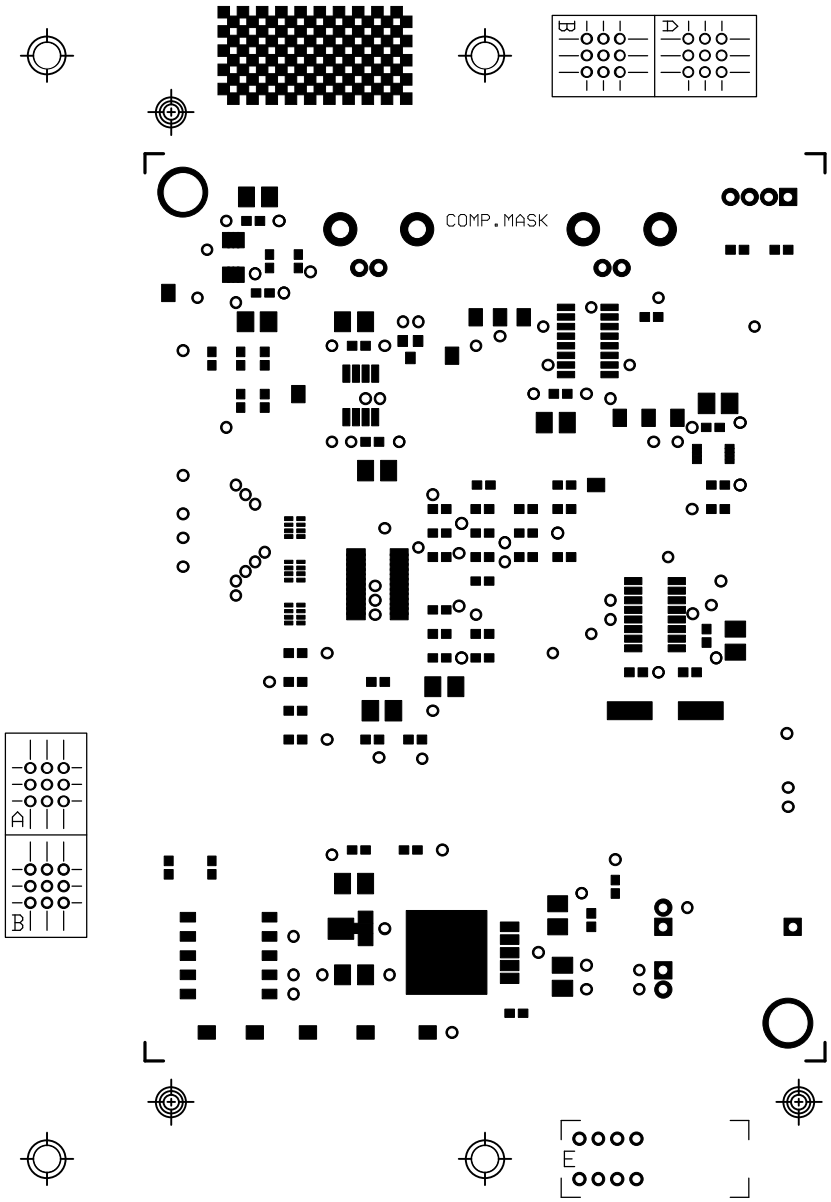
C29
J4
R20
TP2
TP3
TP5
TP6
TP7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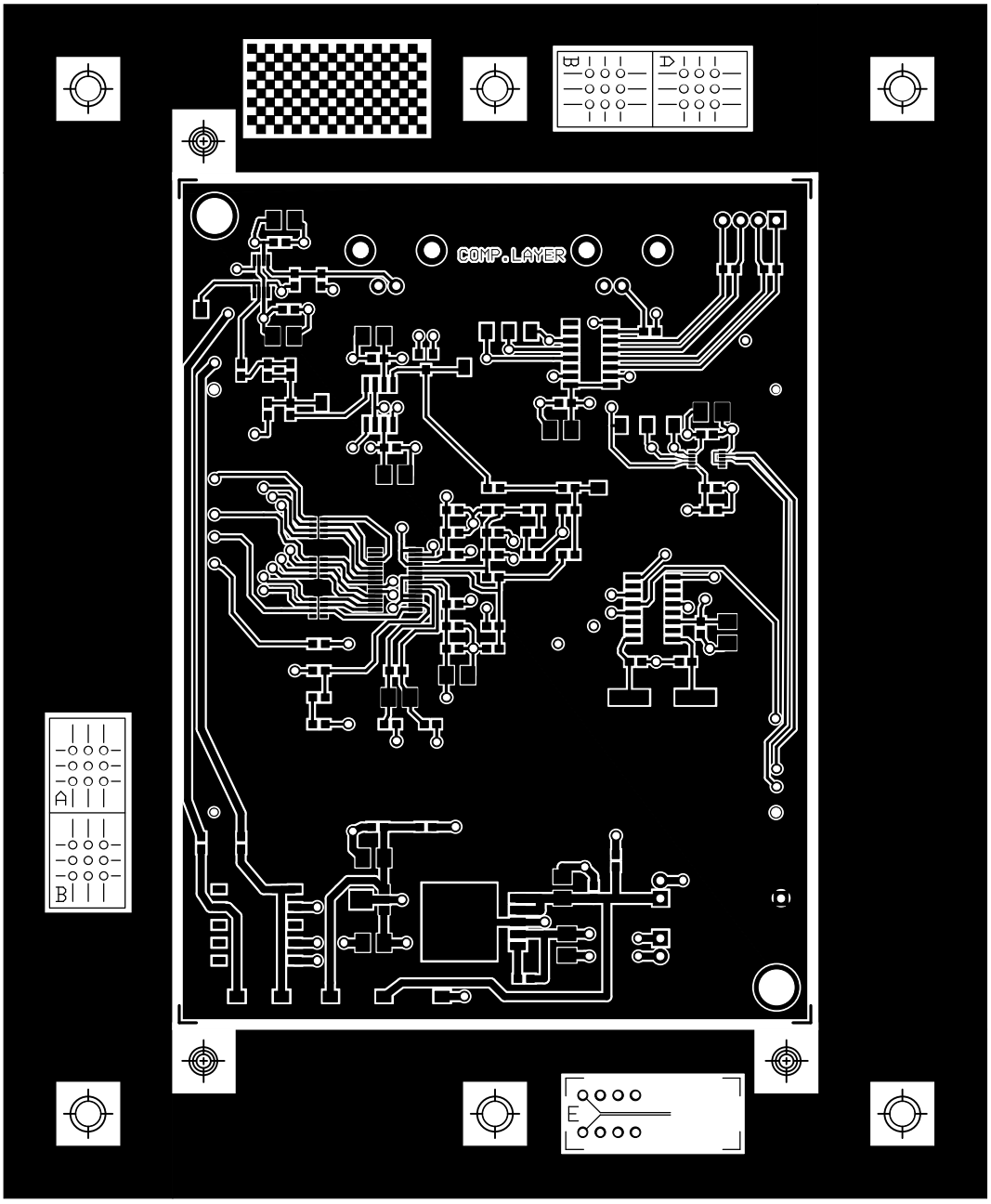
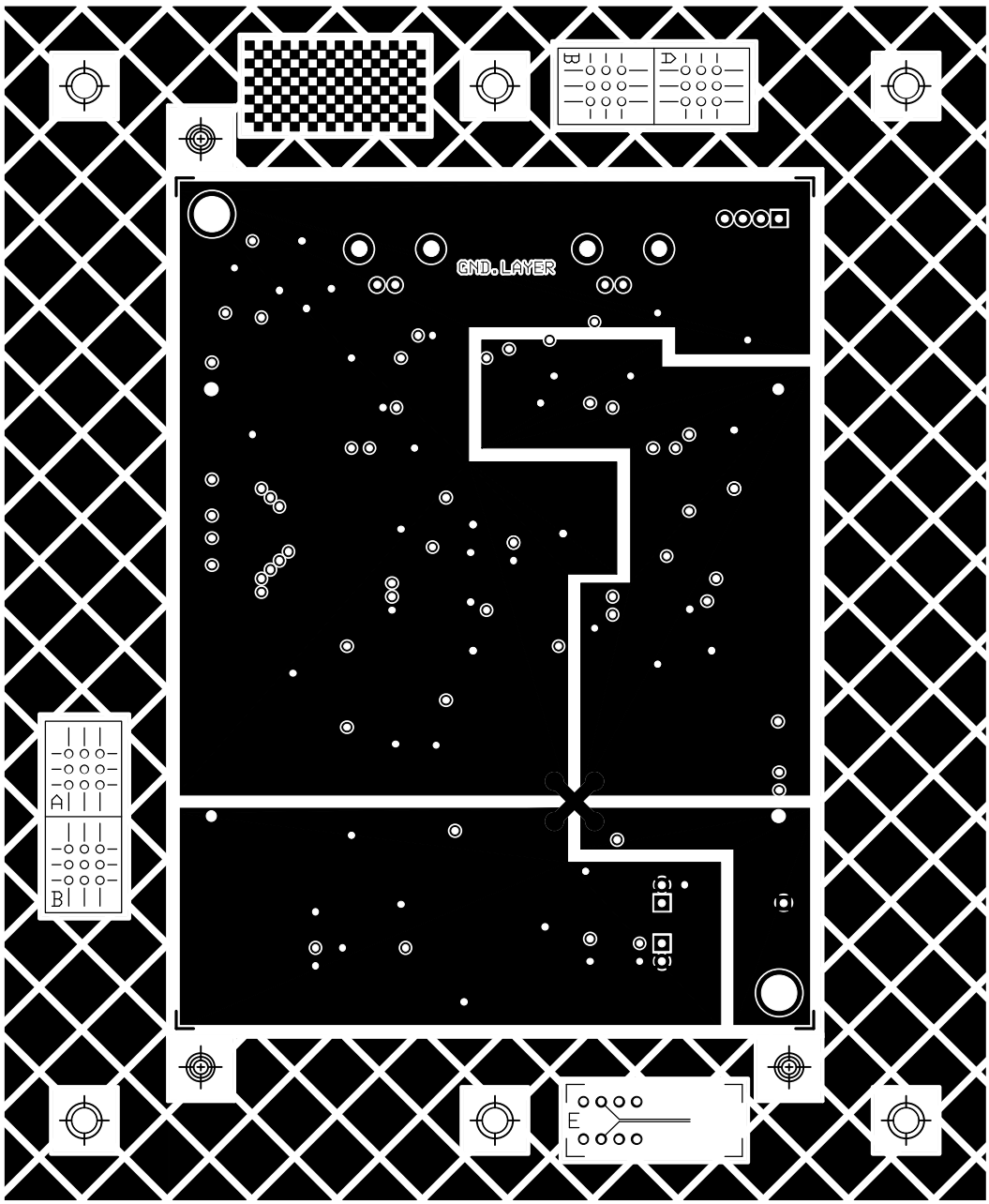
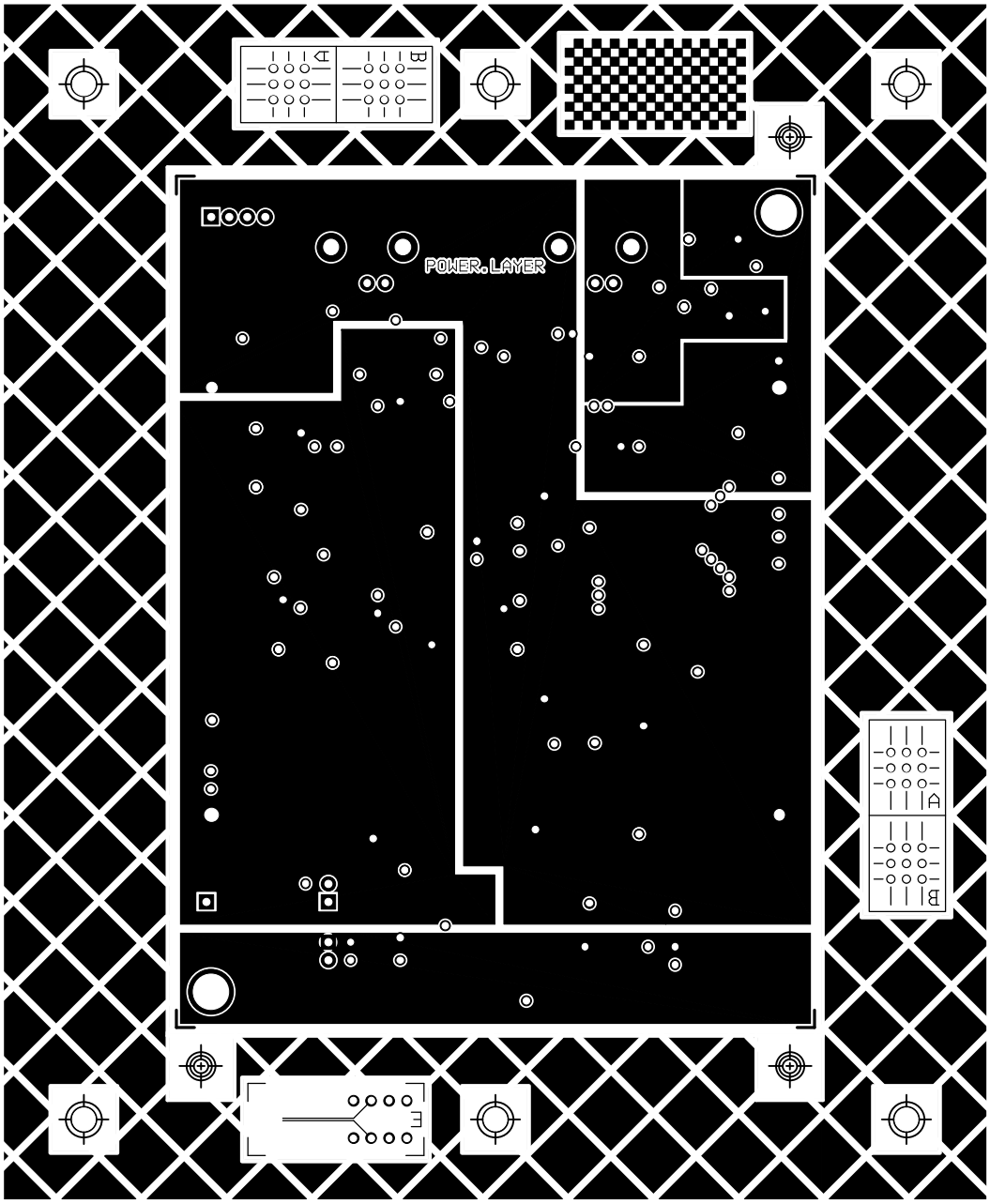
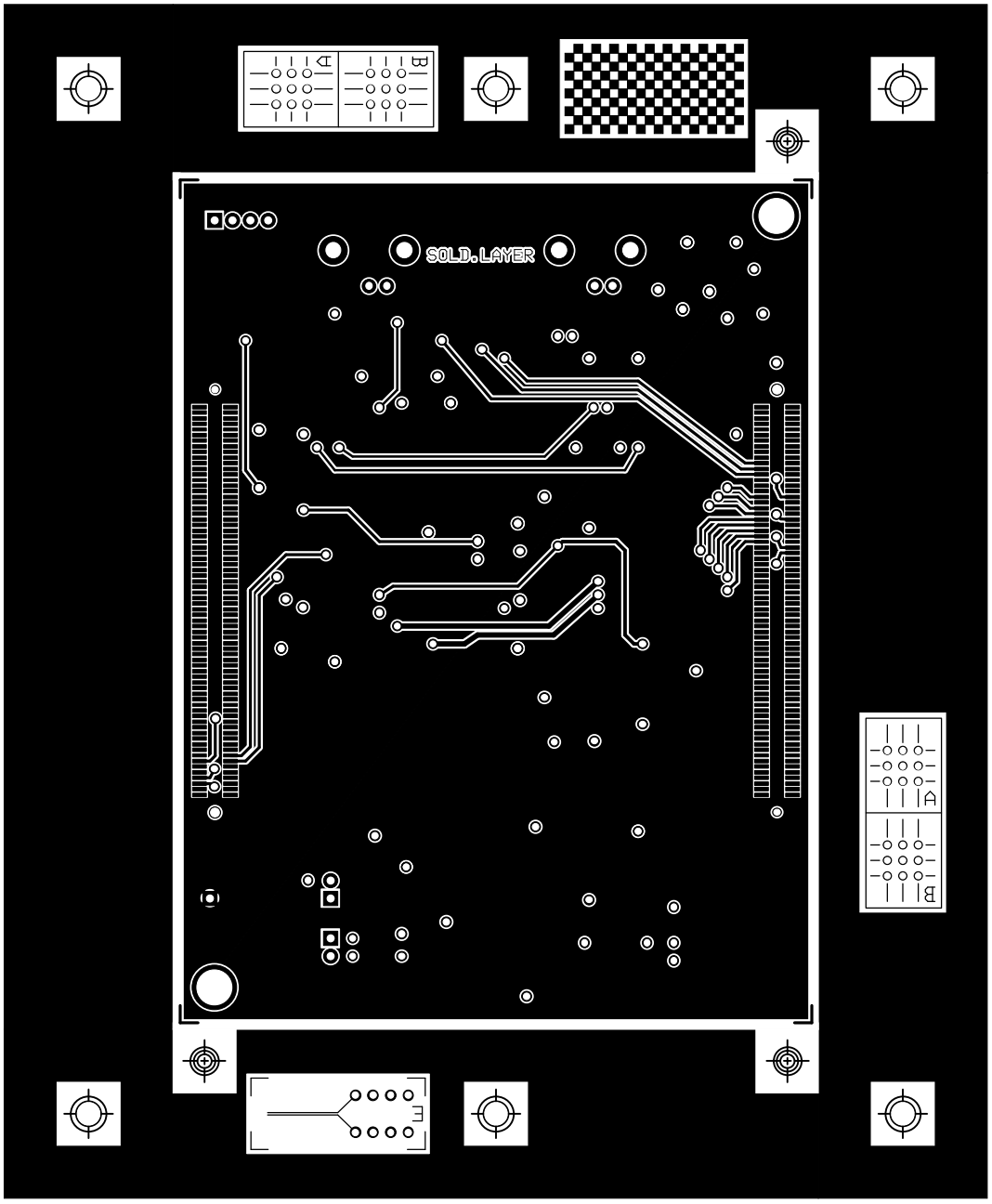
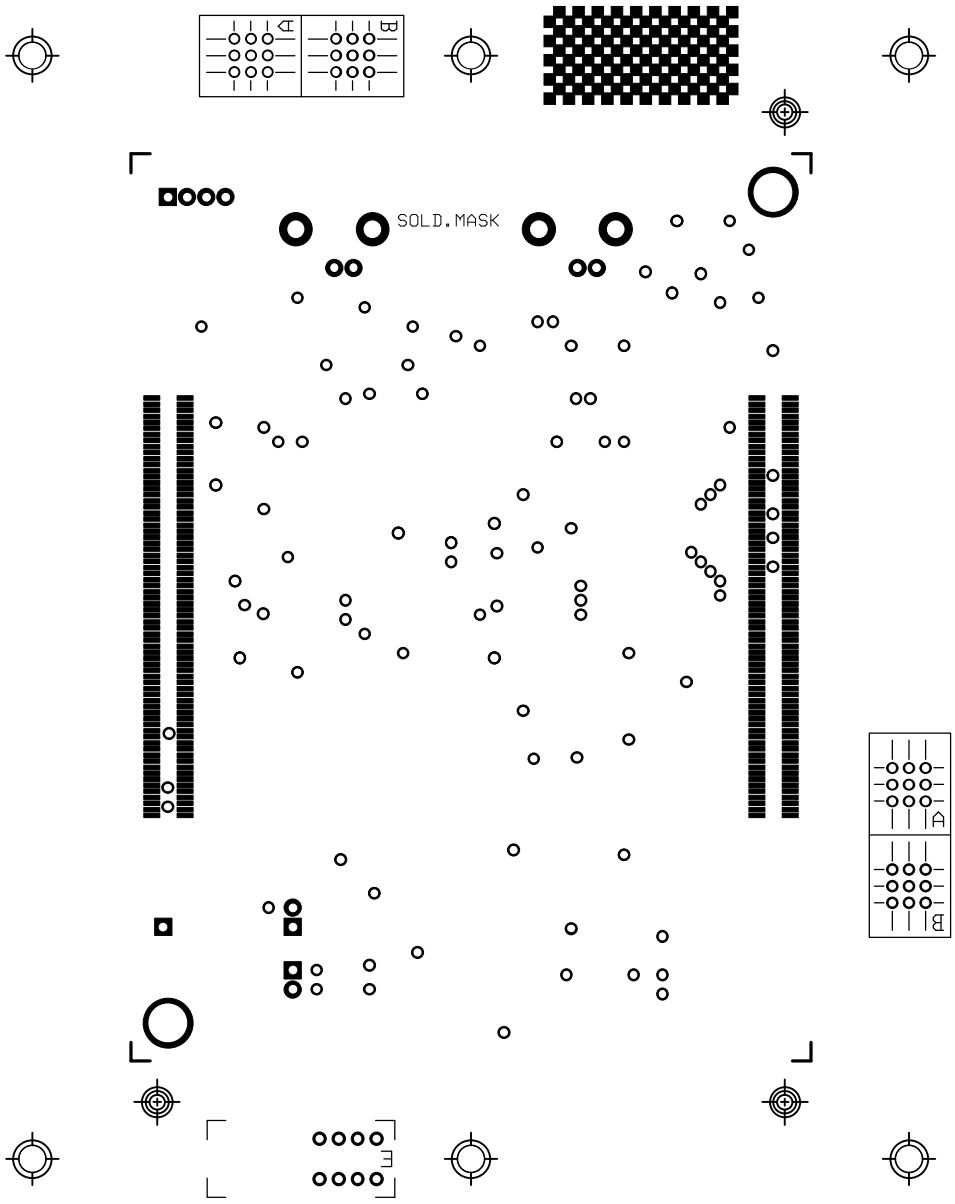
B
B
D
E

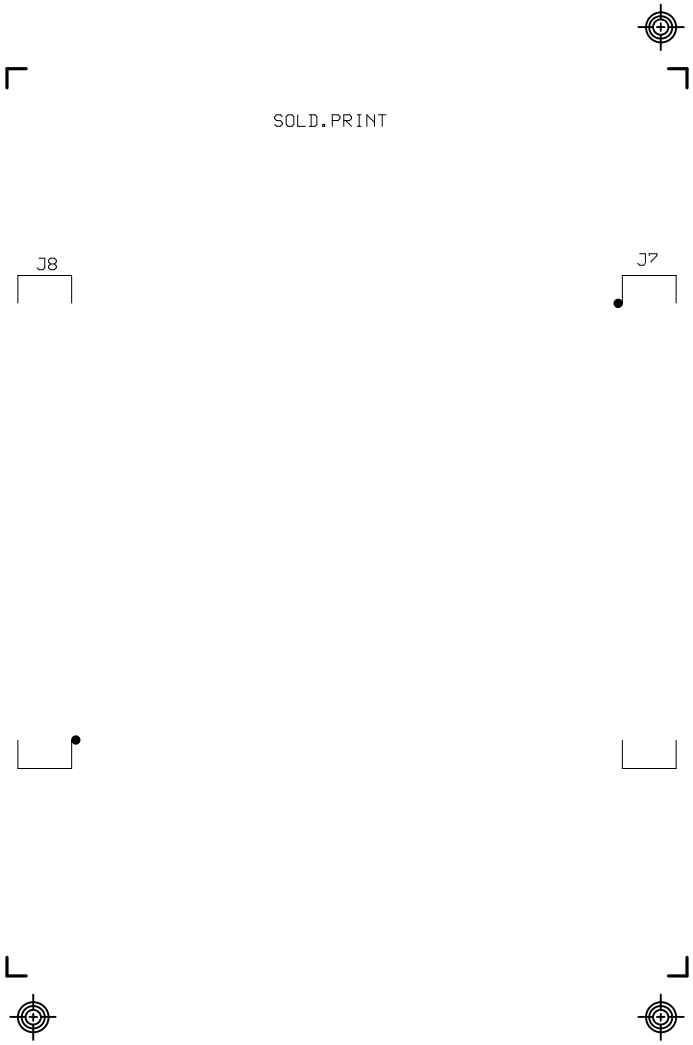

COMP.LAYER
A
B
C
D
E


GND.LAYER
C
D
A
B
E


POWER.LAYER


SOLD. LAYER


SOLD.MASK


SOLD.PRINT
J8
J7