THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Converter-Interfaced Distributed Generation – Grid Interconnection Issues

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To my family

Converter-Interfaced Distributed Generation –
Grid Interconnection Issues

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Abstract

Distributed generation (DG) with a converter interface to the grid is found in many of the green power resources applications. In this thesis, the control of a voltage source converter (VSC), as the DG front end, is in focus regarding the power quality problems that could appear at the connection point. The aims have been set to maintain a stable operation of the DG, in case of network disturbances, and to react in a corrective way during different grid operating conditions (e.g. in case of voltage dips). For this purpose, vector current controllers have been implemented with two different line filters; namely an inductance filter (L-filter) and an inductance-capacitance-inductance filter (LCL-filter). The controllers have incorporated: one sample time delay compensation, limitation of the reference voltage to avoid saturation, an integrator anti-windup, a DC-link voltage controller, a PCC voltage regulator, and an islanding detection algorithm.

The ride-through capability of the DG has been examined against a variety of possible voltage dips that could appear at the connection point. Moreover, the capability of the DG to compensate for the voltage at the connection point has been studied. Finally, the intentional islanding has been considered, where the DG is allowed to energize a part of the grid in case of the utility outage forming what is called an island.

The results found are that the effect of unbalanced voltage dips on the DC-link voltage ripple is minimized if the oscillating powers, produced during that period, are supplied by the grid side instead of the DC-side. Moreover, design equations have been derived in order to calculate the maximum currents that would flow through the VSC valves during voltage dips. These equations are to be used in designing VSC's with voltage dips ride-through capability. In addition, a neural-network based PLL, which extracts the phase angle of the fundamental component of the grid voltage, has been introduced in order to provide better performance in case of a DG with voltage compensation capability. Finally, combining the voltage regulator with the estimated frequency as a measure for islanding condition has, in this work, been found as an appropriate practice, to detect islanding, especially in the case of weak grids.

***Keywords**:* distributed generation, harmonics, intentional islanding, L-filter, LCL-filter, power quality, strong grid, vector control, voltage dips, voltage regulation, VSC, weak grid.

Acknowledgment

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Fainan Abdul-Magueed Hassan

Gothenburg, Sweden,

September, 2007.

Table of Contents

Chapter 1

Introduction

1.1 Motivation

The consumption of electrical energy is an ever growing need worldwide. Yet, growing in tandem to it are concerns about environmental pollution, global warming and the steady depletion of fossil fuels. Electricity generation from renewable resources might be considered as a feasible solution for the next generations [1].

Traditional power systems implement large power generation plants that produce most of the power, which then is transmitted to large consumption centres and further distributed between different customers. This power system design structure has, at some locations, started to change [2] towards new scenarios at which distributed generation (DG) units are spread throughout the distribution network, as shown in Fig. 1.1 for two possible locations. These DGs utilize renewable resources such as wind turbines, photovoltaics, biomass, small hydro-turbines … etc. Beside their environmental benefits, DGs offer a low-cost way for the energy flow into the market since they do not imply substantial transmission losses due to their location near to the customers [3]. Moreover, they could present a reliable and uninterruptible source for the customers especially in rural areas [4] and micro grids [5]. In addition, a possibility where the DG could be beneficial is if it could help to supply load during contingencies until the utility can build up additional delivery capacity [6].

More advantages are introduced using power electronics interfaced DGs [7]. For instance, converter interfaced DGs can be designed to provide ancillary services to the utility; such as reactive power support, load balancing, voltage support, and harmonic mitigation [3]. Moreover, such DGs can be more energy efficient in the sense that they can provide more

energy production, more smooth power production (less dependent on the prime source variations), and controlled energy storage [9].

In addition to the above advantages, the integration of DGs is, to a large extent, owed to political decisions in many countries. For instance, the Swedish government has introduced a legislation (2003:113), which intended to encourage and increase the proportion of electricity produced from renewable resources [8]. The objective is that the amount of electricity produced from renewable resources will provide additional power of about 6.5% of the present total production by the year 2010.

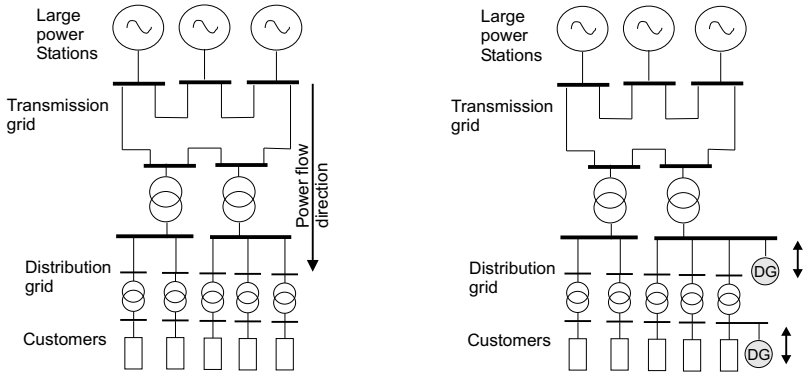

Fig. 1.1 Traditional power system (left) and penetration of distributed generation (right). The arrows present the power flow direction.

Even though large-scale implementation of DGs has several driving forces as mentioned above, there are major challenges concerning network interconnection issues that have to be solved. Grid connection of DGs is considered from two main prospects: power-system prospective and DG-technology prospective. As it is an essential part for the integration of DGs to achieve a reliable and improved performance of the power system, the DG interface to the grid is of focus in this work.

1.2 Background and related work

Background

Power conversion systems of distributed generation (DG) vary according to the nature of the input energy source. They may be implemented by using partially rated power electronics interface, as in wind turbine systems with doubly fed induction generators, or with fully rated power electronics interface [7]. The latter interface is the dominating one in applications related to fuel cells, solar cells, micro turbines and wind turbine systems [9]. There can be one or more power conversion stages in order to adjust the power of the energy source with the grid requirements, as shown in Fig. 1.2 [9]. With DC energy sources, the power electronics interface may consist of one DC/AC converter, or an intermediate DC/DC conversion stage can be added to achieve a specific goal, e.g. in order to regulate the output voltage so that the maximum available power is extracted [9]. The same is valid for AC sources, where they have to be adjusted to match the grid requirement by a DC intermediate stage. An energy storage unit could also be connected in the DC stage to adjust the energy injected into the utility grid in all operating conditions. The focus here will be on DG systems with a DC/AC power converter as a front end, where the DC-link voltage is either controllable or constant and the primary source input power is constant. The power converter to the grid enables a fast control over active and reactive power and could perform voltage and frequency control [10], [11]. Observe that, in order to control the active power, the primary source needs also to be controllable or an energy storage should be provided.

Voltage source converters (VSCs) using insulated gate bipolar transistor (IGBT) switches that are controlled by pulse width modulation (PWM) are used on the grid side at medium/high voltage due to their high controllability and low losses [12], [13], [14]. The good controllability promotes the use of the VSCs in grid connected applications to provide good power quality. An inherent part of a VSC is a filter inductor (L-filter), which is used to minimize the current harmonics injected into the grid [15] - [20].

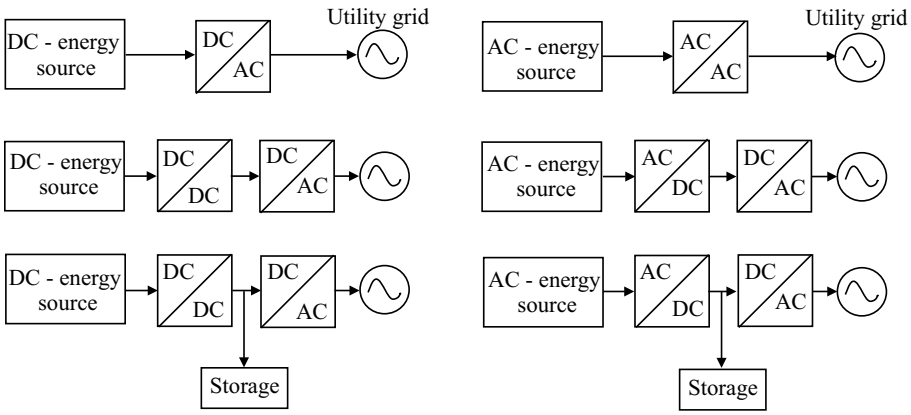

Fig. 1.2 Full-rated power electronics interfaced DG systems.

Like most of the power electronics equipment, an important drawback of using VSCs is their sensitivity to voltage disturbances, e.g. voltage dips [21]. In order to keep the DC-link voltage constant and minimize the grid current amplitude and harmonics during faults, the VSC controller is required to have two main functions: DC-link voltage regulation and current control. Most conventional current controllers have been designed under the assumption of balanced grid voltages [16]. These controllers show undesirable current control characteristics under unbalanced conditions because the current references are distorted by a second-order harmonic [16]. This is due to the negative-sequence voltage in the three-phase domain, which translates into a sinusoidal signal having a frequency of twice the grid frequency in a *dq*-frame synchronized with the positive-sequence voltage.

Related work

A comparison between different types of current controllers (CCs) for shunt-connected VSC based on their transient operation in case of voltage dips is presented in [17]. It has been shown that the dual vector current controller (DVCC) shows the best performance regarding grid current control and DC-link voltage regulation [16], [17]. This controller uses two different vector current controllers for the two sequence components,

together with a DC-link voltage controller based on the instantaneous active and reactive power theory.

Due to the PWM switching of voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [22]-[27]. Inserting an LCL-filter between the grid and the VSC eliminates high frequency harmonics even with lower switching frequency. Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. Damping methods are extensively addressed in literature. In [23] a resistance is used in series with the filter capacitor to passively damp the resonance. This resistance increases the system losses and decreases the efficiency of the filter. Instead, methods to actively damp the resonance are adopted as in [24], [25], [28]. In [25], a comparison between none-damped, passively-damped and actively-damped systems is carried out using Bode plots. It has been concluded that the active damping reduces the resonant peak as effectively as the passive damping. In [24], three cascaded controllers are used with the reference grid current generated from a DC voltage controller. The converter current and capacitor voltage are predicted. Moreover, two active resistances virtually connected in series with the filter inductor resistances are considered in the controller dead-beat gains. However, the use of these resistances is not justified. In [22], and [26] controllers with no damping are proposed. This has been proposed in [22] by controlling the grid current instead of the converter current and the proper choice of the filter parameters. However, by introducing a one sample time delay the system has been unstable acquiring the passive damping. In [26], two control loops are used: an outer current control loop and an inner capacitor voltage control loop. The latter is used to stabilize the controller and in the same time damp the resonance. The effect of adding a time delay has not been considered there as well.

The voltage compensation capability of VSCs' controllers has been also discussed in the literature to overcome the problem of having a decreased voltage at the connection point of the DG due to load/system dynamics [30]-[35], or to mitigate power quality problems [37], [38]. However, the effect of

the grid power quality on the phase locked loop (PLL), which is used to extract the grid phase angle, and on the compensation capability has not been treated in the literature. Moreover, in most of the literature the VSC is assumed to be either not injecting active power or has a controllable active power, which provides a wider compensation range.

One of the important capabilities of the DGs is to locally detect a grid outage condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, to prevent island operation. This capability has been discussed in the literature [39]- [45], where the transfer from grid-connected to island operation has been studied assuming a strong grid. The transfer from island to grid-connected mode is not much discussed. In [46], the load has been connected to the capacitor of the LCL-filter, at which its voltage is controlled in all the operating modes, to attain perfect transition without any transients. In [10], the DG was set into idle mode in case of grid recovery until the synchronization is achieved between the grid voltage and the DG voltage.

1.3 Purpose of the thesis and contributions

The main goals of the thesis and the contributions related to them are:

Goal 1: To determine the interface requirements and the capabilities of DGs with a voltage source converter (VSC) as a front end. For this purpose, two line filters are to be considered at the connection point of the DG; namely inductance line filter (L-filter) and inductance-capacitance-inductance line filter (LCL-filter). Vector current controllers are to be implemented for both systems.

Contribution 1: The derivation of the current reference generation equations, for the LCL-filter system, regarding the oscillating powers that are produced during the unbalanced grid voltage and compensating for them in two different ways. This has been presented in Section 2.5 and Paper A and Paper B.

Goal 2: To study the effect of voltage dips on the converter-interfaced DG and the requirements for ride-through capability.

Contribution 2: The study of all possible types of voltage dips that could appear at the terminals of a DG unit with both L-filter and LCL-filter systems. And, the derivation of the equations of maximum currents that would flow through the DG's converter switches. The main results of this point has been published in Paper B and explained in Section 3.5.

Goal 3: To study the effect of the other power quality problems on the DG operation, and how the DG controller could react in a corrective way to support the grid and provide better power quality at the connection point.

Contribution 3: A synthesis of a neural network based PLL has been proposed to reduce the error due to the voltage distortion, which has resulted in better compensation capability for the DG. This is shown in Paper E and in Section 4.5.

Goal 4: To study the possibility of intentional islanding for very weak grids.

Contribution 4: A passive detection algorithm that combines both the estimated frequency and the voltage regulator has been proposed to detect the islanding condition, especially in a weak grid. This has been shown in Section 5.4 and in Paper F and G, for various loads.

1.4 Thesis outline

The fundamental theory of the work is explained in details in **Chapter 2**. In that chapter the vector current controllers (VCC) for both the L-filter and the LCL-filter VSC-interfaced DG-systems are presented. The dual vector current controller (DVCC) has been implemented, for both systems, in order to achieve better current reference tracking in case of grid-voltage imbalance. Moreover, current reference equations are derived in such a way that they alleviate the DC-link ripples.

In **Chapter 3**, the voltage dips that could appear at the DG terminals are considered. An investigation of the ride-through capability is provided regarding the possible maximum currents that would flow through the VSC switches, and also regarding the DC-link voltage ripples. In addition, the maximum currents that would result during the dip period were obtained

using design equations that have been derived for various dips. Moreover, the DG system, both with the L-filter and the LCL-filter, has been examined for all possible voltage dips that could occur at its terminals. Recommendations of oversizing of the DG have been drawn as a consequence of that study.

If oversizing is not a possibility, the voltage regulation capability might appear as another possibility to correct the terminal voltage instead of riding through the voltage dip period. This is then discussed in **Chapter 4**. This capability might also be beneficial in case of operation in weak grids, where the voltage level is not constant and is dependent on the loads. Moreover, by compensating the grid voltage most of the power quality problems are mitigated. In this chapter, the voltage regulation capability is related to the performance of the phase locked loop (PLL) that estimates the phase angle of the grid voltage. A PLL that extracts the fundamental component of the grid voltage has been implemented using neural network technique.

In **Chapter 5**, the outage (and recovery) of the grid voltage has been considered, regarding the ability to keep the DG into operation to supply sensitive or critical loads. The main conclusions relating the different chapters and the possible future work considering the same topic are reported in **Chapter 6**.

1.5 Publications

The work in this thesis has resulted in eight publications, as shown in Fig. 1.3. The papers, designated in the figure from A to G, are supplemented at the end of this thesis with the same designation. The publications are also listed below with short description.

Journal papers

[J-1] F. Magueed, A. Sannino, and J. Svensson, "Design of Robust Converter Interface for Wind Power Applications," in *Wind Energy Journal, special issue on Electrical Integration of Wind Power*, vol. 8, no. 3, 2005, pp. 319 – 332.

In this paper the study of all possible voltage dips that could occur at the terminal of the DG is studied. This paper is designated as "Paper A" and supplemented at the final part of the thesis.

[J-2] F. Magueed, and T. Thiringer, "Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC," *submitted to Electrical Power Quality and Utilization Journal*.
The neural network based PLL has been presented here and compared with the positive sequence based PLL. This paper is designated as "Paper E" and supplemented at the final part of the thesis.

[J-3] F. Magueed, G. Olsson, and T. Thiringer, "Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation," *submitted to IEEE trans. on Power Delivery*.
An active islanding detection method is proposed, which consists of an under/over frequency passive detection algorithm, a PCC-voltage regulator and a DG reactive current limiter. This paper is designated as "Paper G" and supplemented at the final part of the thesis.

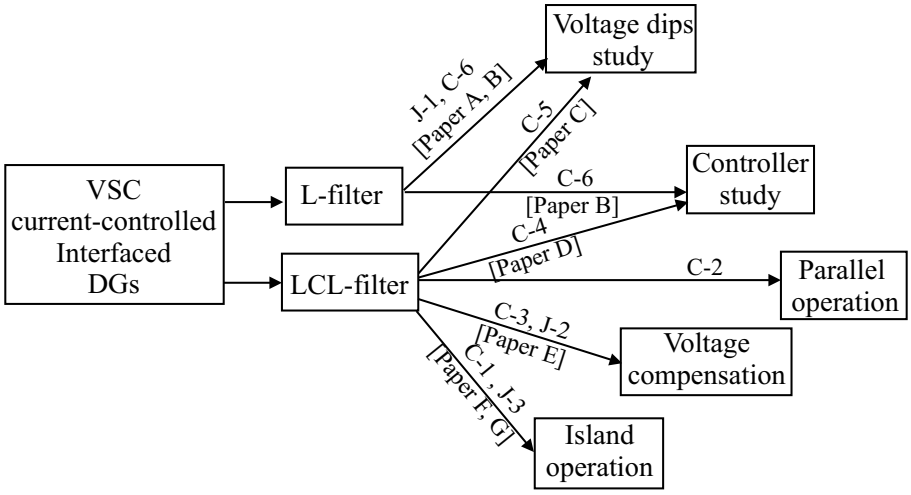

Fig. 1.3 Thesis outline with the resulting publication.

Conference papers (peer reviewed)

[C-1] F. Magueed, and J. Daalder, "Operation of Distributed Generation in Weak Grids with Local Critical Load," at *IEEE Annual Industrial*

Electronics Conference (IECON'06), Paris, France, November 7-10, 2006.

The passive islanding detection algorithm has been presented here with the focus on the operation in weak grids. This paper is designated as "Paper F" and supplemented at the final part of the thesis.

[C-2] F. Magueed, and J. Daalder, "Parallel Operation of Distributed Generation in Weak Distribution Systems," at the *12th International Power Electronics and Motion Control Conference (EPE-PEMC'06)*, Slovenia, August 30 - September 1, 2006, pp. 531 – 536.

A discussion of the voltage compensation limits and the possible parallel operation of DGs to provide better compensation capability is introduced.

[C-3] F. Magueed, and H. Awad, "Voltage Compensation in Weak Grids Using Distributed Generation with Voltage Source Converter as a Front End," at the *6th International Conference on Power Electronics and Drive Systems (PEDS'05)*, Kuala Lumpur, Malaysia, Nov 28 - Dec 1, 2005, pp. 234 – 239.

The main voltage regulator is presented here, with the capability to compensate for voltage dips at the grid.

[C-4] F. Magueed, and J. Svensson, "Control of VSC Connected to the Grid through LCL-Filter to Achieve Balanced Currents," at the *IEEE Industry Applications Society 40th Annual Meeting (IAS'05)*, Kowloon, Hong Kong, October 2-6, 2005.

The control of the VSC is presented here, in case of unbalanced voltage dips at the grid, to provide balanced DG currents. This paper is designated as "Paper D" and supplemented at the final part of the thesis.

[C-5] F. Magueed, J. Svensson, and A. Sannino, "Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage conditions," in *Proc of Power Tech Conference (PT'05)*, St. Petersburg, Russia, June 27-30, 2005.[1]

The performance of the LCL-filter system has been discussed regarding the voltage dips at the grid. This paper is designated as "Paper C" and supplemented at the final part of the thesis.

[1] This paper has been awarded ***High quality paper certificate*** for the presentation from 2005 IEEE Power Tech conference (June 27-30 2005).

[C-6] F. Magueed, A. Sannino, and J. Svensson, "Transient Performance of Voltage Source Converter under Unbalanced Voltage Dips," in *Proc. of Power Electronics Specialists Conference (PESC'04)*, Aachen, Germany, June 20-25 2004, pp. 1163 – 1168.

The study of voltage dips with phase angle jumps and the compensation of the oscillating powers using two different ways have been presented in this paper. This paper is designated as "Paper B" and supplemented at the final part of the thesis.

Chapter 2

Power Electronics Interfaced Distributed Generation – Controller Description

In this chapter, a general description of the power conversion systems, i.e. power electronics interface, for distributed generation is given. Two distributed generation systems are considered with two different line filters; namely an inductance line filter and an inductance-capacitance-inductance line filter, and a voltage source converter as a front end for the energy source. Vector current controllers are proposed for the two systems. The description of the controllers is given in details. Moreover, the generation algorithm for the current references is provided.

2.1 Current-controlled voltage source converters

Current controllers are preferred for shunt connected voltage source converters (VSCs) in order to increase stability of the closed loop and to decrease the time response in case of load transients [19]. Accordingly, a vector current controller (VCC) is considered throughout this work in order to obtain a high performance controller. In a VCC, the active and reactive currents (consequently powers) can be controlled independently. And, as indicated above, a high bandwidth controller with low cross-coupling effect between active and reactive currents can be achieved [20].

In Fig. 2.1, a scheme of the VSC system connected to the grid via a line filter along with the VCC is shown. Since the application of the distributed generation utilizing renewable resources is considered, the variation of the input current i_{in} is relatively slow compared to the response time of the controller. Hence, i_{in} is modelled as a constant current source. In addition,

the DC-link voltage should be regulated to maintain a constant voltage in case of grid voltage variations (e.g. voltage dips). The DC voltage regulator is implemented as a proportional-integral (PI) controller, where the measured DC capacitor voltage u_{dc} is compared with its reference value u_{dc}^{*} and the error signal is used to produce a reference DC current i_{dc}^{*} according to

$$i_{\mathrm{dc}}^{*} = \Delta u_{dc} k_{\mathrm{pdc}} \left(1 + \frac{1}{s T_{\mathrm{idc}}} \right) \tag{2-1}$$

where

k_{pdc}, T_{idc} are the proportional gain and integral time of the PI-controller respectively with their values as given in Appendix D;

s is the Laplace operator; and

$\Delta u_{\mathrm{dc}} = u_{\mathrm{dc}} - u_{\mathrm{dc}}^{*}$.

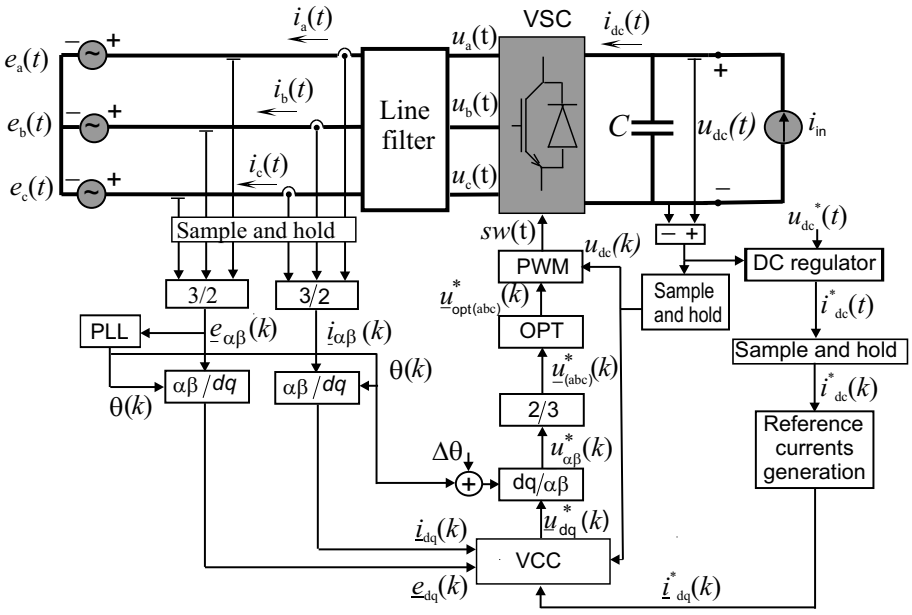

Fig. 2.1 Schematic diagram showing VSC, grid, filter and controller.

The signal flow from the power circuit to the VCC is as follows. The three-phase AC currents and voltages are first sampled and transformed into

the $\alpha\beta$-stationary frame[2]. The resulting rotating vectors $\underline{e}_{\alpha\beta}$ and $\underline{i}_{\alpha\beta}$ are then transformed into the rotating *dq*-frame that is synchronized with the grid voltage using a phase-locked-loop (PLL) that extracts the grid voltage angle θ. The *dq*-vectors of the measured voltages and currents, $\underline{e}_{\mathrm{dq}}$ and $\underline{i}_{\mathrm{dq}}$ respectively, are then used along with the reference current vector $\underline{i}^{*}_{\mathrm{dq}}$ by the VCC to produce the reference voltage vector $\underline{u}^{*}_{\mathrm{dq}}$. The different coordinate transformations are provided in Appendix A, where the *d*-component refers to the real value while the *q*-component refers to the imaginary value of a vector.

The reference currents are produced in such a way as to decrease the DC-link voltage ripple using a "reference currents generation" algorithm that uses the signal coming from the DC-link voltage regulator, and is explained later in this chapter. The reference voltage vector is then transformed to a vector in the $\alpha\beta$-frame using a transformation angle of $\theta+\Delta\theta$, where $\Delta\theta$ compensates for the transformation angle error due to one sample calculation time delay of the controller. The vector $\underline{u}^{*}_{\alpha\beta}$ is then transformed into three-phase control signals. Those signals are then used in the PWM modulator to produce the switching pattern for the VSC. The PWM is optimized to increase the maximum output voltage of the converter without increasing the DC-link voltage [12], [14]. The block "OPT" injects a zero sequence voltage into the control signals. Due to the absence of a neutral wire, the added zero sequence waveforms are cancelled out.

It should be mentioned that the design of the VCC is different for the power circuit with an inductance line filter from the power circuit with inductance-capacitance-inductance line filter, since both circuits have different time and frequency behaviors. Also the generation of reference currents is different for the two filter configurations. This is shown in the next sections.

[2] The coordinate transformation matrices are explained in Appendix A.

2.2 Vector Current Controller with inductance line filter

An inductance line filter is first considered. The plant in Fig. 2.2 represents the filter, the PWM, and the VSC. The last two, however, are assumed to be ideal, having a transfer function of 1. The plant transfer function in the *s*-domain is then represented as

$$G_{\mathrm{pl}}(s) = \frac{1}{sL_{\mathrm{f}} + R_{\mathrm{f}}} \tag{2-2}$$

where

L_{f} is the filter inductance; and

R_{f} is the filter resistance.

The controller design is based on deadbeat control. The measured voltage and current vectors are used to calculate the feedforward vector $\underline{FF}_{\mathrm{dq}}$ as

$$\underline{FF}_{\mathrm{dq}}(k) = \underline{e}_{\mathrm{dq}}(k) + \underline{i}_{\mathrm{dq}}(k)(R_{\mathrm{f}} + \mathrm{j}\omega L_{\mathrm{f}}) \tag{2-3}$$

where

ω is the angular frequency of the grid voltage;

k is the sampling instant; and

j is the imaginary unit.

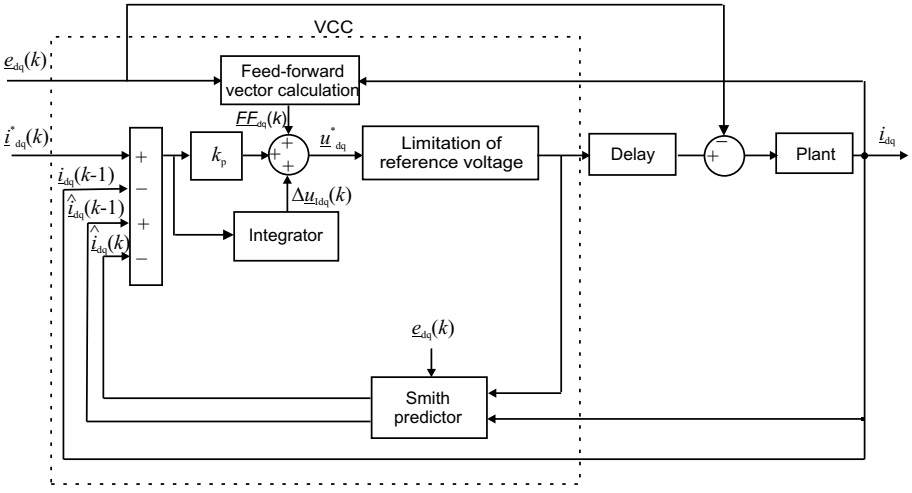

Fig. 2.2 Deadbeat based vector current controller (VCC) for DG with L-filter.

The change in the current reference is met by a change in the voltage reference that is produced by adding $\underline{FF}_{\mathrm{dq}}$ to the output of a PI-controller with a proportional gain k_p, also called here dead-beat gain. The dead-beat strategy has been described in [20]. The Dead-beat gain is given in terms of the filter parameters as

$$k_{\mathrm{p}} = \frac{L_{\mathrm{f}}}{T_{\mathrm{s}}} + \frac{R_{\mathrm{f}}}{2}. \tag{2-4}$$

An integral part $\Delta\underline{u}_{\mathrm{idq}}$ is needed to remove the static errors caused by non-linearity, noisy measurements and non-ideal components. The generated reference voltage is then calculated as

$$\underline{u}^{*}_{\mathrm{dq}}(k+1) = \underline{FF}_{\mathrm{dq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idq}}(k). \tag{2-5}$$

The integral part is implemented as

$$\Delta\underline{u}_{\mathrm{idq}}(k+1) = \Delta\underline{u}_{\mathrm{idq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{i}} \tag{2-6}$$

where k_{i} is the integration constant, which can be written as

$$k_{\mathrm{i}} = \frac{k_{\mathrm{p}}T_{\mathrm{s}}}{T_{\mathrm{i}}} \tag{2-7}$$

where T_{i} is the integral time constant, which is chosen to be equal to the L-filter time constant $T_{\mathrm{i}} = \frac{L_{\mathrm{f}}}{R_{\mathrm{f}}}$, and T_{s} is the sampling time.

The current error vector $\underline{\varepsilon}_{\mathrm{idq}}$ is described by

$$\underline{\varepsilon}_{\mathrm{idq}}(k) = \underline{i}^{*}_{\mathrm{dq}}(k) - \underline{i}_{\mathrm{dq}}(k-1) + \hat{\underline{i}}_{\mathrm{dq}}(k-1) - \hat{\underline{i}}_{\mathrm{dq}}(k) \tag{2-8}$$

which accounts for a one sample time delay in the measured current signal due to the calculation time of the digital controller. This delay has been compensated for using the estimated current $\hat{i}_{\mathrm{dq}}$ at two successive instants,

which is calculated by a Smith predictor [48], [76]. The Smith predictor is implemented in a way analogous to a state observer[3], as proposed by [20], which means running a model of the plant in parallel to the plant itself. In steady state, the estimated and actual currents should be equal, hence $\underline{i}_{\mathrm{dq}}(k-1)=\hat{\underline{i}}_{\mathrm{dq}}(k-1)$ in (2-8), which cancels the time delay effect.

The output reference voltage command is also limited to be inside the control region, which is described by a hexagon composed of six equilateral triangles with a side length of $\sqrt{2/3}u_{\mathrm{dc}}$. In this work the minimum amplitude error (MAE) limiting method has been adopted [20]. In this method a new reference voltage vector on the hexagon boundary that is closest to the original reference vector is chosen as explained by Fig. 2.3. This is done by mapping the voltage reference into new coordinates *xy*. The *xy*-coordinate position depends on the number of the sector in the hexagon that contains the voltage reference. The reference voltage vector in the new coordinates u_{xy}^{*} is obtained as

$$\underline{u}_{\mathrm{xy}}^{*}=\underline{u}_{\alpha\beta}^{*}e^{-\mathrm{j}\theta_{\mathrm{xy}}} \tag{2-9}$$

where θ_{xy} is the angle between the α-axis and the *x*-axis and is calculated as

$$\theta_{\mathrm{xy}}=\left(1+2(n-1)\right)\pi/6 \tag{2-10}$$

where *n* is the sector number at which the reference vector lies in the hexagon.

The components of the limited reference voltage vector are calculated from Fig. 2.3 as

$$u_{\mathrm{x}}=\frac{u_{\mathrm{dc}}}{\sqrt{2}} \tag{2-11}$$

[3] The use of the Smith predictor is described in more details in Paper D.

$$u_{\mathrm{y}} = \begin{cases} u_{\mathrm{y}}^{*} & \left|u_{\mathrm{y}}^{*}\right| \le \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \\ sign(u_{\mathrm{y}}^{*}) \cdot \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} & \left|u_{\mathrm{y}}^{*}\right| > \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \end{cases} . \tag{2-12}$$

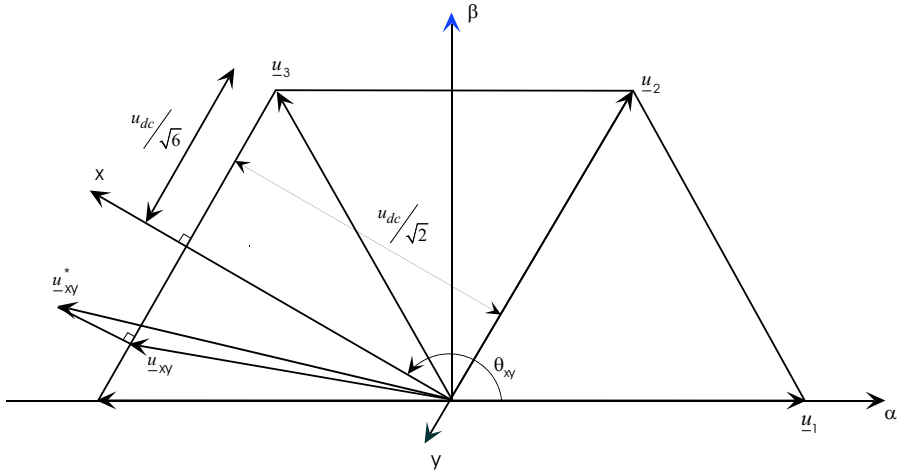

Fig. 2.3 Principle of the minimum amplitude error method.

It is worth noting here that using the limited voltage reference as an input for the Smith predictor, as shown in Fig. 2.2, is important in providing an anti-windup property for the controller, which is useful in case of increased current steps.

The time domain performance of the controller is tested in Fig. 2.4, for the case of a substantial positive active current step, which is considered the worst operational case since it leads the voltage to the saturation area. Due to the high current step of 1.5 p.u. that has been applied at 0.2 s, the controller will go into the voltage reference limitation algorithm, at which the reference voltage will be limited as shown by the same figure. Since the demanded reference voltage, required to achieve the current step, has not been reached, the dead-beat is not accomplished. Hence, it will take several samples for the current to reach its reference value. As shown by the figure, the current will accomplish the step in 2 ms. The figure also shows the cross-coupling effect

on the *q*-component of the current. To eliminate this coupling effect, i_{q}^{*} might be modified to counteract the effect of the active current step [20]. However, this will not be considered here since the reference *q*-component current will be implemented later to compensate for various power quality problems at the grid.

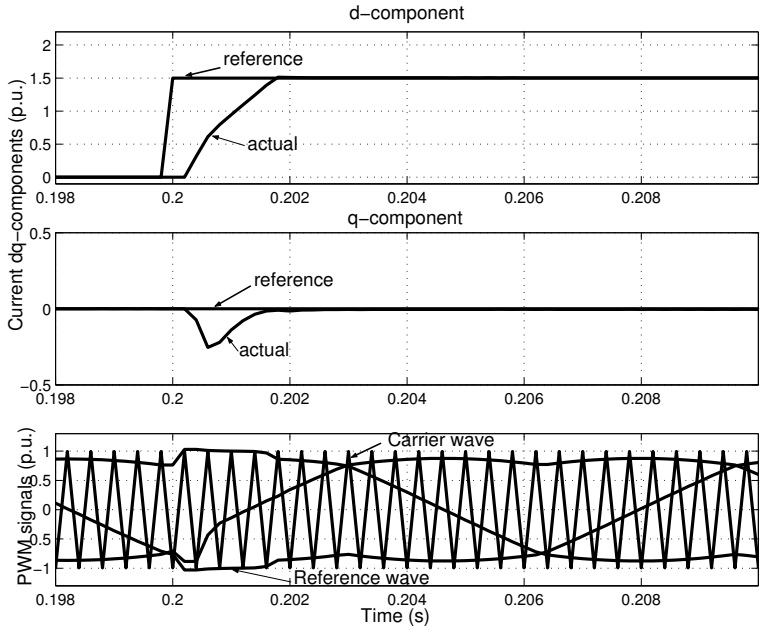

Fig. 2.4 Active current (upper), reactive current (middle), and PWM signals (lower), due to a step in i_{d}^{*} from 0 to 1.5 p.u.

2.3 Dual vector current controller (DVCC)

In case of an unbalanced grid voltage, the voltage vector in the *dq*-frame has oscillations at a frequency of twice the fundamental frequency due to the negative sequence that exists in the grid voltage. That will lead to oscillations in the injected currents to the grid. To deal with that situation a dual vector current controller (DVCC) [18] can be used. The DVCC consists

of two separate VCCs, one for controlling the positive-sequence voltage and the other for controlling the negative-sequence voltage. This controller synthesis has proved to give the best performance regarding grid current control and DC-link voltage regulation [17]. A simplified scheme for the DVCC is shown in Fig. 2.5.

The positive sequence PI-controller is described in the positive *dq*-frame (*dqp*-frame), which rotates in the positive direction, as

$$\underline{u}^{*}_{\mathrm{dqp}}(k+1) = \underline{FF}_{\mathrm{dqp}}(k) + \underline{\varepsilon}_{\mathrm{idqp}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqp}}(k) \qquad (2\text{-}13)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqp}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqp}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqp}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The negative sequence PI-controller is described in the negative *dq*-frame (*dqn*-frame), which rotates in the negative direction, as

$$\underline{u}^{*}_{\mathrm{dqn}}(k+1) = \underline{FF}_{\mathrm{dqn}}(k) + \underline{\varepsilon}_{\mathrm{idqn}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqn}}(k) \qquad (2\text{-}14)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqn}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqn}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqn}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The decomposition of the supply voltage into positive and negative sequence components is performed using the delayed signal cancellation (DSC) algorithm, which has been first proposed in [77]. This algorithm is implemented in the *dq*-frame, which rotates in the positive direction, in the same way as suggested in [17]. In this frame, the positive sequence is a constant vector (constant amplitude and fixed direction), while the negative sequence is a rotating vector, which rotates with twice the line frequency in the opposite direction, as compared with the positive sequence.

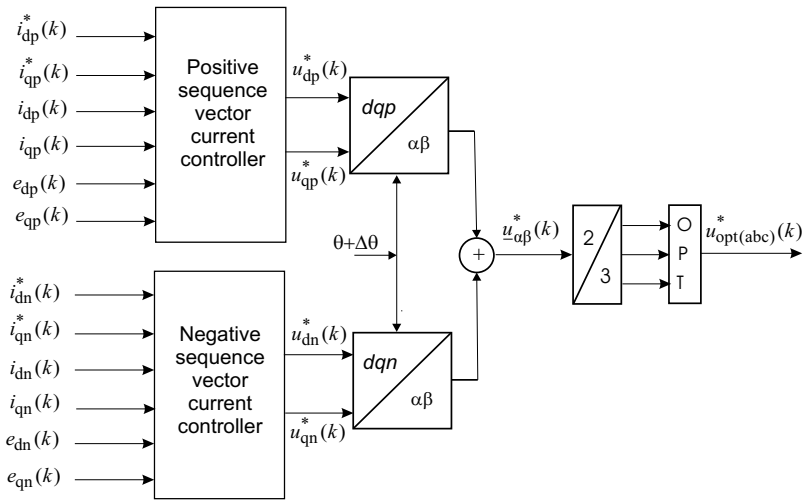

Fig. 2.5 Simplified block diagram of dual vector current controller (DVCC).

In the DSC the measured supply voltage, in the *dq*-frame, and the same signal, delayed by one-quarter of a fundamental frequency period, are considered. Delaying the signal gives a vector composed by the same positive sequence component and a negative sequence component which has equal amplitude but opposite sign. Therefore, if the signal delayed by one-fourth of period is added to the measured supply voltage, the negative sequence voltage will be removed.

The positive sequence voltage vector can thus be extracted from the measured values as

$$\underline{e}_{\mathrm{dqp}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) + \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-15}$$

where T is the period at the fundamental frequency.

The negative sequence can be obtained in the positive rotating plane, as follows

$$\underline{e}_{\mathrm{dqn}_{(\mathrm{p})}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) - \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-16}$$

which is then transformed into the negative rotating plane by transforming it into the $\alpha\beta$-frame and back into the *dqn*-frame using the opposite angle.

The time domain response of the DVCC is compared with the time domain response of the VCC when a grid voltage of 40% imbalance ratio is applied. Moreover, a step in the active current reference is applied at 0.25 s. The injected current is oscillating in the case of using the VCC, as shown in Fig. 2.6, while better tracking is achieved using the DVCC.

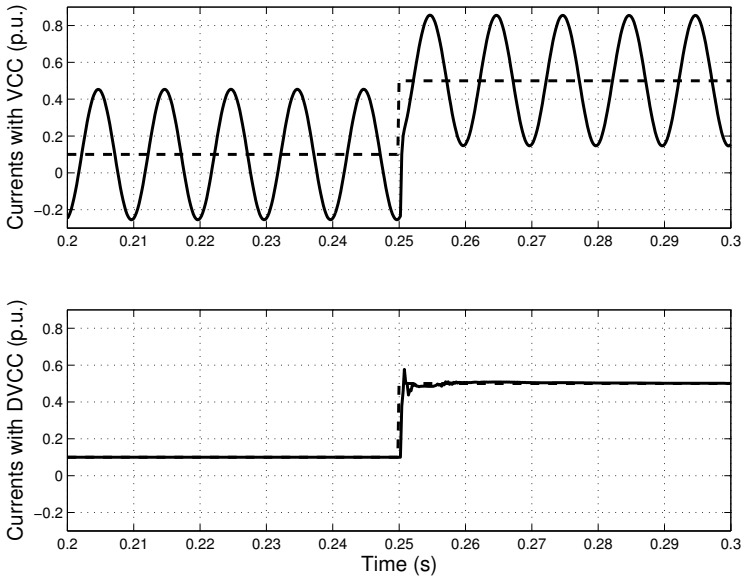

Fig. 2.6 Active grid current i_d (solid) and reference current i^*_d (dashed); with VCC (upper) and DVCC (lower).

2.4 Current reference generation with inductance line filter

In the case of a controllable DC-link voltage, proper current references should be generated in order to improve the performance of the VCC. Two performance measures are considered, which are the minimization of the DC-link voltage ripple and the decrease of the AC currents amplitudes and/or harmonics. The reference currents generation algorithm is based on

the instantaneous power theory [80]. The active power on the AC side of the converter, p_1, is considered equal to the active power on the DC side, P_{dc}, neglecting the switching losses. The power balance equation can be expressed as

$$\begin{bmatrix} p_1 \\ q_1 \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \Delta p \\ \Delta q \end{bmatrix} \tag{2-17}$$

where p_1 and q_1 are the instantaneous active and reactive powers at the AC-side of the converter respectively. The terms Δp and Δq are active and reactive powers dissipated by the filter respectively, and can be calculated instantaneously as

$$\Delta p = R_f \left(i_d^2 + i_q^2 \right) \tag{2-18}$$

$$\Delta q = \omega L_f \left(i_d^2 + i_q^2 \right). \tag{2-19}$$

The instantaneous active power p_2 and reactive power q_2 at the grid are calculated as:

$$\begin{aligned} p_2 &= e_d i_d + e_q i_q \\ q_2 &= -e_d i_q + e_q i_d \end{aligned}. \tag{2-20}$$

To achieve unity power factor, the reactive power at the grid side $q_2 = q_1 - \Delta q$ is nullified. The current references are then calculated using (2-17) as follows

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \end{bmatrix}. \tag{2-21}$$

2.5 Current reference generation for inductance line filter and unbalanced grid voltage

For the DVCC, current reference signals should be provided in the positive and the negative *dq*-coordinates. The derivation[4] is carried out in the same way as for the VCC. The current references are calculated using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ q_{\mathrm{ac},2} \\ p_{\mathrm{s}2,1} - \Delta p_{\mathrm{s}2} \\ p_{\mathrm{c}2,1} - \Delta p_{\mathrm{c}2} \end{bmatrix} \tag{2-22}$$

where the instantaneous active power p_2 and reactive power q_2 at the grid are

$$\begin{aligned} p_2(t) &= p_{\mathrm{ac},2} + p_{\mathrm{c}2,2}\cos(2\omega t) + p_{\mathrm{s}2,2}\sin(2\omega t) \\ q_2(t) &= q_{\mathrm{ac},2} + q_{\mathrm{c}2,2}\cos(2\omega t) + q_{\mathrm{s}2,2}\sin(2\omega t) \end{aligned} \tag{2-23}$$

with the following subscripts notations

ac - stands for the power at the fundamental frequency;

2 - stands for the grid side.

1 - stands for the AC converter side;

c2 - stands for the cosine component of a power that is oscillating with double the fundamental frequency; and

s2 - stands for the sine component of a power that is oscillating with double the fundamental frequency.

The power loss through the filter is encountered for in (2-22) by the terms Δp, $\Delta p_{\mathrm{s}2}$, and $\Delta p_{\mathrm{c}2}$.

Equation (2-22) has been considered in two ways, which are referred to as case 1 and case 2. The injected reactive power $q_{\mathrm{ac},2}$ to the grid is assumed to be zero in both cases.

[4] Details are given in Paper A and Paper B.

Case 1- The oscillating powers flow from the VSC side to the filter

Assuming that the converter supplies the oscillating power to the filter, and neglecting the converter losses which means $p_{ac,1}$ is equal to P_{dc}, the following equations will describe the different powers

$$P_{c2,1} = \Delta P_{c2},\ P_{c2,2} = 0 \tag{2-24}$$

$$P_{s2,1} = \Delta P_{s2},\ P_{s2,2} = 0 \quad . \tag{2-25}$$

Substituting in (2-22), the reference currents are calculated as

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qn} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{2-26}$$

Using (2-26), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.7.

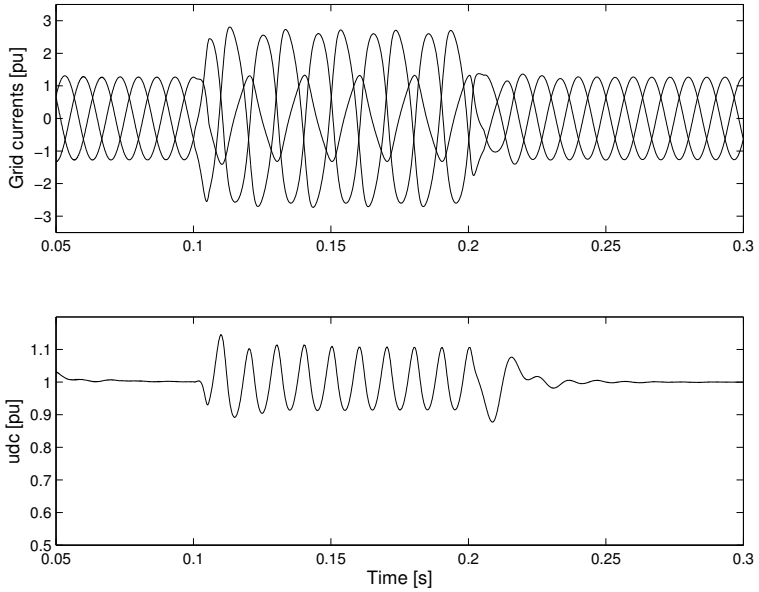

Fig. 2.7 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

Case 2- The oscillating powers flow from the grid side to the filter

In this case the grid is forced to supply the oscillating powers to the filter, by using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ 0 \\ -\Delta p_{\mathrm{s2}} \\ -\Delta p_{\mathrm{c2}} \end{bmatrix}. \qquad (2\text{-}27)$$

Using (2-27), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.8.

Comparing Fig. 2.7 and Fig. 2.8, it is concluded that it is preferred to use the current reference generation in (2-27) over (2-26) since the DC-link voltage ripples are reduced during the fault period.

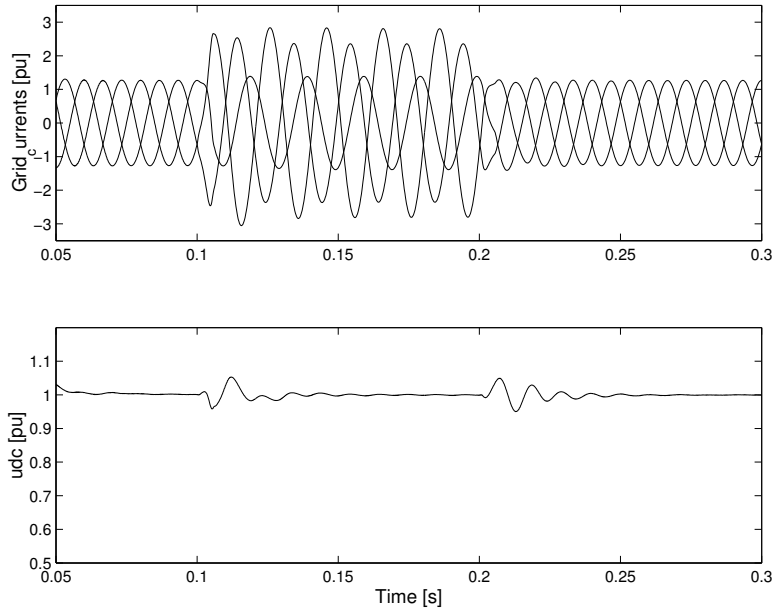

Fig. 2.8 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

2.6 Vector Current Controller with inductance-capacitance-inductance line filter

Due to the PWM switching of the voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [29]. Inserting an LCL-filter[5] between the grid and the VSC, as shown in Fig. 2.9, eliminates high frequency harmonics even with lower switching frequency.

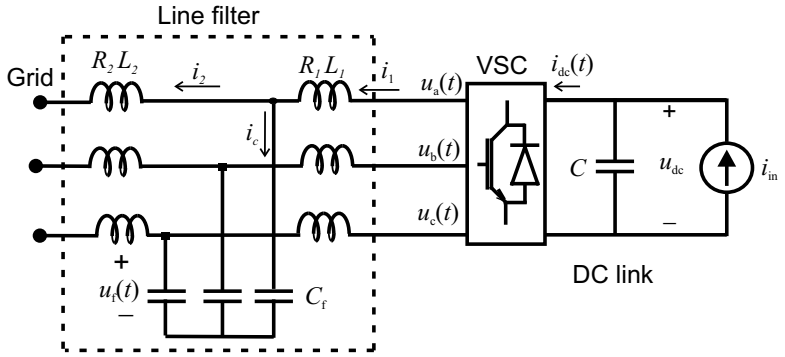

Fig. 2.9 Power circuit of DG system with VSC as a front end and an LCL-filter.

Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. In this work, a cascade control structure ([47], [48], and [49]) has been implemented to increase the stability margin and at the same time to damp oscillations at the resonant frequency of the LCL-filter. As shown in Fig. 2.10, the plant is described by three cascaded transfer functions; G_{p1}, G_{p2}, and G_{p3}, as

[5] The design of the LCL-filter parameters that are adopted here is given in Appendix B.

$$G_{\mathrm{p1}}(s)=\frac{I_2(s)}{U_{\mathrm{f}}(s)-E(s)}=\frac{1}{sL_2+R_2}$$
$$G_{\mathrm{p2}}(s)=\frac{U_{\mathrm{f}}(s)}{I_1(s)-I_2(s)}=\frac{1}{sC_{\mathrm{f}}} \tag{2-28}$$
$$G_{\mathrm{p3}}(s)=\frac{I_1(s)}{U(s)-U_{\mathrm{f}}(s)}=\frac{1}{sL_1+R_1}$$

where

$I_2(s)$ is the Laplace function of the grid side current $i_2(t)$;

$U_{\mathrm{f}}(s)$ is the Laplace function of the filter capacitor voltage $u_{\mathrm{f}}(t)$;

$E(s)$ is the Laplace function of the grid voltage $e(t)$;

$I_1(s)$ is the Laplace function of the converter side current $i_1(t)$; and

$U(s)$ is the Laplace function of the converter output voltage $u(t)$.

The inner controller G_{c3} is used for stabilization of G_{p3} and is designed using dead-beat control strategy. The two outer controllers G_{c2} and G_{c1} are used to stabilize G_{p2} and G_{p1} respectively. G_{c2} is implemented as a P-controller, while G_{c1} is implemented as a PI-controller where the integral part is added to eliminate the steady state error. With the resulting controller, shown in Fig. 2.10, the two controllers G_{c1} and G_{c2} are acting like one PI-controller. The outer controller G_{c1} is a two-degree of freedom controller, since it is using the output signal of a Smith predictor (with a compensation gain k_{ps}) to cancel the time delay effect. The time-delay free plant transfer-function G_{pm} represents the LCL-filter model in steady state, where the capacitor effect is neglected.

The three controllers are described in the rotating dq-frame as follows

$$\underline{y}_{\mathrm{1dq}}(k)=k_{\mathrm{p1}}\left(\underline{\varepsilon}_{\mathrm{idq}}(k)+\frac{T_{\mathrm{s}}}{T_{\mathrm{i}}}\sum_{n=0}^{k}\underline{\varepsilon}_{\mathrm{idq}}(n)\right) \tag{2-29}$$

$$\underline{y}_{\mathrm{2dq}}(k)=k_{\mathrm{p2}}\,\underline{y}_{\mathrm{1dq}}(k) \tag{2-30}$$

$$\underline{u}^{*}_{\mathrm{dq}}(k+1)=\underline{u}_{\mathrm{fdq}}(k)+(R_1+\mathrm{j}\omega L_1)\underline{i}_{\mathrm{1dq}}(k)+k_{\mathrm{p3}}\,\underline{y}_{\mathrm{2dq}}(k) \tag{2-31}$$

where

$\underline{y}_{1dq}$ is the output vector of G_{c1}, which represents the change in the capacitor voltage $\underline{u}_{fdq}$;

k_{p1} is the proportional gain of G_{c1};

T_i is the integral time of G_{c1};

$\underline{y}_{2dq}$ is the output vector of G_{c2}, which represents the required change in the converter side current $\underline{i}_{1dq}$;

k_{p2} is the proportional gain of G_{c2}; and

k_{p3} is the proportional gain of G_{c3}.

The current error vector $\underline{\varepsilon}_{idq}$ is the input to the outer controller G_{c1}, and is described in the same way as in (2-8).

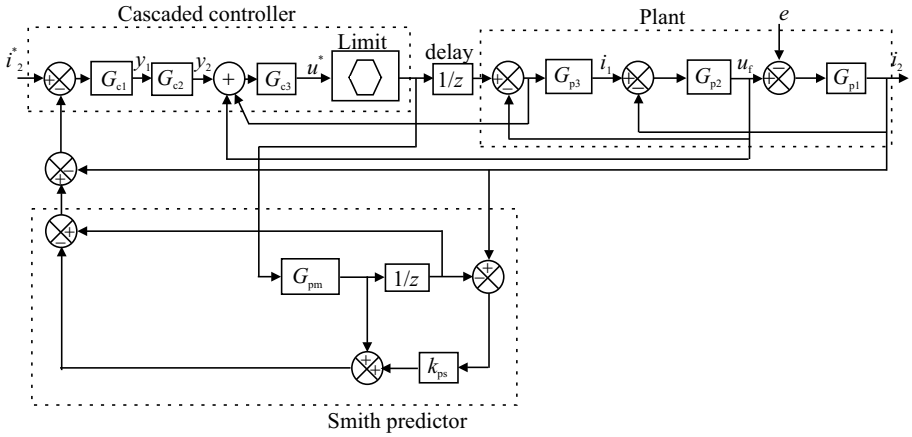

Fig. 2.10 Schematic diagram of the proposed cascaded controller (the z denotes the z transform, thus $1/z$ denotes a delay of one sample). Note that the controller is described in discrete form while the plant is described in continuous form.

The faster the inner loop is in comparison with the outer loops, the better the performance of the cascaded control system becomes in the sense of the transient response [49]. However, reduced gains for the outer controllers will reduce the overall bandwidth of the system. Hence, the inner controller gain is set to the dead-beat gain as [20]

$$k_{\mathrm{p3}} = \frac{L_1}{T_\mathrm{s}} + \frac{R_1}{2} \ . \tag{2-32}$$

The Smith predictor gain is set to a small value to stabilize the overall controller, while k_{p2} and k_{p1} are tuned by changing their values and examining the Bode plot. In Fig. 2.11 the value of k_{p2} is set to 30% of k_{p3}, while k_{p1} assumes values between 30% and 100% of k_{p2}. The same is performed in Fig. 2.12 by setting k_{p1} as 70% of k_{p2}, to achieve a high bandwidth and no overshoot, while k_{p2} is taking values between 25% and 70% of k_{p3}. It is shown by the phase plot in the figure that for k_{p2} values of 70% to 50% of k_{p1} the controller becomes unstable. Hence, the value of k_{p2} has been chosen to 30% of k_{p1}. The values used for the gains are listed in Appendix D.

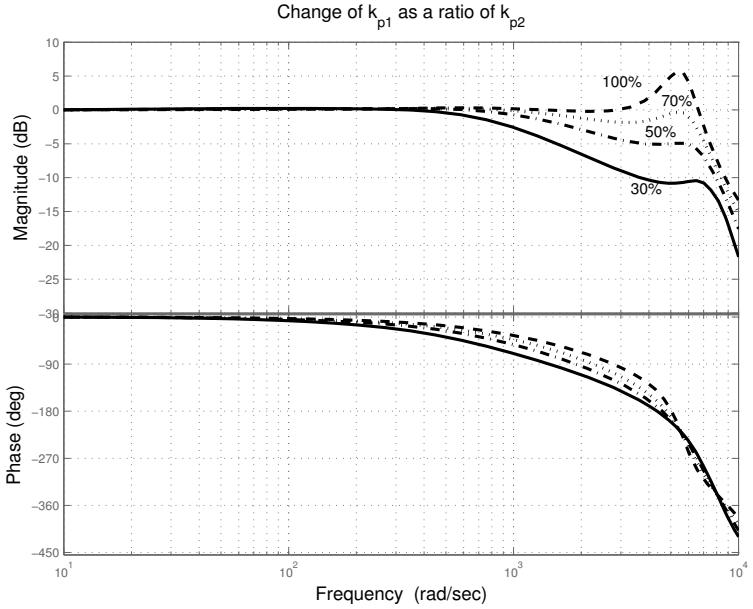

Fig. 2.11 The closed loop system frequency performance as k_{p1} is changed as a certain percentage of k_{p2}, with k_{p2} constant.

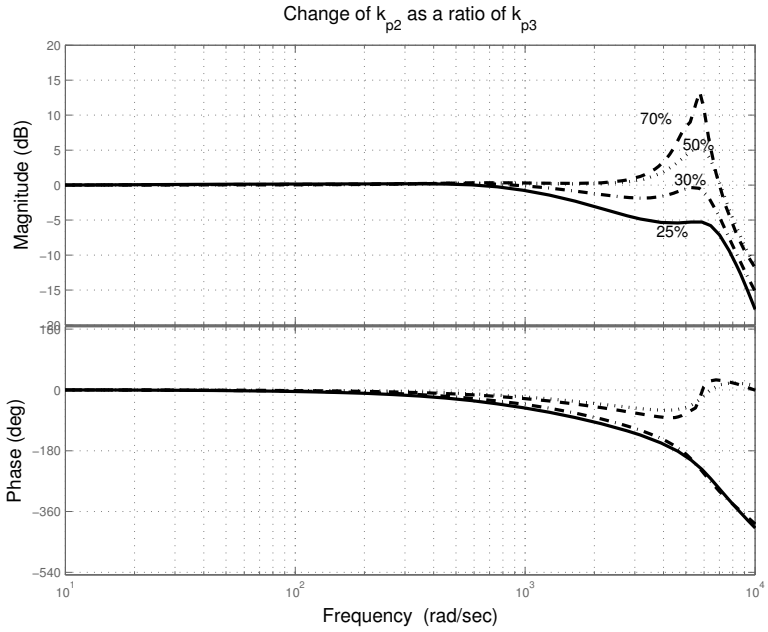

Fig. 2.12 The closed loop system frequency performance as k_{p2} is changed as a certain percentage of k_{p3}, while k_{p1} is constant.

2.7 Current reference generation with inductance-capacitance-inductance line filter

The current references are generated, in the same way as for the L-filter, as

$$\begin{bmatrix} i_{2\mathrm{d}}^{*} \\ i_{2\mathrm{q}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{d}} & e_{\mathrm{q}} \\ e_{\mathrm{q}} & -e_{\mathrm{d}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ \omega C_{\mathrm{f}} \left(u_{\mathrm{cd}}^{2} + u_{\mathrm{cq}}^{2} \right) \end{bmatrix} - \begin{bmatrix} -\omega C_{\mathrm{f}} u_{\mathrm{cq}} \\ \omega C_{\mathrm{f}} u_{\mathrm{cd}} \end{bmatrix} \quad (2\text{-}33)$$

where Δp is the active power dissipated in the filter, and is a function of the grid side and converter side currents

$$\Delta p = R_1\left(i_{1d}^2 + i_{1q}^2\right) + R_2\left(i_{1d}i_{2d} + i_{1q}i_{2q}\right) + \omega L_2\left(-i_{1d}i_{2d} + i_{1q}i_{2d}\right). \tag{2-34}$$

The current references are generated in the same manner for the DVCC[6].

2.8 Conclusions

Two distributed generation systems with a voltage source converter as a front end and two line filters; namely L-filter and LCL-filter, are considered. Vector current controllers have been proposed to control the injected grid currents for both systems. The controller for the L-filter system is based on the dead-beat control and is modified to deal with one sample time delay, integrator windup, grid voltage saturation and grid voltage imbalance. The controller shows good reference tracking even in the worst case of increased current steps. In addition, in the case of controllable DC-link voltage, the current references have been derived in such a way that a regulated DC-link voltage is provided even in the case of unbalanced grid voltage. On the other hand, a cascaded current controller has been proposed for the LCL-filter system. The current references have also been derived in the same manner as for the L-filter system.

[6] The detailed derivation is given in Appendix E and Paper C.

Chapter 3

Voltage Dips Ride-Through Capability

In this chapter, the effect of all possible voltage dips that could appear at the terminal of a converter interfaced DG unit is examined. The two distributed generation systems, described in the previous chapter, with two different line filters are compared regarding the injected grid currents and the DC-link voltage regulation. Moreover, design equations are derived to be able to predict the maximum currents that are expected to flow through the converter switches during different voltage dips.

3.1 Voltage dips definition

A voltage dip is a phenomenon that is experienced at the end user terminals mainly due to a short circuit fault at a certain point in the electrical network. It can also happen due to motor starts or overloads. It is, as defined by IEEE-std 1159-1995 [50], a decrease to between 0.1 to 0.9 p.u. in the RMS value of the voltage at the power frequency for durations of 0.5 cycle to 1 min. Using this definition, the voltage dip magnitude is referring to the remaining voltage.

In spite of the short duration, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [51]. To deeply study the effect of voltage dips on DGs with a power-electronics interface, the classification found in [52] has been adopted.

3.2 Voltage dips classification

Starting from the different types of faults that can occur in a power system, a classification of voltage dips has been accomplished in [52]. It depends on how the load is connected and how the windings of the

supplying transformer are connected. According to this classification, there are seven types of dips designated with the letters "A" to "G". The system in Fig. 3.1 has been used to quantify the magnitude of a voltage dip in a radial system. In this system, the fault occurs at a remote distance from bus 2 and the load, which could be a DG (as in the thesis), is connected at bus 3. Two impedances are connected to bus 2: the impedance of the system, denoted by Z_S, which represents Thevinin's equivalent impedance of the power system, and the fault impedance Z_F. The load is connected through a transformer to bus 2, at which the voltage, in p.u., is given by

$$V_{dip} = \frac{Z_F}{Z_F + Z_S}. \tag{3-1}$$

It is assumed that the pre-fault voltage is used as reference and is equal to 1 p.u. This typically means that voltage dips originated in the transmission system are shallow (since Z_s is small), while voltage dips originated at distribution level can be deep.

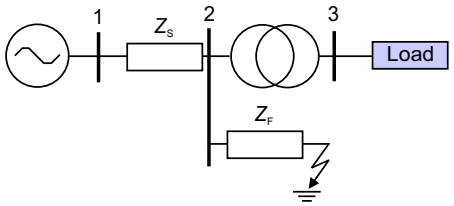

Fig. 3.1 General single-line model for dips classification.

If first it is assumed that the *X*/*R* ratio of the impedances Z_S and Z_F is the same, then V_{dip} has zero phase angle. The resulting voltage dip at bus 3 can be of type "A", which could be a result of a three-phase balanced fault, or any of the six unbalanced types denoted with letters "B" through "G" and reported in Fig. 3.2. In the figure, $E_{i,dip} = E_i V_{dip}$ where the subscript i denotes the phase sequence and takes the values 1, 2, and 3[7], and E_i represents the RMS value of the healthy phase voltage.

[7] Afterwards the three phases will be referred to as a, b, and c.

The transformer connection type has an effect of changing the voltage dip from one type to another. Still, in this work, all dip types are considered for the purpose of providing a general analysis.

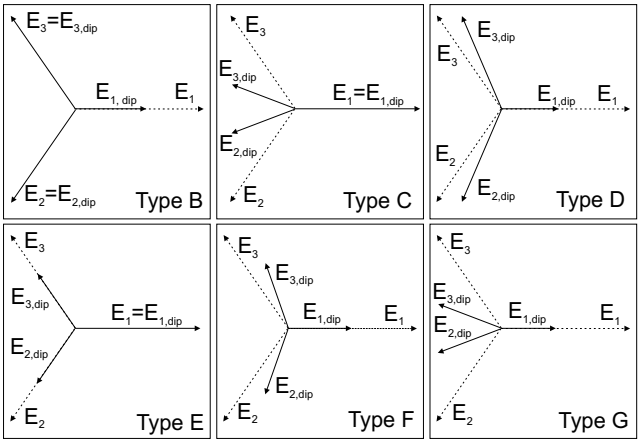

Fig. 3.2 Unbalanced voltage dip classification from "B" to "G". Phasors of three phase voltage before (dotted) and during (solid) fault are displayed. The classification is adopted from [52].

3.3 Voltage dips associated with phase angle jump

If the *X*/*R* ratio for Z_S and Z_F is different, the voltage dip seen at the terminals of the load will have a phase angle "ψ" called "phase angle jump". The impedance angle α is defined as

$$\alpha = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \tag{3-2}$$

where $Z_S = R_S + jX_S$, $Z_F = R_F + jX_F = zl$, z is the feeder impedance per unit length and l is the feeder length. The expression of the voltage dip at bus 2 will be

$$v_{dip} = \frac{\lambda e^{j\alpha}}{1 + \lambda e^{j\alpha}} = V_{dip}\angle\psi \tag{3-3}$$

where $\lambda\, e^{j\alpha} = zl / Z_S$.

The four values for the impedance angle α, that are suggested in [52], are considered: 10^o as the highest expected value for transmission system faults, 0^o as the reference value, -20^o for overhead distribution lines, and -60^o for underground distribution cables. In Fig. 3.3, the relation between the phase angle jump and different dip magnitudes at the four impedance angles is shown. The phase angle jump is larger for smaller dip magnitudes and is more sensitive to the dip magnitude when $\alpha = -60^o$.

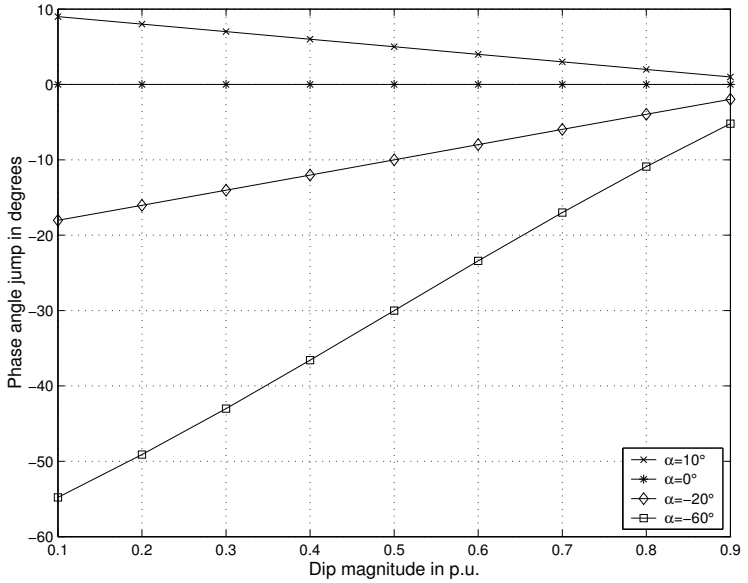

Fig. 3.3 Phase angle jump for different dip magnitudes and impedance angles.

3.4 Positive/negative sequence sub-classification

The magnitudes of the positive sequence (E_p) and the negative sequence (E_n) of the grid voltage for dip types "A" through "G" are calculated using Park transformation and summarized in Table 3-1, where E is the phase-to-phase RMS grid voltage. It shows that dips "C" and "D" have the same positive and negative sequence magnitudes. The same applies for dips "E", "F", and "G". However they may affect the system in different ways

according to Table 3-2, at which the positive and negative sequence components in the *dq*-coordinate system have been calculated. It shows that dips "C" and "D" result in different negative sequence *dq*-components. The same also holds for dip types "F" and "G", while dips "E" and "G" are exactly the same since they both result in the same positive and negative sequence components. This classification is useful in understanding the effect of unbalanced voltage dips on the system. Hence, the following study is carried out using the dual vector current controller (DVCC) that has been described in the previous chapter.

Table 3-1 Positive and negative sequence magnitudes of grid voltage for dip types "A" through "G".

Dip type	E_p	E_n
A	EV_{dip}	0
B	$\frac{E}{3}\sqrt{4+4V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
C, D	$\frac{E}{2}\sqrt{1+2V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{2}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
E, F, G	$\frac{E}{3}\sqrt{1+4V_{dip}\cos\psi+4V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$

Table 3-2 Positive and negative sequence components of the grid voltage in *dq*-coordinates for dip types "A" through "G".

Dip type	e_{dp}	e_{qp}	e_{dn}	e_{qn}
A	$EV_{dip}\cos\psi$	$EV_{dip}\sin\psi$	0	0
B	$\frac{E}{3}(2+V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
C	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{E}{2}(1-V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$
D	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{-E}{2}(1-V_{dip}\cos\psi)$	$\frac{-E}{2}V_{dip}\sin\psi$
E	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$
F	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
G	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$

3.5 Current through the voltage source converter caused by voltage dips

At the distribution level, the voltage source converter (VSC) mostly utilizes isolated gate bipolar transistors (IGBT's). An IGBT is easy to turn on and off, and has low conduction and switching losses [13]. The ratings of a single IGBT can be up to 1.2 kA and 3.3 kV. It has good switching capability (up to 100 kHz for a few kW applications), but for very high power devices and applications the frequency is limited to some kHz. On the other hand, the main drawback is poor overcurrent capability, i.e. it cannot withstand more than the peak current it is designed for, even for a short period of time. Hence, the current that would flow through the IGBTs during voltage dips could have a destructive effect if the valves are not designed to withstand this current level.

In order to calculate the required current rating of the VSC valves to ride through voltage dips occurring at the grid, the maximum current has been calculated for all the dip types. The current components in *dqp*- and *dqn*-frame are calculated using the following assumptions:

1. No switching-losses, which means that the AC active power P_1 of the converter is equal to the DC input power KP_{dc}.
2. In addition, the oscillating powers that are produced due to the imbalance are assumed to be supplied from the VSC side to simplify the calculations.
3. Furthermore, for simplicity, the phase angle jump is assumed to be zero, which results in zero *qp*- and *qn*-components of the grid voltage as seen by Table 3.2.
4. Moreover, perfect tracking is assumed, resulting in equal reference and actual currents.

Using (2-26), the grid currents are described as

$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \frac{KP_{dc}}{e_{dp}^2 - e_{dn}^2} \begin{bmatrix} e_{dp} \\ 0 \\ -e_{dn} \\ 0 \end{bmatrix} \tag{3-4}$$

where P_{dc} is the nominal input DC power and K is the ratio of the input power that is actually delivered to the DC link. The current components are then transformed back to the $\alpha\beta$-coordinates in positive- and negative-sequence frames and then into three-phase currents.

In the case of single phase faults (dip types "B" and "D"), the maximum phase current (phase *a*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp} + e_{dn}} \tag{3-5}$$

while for two phase faults (dip types "C", "E", "F", and "G"), the maximum phase current (phase *b*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp}^2 - e_{dn}^2} \sqrt{\frac{1}{4}\left(e_{dp} - e_{dn} \right)^2 + \frac{3}{4}\left(e_{dp} + e_{dn} \right)^2} \; . \tag{3-6}$$

For three phase faults (dip type "A"), the maximum phase current is

$$I_{max} = \sqrt{\frac{2}{3}} . \frac{K P_{dc}}{E \times V_{dip}} . \tag{3-7}$$

The values of e_{dp} and e_{dn}, which are the positive and negative sequence of the *d*-component of the grid voltage, are calculated using Table 3-2 for different voltage dips.

A comparison between the analytically calculated current values and the simulated ones has been performed for all dip types, in order to verify the analytical equations. For instance, the result with dip type "A" is shown in Fig. 3.4[8], where the simulation[9] has been carried out for the L-filter case. It will be shown later that the currents produced with the LCL-filter have the same amplitudes as for the L-filter, using the same value of the series inductance. As shown by the figure, the calculated curve shows overestimated current values, since the dissipated powers by the filter were

[8] Another example is shown in Paper A.

[9] The simulation has been carried out here in MatLab/Simulink.

neglected in the design equations while they were incorporated in the simulation.

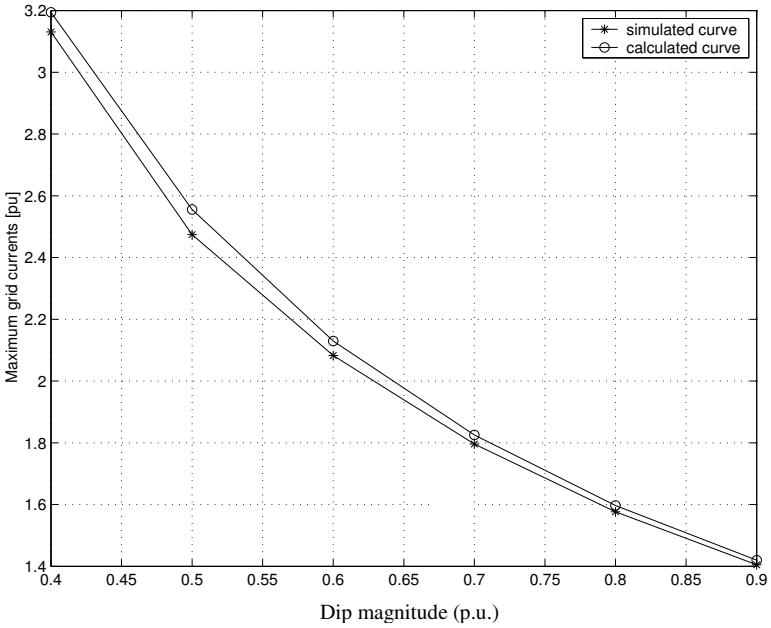

Fig. 3.4 Maximum currents due to voltage dip of type "A".

3.6 Ride-through capability for DGs with L-filter

Depending on the maximum currents that could flow during different voltage dips and using some statistical data regarding the most frequent dip types at the grid, the converter switches could be designed to withstand the increased currents. The peak-to-peak DC-link voltage in case of grid-voltage dips should also be considered in the design of the DC-link. However, the DC-link voltage ripples are found to be negligible when the oscillating powers that are resulting due to the grid-voltage imbalance, are assumed to be supplied from the grid side. This case has been found to be the optimal one for the controller design, if ride-through capability is to be considered.

The effect of all types of dips, with various magnitudes and zero phase angle jump, on the maximum grid current and DC voltage ripples is represented in Fig. 3.5. The maximum current the converter switches should

be able to hold is 3.65 p.u., which happens at 30% dip type “D”. The maximum DC voltage ripple is about 2.5% peak-to-peak and it occurs at 30% magnitude of dip type “F”.

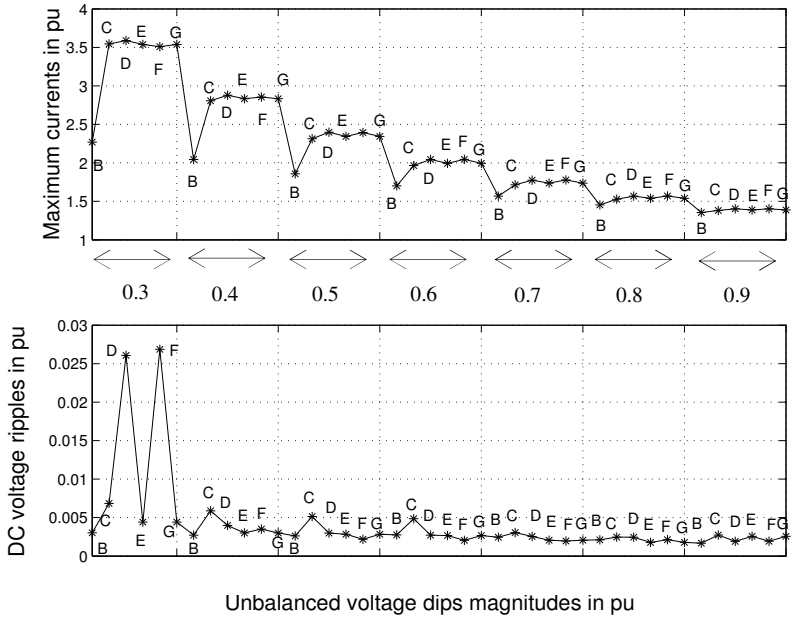

Fig. 3.5 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types.

The effect of the phase angle jump on the DC-link voltage ripples during the dip is found to be negligible. However, their effect over the maximum grid currents is more noticeable as shown in Fig. 3.6. It can be concluded that differences are very small for $\alpha = 10^{o}$ and $\alpha = -20^{o}$ while they seem to be significant when $\alpha = -60^{o}$. In that case the maximum current, with 30% magnitude of dip type “D”, is equal to 4.5 p.u. If the converter valves are designed considering the case of zero phase angle jump, they will be able to handle only 3.65 p.u. current as mentioned previously. Hence, in the case of a voltage dip with phase angle jump, the valves would most probably be destroyed or the VSC will be tripped off.

Moreover, from (3-5), (3-6), and (3-7), it is obvious that there is a direct proportionality between the maximum current and the value of the actual input power. In other words, if the input power is lowered by the ratio *K*, the maximum value of the current will also be lowered by the same ratio. Simulation results presented in Fig. 3.7 represent the effect of lowering the input power P_{in} for different dip types and magnitudes.

Therefore, if the converter switches have to be rated to ride through all dips with 30% minimum magnitude, the current rating can be decreased from about 3.5 p.u. to 3 p.u., if the input power is decreased from 90% to 70% of nominal value.

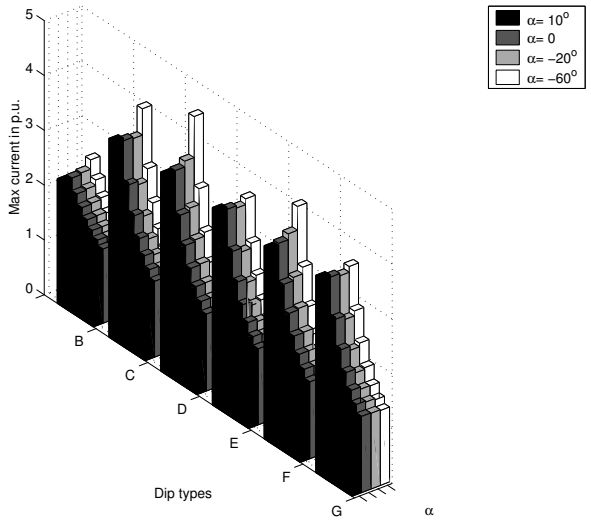

Fig. 3.6 Effect of phase angle jump on the amplitude of phase currents for different unbalanced voltage dips.

One way to optimise the design of the switches is thus to minimize the currents during the fault period, which could be established by temporarily decreasing the input power to the system (decreasing *K* in (3-5), (3-6), and (3-7)) during the fault. If this is possible or not depends on the controllability and the response time of the DC-link or the primary source. By incorporating a DC-chopper, acting as a dump load, or DC energy storage, the input power

could be reduced during the voltage dip period [9]. In addition, for some primary sources it could be possible to reduce the input energy (e.g. by changing the turbine torque reference in wind turbine systems) [36].

On the other hand, if the DC bus is powered by a source that is stochastic in nature, e.g. wind, one could argue that the probability that a dip occurs when the wind turbine is producing full power might be very low, as the turbine often runs at much lower power. Then, to optimize the design it is possible to consider a lower value of the input power, which is delivered by the turbine. This means, accepting a certain risk that the converter (thus the turbine) might still trip, but can lead to greatly reducing the size of the converter[10].

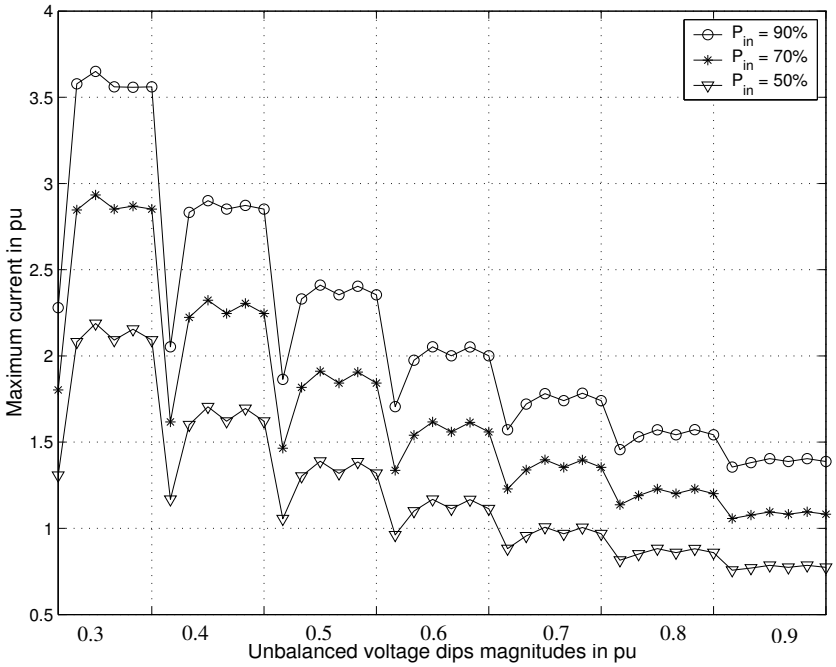

Fig. 3.7 Effect of lowering P_{in} on maximum grid currents for unbalanced voltage dips with magnitudes from 0.3 p.u. to 0.9 p.u. in steps of 0.1. The voltage dip types are shown analogously to Fig. 3.5.

[10] This is investigated numerically by the case study in Paper A.

3.7 Ride-through capability for DGs with LCL-filter

The effect of all unbalanced dips, with various magnitudes, on the maximum grid current and DC voltage ripples (in the middle of the dip period) is presented in Fig. 3.8. The base for the per unit currents is the maximum of the nominal current of the converter. Compared with the case of L-filter interface system (shown in Fig. 3.5 with a current base value equal to the RMS of the nominal current), the currents are almost the same while the DC voltage ripples are slightly increased but still within an acceptable range. This is mainly due to the part of the oscillating power consumed by the filter capacitor and not compensated for in the generated reference currents.

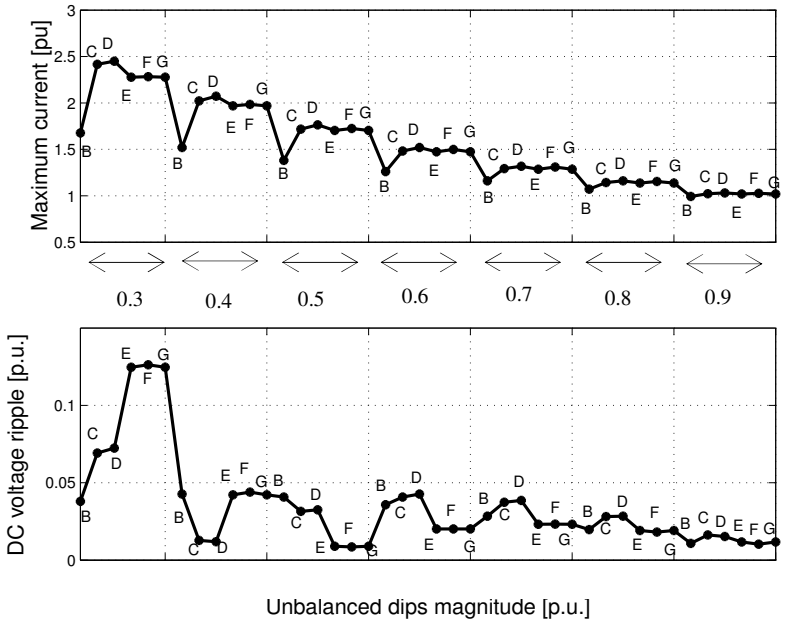

Fig. 3.8 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types and magnitudes from 0.3 to 0.9.

3.8 Conclusions

In this chapter, the effect of different voltage dips over the grid currents and DC-link voltage ripples are examined for the L-filter and the LCL-filter systems. The effect of the phase angle jump has also been examined considering the case when the grid supplies the oscillating powers. It is concluded that the phase angle jump has more effect on voltage dips with smaller magnitudes, and the worst case occurs when the impedance angle $\alpha = -60^{o}$, which corresponds to cable transmission. This effect is more significant for dip types "C" and "D". The maximum current occurs with 30% magnitude of dip type "D" and is equal to 4.5 p.u., i.e. 25% more than its value in case of zero phase angle jump. Thus, the effect of the phase angle jump should be considered when designing the converter switches to ride through all dips.

Since the two considered line filters produce almost the same current amplitudes, having the same value of series inductance, the design equations that have been derived here to calculate the required current ratings of the converter can be used for both systems. These equations give slightly over-estimated values since they are derived without considering the power dissipated in the filter. However, this over-estimation is preferred in the design stage because it gives a safety margin to the design values.

The effect of decreasing the input power has also been examined. Temporarily decreasing the input power to the system during fault reduces the currents during that period, which could be a way to decrease the ratings of the converter valves and in the same time preserving the ride-through capability. This, however, would require that the input power to the DC bus be controllable so as to be reduced very quickly.

Chapter 4

Voltage-Regulation Capability in Weak Grids

By adding a voltage-regulation capability to the DG controller, it is possible to mitigate most of the power quality problems. In addition, this is a highly attractive feature in case of the operation in weak grids. This is the topic of this chapter, where the regulation capability is examined for the mitigation of the decrease of the voltage amplitude specifically in weak grids, the voltage harmonics, and the voltage fluctuation. The DG system with a VSC as a front end and an LCL-filter is considered throughout this chapter. The voltage regulation limits are evaluated regarding the local load of the DG and the DG injected active power. Moreover, the effect of the grid voltage distortion over the phase-angle estimation and the regulation capability is studied. A phase-locked loop (PLL) synthesis based on the extraction of the fundamental component of the grid voltage has been introduced to obtain robust phase estimation.

4.1 Introduction

The term weak grid is here referring to systems where the voltage level is not constant as in a stiff (or strong) grid. Weak grids are usually found in remote areas where the feeders are long. The grids in these areas are usually designed for small loads [32]. When the design load is exceeded, the voltage level may fall below the allowed minimum and/or the thermal capacity of the feeders might be exceeded. Hence, the voltage regulation of long weak distribution lines is an important problem to be considered [30]. The connection of a DG in a weak distribution system can provide voltage support, if the voltage regulation capability is added to its controller, in addition to the main function of injecting active power into the grid. Moreover, by regulating the voltage at the PCC most of the power quality

problems could be mitigated, which might be an attractive requirement in grids with large number of disturbing (non-linear) as well as sensitive loads.

In recent publications, the voltage regulation problem is mainly tackled, in transmission or distribution systems, regarding the power electronics application, using a STATCOM (called DSTATCOM in distribution systems), which is a converter-based shunt connected reactive-power generator. The advantages of a STATCOM, compared to the other thyristor-based reactive power generators (SVCs), are its wider operating area, better performance, and greater application flexibility [75]. The implementation of the DSTATCOM has been discussed in [37], [38] and [58], [60] for voltage flicker mitigation, controlling both the active and the reactive injected powers. In [31] a DSTATCOM is used to regulate and balance the voltage at the distribution bus using only reactive power injection. The voltage regulation limits, however, have not been discussed. Although the application of a STATCOM and a DG are similar in the utilization of a converter as a front end, they are different from the point of view of the active power. STATCOMs could have controllable active power (depending on the grid needs) if they are connected to an energy storage device, while DGs are injecting constant active power that could change due to the changes in the energy source. The DG constant injected active power, consequently, puts some limits on the voltage regulation capability as will be investigated later in this chapter.

The voltage regulation using converter-interfaced DG systems, specifically with LCL-filters at the connection point to the grid, has been less introduced in literature since the emphasis is usually set on the DG technology, not from the power system point of view, and the DG system controllers. Still an example for such a system is found in [32], where a single phase VSI interface of a photovoltaic DG connected to a weak grid through an LCL-filter is considered regarding the voltage regulation purpose. The control algorithm measures the phase of the terminal voltage using Fourier extraction and then computes the required inverter voltage for the desired active and reactive power export commands. The feedback of the filter states has been used to provide the stability of the controller at higher

frequencies. The control of the real and the reactive power flow is done on a cycle-by-cycle basis. Hence, it takes several cycles for the system to settle. Although in [33] the application of a variable speed wind turbine (VSWT) system connected to a weak grid is considered, the emphasis has been placed on the control of the converters for the system and the voltage compensation has been of no interest. The compensation for grid-voltage harmonics has been the main topic of [78], where an inverter-based DG with an L-filter at the connection point to the grid has been considered. Three adaptive regulator gains have been calculated for the 5^{th}, the 7^{th} and the higher harmonics to produce the proper current commands. The focus has been put only on the voltage harmonic compensation, hence the voltage regulation is not considered and the controller takes long time to reach the steady state.

In this chapter, the cascaded controller for the DG system with an LCL-filter[11] is implemented along with a point of common coupling voltage regulator to add the voltage regulation capability. The voltage regulation capability limits are also discussed regarding the DG local load and the DG injected active and reactive powers. Since the output voltage of the VSC is synchronized with the grid voltage using an estimated phase angle, the error in this angle that is mainly due to the distorted grid voltage, should be minimal. The grid voltage phase angle is estimated using a phase locked loop (PLL), which is implemented in the *dq*-frame using a PI controller that tracks the changes in the *q*-component grid voltage by producing the necessary change in the phase angle. This PLL has been well established before [53], however it is first explained here since it will be modified in order to eliminate the effect of the grid voltage power quality problems on the estimated phase angle.

4.2 Phase locked loop (PLL)

The synthesis of the PLL that is commonly used for grid-connected three-phase power conversion systems [53] is based on the quadrature-component extraction of the grid voltage. Hence it will be referred to, here, as a Q-PLL.

[11] This controller has been explained in Chapter 2.

Assuming a balanced three-phase grid voltage at the point of common coupling (PCC)

$$u_{\mathrm{a(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\theta\,, \tag{4-1}$$

$$u_{\mathrm{b(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta - \frac{2\pi}{3}\right), \tag{4-2}$$

and

$$u_{\mathrm{c(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta + \frac{2\pi}{3}\right) \tag{4-3}$$

where U_{PCC} is the line RMS voltage at the PCC, and θ is its phase angle.

Transforming the voltage from three-phase notation into a voltage vector in a fixed $\alpha\beta$-frame, using power invariance transformation, the resulting voltage vector will be

$$\underline{u}_{\alpha\beta} = U_{\mathrm{PCC}}\left(\sin\theta + \mathrm{j}\cos\theta\right). \tag{4-4}$$

Normalizing this voltage vector and transforming it into a rotating dq-coordinate system, which rotates with the estimated angular frequency ($\hat{\omega} = \mathrm{d}\hat{\theta}/\mathrm{d}t$), the resulting normalized voltage-vector components will be

$$\underline{u}^{\mathrm{n}}_{\mathrm{dq}} = \cos\left(\theta - \hat{\theta}\right) + \mathrm{j}\sin\left(\theta - \hat{\theta}\right) \tag{4-5}$$

where $\hat{\theta}$ is the estimated phase angle.

If the estimation error ($\varepsilon = \theta - \hat{\theta}$) is very small, then $u^{\mathrm{n}}_{\mathrm{d}} \cong 1$ (the real part in (4-5)) and $u^{\mathrm{n}}_{\mathrm{q}} \cong \varepsilon$ (the imaginary part in (4-5)). Hence, the normalized q-component of the voltage can be used as an input to a PI-controller to produce a required change in the angular frequency ($\Delta\omega$) to track the changes in the phase angle. The Q-PLL main block diagram is shown in Fig. 4.1.

The on-line normalization of the voltage vector will result in nullifying the phase estimation error due to a balanced voltage amplitude change (e.g. three-phase voltage dips). However, in case of unbalanced voltage dips,

oscillations with double the fundamental frequency of the grid will be superimposed on the estimated frequency. These oscillations will result in an error in the estimated phase-angle of the grid-voltage.

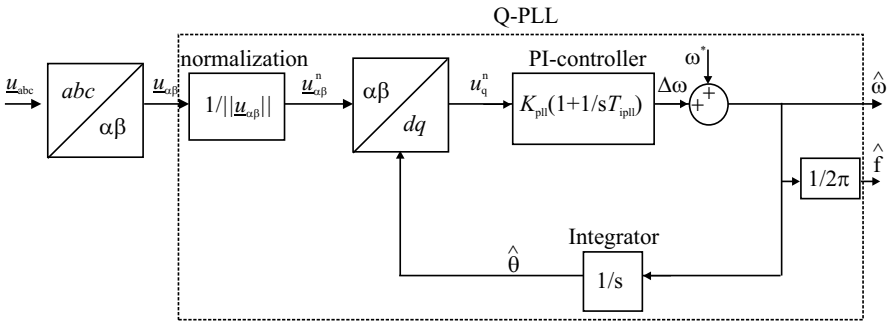

Fig. 4.1 Phase estimation using Q-PLL.

To eliminate this error, the positive sequence of the voltage-vector *q*-component is used as an input to the Q-PLL. This PLL is referred to as a positive sequence PLL (PS-PLL). This PLL is implemented in [55] and [56] by the use of low pass filters (LPF). However, a trade-off has to be made between robustness and good transient performance of the LPFs. Hence, it is instead implemented here as suggested in [57] using the delayed signal cancellation algorithm (DSC) to extract the positive sequence component of the voltage. As shown in Fig. 4.2, the three-phase voltages are measured and transformed into a vector in the stationary αβ-frame. Then the positive sequence voltage vector is extracted using the DSC algorithm, and fed into the Q-PLL that has been described in Fig. 4.1.

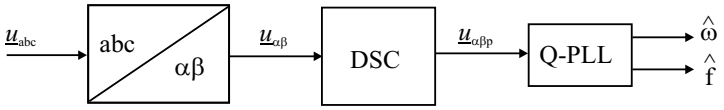

Fig. 4.2 Positive-sequence PLL.

To investigate the effect of the voltage imbalance on the PLL performance, an unbalanced voltage dip of type "C" and remaining voltage amplitude of 0.4 p.u. is applied from 0.5 s to 0.7 s. The estimated frequency

using the Q-PLL and using the PS-PLL are shown in Fig. 4.3 by the middle and lower plots respectively. The estimated frequency using PS-PLL is fairly unaffected by the unbalanced voltage dip apart from the transients at the start and the end of the dip. These transients last for one quarter of the fundamental period and they are resulting due to the implementation of the DSC.

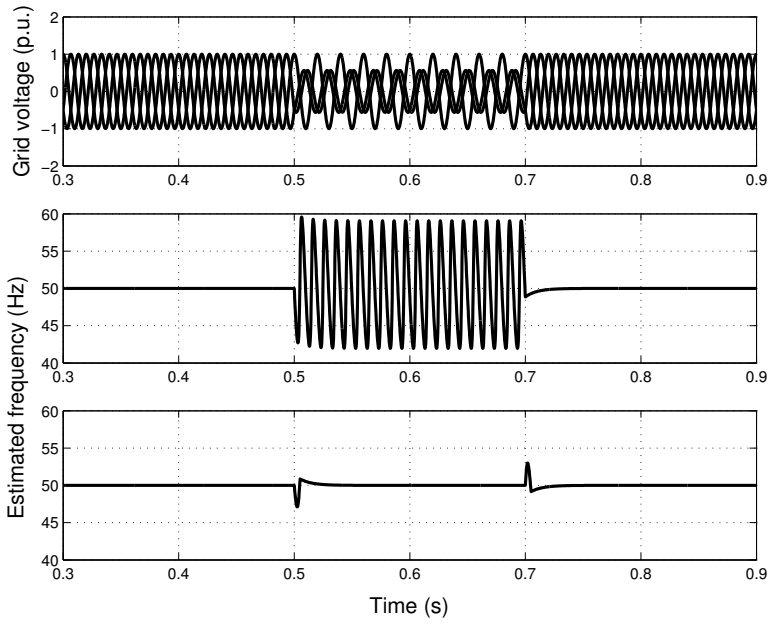

Fig. 4.3 Grid voltage (upper), and estimated frequency using Q-PLL (middle) and PS-PLL (lower).

4.3 PCC-voltage regulation limits

The voltage-regulation capability limit of a converter-interfaced DG is mainly related to the need for the DG to inject constant active power into the grid. To investigate this limit further, the simple weak grid system that is shown in Fig. 4.4 is considered. The parameters that are used for the weak-grid system are listed in Appendix C. For simplicity, it is assumed that the grid impedance Z_s is pure reactive ($Z_s = j\,X_s$). The grid is supplying a load at

the far end of the feeder, where a DG is also connected. It is assumed first that the load is disconnected and the DG is supplying both active power P_{DG} and reactive power Q_{DG} to the grid.

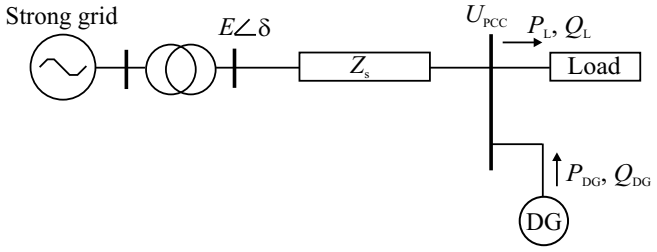

Fig. 4.4 Direction of power flow from VSC to PCC.

The power flow through the system is described by [54]

$$P_{DG} = \frac{U_{PCC}E}{X_s}\sin\delta \tag{4-6}$$

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \frac{U_{PCC}E}{X_s}\cos\delta \tag{4-7}$$

where E is the strong grid RMS line voltage, and δ is the grid voltage angle.

Using (4-6), the adjacent side for the angle δ can be calculated. Then

$$\cos\delta = \frac{\sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}}{\frac{U_{PCC}E}{X_s}}. \tag{4-8}$$

Substituting (4-8) in (4-7), Q_{DG} is obtained as

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}\ . \tag{4-9}$$

The voltage at the strong grid bus E is assumed to be equal to 1 p.u. Since the application of a DG requires injecting constant active power to the grid, the change in the reactive power leads to a change in the voltage at the PCC

(U_{PCC}) as suggested by (4-9). However, the value of the input active power affects the amount of the reactive power that is available for the compensation. A higher value of the injected active power implies that a higher value of reactive power can be injected, considering the same equation. Yet, that implies higher injected current, which could be an issue for the VSC valves capacity and protection[12], and also the increase of the DC-link voltage ripples might be another issue. An illustration of this is presented in Fig. 4.5[13], where the voltage regulation capability has been examined for a case when the grid voltage has a modulating signal with an 8% amplitude superimposed on the fundamental component. The input power from the DG source has been varied from 70% to 140% of the nominal value.

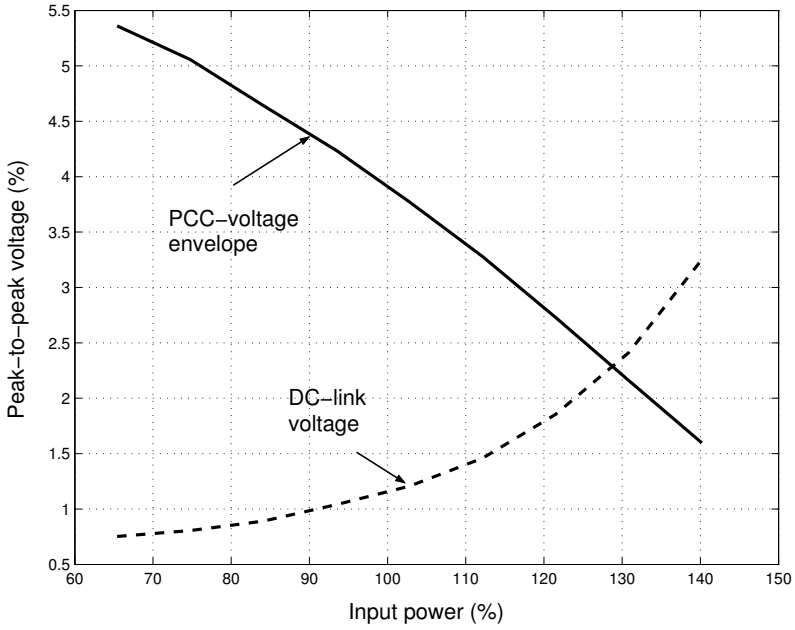

Fig. 4.5 Effect of the injected input power on the PCC voltage envelope oscillation (solid) and DC-link voltage ripples (dashed).

[12] That has been discussed in the previous chapter and in Paper A.
[13] Further details are provided in Paper E.

With the voltage regulation capability, the PCC-voltage has been better regulated at the upper value of the injected active power, where the grid voltage amplitude modulation has been reduced to 1.5%. On the other hand, the DC-link voltage ripples has increased to about 3.2% of its nominal value. Although negligible in value, in this example, the DC ripples amplitude could have a more significant value, for instance, if the amplitude of the modulating signal increases.

Equation (4-9) can be rearranged as

$$P_{\mathrm{DG}}^2 + \left(Q_{\mathrm{DG}} - \frac{U_{\mathrm{PCC}}^2}{X_{\mathrm{s}}} \right)^2 = \left(\frac{U_{\mathrm{PCC}} E}{X_{\mathrm{s}}} \right)^2 . \tag{4-10}$$

Equation (4-10) represents a circle with the radius of $U_{\mathrm{PCC}}E/X_{\mathrm{s}}$ and the centre at $(0,U^2_{\mathrm{PCC}}/X_{\mathrm{s}})$. By varying U_{PCC}, different power circles will result representing different possible operating points related to different values of the injected (or drawn) DG active and reactive powers. Those power circles have been illustrated in Fig. 4.6, where only the possible operating area has been shown (for the PCC voltage varying between 0.5 p.u. and 1 p.u.).

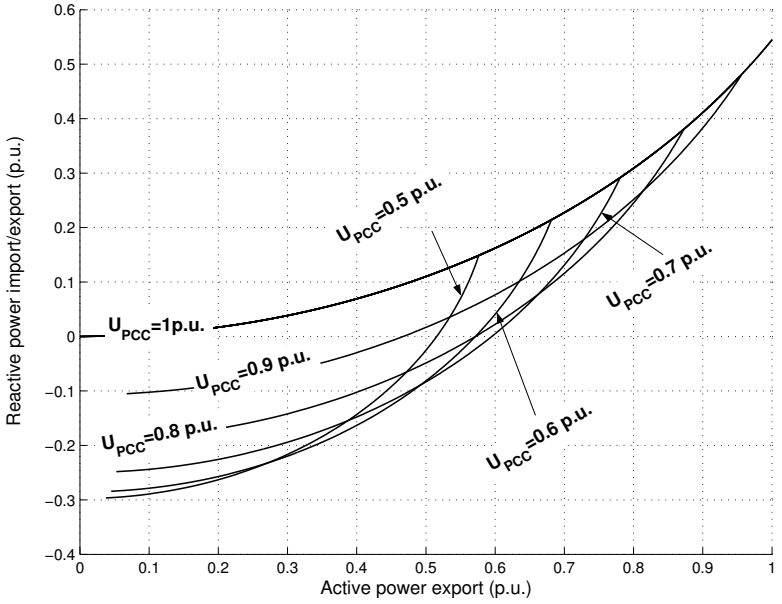

Fig. 4.6 DG import/export power with unloaded weak grid for different PCC voltages.

The figure is indicative of the amount of the reactive power to be injected by the DG at a specific value of the injected active power and a certain voltage drop over the feeder. For instance, for a PCC voltage of 0.7 p.u. and injected active power of 0.5 p.u., the injected reactive power should equal to the difference between the two values resulting from the intersection of the 0.5 p.u. power line and the two circles related to the PCC voltages of 1 p.u. and 0.7 p.u. (in this example, the injected reactive power will be about 0.2 p.u.). For the same PCC voltage (0.7 p.u.), if the DG injected power is 0.8 p.u., this operating condition will represent an unstable operation since the 0.8 p.u. power line does not intersect with the 0.7 p.u. circle.

To calculate the maximum reactive power that should be injected to regulate the voltage at the PCC with different voltage drops, (4-9) is differentiated with respect to the PCC voltage U_{PCC} and the result is set to zero. Then the resulting voltage that would acquire maximum injected reactive power is U_{limit}

$$U_{\mathrm{limit}} = X_{\mathrm{s}} \sqrt{\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2} \ . \tag{4-11}$$

The reactive power lower limit Q_{limit} that will result in maximum injected DG reactive power (to regulate the PCC voltage) is then related to the DG injected active power as

$$Q_{\mathrm{limit}} = X_{\mathrm{s}} \left(\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2 \right) - \frac{1}{2X_{\mathrm{s}}} \, . \tag{4-12}$$

Equation (4-12) is depicted in Fig. 4.7, where it shows again that the maximum power to be injected is inversely proportional to both the PCC voltage and the DG injected active power. The difference between the two curves in the figure indicates the necessary injected reactive power.

To investigate the effect of the loading on the compensation capability of the DG, it is now assumed that a static constant-power load is connected at

the PCC in Fig. 4.4. With a constant-power load, the power circles would be shifted up and/or to the right depending on the load reactive and active powers respectively. This should, in turn, increase the voltage compensation limit of the DG. However, an increased amount of the load reactive power, shifting the circles up, will imply more DG injected reactive-power to compensate for the voltage.

Assuming a constant active power load of 0.1 p.u., the operational part of the power circles relating the DG active and reactive powers to the grid voltage at the PCC is shown in Fig. 4.8. For instant, if the voltage at the PCC is 0.7 p.u. and the input DG active power is 0.8 p.u., then this will imply a stable operation with about 0.1 p.u. reactive power to be injected into the grid to regulate for the voltage.

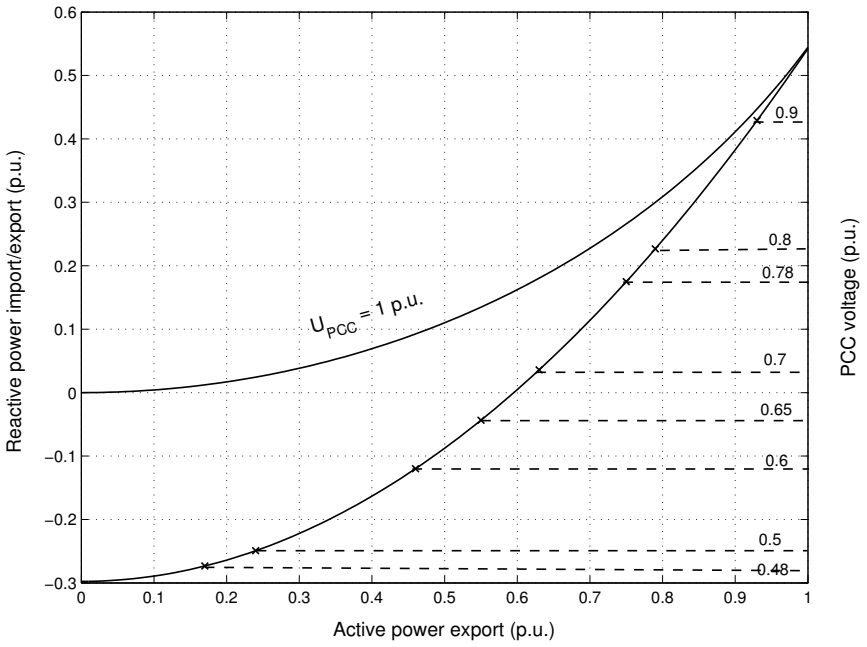

Fig. 4.7 Maximum reactive power (i.e. vertical difference between the two curves) to be injected related to the PCC voltage and the DG injected active power.

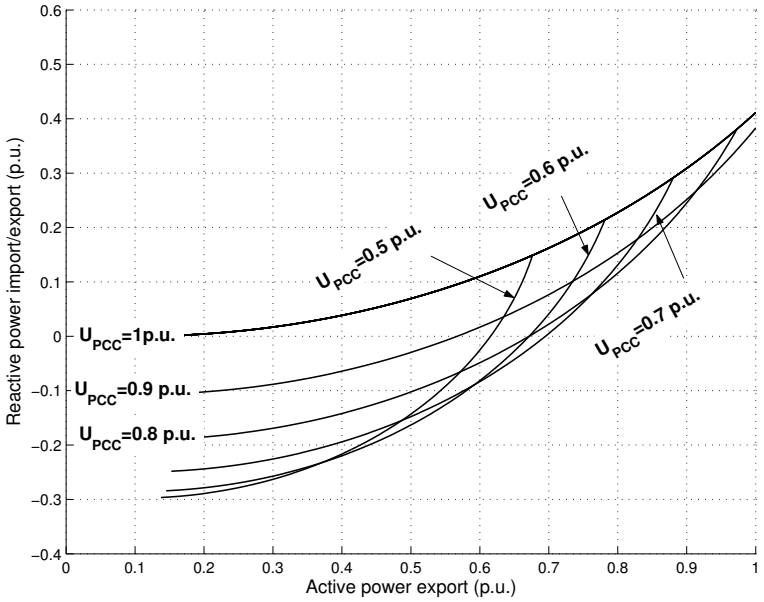

Fig. 4.8 DG import/export power with a constant power load of P_L = 0.1 p.u. and Q_L = 0.0 p.u.

It is worth noting here that the above discussion has been carried out assuming a lossless feeder. By decreasing the *X*/*R* ratio of the feeder, the resistive voltage drop will increase implying decreased PCC voltage related to the same loading condition. For instance, for a pure resistive feeder (Z_s = R_s) the equations for the active and reactive power flow through the feeder will be reversed. That means

$$Q_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}E}{R_{\mathrm{s}}}\sin\delta \tag{4-13}$$

$$P_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}^2}{R_{\mathrm{s}}} - \frac{U_{PCC}E}{R_{\mathrm{s}}}\cos\delta\,. \tag{4-14}$$

This implies that the voltage at the PCC will become more sensitive to the active power change and less sensitive to the reactive power change. This will result in an increased amount of the reactive power to regulate the

voltage compared to the case with a pure inductive feeder. Hence, the decreased *X*/*R* ratio will account for another limit for the regulation capability.

4.4 PCC-voltage regulator

The DG injected reactive power is adjusted by the PCC-voltage regulator to maintain the 1 p.u. grid voltage amplitude. The regulator has been implemented regarding the instantaneous reactive power generated by the DG at the PCC, which is described as

$$q_{(\mathrm{PCC})} = u_{\mathrm{q(PCC)}} i_{2\mathrm{d}} - u_{\mathrm{d(PCC)}} i_{2\mathrm{q}} . \tag{4-15}$$

Since the voltage-oriented synchronous-frame transformation sets the *q*-component of the voltage into zero, then $i_{2\mathrm{q}}$ is used to control the reactive power flow. Since $u_{\mathrm{d(PCC)}}$ is to be regulated, then the reactive current reference is generated to compensate the error in the voltage using a PI-controller[14], as follows

$$i_{2\mathrm{q}}^{*}(k) = k_{\mathrm{pr}} \varepsilon_{\mathrm{e}}(k) + \frac{k_{\mathrm{pr}} T_{\mathrm{s}}}{T_{\mathrm{ir}}} \sum_{n=1}^{k} \varepsilon_{\mathrm{e}}(n-1) \tag{4-16}$$

$$\varepsilon_{\mathrm{e}}(k) = u_{\mathrm{d(PCC)}}(k) - u_{\mathrm{d(PCC)}}^{*}(k) \tag{4-17}$$

where

k_{pr} is the proportional gain of the PCC-voltage regulator;

k is the sampling instant;

T_{ir} is the integral time; and

T_{s} is the sampling time.

Assuming, now, that the loading condition of the grid allows for a stable operation of the PCC-voltage regulator, the mitigation of the power quality problems at the grid is to be considered next.

[14] The controller parameters are given in Appendix D.

4.5 Compensation for grid-voltage harmonics

The effect of the voltage harmonics on the estimated phase using the PS-PLL is first discussed. If it is assumed that the voltage has a harmonic signal that is superimposed on the fundamental component, then it can be described in the αβ-frame as

$$\underline{u}_{\alpha\beta}(t) = U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \tag{4-18}$$

where

U_1 and U_h are the amplitudes of the fundamental and the h^{th} harmonic respectively;

ω is the fundamental grid-voltage angular-frequency; and

h_s is the related harmonic sequence that takes a value of either $+1$ (for positive sequence) or -1 (for negative sequence) according to [54]

$$h_s = \begin{cases} +1 & h = 3n+1 \\ -1 & h = 3n+2 \\ 0 & h = 3n \end{cases} \tag{4-19}$$

where n is a positive integer starting from zero.

The zero sequence harmonics will not be treated in this analysis due to the absence of a neutral wire.

Substituting (4-18) in (2-15), the positive-sequence vector of the grid voltage in $\alpha\beta-$frame is:

$$\begin{aligned} \underline{u}_{\alpha\beta\mathrm{p}}(t) &= \frac{1}{2}\left(U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t}\right) \\ &+ \frac{\mathrm{j}}{2}\left(U_1 e^{\mathrm{j}\omega(t-T_g/4)} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega(t-T_g/4)}\right) \end{aligned} \tag{4-20}$$

where $\dfrac{\omega T_g}{4} = \dfrac{\pi}{2}$.

The harmonic part of (4-20) can be expressed using trigonometric functions as follows

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = \frac{U_{\mathrm{h}}}{2}\left(\cos(h\omega t) + \mathrm{j}(h_{\mathrm{s}})\sin(h\omega t)\right) + \mathrm{j}\frac{U_{\mathrm{h}}}{2}\cos\left(h\omega t - h\frac{\pi}{2}\right) - (h_{\mathrm{s}})\sin\left(h\omega t - h\frac{\pi}{2}\right). \tag{4-21}$$

For the harmonics of the orders 5th and 7th, $\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}$ will be nullified since

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = -(h_{\mathrm{s}})\sin(h\omega t) \tag{4-22.a}$$

and

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = (h_{\mathrm{s}})\cos(h\omega t). \tag{4-22.b}$$

For harmonics of the orders 11th and 13th, the positive-sequence harmonic voltage vector will have the same amplitude as of the imposed harmonic signal and will rotate with the same angle. Equation (4-21) for the two harmonics will become

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = U_h e^{\mathrm{j}h_{\mathrm{s}}h\omega t}. \tag{4-23}$$

Since the 5th and 7th harmonics are the most dominant in the power system [54], it is expected that good results will be obtained using the PS-PLL in estimating the grid-voltage phase angle. Moreover, since the operation of the PS-PLL is similar to a LPF operation, the higher harmonics will be attenuated as well.

To investigate the capability of the voltage-harmonics compensation, a parallel RC-load is connected to the grid, through a diode rectifier, upstream of the DG. The phase-voltage at the PCC is shown in Fig. 4.9 before and after the connection of the DG. In addition, the harmonics content is also shown for both voltages in Fig. 4.10. The harmonics are comparatively negligible when connecting the DG, with the PCC-voltage regulation capability. For instance, the 5th harmonic component amplitude has decreased from about 9.5% without the DG to about 3% with the DG. This will result in a voltage that complies with the IEEE-std 1547-2003, which specifies the maximum harmonic voltage distortion as 4% for the harmonics' orders less than the 11th.

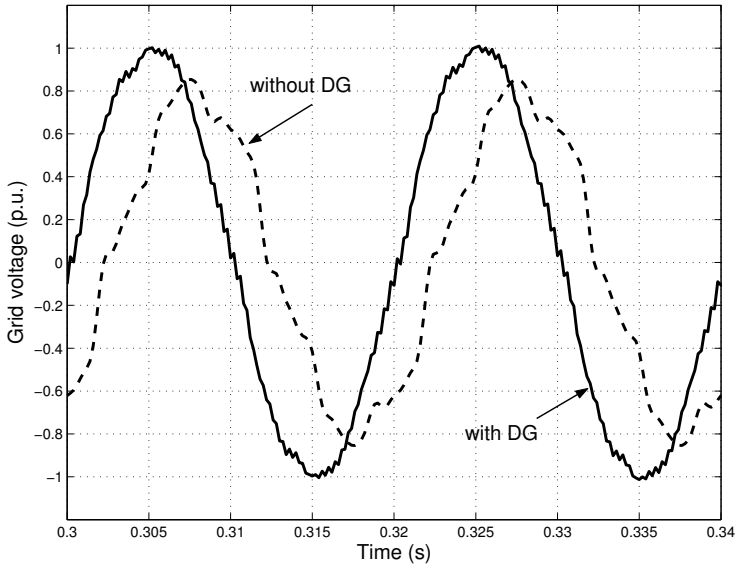

Fig. 4.9 Grid Phase-voltage with (solid) the DG and without (dashed) the DG.

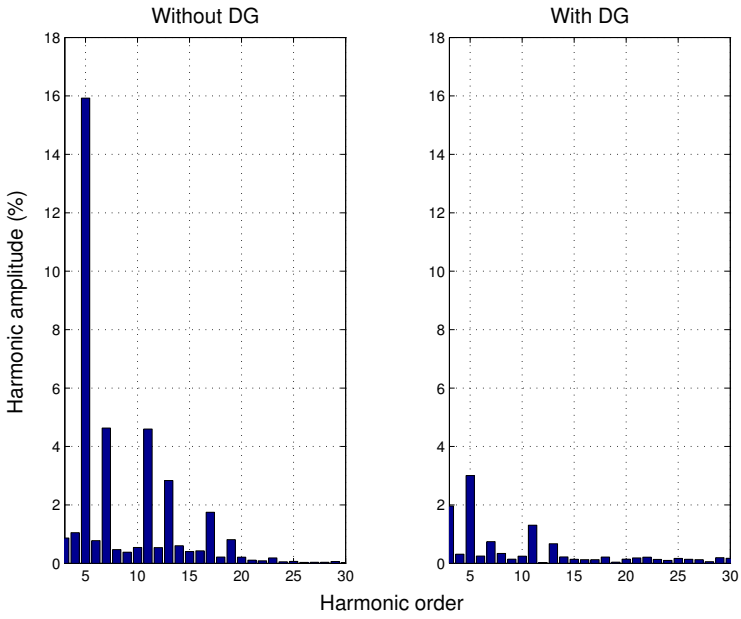

Fig. 4.10 Grid voltage harmonics content with the DG (right) and without the DG (left).

4.6 Compensation for grid-voltage fluctuation

Grid voltage amplitude fluctuations may result due to fast periodically-changing heavy loads that are connected to the grid [58]. If a distribution network is considered, one of the direct effects could be light flicker. The frequency of light flicker ranges between 0.5 Hz and 30 Hz, since this is the range of the human eye sensibility [59]. One way to mitigate this phenomenon is to compensate for the oscillating reactive power using a STATCOM [59] - [60], which is a three-phase VSC based device. The VSC-interfaced DG with the voltage compensation capability is considered here for that purpose.

Proposed PLL modification

The effect of the voltage amplitude modulation on the PS-PLL is first to be examined. For this purpose, a sinusoidal modulating signal is added to the voltage magnitude. With a variable voltage-amplitude, the q-component of the grid voltage will oscillate with the same frequency as the modulating signal. Substituting $h_s = 0$ and $h = 1/5$ (for 10 Hz amplitude modulation) in (4-21), it is obvious that the positive sequence will also be oscillating, producing an error in the estimated phase. To nullify this error and obtain a robust performance, the fundamental component of the grid voltage could be used, instead of the positive sequence component, as input to the Q-PLL. This has been implemented in [61] using two LPFs to extract both the positive-sequence and its fundamental component.

In order to cope with this situation, the adaptive linear neural network extractor (ADALINE) [62] is introduced next. A simple ADALINE consists of one neuron that has a linear input-output relationship, where each input is simply multiplied by a certain weight and all inputs are summed together to produce the output. The power of ADALINE comes from the on-line adaptation of its weights that gives it a non-linear property [62]. For this purpose, the least mean square (LMS) algorithm is used [63].

ADALINE has been implemented in [64] as a combiner to identify the voltage waveform for the classification of the power quality problems. It will

be used here in the same way, however, as an extractor to relieve the fundamental component of the source polluted voltage. The structure of ADALINE is shown in Fig. 4.11, where the discrete input vector $\mathbf{x}(k)$ is composed of sine and cosine elements of all possible frequency components that are contained in the source voltage

$$\mathbf{x}(k) = \left[\sin(\omega k T_s) \quad \cos(\omega k T_s) \quad \ldots \quad \sin(h\omega k T_s) \quad \cos(h\omega k T_s)\right]^T \tag{4-24}$$

where h is the highest harmonic order expected, k is the sampling instant, T_s is the sampling time, and the superscript T indicates the transpose of the vector. This input vector $\mathbf{x}(k)$ is then multiplied by a weight vector $\mathbf{w}(k)$ to produce the ADALINE output $u_{nn}(k)$, as follows

$$\mathbf{w}(k) = \left[w_{11} \quad w_{12} \quad w_{21} \quad w_{22} \quad \ldots \quad w_{h1} \quad w_{h2}\right] \tag{4-25}$$

$$u_{nn}(k) = \mathbf{w}(k) \cdot \mathbf{x}(k) = \sum_{i=1}^{2h} w_i x_i \tag{4-26}$$

where w_i and x_i is the i^{th} element in the vectors $\mathbf{w}$ and $\mathbf{x}$ respectively.

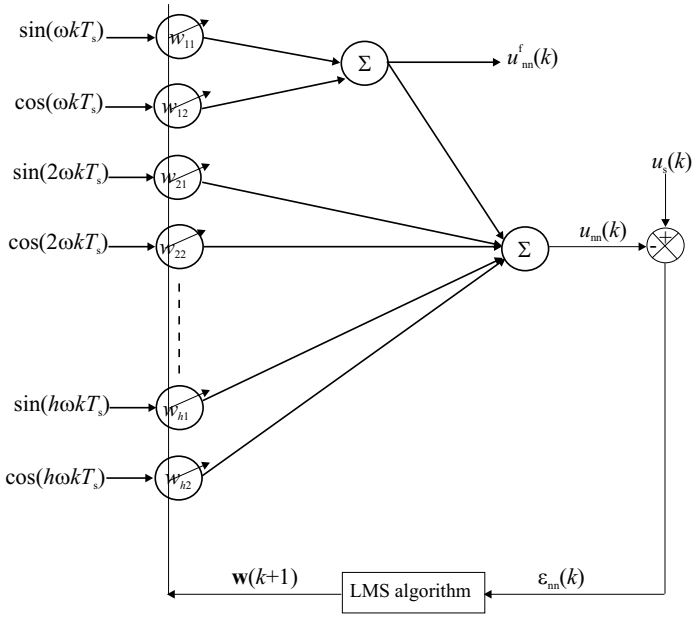

Fig. 4.11 The structure of the adaptive linear extractor (ADALINE).

The output is then compared with the measured and sampled voltage signal $u_s(k)$, where the resulting error ε_{nn} is used by the recursive algorithm to modify the weight vector according to

$$\mathbf{w}(k+1) = \mathbf{w}(k) + \lambda \frac{\mathbf{x}(k)\varepsilon_{nn}(k)}{\mathbf{x}(k)^{\mathrm{T}}\mathbf{x}(k)} \tag{4-27}$$

where λ is the learning factor. The size of λ determines how quickly old data are to be discarded. A small λ means that new data inputs will not have a significant weight and the system becomes less sensitive to disturbances, but also slower in reactions. On the other hand, a large λ makes the system react quickly, but responds more sensitively to disturbances[15].

The block diagram of the PLL implementing ADALINE (NN-PLL) is shown in Fig. 4.12. The three-phase voltage is transformed into the stationary $\alpha\beta$-frame. Then each component is fed into a separate ADALINE algorithm to extract the fundamental component that is fed into a Q-PLL.

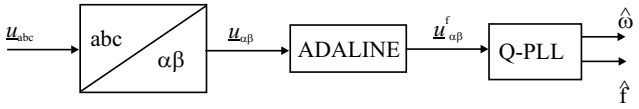

Fig. 4.12 Implementation of NN-PLL.

Performance of the proposed PLL

The performance of the NN-PLL is also compared to the PS-PLL regarding the grid voltage harmonics. The error in the estimated phase angle due to the grid voltage harmonics is shown in Fig. 4.13, using three different bandwidth values for the Q-PLL, for the two estimators. 2% amplitude of the 2nd, 4th, 5th, 7th, 11th and 13th harmonic orders has been superimposed separately on the fundamental grid-voltage. The phase error has been

[15] More discussion about the learning factor can be found in Paper E.

calculated as the peak-to-peak amplitude of the normalized quadrature-voltage.

With the PS-PLL, the error in the estimated phase-angle increases with higher values of the bandwidth. Moreover, the amplitude of the error increases with the increase of the harmonic order, excluding the case for the 5^{th} and 7^{th} harmonics at which it was proven that the error will be nullified. This can be understood by observing (4-17), where the harmonic order is in proportional relationship with the frequency of the oscillations superimposed on the fundamental grid-voltage.

Using the NN-PLL the error is nullified with all harmonic orders and all values of bandwidth, which means that it is robust and in the same time could have better dynamics. Moreover, the case of unbalanced harmonics has been examined with the same order of harmonics as before. Figure 4.14 shows that the NN-PLL is superior to the PS-PLL even when unbalanced 5^{th} and 7^{th} harmonics are present in the grid.

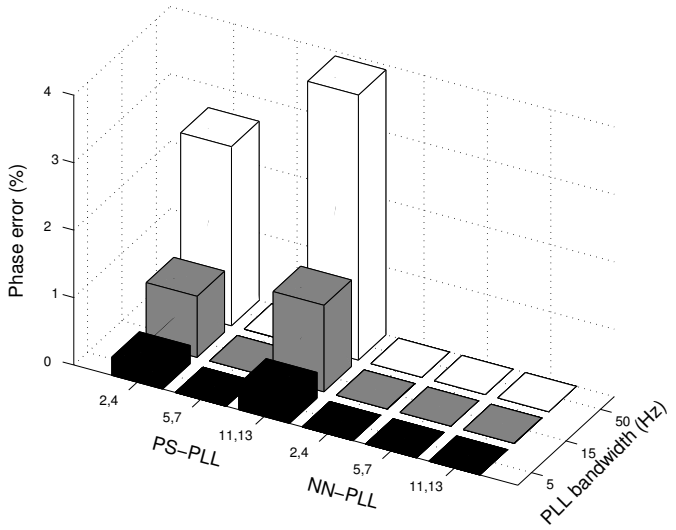

Fig. 4.13 Phase error due to different balanced harmonics using PS-PLL and NN-PLL with different BW values.

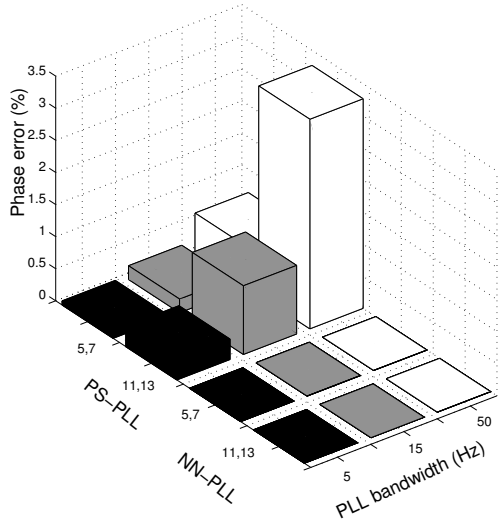

Fig. 4.14 Phase error due to different unbalanced harmonics using PS-PLL and NN-PLL with different BW values.

Mitigation of grid voltage amplitude fluctuation

The mitigation of the grid voltage fluctuation is to be examined. A fluctuating load is assumed to be connected at bus 1, in Fig. 4.4, and is further assumed to be disconnected in case of a fault at the same bus. Its effect is encountered as about 8% amplitude fluctuation of the grid voltage at bus 1 using a cosine modulation signal with a frequency of 10 Hz. In reality this modulation signal could have an infinite number of frequencies, but for the sake of clarity only a 10 Hz component is displayed here, which represents a value in the frequency band (between 2 and 15 Hz [58]) that the human eye is most sensitive to. The PCC-voltage is shown in Fig. 4.15 before the connection of the DG, and with the DG connected with the PS-PLL and the NN-PLL. From the figure, it can be concluded that the ability of the DG with an NN-PLL to mitigate the voltage fluctuation is better. The peak-to-peak voltage-envelope has been oscillating with 8% before the voltage compensation, and with 5% in case of voltage regulation using the PS-PLL and 3.5% in case of using the NN-PLL.

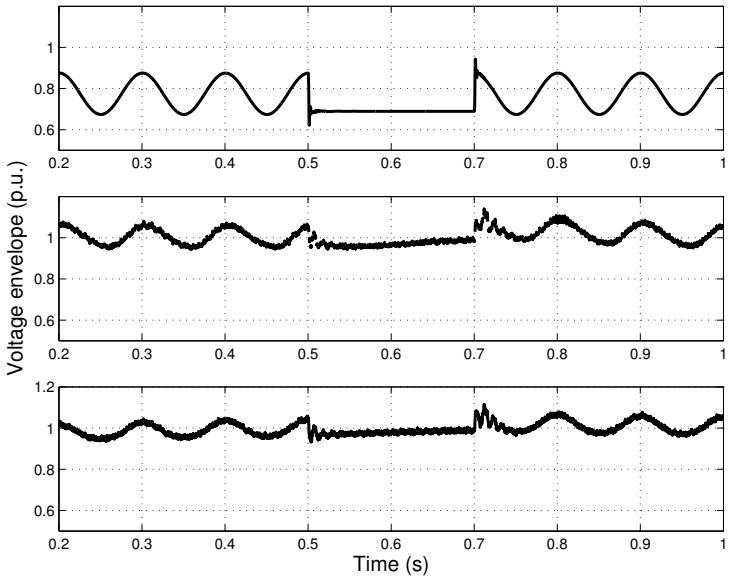

Fig. 4.15 Voltage envelop with DG disconnected (upper), DG with PS-PLL (middle), and DG with NN-PLL (lower).

Moreover, the voltage amplitude variation at the PCC has been tested with different modulation signal frequencies and the result is shown in Fig. 4.16, where the system using the NN-PLL has lower peak-to-peak value of the oscillation of the voltage envelope.

It is worth noting here that the oscillations of the voltage envelope will not be completely nullified since both the active and the reactive powers are oscillating at the grid, because of the modelling that is considered here. That means that both the injected active and reactive powers should be oscillating in order to completely compensate for the voltage fluctuation. However, this is not possible, here, since the application of the converter interfaced DG that is considered implies constant injected active power into the grid. On the other hand, the behaviour of the NN-PLL is dependent on the input-vector length, the order of harmonic frequencies used in that vector, and the initial weights' values. The input-vector length is taken, here, as 18 and the initial weight vector was set to zero. Using different setup for the ADALINE could give different results.

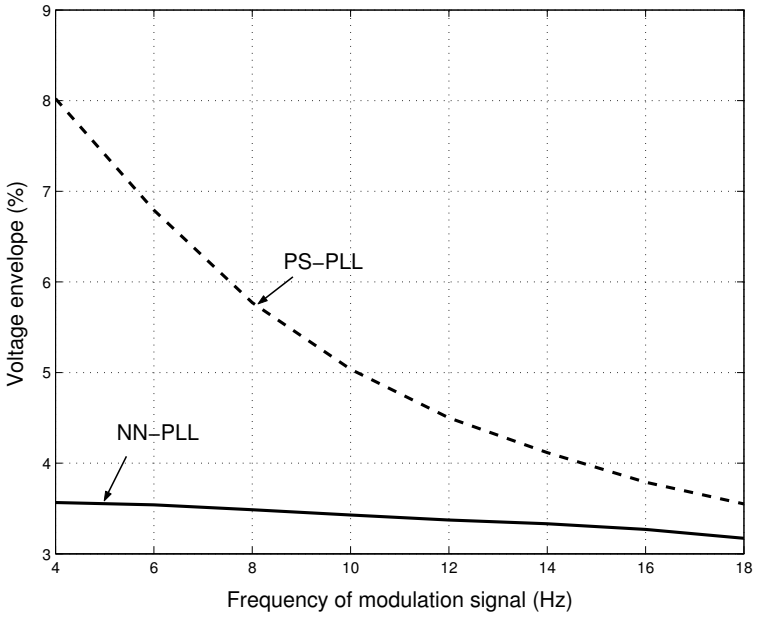

Fig. 4.16 Voltage amplitude variation owing to the change of the modulation signal frequency; with PS-PLL (dashed curve) and NN-PLL (solid curve).

4.7 Conclusions

The possibility to regulate the local voltage using a converter-interfaced DG has been discussed in this chapter. The aim is to maintain the voltage at its nominal value in case of operation in weak grids, and to mitigate the power quality problems at the point of common coupling (PCC). The voltage regulation capability has been investigated by studying the regulation limits regarding the DG injected power and the loading of the grid. The regulation capability is increased if the DG is injecting more active power into the grid and the load is mostly a constant active power load. However, this could require oversizing of the converter valves.

The PCC-voltage regulator sets the reactive current reference in such a way that the reactive power injected into the grid is controlled. The reactive current is represented by the quadrature-component of the measured current,

which is obtained through a coordinate transformation that uses an estimated angle that is obtained using a PLL. The error in the estimated angle could result in an erroneous reactive current command, which could affect the voltage compensation quality. For that purpose, the PLL algorithm has been discussed regarding the grid voltage imbalance, the grid voltage harmonics, and the grid voltage fluctuation. A neural-network based PLL (NN-PLL) has been proposed to extract the fundamental component of the grid voltage, and to estimate its phase angle. This NN-PLL has been compared with a previously investigated PLL algorithm (here referred to as PS-PLL), which estimates the phase angle of the positive-sequence component of the grid voltage. It has been shown that the NN-PLL is more robust against grid voltage harmonics. The NN-PLL has shown superiority also in the special case of unbalanced 5^{th} and 7^{th} harmonics in the grid voltage. In addition, the NN-PLL has proven to be better in case of grid-voltage fluctuation, where in a demonstrated case the oscillation of the voltage envelope has been decreased from 8% (without voltage regulation) to 3.5% (with voltage regulation and using NN-PLL), compared to 5% when using the PS-PLL.

Chapter 5

Intentional Islanding Capability

Intentional islanding refers to the case when the distributed generation (DG) is allowed to work autonomously to energize a part of the grid. For safe operation, detection methods should be applied to change the DG operating mode from grid-connected operation to island operation and vice-versa. Two different detection methods are described and examined in this chapter; namely passive and active methods. Their non-detectable zone is briefly discussed. The operation of the DG in both a strong grid and a weak grid has been examined in case of islanding.

5.1 Intentional islanding definition

Islanding refers to a condition in which a portion of the power system is energized by a local energy source, while it is electrically separated from the rest of the power system [65]. This situation, if not planned, poses a safety hazard to utility repair and maintenance personnel, and could lead to unstable island and instability problems when the utility grid is recovered [66].

Hence, islanding detection is an important aspect in DG applications. DGs should be able to detect the islanding condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, which specifies the acceptable clearing times as shown in Fig. 5.1. Yet, as recommended by the same standard, the detection could lead to an island operation of a DG, which is referred to as intentional islanding.

Besides enhancing the supply reliability for the utility grid [83] (e.g. in rural areas [4]), intentional islanding of DGs represents a required practice for some critical micro-grids [5], [84], [85]. Hence, developing reliable and robust islanding detection methods is of major importance.

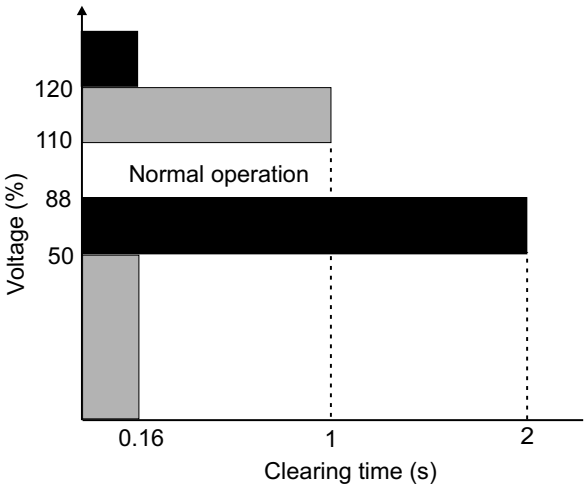

Fig. 5.1 Clearing time for a DG as described in IEEE-std 1547-2003.

5.2 Islanding detection methods

There are two types of islanding detection methods; passive and active. In passive detection algorithms, the sensed grid states (voltage, frequency … etc.) are compared with their nominal values and the deviations are used to decide on the islanding condition. For instance, in [10], the grid outage is detected using the phase angle error, between the grid voltage and the inverter voltage, which is compared to a set value to generate the disconnection signal. Then the DG operates in a stand-alone mode. When the grid is back, the increased currents are used to trip the DG. Then the DG is connected back to the grid after synchronization. Using the voltage phase-angle for islanding detection, however, may lead to false islanding in case of other power system dynamics [68]. Instead, in [40], both the voltage and the frequency are measured at the PCC to detect islanding. However, the effect of a voltage limitation, which could be incorporated in the converter controller for its safe operation, is not considered.

Although they are simple to implement, passive algorithms may fail to detect islanding if the load and generation on the island are closely matched

[67]. The active and reactive power mismatch limits that will lead to this situation are referred to as the non-detectable zone (NDZ) and they are calculated for current-controlled and power controlled DGs in [68] for different passive algorithms using an RLC-resonant load with a certain quality factor. It has been shown, in that reference, that the algorithms that are using the under/over frequency and/or the phase-angle jump are insensitive to active power mismatch. Moreover, the under/over frequency methods are, unlike the phase angle jump methods, dependent on the load quality factor. In addition, there are practical issues related to using phase-angle jump methods. Power system switching events, not resulting in islanding, can falsely trigger such schemes. When the islanding detection is delayed or not activated due to the NDZ, the DG system may lose control on its output terminal voltage, which may lead to island instability. In a way to overcome this problem and to provide seamless transfer between the grid-connected and island modes of operation, the island load (or emergency load) in [46] has been connected in parallel to the capacitor of the LCL-filter. Since the capacitor voltage is always controlled, even in the case of grid-detection failure, the load is not affected by the change of the DG operating mode, or the delay or mal-operation of the detection algorithm. However, this solution might not be feasible for all grids or loads. Another way is to decrease the NDZ by improving the detection method.

In active detection methods, the NDZ is very small [69]. Active techniques are usually incorporated within the controller, where they aim at disturbing the grid states by injecting disturbance signals. In the case of the utility supply outage, the island will be disturbed and the passive detection will succeed. In spite of the small NDZ, active methods may affect the power quality of the distribution system [39]. Moreover, in case of a weak grid system, active methods may lead to false tripping.

Hence, the passive islanding-detection method is considered first since it is the main islanding decision maker. Then, an active islanding detection method is introduced for the operation of the DG in both a strong and a weak grid.

5.3 Passive islanding-detection

A passive islanding detection algorithm has been developed to detect both the grid outage and recovery. To evaluate the grid states that could be reliable enough to be used in the detection algorithm, the grid outage is first considered.

The effect of the grid outage on the PCC-voltage

At the moment of the grid outage, the voltage at the point of common coupling (PCC) will either increase or decrease instantly depending on the sign of the power mismatch (ΔP and ΔQ in Fig. 5.2). The power mismatch represents the amount of power that the grid either delivers or absorbs in the normal operation. This power is equal to the power absorbed by the load at the PCC subtracted from the power injected by the DG, as designated in Fig. 5.2[16]. If the DG injected power is higher than the load absorbed-power, then the PCC-voltage will increase implying increased $u_{\mathrm{d(PCC)}}$. In that case, the increase of the voltage will be limited by the voltage limitation algorithm incorporated in the DG controller. Regarding the algorithm that has been implemented here, $u_{\mathrm{d(PCC)}}$ will be limited to $\frac{u_{\mathrm{dc}}}{\sqrt{2}}$ as has been shown in Section 2.2.

This case is presented in Fig. 5.3, where the grid outage occurs at 0.4 s. The DG controller that has been tested here has the PCC-voltage regulator and the DC-link voltage regulator incorporated. Hence, the *d*-component of the DG injected-current is controlled to be constant to keep the DC-link voltage constant, as shown by the lower plot in Fig. 5.3, while the *q*-component of the current starts to decrease in magnitude after the grid outage to retain the voltage at its nominal value. Since the PCC-voltage amplitude is limited (due to both the limiting algorithm and the operation of the PCC-voltage regulator), this increase in the grid voltage could also correspond to any other dynamics at the grid (e.g. load disconnection), then the over-voltage state cannot be a measure for islanding.

[16] The feeder parameters are given in Appendix C.

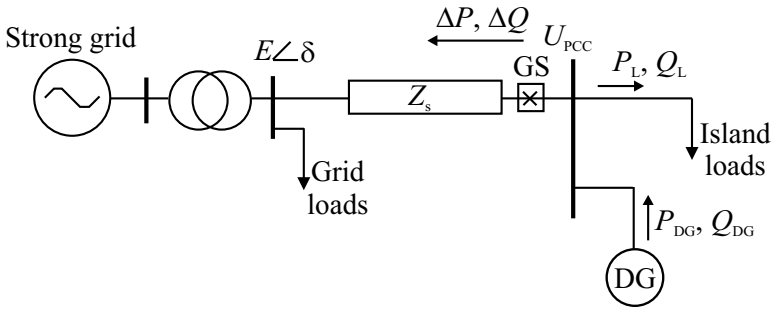

Fig. 5.2 System considered for islanding study.

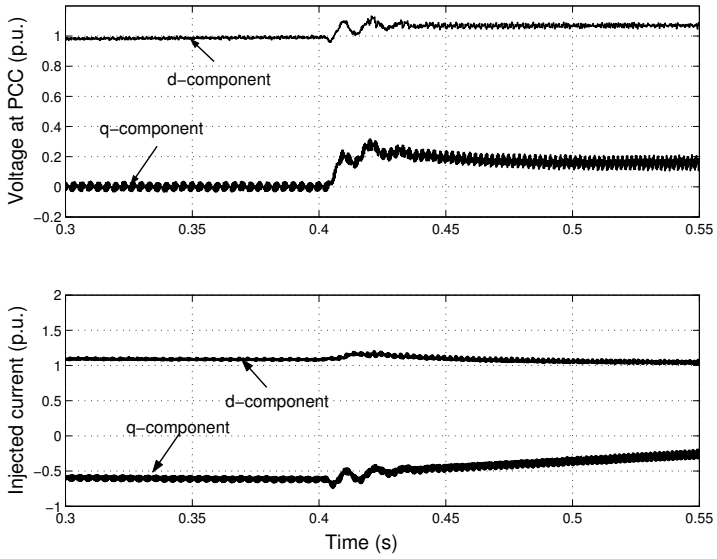

Fig. 5.3 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.4 s and $P_L < P_{DG}$.

If the load absorbed power is higher than the DG injected-power (in which case a load shedding criterion is important for a stable island operation), the PCC voltage will decrease in case of the grid outage. This case is represented in Fig. 5.4, where the grid outage occurs at 0.3 s, and the load active power is higher than the DG active power ($P_L = 1.07P_{DG}$) while the reactive power for both the load and the DG are equal. The DG controller, here, injects constant current into the grid, as shown by the lower

plot in the same figure. Since this decreased voltage could occur also due to voltage dips at the grid, hence the undervoltage is not a reliable state for islanding detection especially if the voltage dips ride-through capability is required. In other words, using the undervoltage state for the islanding detection may lead to false tripping during voltage dips.

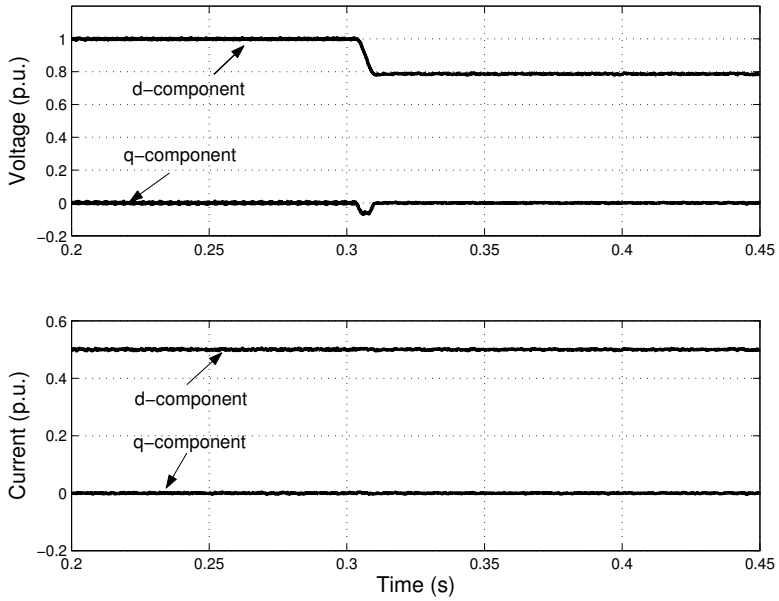

Fig. 5.4 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s and $P_L > P_{DG}$ (ΔP = -0.07 p.u.) and $Q_L = Q_{DG} = 0$.

In conclusion, an overvoltage/undervoltage islanding detection algorithm is not appropriate to be implemented. In addition, measuring other grid states (e.g. the phase angle jump) within a narrow threshold may falsely lead to islanding in case of other grid dynamics (e.g. switching events) [68].

Instead, using the signals generated within the DG controller to detect the islanding condition is considered. A disturbed signal within the controller will lead to a disturbed operation of the DG unit, and hence changing the control mode might be a good practice (even if the utility grid is not

disconnected). For instance, due to the grid outage and the reactive-power mismatch a constant nonzero value of the q-component of the voltage at the PCC will result (e.g. as shown in Fig. 5.3). This will cause an integrator windup of the PLL that in turn will result in a continuous increase (or decrease) in the estimated frequency as shown in Fig. 5.5 for a grid outage at 0.4 s. Hence, the estimated frequency signal is implemented here to detect the grid outage. This is done by assigning a threshold band for the estimated frequency. If the frequency crosses the band for a certain period of time, then the islanding condition is detected. For example, if the detection limit is set to 52 Hz then the islanding conditions are detected within 0.03 s.

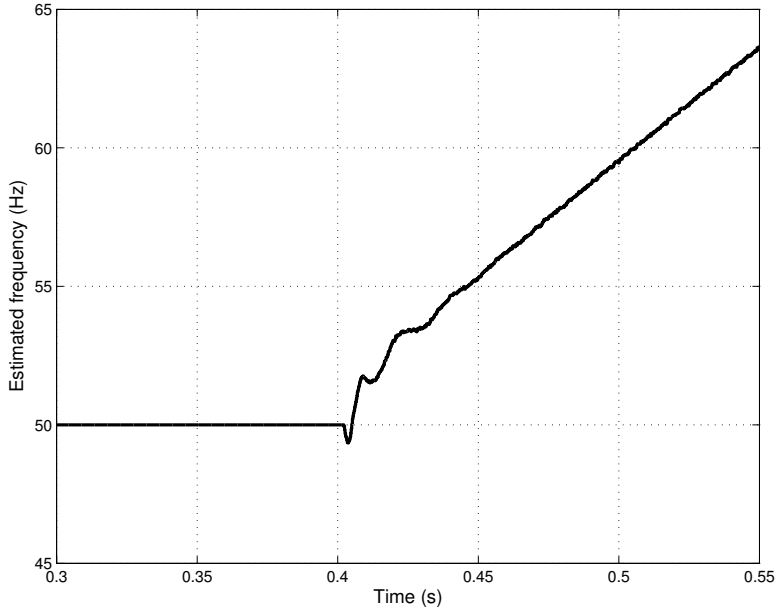

Fig. 5.5 Estimated frequency; grid outage at 0.4 s (P_L<P_{DG}).

To detect the grid recovery, the voltage measurement on the grid side of the grid switch (GS), shown in Fig. 5.2, is needed. If the voltage is back an extra PLL is used for the synchronization between the DG-output voltage and the grid voltage before connecting back the island to the grid.

Passive detection algorithm

The passive detection algorithm, which is implemented here, is shown in Fig. 5.6. Starting from the parallel (or grid-connected) operation, where the DG is aiming at controlling the active and reactive currents injected into the grid, the detection algorithm will be activated to detect the grid outage. The algorithm uses the deviation between the estimated frequency signal, which is produced by the PLL, and the nominal value. A time threshold t_s is also incorporated to avoid false tripping due to load dynamics. This time threshold is set equal to the settling time of the PLL, which could be calculated using the PLL gain as follows

$$t_s = \frac{\ln 50}{k_{pll}} \tag{5-1}$$

where the settling time is defined as the time for the PLL output to settle down to within a tolerance band of 2% of the final value [70], and k_{pll} is the proportional gain of the PLL.

Once the islanding condition is detected, the DG starts an island operation mode where its aim is to hold the voltage and frequency at their nominal values as well as to adjust the injected active and reactive powers to support the island loads. In addition, the GS is used to disconnect the utility grid from the island for safety operation. A DC chopper is also needed to consume the extra power that could be coming from the primary energy source in a way to adjust the input power to match the load needs. Moreover, in this mode, the grid recovery detection is activated where the voltage on the grid side is sensed. Once the utility grid is recovered, the synchronization between the DG voltage and grid voltage is carried out using an extra PLL on the grid side. The connection to the grid is then done by enabling the GS and disabling the DC chopper.

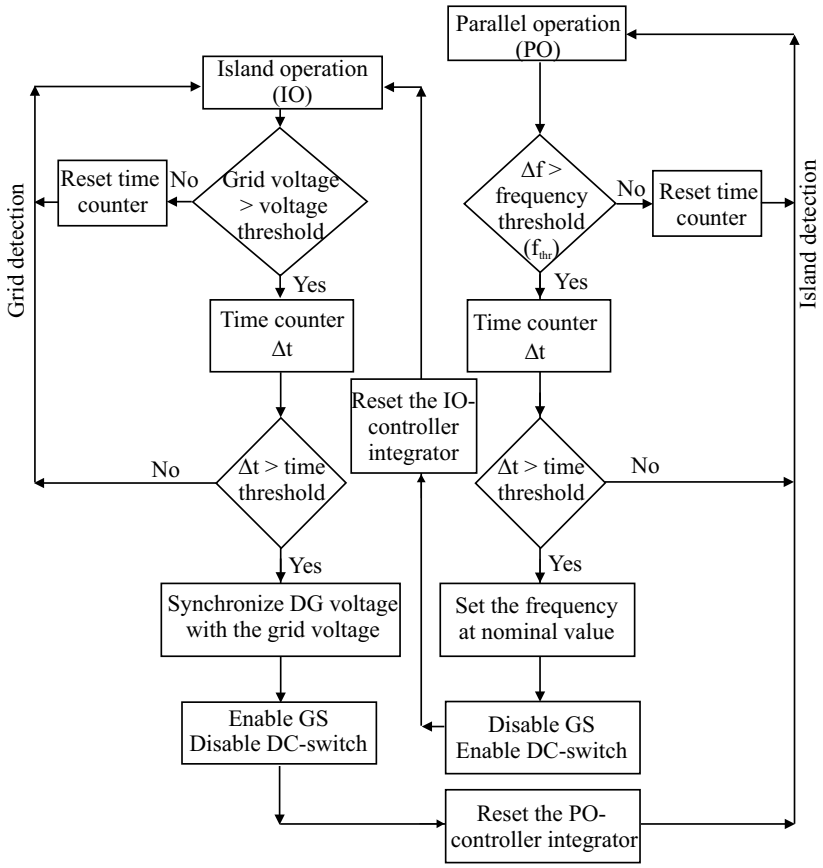

Fig. 5.6 Passive detection algorithm.

5.4 Non-detectable zone for passive detection

The non-detectable zone (NDZ) is usually described by the limits of active and reactive power mismatch (ΔP and ΔQ in Fig. 5.2) in which the detection algorithm would fail to recognize the grid outage [68]. These limits are related to the load characteristics, the detection method, and the controller of the DG.

The above described passive detection algorithm suffers from an open limit for ΔP in the NDZ. In other words, if the load reactive power exactly

matches the DG-injected reactive power, then, in case of the grid outage, the *q*-component of the PCC-voltage will not change irrespective of the amount of ΔP. This leads to undetectable islanding whatever the load active power is.

This case has been shown in Fig. 5.4, for $P_L > P_{DG}$ and constant active and reactive powers that are injected by the DG. Incorporating a PCC-voltage regulator within the DG controller, the change in the *d*-component of the PCC-voltage will lead to a change in the injected DG reactive current. Since the PCC-voltage will keep its decreased (or increased) value, due to the grid outage, the injected reactive current will keep a constant value (in case the DG is operating towards a strong grid) that will produce a reactive power mismatch and a change in the *q*-component of the PCC-voltage. This case is represented in Fig. 5.7, for the same loading condition as in Fig. 5.4. With the change in the *q*-component, an integrator windup in the PLL will result. Hence, the estimated frequency, shown in Fig. 5.8, will drop instantly leading to successful islanding-detection. As an example a frequency threshold of 48 Hz is detected within 0.01 s. This will lead to the decrease of the NDZ since either the active or reactive power mismatches will lead to a successful islanding detection.

In conclusion, combining the passive islanding-detection with the PCC-voltage regulator, described in Section 4.4, results in decreased NDZ. However, a complete match between the load and the DG unit active and reactive powers ($\Delta P = \Delta Q = 0$) would not be detected, since neither the *d*-component nor the *q*-component of the PCC-voltage would be affected by the grid outage. In this case, an active detection algorithm that injects a disturbance signal would be beneficial especially in case of a strong grid.

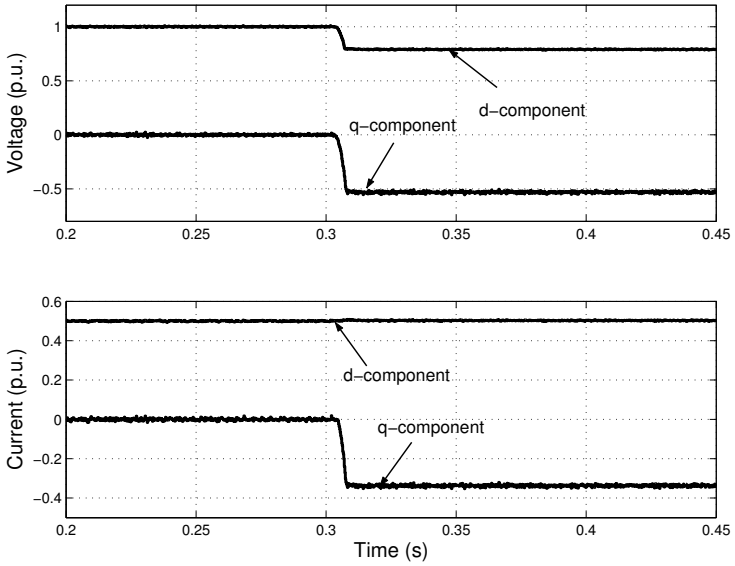

Fig. 5.7 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s; current-controlled DG with voltage regulation capability, and $P_L > P_{DG}$ ($\Delta P = -$ 0.07 p.u.).

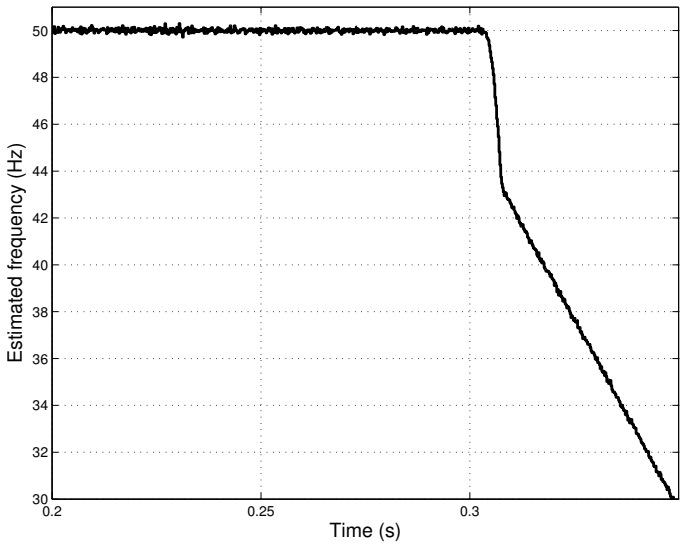

Fig. 5.8 Estimated frequency; grid outage at 0.3 s and current-controlled DG with voltage compensation capability, and ($\Delta P = -$ 0.07 p.u.).

5.5 Active Detection

The idea of the active detection is to try to disturb the grid in such a way that the passive detection will succeed to operate in the NDZ [69]. In a way to implement that, the active frequency drift method has been used in [79] and [43]. In this method, the waveform of the injected current is slightly distorted such that when islanding occurs the frequency of the phase voltage will drift up or down. Islanding is done in [43] by incorporating a washout function in the PLL that determines the change in the frequency and adds it to the frequency reference. Instead, in [39] a band pass filter is used, with the *d*-component voltage as an input, to deviate the voltage from its nominal value by changing the switching duty cycles.

In a way to optimize the design of the DG controller, the active detection is implemented here, using the PCC-voltage regulator. In case of a strong grid, the reference voltage signal in the PCC-voltage regulator is set to a value that is less than 1 p.u., while in case of a weak grid the reference voltage is set to 1 p.u.

The PCC-voltage regulator that is devoted for the operation in a strong grid is shown in Fig. 5.9. It operates in a way to produce a reactive current command i_q^* in such a way to force the voltage to deviate from its nominal value. The reference signal e_{dset} is set to a value that, when compared to the PCC-voltage e_d, produces an injected current within the maximum current limit of the DG. The limiter in the figure resets the integral part of the PI controller so that the current reference changes in a narrow band in order to decrease the current harmonics injected to the grid.

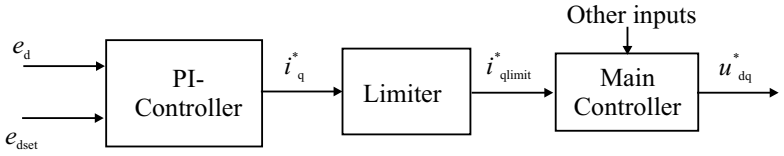

Fig. 5.9 Active islanding detection (PCC-voltage regulator).

The effect of adding the active islanding detection using the PCC-voltage controller is examined using a load that completely matches the DG power input (i.e. $\Delta P = \Delta Q = 0$). The DG injected active (*d*-component) and reactive (*q*-component) currents are shown in Fig. 5.10, without incorporating the active detection part (in the upper plot) and with incorporating it (in the lower plot), for a grid outage from 0.3 s to 0.4 s. From the figure, the increased value of the injected reactive current, in case of incorporating the active detection controller, implies producing a reactive power mismatch, in the normal operation, that in turn results in an islanding signal from the passive detection algorithm in case of grid outage.

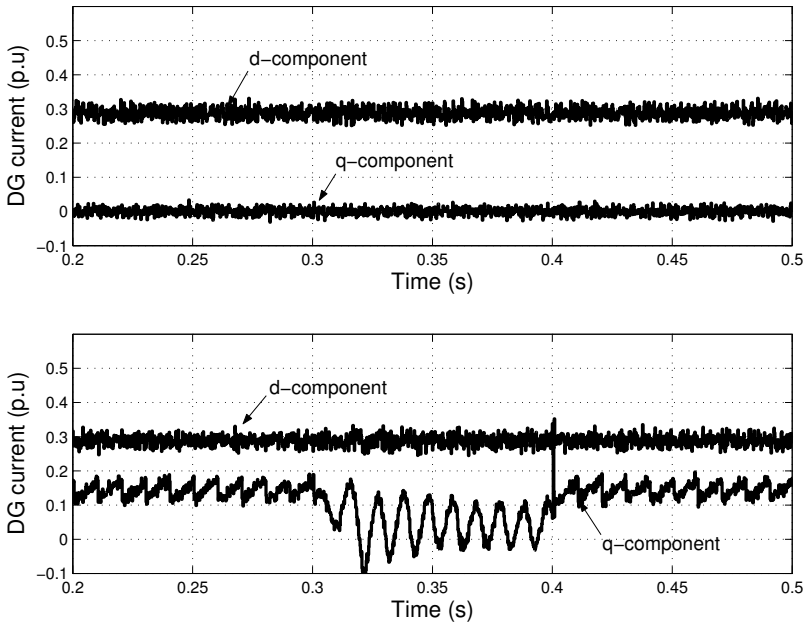

Fig. 5.10 DG injected active (d-component) and reactive (q-component) currents; without active detection controller (upper) and with active detection controller (lower) with a matching load.

The effect of using the active detection controller (i.e. the PCC-voltage controller) is also examined in case of a weak grid using a quadratic voltage dependent load that produces active power mismatch (ΔP) of 0.15 p.u. and

zero reactive power mismatch (ΔQ = 0) at the normal operation. A grid outage at 0.8 s is encountered. As shown in Fig. 5.11 (a) by the dashed line, the estimated frequency has a constant increase after 0.8 s, with the PCC-voltage regulator deactivated, due to a small change in the reactive power of the load that is in turn resulting from the increase of the PCC voltage, as shown in Fig. 5.11 (c). This increase in the estimated frequency could be relatively small and, depending on the frequency threshold set in the passive detection algorithm, it might not successfully detect the islanding condition. By activating the PCC-voltage regulator, the estimated frequency will continue to increase, as shown in Fig. 5.11 (a) by the solid line, after the grid outage at 0.8 s, due to the continuous increase in the DG injected reactive current that is shown in Fig. 5.11 (b), implying the successful detection of the islanding condition.

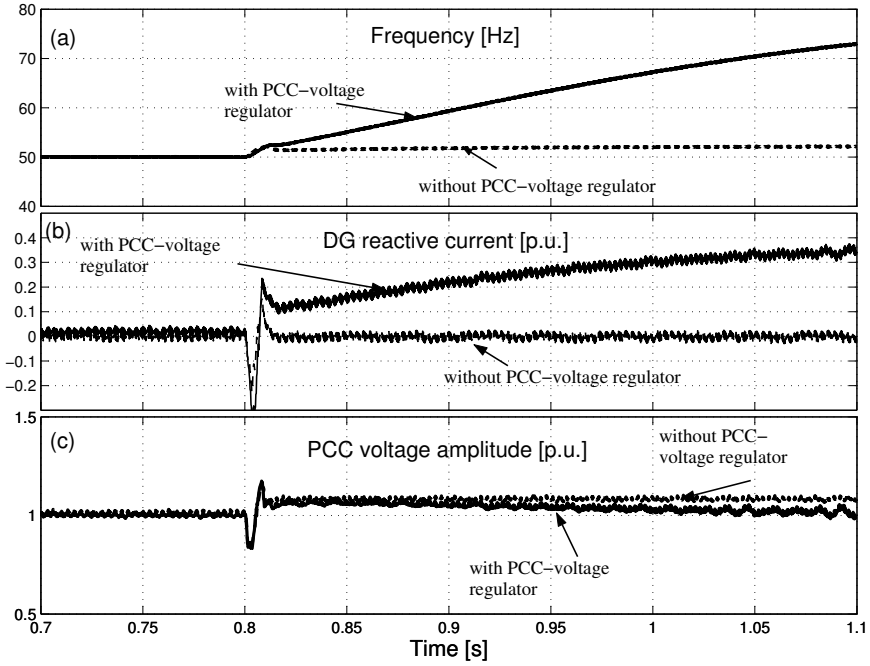

Fig. 5.11 Grid outage at 0.8 s, for ΔP = 0.15 and ΔQ = 0, with and without the PCC-voltage regulator. (a) the estimated frequency. (b) The DG injected reactive current. (c) The PCC-voltage amplitude.

The active detection method, using both the passive detection algorithm and the PCC-voltage regulator, are now to be examined.

5.6 Intentional islanding in a strong grid

A strong grid system is referring to a power system where the voltage and frequency at the load bus are kept constant, by the utility, regardless of the load dynamics. The system shown in Fig. 5.2 is considered where the PCC-voltage amplitude is kept constant at 1 p.u. during normal operation. The DG system is assumed to have an L-filter to smoothen out the current harmonics, and the DC-side is assumed to be controlled from the DG energy-source side for simplicity.

The DG controller will work on either one of the two operations; current-controlled or voltage-controlled, depending on the state of the utility grid as shown in Fig. 5.12.

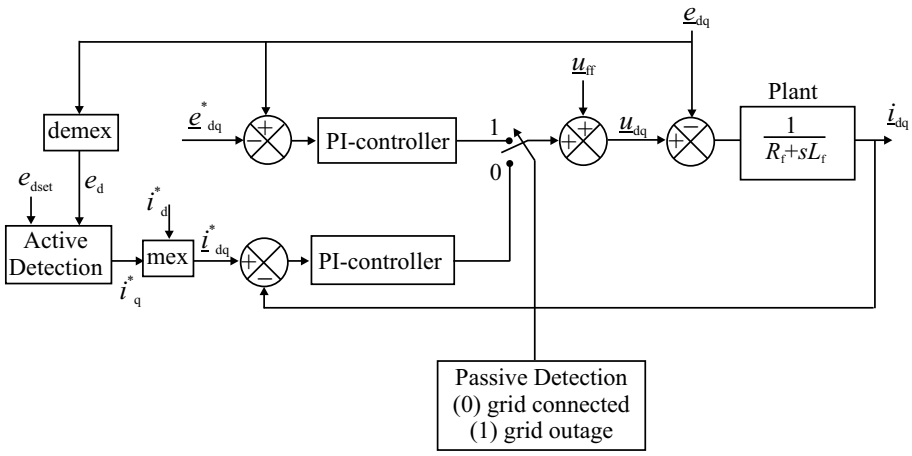

Fig. 5.12 Control transition between grid-connected and island modes.

The grid state is detected using the passive detection algorithm, shown in Fig. 5.6. In case of the grid outage, the detection algorithm will set the controller on the voltage control mode. In this mode the voltage nominal value is set as reference and compared with the measured voltage signal using a PI-controller. The output of this controller is added to the

feedforward voltage vector $\underline{u}_{ff}$. When the grid recovery occurs, the current controller will be activated. Moreover, the active detection is also incorporated in the controller in order to minimize the non-detectable zone as discussed before.

The island loads are set to draw higher power than the DG injected power, as described before for the case related to Fig. 5.4, to test the islanding detection and operation. It is assumed in this case that the energy source of the DG can inject more power to match the load in case of the occurrence of islanding (otherwise a load shedding criterion should be implemented). A grid outage has been encountered at 0.4 s, and the recovery of the grid occurred at 0.6 s. The controller has detected the outage and a transition to the voltage control mode has been performed, where the voltage has been set to 1 p.u., as shown in Fig. 5.13.

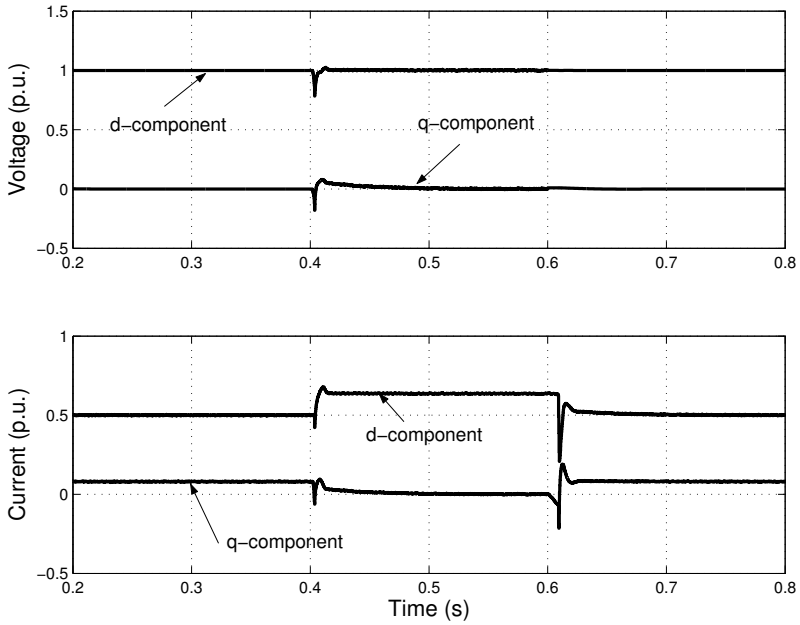

Fig. 5.13 PCC-voltage (upper), and DG injected currents (lower) in case of grid outage from 0.4 s to 0.6 s.

Before islanding, the *d*-component current has been set to 0.5 p.u., as shown by the lower trace of the same figure, while the *q*-component current i_q has been adjusted by the active detection controller to reduce the PCC-voltage *d*-component to 0.95 p.u. (i.e. e_{dset} = 0.95 p.u.). At the grid outage (at 0.4 s), i_q will start to change in a way to put the PCC-voltage amplitude to e_{dset}. However, this will change also the *q*-component of the voltage, which in turn will affect the estimated frequency as shown in Fig. 5.14 by the upper plot. This will lead to the setting of the passive detection signal, as shown in the same figure by the lower plot. Hence, the grid outage is detected and the grid switch GS is disconnected.

During the island operation, the DG injected currents will be set to match the load requirements. Moreover, the voltage angle is set to the reference value. When the grid is back, the voltage on the grid side of the GS will be sensed, and an extra PLL is used to synchronize the island back to the grid, then the GS is connected.

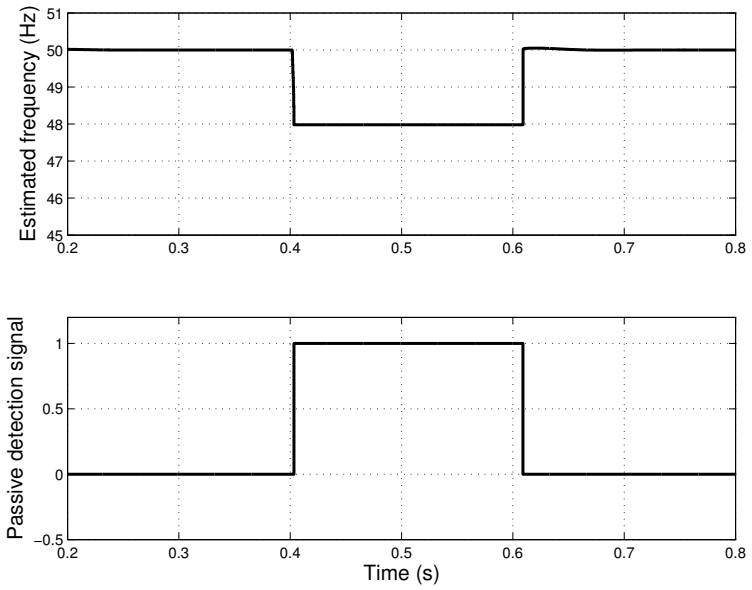

Fig. 5.14 Estimated frequency (upper), and passive detection signal (lower) in case of grid outage from 0.4 s to 0.6 s.

5.7 Intentional islanding in a weak grid

A weak grid system is referring, here, to systems where the voltage level at the load bus is not constant and is affected by the load dynamics. The system in Fig. 5.2 will be considered, where the voltage at the PCC is affected by the feeder voltage drop and the load dynamics. The island-loads are set such that their consumed power is lower than the DG-injected power. They are implemented as an aggregated quadratic voltage-dependent load, with a nominal active power mismatch (ΔP) of 0.55 p.u. and reactive power mismatch (ΔQ) of 0.2 p.u.

As has been discussed in the previous chapter, the voltage regulation capability of the DG is advantageous in the operation of weak grids since it will maintain the PCC voltage at the nominal value regardless of the load dynamics. Another advantage is highlighted here regarding the islanding. With the voltage regulation capability, the islanding non-detectable zone is reduced. This is especially important in the application of weak grids, since the active detection methods, which aim at disturbing the grid states, are not adequate for such grids since, during normal operation, the weak grid states (as opposite to strong grids) are changeable.

The DG system is considered here with the VSC as a front end and an LCL-filter to damp the line current harmonics. The grid-connected controller for this system has been described before in Section 2.6. The island-operation controller is shown in Fig. 5.15[17], where the voltage reference and the phase angle reference are set to their nominal values. A DC-link chopper is incorporated to dissipate the extra power that would come from the DG energy-source, in order to adjust the DG injected-power to match the load requirements.

The PCC-voltage is shown in Fig. 5.16, in the upper plot, for the operation of the DG before, during, and after islanding. The grid is disconnected at 0.3 s and recovered at 0.5 s.

[17] This controller has been explained in more details in Paper F.

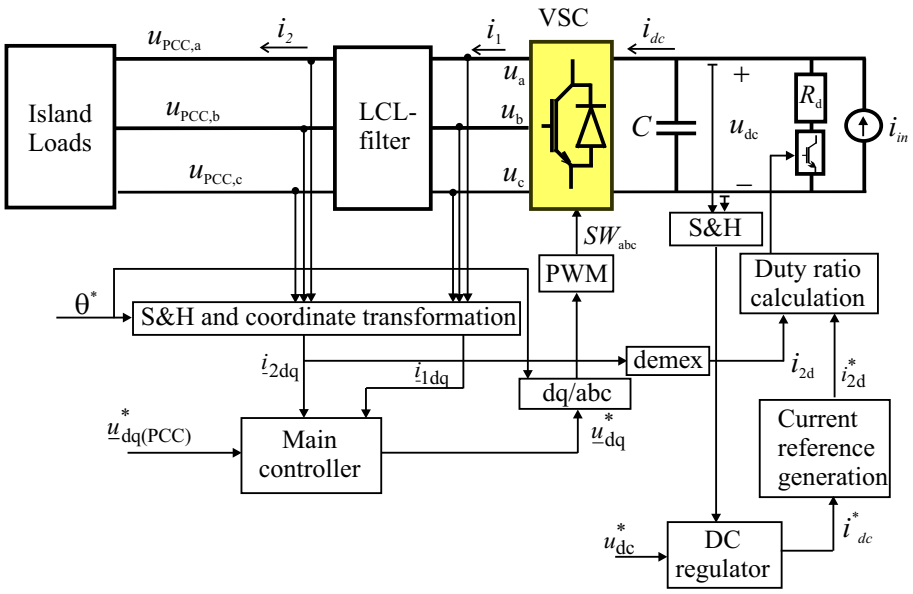

Fig. 5.15 Island operation controller for DG with LCL line filter.

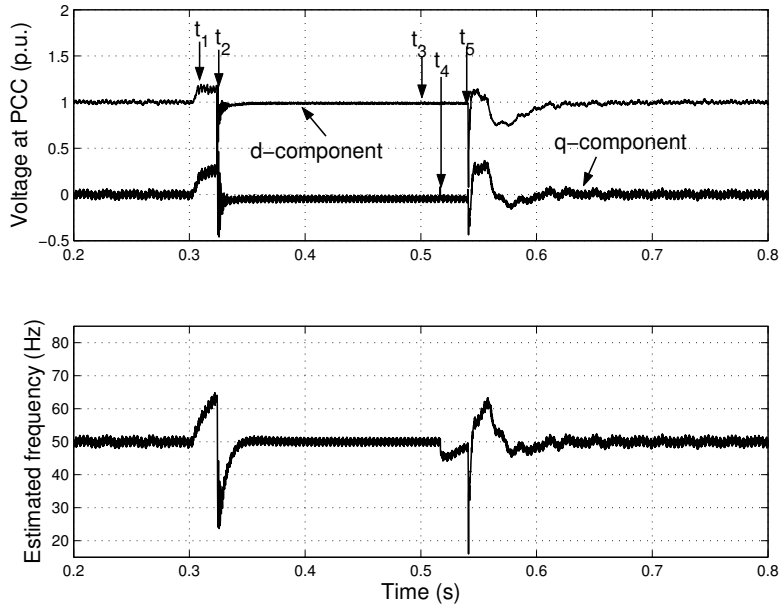

Fig. 5.16 Voltage in *dq*-frame at the PCC (upper) and estimated frequency (lower) for grid outage at 0.3 s and recovery at 0.5 s.

When the grid outage occurs at 0.3 s, the PCC voltage starts to increase in magnitude. When the *d*-component of the PCC-voltage $u_{d(PCC)}$ reaches the voltage limit, that is set by the controller, at t_1, the constant-limited value is maintained (until t_2). The frequency, which is shown by the lower plot of the same figure, will continue to increase after t_1, due to the constant value of the voltage *q*-component, until the island is detected at t_2. The detection algorithm will start to react after reaching the time threshold t_s, when the detection signal is activated (at t_2), resulting in transferring the controller from grid-connected mode to island-operation mode. At t_2 the frequency will be reset to its nominal value, and the DG injected powers, which are shown by the upper plot in Fig. 5.17, will start to adjust to match the load requirements. In consequence, the injected currents will decrease in magnitude, as shown in Fig. 5.18. Moreover, the DC-link voltage, which is shown in Fig. 5.17 by the lower plot, will maintain its nominal value in spite of the decreased injected DG-active power to the grid, since the DC chopper switch has been activated to dissipate the extra power in the chopper.

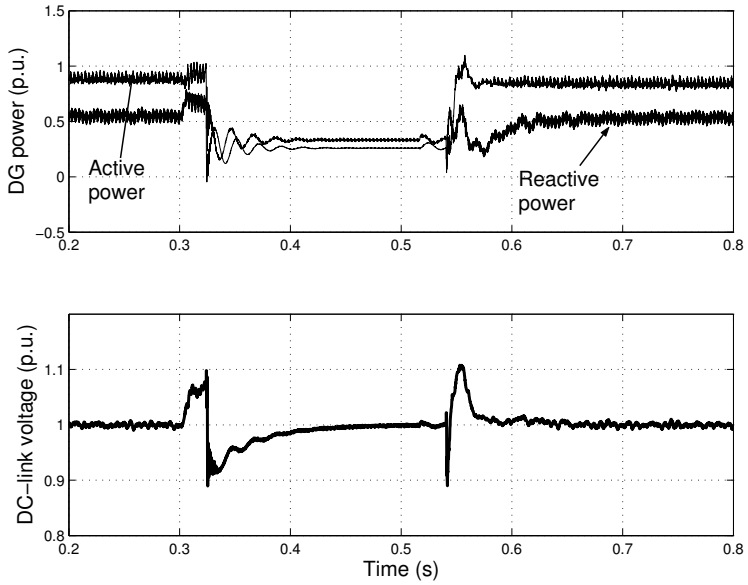

Fig. 5.17 DG injected power (upper) and DC-link voltage (lower) for grid outage at 0.3 s and recovery at 0.5 s.

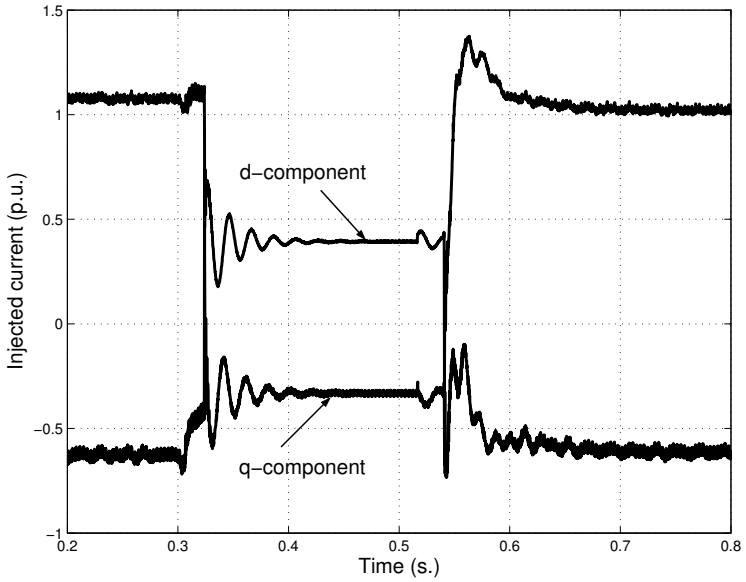

Fig. 5.18 DG injected current in dq-frame; grid outage at 0.3 s and recovery at 0.5 s.

When the grid voltage is recovered at t_3, a time threshold is also encountered before the synchronization of the grid voltage and DG voltage starts at t_4. This is done by using an extra PLL that is implemented for the voltage before the grid switch (GS in Fig. 5.2) from the utility grid side. At t_4, the phase angle of the DG voltage is set equal to the phase angle of the grid voltage. This could be seen from the change of the frequency signal in Fig. 5.16. After about one cycle of the fundamental frequency, the island is connected back to the utility grid at t_5. The DC-chopper is left in operation to buck the over-voltage that could occur at the starting of the grid-connected controller mode, until the PCC-voltage is stabilized.

At the starting of the grid-connected operation, $u_{d(PCC)}$ will drop to a value that represents its normal amplitude in case of deactivating the voltage regulator of the DG. This is mainly due to the PCC-voltage regulator transient time, which has been set long enough to stabilize the overall DG controller. In spite of the decreased value of the voltage during this time, the duration is very small compared with the clearing times that are shown in Fig. 5.1. After the transient time of the PCC-voltage regulator, the PCC-

voltage amplitude will be regained to the nominal value. In addition, the DG injected powers and currents will regain the values that are set for the grid connected operating mode.

5.8 Islanding detection reliability

Voltage dips appearing at the PCC, due to remote faults or motor starts, may lead to false tripping of the DG. The reason is that for small voltage dip amplitudes, the PCC voltage regulator may become unstable resulting in a disturbed PCC voltage that in turn will result in islanding. For instance, referring to Fig. 4.6 with a DG injected active power of 0.8 p.u. and a voltage dip magnitude of 0.7 p.u., the voltage regulator will become unstable and islanding will be detected for this case. Decreasing the DG input power would result in improving the voltage dip ride-through capability (as has been discussed in Chapter 3) and the reliability of the islanding detection.

Moreover, the effect of limiting the VSC current on the estimated frequency in case of voltage dips at the grid with induction motor loads at the PCC has been discussed in [81]. For sufficiently high current limit, the controller is able to maintain the voltage and frequency at the PCC at their nominal values. That would imply robust islanding detection.

The effect of setting a reactive current limit on the robustness of the islanding detection has been, also, discussed in Paper G, where the island loads have been implemented as an induction machine load. By setting the proper current limit, the DG unit can have the ability to ride-through voltage dips with magnitudes above a certain limit, which can be set according to the grid codes, and detect islanding for voltage dips with magnitudes lower than that limit.

5.9 Conclusions

In this chapter, the possibility of intentional islanding has been discussed. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection method should be applied. The islanding detection technique should be able to differentiate between grid dynamics and the islanding condition, and to provide the correct detection signal irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch. The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC). The NDZ, for the converter-interfaced DGs, also depends on the control method.

Two islanding methods have been introduced here; namely passive and active. An active islanding detection method has been proposed to minimize the inherent NDZ of the passive technique. In this method, the estimated frequency signal has been used to detect islanding along with the PCC-voltage regulator. This detection method is motivated by the operation of the DG in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the same method can be used by changing the reference value of the PCC-voltage regulator so as to produce a disturbing current signal in the grid.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The main focus of the thesis has been put on the study of the interface requirements and capabilities of a DG with a voltage source converter (VSC) as a front end. Two line filters have been considered at the connection point of the DG; namely an inductance line filter (L-filter) and an inductance-capacitance-inductance line filter (LCL-filter).

Vector current controller (VCC)

In the first place, **vector current controllers (VCC)** have been implemented, in the rotating synchronous *dq*-frame, for both systems. The time delay, with one sample length, that results due to the calculation time has been compensated for using a Smith predictor, which predicts the grid currents one sample ahead. In addition, the controller saturation, which could result due to high current steps, has been avoided using a voltage limiting algorithm. Besides, to avoid integrator windup, which also could result due to high current steps, the limited voltage has been used in the Smith predictor to recalculate the currents. A DC-link voltage regulator has been also incorporated in the controller to protect the capacitor on the DC-side during different load changes. Moreover, a dual vector current controller (DVCC) has been implemented, which comprises two VCCs. One of them is described in the positive rotating *dq*-frame and the other is described in the negative rotating *dq*-frame, to improve the performance in the case of unbalanced grid-voltage. Moreover, convenient current reference equations have been derived based on the power balance between the DC-side and the

AC-side of the VSC. The controllers have shown good current reference tracking even when high current steps are applied. In addition, in case of unbalanced grid-voltage, oscillating powers will be produced. When those powers are forced to be supplied from the grid side, it has been also shown that the DC-link voltage oscillations are negligible.

Voltage dips ride-through capability

Furthermore, the current-controlled converter interfaced DG has been studied in relation to different grid interface issues. First the **voltage dips ride through capability** has been discussed. For that purpose, a previously investigated voltage dips classification has been adopted to study the effect of all the possible voltage dips that could appear at the DG terminals. In addition, that classification has been modified to be implemented in the positive and negative sequence *dq*-frames. The equations of the maximum currents that would flow through the VSC valves due to all possible voltage dips have been derived. It has been shown that these analytical expressions give almost the same maximum current values as the numerical calculations based on simulation. It has been shown that if the converter-interfaced DG should ride-through the dip period there are two alternatives. One is to oversize the converter switches to withstand the increased currents. The other is to decrease the power input from the source during the dip period, so that the currents will be decreased. However, the latter would require that the input power to the DC-link be reduced very quickly, which could be an issue regarding the energy source or the control of an energy storage connected to the DC-link.

Voltage regulation capability

Thereafter, the **voltage regulation capability** has been discussed. This capability is beneficial if the compensation for the grid voltage quality problems is required. With this capability, the compensation of voltage dips, voltage harmonics, voltage amplitude modulation … etc. would be possible resulting in better power quality at the grid. Moreover, if the DG is working towards a weak grid, where the voltage level is dependable on the load

dynamics, this capability will help in maintaining the voltage level at its nominal value. However, an important issue is the voltage regulation limits, at which the voltage regulator is stable. These limits were discussed and are related to the loading at the grid. It has been shown that, the more input power coming from the DG source, the more reactive power is available to compensate for the voltage. However, in case of increased active and reactive powers, the current limit could be reached. Hence, the compensation capability is limited by the maximum current that the VSC would stand. Another limit is presented by the load that is connected at the same connection point as the DG. If the load has a low power factor, it means that more injected reactive power is needed to regulate the voltage. This in turn would increase the injected current. Another issue that could affect the voltage regulation capability is the voltage phase-angle extraction.

It has been shown that using a PLL that implements the fundamental component of the grid voltage a smaller error in the estimated phase angle would be produced and hence resulting in better grid voltage regulation. A neural-networks based PLL has (NN-PLL) been introduced for that purpose. The NN-PLL has been compared with a previously investigated PLL that extracts the angle of the positive sequence voltage, which is referred to here as PS-PLL. The NN-PLL has performed superior compared to the conventional PLL when the grid voltage harmonics are significant, and the case of grid voltage amplitude modulation.

Intentional islanding capability

Finally, the **intentional islanding capability** has been studied. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection algorithm should be applied. The islanding detection technique should be able to differentiate between grid dynamics and islanding condition, so that a correct detection signal is provided, irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch at which the detection algorithm will malfunction.

The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC).

Two islanding techniques have been examined here; namely passive and active techniques. In the passive technique, the estimated frequency signal in combination with the PCC-voltage regulator has been used to detect islanding with a minimum NDZ. That could be a beneficial application in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the active technique has shown to be beneficial. In this technique, which incorporates also the passive algorithm using the estimated frequency, a reactive current reference is set in order to change the voltage at the PCC. If the voltage changes, it will result in the detection of the island. The two islanding-detection methods have been examined for the operation of a converter-interfaced DG that is working together with both a strong grid and a weak grid. The islanding-detection technique has successfully detected the island in case of islanding condition, while it did not react during a voltage dip at the grid.

6.2 Future work

The grid interconnection capability of a converter-interfaced DG has been studied here regarding the front end converter only. The study of the whole DG system and its effect on the interface capabilities is an interesting topic and could result in setting preferable topologies for the optimal operation. For instance, the capability of voltage dips ride through has been related to the DG source input power. If this input power could be changed in a very short time, then the ride through capability could be provided without oversizing the front end converter. Moreover, providing controllable storage at the DC-link could help in storing the extra power during island operation. That could result in supporting the island for longer time duration and the stored power could be used during voltage dips to ride through the dip period.

Another interesting research point is the study of the parallel operation of converter interfaced DGs regarding the voltage regulation capability and

islanding. The parallel operation could be already motivated from the energy resource point of view. For instance the aggregated DG systems are common for wind energy applications. Using several DGs at the same connection point could increase the voltage regulation capability and provide better support in case of islanding. The design of a central controller, however, is an important issue. The controller should be designed to provide control coordination between different DG units with possibly different control aims. Sliding mode control approach could be implemented for the control of parallel converter-interfaced DGs that are operating in close proximity [72]. This control technique is based on variable structure systems (VSS), which are defined as systems where the circuit topology is intentionally changed following certain rules to improve the system behaviour in terms of speed of response, stability and robustness [12]. Hence, the operational idea of this controller could be to change the physical structure of the connected DGs to meet the physical or electrical changes on the grid.

Furthermore, since the grid outage detection algorithm plays an important role in providing a stable island by setting the DG controller into the required function, it is of great importance to develop a reliable detection algorithm. An algorithm with a negligible non-detectable zone (NDZ) implies a successful grid outage detection regardless of the loading condition of the grid or the injected power of the DG. Active islanding has been previously introduced to provide such a reliable detection. However, the equipment of active islanding can have a drawback of polluting the grid. Besides, the equipment cannot be implemented in the case of a weak grid, where the grid states are changeable even during normal operation. The use of smart sensors could present another possible and reliable way in the grid outage detection. A smart or wireless sensor is comprised of a sensor, a processor, and wireless communication all on a single chip owing to the recent advances in micro-electro-mechanical systems (MEMS) technology [73], [74]. Smart sensors could be implemented for the coordination between the controllers for islanding detection through the interaction with the protection system or the grid operator. In addition, smart sensors could be

implemented for the coordination between the controllers for parallel operating DGs.

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Appendix A
Transformations for three-phase systems

A.1 Transformation of three-phase quantities into vectors

A three-phase positive system constituted by the three quantities $x_1(t)$, $x_2(t)$ and $x_3(t)$ can be transformed into a vector in a complex reference frame, usually called $\alpha\beta$-frame, by applying the transformation defined by

$$\underline{x} = x_\alpha(t) + \mathrm{j}x_\beta(t) = \frac{2}{3}K\left[x_1(t) + x_2(t)\cdot \mathrm{e}^{\mathrm{j}\frac{2}{3}\pi} + x_3(t)\cdot \mathrm{e}^{\mathrm{j}\frac{4}{3}\pi}\right] \tag{A.1}$$

where the factor K is usually taken equal to $\sqrt{\frac{3}{2}}$ for ensuring power invariance between the two systems. Equation (A.1) can be expressed as a matrix equation:

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = \mathbf{C_{23}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.2}$$

where

$$\mathbf{C_{23}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.3}$$

The inverse transformation is given by:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{32}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \tag{A.4}$$

where

$$\mathbf{C_{32}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.5}$$

This holds under the assumption that the sum of the three quantities is zero. Otherwise, there will also be a constant (zero-sequence) component. In the latter case, (A.2) and (A.4) become

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} = \mathbf{C_{230}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.6}$$

and for the inverse transformation

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{320}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} \tag{A.7}$$

with the two matrixes given by

$$\mathbf{C_{230}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} \end{bmatrix} \tag{A.8}$$

and

$$\mathbf{C_{320}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \end{bmatrix}. \tag{A.9}$$

A.2 Transformation from fixed to rotating coordinate system

Let the vectors $\underline{v}(t)$ and $\underline{w}(t)$ rotate in the $\alpha\beta$-frame with the angular frequency $\omega(t)$ in the positive (counter-clockwise) direction. If the vector $\underline{w}(t)$ is taken as the *d*-axis of a *dq*-frame that rotates in the same direction with the same angular frequency $\omega(t)$, both vectors $\underline{v}(t)$ and $\underline{w}(t)$ will appear as fixed vectors in that frame. The components of $\underline{v}(t)$ in the *dq*-frame are thus given by the projections of the vector on the direction of $\underline{w}(t)$ and on the orthogonal direction, as illustrated in Fig. A.1.

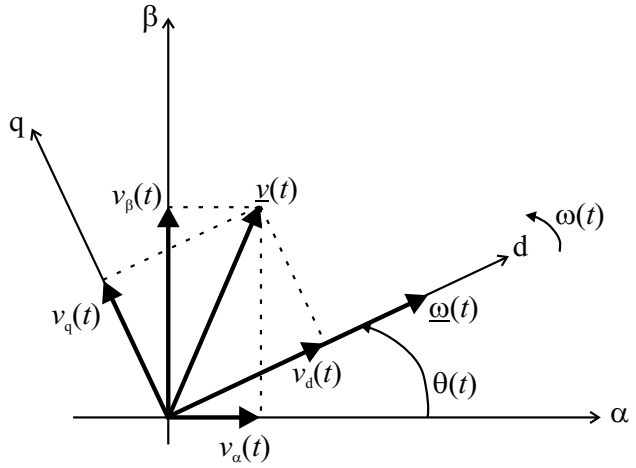

Fig. A.1 Relation between the $\alpha\beta$-frame and *dq*-frame.

The transformation can be written in vector form as:

$$\underline{v}_{\mathrm{dq}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{v}_{\alpha\beta}(t) \tag{A.10}$$

with the angle $\theta(t)$ in Fig. A.1 given by

$$\theta(t) = \theta_0(t) + \int_0^{\tau} \omega(\tau)\, d\tau \tag{A.11}$$

and the inverse transformation is defined by the expression

$$\underline{v}_{\alpha\beta}(t) = \mathrm{e}^{\mathrm{j}\theta(t)} \cdot \underline{v}_{\mathrm{dq}}(t) \tag{A.12}$$

The components in the *dq*-frame can be determined from Fig. A.1. In matrix form, the transformation from the $\alpha\beta$-frame to the *dq*-frame can be written as:

$$\begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}(-\theta(t)) \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} \tag{A.13}$$

and the inverse is given by

$$\begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} = \mathbf{R}(\theta(t)) \begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} \tag{A.14}$$

where the projection matrix is

$$\mathbf{R}(\theta(t)) = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \tag{A.15}$$

A.3 Transformations for voltage and current vectors in the *dq*-system

Suppose a symmetrical sinusoidal three-phase voltage with angular frequency $\omega(t)$ is transformed into a vector $\underline{u}(t) = u_{\alpha}(t) + \mathrm{j}u_{\beta}(t)$ in the $\alpha\beta$-frame. When transforming it further to the *dq*-frame, the *q*-axis in the *dq*-frame is normally defined as parallel to the voltage vector $\underline{u}(t)$. This definition originates from a flux vector parallel to the *d*-axis in the *dq*-frame. The voltage vector is proportional to the time derivative of the flux vector. As a consequence of the chosen reference vector, the voltage vector $\underline{u}(t)$ will only contain a *q*-component in the *dq*-frame. The transformation equation for a current vector from the $\alpha\beta$-frame to the *dq*-frame becomes, in matrix form:

$$\begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}\left(-\left(\omega t - \frac{\pi}{2}\right)\right) \cdot \begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} \tag{A.16}$$

and the inverse

$$\begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} = \mathbf{R}\left(\omega t - \frac{\pi}{2}\right) \cdot \begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} \tag{A.17}$$

The transformation from the $\alpha\beta$-frame into the dq-frame for current vectors is the same as for voltage vectors.

A.4 Voltage vectors for unsymmetrical three-phase systems

The phase voltages for a three-phase system can be written as

$$\begin{aligned} e_{\mathrm{a}}(t) &= E_{\mathrm{a}}(t)\cdot\cos(\omega t-\varphi_{\mathrm{a}}) \\ e_{\mathrm{b}}(t) &= E_{\mathrm{b}}(t)\cdot\cos(\omega t-\frac{2}{3}\pi-\varphi_{\mathrm{b}}) \\ e_{\mathrm{c}}(t) &= E_{\mathrm{c}}(t)\cdot\cos(\omega t-\frac{4}{3}\pi-\varphi_{\mathrm{c}}) \end{aligned} \tag{A.18}$$

where $E_{\mathrm{a}}(t)$, $E_{\mathrm{b}}(t)$ and $E_{\mathrm{c}}(t)$ are the amplitudes of the three-phase voltages, φ_{a}, φ_{b} and φ_{c} are the phase angles of the three-phase voltages, and ω is the angular frequency of the system.

If the amplitudes $\hat{e}_{\mathrm{a}}(t)$, $\hat{e}_{\mathrm{b}}(t)$ and $\hat{e}_{\mathrm{c}}(t)$ are unequal, the voltage vector can be written as the sum of two vectors rotating in opposite directions and interpreted as positive- and negative-sequence vectors

$$\underline{e}_{\alpha\beta}(t) = E_{\mathrm{p}}\mathrm{e}^{\mathrm{j}(\omega t+\varphi_{\mathrm{p}})} + E_{\mathrm{n}}\mathrm{e}^{-\mathrm{j}(\omega t+\varphi_{\mathrm{n}})} \tag{A.19}$$

where E_{p} and E_{n} are the amplitudes of positive- and negative-sequence vectors, respectively, and the corresponding phase angles are denoted by φ_{p} and φ_{n}. To determine amplitudes and phase angles of positive- and negative-sequence vectors in (A.19), a two-step solving technique can be used. First, the phase shifts are set to zero, so that the amplitudes E_{p} and E_{n} can easily be detected. In the next step, the phase shifts φ_{p} and φ_{n} are determined.

When transforming an unsymmetrical three-phase voltage into the dq-coordinate system, two rotating frames are used, accordingly. They are

called positive and negative synchronous reference frames and denoted by *dqp*- and *dqn*-, respectively. They can be defined by the transformations

$$\underline{e}_{\mathrm{dqp}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.20}$$

$$\underline{e}_{\mathrm{dqn}}(t) = \mathrm{e}^{+\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.21}$$

where the transformation angle $\theta(t)$ is locked to the positive phase sequence flux vector. The positive phase sequence vector in the *dqp*-coordinate system is expressed as

$$e_{\mathrm{dp}} + \mathrm{j}e_{\mathrm{qp}} = -E_{\mathrm{p}}\sin(\varphi_{\mathrm{p}}) + \mathrm{j}E_{\mathrm{p}}\cos(\varphi_{\mathrm{p}}) \tag{A.22}$$

and the negative phase sequence vector in the *dqn*-coordinate system is given by

$$e_{\mathrm{dn}} + \mathrm{j}e_{\mathrm{qn}} = -E_{\mathrm{n}}\sin(\varphi_{\mathrm{n}}) + \mathrm{j}E_{\mathrm{n}}\cos(\varphi_{\mathrm{n}})\,. \tag{A.23}$$

Appendix B
LCL-filter design

The schematic diagram of the power circuit of the VSC connected to the grid through LCL-filter has been shown in Fig. 2.9.

Assuming the grid-voltage as a disturbance and neglecting R_1 and R_2, the transfer function of the filter is then $I_2(s)$ /$U(s)$, where I_2 is the filter current on the grid side and U is the VSC output voltage, and is calculated as follows:

$$\frac{U(s)}{I_1(s)} = \frac{L_2/C_f}{\left(sL_2 + \frac{1}{sC_f}\right)} + sL_1 = \frac{sL_2 + 1/sC_f}{s^2 L_1 L_2 + \frac{(L_1 + L_2)}{C_f}} \tag{B-1}$$

Using the current divider rule, the grid-side current is

$$I_2(s) = I_1(s)\frac{1/sC_f}{sL_2 + \frac{1}{sC_f}} \tag{B-2}$$

It follows that

$$I_1(s) = I_2(s)\cdot\left(s^2 L_2 C_f + 1\right) \tag{B-3}$$

Then the transfer function becomes

$$\frac{I_2(s)}{U(s)} = \frac{1/C_f L_1 L_2}{s\left(s^2 + \frac{L_1 + L_2}{L_1 L_2 C_f}\right)} \tag{B-4}$$

The resonant frequency is then:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{B-5}$$

The filter parameters are chosen such that the following conditions are satisfied [23], [71]:

- Neglecting the filter resistances, the voltage drop across the inductances should be limited to 10% during nominal operation, which agrees with the previous design criteria for L-filter;
- The grid side inductance is a fraction of the converter side inductance, since the latter is responsible for the attenuation of most of the switching ripple;
- The capacitive value is limited by the decrease of the power factor at rated power in case of idle operation of the VSC (it will be considered as less or equal 10%);
- The resonance frequency is in the range between ten times the fundamental frequency and one half the switching frequency;
- The IEC 1000-3-4 regulation states that current harmonics above 33rd should be less than 0.6% of the nominal current;
- The resistances are taken as 10% of the value of the corresponding inductances.

According to these conditions the following equations can be used

$$L_1 + L_2 = 0.1 \text{ p.u.} \tag{B-6}$$

$$L_2 = r \cdot L_1 \tag{B-7}$$

where r is the ratio between the inductance on the grid side to the inductance on the converter side, which is less than 1.

$$C_f \leq 0.1 \quad \text{p.u.} \tag{B-8}$$

$$500 \text{ Hz} < f_{res} < 1250 \text{ Hz} \quad \text{(for sampling frequency of 5kHz)} \tag{B-9}$$

From (B-4), the gain of the system at the h harmonic is expressed as

$$\left|G(jh\omega)\right| = \frac{1/C_f L_1 L_2}{\left| jh\omega\left((jh\omega)^2 + \frac{L_1 + L_2}{L_1 L_2 C_f} \right) \right|} \leq 0.006 \text{ .} \tag{B-10}$$

Equations (B-9) and (B-10) are used as check up conditions. Using a capacitance value of 0.05 p.u., (B-9) is not satisfied for different inductance ratios (r), as shown in Fig. B.1. Increasing the capacitance value to 0.1 p.u.,

a value of r = 0.4 has been chosen to satisfy all conditions (see Fig. B.2 and Fig. B.3). The LCL-filter parameters are then calculated as reported in Appendix C.

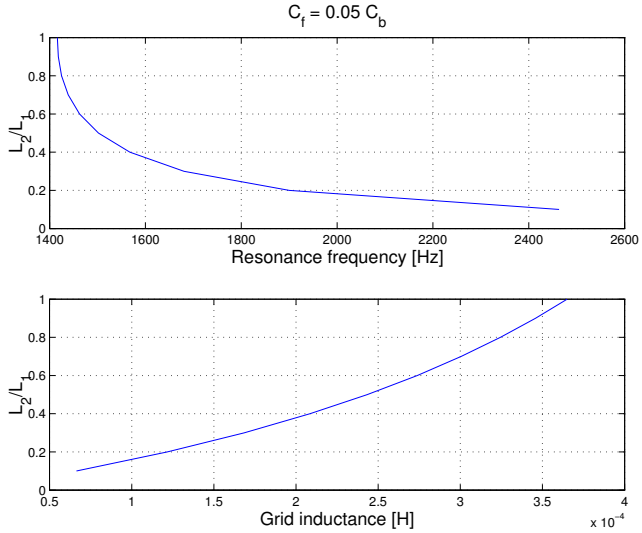

Fig. B.1 Relation between *r*, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 5% of the base value.

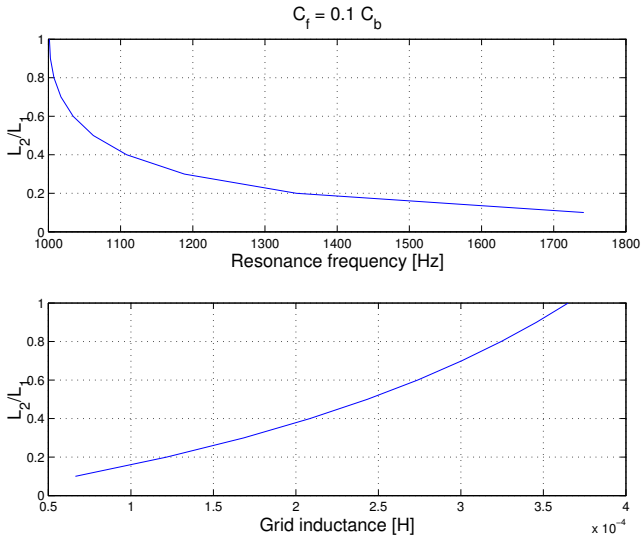

Fig. B.2 Relation between r, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 10% of the base value.

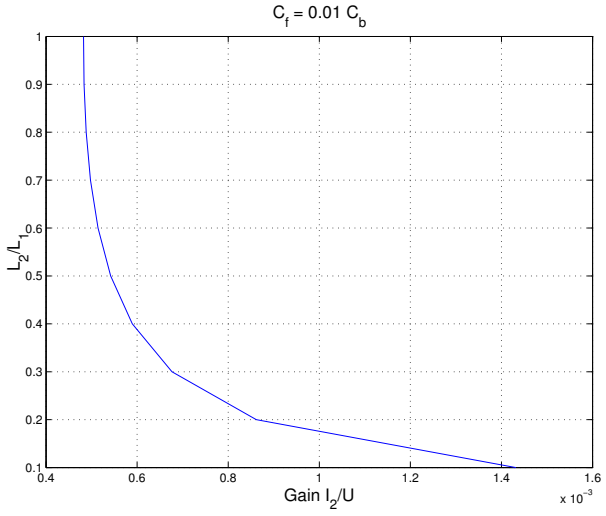

Fig. B.3 Relation between *r* and the gain filter I_2/U.

Appendix C
Power system parameters

C.1 Per-unit base values

The base values for the AC voltage and current are

$$E_{\text{base}} = 400 \text{ V} \tag{C-1}$$

$$I_{\text{base}} = 100 \text{ A} \tag{C-2}$$

The base value of the impedance is then obtained according to

$$Z_{\text{base}} = \frac{E_{\text{base}}}{\sqrt{3} I_{\text{base}}} = 2.3\Omega \tag{C-3}$$

The base values for the DC-link voltage and current are equal to

$$U_{\text{DC,base}} = 650 \text{ V} \tag{C-4}$$

$$I_{\text{DC,base}} = \frac{\sqrt{3} E_{\text{base}} I_{\text{base}}}{U_{\text{DC,base}}} = 107\text{A} \tag{C-5}$$

C.2 L-filter system data

Table C-1 System data with L-filter.

Description	Symbol	Value
Nominal RMS phase-to-phase AC voltage	E	400 V
Nominal RMS phase current	I_{n}	100 A
Nominal grid frequency	f_{n}	50 Hz
Nominal DC link voltage	U_{dc}	650 V
Nominal DC input current	I_{dc}	107 A
Filter resistance	R	23 mΩ
Filter inductance	L	0.73 mH
DC-link capacitance	C	550 µF
DC-chopper damping resistance	R_{d}	10 Ω

C.3 LCL-filter parameters

Table C-2 LCL-Filter parameters.

Parameter	p.u.	Actual
L_1	0.071	0.52 mH
R_1	0.1 L_1	1.6 mΩ
L_2	0.027	0.2 mH
R_2	0.1 L_2	0.6 mΩ
C_f	0.1	137.8 μF

C.4 Weak grid parameters

Table C-3 Weak network parameters.

Parameter	Value
V_s	400 V
R_s	3x0.05 Ω
L_s	3x2.05 mH
C_s	3x46 μF

Appendix D
Controller parameters

D.1 Parameters for VCC for L-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Dead beat gain	k_p	3.7
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.5

D.2 Parameters for VCC for LCL-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Outer controller gain	k_{p1} (0.7 k_{p2})	0.546
Second controller gain	k_{p2} (0.3 k_{p3})	0.78
Inner controller gain	k_{p3}	2.6
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.07

D.3 Parameters for DC-link voltage regulator

Table D-3 DC-link voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pdc}	0.4
Integral time	T_{idc}	0.04 s

D.4 Parameters for PCC-voltage regulator

Table D-4 PCC-voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pr}	0.5
Integral time	T_{ir}	0.05 s

Appendix E
LCL-filter current reference-generation

The power at the grid side S_2 is expressed as

$$S_2 = S_{\mathrm{ac},2} + S_{\mathrm{s}2,2} + S_{\mathrm{c}2,2} \tag{E-1}$$

where S_{ac} is the power at the fundamental frequency, $S_{\mathrm{s}2}$ and $S_{\mathrm{c}2}$ are sine and cosine components of the power at double the fundamental frequency, which are called the oscillating powers. The power is calculated in *dqp*- and *dqn*-frames as follows

$$S_2 = \left(e^{\mathrm{j}\omega t}\underline{e}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{e}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-2}$$

Expanding this equation leads to

$$\begin{aligned} S_{\mathrm{s}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{qn}} - e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dn}}i_{2\mathrm{qp}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dp}}i_{2\mathrm{dn}} - e_{\mathrm{qn}}i_{2\mathrm{qp}} - e_{\mathrm{dn}}i_{2\mathrm{dp}}\right) \end{aligned} \tag{E-3}$$

$$\begin{aligned} S_{\mathrm{c}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{dn}} + e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dn}}i_{2\mathrm{dp}} + e_{\mathrm{qn}}i_{2\mathrm{qp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dp}}i_{2\mathrm{qn}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} - e_{\mathrm{dn}}i_{2\mathrm{qp}}\right) \end{aligned} \tag{E-4}$$

The power at the converter side S_1 is expressed in the same manner and same designations as

$$S_1 = S_{\mathrm{ac},1} + S_{\mathrm{s}2,1} + S_{\mathrm{c}2,1} \tag{E-5}$$

It is calculated in *dqp*- and *dqn*- frames as follows:

$$S_1 = \left(e^{\mathrm{j}\omega t}\underline{u}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{u}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-6}$$

Expanding this equation results in the following:

$$\begin{aligned} S_{\mathrm{ac},1} &= u_{\mathrm{dp}} i_{\mathrm{1dp}} + u_{\mathrm{qp}} i_{\mathrm{1qp}} + u_{\mathrm{dn}} i_{\mathrm{1dn}} + u_{\mathrm{qn}} i_{\mathrm{1qn}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dp}} - u_{\mathrm{dp}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qn}}\right) \end{aligned} \tag{E-7}$$

$$\begin{aligned} S_{\mathrm{s}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1qn}} - u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dp}} i_{\mathrm{1dn}} - u_{\mathrm{qn}} i_{\mathrm{1qp}} - u_{\mathrm{dn}} i_{\mathrm{1dp}}\right) \end{aligned} \tag{E-8}$$

$$\begin{aligned} S_{\mathrm{c}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1dn}} + u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dn}} i_{\mathrm{1dp}} + u_{\mathrm{qn}} i_{\mathrm{1qp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dp}} i_{\mathrm{1qn}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} - u_{\mathrm{dn}} i_{\mathrm{1qp}}\right) \end{aligned} \tag{E-9}$$

Applying KVL to the outer loop of the LCL-filter

$$\underline{u}_{\mathrm{dqp}} = \underline{e}_{\mathrm{dqp}} + R_1 \underline{i}_{\mathrm{1dqp}} + \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqp}} + R_2 \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqp}} \tag{E-10}$$

$$\underline{u}_{\mathrm{dqn}} = \underline{e}_{\mathrm{dqn}} + R_1 \underline{i}_{\mathrm{1dqn}} - \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqn}} + R_2 \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqn}} \tag{E-11}$$

Applying KCL at the filter capacitor connection node

$$\underline{i}_{\mathrm{1dqp}} = \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqp}} \tag{E-12}$$

$$\underline{i}_{\mathrm{1dqn}} = \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqn}} \tag{E-13}$$

Substituting (E-10) to (E-13) in (E-7), the active power at the converter side will be

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}}\left(i_{\mathrm{2dp}} - Y_{\mathrm{c}} u_{\mathrm{cqp}}\right) + i_{\mathrm{1dp}}\left(R_1 i_{\mathrm{1dp}} - \omega L_1 i_{\mathrm{1qp}} + R_2 i_{\mathrm{2dp}} - \omega L_2 i_{\mathrm{2qp}}\right) \\ & + e_{\mathrm{qp}}\left(i_{\mathrm{2qp}} + Y_{\mathrm{c}} u_{\mathrm{cdp}}\right) + i_{\mathrm{1qp}}\left(R_1 i_{\mathrm{1qp}} + \omega L_1 i_{\mathrm{1dp}} + R_2 i_{\mathrm{2qp}} + \omega L_2 i_{\mathrm{2dp}}\right) \\ & + e_{\mathrm{dn}}\left(i_{\mathrm{2dn}} + Y_{\mathrm{c}} u_{\mathrm{cqn}}\right) + i_{\mathrm{1dn}}\left(R_1 i_{\mathrm{1dn}} + \omega L_1 i_{\mathrm{1qn}} + R_2 i_{\mathrm{2dn}} + \omega L_2 i_{\mathrm{2qn}}\right) \\ & + e_{\mathrm{qn}}\left(i_{\mathrm{2qn}} - Y_{\mathrm{c}} u_{\mathrm{cdn}}\right) + i_{\mathrm{1qn}}\left(R_1 i_{\mathrm{1qn}} - \omega L_1 i_{\mathrm{1dn}} + R_2 i_{\mathrm{2qn}} - \omega L_2 i_{\mathrm{2dn}}\right) \end{aligned} \tag{E-14}$$

where $Y_{\mathrm{c}} = \omega C_{\mathrm{f}}$. This reduces to

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}} i_{\mathrm{2dp}} + e_{\mathrm{qp}} i_{\mathrm{2qp}} + e_{\mathrm{dn}} i_{\mathrm{2dn}} + e_{\mathrm{qn}} i_{\mathrm{2qn}} \\ & + R_1\left(i_{\mathrm{1dp}}^2 + i_{\mathrm{1qp}}^2 + i_{\mathrm{1dn}}^2 + i_{\mathrm{1qn}}^2\right) \\ & + R_2\left(i_{\mathrm{2dp}} i_{\mathrm{1dp}} + i_{\mathrm{2qp}} i_{\mathrm{1qp}} + i_{\mathrm{2dn}} i_{\mathrm{1dn}} + i_{\mathrm{2qn}} i_{\mathrm{1qn}}\right) \\ & + \omega L_2\left(-i_{\mathrm{2qp}} i_{\mathrm{1dp}} + i_{\mathrm{2dp}} i_{\mathrm{1qp}} + i_{\mathrm{2qn}} i_{\mathrm{1dn}} - i_{\mathrm{2dn}} i_{\mathrm{1qn}}\right) \\ & + Y_{\mathrm{c}}\left(-u_{\mathrm{cqp}} e_{\mathrm{dp}} + u_{\mathrm{cdp}} e_{\mathrm{qp}} + u_{\mathrm{cqn}} e_{\mathrm{dn}} - u_{\mathrm{cdn}} e_{\mathrm{qn}}\right) \end{aligned} \tag{E-15}$$

which can be separated into three different parts as follows

$$P_{\mathrm{ac},1} = P_{\mathrm{ac},2} + \Delta P(i) + \Delta P(e) \tag{E-16}$$

where $\Delta P(i)$ is the active power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta P(e)$ is the active power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

In the same way, the reactive power at the converter side is calculated as

$$\begin{aligned} Q_{\mathrm{ac},1} = {} & e_{\mathrm{qp}} i_{2\mathrm{dp}} - e_{\mathrm{dp}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qn}} \\ & + \omega L_1 \left(i_{1\mathrm{dp}}^2 + i_{1\mathrm{qp}}^2 - i_{1\mathrm{dn}}^2 - i_{1\mathrm{qn}}^2 \right) \\ & + R_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{dp}} - i_{2\mathrm{dp}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qn}} \right) \\ & + \omega L_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{dp}} + i_{2\mathrm{qp}} i_{1\mathrm{qp}} - i_{2\mathrm{dn}} i_{1\mathrm{dn}} - i_{2\mathrm{qn}} i_{1\mathrm{qn}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cqp}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dp}} + u_{\mathrm{cqn}} e_{\mathrm{qn}} + u_{\mathrm{cdn}} e_{\mathrm{dn}} \right) \end{aligned} \tag{E-17}$$

which can be separated into three different parts, as follows

$$Q_{\mathrm{ac},1} = Q_{\mathrm{ac},2} + \Delta Q(i) + \Delta Q(e) \tag{E-18}$$

where $\Delta Q(i)$ is the reactive power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta Q(e)$ is the reactive power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

The sine and cosine components of the active oscillating power are derived as

$$\begin{aligned} P_{\mathrm{s}2,1} = {} & e_{\mathrm{dp}} i_{2\mathrm{qn}} - e_{\mathrm{qp}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dp}} \\ & + 2R_1 \left(i_{1\mathrm{dp}} i_{1\mathrm{qn}} - i_{1\mathrm{qp}} i_{1\mathrm{dn}} \right) \\ & - 2\omega L_1 \left(i_{1\mathrm{qp}} i_{1\mathrm{qn}} + i_{1\mathrm{dp}} i_{1\mathrm{dn}} \right) \\ & + R_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{qn}} - i_{2\mathrm{qp}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dp}} \right) \\ & - \omega L_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{qn}} + i_{2\mathrm{dp}} i_{1\mathrm{dn}} + i_{2\mathrm{qn}} i_{1\mathrm{qp}} + i_{2\mathrm{dn}} i_{1\mathrm{dp}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cdn}} e_{\mathrm{dp}} - u_{\mathrm{cqn}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dn}} - u_{\mathrm{cqp}} e_{\mathrm{qn}} \right) \end{aligned} \tag{E-19}$$

$$P_{s2,1} = P_{s2,2} + \Delta P_{s2}(i) + \Delta P_{s2}(e) \tag{E-20}$$

$$\begin{aligned} P_{c2,1} = {} & e_{dp} i_{2dn} + e_{qp} i_{2qn} + e_{dn} i_{2dp} + e_{qn} i_{2qp} \\ & + 2R_1 \left(i_{1dp} i_{1dn} + i_{1qp} i_{1qn} \right) \\ & + 2\omega L_1 \left(i_{1dp} i_{1qn} - i_{1dn} i_{1qp} \right) \\ & + R_2 \left(i_{2dp} i_{1dn} + i_{2qp} i_{1qn} + i_{2dn} i_{1dp} + i_{2qn} i_{1qp} \right) \\ & + \omega L_2 \left(-i_{2qp} i_{1dn} + i_{2dp} i_{1qn} + i_{2qn} i_{1dp} - i_{2dn} i_{1qp} \right) \\ & + Y_c \left(u_{cqn} e_{dp} - u_{cdn} e_{qp} - u_{cqp} e_{dn} + u_{cdp} e_{qn} \right) \end{aligned} \tag{E-21}$$

$$P_{c2,1} = P_{c2,2} + \Delta P_{c2}(i) + \Delta P_{c2}(e) \tag{E-22}$$

Expressing (E-15) to (E-21) in matrix form will result in

$$\begin{aligned} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} = {} & \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \begin{bmatrix} i_{2dp} \\ i_{2qp} \\ i_{2dn} \\ i_{2qn} \end{bmatrix} \\ & + \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \end{aligned} \tag{E-23}$$

The current references are then calculated using the following matrix

$$\begin{bmatrix} i_{2dp}^* \\ i_{2qp}^* \\ i_{2dn}^* \\ i_{2qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} - Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \tag{E-24}$$

The oscillating power, which is consumed by the filter inductors, is compensated by the power flow from the VSC side. Hence

$$P_{s2,1} = \Delta P_{s2}(i) \tag{E-25}$$

$$P_{c2,1} = \Delta P_{c2}(i) \tag{E-26}$$

Moreover, the active power at the VSC side is assumed to be equal to the power at the DC side of the converter.

$$P_{ac,1} = u_{dc}^{*} i_{v}^{*} \tag{E-27}$$

To achieve zero reactive power at the grid, $Q_{ac,1}$ should supply the reactive power consumed by the filter. Hence

$$Q_{ac,1} = \Delta Q(i) + \Delta Q_{c} \tag{E-28}$$

where ΔQ_{c} is the power loss in the filter capacitor, which is calculated as

$$\Delta Q_{c} = \omega C_{f} \left(u_{cdp}^{2} + u_{cqp}^{2} + u_{cdn}^{2} + u_{cqn}^{2} \right) \tag{E-29}$$

Paper A

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Design of Robust Converter Interface for Wind Power Applications

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Key words:
wind power;
distributed generation;
voltage source converter (VSC);
control;
power electronics;
voltage dips (sags)

As the amount of wind power and other distributed generation with power electronic interface in the grid grows, it becomes unacceptable to disconnect generating units every time a disturbance occurs, as was common practice in the past. Keeping the voltage source converter on-line during unbalanced voltage dips thus becomes a very critical issue. In this article the design of a robust converter interface for wind turbines is investigated. Based on the classification of unbalanced faults that can occur in the grid, resulting in voltage dips at the bus where the turbine is connected, the maximum current that the converter valves must be able to withstand is calculated. The effect of phase angle jumps during faults is also investigated. It is demonstrated that, ultimately, the converter design can be optimized by using statistics of voltage dips and the wind speed distribution for the specific site considered. This is shown by a design example. Copyright © 2005 John Wiley & Sons, Ltd.

Introduction

Integration of distributed generation (DG) in the utility grid offers a number of technical, environmental and economic benefits, both from the utility and the end-user point of view,[1–3] and is therefore becoming more and more popular. The amount of wind power installed in the grid is especially predicted to grow in the coming years.

For variable speed wind turbines, like many other DG technologies, a power electronic interface is used to connect the DG system to the utility grid, with the main function of adapting the characteristics of the active power supplied from the DG to the grid. This power electronic interface usually comprises a current-controlled voltage source converter (VSC) based on IGBT valves, which can be controlled with pulse width modulation (PWM) techniques with high switching frequencies to achieve high controllability and power quality.

The drawback of using a VSC is its sensitivity to voltage disturbances, e.g. voltage dips. A voltage dip is a short-duration drop in voltage that is normally due to a fault.[4] For a VSC a sudden decrease in grid voltage normally causes an increase in current as the control attempts to maintain the power to the DC-link constant. This can lead to tripping of the VSC because of overcurrent in order to protect the IGBTs. Moreover, most faults are unbalanced and result in unbalanced dips, which produce undesirable power oscillations of low-order frequencies resulting in current harmonics and poor DC-link voltage regulation.[5] Ultimately, this can also lead to tripping of the VSC due to DC overvoltage. The common practice in the past has been to disconnect the unit when a fault occurs. However, as the amount of DG with power electronic interface in the grid grows, it becomes unacceptable to lose generating units every time a disturbance occurs. Keeping the VSC on-line during unbalanced voltage dips thus becomes a very critical issue.

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The VSC controller is required to have two main functions: current control and DC-link voltage regulation. A comparison between different types of current controllers for a shunt-connected VSC presented in Reference 6 has proved that the dual vector current controller (DVCC), first proposed in Reference 7, is capable of providing sinusoidal grid currents and regulated DC-link voltage during unbalanced faults. However, an increase in the VSC rating is unavoidable if ride-through capability is desired.

In this article the design of a robust VSC interface for wind turbines is investigated. The performance of the investigated controller during unbalanced dips is demonstrated. Based on the assumption of constant active power flow and the classification of unbalanced faults that can occur in the grid, resulting in voltage dips at the bus where the turbine is connected, the maximum current that the VSC must be able to withstand is calculated. The effect of phase angle jumps during faults is also investigated. It is demonstrated that, ultimately, the VSC design can be optimized by using statistics of voltage dips and the wind speed distribution for the specific site considered. This is shown by a design example.

Voltage Dip Classification

A voltage dip is the voltage experienced at the end-user terminals normally owing to a short-circuit fault somewhere in the grid. In spite of their short duration, between 1 cycle and several seconds, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices. The classification of voltage dips defined by Bollen[4] and reported in Figure 1 is used in this article to quantify the unbalanced voltage dips at the VSC bus. Owing to a fault at bus 3 in Figure 2, a voltage dip occurs at bus 1, which can be either balanced (due to a three-phase fault and called type A) or one of the six unbalanced types in Figure 1.

According to the transformer type, the dip that occurs at bus 1 may change from one type to another, as seen by the VSC connected at bus 2. This transformer (TR) can be one of the following types.

- Type 1: transformers that do not change anything to voltages (e.g. star grounded/star grounded).
- Type 2: transformers that block the zero-sequence voltage (e.g. Y/Y with at least one not grounded or D/Z).
- Type 3: transformers that swap line and phase voltages (e.g. D/Y, Y/D, Y/Z).

The transfer from one dip type to another is listed in Table I. Since this transformer is mainly D/Y (type 3), dips at the equipment terminals are normally of the following five types.

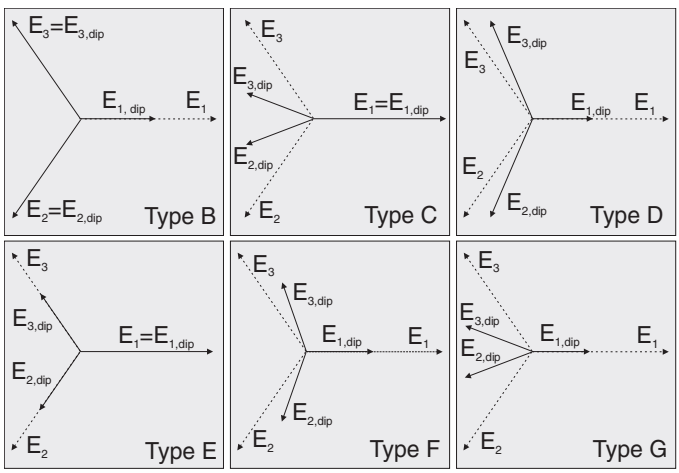

Figure 1. Classification of unbalanced voltage dips from B to G. Phasors of three-phase voltage before (dotted lines) and during fault (full lines) are displayed

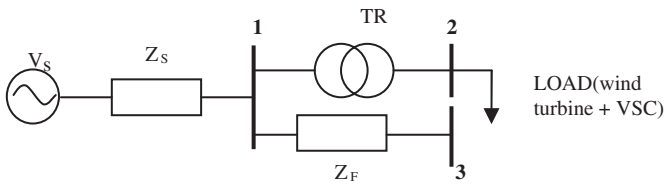

Figure 2. Single-line diagram for dip classification

Table I. Transformation of dip types due to different transformers

Dip type at primary side	A	B	C	D	E	F	G
	Dip type at secondary side						
TR type 1	A	B	C	D	E	F	G
TR type 2	A	D*	C	D	G	F	G
TR type 3	A	C*	D	C	F	G	F

* Indicates that the dip magnitude is not equal to V_{dip} but equal to $\frac{1}{3}+\frac{2}{3}V_{dip}$.

- Type A, due to three-phase faults.
- Types C and D, due to single-phase and double-phase faults.
- Types F and G, due to double-phase-to-ground faults.

Note, however, that the load can in principle be subjected to dips of types B and E if the fault occurs at the same voltage level as the load or if the transformer is of type 1. Therefore we will still consider all seven dip types in the following analysis. In Figure 2, if the X/R ratios for supply impedance Z_S and feeder impedance Z_F are different, the voltage during the fault seen at the terminals of the VSC will have in general a different phase angle as compared with the pre-fault voltage. The impedance angle γ is defined as

$$\gamma = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \tag{1}$$

with $Z_S = R_S + jX_S$ and $Z_F = R_F + jX_F = zl$, where z is the feeder impedance per unit length and l is the feeder length. The expression of the dip voltage at bus 1 will be

$$v_{dip} = \frac{\lambda e^{j\gamma}}{1+\lambda e^{j\gamma}} = V_{dip}\angle\psi \tag{2}$$

where $\lambda e^{j\gamma} = zl/Z_S$, V_{dip} is the dip magnitude and ψ is the phase angle jump. Reference 4 suggests considering four values for the impedance angle γ: 10° as the highest expected value for transmission system faults, 0° as the reference value, −20° for overhead distribution lines and −60° for underground distribution cables. In Figure 3 the relation between the phase angle jump and different dip magnitudes at the four impedance angles is shown. The phase angle jump is bigger for smaller dip magnitudes and is more significant when $\gamma = -60°$.

Investigated System

The investigated system is shown in Figure 4. The VSC is connected to the grid via filter inductors. The three-phase grid currents and voltages are sampled and transformed into dq-vectors via the transformation angle $\theta(k)$ obtained by using a phase-locked loop, which is assumed here to be slow and not to react during faults. The

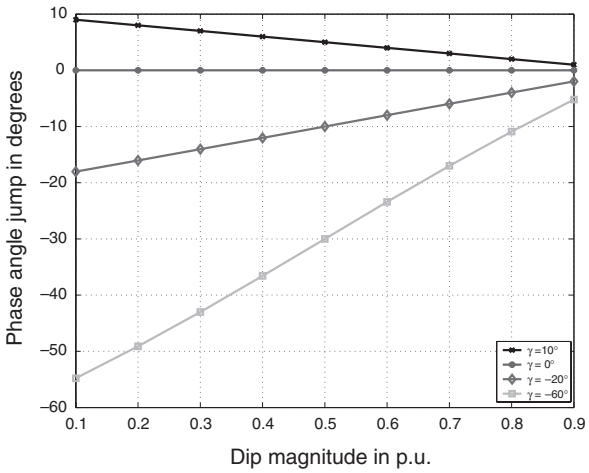

Figure 3. Phase angle jump for different dip magnitudes and impedance angles γ

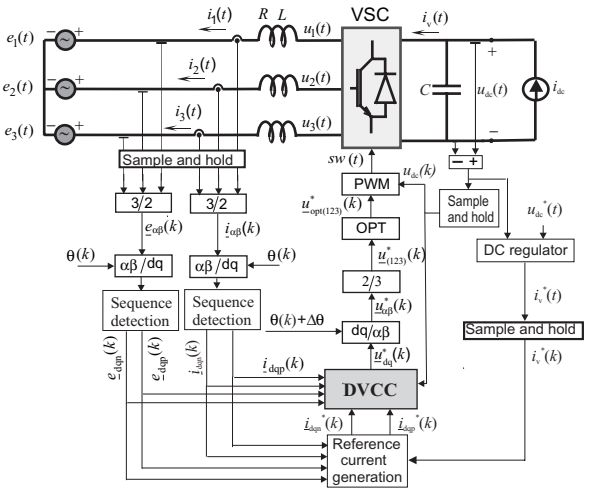

Figure 4. Scheme of investigated system with controller

dq-components of currents and voltages are then used along with the reference current signals in the DVCC to produce the reference voltage signals for the PWM modulator. The voltage across the DC-link capacitor is regulated by using a PI controller, and the output of the DC-link voltage regulator is used to generate the reference currents in order to minimize the ripple of the DC-link voltage by using the algorithm explained later. The reference voltage signals in the *dq*-frame are transformed to three-phase quantities using the angle $\theta(k) + \Delta\theta(k)$, where $\Delta\theta(k)$ compensates for the phase delay due to the execution time of the control computer. The three-phase control signals are then used in the PWM to produce the switching pattern for the VSC. The PWM is optimized to increase the maximum output voltage of the VSC without increasing the DC-link voltage. The block 'OPT' adds a zero-sequence voltage to the control signals. Owing to the absence of a neutral wire, the added zero-sequence waveforms do not result in zero-sequence currents in the grid.

Sequence Detection

The decomposition of the supply voltage into positive and negative sequences is performed in the $\alpha\beta$-frame using the technique proposed in Reference 6. By delaying the measured supply voltage by one-fourth of the

line period T, a vector composed of the same positive-sequence component and a negative-sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative-sequence voltage will be removed. The positive-sequence voltage component can thus be extracted from the measured values as

$$\mathbf{e}_{\mathrm{Pos}}^{(\alpha\beta)} = \frac{1}{2}\left[\mathbf{e}^{(\alpha\beta)}(t) + \mathrm{j}\mathbf{e}^{(\alpha\beta)}\left(t - \frac{T}{4}\right)\right] \tag{3}$$

The negative sequence can be calculated as

$$\mathbf{e}_{\mathrm{neg}}^{(\alpha\beta)} = \frac{1}{2}\left[\mathbf{e}^{(\alpha\beta)}(t) - \mathrm{j}\mathbf{e}^{(\alpha\beta)}\left(t - \frac{T}{4}\right)\right] \tag{4}$$

Then the positive-sequence voltage in the positive-rotating co-ordinate (dqp) is

$$\mathbf{e}_{dq\mathrm{p}} = e^{-\mathrm{j}\theta}\mathbf{e}_{\mathrm{Pos}}^{(\alpha\beta)} \tag{5}$$

and the negative-sequence voltage in the negative-rotating co-ordinate (dqn) is

$$\mathbf{e}_{dq\mathrm{n}} = e^{\mathrm{j}\theta}\mathbf{e}_{\mathrm{neg}}^{(\alpha\beta)} \tag{6}$$

The latter will be seen as a constant signal in the negative-rotating plane dqn, which utilizes the opposite angle for the dq-transformation.

Implementing the DVCC

The DVCC consists of two PI controllers that control the positive- and negative-sequence currents separately, as shown in Figure 5. Since all unbalanced faults contain positive- and negative-sequence components, the DVCC has proved to give better performance than only one controller implemented in the positive dq-frame concerning the grid current harmonics and DC voltage ripples.[6]

The positive-sequence current controller is described for a sampling instant k in the dqp-frame by the equation

$$\mathbf{u}_{dq\mathrm{p}}^{*}(k+1) = \mathbf{e}_{dq\mathrm{p}}(k) + R\mathbf{i}_{dq\mathrm{p}}(k) + \mathrm{j}\omega L\mathbf{i}_{dq\mathrm{p}}(k) + 0.7k_{\mathrm{p}}(\mathbf{i}_{dq\mathrm{p}}^{*}(k)\mathbf{i}_{dq\mathrm{p}}(k)) - \Delta\mathbf{u}_{\mathrm{I},dq\mathrm{p}}(k) \tag{7}$$

where $\mathbf{i}_{dq\mathrm{p}}(k)$ is the positive-sequence grid dq-current, $\mathbf{i}^{*}_{dq\mathrm{p}}(k)$ is the positive-sequence reference dq-current and k_{p} is the dead-beat gain. The integration term $\Delta\mathbf{u}_{\mathrm{I},dq\mathrm{p}}(k)$ is defined as

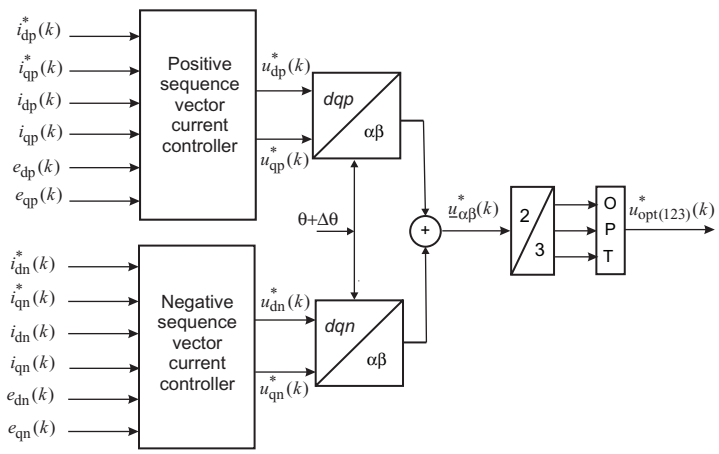

Figure 5. Block scheme of DVCC

$$\Delta\mathbf{u}_{\mathrm{I},dqp}(k+1) = \Delta\mathbf{u}_{\mathrm{I},dqp}(k) + k_{\mathrm{I}}\left(\mathbf{i}^{*}_{dqp}(k-1) - \mathbf{i}_{dqp}(k)\right) \tag{8}$$

With analogous notation the negative-sequence current controller is described by the equation

$$\mathbf{e}^{*}_{dqn}(k+1) = \mathbf{e}_{dqn}(k) + R\mathbf{i}_{dqn}(k) - \mathrm{j}\omega L\mathbf{i}_{dqn}(k) + 0.7k_p\left(\mathbf{i}^{*}_{dqn}(k) - \mathbf{i}_{dqn}(k)\right) + \Delta\mathbf{u}_{\mathrm{I},dqn}(k) \tag{9}$$

and is implemented in the *dq*n-frame.

Reference Current Generation

In order to generate proper current references, consider the complex apparent power from the grid

$$\mathbf{S}_{\mathrm{g}} = \left(\mathbf{e}_{dqp}e^{\mathrm{j}\omega t} + \mathbf{e}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)\left(\mathbf{i}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \mathbf{i}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)^{\mathrm{conj}} \tag{10}$$

which is the sum of a constant apparent power and two terms in sine and cosine, oscillating with double the grid frequency. By expanding equation 10, the following expression in matrix form can be written:

$$\begin{bmatrix} P_{\mathrm{g}} \\ Q_{\mathrm{g}} \\ P_{\mathrm{S2g}} \\ P_{\mathrm{c2g}} \end{bmatrix} = \begin{bmatrix} e_{d\mathrm{p}} & e_{q\mathrm{p}} & e_{d\mathrm{n}} & e_{q\mathrm{n}} \\ e_{q\mathrm{p}} & -e_{d\mathrm{p}} & e_{q\mathrm{n}} & -e_{d\mathrm{n}} \\ e_{q\mathrm{n}} & -e_{d\mathrm{n}} & -e_{q\mathrm{p}} & e_{d\mathrm{p}} \\ e_{d\mathrm{n}} & e_{q\mathrm{n}} & e_{d\mathrm{p}} & e_{q\mathrm{p}} \end{bmatrix} \begin{bmatrix} i_{d\mathrm{p}} \\ i_{q\mathrm{p}} \\ i_{d\mathrm{n}} \\ i_{q\mathrm{n}} \end{bmatrix} \tag{11}$$

where P_{g} and Q_{g} are the constant active and reactive powers respectively and P_{s2g} and P_{c2g} represent the second-harmonic sine and cosine components of the active power respectively. These are the oscillating powers due to the imbalance in the grid voltages. The fluctuating reactive powers are not considered since they do not affect the DC-link voltage and its control.

Calculating the apparent power $\mathbf{S}_{\mathrm{ac}}$ at the VSC terminals as in (10), but with the VSC voltages in place of the grid voltages, and considering that $\mathbf{S}_{\mathrm{ac}}$ is the sum of the apparent power from the grid ($\mathbf{S}_{\mathrm{g}}$) and the apparent power dissipated in the filter ($\Delta\mathbf{S}$), i.e.

$$\mathbf{S}_{\mathrm{ac}} = \mathbf{S}_{\mathrm{g}} + \Delta\mathbf{S} \tag{12}$$

the reference currents can be calculated as

$$\begin{bmatrix} i^{*}_{d\mathrm{p}} \\ i^{*}_{q\mathrm{p}} \\ i^{*}_{d\mathrm{n}} \\ i^{*}_{q\mathrm{n}} \end{bmatrix} = \begin{bmatrix} e_{d\mathrm{p}} & e_{q\mathrm{p}} & e_{d\mathrm{n}} & e_{q\mathrm{n}} \\ e_{d\mathrm{p}} & -e_{q\mathrm{p}} & e_{q\mathrm{n}} & -e_{d\mathrm{n}} \\ e_{q\mathrm{n}} & -e_{d\mathrm{n}} & -e_{q\mathrm{p}} & e_{d\mathrm{p}} \\ e_{d\mathrm{n}} & e_{q\mathrm{n}} & e_{d\mathrm{p}} & e_{q\mathrm{p}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta P \\ 0 \\ -\Delta P_{\mathrm{s2}} \\ -\Delta P_{\mathrm{c2}} \end{bmatrix} \tag{13}$$

where P_{dc} is the power at the DC side of the converter, which is considered equal to the active power at the AC terminals neglecting the losses, and ΔP, ΔP_{c2} and ΔP_{s2} are the active powers dissipated in the filter, given by

$$\Delta P = R(i^2_{d\mathrm{p}} + i^2_{q\mathrm{p}} + i^2_{d\mathrm{n}} + i^2_{q\mathrm{n}}) \tag{14}$$

$$\Delta P_{\mathrm{c2}} = 2R(i_{d\mathrm{p}}i_{d\mathrm{n}} + i_{q\mathrm{p}}i_{q\mathrm{n}}) + 2\omega L(i_{d\mathrm{p}}i_{q\mathrm{n}} - i_{q\mathrm{p}}i_{d\mathrm{n}}) \tag{15}$$

$$\Delta P_{\mathrm{s2}} = 2R(i_{d\mathrm{p}}i_{d\mathrm{n}} - i_{q\mathrm{p}}i_{d\mathrm{n}}) + 2\omega L(-i_{d\mathrm{p}}i_{d\mathrm{n}} - i_{q\mathrm{p}}i_{q\mathrm{n}}) \tag{16}$$

DC-link Voltage Regulator

In variable speed wind turbine systems the DC-link voltage cannot be considered constant. It should be regulated to ensure correct operation of the VSC and to avoid damage to the valves and the DC-link capacitor. The current from the DG source to the DC-link is also not constant, but its variations can be assumed to be much

slower than the time range of the transient phenomena considered here. Therefore the DC-link is modelled as a capacitor with a current source in parallel. A simple PI controller is implemented, where the measured DC capacitor voltage u_{dc} is compared with its reference value u^*_{dc} and the error signal is used to produce a reference DC current signal i^*_v according to

$$i_v^*(s) = -k_{pdc}\left(1 + \frac{1}{sT_{idc}}\right)\left(u_{dc}^*(s) - u_{dc}(s)\right) \tag{17}$$

where k_{pdc} and T_{idc} are the proportional gain and integral time constant of the DC PI controller respectively and s is the Laplace operator.

DC-link Capacitor Design

The instantaneous active power difference between the AC and DC side is stored in the capacitor, which causes the DC link voltage to vary. Hence the size of the capacitor can be determined from the constraint on the maximum allowed DC-link voltage ripple Δu_{dc}. The design expression for the DC-link capacitor size, which has been derived based on a simplified analysis of the instantaneous active power flow in Reference 8, is

$$C = \frac{S_n}{u_{dc}^* \Delta u_{dc}} \frac{1}{2\omega_n} \tag{18}$$

where S_n and ω_n are the rated power of the VSC and the fundamental angular frequency of the grid respectively. The allowed Δu_{dc} is considered as ±5% of the rated voltage, resulting in a DC capacitance of 5.2 mF. However, owing to the high performance of the DC-link voltage controller along with DVCC, the size of the capacitance is reduced to 550 μF.

Performance Analysis

Response to Unbalanced Dips

For the investigated system, all six unbalanced dip types with magnitude varying between 0.3 and 0.9 pu in steps of 0.1 pu have been simulated using Matlab/Simulink. The dip starts at 0.1 s and ends at 0.2 s. System data and controller data are shown in Tables II and III, respectively.

As an example, the grid currents in the three-phase domain and the DC-link voltage are shown in Figure 6 for a dip of type C with magnitude 40%. During the dip the grid currents increase to about 3 pu. The DC voltage shows a variation during the transients at the beginning and end of the dip. However, the ripple during the transient is not bigger than 10% peak-to-peak and is quite quickly damped to almost zero.

Table II. System data

Constant	Symbol	Value	Value in pu
Nominal AC voltage	E	400 V	1.0
Nominal phase current	I_n	100 A	1.0
Nominal grid frequency	f_n	50 Hz	
Nominal DC voltage	U_{dc}	650 V	1.0 (DC)
Nominal DC current	I_{dc}	107 A	1.0 (DC)
Filter resistance	R	23 mΩ	0.01
Filter inductance	L	0.73 mH	0.1
DC-link capacitance	C	550 μF	τ = 1.7 ms

Table III. Controller data

Constant	Symbol	Value/equation
Sampling frequency	f_S	5 kHz
Sampling time	T_S	200 μs
Dead-beat gain	K_p	$\frac{L}{T_S}+\frac{R}{2}=3.7$
Integration time constant	T_i	0.03
DC controller proportional gain	k_{pdc}	0.2
DC controller integral constant	T_{idc}	$\frac{4\zeta^2}{K_{pdc}}C$
DC controller damping ratio	ζ	0.7

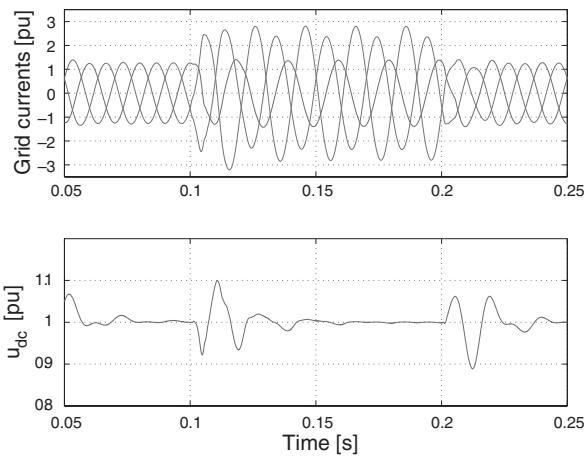

Figure 6. Grid currents (top) and DC voltage (bottom) for 40% dip type C

Maximum grid current and peak-to-peak DC voltage ripple during the dip are shown for all dip types with varying magnitudes in Figure 7. In order to ride through dips with a minimum retained voltage of 30%, the VSC valves should be able to carry a maximum current of 3.65 pu. The maximum DC voltage ripple is ±0.5% around the nominal value for dip magnitudes higher than 30%.

Effect of the Phase Angle Jump

The four values of impedance angle $\gamma = 10°, 0°, -20°$ and $-60°$ are used. Again for a dip of type C with retained voltage 40%, Figure 8 shows that only in the case of $\gamma = -60°$ does the phase angle jump seem to have an effect on the DC voltage ripple. The effect of the phase angle jump on the maximum grid current is represented in Figure 9 for all unbalanced dip types.

No noticeable effect can be seen for $\gamma = 10°$ or $\gamma = -20°$, where the maximum grid current is the same as without phase angle jump. On the other hand, for $\gamma = -60°$ the current is higher and the effect is more significant as the dip magnitude decreases. The absolute maximum current is found for dip type D with magnitude 30% and is equal to 4.5 pu, which is significantly higher than the corresponding value found with zero phase angle jump (3.65 pu). It might therefore be deemed necessary to consider the phase angle jump explicitly in the design.

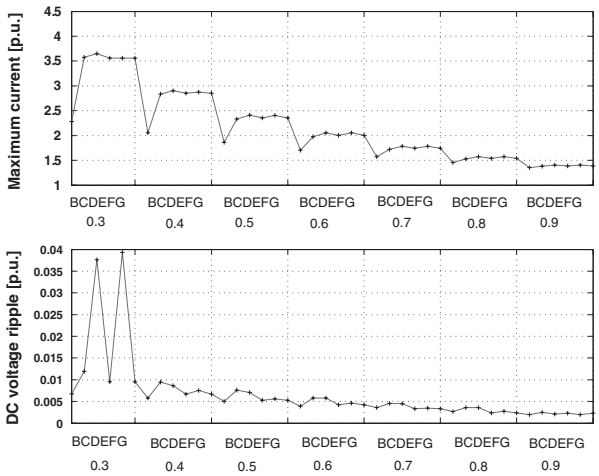

Figure 7. Maximum grid current (top) and DC voltage ripple (bottom) for all unbalanced dip types with magnitude between 0.3 and 0.9 pu

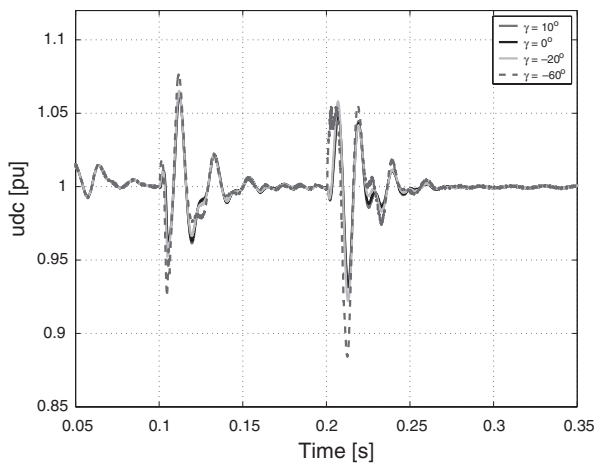

Figure 8. DC-link voltage for 40% dip type C

Converter Design

Design Equations of Maximum Current

In order to calculate the required current rating of the VSC valves to ride through voltage dips in the grid, the maximum current has been calculated for unbalanced faults. Equation (13) has been used to calculate the current components in the *dq*p- and *dq*n-frame assuming zero oscillating powers. Furthermore, the phase angle jump is assumed to be zero, which result in zero *q*p- and *q*n-components of the grid voltage according to Table IV. The grid current is then described as

$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \frac{KP_{dc}}{e_{dp}^2 - e_{dn}^2} \begin{bmatrix} e_{dp} \\ 0 \\ -e_{dn} \\ 0 \end{bmatrix} \tag{19}$$

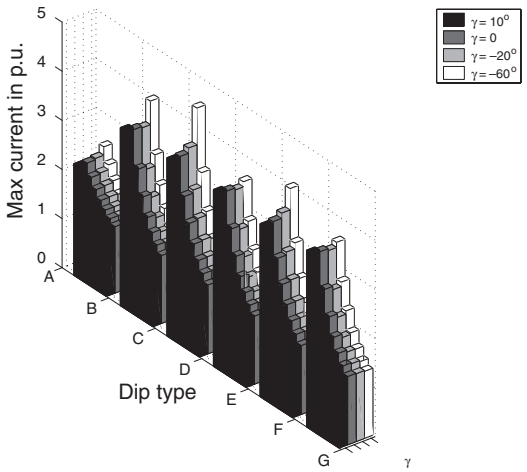

Figure 9. Effect of phase angle jump on maximum grid current for all unbalanced dips (types B–G) with magnitude between 30% and 90% (dip magnitude increases for each type going from left to right)

Table IV. Positive- and negative-sequence *dq*-components of grid voltage for unbalanced voltage dips with phase angle jump

Dip	e_{dp}	e_{qp}	e_{dn}	e_{qn}
A	$EV_{\text{dip}}\cos\psi$	$EV_{\text{dip}}\sin\psi$	0	0
B	$\frac{E}{3}(2+V_{\text{dip}}\cos\psi)$	$\frac{E}{3}V_{\text{dip}}\sin\psi$	$\frac{-E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{-E}{3}V_{\text{dip}}\sin\psi$
C	$\frac{E}{2}(1+V_{\text{dip}}\cos\psi)$	$\frac{E}{2}V_{\text{dip}}\sin\psi$	$\frac{E}{2}(1-V_{\text{dip}}\cos\psi)$	$\frac{E}{2}V_{\text{dip}}\sin\psi$
D	$\frac{E}{2}(1+V_{\text{dip}}\cos\psi)$	$\frac{E}{2}V_{\text{dip}}\sin\psi$	$\frac{-E}{2}(1-V_{\text{dip}}\cos\psi)$	$\frac{-E}{2}V_{\text{dip}}\sin\psi$
E	$\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$	$\frac{2E}{3}V_{\text{dip}}\sin\psi$	$\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{E}{3}V_{\text{dip}}\sin\psi$
F	$\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$	$\frac{2E}{3}V_{\text{dip}}\sin\psi$	$\frac{-E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{-E}{3}V_{\text{dip}}\sin\psi$
G	$\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$	$\frac{2E}{3}V_{\text{dip}}\sin\psi$	$\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{E}{3}V_{\text{dip}}\sin\psi$

where P_{dc} is the nominal input DC power and K is the ratio of the input power actually delivered to the DC-link. The current components are then transformed back into three-phase quantities in positive and negative-sequence frames and then into three-phase current using the Park transformation.

In the case of single-phase faults (dip types B and D) the maximum phase current (phase *a*) is calculated as

$$I_{\max}=\sqrt{\frac{2}{3}}\frac{KP_{\text{dc}}}{e_{dp}+e_{dn}} \tag{20}$$

while for two-phase faults (dip types C, E, F and G) the maximum phase current (phase *b*) is calculated as

$$I_{\max}=\sqrt{\frac{2}{3}}\frac{KP_{dc}}{e_{dp}^2-e_{dn}^2}\sqrt{\frac{1}{4}(e_{dp}-e_{dn})^2+\frac{3}{4}(e_{dp}+e_{dn})^2} \tag{21}$$

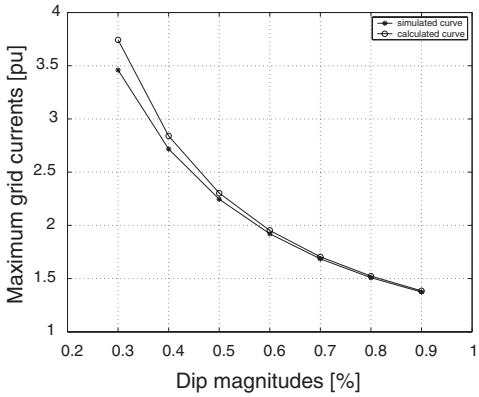

Figure 10. Maximum current for dip type C: simulated (asterisks) and calculated (circles)

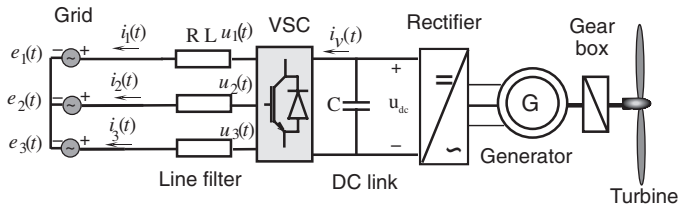

Figure 11. Wind turbine system

The values of $e_{d\mathrm{p}}$ and $e_{d\mathrm{n}}$, which are the positive and negative sequences of the d-component of the grid voltage respectively, are calculated using Table IV for different voltage dips (where E is the phase-to-phase RMS grid voltage, V_{dip} is the dip magnitude and ψ is the phase angle jump). Note that since the dips have zero phase angle jump, the d-components correspond to the magnitudes of their sequence voltages.

A comparison between the calculated and simulated maximum current values has been performed for all dip types. The calculated values are slightly overestimated, as shown in Figure 10 for dip type C. However, the error, which is mostly due to not considering the oscillating powers dissipated in the filter in the calculations, is considered acceptable. The overestimation gives a safety margin to the design.

Design Example

The system in Figure 4 is to be implemented in a wind turbine system (Figure 11) with turbine rated power 180 kW, turbine speed $\omega_{\mathrm{S}} = 42$ rpm, gearbox ratio 23.75 and blade radius $R = 11.5$ m. The mechanical efficiency of the turbine, C_{P}, which measures how efficiently the turbine converts the energy in the wind to electricity, has its largest value of 44% at a wind speed around 9 m s^{-1}.[9]

The conversion from wind speed to mechanical power is described by

$$P = \frac{\pi \rho \omega_{\mathrm{S}}^3 R^2}{2} C_{\mathrm{P}}(\omega_{\mathrm{S}}) \tag{22}$$

where ρ is the air density, which is set to 1.225 kg m^{-3}. Using the given data, the power curve for the turbine is obtained as in Figure 12. The power is expressed in per unit of the rated power of the turbine. The efficiency of the electrical generator is set to 100%. The wind variation of a typical site can be described using the Weibull distribution, as displayed in Figure 13, which shows the probability density for the wind speed at two sites

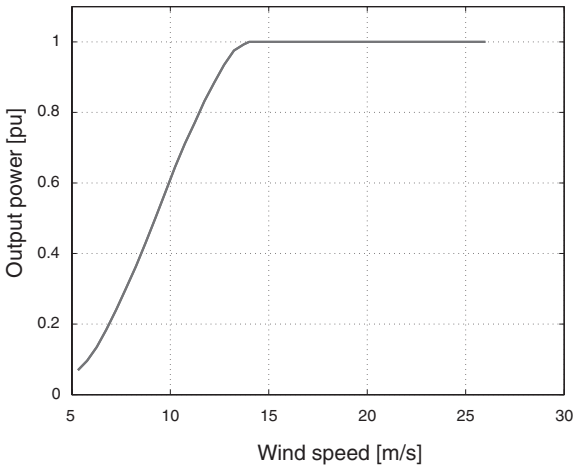

Figure 12. Electrical power output of turbine as a function of wind speed

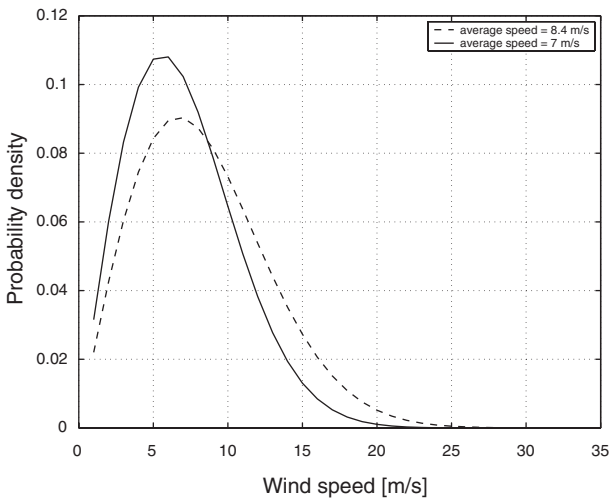

Figure 13. Weibull distribution for a site with average wind speed 8.4 m s^{-1} (broken line) and 7 m s^{-1} (full line)

with average speeds of 8.4 and 7 m s^{-1}, respectively. The shape parameter for the two curves is set to 2.[10] By integrating the probability density in Figure 13 and combining it with the power curve in Figure 12, the curve in Figure 14 is obtained. This represents the probability that a given maximum output power is produced.

Assume now that it is required to keep the system on-line for 80% of the time during a year. This means that the maximum power that can be obtained statistically is about 0.86 pu for a site with an average wind speed of 8.4 m s^{-1}. For a site with an average wind speed of 7 m s^{-1}, a maximum power of 0.61 pu is obtained. The maximum VSC currents for these two power levels for all unbalanced voltage dips are plotted in Figure 15.

From Figure 15 it is concluded that the VSC will stay in operation in the case of dips with magnitude higher than 80% for the first site and 50% for the second site. If the VSC must ride through all dips starting with magnitude higher than 30%, it must be rated 2.4 pu for the first site and about 1.8 pu for the second site. The same figures can be calculated using the design equations derived previously.

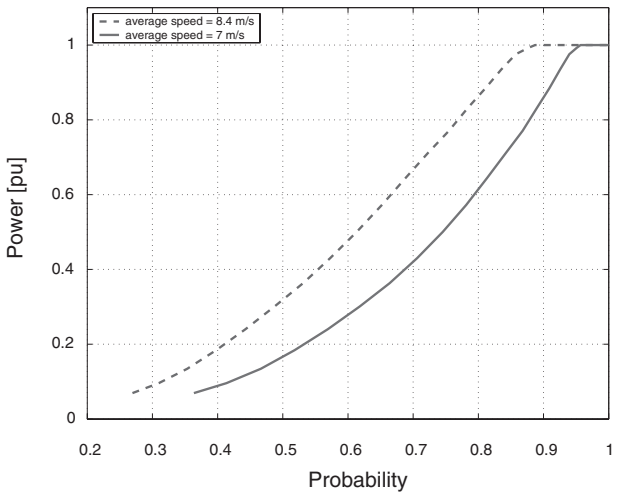

Figure 14. Probability of output power production from wind turbine

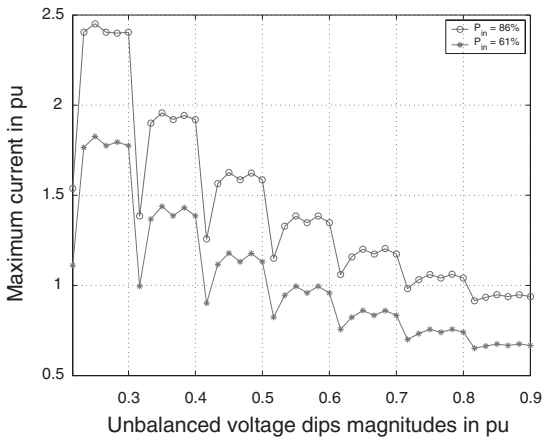

Figure 15. Maximum grid current for unbalanced voltage dips with magnitudes 0.3–0.9 pu with VSC input power P_{in} = 86% and 61%

By considering the statistical character of the wind power output, it becomes clear that, even without oversizing the VSC interface, some limited ride-through capability is ensured. However, if a higher ride-through capability is required, some overrating of the VSC will be necessary. This can be limited by accepting a certain risk of tripping (in the given example the risk would be 20%).

Conclusions

In this article, the design of a robust voltage source converter (VSC) interface for a wind turbine with a VSC has been investigated. The performance of the dual vector current controller (DVCC) has been presented for all unbalanced voltage dips that can occur at the point of connection of the wind turbine. Attention is focused

on the DC-link voltage ripple, which should be minimized, and on the maximum grid current during the dip, which determines the ride-through capability for the whole wind turbine system.

Based on the classification of unbalanced faults that can occur in the grid, resulting in voltage dips at the bus where the turbine is connected, the maximum current that the VSC must be able to withstand has been calculated. The effect of phase angle jumps during faults has also been investigated. It is demonstrated that, ultimately, the VSC design can be optimized by using statistics of wind speed distribution for the specific site considered. This is shown by a design example.

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Paper B

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Transient Performance of Voltage Source Converter under Unbalanced Voltage Dips

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***Abstract*- Robust operation of Voltage Source Converters under unbalanced voltage dips can be obtained by controlling the positive and negative-sequence currents separately with a Dual Vector Current Controller (DVCC). In this paper, the performance of the DVCC is investigated under all voltage dips that can affect the converter. Two different methods for taking into account the oscillating powers dissipated in the filter are presented, tested and compared. The effect of the phase-angle jump of the dip is also studied.**

***Index Terms*- Voltage Source Converter (VSC), current controller, voltage dip (sag), unbalance.**

I. Introduction

The three-phase Voltage Source Converter (VSC) is the basic component of most new FACTS and custom power equipment because of its good controllability and power quality. It is also used as interface to dispersed or distributed generation or in electric drive applications. In many of these applications, the voltage across the DC-link capacitor must be regulated.

A drawback of using VSC is its sensitivity to voltage disturbances, e.g. voltage dips. For a VSC, a sudden decrease in the grid voltage normally causes an increase in current, as the control attempts at maintaining the power to the DC-link constant, which can cause the VSC to trip to protect the valves. Moreover, most dips are due to unbalanced faults propagating in the grid. The resulting unbalanced voltages produce undesirable power oscillations of low order frequencies, which result in current harmonics and poor DC-link voltage regulation. The latter can also lead to tripping of the converter to avoid damage to the equipment due to DC overvoltage. In order to keep the VSC working adequately in these conditions, a robust control scheme should be developed.

A comparison between different types of vector current controllers (VCCs) for shunt connected VSC presented in [1] has proved that the Dual Vector Current Controller (DVCC) shows the best performance regarding grid currents and DC-link voltage during faults. This controller, which was first proposed in [2], uses two different VCCs for positive and negative sequence components, together with a DC-link voltage controller based on the instantaneous active and reactive power theory. However, in reference [2] the oscillating powers that are dissipated in the filter are neglected. In reference [3] these oscillating powers are considered compensated by the filter, but the performance of the controller is shown only in two unbalance cases. Moreover, both [2] and [3] only show results in steady-state conditions. When the VSC is subjected to voltage dips, the speed of response becomes critical. The method for sequence separation applied in [3] implies a delay of 2/3 of period, which will greatly impact the transient performance.

In this paper, the performance of the DVCC is investigated under all voltage dips that can affect the VSC. Two different methods for taking into account the oscillating powers dissipated in the filter are presented, tested and compared. The effect of the phase-angle jump of the dip is also studied.

II. Voltage Dips

A voltage dip is the voltage experienced at the end user terminals due to a short-circuit fault at a certain point in the electrical network. It can also happen due to motor starting or overloads. In spite of their short duration, between one cycle and several seconds, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [4] [5].

A. Voltage Dip Classification

The voltage dip classification defined by Bollen [6] and reported in Fig.1 has been used in this paper to quantify the unbalanced voltage dips at the VSC bus. The magnitude, indicated as E_{dip} or V_{dip}, is equal to the retained voltage for a single-phase dip. For a three-phase dip, the expressions of the three phase voltages for given dip magnitude and type are given in [6]. Due to a fault at bus 3 in Fig.2, a voltage dip occurs at bus 1, which can be balanced (due to a three-phase fault, and called type A), or of any of the six unbalanced types in Fig.1. According to the transformer (TRF) type, the dip that occurs at bus 1 may change from one type to another, as seen by the VSC connected at bus 2. This transformer can be: Type 1, which does not change anything to voltages (e.g. star grounded/star grounded); Type 2, which removes the zero-sequence voltage (e.g. Y/Y with at least one side not grounded or D/Z); Type 3, which swaps line and phase voltages (e.g. D/Y, Y/D, Y/Z). The transformation from one type to another is listed in Table 1. Since distribution transformers are often D/Y (Type 3), we normally find five types at the equipment terminals: Type A, due to three-phase faults; Type C and D, due to single-phase and double-phase faults; Type F and G, due to double-phase to ground faults. Note, however, that the load can in principle be subjected to dips of type B and E if the fault occurs at the same voltage level as the load or if the transformer is type 1.

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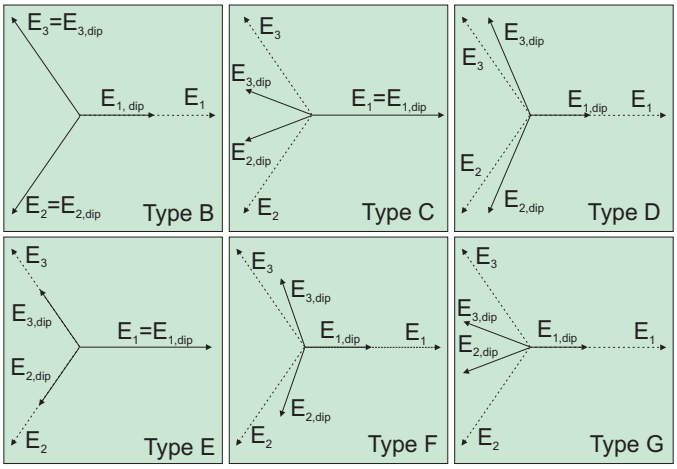

Fig.1. Voltage dip classification from B to G. Phasors of three phase voltage before (dotted) and during fault (solid) are displayed.

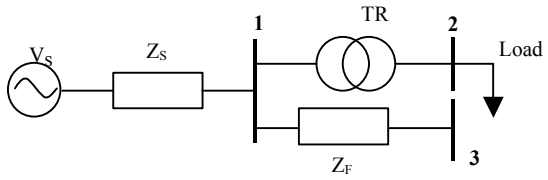

Fig.2. One-line model for dip analysis.

TABLE 1
TRANSFORMATION OF VOLTAGE DIPS THROUGH TRF

	Dip on the primary side						
Dip type	A	B	C	D	E	F	G
TRF type1	A	B	C	D	E	F	G
TRF type2	A	D*	C	D	G	F	G
TRF type3	A	C*	D	C	F	G	F

The superscript * indicates that the dip magnitude is equal to $\frac{1}{3}+\frac{2}{3}V_{dip}$.

B. Phase-angle jump

In Fig.2, if the X/R ratio for Z_S and Z_F is different, the voltage seen at the VSC terminals during the fault will have a different phase angle as compared to the pre-fault voltage. If the impedance angle α is defined as:

$$\alpha = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \quad (1)$$

where $Z_S = R_S + jX_S$, $Z_F = R_F + jX_F = zl$, z is the feeder impedance per unit length and l is the feeder length, the expression of the dip voltage at bus 1 will be:

$$v_{dip} = \frac{\lambda e^{j\alpha}}{1+\lambda e^{j\alpha}} = V_{dip}\angle\psi \quad (2)$$

where $\lambda e^{j\alpha} = zl / Z_S$, V_{dip} is the dip magnitude and ψ the "phase angle jump". In Fig.3 the relation between dip magnitude and phase angle jump for different impedance angles is shown.

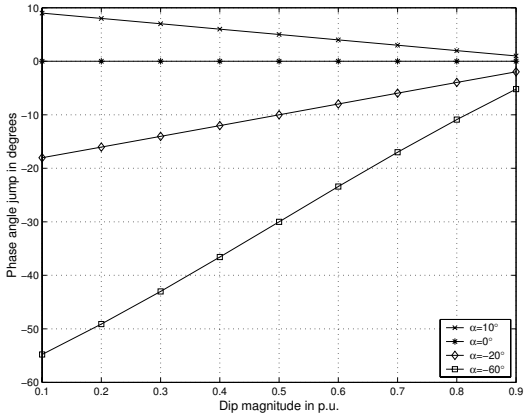

Fig.3. Phase angle jump for different dip magnitudes and impedance angles.

Four values for the angle α suggested by reference [6] are considered: 10^o as the highest expected value for transmission system faults, 0^o as the reference value, -20^o for overhead distribution lines, and -60^o for underground distribution cables. The phase angle jump is bigger for smaller dip magnitudes and is more significant when $\alpha = -60^o$.

III. INVESTIGATED SYSTEM

A scheme of the investigated system is shown in Fig.4. The VSC of rated power 69KVA is connected to the 400 V grid via a filter inductor. The DC side has a constant input DC current, while the DC voltage across the capacitor is regulated.

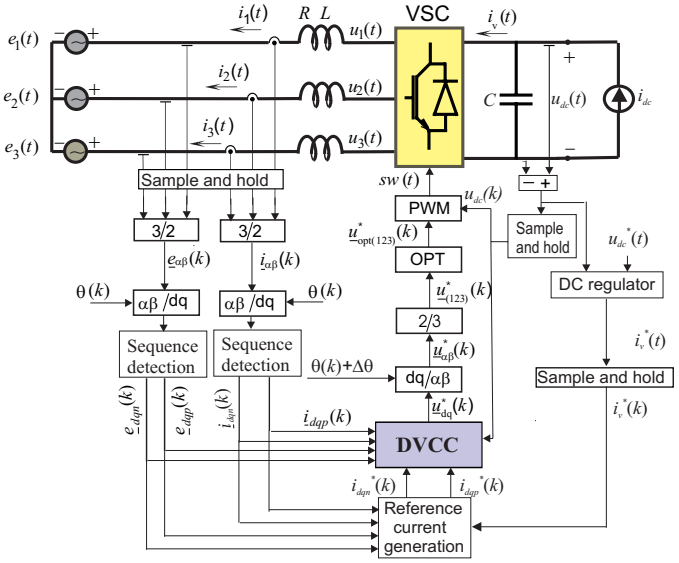

Fig.4. Scheme of investigated system.

The three-phase grid currents and voltages are sampled and transformed into vectors in the fixed $\alpha\beta$-frame and then into a rotating dq-frame synchronized with the grid voltage. This is done by using the transformation angle $\theta(k)$ obtained by using a PLL, which is assumed here to be slow and not to react during faults. The dq-components of currents and voltages are then separated into their positive and negative

sequence components, which are used along with the reference current signals in the DVCC to produce the reference voltage signals for the PWM modulator. The reference currents are produced by the "reference current generation algorithm" explained later, which uses the signal coming from the DC voltage regulator. The reference voltage signals in the *dq*-frame are transformed to three-phase quantities using the angle $\theta(k)+\Delta\theta(k)$, where $\Delta\theta(k)$ compensates for the error due to the calculation time. The three-phase control signals are then used in the PWM modulator to produce the switching pattern for the VSC. The PWM is optimized by adding a zero sequence voltage to the control signals in the block "OPT," in order to increase the maximum output voltage of the converter without increasing the DC-link voltage.

The different parts of the controller are described in more detail in the following.

A. Sequence detection

The decomposition of the supply voltage into positive and negative-sequence is performed in a *dq*-frame synchronised with the positive sequence (indicated as *dqp*), with the technique proposed in [7]. By delaying the *dq*-vector of the measured supply voltage by one fourth of the period *T* at the fundamental frequency, a vector composed of the same positive sequence component and a negative sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative sequence voltage will be removed. The positive sequence voltage component can thus be extracted from the measured values as

$$\underline{e}_{dqp} = \frac{1}{2}\left(\underline{e}_{dq}(t) + \underline{e}_{dq}\left(t - \frac{T}{4} \right) \right) \tag{3}$$

The negative sequence can be calculated as

$$\underline{e}_{dqn} = \frac{1}{2}\left(\underline{e}_{dq}(t) - \underline{e}_{dq}\left(t - \frac{T}{4} \right) \right) \tag{4}$$

The latter will be seen as a constant signal in the negative rotating plane *dqn*, which utilizes the opposite angle for the *dq*-transformation.

B. Implementing DVCC

The DVCC consists of two separate PI-controllers, for controlling the positive-sequence and the negative-sequence currents separately, as shown in Fig.5. The positive-sequence VCC is described for a sampling instant *k* in the *dqp*-frame by the following equation:

$$\begin{aligned} \underline{u}^{*}_{dqp}(k) = {} & \underline{e}_{dqp}(k) + R \cdot \underline{i}_{dqp}(k) + \mathrm{j}\omega L \cdot \underline{i}_{dqp}(k) + \\ & k_p \cdot \left(\underline{i}^{*}_{dqp}(k) - \underline{i}_{dqp}(k) \right) + \Delta \underline{u}_{I,dqp}(k) \end{aligned} \tag{5}$$

where $\underline{i}_{dqp}(k)$ is the positive sequence grid *dq*-current, $\underline{i}^{*}_{dqp}(k)$ is the positive sequence reference *dq*-current, k_p is the dead beat gain. The integration term $\Delta \underline{u}_{I,dqp}(k)$ is defined as

$$\Delta \underline{u}_{I,dqp}(k+1) = \Delta \underline{u}_{I,dqp}(k) + k_I \cdot \left(\underline{i}^{*}_{dqp}(k-1) - \underline{i}_{dqp}(k) \right) \tag{6}$$

With analogous notations, the negative sequence VCC is described by the following equation

$$\begin{aligned} \underline{u}^{*}_{dqp}(k) = {} & \underline{e}_{dqn}(k) + R \cdot \underline{i}_{dqn}(k) - \mathrm{j}\omega L \cdot \underline{i}_{dqn}(k) + \\ & k_p \cdot \left(\underline{i}^{*}_{dqn}(k) - \underline{i}_{dqn}(k) \right) + \Delta \underline{u}_{I,dqn}(k) \end{aligned} \tag{7}$$

and is implemented in the *dqn*-frame.

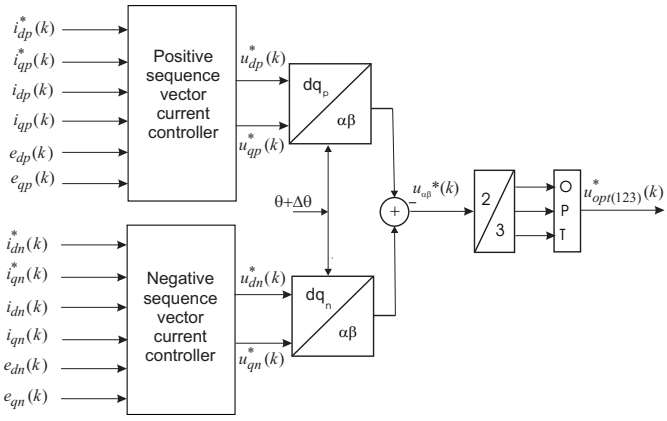

Fig.5. Simplified block scheme for DVCC.

C. DC-link voltage regulator

In many applications, e.g. drive systems and variable-speed wind turbines, the DC-link voltage cannot be considered constant. However, it should be regulated to insure correct operation of the VSC and to avoid damage to the power electronic switches and DC-link capacitor. Also the current to the DC-link is not constant. But its variations can be assumed to be much slower than the time range of the transient phenomena considered here. Therefore the DC-link is modeled as a capacitor with a current source in parallel.

A simple PI-controller is implemented, where the measured DC capacitor voltage u_{dc} is compared with its reference value u^{*}_{dc} and the error signal is used to produce a reference DC current signal i^{*}_{v} according to

$$i^{*}_{v} = -k_{pdc} \cdot \left(1 + \frac{1}{sT_{idc}} \right) \left(u^{*}_{dc} - u_{dc} \right) \tag{8}$$

where k_{pdc}, T_{idc} are the proportional gain and integral time constant of the DC PI-controller respectively, and *s* is Laplace operator.

D. Generation of current references

Proper current references should be generated in order to minimize the DC ripple and decrease the AC current

magnitude and harmonics content. Consider the apparent power from the grid

$$\underline{S}_g = \left(\underline{e}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{e}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)\cdot\left(\underline{i}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{i}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)^{conj} \quad (9)$$

which is the sum of a constant apparent power and two terms in sine and cosine, oscillating with double the grid frequency. By expanding Eq.(9), the following expression in matrix form can be written

$$\begin{bmatrix} P_g \\ Q_g \\ P_{s2g} \\ P_{c2g} \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \cdot \begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} \quad (10)$$

where P_g and Q_g are the constant active and reactive power, respectively, while P_{s2g} and P_{c2g} represent the second-harmonic sine and cosine component of the active power. These are the oscillating powers due to the unbalance in the grid voltages.

The apparent power at the converter terminals is

$$\underline{S}_{ac} = \left(\underline{u}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{u}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)\cdot\left(\underline{i}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{i}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)^{conj} \quad (11)$$

and the following expression gives the power balance at the converter terminals

$$\underline{S}_{ac} = \underline{S}_g + \Delta\underline{S} \quad (12)$$

where ΔS is the apparent power dissipated in the filter. This contains also constant active and reactive power and two sine and cosine components oscillating with double the grid frequency. By substituting Eq.(12) in Eq.(11) and expressing the converter output voltages in terms of grid voltages by applying KVL, the following expressions for the active powers dissipated in the filter are obtained:

$$\Delta P = R\cdot\left(i_{dp}^2 + i_{qp}^2 + i_{dn}^2 + i_{qn}^2\right) \quad (13)$$

$$\Delta P_{c2} = 2R\left(i_{dp}\cdot i_{dn} + i_{qp}\cdot i_{qn}\right) + 2\omega L\left(i_{dp}\cdot i_{qn} - i_{qp}\cdot i_{dn}\right) \quad (14)$$

$$\Delta P_{s2} = 2R\left(i_{dp}\cdot i_{qn} - i_{qp}\cdot i_{dn}\right) + 2\omega L\left(-i_{dp}\cdot i_{dn} - i_{qp}\cdot i_{qn}\right) \quad (15)$$

where ΔP is the constant term of the active power dissipated in the filter, while ΔP_{c2} and ΔP_{s2} are the cosine and sine oscillating components of the active power, respectively. The current references are then calculated by nullifying Q_g, to achieve average unity power factor. The converter losses are neglected, so that $P_{ac} = P_{dc}$ which is the DC-link power.

Two different methods are used here for considering the oscillating powers. In the first case (Case I), the DC side of the converter supplies the oscillating power to the filter, which means that the oscillating power is set to zero on the grid side, i.e. $P_{c2g} = P_{s2g} = 0$. The reference currents from Eq.(10) can thus be expressed as:

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (16)$$

In the second case (Case II), the oscillating powers flow from the grid into the filter, i.e. the oscillating powers are forced to zero at the converter terminals, $P_{c2g} = -\Delta P_{c2}$ and $P_{s2g} = -\Delta P_{s2}$. The reference currents for the DVCC are

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ 0 \\ -\Delta P_{s2} \\ -\Delta P_{c2} \end{bmatrix} \quad (17)$$

In both Eq.(16) and Eq.(17), the filter powers are non-linear combinations of the grid currents. This can be solved on line with mathematical iterative methods as done in [3]. However, this will make the controller quite complex and increase the calculation time. Here, the actual values of the grid currents sampled one time step back are used.

IV. Simulation Results

To test the controller, simulations have been run with all six unbalanced dip types mentioned previously and with magnitudes varying from 0.1 pu to 0.9 pu in steps of 0.1 pu using Matlab/Simulink for the two algorithms mentioned as case I and case II. System data and main controller data are shown in Table 2 and, respectively.

If only one VCC implemented in the *dqp*-frame is used, current harmonics appear during faults, as shown in Fig. 6 for a dip type C with magnitude 40%. This is due to the negative sequence component in the unbalanced grid voltage, which also causes ripple in the DC-link voltage, also shown in Fig. 6, equal to 6.5%. Separating the sequences and using the algorithm of case I to generate the current references smoothes out the currents, as shown in Fig. 7. However, the DC side supplies the oscillating powers and the DC ripple increases to 20%. With the oscillating powers supplied by the grid in case II, the DC voltage is significantly smoothed out, apart from the transients at the beginning and end of the dip, see Fig. 8. The currents are almost the same in magnitude in both cases, however they are more smoothed in case II.

TABLE 2
SYSTEM DATA

Constant	Symbol	Actual value	Value in pu
Nominal line AC voltage	E	400 V	1.0
Nominal phase current	I_n	100 A	1.0
Nominal grid frequency	f_n	50 Hz	
Nominal DC-link voltage	U_{dc}	650 V	1.0 (dc)
Nominal DC input current	I_{dc}	107 A	1.0 (dc)
Filter resistance	R	23 mΩ	0.01
Filter inductance	L	0.73 mH	0.1
DC link capacitance	C	550 µF	τ=1.7 ms

TABLE 3
MAIN CONTROLLER DATA

Constant	Symbol	Value
Sampling frequency	f_S	5 kHz
Sampling time	T_S	200 µs
Proportional gain (dead-beat)	K_P	$L/T_S + R/2 = 3.7$
Integration time constant	T_i	0.03 s

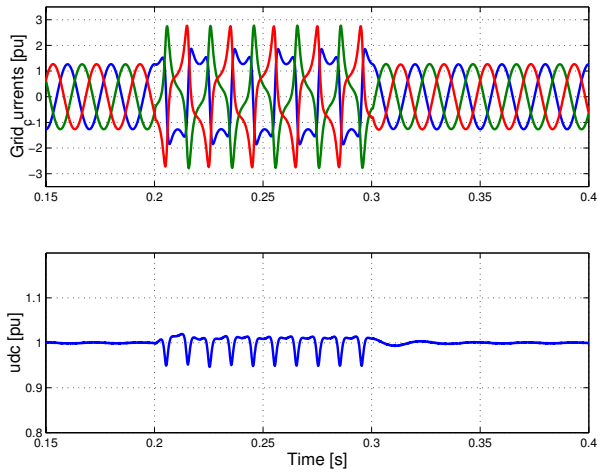

Fig. 6 Grid currents (top) and DC voltage (bottom) for 40% dip type C, with VCC.

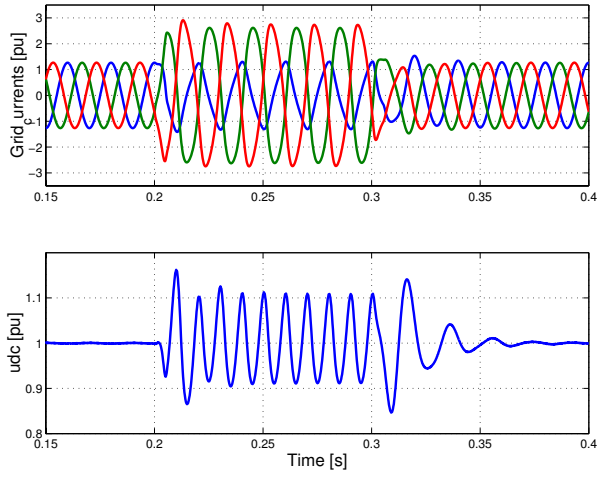

Fig. 7 Grid currents (top) and DC voltage (bottom) for 40% dip type C, with DVCC in case I.

The effect of all types of dips in both cases, with magnitude between 0.3 and 0.9 pu, on the maximum grid current and peak-to-peak DC-voltage ripple measured in the middle of the dip is represented in Fig. 9. The maximum current the valves should be able to hold is reduced in case II to 3.65 pu. The maximum DC voltage ripple is about ± 1.6 V around the nominal value. The maximum DC voltage ripple during the transient for all dips is less than 1.1 pu for case II, compared to about 1.13 pu in case I. The required rating of the converter is reduced in case II and also the performance of the system is improved.

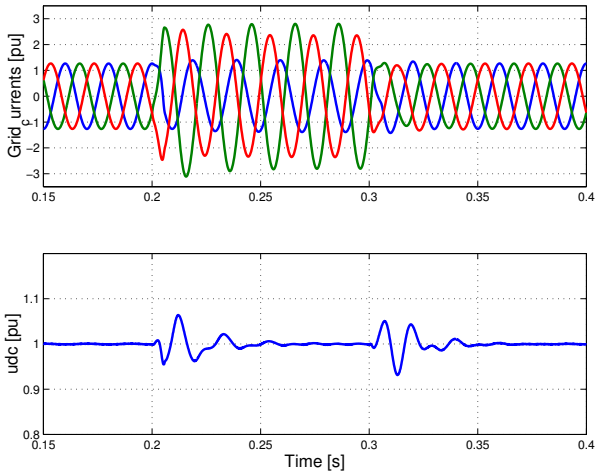

Fig. 8 Grid currents (top) and DC voltage (bottom) for 40% dip type C, with DVCC in case II.

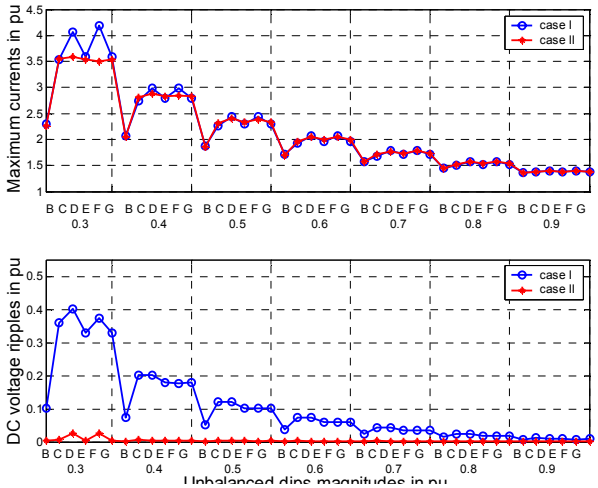

Fig. 9 Maximum grid current (top) and DC voltage ripple (bottom) in pu for different unbalanced dip types and magnitudes between 0.3 and 0.9 for case I (circle marked) and case II (asterisk marked).

V. EFFECT OF PHASE ANGLE JUMP

The system is further examined considering the phase angle jump. Four values of the impedance angles α specified in [6], which are 10°, 0, −20° and −60°, are used in the simulations. For 40% dip type C, Fig. 10 show that changing the phase angle jump has a negligible effect on the DC-voltage ripples. The effect of various phase angle jumps for the different unbalanced dip types and different impedance angles has been simulated and shown in Fig. 11. The dip magnitude increases for each dip type going from left to right. The phase angle jump appears to have more effect on the maximum grid currents in case of smaller dip magnitudes There is practically no difference for α = 0°, +10°, or −20°, but a significant increase in current occurs when α equals −60°. In that case the maximum current, with 30% magnitude of dip type D, is equal to 4.5 pu. This is significantly higher than in case of zero phase-angle jump (3.65 pu). If the converter switches are designed for a minimum dip magnitude considering the case of zero phase angle jump, they will be damaged if the same dip with a significant phase angle jump occurs.

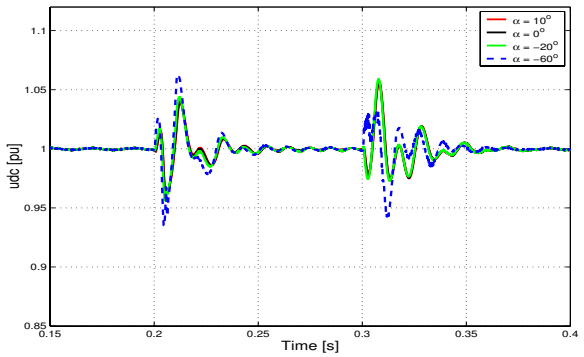

Fig. 10 DC ripple in pu for a 40% dip types C, $\alpha = 10^o, 0^o, -20^o, -60^o$.

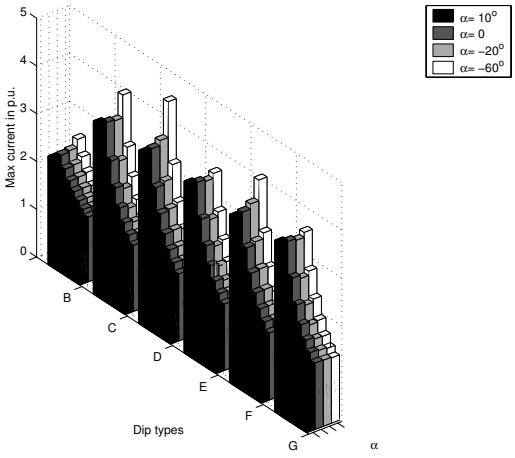

Fig. 11 Effect of phase angle jump on amplitude of phase currents for different unbalanced dips each from 30% to 90% dip magnitude.

VI. Conclusion

In this paper, the transient performance of a voltage source converter subject to unbalanced voltage dips has been treated. The Dual Vector Current Controller (DVCC) has been implemented and tested exhaustively through simulations of all voltage dips that can occur at the converter terminals.

Two methods for generation of the current references have been implemented and compared, in which the instantaneous active and reactive powers are controlled at the grid side and the converter terminals, respectively. In the latter case, it has been shown that the grid currents are slightly decreased and the DC voltage is significantly smoothed out.

Dips with significant phase angle jumps, corresponding to an impedance angle $\alpha = -60^o$, are characterized by an increase of maximum grid currents and DC-link voltage ripple, and this effect is more significant at lower dip magnitudes. This effect should be taken into account when designing converters with high ride-through capability for voltage dips.

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Paper C

F. Magueed, J. Svensson, and A. Sannino, "Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage conditions," in *Proc of Power Tech Conference (PT'05)*, St. Petersburg, Russia, June 27-30, 2005.

Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage Conditions

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***Abstract*-- Grid-connected voltage source converters (VSC's) are used in many applications with power quality concerns due to good controllability and output power quality. However, the major drawback is their sensitivity to grid disturbances, e.g. voltage dips. Moreover, when VSCs are used in distributed generation (DG) applications, voltage imbalance may be intolerant. The VSC may trip due to current imbalance or due to overcurrent. In this paper, dual vector current controller is adopted for the VSC connected to the grid through LCL-filter to achieve sinusoidal grid currents with no harmonics and smooth DC-link voltage during voltage dips. The LCL-filter resonance is damped by adjusting the controller gain. Proper current references are generated using a signal command from the DC-link voltage controller and compensates for oscillating powers produced in fault cases. The controller is examined for all types of unbalanced dips.**

***Index Terms*-- DG, LCL-filter, power quality, VSC, vector current control, voltage dips.**

I. Introduction

Integration of Distributed Generation (DG) in the utility grid offers a number of technical, environmental and economical benefits, both from the utility and the end-user point of view ([1], [2], and [3]), and is therefore becoming more and more popular. In variable-speed wind turbines, like many other DG technologies, a power-electronic interface is used to connect the DG system to the utility grid. This power electronics interface usually comprises a current-controlled voltage source converter (VSC), which has the advantages of good controllability (controls active and reactive power independently) and power quality (no low-frequency harmonics). The grid-connected VSC is used to control the active power flow to the grid by keeping the DC-link voltage constant independently of the operation of the generation part of the DG. This is done by using a cascade controller, where the outer-loop controller tracks the DC-link voltage reference and sets the reference current to the inner vector-current controller, which controls the instantaneous active and reactive current.

The drawback of using VSCs is their sensitivity to voltage disturbances, e.g. voltage dips. A voltage dip is a short duration drop in voltage that is normally due to a fault [4]. For a VSC, a sudden decrease in grid voltage normally causes an increase in current, as the control attempts at maintaining the power to the DC link constant. This can lead to tripping of the VSC because of over-current, in order to protect the valves. Moreover, most faults are unbalanced and result in unbalanced dips, which produce undesirable power oscillations of low-order frequencies resulting in current harmonics and poor DC-link voltage regulation [5]. Ultimately, this can also lead to tripping of the VSC due to DC over-voltage. When a large amount of DGs are installed in the grid it becomes unacceptable to disconnect generating units every time a disturbance occurs. Hence, a robust controller should be developed to enhance the transient performance of a DG.

In references [4], [5], and [6] investigations have been carried out in order to improve the controllability of the VSC connected to the grid through L-filter for unbalanced voltages of the grid. Dual vector current controller (DVCC) has proved to perform adequately concerning the grid current. An advanced DC-link voltage controller has been introduced in order to reduce the voltage ripple on the DC-link when running the VSC on unbalanced grids.

However, to eliminate the grid current harmonics an LCL-filter is inserted between the grid and the VSC due to its higher attenuation ability of current harmonics at higher frequencies compared with the L-filter. Implementing LCL- filter may lead to instability problem that could occur at the resonance frequency of the filter. Damping methods are extensively addressed in literature [7]-[12], where the high gain at the resonance frequency of the filter is either passively or actively damped. In passive damping method, a resistor is connected in series with the filter capacitor. Although this method is easy to implement, it increases the system losses and decreases the efficiency of the filter. Instead, methods to actively damp the resonance are adopted ([8], [11] and [12]), which increases the control system complexity.

In this paper, the DVCC is adopted for the VSC connected to the grid through LCL-filter to achieve sinusoidal grid currents with no harmonics and smooth DC-link voltage during different voltage dips. The LCL-filter resonance is damped by

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adjusting the cascaded controller gains. Proper current references are generated using a signal command from a DC-link voltage controller and compensating for the oscillating powers produced in fault cases. The controller is examined for all types of unbalanced dips.

II. System Description

A scheme of the investigated system using VSC with LCL-filter is shown in Fig. 1. The generating part of the DG is modeled by a constant DC current source, while the DC voltage across the capacitor is regulated. The system data are shown in Table 1 and the filter parameters are shown in Table 2.

The grid currents and voltages, the VSC currents, the capacitor voltages and the DC-link voltage are measured and fed into the cascaded controller. The outer controller (PI1) tracks the reference current of the grid i_2^* and the output is the reference capacitor voltage u_c^*, which is the reference for the second controller (P2). In P2 the measured capacitor voltage u_c is compared with the reference command using a proportional controller, which produces the reference current i_1^* for the third controller (P3). The third controller is also a proportional controller, which output is the reference voltage u^* to the PWM-block to generate the proper switching pattern (SW_{123}) necessary for the operation of the VSC.

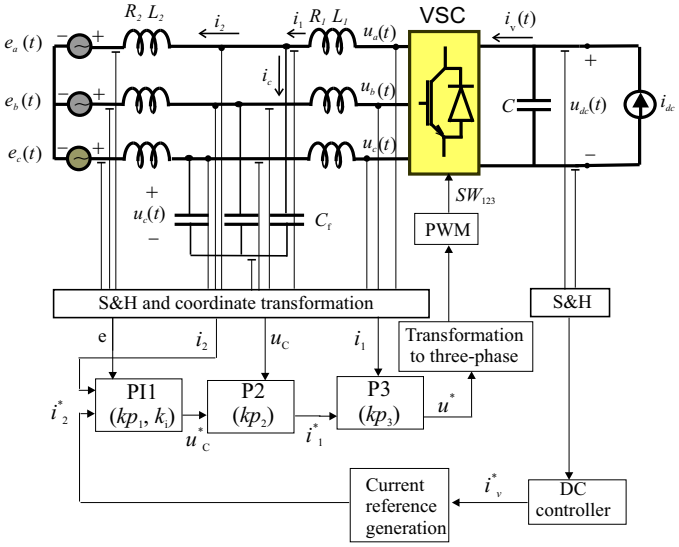

Fig. 1 Investigated system schematic diagram.

The controller equations in *dq*-frame, which is synchronized with the grid voltage by a PLL, are derived. A time delay of one sample is considered in the inner controller (P3) to model the inherited time delay resulting from the calculation time in practical systems and an integral part is used in the outer controller (PI1) to eliminate steady-state error.

TABLE 1
SYSTEM DATA

Description	Symbol	Value
Nominal (base) rms phase-to-phase AC voltage	E	400 V
Nominal (base) rms phase current	I_n	100 A
Nominal (base) grid frequency	f_n	50 Hz
Nominal (base) DC link voltage	U_{dc}	650 V
Nominal (base) DC input current	I_{dc}	107 A
DC link capacitance	C	550 µF

TABLE 2
FILTER PARAMETERS

Description	Parameter	Value
VSC-side inductance	L_1	0.52 mH
VSC-side resistance	R_1	1.6 mΩ
Grid-side inductance	L_2	0.2 mH
Grid-side resistance	R_2	0.6 mΩ
Filter capacitance	C_f	137.83 µF

The controller equations are:

$$\underline{u}_{cdq}^*(k) = \underline{e}_{dq}(k) + (R_2 + j\omega L_2)\underline{i}_{2dq}(k) + kp_1\left(\underline{i}_{2dq}^*(k) - \underline{i}_{2dq}(k)\right) + \underline{\Delta u}_{idq}(k) \quad (1)$$

$$\underline{i}_{1dq}^*(k) = \underline{i}_{2dq}(k) + j\omega C_f \underline{u}_{cdq}(k) + kp_2\left(\underline{u}_{cdq}^*(k) - \underline{u}_{cdq}(k)\right) \quad (2)$$

$$\underline{u}_{dq}^*(k+1) = \underline{u}_{cdq}(k) + (R_1 + j\omega L_1)\underline{i}_{1dq}(k) + kp_3\left(\underline{i}_{1dq}^*(k) - \hat{\underline{i}}_{1dq}(k)\right) \quad (3)$$

where $\underline{e}_{dq}$ is the grid voltage vector, kp_1, kp_2, and kp_3 are the controller proportional gains that are fractions of the corresponding dead-beat gains, k_{DB1}, k_{DB2}, and k_{DB3}, as explained by the following equations:

$$kp_1 = k_1 k_{DB1} = k_1\left(\frac{L_2}{T_s} + \frac{R_2}{2}\right)$$
$$kp_2 = k_2 k_{DB2} = k_2\left(\frac{C_f}{T_s}\right) \quad (4)$$
$$kp_3 = k_3 k_{DB3} = k_3\left(\frac{L_1}{T_s} + \frac{R_1}{2}\right)$$

where T_s is the sampling time. The integral part is calculated as:

$$\underline{\Delta u}_{idq}(k+1) = \underline{\Delta u}_{idq}(k) + k_i\left(\underline{i}_{2dq}^*(k-1) - \underline{i}_{2dq}(k)\right) \quad (5)$$

where k_i is the integrator gain.

Predicting the VSC current one sample ahead instead of

using the delayed measured current in P3 compensates for the time delay. The predicted current equation is:

$$\hat{\underline{i}}_{1dq}(k+1)=\frac{T_s}{L_1}\left(\underline{u}^*_{dq}(k)-\underline{u}_{cdq}(k)\right)+\left(1-\frac{R_1}{L_1}-j\omega T_s\right)\hat{\underline{i}}_{1dq}(k)$$
$$+kp_s\left(\underline{i}_{1dq}(k)-\hat{\underline{i}}_{1dq}(k-1)\right) \quad (6)$$

where kp_s is a proportional gain that compensates for the error between the actual and the estimated current.

Theoretically, choosing dead-beat gains for the controller should result in fast transient response. However, this is not possible in cascaded controllers, since the operation of the controllers should be decoupled. In another sense, the voltage reference (output of P3) is not modified after one sample and then the actual grid current is not able to follow its reference within one sample. To choose the proper gains, the stability of the complete system has been examined looking at the pole locations on the unit disc, shown in Fig. 2. The two poles near the upper bound of the unit disc (and their conjugates at the lower bound) are fast moving poles depending on the gain of P3. They move into the unit disc as kp_3 takes values less than 30% of the dead-beat gain. However, increased values of kp_3 decrease the peak value in the gain from grid voltage to grid-side current (i_{2d}/e_d in Fig. 3) insuring proper transient response at high frequencies. Hence, a trade-off should be considered to choose the controller gains. The transient response for the controller, using the gains that are reported in Table 3, is shown in Fig. 4. The settling time in i_{2d} is about 0.02 s for a step in the active component of the reference current i^*_{2d}, while it is about 0.015 s for a step in the active component of the grid voltage e_d. Moreover, the effect of a step in i^*_{2d} over i_{2q}, which is called the cross-coupling effect, is negligible.

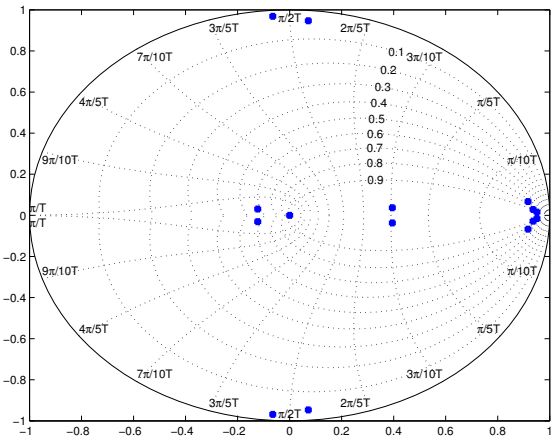

Fig. 2 System poles.

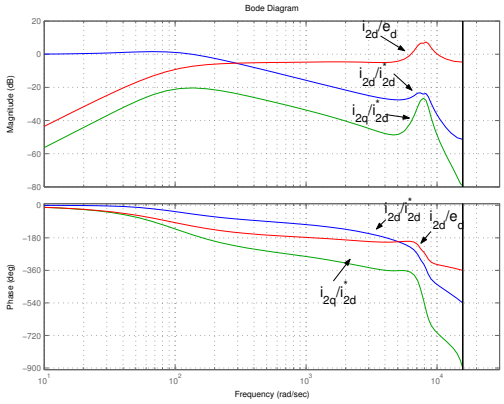

Fig. 3 Bode plot for the controller.

TABLE 3
CONTROLLER PARAMETERS

kp_1	k_{DB1}	kp_s	0.5
T_i	10 ms	f_s	5 kHz
kp_2	k_{DB2}	k_{pdc}	0.2
kp_3	$0.2k_{DB3}$	T_{idc}	5 ms

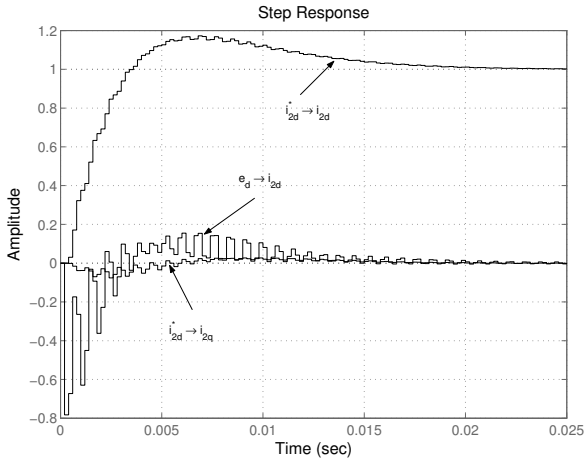

Fig. 4 Transient response for the controller.

III. VOLTAGE DIPS

A voltage dip is the voltage experienced at the end user terminals due to a short-circuit fault at a certain point in the electrical network. It can also happen due to motor starting or overloads. In spite of their short duration, between one cycle and several seconds, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [13], [14].

The voltage dip classification defined by Bollen [20] and reported in Fig.5 has been used in this paper to quantify the unbalanced voltage dips at the VSC bus. The magnitude, indicated as E_{dip} or V_{dip}, is equal to the retained voltage for a single-phase dip. For a three-phase dip, the expressions of the three phase voltages for a given dip magnitude and type are given in [20]. Due to a fault at bus 3 in Fig. 6, a voltage dip

occurs at bus 1, which can be balanced (due to a three-phase fault, and called type A), or of any of the six unbalanced types in Fig.5. According to the transformer (TR) type, the dip that occurs at bus 1 may change from one type to another, as seen by the VSC connected at bus 2. This transformer can be: Type 1, which does not change anything to voltages (e.g. star grounded/star grounded); Type 2, which removes the zero-sequence voltage (e.g. Y/Y with at least one side not grounded or D/Z); Type 3, which swaps line and phase voltages (e.g. D/Y, Y/D, Y/Z). The transformation from one type to another is listed in Table 4. Since distribution transformers are often D/Y (Type 3), we normally find five types at the equipment terminals: Type A, due to three-phase faults; Type C and D, due to single-phase and double-phase faults; Type F and G, due to double-phase to ground faults. Note, however, that the load can in principle be subjected to dips of type B and E if the fault occurs at the same voltage level as the load or if the transformer is type 1.

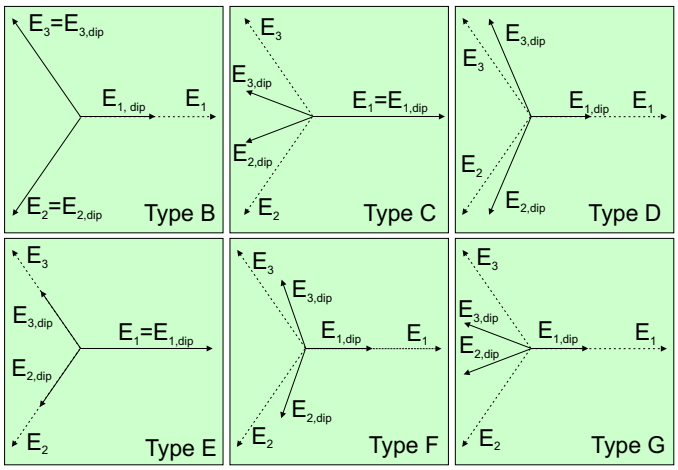

Fig.5. Voltage dip classification from B to G. Phasors of three phase voltage before (dotted) and during fault (solid) are displayed.

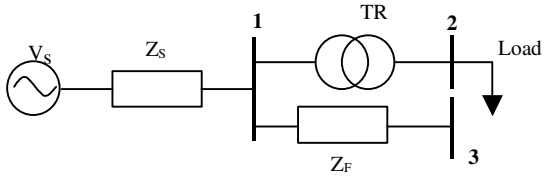

Fig. 6 One-line model for dip analysis.

TABLE 4
TRANSFORMATION OF VOLTAGE DIPS THROUGH TR

	Dip on the primary side						
Dip type	A	B	C	D	E	F	G
TRF type1	A	B	C	D	E	F	G
TRF type2	A	D*	C	D	G	F	G
TRF type3	A	C*	D	C	F	G	F

The superscript * indicates that the dip magnitude is equal to $\frac{1}{3}+\frac{2}{3}V_{dip}$.

IV. PERFORMANCE DURING UNBALANCED VOLTAGE DIPS

To examine the performance of the controller in case of unbalanced voltage dips on the grid side, proper current references should be generated. The active current reference should be produced in such a way to keep the DC-link voltage constant. Hence, the current reference generation block in Fig. 1 is commanded using the output signal of the DC-link voltage controller.

A. DC-link voltage controller

In many applications, e.g. drive systems and variable-speed wind turbines, the DC-link voltage cannot be considered constant. However, it should be regulated to insure correct operation of the VSC and to avoid damage to the power electronic switches and DC-link capacitor. Also the current to the DC-link is not constant. But its variations can be assumed to be much slower than the time range of the transient phenomena considered here. Therefore the DC-link is modeled as a capacitor with a current source in parallel.

A simple PI-controller is implemented, where the measured DC capacitor voltage u_{dc} is compared with its reference value u_{dc}^{*} and the error signal is used to produce a reference DC current signal i_{v}^{*} according to

$$i_{\mathrm{v}}^{*}=-k_{\mathrm{pdc}}\cdot\left(1+\frac{1}{sT_{\mathrm{idc}}}\right)\left(u_{\mathrm{dc}}^{*}-u_{\mathrm{dc}}\right) \tag{7}$$

where k_{pdc}, T_{idc} are the proportional gain and integral time constant of the DC PI-controller respectively, and s is Laplace operator.

B. Current reference generation

The current references are then generated to keep power balance through the system, neglecting the power loss in VSC switches. The power at the VSC side is:

$$S_1=\underline{u}_{\mathrm{dq}}\underline{i}_{\mathrm{1dq}}^{\mathrm{conj}} \tag{8}$$

which is expanded as follows:

$$S_1=u_{\mathrm{d}}i_{\mathrm{1d}}+u_{\mathrm{q}}i_{\mathrm{1q}}+\mathrm{j}\left(u_{\mathrm{q}}i_{\mathrm{1d}}-u_{\mathrm{d}}i_{\mathrm{1q}}\right) \tag{9}$$

Applying KVL and KCL, we get:

$$\underline{u}_{\mathrm{dq}}=\underline{e}_{\mathrm{dq}}+R_1\underline{i}_{\mathrm{1dq}}+\mathrm{j}\omega L_1\underline{i}_{\mathrm{1dq}}+R_2\underline{i}_{\mathrm{2dq}}+\mathrm{j}\omega L_2\underline{i}_{\mathrm{2dq}} \tag{10}$$

$$\underline{i}_{\mathrm{1dq}}=\underline{i}_{\mathrm{2dq}}+\mathrm{j}\omega C_{\mathrm{f}}\underline{u}_{\mathrm{cdq}} \tag{11}$$

Substituting in (9) and expressing the equation in matrix form:

$$\begin{bmatrix}P_1\\Q_1\end{bmatrix}=\begin{bmatrix}e_{\mathrm{d}} & e_{\mathrm{q}}\\ e_{\mathrm{q}} & -e_{\mathrm{d}}\end{bmatrix}\begin{bmatrix}i_{\mathrm{2d}}\\ i_{\mathrm{2q}}\end{bmatrix}+\begin{bmatrix}\Delta P(i)\\ \Delta Q(i)\end{bmatrix}+\begin{bmatrix}\Delta P(e)\\ \Delta Q(e)\end{bmatrix}$$

where, P_1 and Q_1 are active and reactive powers at the VSC

side, $\Delta P(i)$ and $\Delta Q(i)$ are active and reactive powers consumed in the filter inductors and expressed as functions in grid-current and VSC-current, and $\Delta P(e)$ and $\Delta Q(e)$ are active and reactive powers consumed by the filter capacitor and expressed as function in the grid voltage.

To achieve zero reactive power at the grid, Q_1 should supply the reactive power consumed by the filter. In equation:

$$Q_1 = \Delta Q(i) + \Delta Q_c \tag{12}$$

where ΔQ_c is the power loss in the filter capacitor, it is calculated as:

$$\Delta Q_c = \omega C_f \left(u_{cd}^2 + u_{cq}^2\right) \tag{13}$$

Moreover, neglecting the switching losses, the active power at the VSC side is considered equal to the power at the DC side. The current references are then generated as:

$$\begin{bmatrix} i_{2d}^* \\ i_{2q}^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} u_{dc} i_v^* - \Delta P(i) \\ \Delta Q_c \end{bmatrix} - \begin{bmatrix} -\omega C_f u_{cq} \\ \omega C_f u_{cd} \end{bmatrix} \tag{14}$$

where

$$\begin{aligned} \Delta P(i) = {} & R_1 \left(i_{1d}^2 + i_{1q}^2\right) + R_2 \left(i_{1d} i_{2d} + i_{1q} i_{2q}\right) \\ & + \omega L_2 \left(-i_{1d} i_{2q} + i_{1q} i_{2d}\right) \end{aligned} \tag{15}$$

C. Performance

The controller that has been described above has been examined in case of unbalanced voltage dips. A dip, resulting from two-phase fault (dip type C), is applied at the grid side. The dip starts at 0.2 s for duration of 0.1s with a remaining voltage of 40%. The grid currents are distorted during the dip, as shown in Fig. 7, and the DC-link voltage contains about 20% peak-to-peak ripples.

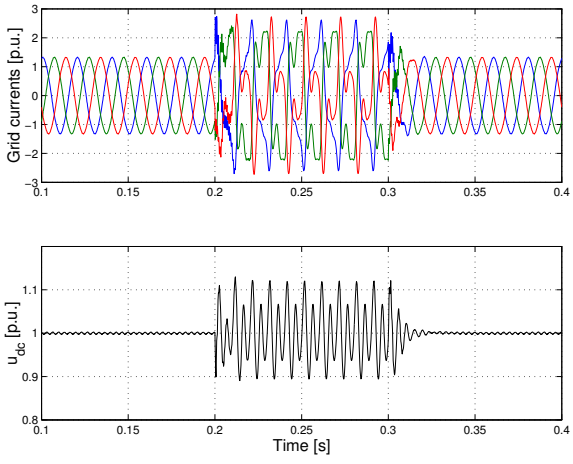

Fig. 7 Grid currents (upper) and DC-link voltage (lower) in case of voltage dip.

V. Dual Vector Current Controller (DVCC)

To improve the transient response during voltage dips, DVCC is implemented. It consists of two separate controllers for controlling the positive and negative sequences.

The decomposition of the supply voltage (and all measured signals) into positive and negative-sequence is performed in the *dq*-frame synchronized with the positive sequence (indicated as *dqp*), with the technique proposed in [21]. By delaying the *dq*-vector of the measured supply voltage by one fourth of the period T at the fundamental frequency, a vector composed of the same positive sequence component and a negative sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative sequence voltage will be removed. The positive sequence voltage component can thus be extracted from the measured values as

$$\underline{e}_{dqp} = \frac{1}{2}\left(\underline{e}_{dq}(t) + \underline{e}_{dq}\left(t - \frac{T}{4}\right)\right) \tag{16}$$

The negative sequence can be calculated as

$$\underline{e}_{dqn} = \frac{1}{2}\left(\underline{e}_{dq}(t) - \underline{e}_{dq}\left(t - \frac{T}{4}\right)\right) \tag{17}$$

The latter will be seen as a constant signal in the negative rotating plane *dqn*, which utilizes the opposite angle for the *dq*-transformation.

Equations (1) to (3) are then expressed in the positive sequence frame (*dqp*-frame) and negative sequence frame (*dqn*-frame) as follows:

$$\begin{aligned} \underline{u}_{cdqp}^*(k) = {} & \underline{e}_{dqp}(k) + (R_2 + j\omega L_2)\underline{i}_{2dqp}(k) \\ & + kp_1\left(\underline{i}_{2dqp}^*(k) - \underline{i}_{2dqp}(k)\right) + \underline{\Delta u}_{idqp}(k) \end{aligned} \tag{18}$$

$$\begin{aligned} \underline{u}_{cdqn}^*(k) = {} & \underline{e}_{dqn}(k) + (R_2 - j\omega L_2)\underline{i}_{2dqn}(k) \\ & + kp_1\left(\underline{i}_{2dqn}^*(k) - \underline{i}_{2dqn}(k)\right) + \underline{\Delta u}_{idqn}(k) \end{aligned} \tag{19}$$

$$\begin{aligned} \underline{i}_{1dqp}^*(k) = {} & \underline{i}_{2dqp}(k) + j\omega C_f \underline{u}_{cdqp}(k) \\ & + kp_2\left(\underline{u}_{cdqp}^*(k) - \underline{u}_{cdqp}(k)\right) \end{aligned} \tag{20}$$

$$\begin{aligned} \underline{i}_{1dqn}^*(k) = {} & \underline{i}_{2dqn}(k) - j\omega C_f \underline{u}_{cdqn}(k) \\ & + kp_2\left(\underline{u}_{cdqn}^*(k) - \underline{u}_{cdqn}(k)\right) \end{aligned} \tag{21}$$

$$\begin{aligned} \underline{u}_{dqp}^*(k+1) = {} & \underline{u}_{cdqp}(k) + (R_1 + j\omega L_1)\underline{i}_{1dqp}(k) \\ & + kp_3\left(\underline{i}_{1dqp}^*(k) - \hat{\underline{i}}_{1dqp}(k)\right) \end{aligned} \tag{22}$$

$$\underline{u}^{*}_{\mathrm{dqn}}(k+1)=\underline{u}_{\mathrm{cdqn}}(k)+(R_1-\mathrm{j}\omega L_1)\underline{i}_{\mathrm{1dqn}}(k)+kp_3\left(\underline{i}^{*}_{\mathrm{1dqn}}(k)-\underline{\hat{i}}_{\mathrm{1dqn}}(k)\right) \tag{23}$$

A. *Current reference generation*

The power at the VSC side is expressed as:

$$S_1=\left(e^{\mathrm{j}\omega t}\underline{u}_{\mathrm{dqp}}+e^{-\mathrm{j}\omega t}\underline{u}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{\mathrm{1dqp}}+e^{-\mathrm{j}\omega t}\underline{i}_{\mathrm{1dqn}}\right)^{\mathrm{conj}} \tag{24}$$

Expressing (10) and (11) in *dqp-* and *dqn-* frames, and substituting in (24) results in the following matrix to generate the current references:

$$\begin{bmatrix} i^{*}_{2\mathrm{dp}} \\ i^{*}_{2\mathrm{qp}} \\ i^{*}_{2\mathrm{dn}} \\ i^{*}_{2\mathrm{qn}} \end{bmatrix}=\begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qp}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1}\begin{bmatrix} u_{\mathrm{dc}}i^{*}_{\mathrm{v}}-\Delta P(i) \\ \Delta Q_{\mathrm{c}} \\ P_{\mathrm{s}2}-\Delta P_{\mathrm{s}2}(i) \\ P_{\mathrm{c}2}-\Delta P_{\mathrm{c}2}(i) \end{bmatrix}-Y_c\begin{bmatrix} -u_{\mathrm{cqp}} \\ u_{\mathrm{cdp}} \\ u_{\mathrm{cqn}} \\ -u_{\mathrm{cdn}} \end{bmatrix} \tag{25}$$

where $Y_{\mathrm{c}}=\omega C_{\mathrm{f}}$, $\Delta P(i)$ is the power consumed by the filter inductors that is read as:

$$\begin{aligned}\Delta P(i)=&R_1\left(i^2_{1dp}+i^2_{1qp}+i^2_{1dn}+i^2_{1qn}\right)\\&+R_2\left(i_{2dp}i_{1dp}+i_{2qp}i_{1qp}+i_{2dn}i_{1dn}+i_{2qn}i_{1qn}\right)\\&+\omega L_2\left(-i_{2qp}i_{1dp}+i_{2dp}i_{1qp}+i_{2qn}i_{1dn}-i_{2dn}i_{1qn}\right)\end{aligned} \tag{26}$$

$$, \Delta Q_{\mathrm{c}}=Y_{\mathrm{c}}\left(u^2_{\mathrm{cdp}}+u^2_{\mathrm{cqp}}+u^2_{\mathrm{cdn}}+u^2_{\mathrm{cqn}}\right) \tag{27}$$

, and $P_{\mathrm{s}2}$ and $P_{\mathrm{c}2}$ are sine and cosine components of the active power generated from the VSC at double the fundamental frequency (which is called the oscillating power) while $\Delta P_{\mathrm{s}2}$ and $\Delta P_{\mathrm{c}2}$ are the oscillating power consumed by the filter inductors and will be compensated by the power from the VSC side. Hence:

$$P_{\mathrm{s}2}=\Delta P_{\mathrm{s}2}(i) \tag{28}$$

$$P_{\mathrm{c}2}=\Delta P_{\mathrm{c}2}(i) \tag{29}$$

B. *Results*

An unbalanced voltage dip, resulting from two-phase fault (dip type C), is applied at the grid side. The dip starts at 0.2 s for duration of 0.1s with a remaining voltage of 40%. The resulting grid currents and DC-link voltage are shown in Fig. 8. The grid currents are sinusoidal during the voltage dip and the DC-link voltage is almost constant with no ripples. The transient at the start and end of the dip is mainly due to the delay in the sequence detection algorithm.

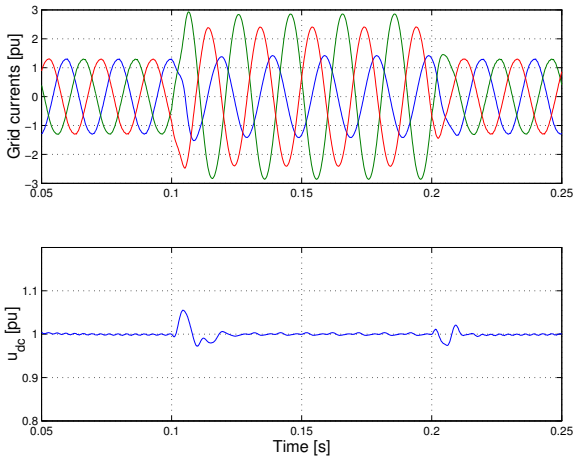

Fig. 8 Grid currents (upper) and DC-link voltage (lower) in case of voltage dip for DVCC.

All dips shown in Fig.5 are then tested. The instantaneous maximum current referred to the maximum of the nominal current and DC-link voltage peak-to-peak ripples referred to nominal DC voltage during the dip period are shown in Fig. 9 for all dips. For remaining voltage (V_{dip}) of 40% and higher, the maximum current that can occur is about 2 p.u. and maximum peak-to-peak DC ripples is about 0.05 p.u. (5% of nominal voltage).

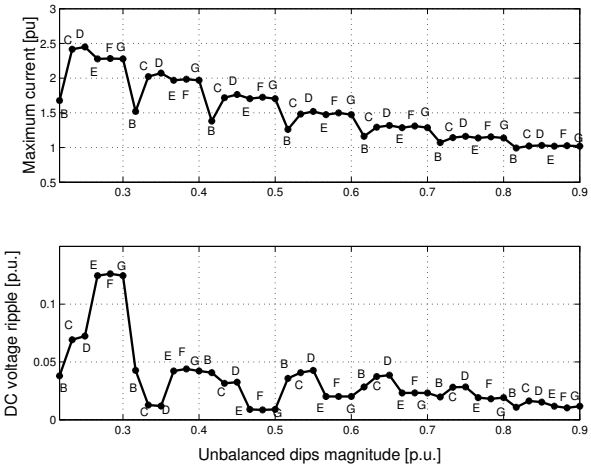

Fig. 9 Maximum grid current (upper), and DC-link voltage peak-to-peak ripples (lower) during different unbalanced dips.

VI. Conclusions

A dual vector current controller (DVCC) has been developed for the VSC connected to the grid through LCL-filter. The controller different gains have been adjusted to enhance the transient operation at higher frequencies. Proper current references are generated using a signal command from a DC-link voltage controller and compensating for the oscillating power produced in fault cases. The controller is examined and compared with a regular vector controller in

case of unbalanced voltage dips. It has proved to give better performance considering the grid current, which is sinusoidal, and DC-link voltage, which is smooth, during the dip period.

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VIII. BIOGRAPHIES

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Paper D

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Control of VSC connected to the grid through LCL-filter to achieve balanced currents

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Abstract— **Grid-connected voltage source converters (VSCs) are the heart of many applications with power quality concerns due to their reactive power controllability. However, the major drawback is their sensitivity to grid disturbances. Moreover, when VSCs are used in DG applications, voltage unbalance may be intolerant. The current protection may trip due to current unbalance or due to overcurrent. In this paper, a vector current controller for VSC connected to the grid through LCL-filter is developed with the main focus on producing symmetrical and balanced currents in case of unbalanced voltage dips. Implementing this controller helps the VSC system not to trip during voltage dips.**

Keywords- DG, LCL-filter, power quality, VSC, vector current control, voltage dips.

I. INTRODUCTION

Voltage source converters (VSCs) are now widely used in many grid-connected applications including STATCOMs, UPFCs, DVRs and as active interfaces for distributed generation (DG) systems (for instance photovoltaics, wind, fuel cells and microturbines). Benefits of using a VSC are sinusoidal grid currents and high controllability of both active and reactive power. To make the VSC operating towards the grid, an inductor is needed in each phase to limit and to control the currents. For DG systems, the output voltage of the grid-connected VSC needs often to be stepped up to the distribution level. Therefore, a step-up transformer should be used and the leakage inductance of the transformer will be equivalent to the needed series inductance. However, high frequency current harmonics are generated due to PWM switching of the VSC, which may affect the EMC sensitive loads connected to the same bus. The isolation of transformers is sensitive to high dv/dt. Therefore, the VSC voltages should be filtered. This can be done by inserting a reactor (inductor) towards the VSC and shunt-connected capacitors between the reactor and the transformer. Hence, LCL-filters are utilized to interface the VSC to the grid, which have the potential of improved grid current harmonics [1]-[4].

The major drawback of using VSC is its sensitivity to voltage disturbances, e.g. voltage dips. A voltage dip is a short duration drop in voltage that is normally due to a fault. For a VSC, a sudden decrease in grid voltage normally causes an increase in the current, as the control attempts at maintaining the power to the DC link constant. This can lead to tripping of the VSC because of overcurrent, in order to protect the IGBTs. Moreover, most faults are unbalanced and result in unbalanced voltage dips, which produce current harmonics and unbalance that also cause current protection to trip.

Many controllers have been developed to deal with grid voltage unbalance for a VSC system connected to the grid through L-filter [5] - [8]. In [9], LCL-filter is considered along with grid voltage unbalance. Moreover, a dual controller, that comprises one controller in the positive and one controller in the negative sequence frame, has been implemented. The reference negative sequence currents are set to zero. One case of voltage unbalance has been discussed showing the response only in the grid current.

In this paper, a vector current controller for VSC connected to the grid through LCL-filter is developed with the main focus on reducing current unbalance in case of different unbalanced voltage dips. The idea of implementing the controller in positive synchronous reference frame with feed-forward of negative voltage (first introduced in [7]) is adopted and modified for the system with LCL-filter. The performance of this controller is compared with a dual vector controller (DVC) regarding the VSC side current unbalance and the grid side current unbalance. This comparison is done by calculating the amount of unbalance, which is the ratio of negative sequence to positive sequence components, for each current and for different types of unbalanced voltage dips at the grid.

II. SYSTEM DESCRIPTION

A scheme of the investigated system is shown in Fig. 1. The VSC of rated power 69 kVA is connected to 400 V grid via LCL-filter, which has the parameters provided in Table I. The inductor on the grid side represents the leakage inductance of the transformer needed to match the grid requirement. Its inductance value is a ratio of the inductance at the VSC side. The ratio is higher than one in order to limit the high frequency harmonics in the VSC current. The choice of the LCL-filter parameters depends on the system rating. The criterion that is described in [4] and [10] has been used to choose the parameters. In this paper, the DC side has been assumed to have a constant DC voltage equal to 650 V. This assumption is reasonable if the DC capacitance C_{dc} is high [2].

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The LCL-filter is described in the instantaneous time domain and with single-phase notation, using KVL in the outer loop and KCL at the capacitor connection bus, as follows:

$$\frac{di_1}{dt} = \frac{-R_1}{L_1} i_1 - \frac{1}{L_1} u_c + \frac{1}{L_1} u \tag{1}$$

$$\frac{di_2}{dt} = \frac{-R_2}{L_2} i_2 + \frac{1}{L_2} u_c - \frac{1}{L_2} e \tag{2}$$

$$\frac{du_c}{dt} = \frac{1}{C_f} i_1 - \frac{1}{C_f} i_2 \tag{3}$$

where

i_1 is the phase current on the VSC side;
i_2 is the phase current on the grid side;
u_c is the capacitor phase voltage;
u is the VSC phase voltage;
e is the grid phase voltage.

Using the foregoing equations, the frequency response from the VSC voltage to the grid current is calculated and shown in Fig. 2. The figure shows that the LCL-filter has harmonic attenuation of 60 dB/decade at frequencies above the resonance peak equal to 1.1 kHz, thus eliminating the PWM switching current harmonics. The switching frequency is set to 2.5 kHz. The drawback of the LCL-filter is its peak gain at the resonance frequency, which implies an oscillatory behavior and consequently controller instability. Hence, this resonant peak should be damped actively within the controller.

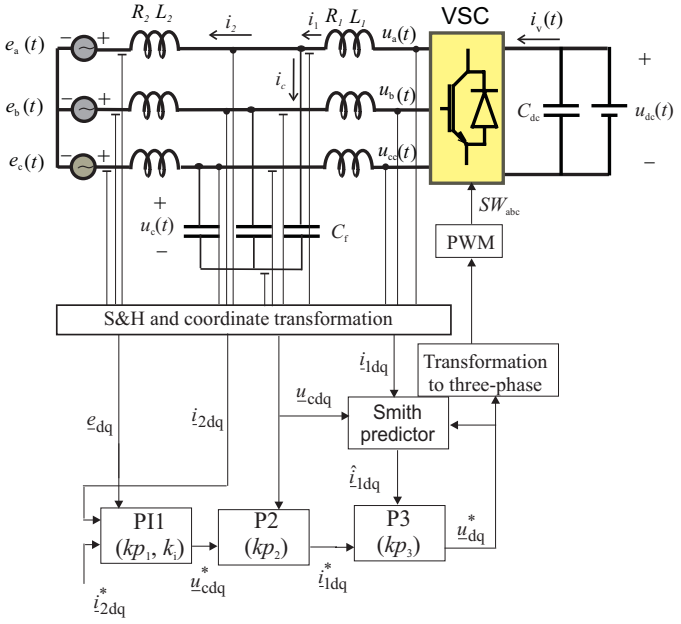

Figure 1. Power circuit along with main controller blocks.

TABLE I. LCL FILTER PARAMETERS (BASE IMPEDANCE IS ZBASE =2.3Ω).

Parameter	Description	pu
L_1	VSC side inductance	0.071
R_1	VSC side inductor resistance	0.1 L_1
L_2	Grid side inductance	0.027
R_2	Grid side inductor resistance	0.1 L_2
C_f	Filter capacitance	0.1

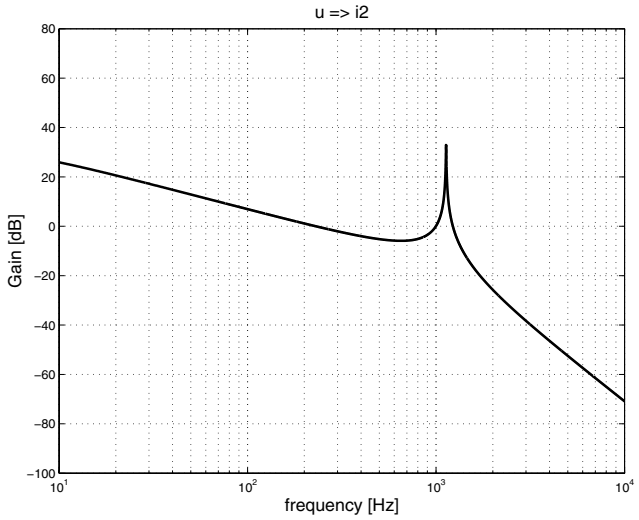

Figure 2. LCL-filter frequency response from VSC voltage to grid current.

III. CONTROLLER DESCRIPTION

A. Basic controller

The basic controller block diagram is shown in Fig. 1. The three-phase grid currents and voltages, VSC currents and voltages, and capacitor three phase voltages, are all measured and sampled with 5 kHz sampling frequency. All signals are then transformed into vectors in the fixed $\alpha\beta$-frame and then in the rotating dq-frame synchronized with the grid voltage. This is done by using the transformation angle θ obtained by using a PLL, which is assumed here to be slow and not to react on voltage dips. To increase the stability limits and in the same time damping oscillations at resonant frequency, three cascaded controllers are applied [13]. The outer controller (PI1) tracks the reference grid current vector $\underline{i}^*_{2dq}$ and the output is the reference capacitor voltage vector $\underline{u}^*_{cdq}$, which is the reference for the second controller (P2). In P2 the measured capacitor voltage vector $\underline{u}_{cdq}$ is compared with the reference command using a proportional controller, which produces the reference VSC current vector $\underline{i}^*_{1dq}$ for the third controller (P3). The third controller is also a proportional controller, which outputs the reference voltage vector $\underline{u}^*_{dq}$. The equations describing the cascaded controller in the dq-frame in the discrete time domain are:

$$\underline{u}^{*}_{\mathrm{cdq}}(k)=\underline{e}_{\mathrm{dq}}(k)+(R_2+\mathrm{j}\omega L_2)\underline{i}_{2\mathrm{dq}}(k)+k_{\mathrm{p1}}\left(\underline{i}^{*}_{2\mathrm{dq}}(k)-\underline{i}_{2\mathrm{dq}}(k)\right)+\underline{\Delta u}_{\mathrm{idq}}(k) \quad (4)$$

$$\underline{i}^{*}_{1\mathrm{dq}}(k)=\underline{i}_{2\mathrm{dq}}(k)+\mathrm{j}\omega C_{\mathrm{f}}\underline{u}_{\mathrm{cdq}}(k)+k_{\mathrm{p2}}\left(\underline{u}^{*}_{\mathrm{cdq}}(k)-\underline{u}_{\mathrm{cdq}}(k)\right) \quad (5)$$

where k is a sampling instant, $\underline{e}_{\mathrm{dq}}$ is the grid voltage vector in dq-frame, $\Delta\underline{u}_{\mathrm{idq}}$ is the integration part that eliminates steady state errors and finally ω is the angular frequency of the grid voltage. The integration part is calculated using the following equation:

$$\underline{\Delta u}_{\mathrm{idq}}(k+1)=\underline{\Delta u}_{\mathrm{idq}}(k)+k_{\mathrm{i}}\left(\underline{i}^{*}_{2\mathrm{dq}}(k)-\underline{i}_{2\mathrm{dq}}(k)\right) \quad (6)$$

where $k_{\mathrm{i}}=k_{\mathrm{p1}}T_{\mathrm{s}}/T_{\mathrm{i}}$, T_{i} and T_{s} are the integral time constant and the sampling time respectively. The reference voltage is then generated as:

$$\underline{u}^{*}_{\mathrm{dq}}(k+1)=\underline{u}_{\mathrm{cdq}}(k)+(R_1+\mathrm{j}\omega L_1)\underline{i}_{1\mathrm{dq}}(k)+k_{\mathrm{p3}}\left(\underline{i}^{*}_{1\mathrm{dq}}(k)-\underline{\hat{i}}_{1\mathrm{dq}}(k-1)\right) \quad (7)$$

The controller constants k_{p1}, k_{p2}, and k_{p3} are fractions of the corresponding dead-beat gains, k_{DB1}, k_{DB2}, and k_{DB3}, as

$$\begin{aligned}k_{\mathrm{p1}}&=k_1k_{\mathrm{DB1}}=k_1\left(\frac{L_2}{T_{\mathrm{s}}}+\frac{R_2}{2}\right)\\ k_{\mathrm{p2}}&=k_2k_{\mathrm{DB2}}=k_2\left(\frac{C_{\mathrm{f}}}{T_{\mathrm{s}}}\right)\\ k_{\mathrm{p3}}&=k_3k_{\mathrm{DB3}}=k_3\left(\frac{L_1}{T_{\mathrm{s}}}+\frac{R_1}{2}\right)\end{aligned} \quad (8)$$

To compensate for the time delay due to the calculation time, Smith predictor is used [14], which attempts to remove the effect of the delay time from the closed loop control system so that the controller can be designed as if no time delay was present. Hence, the Smith predictor is implemented in a way analogous to a state observer, which means running a model of the plant parallel to the plant itself. The predicted current equation is then calculated in the dq-frame as:

$$\hat{\underline{i}}_{1\mathrm{dq}}(k+1)=\frac{T_{\mathrm{s}}}{L_1}\left(\underline{u}^{*}_{\mathrm{dq}}(k)-\underline{u}_{\mathrm{cdq}}(k)\right)+\left(1-\frac{R_1}{L_1}-\mathrm{j}\omega T_{\mathrm{s}}\right)\hat{\underline{i}}_{1\mathrm{dq}}(k)+k_{\mathrm{ps}}\left(\underline{i}_{1\mathrm{dq}}(k)-\hat{\underline{i}}_{1\mathrm{dq}}(k-1)\right) \quad (9)$$

where k_{ps} is the observer gain that compensates for the error between the actual and the predicted currents.

Theoretically, choosing dead-beat gains for the controller should result in fast transient response. However, this is not possible in cascaded controllers, since the operation of the controllers should be decoupled. To choose the proper gains, the stability of the complete system has been examined looking at the pole location on the unit disc [13]. The controller parameters stated in Table II are chosen to produce an adequate response considering the overshoot, the rise time and the damping at the resonance frequency.

TABLE II. LCL-CONTROLLER PARAMETERS.

k_1	1
k_2	1
k_3	0.2
T_{i}	0.01 s
k_{ps}	0.07

B. Performance in case of grid voltage unbalance

To be able to analyze the grid voltage unbalance, the decomposition of the voltage vector into positive and negative-sequence is needed. This is performed in a *dqp*-frame with the technique proposed in [8], which originates from [15]. By delaying the voltage vector by one fourth of the grid cycle T, a vector composed of the same positive sequence component and a negative sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative sequence voltage will be removed. The positive sequence voltage component can, thus, be extracted from the measured values as

$$\underline{e}_{dqp}(t)=\tfrac{1}{2}\left(\underline{e}_{dq}(t)+\underline{e}_{dqp}(t-T/4)\right) \quad (10)$$

The negative sequence, in *dqp*-frame, can be calculated as

$$\underline{e}_{dqn(p)}(t)=\tfrac{1}{2}\left(\underline{e}_{dq}(t)-\underline{e}_{dqp}(t-T/4)\right) \quad (11)$$

The latter will be seen as a constant signal in the negative rotating plane *dqn*, which utilizes the opposite angle for the *dq*-transformation. This technique is applied to the current vectors as well, to be able to look at positive and negative sequence currents resulting due to the voltage imbalance.

The voltage imbalance due to unbalanced voltage dips is considered here. Three different dips are applied; one is due to a single phase fault, another is due to double phase fault, and the third is due to double phase to ground fault. The phasor diagram of voltage dips resulting from the three different faults is shown in Fig. 3. The dip magnitude E_{dip}, which is the magnitude of the remaining voltage during the dip, is chosen such that all dips have the same positive sequence component. The active current reference is chosen to be 1 pu while the reactive current reference is set to zero to produce unity power factor at the grid side. The resulting positive sequence current is shown in Fig. 4. This current is the same for all dips apart from the transients at the start and the end of the dip. This transient time is produced mainly due to the delay introduced by the sequence detection algorithm.

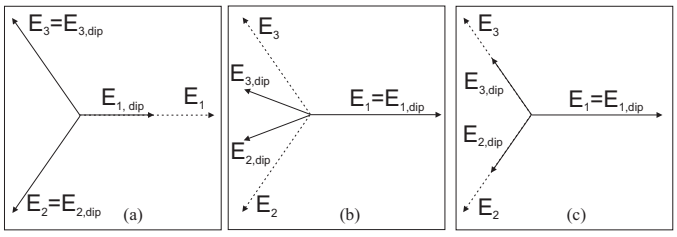

Figure 3. Voltage dips due to (a) single phase fault, (b) double phase fault, and (c) double phase to ground fault.

A dip due to a single phase fault with 10 % remaining voltage has been applied at 0.2 s for duration of 0.1 s, as shown in Fig. 5. The resulting negative sequence currents, on the VSC and grid sides, in *dq*-frame will be as shown in Fig. 6. The amount of imbalance, which is the ratio of negative sequence to positive sequence components at fundamental frequency [12], given by

$$r_i = \frac{\sqrt{i_{2\mathrm{dn}}^2 + i_{2\mathrm{qn}}^2}}{\sqrt{i_{2\mathrm{dp}}^2 + i_{2\mathrm{qp}}^2}} \times 100 \qquad (12)$$

is 132 % in this case. For a dip due to double phase fault with 40% remaining voltage, shown in Fig. 7, $r_i = 89$ %. In this case, the negative sequence currents are shown in Fig. 8. For the last case, which is a dip due to double phase to ground fault, $r_i = 69$ %. The voltage and negative sequence current are shown in Fig. 9 and Fig. 10, respectively.

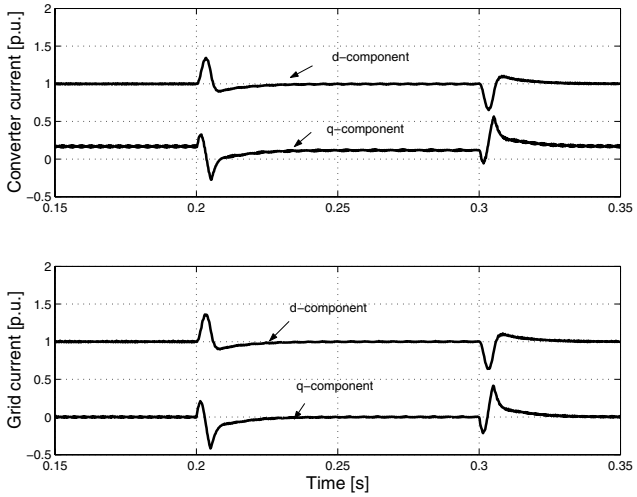

Figure 4. Positive sequence VSC current (upper) and grid current (lower) in *dq*-frame.

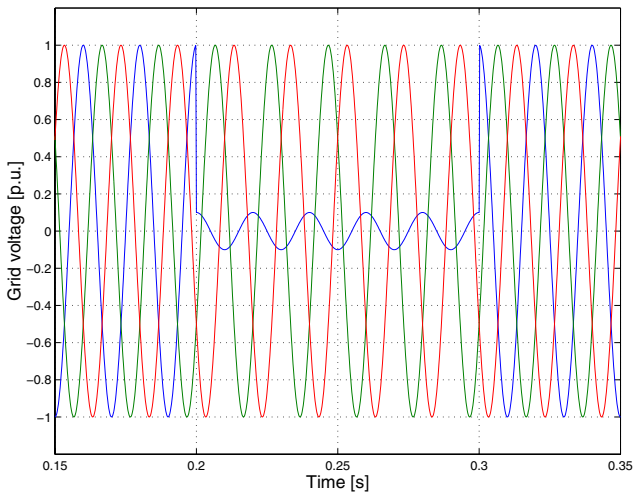

Figure 5. Grid voltage: 10 % voltage dip due to single phase fault.

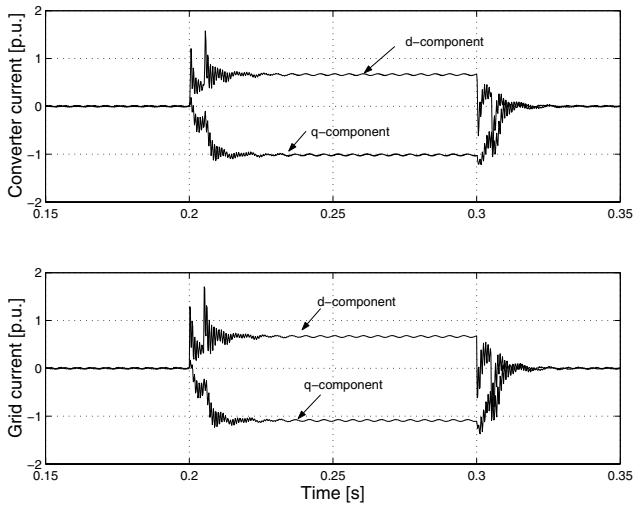

Figure 6. Negative sequence of VSC current (upper) and grid current (lower): 10 % voltage dip due to single phase fault.

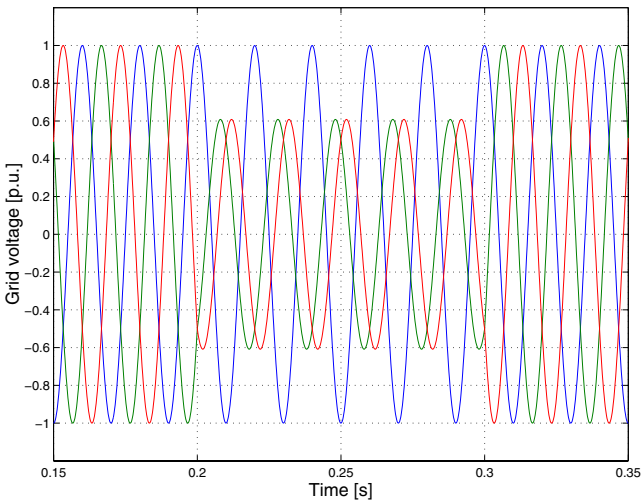

Figure 7. Grid voltage: 40 % voltage dip due to double phase fault.

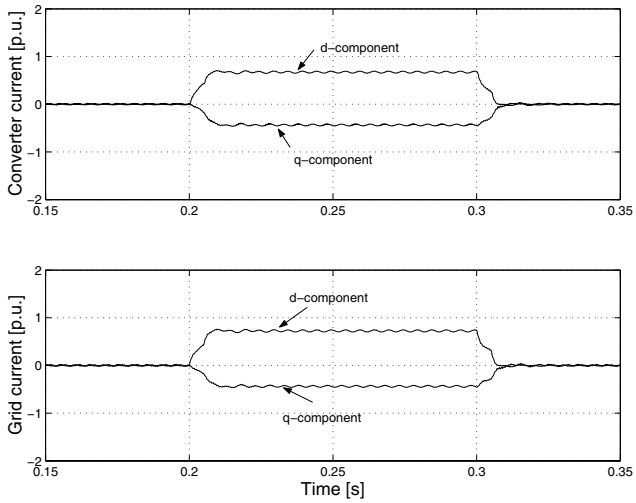

Figure 8. Negative sequence of VSC current (upper) and grid current (lower): 40 % voltage dip due to double phase fault.

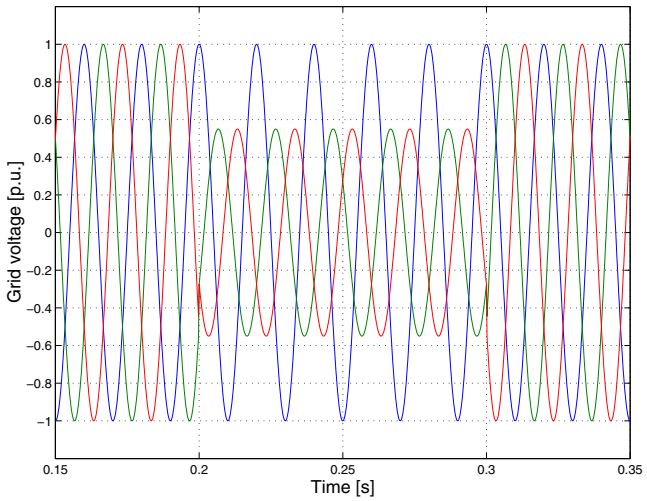

Figure 9. Grid voltage: 55 % voltage dip due to double phase to ground fault.

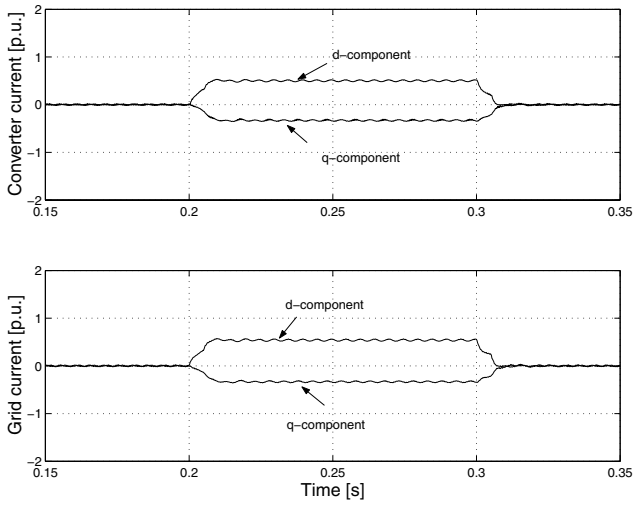

Figure 10. Negative sequence of VSC current (upper) and grid current (lower): 55 % voltage dip due to double phase to ground fault.

IV. Proposed Controller for Balanced Currents

A. *One controller in the positive sequence frame with feed forward for the negative sequence (NSFF)*

Since the main interest of the controller is to deal with voltage imbalance, the LCL-filter should be described in positive and negative sequence synchronous frames (*dqp*- and *dqn*- frames) to derive relevant control laws. The *dqp*-frame is synchronized with the grid voltage with the same direction of rotation, while *dqn*-frame rotates in the opposite direction.

The LCL-filter equations (1) to (3), is described in the *dqp*-frame as follows:

$$\frac{d}{dt}\underline{i}_{1dq} = -j\omega\underline{i}_{1dq} - \frac{R_1}{L_1}\underline{i}_{1dq} - \frac{1}{L_1}\underline{u}_{cdq} + \frac{1}{L_1}\underline{u}_{dq} \tag{13}$$

$$\frac{d}{dt}\underline{i}_{2dq} = \frac{-R_2}{L_2}\underline{i}_{2dq} - j\omega\underline{i}_{2dq} + \frac{1}{L_2}\underline{u}_{cdq} - \frac{1}{L_2}\underline{e}_{dq} \tag{14}$$

$$\frac{d}{dt}\underline{u}_{cdq} = \frac{1}{C_f}\underline{i}_{1dq} - \frac{1}{C_f}\underline{i}_{2dq} + j\omega\underline{u}_{cdq} \tag{15}$$

In steady state and *dqn*-frame, the foregoing equations are read as follows:

$$\frac{-R_1}{L_1}\underline{i}_{1dqn} + j\omega\underline{i}_{1dqn} - \frac{1}{L_1}\underline{u}_{cdqn} + \frac{1}{L_1}\underline{u}_{dqn} = 0 \tag{16}$$

$$\frac{-R_2}{L_2}\underline{i}_{2dqn} + j\omega\underline{i}_{2dqn} - \frac{1}{L_2}\underline{u}_{cdqn} + \frac{1}{L_2}\underline{e}_{dqn} = 0 \tag{17}$$

$$\frac{1}{C_f}\underline{i}_{1dqn} - \frac{1}{C_f}\underline{i}_{2dqn} - j\omega\underline{u}_{cdqn} = 0 \tag{18}$$

For the grid currents to be symmetrical, the negative sequence components in *dq*-frame should be nullified; i.e. $\underline{i}_{2dqn}=0$. That should be achieved by adjusting the reference VSC voltage vector described in (7). Substituting with $\underline{i}_{2dqn}=0$ in (18) and using the result in (16) yields

$$\underline{u}^*_{dqn} = \underline{u}_{cdqn}\left(1+\omega^2 C_f L_1\right) + jR_1\omega C_f\,\underline{u}_{cdqn} \tag{19}$$

This is implemented using positive sequence grid and capacitor voltage vectors within the controller equations and the negative sequence capacitor voltage vector is fed-forward to calculate the negative part of the VSC reference voltage vector, as suggested in Fig. 11.

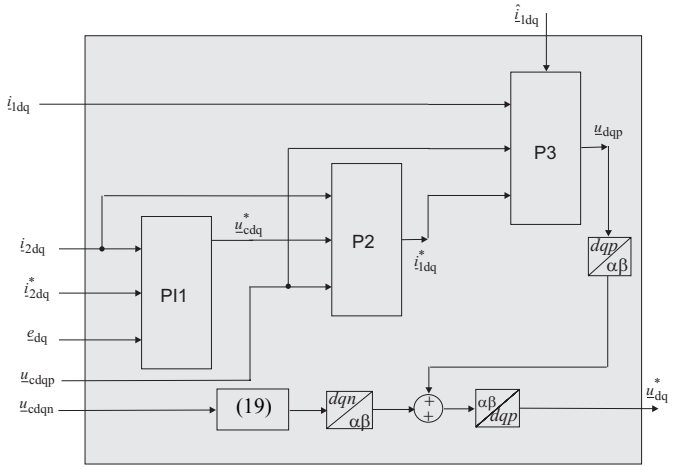

Figure 11. Schematic diagram for the controller for balanced currents.

However, recalculating (19) with the specified filter parameters, yields

$$\underline{u}^*_{dqn} \approx \underline{u}_{cdqn} \tag{20}$$

which is the condition for balanced converter currents. With this algorithm, the VSC currents are forced to be balanced, which reduces the ratio of imbalance in the grid currents.

Moreover, substituting $\underline{i}_{1dqn} = 0$ and $\underline{i}_{2dqn} = 0$ in (17) results in $\underline{u}^*_{cdqn} = \underline{e}_{dqn}$ and in (18) results in $\underline{u}^*_{cdqn} = 0$. Since these conditions contradict with each other, it is not possible to achieve symmetrical grid and VSC currents simultaneously.

B. Dual vector controller (DVC)

The controller equations (4) to (9) can be described in *dqp*-frame and *dqn*-frame, and then two parallel controllers, one for each frame, can be implemented as shown in Fig. 12 [8]. To achieve symmetrical grid currents during grid voltage unbalance, the reference negative sequence currents are set to zero. This controller cannot achieve symmetrical VSC current, since there is no direct access to the VSC current reference.

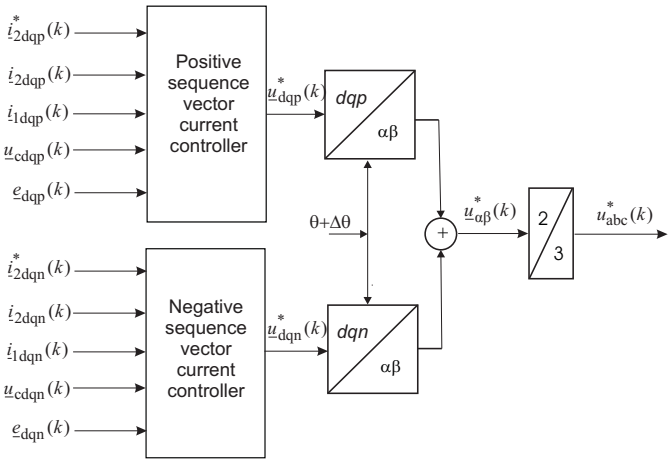

Figure 12. Dual vector controller.

C. Results

The first proposed controller, to achieve balanced currents in case of grid voltage unbalance, using the feed forward of the negative sequence capacitor voltage (NSFF) is tested in case of unbalanced voltage dips. The VSC negative sequence current is nullified, for the three introduced different voltage dips, while the negative sequence grid current is significantly reduced. This is shown for the dip due to single phase fault, since it produces the most amount of imbalance, in Fig. 13. This amount of unbalance is reduced from 132 % to less than 5 % when applying the current balancing algorithm. The three phase VSC and grid currents are also shown in Fig. 14. When the dual controller, DVC, is implemented with the same voltage dip, the resulting negative sequence in the grid and VSC currents is as shown in Fig. 15. The negative sequence of the grid current is nullified during the dip, while the negative sequence of the VSC current is reduced to less that 5 %.

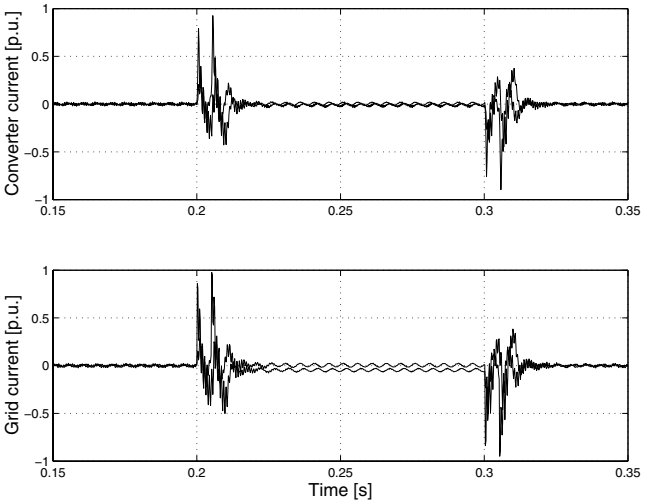

Figure 13. Negative sequence of VSC current (upper) and grid current (lower): NSFF and 10 % voltage dip due to single phase to ground fault.

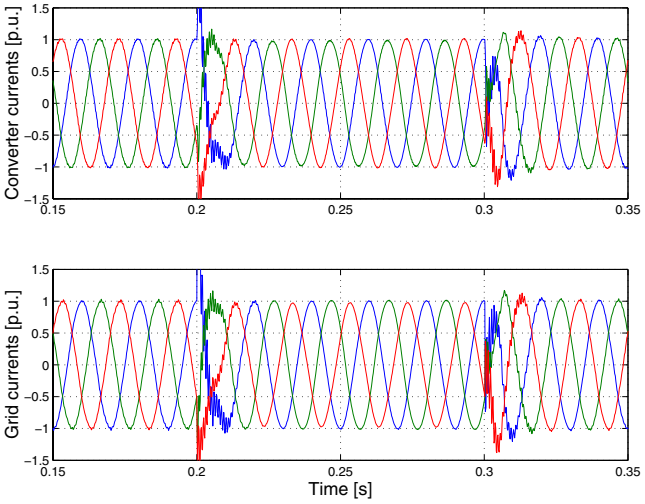

Figure 14. VSC current phasors (upper) and grid current phasors (lower) balanced current control.

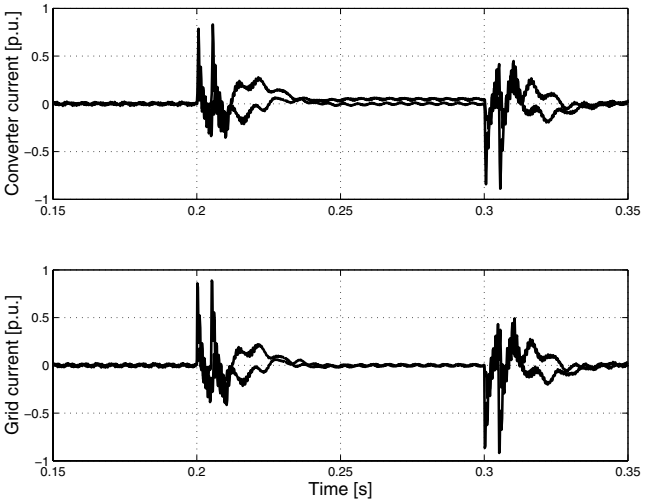

Figure 15. Negative sequence of VSC current (upper) and grid current (lower): DVC and 10 % voltage dip due to single phase to ground fault.

V. CONCLUSIONS

A vector current controller for VSC connected to the grid through LCL-filter is developed with the main focus on reducing current imbalance in case of unbalanced voltage dips at the grid. The controller is applied in the positive sequence frame and the negative sequence capacitor voltage vector is fed-forward with relevant relations that are derived here. Implementing this controller the currents on the VSC side are symmetrical while the amount of imbalance in the current on the grid side is reduced from 132 % to 5 % in case of a voltage dip due to a single phase fault with 10 % remaining voltage. The controller has been tested also for dips due to double phase fault and double phase to ground fault. The grid currents are almost symmetrical during the different voltage dips, which results in protecting the VSC from tripping due to overcurrents or current imbalance during the dip period. This controller has been compared with a dual vector controller (DVC) that is composed of two controllers; one is implemented in the positive sequence frame and the other is implemented in the negative sequence frame. The DVC has been tested with the same cases of grid voltage imbalance. The resulting grid side current is balanced while the VSC side current has an amount of imbalance of less than 5 %.

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Paper E

F. Magueed, and T. Thiringer, “Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC,” *submitted to Electrical Power Quality and Utilization Journal.*

Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC

Fainan Magueed, *Member, IEEE*, and Torbjörn Thiringer, *Member, IEEE*

***Abstract*— The phase locked loop (PLL) is an important part of the current-controlled grid-connected converter. Its job is to estimate the phase angle of the grid voltage. If the PLL is not robust, the grid-voltage distortion will lead to an error in the estimated phase leading to a degradable performance of the converter's function. In this paper, the effect of the PLL on the operation of a current-controlled voltage-source converter is examined. A PLL synthesis is proposed, to track the phase angle of the distorted grid voltage, and compared with a previously investigated PLL. The result found is that the proposed synthesis of the PLL is superior in case of grid voltage harmonics other than the 5th and the 7th orders. Moreover, the capability of compensating for the voltage amplitude modulation was improved using the proposed PLL. The amplitude oscillation has been reduced from 8% to 3%, with the proposed PLL, compared to from 8% to 5% with the previously investigated PLL.**

***Index Terms*— Amplitude modulation, Distributed generation, harmonics, phase locked loop, light flicker, power quality, voltage dips, voltage source converters.**

I. Introduction

Grid-connected voltage-source converters (VSCs) are the basic elements of most new FACTS, custom power equipment and HVDC systems due to their good controllability [1]. They are also used as an interface for distributed generation systems and in adjustable speed drives applications. To keep their control goals, which are dependent on the instantaneous state of the grid, a good estimation of the grid phase angle is needed. This is usually done using a software phase locked loop (PLL) instead of a classical hardware PLL to reduce the controller cost and provide the flexibility to modify the PLL's parameters to match a specific control requirement.

In three-phase systems, the PLL algorithm is usually implemented in a rotating reference frame (*dq*-frame) that is synchronized with the grid voltage using the estimated phase angle [2]. This type of PLL will be referred to as Q-PLL, since its major input is the quadrature (*q*) component of the voltage vector. The latter reflects the error between the estimated and the actual phase. When this error is fed into a PI controller, the estimated angle will change in a way to eliminate this error. The Q-PLL yields good results during non-disturbed conditions. However, in the presence of grid-voltage harmonics, imbalance, or voltage amplitude change, an error in the estimated phase will occur [2]. In order to make the PLL robust towards this polluted voltage and to recover the correct phase angle, the use of low pass filters (LPF) has been proposed in [3] and [4]. The aim of using an LPF is to extract the positive sequence of the grid voltage in the *q*-direction, in which the negative sequence should not appear. In this way the effect of the grid voltage imbalance on the estimated phase is negligible. However, a trade-off has to be made between robustness and good transient performance of the LPFs [5]. Lower cut-off frequency of the filters results in less distortion in the estimated phase, yet slower dynamics will occur. In order to overcome this problem, a second order generalized integrator has been proposed in [6] to extract the positive sequence of the grid voltage. The task of this integrator is to produce a 90^{o} delayed signal, which is adaptive to the change of the grid fundamental frequency. However, the need for tuning the integrator is adding to the complexity of the PLL-design. On the other hand, for the grid-connected applications considered here, the frequency change is assumed to be kept within the allowed limits (e.g. in Sweden $\pm$ 0.5 Hz is respected according to the Swedish standard SS EN-50160:2000) by the strong grid.

The purpose of this paper is to investigate the effect of the PLL on the operation of a current-controlled power-electronics interfaced distributed-generation with a voltage source converter as a front end. This is done through the implementation of two PLL configurations, considering the case of a distorted grid voltage. The previously investigated PLL, which uses the positive-sequence of the quadrature component of the grid voltage to extract the angle, is compared with a proposed PLL synthesis based upon the neural networks application. The two PLL configurations have been evaluated regarding the voltage quality at the connection point of the VSC, where the VSC controller is aiming at regulating the terminal voltage in addition to its original task, which is injecting active power to the grid.

II. Phase Locked Loop (PLL)

The output voltage of a grid-connected VSC is synchronized with the grid voltage using a PLL. The estimated phase output of the PLL could also be used for the detection of an islanding condition to protect the VSC and the system that is connected

through it, in case of severe voltage changes in the grid [7]. Hence, for proper operation of the controller, the error in the estimated phase should be minimal. Two PLL algorithms will be evaluated regarding their performance to handle the voltage disturbaces. Since the quadrature component PLL is the basic building element for both, it will be explained first.

A. Quadrature-Component Based PLL (Q-PLL)

This type of PLL has been investigated previously in [2], for instance, and is shown here in Fig. 1. The measured grid voltage is transformed from three-phase notation into a voltage vector in a fixed $\alpha\beta$-frame, using power invariance transformation. This voltage vector is then normalized and transformed into a vector in a rotating *dq*-coordinate, which rotates with the estimated angular frequency $\hat{\omega} = \mathrm{d}\hat{\theta}/\mathrm{d}t$, where $\hat{\theta}$ is the estimated phase angle. The normalized *q*-component of the voltage is then used as an input to a PI-controller to produce a required change in the angular frequency ($\Delta\omega$) to track the changes in the phase angle.

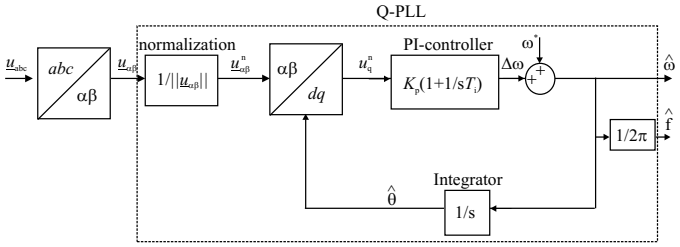

Fig. 1 Phase estimation using Q-PLL.

The normalization of the voltage vector results in nullifying the phase estimation error due to a balanced voltage amplitude change (e.g. three-phase voltage dips). However, in case of an unbalanced voltage amplitude variation (e.g. an unbalanced voltage dips), oscillations having the frequency of twice the fundamental frequency will be superimposed in the *q*-component voltage due to the introduced negative sequence that rotates in the opposite direction [2].

B. Positive Sequence Frame PLL (PS-PLL)

To reduce the error in the estimated phase-angle due to the existence of the negative sequence in case of an unbalanced grid voltage, a PS-PLL is implemented. As shown in Fig. 2, the three-phase voltages are measured and transformed into a vector in the stationary $\alpha\beta$-frame. Then the positive sequence voltage vector is extracted using the DSC algorithm, and fed into the Q-PLL that has been described in Fig. 1.

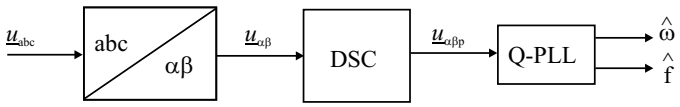

Fig. 2 PS-PLL.

1) The delayed signal cancellation method (DSC)

The method of DSC, which has been proposed in [8], is adopted here for the decomposition of the supply voltage into the positive and the negative sequences. It is defined in the $\alpha\beta$-plane by the following expressions:

$$\underline{u}_{\alpha\beta\mathrm{p}}(t) = \frac{1}{2}\left(\underline{u}_{\alpha\beta}(t) + \mathrm{j}\underline{u}_{\alpha\beta}(t - \frac{T_g}{4})\right) \tag{1}$$

$$\underline{u}_{\alpha\beta\mathrm{n}}(t) = \frac{1}{2}\left(\underline{u}_{\alpha\beta}(t) - \mathrm{j}\underline{u}_{\alpha\beta}(t - \frac{T_g}{4})\right) \tag{2}$$

where T_g is the fundamental period of the grid voltage;
$\underline{u}_{\alpha\beta\mathrm{p}}$ is the positive sequence voltage vector in the $\alpha\beta$-frame; and
$\underline{u}_{\alpha\beta\mathrm{n}}$ is the negative sequence voltage vector in the $\alpha\beta$-frame.

2) DSC effect on grid voltage harmonics

It is assumed that the grid voltage has an h^{th} harmonic component superimposed on its fundamental component. In the stationary $\alpha\beta$ −frame, this will be expressed in the time domain as follows:

$$\underline{u}_{\alpha\beta}(t) = U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \tag{3}$$

where U_1 and U_h are the amplitudes of the fundamental and the h^{th} harmonic respectively, ω is the fundamental grid-voltage angular-frequency, and h_s is the related harmonic sequence that takes a value of either +1 (for positive sequence) or -1 (for negative sequence) according to [9]:

$$h_s = \begin{cases} +1 & h = 3n+1 \\ -1 & h = 3n+2 \\ 0 & h = 3n \end{cases} \tag{4}$$

where n is any number starting from zero.

The zero sequence harmonics will not be regarded in this analysis, since the VSC is normally connected to the grid through a Y/D transformer that eliminates the triplet harmonics.

Substituting (3) in (1), the positive-sequence vector of the grid voltage in $\alpha\beta$ −frame is:

$$\underline{u}_{\alpha\beta\mathrm{p}}(t) = \frac{1}{2}\begin{pmatrix} U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \\ + \mathrm{j}\left(U_1 e^{\mathrm{j}\omega(t - T_g/4)} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega(t - T_g/4)}\right) \end{pmatrix} \tag{5}$$

where $\dfrac{\omega T_g}{4} = \dfrac{\pi}{2}$.

The harmonic part of (5) can be expressed using trigonometric functions as follows:

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = \frac{U_\mathrm{h}}{2}\begin{pmatrix} \cos(h\omega t) + \mathrm{j}(h_\mathrm{s})\sin(h\omega t) \\ + \mathrm{j}\cos\left(h\omega t - h\dfrac{\pi}{2}\right) - (h_\mathrm{s})\sin\left(h\omega t - h\dfrac{\pi}{2}\right) \end{pmatrix} \tag{6}$$

For the odd harmonics of orders less than 11^{th} (i.e. 5^{th} and 7^{th}), $\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}$ will be nullified since:

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = -(h_\mathrm{s})\sin(h\omega t) \tag{7.a}$$

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = (h_s)\cos(h\omega t) \quad (7.b)$$

However, opposite signs will appear in (7) for higher harmonics (e.g. the 11th), implying the existence of such harmonics superimposed on the positive sequence voltage.

For the even harmonics of orders less than the 10th, the following will hold:

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = (h_s)\cos(h\omega t) \quad (8.a)$$

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = -(h_s)\sin(h\omega t) \quad (8.b),$$

which implies the existence of these harmonics superimposed on the fundamental component in the positive sequence frame. In spite of the opposed sign in (8) for higher harmonics (more than the 10th), they will still exist in the positive sequence as (6) suggests.

Yet, since the 5th and 7th harmonics are the most dominant in the power system [9], it is expected that using the PS-PLL in estimating the grid-voltage phase angle will give good results as it will be shown later in the case study.

3) DSC effect on grid-voltage amplitude modulation

Grid voltage amplitude modulation is a result of fast periodically-changing heavy loads that are connected at the grid. If a distribution network is considered, one of the direct effects would be the light flicker. The frequency of light flicker ranges between 0.5 Hz and 30 Hz, since this is the range of the human eye sensibility [10]. One way to mitigate this phenomenon is to compensate for the oscillating reactive power using a STATCOM [10], which is a three-phase VSC.

If the VSC controller is aimed at mitigating the voltage-amplitude modulation, the *q*-component of the grid voltage will be forced to oscillate with the same frequency as the modulating function. Substituting $h_s = 0$ and $h = 1/5$ (for a 10 Hz amplitude modulation) in (6), will show that the positive sequence will also be oscillating, producing an error in the estimated phase. To nullify this error, a bandwidth less than the frequency of the amplitude-modulating signal should be adopted. However, this will affect the transient performance of the VSC.

C. Neural-Network Fundamental-Extractor Based PLL (NN-PLL)

To nullify the phase-estimation error produced due to the harmonics and amplitude modulation of the grid voltage and in the same time to obtain a good dynamic performance, the implementation of an adaptive linear neural-network is proposed. The advantages are the easy synthesis and programming, the adaptation capability to the change in the grid voltage, and the fast response.

1) Adaptive linear neural-network extractor (ADALINE)

ADALINE is one of the earliest neural network models that was proposed in [11]. A simple ADALINE consists of one neuron that has a linear input-output relationship, where each input is simply multiplied by a certain weight and all inputs are summed together to produce the output. The power of ADALINE, though, comes from the on-line adaptation of its weights that gives it a non-linear property. For this purpose, the least mean square (LMS) algorithm is used [12].

ADALINE has been implemented in [13] as a combiner to identify the voltage waveform for the classification of power quality issue. It will be used here in the same way, however, as an extractor to relieve the fundamental component of the source polluted voltage. ADALINE is shown in Fig. 3, where the discrete input vector $\mathbf{x}(k)$ is composed of sine and cosine elements of all possible frequency components that could be contained in the source voltage

$$\mathbf{x}(k) = \left[\sin(\omega k T_s) \quad \cos(\omega k T_s) \quad \ldots \quad \sin(h\omega k T_s) \quad \cos(h\omega k T_s)\right]^T \quad (9)$$

where h is the highest harmonic order expected, k is the sampling instant, T_s is the sampling time, and the superscript T indicates the transpose of the vector. This input vector $\mathbf{x}(k)$ is then multiplied by a weight vector $\mathbf{w}(k)$ to produce the ADALINE output $u_{nn}(k)$.

$$\mathbf{w}(k) = \left[w_{11} \quad w_{12} \quad w_{21} \quad w_{22} \quad \ldots \quad w_{h1} \quad w_{h2}\right] \quad (10)$$

$$u_{nn}(k) = \mathbf{w}(k)\cdot\mathbf{x}(k) = \sum_{i=1}^{2h} w_i x_i \quad (11)$$

where w_i and x_i is the i^{th} element in the vectors $\mathbf{w}$ and $\mathbf{x}$ respectively.

The output is then compared with the measured and sampled voltage signal $u_s(k)$, where the resulting error $\varepsilon_{nn}(k)$ is used by the LMS algorithm to modify the weight vector according to

$$\mathbf{w}(k+1) = \mathbf{w}(k) + \lambda\frac{\mathbf{x}(k)\varepsilon_{nn}(k)}{\mathbf{x}(k)^T\mathbf{x}(k)} \quad (12),$$

where λ is the learning factor.

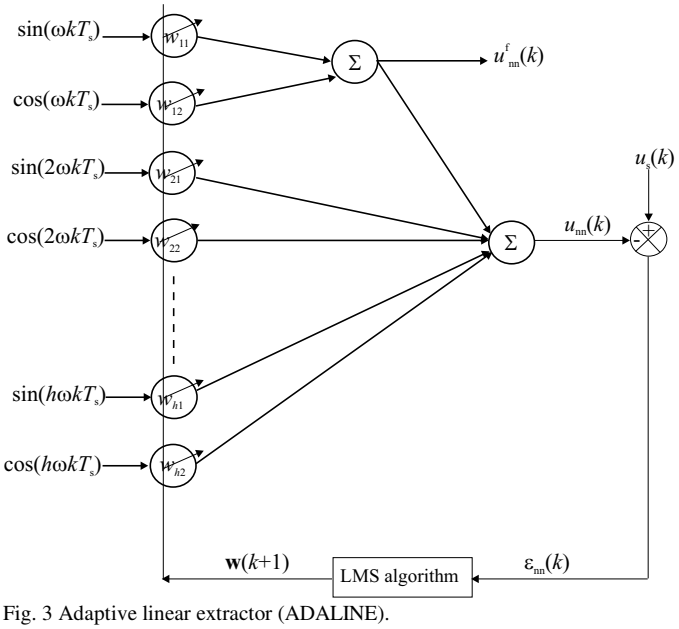

Fig. 3 Adaptive linear extractor (ADALINE).

The learning factor λ is given a value between 0 and 1, where this value specifies the speed of the correction of the error ε_{nn} [14]. The upper limit value of 1 corrects the error within one iteration, while decreasing this value will increase the number of iterations used for the correction. This is evaluated applying an input sinusoidal signal with a 5% magnitude of the 5th harmonic and a 3% magnitude of the 7th harmonic and a 30% voltage decrease at 0.6 s with a phase-angle jump of -60°. The output of ADALINE is examined using two different learning rates: 0.07 and 0.7. The tracking signal u_{nn} and the fundamental signal u_{nn}^{f} are shown for λ = 0.07 in Fig. 4, whereas counterpart signals corresponding to $\lambda = 0.7$ are shown in Fig. 5. As expected, the tracking is faster with the higher learning rate. However, the fundamental wave is distorted in the transient period and an overshoot occurs due to the fast change in the weight vector. With lower λ, the change in the weight vector is slower and hence the fundamental wave will ride-through the transient period keeping its sinusoidal shape and implying better performance of the PLL.

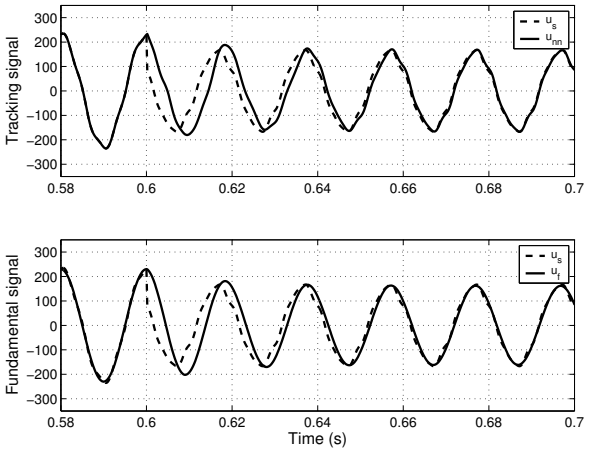

Fig. 4 ADALINE tracking signal (upper) and fundamental signal (lower) with λ =0.07.

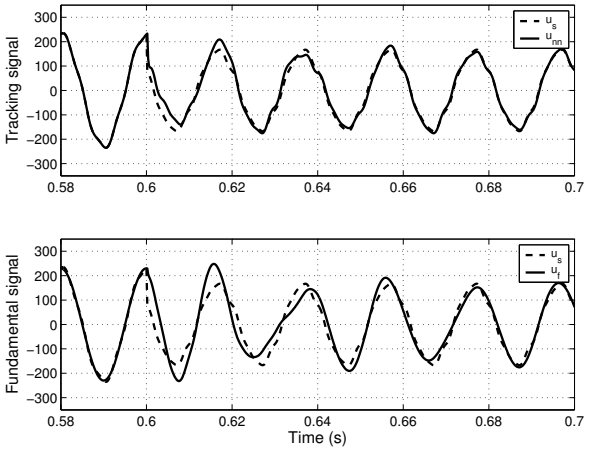

Fig. 5 ADALINE tracking signal (upper) and fundamental signal (lower) with λ =0.7.

The block diagram of the PLL implementing ADALINE (NN-PLL) is shown in fig. 6. The three-phase voltage is transformed into the stationary $\alpha\beta$-frame. Then each component is fed into a separate ADALINE algorithm, shown in Fig. 3, to extract the fundamental component that is fed into a Q-PLL. The effect of changing the learning rate is reexamined regarding the overshoot in the estimated-phase due to an unbalanced voltage dip with about -45° phase angle jump. The result is shown in Fig. 7, indicating the increase of the overshoot as the learning rate increases. This is again justifies the use of lower value for the learning rate.

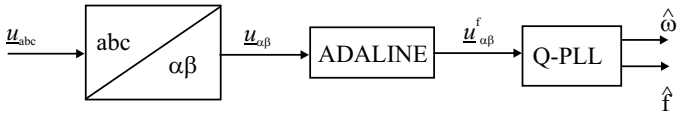

Fig. 6 NN-PLL.

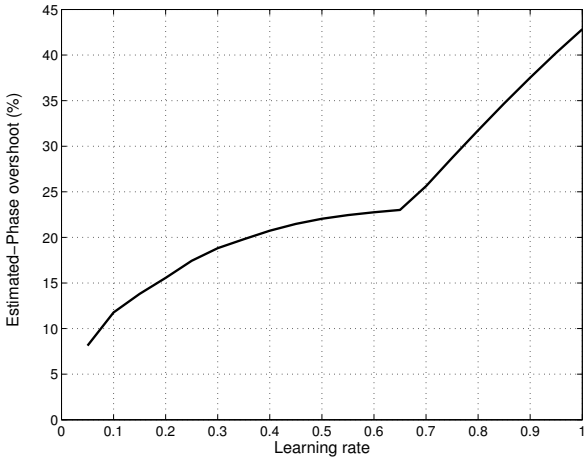

Fig. 7 Estimated-phase overshoot due to unbalanced voltage dip with phase angle jump.

III. The Performance of PS-PLL, and NN-PLL

The performance of PS-PLL and NN-PLL has been tested in MatLab/Simulink regarding the harmonics effect and the dynamic behavior.

The error in the estimated phase angle due to the presence of the grid voltage harmonics is shown in Fig. 8, with a three different bandwidth values for the Q-PLL, for the two estimators. A 2% amplitude of the 2nd, 4th, 5th, 7th, 11th and 13th harmonic orders has been superimposed separately on the fundamental grid-voltage. The phase error has been calculated as the peak-to-peak amplitude of the normalized quadrature-voltage.

With the PS-PLL, the error in the estimated phase-angle increases using higher values of the bandwidth. Moreover, the amplitude of the error increases with the increase of the harmonic order, excluding the case for the 5th and 7th harmonics at which it was proven that the error is nullified. This can be understood by inspecting (6), where the harmonic order is in proportional relationship with the frequency of the

oscillations superimposed on the fundamental grid voltage.

Using the NN-PLL the error is nullified for all harmonic orders and all values of bandwidth, which means that it is robust and in the same time provides a better dynamics.

To study the dynamical behavior, a balanced voltage dip having a -40° phase angle jump has been applied at the grid as shown in Fig. 9. The dip starts at 0.4 s and ends at 0.6 s. The actual phase angle of the grid voltage is shown by the solid line while the estimated phase angle is shown by the dashed line for PS-PLL and dash-dotted line for NN-PLL. The NN-PLL has been implemented using a bandwidth of 50 Hz, while the PS-PLL has a bandwidth of 5 Hz since it should be slow to be robust against the grid voltage harmonics. As expected, using the NN-PLL results in the fast tracking of the phase angle of the grid voltage, implying a better dynamic performance.

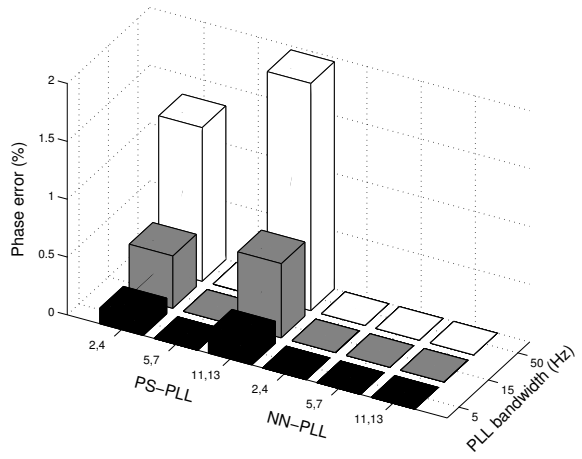

Fig. 8 Estimated-phase error due to different harmonics and in case of bandwidth of 5, 15, and 50 Hz.

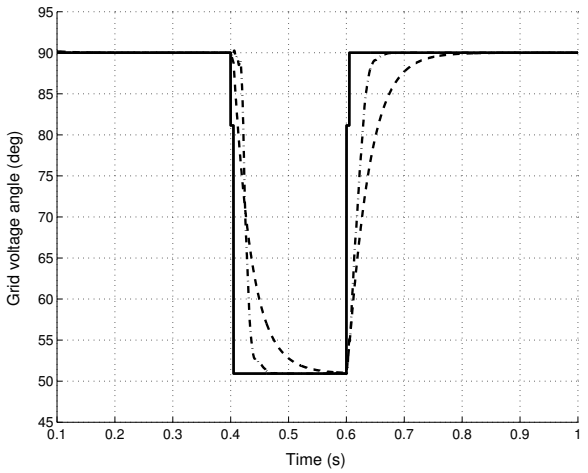

Fig. 9 Grid voltage angle; actual (solid), estimated using PS-PLL with small bandwidth (dashed), and estimated using NN-PLL with large bandwidth (dash-dotted).

IV. Case Study: Grid Connected VSC as an Interface for Distributed Generation

A distributed generation (DG) unit is considered in this case study, in which the EMTDC is used for the simulation, to evaluate the effect of the two previously discussed PLL algorithms on its controller's performance. The mitigation of grid voltage amplitude modulation and voltage dips with phase angle jumps are considered here.

A. System Model

In Fig. 10 an example part of a distribution system with a DG is presented. A fluctuating load is assumed to be connected at bus 1, and is further assumed to be disconnected in case of a fault at the same bus. Its effect is encountered as an 8% amplitude modulation of the grid voltage at bus 1 using a cosine modulating signal with a frequency of 10 Hz. In reality this modulating signal could have an infinite number of frequencies, but for the sake of clarity only the 10 Hz component is displayed here. A distributed generation unit is connected at bus 3, where a sensitive load is also connected. The latter is assumed to be a static inductive load that requires the voltage to be maintained at 1 p.u. all the time at the point of common coupling (bus 3) with a good power quality.

The DG unit could represent a small wind turbine, a photovoltaic unit, or a fuel cell system. Since the energy source is not the issue here, it has been assumed that its dynamics are slower than that of the control system. Hence, the energy source is modeled as a constant current source i_{in}, as shown in Fig. 11. The injected power, coming from the energy source, is transferred through a DC-link and adjusted to match the grid-connection requirements using a controlled voltage source converter (VSC). Moreover, an LCL-filter is used in order to eliminate the higher grid-side current harmonics caused by the PWM switching of the VSC [15]. The grid side inductance, which is connected to the PCC, represents the leakage inductance of a step-up transformer.

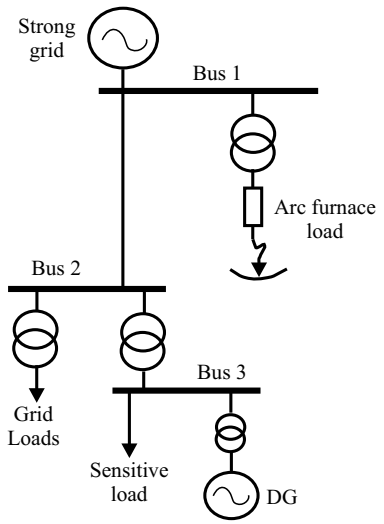

Fig. 10 Distribution system for the case study.

B. Controller description and targets

The main task of the controller of the DG is to inject active power into the grid. In addition, using the power electronics system with the controller, shown in Fig. 11, it can mitigate power quality problems. Accordingly, in grids with large industrial loads (polluting the grid with harmonics, voltage

fluctuations, voltage dips … etc.) and sensitive loads (requiring a certain level of power quality), the DG should maintain a controlled operation and in the same time grid power quality improving. For this purpose, a PCC-voltage regulator is used to provide the ability to inject reactive power at the PCC to maintain the voltage at its nominal value and condition. Hence, the DG controller is composed of the following parts.

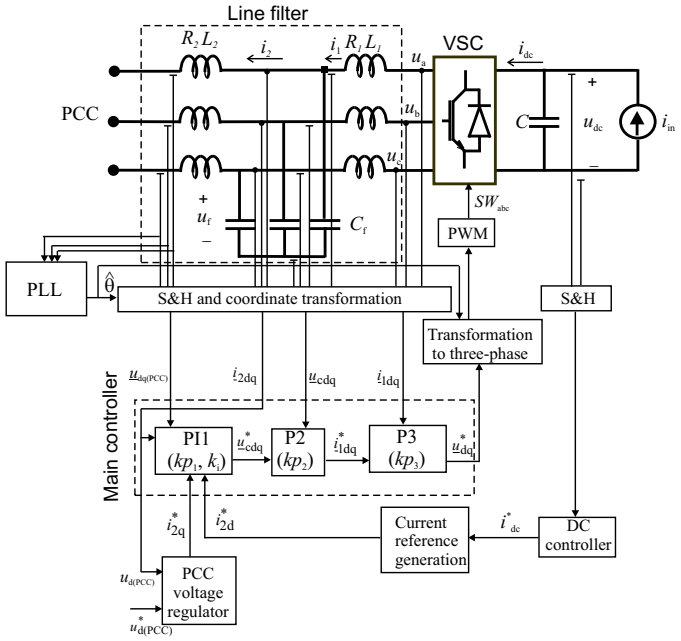

Fig. 11 Power electronics converter-interfaced DG system with robust controller.

1) Main Controller

The control system for the DG unit is implemented in a rotating *dq*-frame that is synchronized with the voltage at the PCC using a phase locked loop (PLL).

The main controller, which is shown in Fig. 11, consists of three cascaded controllers to obtain proper dynamics and at the same time to damp the oscillations at the resonance frequency of the LCL-filter as explained in [15]. The three-cascaded controllers are: an outer current controller, a capacitor voltage controller, and an inner current controller. The outer controller (PI1) tracks the reference current of the grid $\underline{i}^*_{2\mathrm{dq}}$ and its output is the reference capacitor voltage $\underline{u}^*_{\mathrm{fdq}}$, which is fed to the capacitor voltage controller (P2). In P2, the measured (or estimated) capacitor voltage $\underline{u}_{\mathrm{fdq}}$ is compared with its reference command using a proportional controller, which produces the reference current $\underline{i}^*_{1\mathrm{dq}}$ for the inner current controller (P3). The latter is also a proportional controller, which generates the reference voltage $\underline{u}^*_{\mathrm{dq}}$. This reference voltage is then transformed into a three-phase voltage vector to be used in the PWM as a reference signal to generate the proper switching commands. This controller is explained in more details in [15].

2) DC-regulator

In the case of grid voltage variations, the DC-link voltage should be regulated to maintain a constant value in order to protect the DC capacitor and maintain the correct operation of the VSC.

The DC regulator is a PI-controller that generates a DC current reference i^*_{dc}. Then, the active current reference $i^*_{2\mathrm{d}}$ is generated (current reference generation block in Fig. 11), based on the power balance between the AC and DC side of the VSC, to maintain the DC voltage at its nominal value during voltage disturbances at the PCC.

3) PCC-voltage regulator

Since the *q*-component of the PCC voltage is set to zero using the coordinate transformation, the *d*-component $u_{\mathrm{d(PCC)}}$, should be regulated to maintain the PCC voltage at its nominal value $u^*_{\mathrm{d(PCC)}}$. The reactive current reference $i^*_{2\mathrm{q}}$ is generated to compensate for the error in the PCC voltage using a PI-controller. More details of the control system are given in [16].

C. Operation in case of voltage amplitude modulation, and voltage dips

Due to the loads connected to the grid, a voltage amplitude modulating signal is superimposed on the fundamental grid voltage. Moreover, a voltage dip with a phase angle jump will appear at the PCC, from 0.5 s to 0.7 s, caused by a three phase fault at bus 1. In addition, due to the voltage drop through the feeder, the voltage at the PCC will decrease in amplitude. All these phenomena should be compensated for locally at the PCC by the DG injected power, which is adjusted by the controller. The impact of the two PLL algorithms on the controller performance is now to be investigated.

1) Using the PS-PLL

With the voltage compensation capability of the DG, the voltage at the PCC should be regulated to 1 p.u. However, the error in the phase estimation, due to the polluted voltage, will result in an error in the value of the current command $i^*_{2\mathrm{q}}$ leading to uncompensated oscillations in e_{d}. Moreover, regarding the equation of the instantaneous reactive power injected by the DG at PCC [16]

$$q_{(\mathrm{PCC})} = u_{\mathrm{q(PCC)}} i_{2\mathrm{d}} - u_{\mathrm{d(PCC)}} i_{2\mathrm{q}} \quad (13),$$

and since the active power is regulated using the DC-regulator, which implies regulated $i_{2\mathrm{d}}$, the *q*-component voltage $u_{\mathrm{q(PCC)}}$ will oscillate in consequence of the oscillating $q_{(\mathrm{PCC})}$. Though, due to the phase estimation error, it is unavoidable that the oscillations will increase in amplitude. Hence, the three-phase voltage-envelope will oscillate around the nominal value.

This is shown in Fig. 12, where the voltage envelope at the PCC is shown in the upper trace for the case of no DG installed. The middle trace in the same figure represents the case for using the PS-PLL with a 15 Hz bandwidth. The amplitude modulation still exists, with about 5% peak-to-peak value, due to the high bandwidth of the PLL compared to the

frequency of the modulating signal.

2) Using NN-PLL

The three-phase voltage-envelope at the PCC is shown, in this case, by the lower trace of Fig. 12. The peak-to-peak value of the oscillation is reduced to 3% using the same bandwidth as before. Moreover, the dynamic behavior is better, which is obvious regarding the amplitude of the overshoot during and after the voltage dip.

The estimated frequency is shown in Fig. 13 for the two PLL configurations.

Moreover, the voltage amplitude variation at PCC has been tested with different modulating signal frequencies and the result is shown in Fig. 14, where it can be noted that the system with NN-PLL has a lower peak-to-peak value of the oscillation of the voltage envelope.

It is worth noting here that the oscillations of the voltage envelope will not be completely nullified since both active and reactive powers are oscillating, due to the modeling that is considered here, which means that both injected active and reactive powers should be oscillating in order to compensate for it. However, this is not possible since the application of a DG implies constant injected active power into the grid. Moreover, the behavior of the NN-PLL is dependent on the input-vector length, the order of harmonic frequencies used in that vector, and the initial weights values. The input-vector length is taken, here, as 18 and the initial weight vector was set to zero.

In addition, regarding the application considered here, which is DG systems, it is assumed that there is an injected active power to the grid. The value of this active power, though, affects the voltage compensation capability. More injected active power implies more available reactive power to be injected. Yet, the current amplitude will increase leading to increased DC-link voltage ripples, as shown in Fig. 15. Hence, if a current limiter is applied, to protect the VSC valves and improve the DC-link voltage regulation, it will mean limiting the voltage compensation capability.

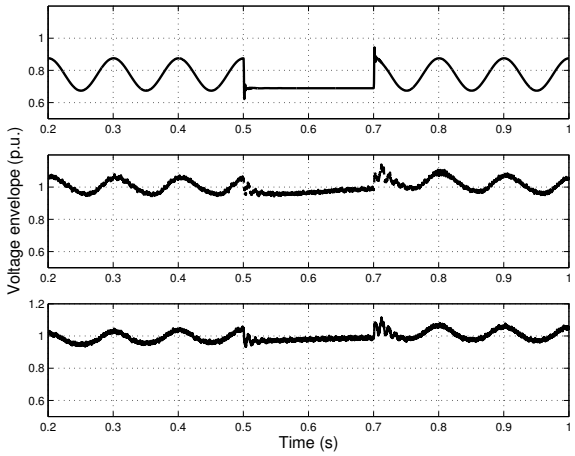

Fig. 12 Voltage envelop with DG not connected (upper), DG with PS-PLL (middle), and DG with NN-PLL (lower).

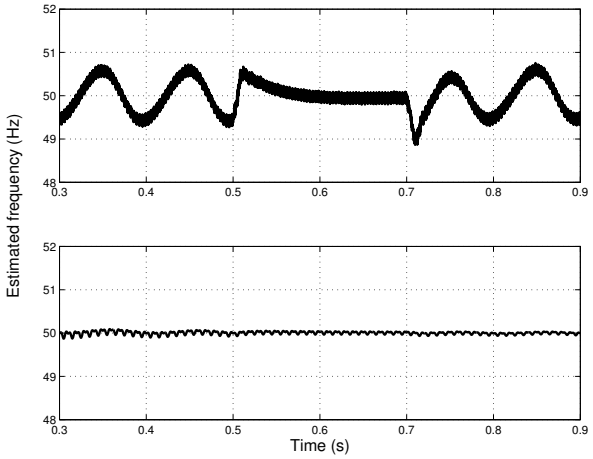

Fig. 13 Estimated frequency using: PS-PLL (upper), and NN-PLL (lower) with 15 Hz bandwidth.

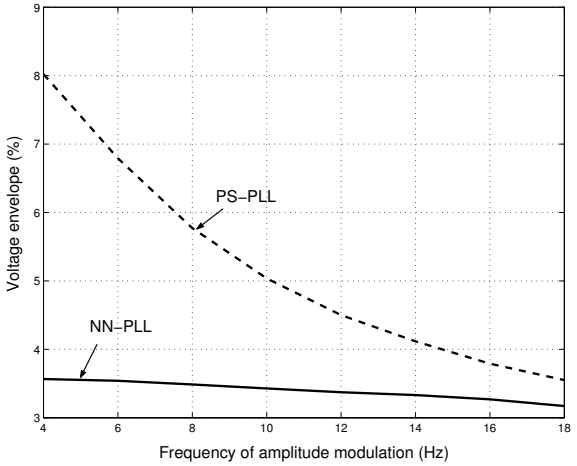

Fig. 14 Voltage amplitude variation due to changing the modulating signal frequency; with PS-PLL (dashed curve) and NN-PLL (solid curve).

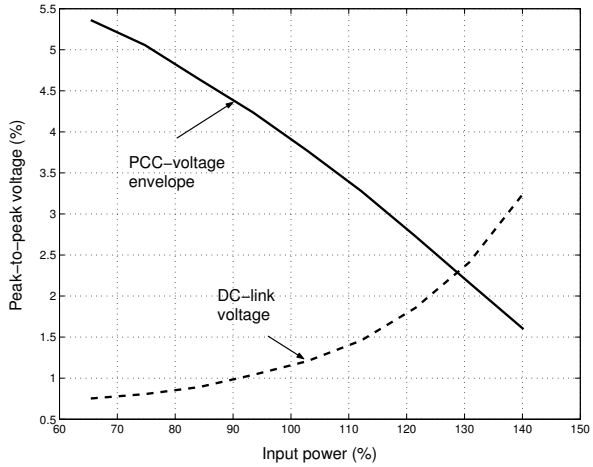

Fig. 15 Effect of the input power on PCC voltage envelope oscillation (solid), and DC-link voltage ripples (dashed).

V. CONCLUSIONS

The error in the phase estimation of the grid voltage affects the performance of the current-controlled grid-connected voltage source converters (VSC). In this paper, a neural network phase locked loop (NN-PLL) estimator has been compared with a previously investigated PLL, which extracts the phase angle from the positive-sequence quadrature-component of the grid voltage. It was shown in this paper that, the proposed PLL synthesis is more robust against grid voltage harmonics, is better in handling the transients, and can improve the voltage compensation function of the VSC.

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Paper G

F. Magueed, G. Olsson, and T. Thiringer, “Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation,” submitted to *IEEE trans. on Power Delivery.*

Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation

Fainan Magueed, *Member, IEEE,* Gustaf Olsson, *Member, IEEE,* Torbjörn Thiringer, *Member, IEEE*

***Abstract*—Islanding of a voltage source converter (VSC) equipped DG unit connected to a weak grid is considered in this paper. The islanding detection using over/under voltage, which is commonly used for passive detection methods, is not adequate due to the voltage limitation that is incorporated in the DG controller for its safe operation. Hence, the estimated frequency of the grid voltage along with a point of common coupling (PCC) voltage regulator, with a reactive current reference limiter incorporated, is proposed for islanding detection algorithm. Using a PCC-voltage regulator adds the active, or dynamic, property for the detection algorithm and increases its reliability. Moreover, using the current limiter increases its robustness, which has been tested for the case of voltage dips at the grid. By setting the proper current limit, the DG unit can have the ability to ride-through voltage dips with magnitudes above a certain limit, which can be set according to the grid codes, and detect islanding for voltage dips with magnitudes lower than that limit. This has been tested for the case of island motor load, which is considered as a difficult type of load since it affects the grid states in the case of islanding.**

***Index Terms*—Distributed generation, Intentional islanding, LCL-filter, PLL, Voltage source converters, Vector control, weak grid.**

I. Introduction

Although the integration of distributed generation (DG) has many driving forces, it still has many challenges [1]. Islanding, due to utility outage, is one of the problems that can cause improper operation of a DG unit, and its connected loads, if it is not detected.

There are two types of islanding detection techniques; passive and active [2]. In the passive techniques, the sensed grid states (voltage, frequency …etc.) are compared with their nominal values and the deviations are used to identify the islanding condition. Although they are simple to implement, the passive techniques suffer from a certain non detectible zone (NDZ), which represents the amount of the active and reactive power mismatch between the DG and its local loads at which the passive detection algorithm fails [2], [3]. Incorporating the active detection techniques, the NDZ becomes negligible. An active detection technique could typically be incorporated in the main controller of the DG, using active disturbance injection into the grid [4]. If the grid is disturbed, the passive detection starts to react to identify the islanding condition.

The problem of islanding can be more crucial with the application of the DG in a weak grid, where the grid states are not robust [5]. That implies that the active detection techniques that tend to disturb the grid are not adequate. Instead, active techniques that tend to improve the power quality at the grid might be more adequate.

The steady state performance of different passive detection algorithms regarding the reduction of the non-detectible zone (NDZ) has been studied in literature [2] - [3]. The under/over frequency has been found to have an NDZ that is independent on the active power mismatch and dependent on the quality factor of the load. To overcome this dependency, an under/over frequency passive detection algorithm has, in this paper, been incorporated in an active detection technique. The detection technique consists of three parts; a passive detection algorithm, a PCC voltage regulator, and a reactive current limiter. The dynamic performance and robustness of the proposed active islanding detection are studied regarding the voltage dips at the grid and the load dynamics.

II. System Description

A. Investigated network

A weak grid system is, here, referring to a rural electric feeder where the voltage level at the load bus is not constant and is affected by the load dynamics. The system in Fig. 1 will be considered, where the voltage at the point of common coupling (PCC) is affected by the feeder voltage drop and the load dynamics. The feeder has an X/R ratio of 10, and its inductance is 6.15 mH per phase. The island-loads consume power that is assumed to be lower than the DG-injected power, implying the directions of the active and reactive power mismatches (ΔP and ΔQ) as designated in the same figure. The island loads will be set (models and parameters) later in order to investigate the ability of the islanding detection method for various cases.

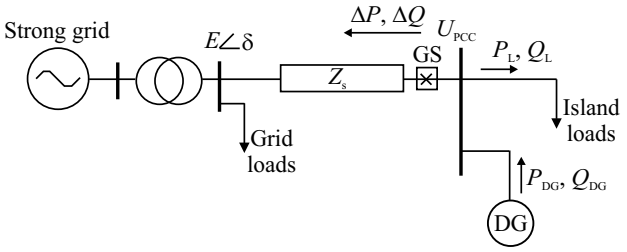

Fig. 1. System considred for islanding study.

The grid loads are assumed to be static loads that have rated power of 0.2 p.u. based on the DG nominal settings. The DG unit is an inverter based system that is connected through an LCL-filter to the PCC. The data of the DG unit are reported in Table I.

TABLE I
DG SYSTEM DATA

Symbol	Quantity	Value
E_{DG}	Nominal RMS line AC voltage	0.4 kV
I_{DG}	Nominal RMS phase current	0.1 kA
f	Nominal grid frequency	50 Hz
U_{dc}	Nominal DC link voltage	0.65 kV
I_{dc}	Nominal DC current	0.107 kA
L_1	Converter-side LCL-filter inductance	0.52 mH
R_1	Converter-side LCL inductor resistance	1.6 mΩ
L_2	Grid-side LCL-filter inductance	0.2 mH
R_2	Grid-side LCL-filter inductor resistance	0.6 mΩ
C_f	LCL-filter capacitance	138 μF
R_d	DC-chopper damping resistance	10 Ω

The main part of the DG system, which is considered here, is a PWM voltage source converter (VSC), which represents the front end of an energy source. The latter is modeled as a constant current source i_{in} (in Fig. 2), since the variations in the input power are considered slow compared to the transient response of the VSC controller. The LCL-filter is implemented on the AC-side of the VSC to prevent harmonic current injection into the grid.

B. DG main controller

The DG controller is implemented in a rotating *dq*-frame that is synchronized with the grid-voltage angular-frequency using a phase locked loop (PLL). The PLL estimates the angular frequency of the grid voltage $\hat{\theta}$ using a PI-controller [6]. In the case of island operation the output of the PLL is set to the reference angular frequency θ^*. As shown in Fig. 2, the grid states (voltages and currents) are measured and transformed into vectors in the *dq*-frame. The transformation matrices set the *q*-component of the grid voltage to zero, while the *d*-component represents the amplitude of the line voltage. A DC-link voltage regulator is also incorporated to maintain a constant DC voltage value in order to protect the DC-capacitor and maintain correct operation of the VSC. The DC-regulator is implemented as a PI-controller that outputs a DC current reference i^*_{dc}, which is then used to generate the active current reference i^*_{2d}. The latter is generated based on the power balance between the AC-side and the DC-side of the VSC. The current i^*_{2d} is fed to the VSC controller in the case of grid connected operation. In the case of island operation, i^*_{2d} is used to determine the duty ratio of the DC-chopper switch that is only activated in this case. The DC-chopper is incorporated in the DC-side of the VSC in order to dissipate the extra power that is produced during island operation by the energy source.

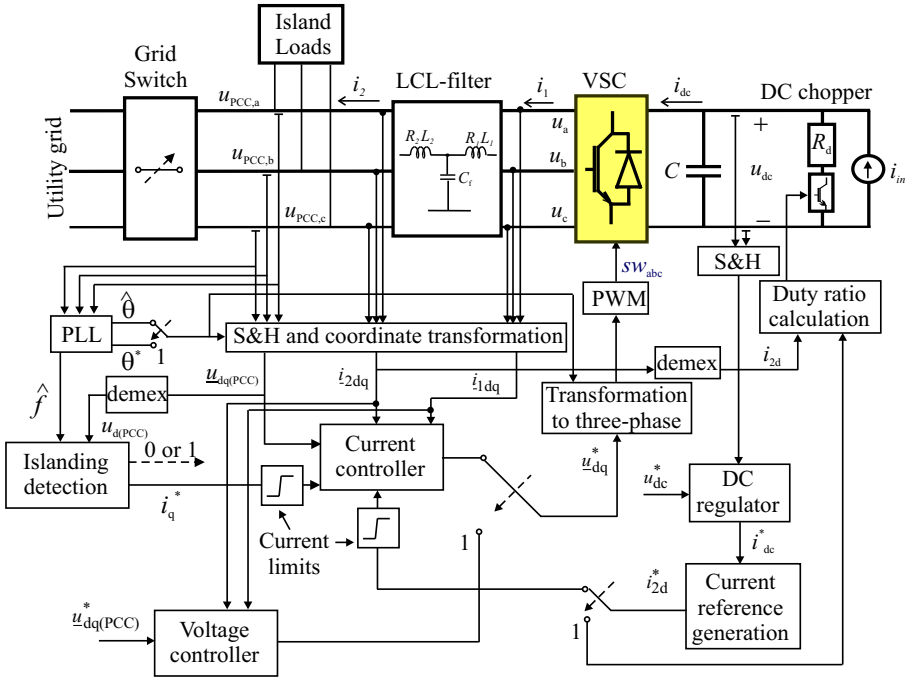

Fig. 2. System as seen by the DG. The dashed lines in the controller denote the islanding detection status.

Neglecting the switching losses of the VSC, the plant to be controlled is mainly the LCL-filter. It is described using three transfer functions; G_{p1}, G_{p2}, and G_{p3}, as

$$G_{p1}(s)=\frac{I_2(s)}{U_f(s)-U_{PCC}(s)}=\frac{1}{sL_2+R_2}$$
$$G_{p2}(s)=\frac{U_f(s)}{I_1(s)-I_2(s)}=\frac{1}{sC_f} \quad (1)$$
$$G_{p3}(s)=\frac{I_1(s)}{U(s)-U_f(s)}=\frac{1}{sL_1+R_1}$$

where s is the Laplace operator and U_f is the voltage over the filter's capacitor in the s-domain.

The DG main controller is the vector current controller that is shown in Fig. 3, which is devoted to the grid connected operation and is then modified as a voltage controller in case of island operation.

1) Vector current controller:

The current controller consists of three cascaded controllers. The inner controller G_{c3} is used for stabilization of G_{p3} and is designed based on dead-beat control. The two outer controllers G_{c2} and G_{c1} are used to stabilize G_{p2} and G_{p1} respectively. G_{c2} is implemented as a P-controller, while G_{c1} is implemented as a PI-controller where the integral part is added to eliminate the steady state error. G_{c1} is a two-degree of freedom controller, since it exploits the output signal of a Smith predictor (with a compensation gain k_{ps}) to cancel the time delay effect. The time-delay free plant transfer-function G_{pm} (incorporated in the Smith predictor) represents the LCL-filter model in steady state.

The three controllers are implemented in discrete form and described in the rotating dq-frame as follows

$$\underline{y}_{1dq}(k)=k_{p1}\left(\underline{\varepsilon}_{idq}(k)+\frac{T_s}{T_i}\sum_{n=0}^{k}\underline{\varepsilon}_{idq}(n)\right) \quad (2)$$

$$\underline{y}_{2dq}(k)=k_{p2}\,\underline{y}_{1dq}(k) \quad (3)$$

$$\underline{u}^{*}_{dq}(k+1)=\underline{u}_{fdq}(k)+(R_1+j\omega L_1)\underline{i}_{1dq}(k)+k_{p3}\,\underline{y}_{2dq}(k) \quad (4)$$

where

$\underline{y}_{1dq}$ is the output vector of G_{c1}, which represents the change in the capacitor voltage $\underline{u}_{fdq}$;

k is the sampling instant;

k_{p1} is the proportional gain of G_{c1};

T_i is the integral time of G_{c1};

$\underline{y}_{2dq}$ is the output vector of G_{c2}, which represents the required change in the converter side current $\underline{i}_{1dq}$;

k_{p2} is the proportional gain of G_{c2};

k_{p3} is the proportional gain of G_{c3}; and

$\underline{\varepsilon}_{idq}$ is the current error vector.

The faster the inner loop is in comparison with the outer loops, the better is the performance of the cascaded control system in the sense of the transient response. However, reduced gains for the outer controllers will reduce the overall bandwidth of the system. Hence, the inner controller gain is set to the dead-beat gain as

$$k_{p3}=\frac{L_1}{T_s}+\frac{R_1}{2} \quad (5)$$

And the inner controller parameters are given as ratios of k_{p3}, as reported in Table II.

TABLE II
DG MAIN CONTROLLER PARAMETERS

Symbol	Quantity	Value
f_s	Sampling frequency	5 kHz
k_{p1}	Outer controller gain	0.55
k_{p2}	Second controller gain	0.78
k_{p3}	Inner controller gain	2.6
T_i	Integral time	0.03 s
k_{ps}	Smith predictor gain	0.07

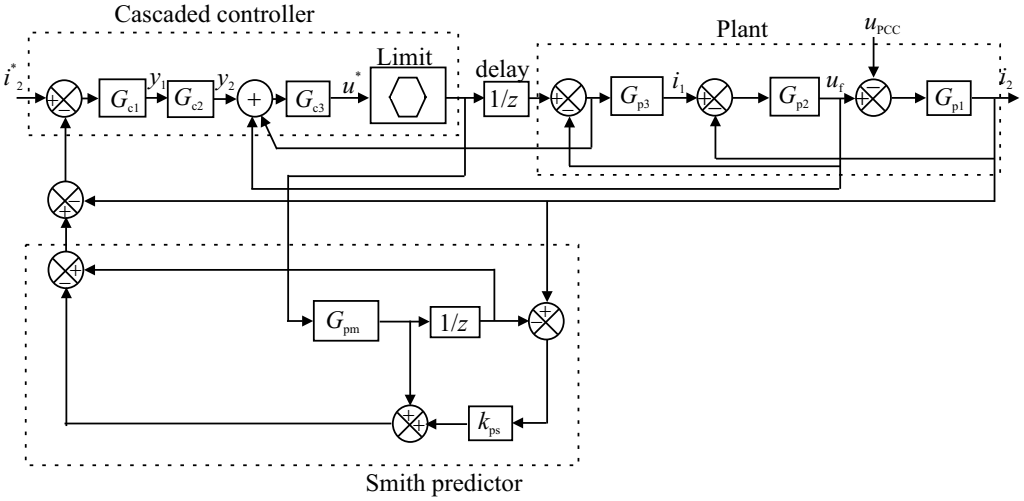

Fig. 3. Schematic diagram of the main current controller (z denotes the z-transform, thus $1/z$ denotes a delay of one sample).

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Converter-Interfaced Distributed Generation – Grid Interconnection Issues

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Division of Electric Power Engineering
Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2007

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To my family

Converter-Interfaced Distributed Generation –
Grid Interconnection Issues

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Abstract

Distributed generation (DG) with a converter interface to the grid is found in many of the green power resources applications. In this thesis, the control of a voltage source converter (VSC), as the DG front end, is in focus regarding the power quality problems that could appear at the connection point. The aims have been set to maintain a stable operation of the DG, in case of network disturbances, and to react in a corrective way during different grid operating conditions (e.g. in case of voltage dips). For this purpose, vector current controllers have been implemented with two different line filters; namely an inductance filter (L-filter) and an inductance-capacitance-inductance filter (LCL-filter). The controllers have incorporated: one sample time delay compensation, limitation of the reference voltage to avoid saturation, an integrator anti-windup, a DC-link voltage controller, a PCC voltage regulator, and an islanding detection algorithm.

The ride-through capability of the DG has been examined against a variety of possible voltage dips that could appear at the connection point. Moreover, the capability of the DG to compensate for the voltage at the connection point has been studied. Finally, the intentional islanding has been considered, where the DG is allowed to energize a part of the grid in case of the utility outage forming what is called an island.

The results found are that the effect of unbalanced voltage dips on the DC-link voltage ripple is minimized if the oscillating powers, produced during that period, are supplied by the grid side instead of the DC-side. Moreover, design equations have been derived in order to calculate the maximum currents that would flow through the VSC valves during voltage dips. These equations are to be used in designing VSC's with voltage dips ride-through capability. In addition, a neural-network based PLL, which extracts the phase angle of the fundamental component of the grid voltage, has been introduced in order to provide better performance in case of a DG with voltage compensation capability. Finally, combining the voltage regulator with the estimated frequency as a measure for islanding condition has, in this work, been found as an appropriate practice, to detect islanding, especially in the case of weak grids.

***Keywords**:* distributed generation, harmonics, intentional islanding, L-filter, LCL-filter, power quality, strong grid, vector control, voltage dips, voltage regulation, VSC, weak grid.

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Fainan Abdul-Magueed Hassan

Gothenburg, Sweden,

September, 2007.

Table of Contents

Chapter 1

Introduction

1.1 Motivation

The consumption of electrical energy is an ever growing need worldwide. Yet, growing in tandem to it are concerns about environmental pollution, global warming and the steady depletion of fossil fuels. Electricity generation from renewable resources might be considered as a feasible solution for the next generations [1].

Traditional power systems implement large power generation plants that produce most of the power, which then is transmitted to large consumption centres and further distributed between different customers. This power system design structure has, at some locations, started to change [2] towards new scenarios at which distributed generation (DG) units are spread throughout the distribution network, as shown in Fig. 1.1 for two possible locations. These DGs utilize renewable resources such as wind turbines, photovoltaics, biomass, small hydro-turbines … etc. Beside their environmental benefits, DGs offer a low-cost way for the energy flow into the market since they do not imply substantial transmission losses due to their location near to the customers [3]. Moreover, they could present a reliable and uninterruptible source for the customers especially in rural areas [4] and micro grids [5]. In addition, a possibility where the DG could be beneficial is if it could help to supply load during contingencies until the utility can build up additional delivery capacity [6].

More advantages are introduced using power electronics interfaced DGs [7]. For instance, converter interfaced DGs can be designed to provide ancillary services to the utility; such as reactive power support, load balancing, voltage support, and harmonic mitigation [3]. Moreover, such DGs can be more energy efficient in the sense that they can provide more

energy production, more smooth power production (less dependent on the prime source variations), and controlled energy storage [9].

In addition to the above advantages, the integration of DGs is, to a large extent, owed to political decisions in many countries. For instance, the Swedish government has introduced a legislation (2003:113), which intended to encourage and increase the proportion of electricity produced from renewable resources [8]. The objective is that the amount of electricity produced from renewable resources will provide additional power of about 6.5% of the present total production by the year 2010.

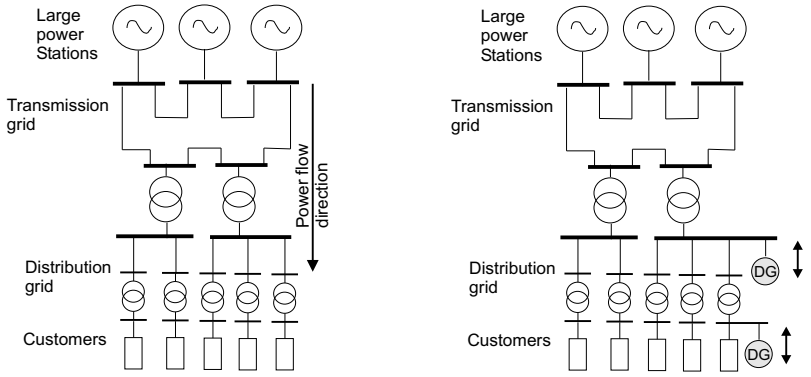

Fig. 1.1 Traditional power system (left) and penetration of distributed generation (right). The arrows present the power flow direction.

Even though large-scale implementation of DGs has several driving forces as mentioned above, there are major challenges concerning network interconnection issues that have to be solved. Grid connection of DGs is considered from two main prospects: power-system prospective and DG-technology prospective. As it is an essential part for the integration of DGs to achieve a reliable and improved performance of the power system, the DG interface to the grid is of focus in this work.

1.2 Background and related work

Background

Power conversion systems of distributed generation (DG) vary according to the nature of the input energy source. They may be implemented by using partially rated power electronics interface, as in wind turbine systems with doubly fed induction generators, or with fully rated power electronics interface [7]. The latter interface is the dominating one in applications related to fuel cells, solar cells, micro turbines and wind turbine systems [9]. There can be one or more power conversion stages in order to adjust the power of the energy source with the grid requirements, as shown in Fig. 1.2 [9]. With DC energy sources, the power electronics interface may consist of one DC/AC converter, or an intermediate DC/DC conversion stage can be added to achieve a specific goal, e.g. in order to regulate the output voltage so that the maximum available power is extracted [9]. The same is valid for AC sources, where they have to be adjusted to match the grid requirement by a DC intermediate stage. An energy storage unit could also be connected in the DC stage to adjust the energy injected into the utility grid in all operating conditions. The focus here will be on DG systems with a DC/AC power converter as a front end, where the DC-link voltage is either controllable or constant and the primary source input power is constant. The power converter to the grid enables a fast control over active and reactive power and could perform voltage and frequency control [10], [11]. Observe that, in order to control the active power, the primary source needs also to be controllable or an energy storage should be provided.

Voltage source converters (VSCs) using insulated gate bipolar transistor (IGBT) switches that are controlled by pulse width modulation (PWM) are used on the grid side at medium/high voltage due to their high controllability and low losses [12], [13], [14]. The good controllability promotes the use of the VSCs in grid connected applications to provide good power quality. An inherent part of a VSC is a filter inductor (L-filter), which is used to minimize the current harmonics injected into the grid [15] - [20].

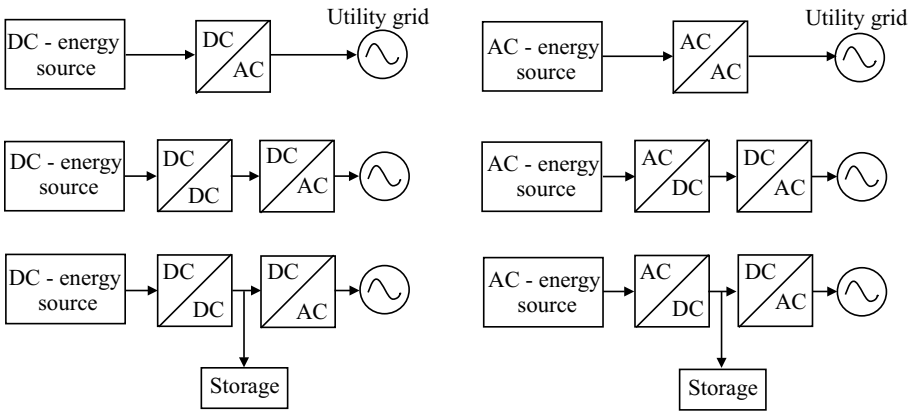

Fig. 1.2 Full-rated power electronics interfaced DG systems.

Like most of the power electronics equipment, an important drawback of using VSCs is their sensitivity to voltage disturbances, e.g. voltage dips [21]. In order to keep the DC-link voltage constant and minimize the grid current amplitude and harmonics during faults, the VSC controller is required to have two main functions: DC-link voltage regulation and current control. Most conventional current controllers have been designed under the assumption of balanced grid voltages [16]. These controllers show undesirable current control characteristics under unbalanced conditions because the current references are distorted by a second-order harmonic [16]. This is due to the negative-sequence voltage in the three-phase domain, which translates into a sinusoidal signal having a frequency of twice the grid frequency in a *dq*-frame synchronized with the positive-sequence voltage.

Related work

A comparison between different types of current controllers (CCs) for shunt-connected VSC based on their transient operation in case of voltage dips is presented in [17]. It has been shown that the dual vector current controller (DVCC) shows the best performance regarding grid current control and DC-link voltage regulation [16], [17]. This controller uses two different vector current controllers for the two sequence components,

together with a DC-link voltage controller based on the instantaneous active and reactive power theory.

Due to the PWM switching of voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [22]-[27]. Inserting an LCL-filter between the grid and the VSC eliminates high frequency harmonics even with lower switching frequency. Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. Damping methods are extensively addressed in literature. In [23] a resistance is used in series with the filter capacitor to passively damp the resonance. This resistance increases the system losses and decreases the efficiency of the filter. Instead, methods to actively damp the resonance are adopted as in [24], [25], [28]. In [25], a comparison between none-damped, passively-damped and actively-damped systems is carried out using Bode plots. It has been concluded that the active damping reduces the resonant peak as effectively as the passive damping. In [24], three cascaded controllers are used with the reference grid current generated from a DC voltage controller. The converter current and capacitor voltage are predicted. Moreover, two active resistances virtually connected in series with the filter inductor resistances are considered in the controller dead-beat gains. However, the use of these resistances is not justified. In [22], and [26] controllers with no damping are proposed. This has been proposed in [22] by controlling the grid current instead of the converter current and the proper choice of the filter parameters. However, by introducing a one sample time delay the system has been unstable acquiring the passive damping. In [26], two control loops are used: an outer current control loop and an inner capacitor voltage control loop. The latter is used to stabilize the controller and in the same time damp the resonance. The effect of adding a time delay has not been considered there as well.

The voltage compensation capability of VSCs' controllers has been also discussed in the literature to overcome the problem of having a decreased voltage at the connection point of the DG due to load/system dynamics [30]-[35], or to mitigate power quality problems [37], [38]. However, the effect of

the grid power quality on the phase locked loop (PLL), which is used to extract the grid phase angle, and on the compensation capability has not been treated in the literature. Moreover, in most of the literature the VSC is assumed to be either not injecting active power or has a controllable active power, which provides a wider compensation range.

One of the important capabilities of the DGs is to locally detect a grid outage condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, to prevent island operation. This capability has been discussed in the literature [39]- [45], where the transfer from grid-connected to island operation has been studied assuming a strong grid. The transfer from island to grid-connected mode is not much discussed. In [46], the load has been connected to the capacitor of the LCL-filter, at which its voltage is controlled in all the operating modes, to attain perfect transition without any transients. In [10], the DG was set into idle mode in case of grid recovery until the synchronization is achieved between the grid voltage and the DG voltage.

1.3 Purpose of the thesis and contributions

The main goals of the thesis and the contributions related to them are:

Goal 1: To determine the interface requirements and the capabilities of DGs with a voltage source converter (VSC) as a front end. For this purpose, two line filters are to be considered at the connection point of the DG; namely inductance line filter (L-filter) and inductance-capacitance-inductance line filter (LCL-filter). Vector current controllers are to be implemented for both systems.

Contribution 1: The derivation of the current reference generation equations, for the LCL-filter system, regarding the oscillating powers that are produced during the unbalanced grid voltage and compensating for them in two different ways. This has been presented in Section 2.5 and Paper A and Paper B.

Goal 2: To study the effect of voltage dips on the converter-interfaced DG and the requirements for ride-through capability.

Contribution 2: The study of all possible types of voltage dips that could appear at the terminals of a DG unit with both L-filter and LCL-filter systems. And, the derivation of the equations of maximum currents that would flow through the DG's converter switches. The main results of this point has been published in Paper B and explained in Section 3.5.

Goal 3: To study the effect of the other power quality problems on the DG operation, and how the DG controller could react in a corrective way to support the grid and provide better power quality at the connection point.

Contribution 3: A synthesis of a neural network based PLL has been proposed to reduce the error due to the voltage distortion, which has resulted in better compensation capability for the DG. This is shown in Paper E and in Section 4.5.

Goal 4: To study the possibility of intentional islanding for very weak grids.

Contribution 4: A passive detection algorithm that combines both the estimated frequency and the voltage regulator has been proposed to detect the islanding condition, especially in a weak grid. This has been shown in Section 5.4 and in Paper F and G, for various loads.

1.4 Thesis outline

The fundamental theory of the work is explained in details in **Chapter 2**. In that chapter the vector current controllers (VCC) for both the L-filter and the LCL-filter VSC-interfaced DG-systems are presented. The dual vector current controller (DVCC) has been implemented, for both systems, in order to achieve better current reference tracking in case of grid-voltage imbalance. Moreover, current reference equations are derived in such a way that they alleviate the DC-link ripples.

In **Chapter 3**, the voltage dips that could appear at the DG terminals are considered. An investigation of the ride-through capability is provided regarding the possible maximum currents that would flow through the VSC switches, and also regarding the DC-link voltage ripples. In addition, the maximum currents that would result during the dip period were obtained

using design equations that have been derived for various dips. Moreover, the DG system, both with the L-filter and the LCL-filter, has been examined for all possible voltage dips that could occur at its terminals. Recommendations of oversizing of the DG have been drawn as a consequence of that study.

If oversizing is not a possibility, the voltage regulation capability might appear as another possibility to correct the terminal voltage instead of riding through the voltage dip period. This is then discussed in **Chapter 4**. This capability might also be beneficial in case of operation in weak grids, where the voltage level is not constant and is dependent on the loads. Moreover, by compensating the grid voltage most of the power quality problems are mitigated. In this chapter, the voltage regulation capability is related to the performance of the phase locked loop (PLL) that estimates the phase angle of the grid voltage. A PLL that extracts the fundamental component of the grid voltage has been implemented using neural network technique.

In **Chapter 5**, the outage (and recovery) of the grid voltage has been considered, regarding the ability to keep the DG into operation to supply sensitive or critical loads. The main conclusions relating the different chapters and the possible future work considering the same topic are reported in **Chapter 6**.

1.5 Publications

The work in this thesis has resulted in eight publications, as shown in Fig. 1.3. The papers, designated in the figure from A to G, are supplemented at the end of this thesis with the same designation. The publications are also listed below with short description.

Journal papers

[J-1] F. Magueed, A. Sannino, and J. Svensson, "Design of Robust Converter Interface for Wind Power Applications," in *Wind Energy Journal, special issue on Electrical Integration of Wind Power*, vol. 8, no. 3, 2005, pp. 319 – 332.

In this paper the study of all possible voltage dips that could occur at the terminal of the DG is studied. This paper is designated as "Paper A" and supplemented at the final part of the thesis.

[J-2] F. Magueed, and T. Thiringer, "Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC," *submitted to Electrical Power Quality and Utilization Journal*.
The neural network based PLL has been presented here and compared with the positive sequence based PLL. This paper is designated as "Paper E" and supplemented at the final part of the thesis.

[J-3] F. Magueed, G. Olsson, and T. Thiringer, "Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation," *submitted to IEEE trans. on Power Delivery*.
An active islanding detection method is proposed, which consists of an under/over frequency passive detection algorithm, a PCC-voltage regulator and a DG reactive current limiter. This paper is designated as "Paper G" and supplemented at the final part of the thesis.

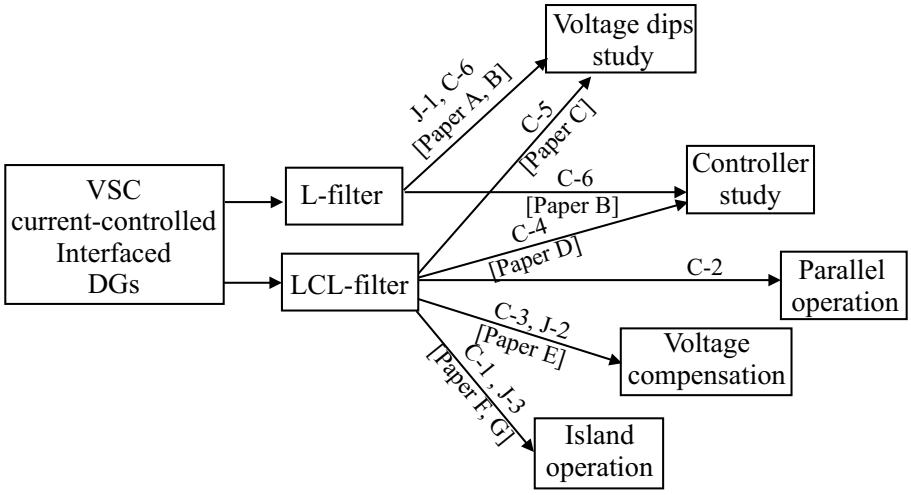

Fig. 1.3 Thesis outline with the resulting publication.

Conference papers (peer reviewed)

[C-1] F. Magueed, and J. Daalder, "Operation of Distributed Generation in Weak Grids with Local Critical Load," at *IEEE Annual Industrial*

Electronics Conference (IECON'06), Paris, France, November 7-10, 2006.

The passive islanding detection algorithm has been presented here with the focus on the operation in weak grids. This paper is designated as "Paper F" and supplemented at the final part of the thesis.

[C-2] F. Magueed, and J. Daalder, "Parallel Operation of Distributed Generation in Weak Distribution Systems," at the *12th International Power Electronics and Motion Control Conference (EPE-PEMC'06)*, Slovenia, August 30 - September 1, 2006, pp. 531 – 536.

A discussion of the voltage compensation limits and the possible parallel operation of DGs to provide better compensation capability is introduced.

[C-3] F. Magueed, and H. Awad, "Voltage Compensation in Weak Grids Using Distributed Generation with Voltage Source Converter as a Front End," at the *6th International Conference on Power Electronics and Drive Systems (PEDS'05)*, Kuala Lumpur, Malaysia, Nov 28 - Dec 1, 2005, pp. 234 – 239.

The main voltage regulator is presented here, with the capability to compensate for voltage dips at the grid.

[C-4] F. Magueed, and J. Svensson, "Control of VSC Connected to the Grid through LCL-Filter to Achieve Balanced Currents," at the *IEEE Industry Applications Society 40th Annual Meeting (IAS'05)*, Kowloon, Hong Kong, October 2-6, 2005.

The control of the VSC is presented here, in case of unbalanced voltage dips at the grid, to provide balanced DG currents. This paper is designated as "Paper D" and supplemented at the final part of the thesis.

[C-5] F. Magueed, J. Svensson, and A. Sannino, "Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage conditions," in *Proc of Power Tech Conference (PT'05)*, St. Petersburg, Russia, June 27-30, 2005.[1]

The performance of the LCL-filter system has been discussed regarding the voltage dips at the grid. This paper is designated as "Paper C" and supplemented at the final part of the thesis.

[1] This paper has been awarded ***High quality paper certificate*** for the presentation from 2005 IEEE Power Tech conference (June 27-30 2005).

[C-6] F. Magueed, A. Sannino, and J. Svensson, "Transient Performance of Voltage Source Converter under Unbalanced Voltage Dips," in *Proc. of Power Electronics Specialists Conference (PESC'04)*, Aachen, Germany, June 20-25 2004, pp. 1163 – 1168.

The study of voltage dips with phase angle jumps and the compensation of the oscillating powers using two different ways have been presented in this paper. This paper is designated as "Paper B" and supplemented at the final part of the thesis.

Chapter 2

Power Electronics Interfaced Distributed Generation – Controller Description

In this chapter, a general description of the power conversion systems, i.e. power electronics interface, for distributed generation is given. Two distributed generation systems are considered with two different line filters; namely an inductance line filter and an inductance-capacitance-inductance line filter, and a voltage source converter as a front end for the energy source. Vector current controllers are proposed for the two systems. The description of the controllers is given in details. Moreover, the generation algorithm for the current references is provided.

2.1 Current-controlled voltage source converters

Current controllers are preferred for shunt connected voltage source converters (VSCs) in order to increase stability of the closed loop and to decrease the time response in case of load transients [19]. Accordingly, a vector current controller (VCC) is considered throughout this work in order to obtain a high performance controller. In a VCC, the active and reactive currents (consequently powers) can be controlled independently. And, as indicated above, a high bandwidth controller with low cross-coupling effect between active and reactive currents can be achieved [20].

In Fig. 2.1, a scheme of the VSC system connected to the grid via a line filter along with the VCC is shown. Since the application of the distributed generation utilizing renewable resources is considered, the variation of the input current i_{in} is relatively slow compared to the response time of the controller. Hence, i_{in} is modelled as a constant current source. In addition,

the DC-link voltage should be regulated to maintain a constant voltage in case of grid voltage variations (e.g. voltage dips). The DC voltage regulator is implemented as a proportional-integral (PI) controller, where the measured DC capacitor voltage u_{dc} is compared with its reference value u_{dc}^{*} and the error signal is used to produce a reference DC current i_{dc}^{*} according to

$$i_{\mathrm{dc}}^{*} = \Delta u_{dc} k_{\mathrm{pdc}} \left(1 + \frac{1}{s T_{\mathrm{idc}}} \right) \tag{2-1}$$

where

k_{pdc}, T_{idc} are the proportional gain and integral time of the PI-controller respectively with their values as given in Appendix D;

s is the Laplace operator; and

$\Delta u_{\mathrm{dc}} = u_{\mathrm{dc}} - u_{\mathrm{dc}}^{*}$.

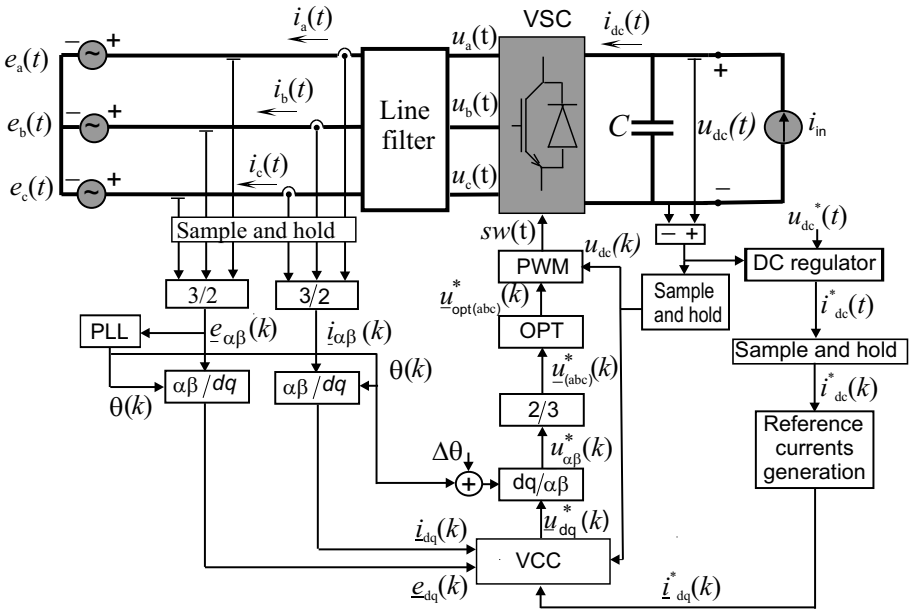

Fig. 2.1 Schematic diagram showing VSC, grid, filter and controller.

The signal flow from the power circuit to the VCC is as follows. The three-phase AC currents and voltages are first sampled and transformed into

the $\alpha\beta$-stationary frame[2]. The resulting rotating vectors $\underline{e}_{\alpha\beta}$ and $\underline{i}_{\alpha\beta}$ are then transformed into the rotating *dq*-frame that is synchronized with the grid voltage using a phase-locked-loop (PLL) that extracts the grid voltage angle θ. The *dq*-vectors of the measured voltages and currents, $\underline{e}_{\mathrm{dq}}$ and $\underline{i}_{\mathrm{dq}}$ respectively, are then used along with the reference current vector $\underline{i}^{*}_{\mathrm{dq}}$ by the VCC to produce the reference voltage vector $\underline{u}^{*}_{\mathrm{dq}}$. The different coordinate transformations are provided in Appendix A, where the *d*-component refers to the real value while the *q*-component refers to the imaginary value of a vector.

The reference currents are produced in such a way as to decrease the DC-link voltage ripple using a "reference currents generation" algorithm that uses the signal coming from the DC-link voltage regulator, and is explained later in this chapter. The reference voltage vector is then transformed to a vector in the $\alpha\beta$-frame using a transformation angle of $\theta+\Delta\theta$, where $\Delta\theta$ compensates for the transformation angle error due to one sample calculation time delay of the controller. The vector $\underline{u}^{*}_{\alpha\beta}$ is then transformed into three-phase control signals. Those signals are then used in the PWM modulator to produce the switching pattern for the VSC. The PWM is optimized to increase the maximum output voltage of the converter without increasing the DC-link voltage [12], [14]. The block "OPT" injects a zero sequence voltage into the control signals. Due to the absence of a neutral wire, the added zero sequence waveforms are cancelled out.

It should be mentioned that the design of the VCC is different for the power circuit with an inductance line filter from the power circuit with inductance-capacitance-inductance line filter, since both circuits have different time and frequency behaviors. Also the generation of reference currents is different for the two filter configurations. This is shown in the next sections.

[2] The coordinate transformation matrices are explained in Appendix A.

2.2 Vector Current Controller with inductance line filter

An inductance line filter is first considered. The plant in Fig. 2.2 represents the filter, the PWM, and the VSC. The last two, however, are assumed to be ideal, having a transfer function of 1. The plant transfer function in the *s*-domain is then represented as

$$G_{\mathrm{pl}}(s) = \frac{1}{sL_{\mathrm{f}} + R_{\mathrm{f}}} \tag{2-2}$$

where

L_{f} is the filter inductance; and

R_{f} is the filter resistance.

The controller design is based on deadbeat control. The measured voltage and current vectors are used to calculate the feedforward vector $\underline{FF}_{\mathrm{dq}}$ as

$$\underline{FF}_{\mathrm{dq}}(k) = \underline{e}_{\mathrm{dq}}(k) + \underline{i}_{\mathrm{dq}}(k)(R_{\mathrm{f}} + \mathrm{j}\omega L_{\mathrm{f}}) \tag{2-3}$$

where

ω is the angular frequency of the grid voltage;

k is the sampling instant; and

j is the imaginary unit.

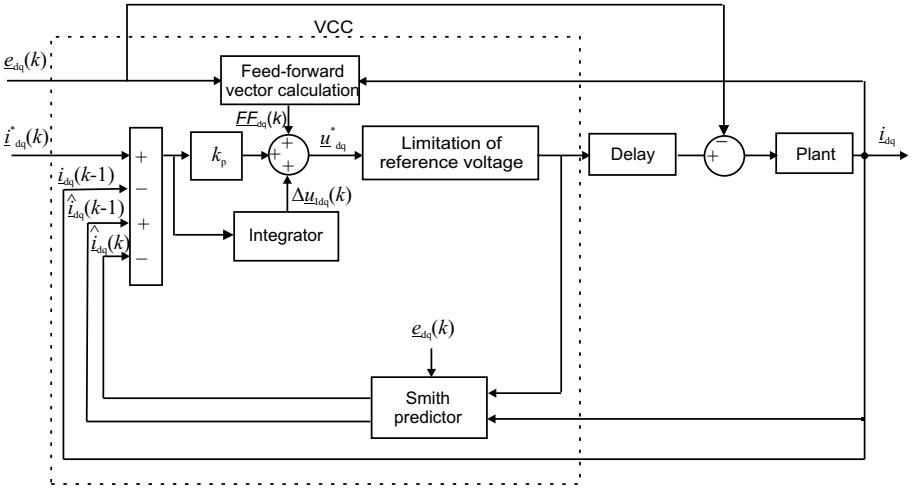

Fig. 2.2 Deadbeat based vector current controller (VCC) for DG with L-filter.

The change in the current reference is met by a change in the voltage reference that is produced by adding $\underline{FF}_{\mathrm{dq}}$ to the output of a PI-controller with a proportional gain k_p, also called here dead-beat gain. The dead-beat strategy has been described in [20]. The Dead-beat gain is given in terms of the filter parameters as

$$k_{\mathrm{p}} = \frac{L_{\mathrm{f}}}{T_{\mathrm{s}}} + \frac{R_{\mathrm{f}}}{2}. \tag{2-4}$$

An integral part $\Delta\underline{u}_{\mathrm{idq}}$ is needed to remove the static errors caused by non-linearity, noisy measurements and non-ideal components. The generated reference voltage is then calculated as

$$\underline{u}^{*}_{\mathrm{dq}}(k+1) = \underline{FF}_{\mathrm{dq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idq}}(k). \tag{2-5}$$

The integral part is implemented as

$$\Delta\underline{u}_{\mathrm{idq}}(k+1) = \Delta\underline{u}_{\mathrm{idq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{i}} \tag{2-6}$$

where k_{i} is the integration constant, which can be written as

$$k_{\mathrm{i}} = \frac{k_{\mathrm{p}}T_{\mathrm{s}}}{T_{\mathrm{i}}} \tag{2-7}$$

where T_{i} is the integral time constant, which is chosen to be equal to the L-filter time constant $T_{\mathrm{i}} = \frac{L_{\mathrm{f}}}{R_{\mathrm{f}}}$, and T_{s} is the sampling time.

The current error vector $\underline{\varepsilon}_{\mathrm{idq}}$ is described by

$$\underline{\varepsilon}_{\mathrm{idq}}(k) = \underline{i}^{*}_{\mathrm{dq}}(k) - \underline{i}_{\mathrm{dq}}(k-1) + \hat{\underline{i}}_{\mathrm{dq}}(k-1) - \hat{\underline{i}}_{\mathrm{dq}}(k) \tag{2-8}$$

which accounts for a one sample time delay in the measured current signal due to the calculation time of the digital controller. This delay has been compensated for using the estimated current $\hat{i}_{\mathrm{dq}}$ at two successive instants,

which is calculated by a Smith predictor [48], [76]. The Smith predictor is implemented in a way analogous to a state observer[3], as proposed by [20], which means running a model of the plant in parallel to the plant itself. In steady state, the estimated and actual currents should be equal, hence $\underline{i}_{\mathrm{dq}}(k-1)=\hat{\underline{i}}_{\mathrm{dq}}(k-1)$ in (2-8), which cancels the time delay effect.

The output reference voltage command is also limited to be inside the control region, which is described by a hexagon composed of six equilateral triangles with a side length of $\sqrt{2/3}u_{\mathrm{dc}}$. In this work the minimum amplitude error (MAE) limiting method has been adopted [20]. In this method a new reference voltage vector on the hexagon boundary that is closest to the original reference vector is chosen as explained by Fig. 2.3. This is done by mapping the voltage reference into new coordinates *xy*. The *xy*-coordinate position depends on the number of the sector in the hexagon that contains the voltage reference. The reference voltage vector in the new coordinates u_{xy}^{*} is obtained as

$$\underline{u}_{\mathrm{xy}}^{*}=\underline{u}_{\alpha\beta}^{*}e^{-\mathrm{j}\theta_{\mathrm{xy}}} \tag{2-9}$$

where θ_{xy} is the angle between the α-axis and the *x*-axis and is calculated as

$$\theta_{\mathrm{xy}}=\left(1+2(n-1)\right)\pi/6 \tag{2-10}$$

where *n* is the sector number at which the reference vector lies in the hexagon.

The components of the limited reference voltage vector are calculated from Fig. 2.3 as

$$u_{\mathrm{x}}=\frac{u_{\mathrm{dc}}}{\sqrt{2}} \tag{2-11}$$

[3] The use of the Smith predictor is described in more details in Paper D.

$$u_{\mathrm{y}} = \begin{cases} u_{\mathrm{y}}^{*} & \left|u_{\mathrm{y}}^{*}\right| \le \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \\ sign(u_{\mathrm{y}}^{*}) \cdot \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} & \left|u_{\mathrm{y}}^{*}\right| > \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \end{cases} . \tag{2-12}$$

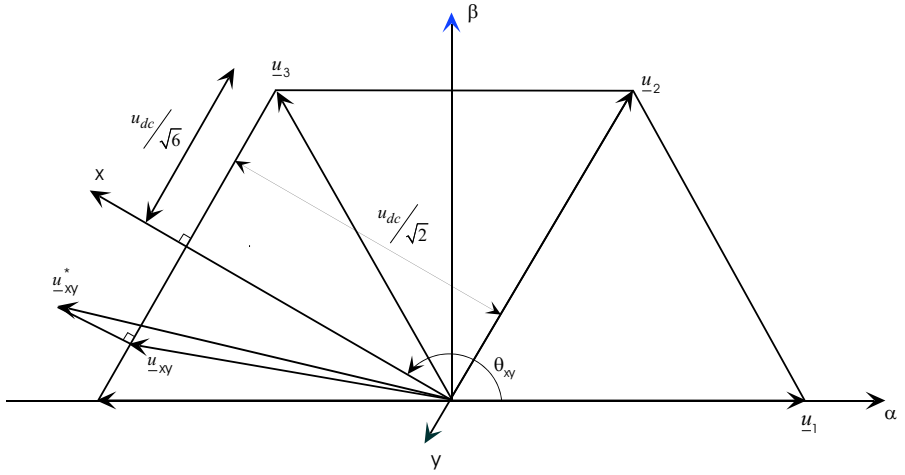

Fig. 2.3 Principle of the minimum amplitude error method.

It is worth noting here that using the limited voltage reference as an input for the Smith predictor, as shown in Fig. 2.2, is important in providing an anti-windup property for the controller, which is useful in case of increased current steps.

The time domain performance of the controller is tested in Fig. 2.4, for the case of a substantial positive active current step, which is considered the worst operational case since it leads the voltage to the saturation area. Due to the high current step of 1.5 p.u. that has been applied at 0.2 s, the controller will go into the voltage reference limitation algorithm, at which the reference voltage will be limited as shown by the same figure. Since the demanded reference voltage, required to achieve the current step, has not been reached, the dead-beat is not accomplished. Hence, it will take several samples for the current to reach its reference value. As shown by the figure, the current will accomplish the step in 2 ms. The figure also shows the cross-coupling effect

on the *q*-component of the current. To eliminate this coupling effect, i_{q}^{*} might be modified to counteract the effect of the active current step [20]. However, this will not be considered here since the reference *q*-component current will be implemented later to compensate for various power quality problems at the grid.

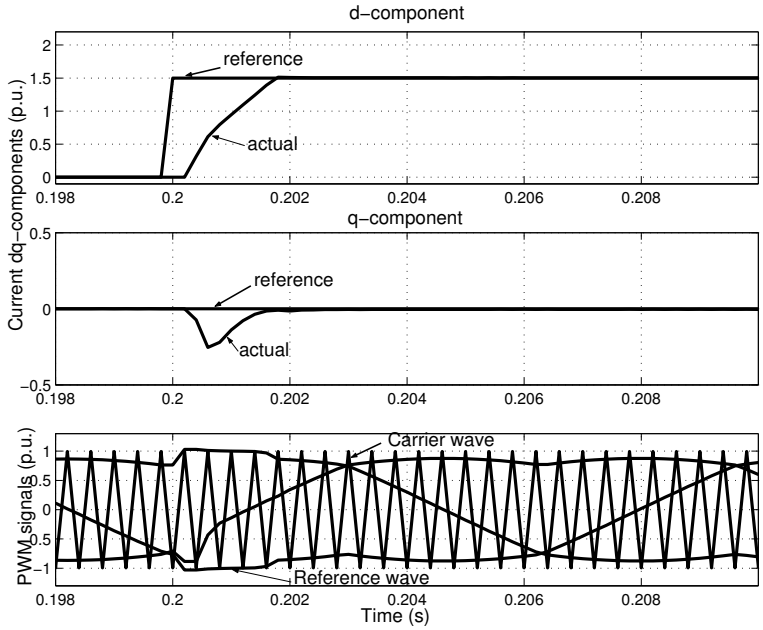

Fig. 2.4 Active current (upper), reactive current (middle), and PWM signals (lower), due to a step in i_{d}^{*} from 0 to 1.5 p.u.

2.3 Dual vector current controller (DVCC)

In case of an unbalanced grid voltage, the voltage vector in the *dq*-frame has oscillations at a frequency of twice the fundamental frequency due to the negative sequence that exists in the grid voltage. That will lead to oscillations in the injected currents to the grid. To deal with that situation a dual vector current controller (DVCC) [18] can be used. The DVCC consists

of two separate VCCs, one for controlling the positive-sequence voltage and the other for controlling the negative-sequence voltage. This controller synthesis has proved to give the best performance regarding grid current control and DC-link voltage regulation [17]. A simplified scheme for the DVCC is shown in Fig. 2.5.

The positive sequence PI-controller is described in the positive *dq*-frame (*dqp*-frame), which rotates in the positive direction, as

$$\underline{u}^{*}_{\mathrm{dqp}}(k+1) = \underline{FF}_{\mathrm{dqp}}(k) + \underline{\varepsilon}_{\mathrm{idqp}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqp}}(k) \qquad (2\text{-}13)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqp}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqp}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqp}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The negative sequence PI-controller is described in the negative *dq*-frame (*dqn*-frame), which rotates in the negative direction, as

$$\underline{u}^{*}_{\mathrm{dqn}}(k+1) = \underline{FF}_{\mathrm{dqn}}(k) + \underline{\varepsilon}_{\mathrm{idqn}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqn}}(k) \qquad (2\text{-}14)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqn}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqn}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqn}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The decomposition of the supply voltage into positive and negative sequence components is performed using the delayed signal cancellation (DSC) algorithm, which has been first proposed in [77]. This algorithm is implemented in the *dq*-frame, which rotates in the positive direction, in the same way as suggested in [17]. In this frame, the positive sequence is a constant vector (constant amplitude and fixed direction), while the negative sequence is a rotating vector, which rotates with twice the line frequency in the opposite direction, as compared with the positive sequence.

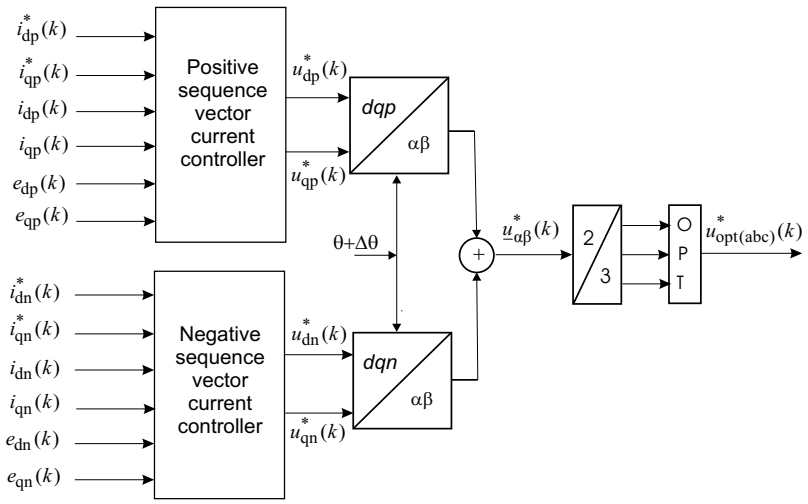

Fig. 2.5 Simplified block diagram of dual vector current controller (DVCC).

In the DSC the measured supply voltage, in the *dq*-frame, and the same signal, delayed by one-quarter of a fundamental frequency period, are considered. Delaying the signal gives a vector composed by the same positive sequence component and a negative sequence component which has equal amplitude but opposite sign. Therefore, if the signal delayed by one-fourth of period is added to the measured supply voltage, the negative sequence voltage will be removed.

The positive sequence voltage vector can thus be extracted from the measured values as

$$\underline{e}_{\mathrm{dqp}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) + \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-15}$$

where T is the period at the fundamental frequency.

The negative sequence can be obtained in the positive rotating plane, as follows

$$\underline{e}_{\mathrm{dqn}_{(\mathrm{p})}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) - \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-16}$$

which is then transformed into the negative rotating plane by transforming it into the $\alpha\beta$-frame and back into the *dqn*-frame using the opposite angle.

The time domain response of the DVCC is compared with the time domain response of the VCC when a grid voltage of 40% imbalance ratio is applied. Moreover, a step in the active current reference is applied at 0.25 s. The injected current is oscillating in the case of using the VCC, as shown in Fig. 2.6, while better tracking is achieved using the DVCC.

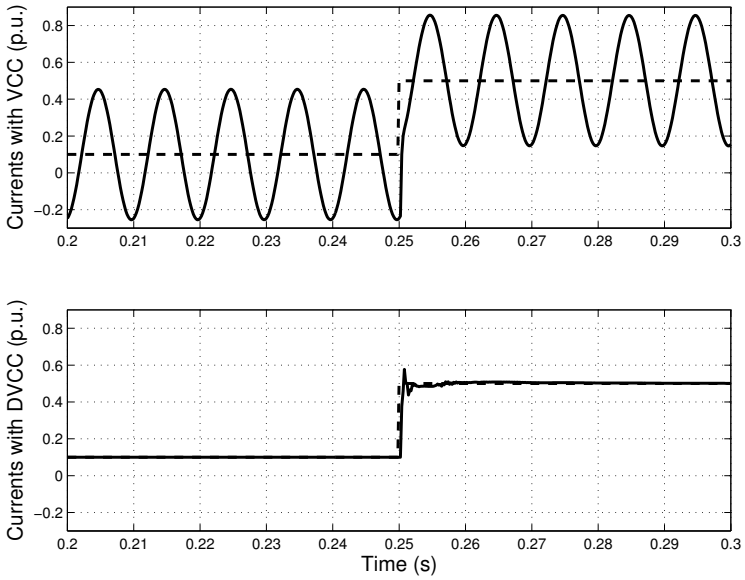

Fig. 2.6 Active grid current i_d (solid) and reference current i^*_d (dashed); with VCC (upper) and DVCC (lower).

2.4 Current reference generation with inductance line filter

In the case of a controllable DC-link voltage, proper current references should be generated in order to improve the performance of the VCC. Two performance measures are considered, which are the minimization of the DC-link voltage ripple and the decrease of the AC currents amplitudes and/or harmonics. The reference currents generation algorithm is based on

the instantaneous power theory [80]. The active power on the AC side of the converter, p_1, is considered equal to the active power on the DC side, P_{dc}, neglecting the switching losses. The power balance equation can be expressed as

$$\begin{bmatrix} p_1 \\ q_1 \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \Delta p \\ \Delta q \end{bmatrix} \tag{2-17}$$

where p_1 and q_1 are the instantaneous active and reactive powers at the AC-side of the converter respectively. The terms Δp and Δq are active and reactive powers dissipated by the filter respectively, and can be calculated instantaneously as

$$\Delta p = R_f \left(i_d^2 + i_q^2 \right) \tag{2-18}$$

$$\Delta q = \omega L_f \left(i_d^2 + i_q^2 \right). \tag{2-19}$$

The instantaneous active power p_2 and reactive power q_2 at the grid are calculated as:

$$\begin{aligned} p_2 &= e_d i_d + e_q i_q \\ q_2 &= -e_d i_q + e_q i_d \end{aligned}. \tag{2-20}$$

To achieve unity power factor, the reactive power at the grid side $q_2 = q_1 - \Delta q$ is nullified. The current references are then calculated using (2-17) as follows

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \end{bmatrix}. \tag{2-21}$$

2.5 Current reference generation for inductance line filter and unbalanced grid voltage

For the DVCC, current reference signals should be provided in the positive and the negative *dq*-coordinates. The derivation[4] is carried out in the same way as for the VCC. The current references are calculated using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ q_{\mathrm{ac},2} \\ p_{\mathrm{s}2,1} - \Delta p_{\mathrm{s}2} \\ p_{\mathrm{c}2,1} - \Delta p_{\mathrm{c}2} \end{bmatrix} \tag{2-22}$$

where the instantaneous active power p_2 and reactive power q_2 at the grid are

$$\begin{aligned} p_2(t) &= p_{\mathrm{ac},2} + p_{\mathrm{c}2,2}\cos(2\omega t) + p_{\mathrm{s}2,2}\sin(2\omega t) \\ q_2(t) &= q_{\mathrm{ac},2} + q_{\mathrm{c}2,2}\cos(2\omega t) + q_{\mathrm{s}2,2}\sin(2\omega t) \end{aligned} \tag{2-23}$$

with the following subscripts notations

ac - stands for the power at the fundamental frequency;

2 - stands for the grid side.

1 - stands for the AC converter side;

c2 - stands for the cosine component of a power that is oscillating with double the fundamental frequency; and

s2 - stands for the sine component of a power that is oscillating with double the fundamental frequency.

The power loss through the filter is encountered for in (2-22) by the terms Δp, $\Delta p_{\mathrm{s}2}$, and $\Delta p_{\mathrm{c}2}$.

Equation (2-22) has been considered in two ways, which are referred to as case 1 and case 2. The injected reactive power $q_{\mathrm{ac},2}$ to the grid is assumed to be zero in both cases.

[4] Details are given in Paper A and Paper B.

Case 1- The oscillating powers flow from the VSC side to the filter

Assuming that the converter supplies the oscillating power to the filter, and neglecting the converter losses which means $p_{ac,1}$ is equal to P_{dc}, the following equations will describe the different powers

$$P_{c2,1} = \Delta P_{c2},\ P_{c2,2} = 0 \tag{2-24}$$

$$P_{s2,1} = \Delta P_{s2},\ P_{s2,2} = 0 \quad . \tag{2-25}$$

Substituting in (2-22), the reference currents are calculated as

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qn} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{2-26}$$

Using (2-26), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.7.

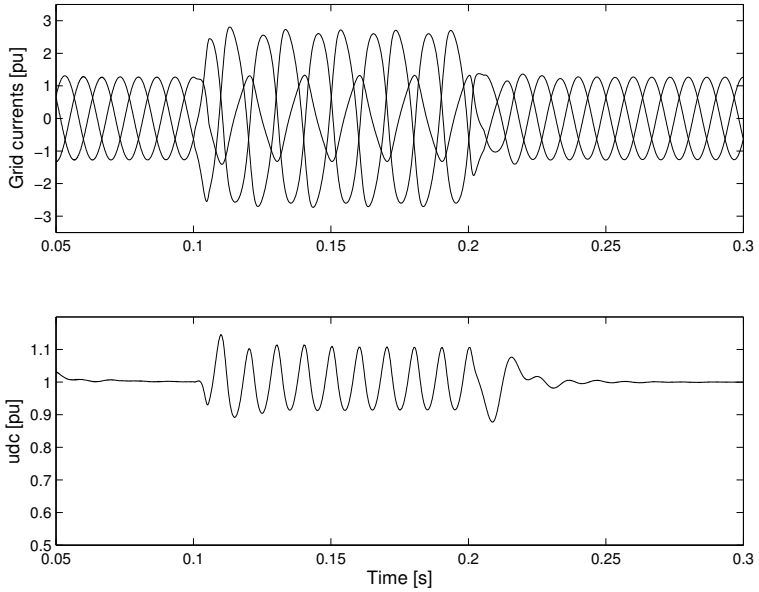

Fig. 2.7 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

Case 2- The oscillating powers flow from the grid side to the filter

In this case the grid is forced to supply the oscillating powers to the filter, by using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ 0 \\ -\Delta p_{\mathrm{s2}} \\ -\Delta p_{\mathrm{c2}} \end{bmatrix}. \qquad (2\text{-}27)$$

Using (2-27), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.8.

Comparing Fig. 2.7 and Fig. 2.8, it is concluded that it is preferred to use the current reference generation in (2-27) over (2-26) since the DC-link voltage ripples are reduced during the fault period.

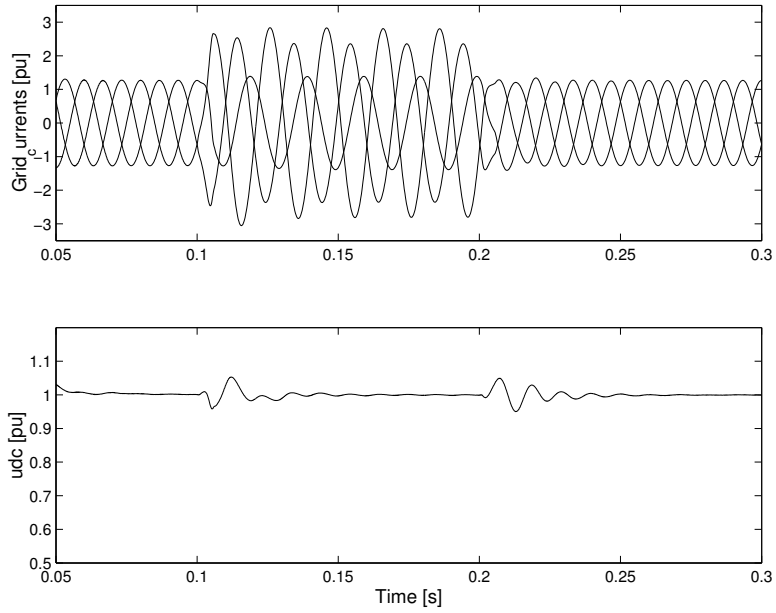

Fig. 2.8 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

2.6 Vector Current Controller with inductance-capacitance-inductance line filter

Due to the PWM switching of the voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [29]. Inserting an LCL-filter[5] between the grid and the VSC, as shown in Fig. 2.9, eliminates high frequency harmonics even with lower switching frequency.

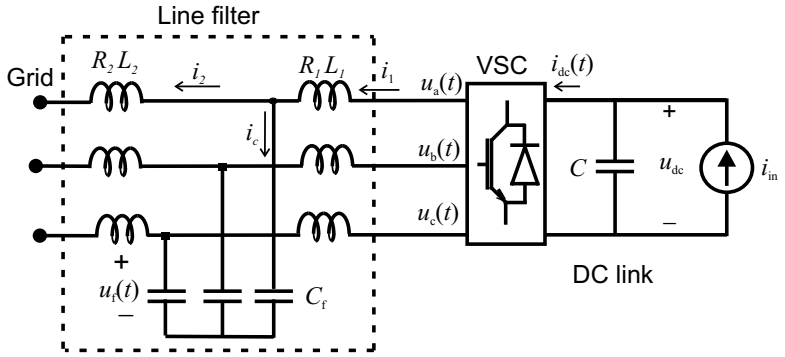

Fig. 2.9 Power circuit of DG system with VSC as a front end and an LCL-filter.

Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. In this work, a cascade control structure ([47], [48], and [49]) has been implemented to increase the stability margin and at the same time to damp oscillations at the resonant frequency of the LCL-filter. As shown in Fig. 2.10, the plant is described by three cascaded transfer functions; G_{p1}, G_{p2}, and G_{p3}, as

[5] The design of the LCL-filter parameters that are adopted here is given in Appendix B.

$$G_{\mathrm{p1}}(s)=\frac{I_2(s)}{U_{\mathrm{f}}(s)-E(s)}=\frac{1}{sL_2+R_2}$$
$$G_{\mathrm{p2}}(s)=\frac{U_{\mathrm{f}}(s)}{I_1(s)-I_2(s)}=\frac{1}{sC_{\mathrm{f}}} \tag{2-28}$$
$$G_{\mathrm{p3}}(s)=\frac{I_1(s)}{U(s)-U_{\mathrm{f}}(s)}=\frac{1}{sL_1+R_1}$$

where

$I_2(s)$ is the Laplace function of the grid side current $i_2(t)$;

$U_{\mathrm{f}}(s)$ is the Laplace function of the filter capacitor voltage $u_{\mathrm{f}}(t)$;

$E(s)$ is the Laplace function of the grid voltage $e(t)$;

$I_1(s)$ is the Laplace function of the converter side current $i_1(t)$; and

$U(s)$ is the Laplace function of the converter output voltage $u(t)$.

The inner controller G_{c3} is used for stabilization of G_{p3} and is designed using dead-beat control strategy. The two outer controllers G_{c2} and G_{c1} are used to stabilize G_{p2} and G_{p1} respectively. G_{c2} is implemented as a P-controller, while G_{c1} is implemented as a PI-controller where the integral part is added to eliminate the steady state error. With the resulting controller, shown in Fig. 2.10, the two controllers G_{c1} and G_{c2} are acting like one PI-controller. The outer controller G_{c1} is a two-degree of freedom controller, since it is using the output signal of a Smith predictor (with a compensation gain k_{ps}) to cancel the time delay effect. The time-delay free plant transfer-function G_{pm} represents the LCL-filter model in steady state, where the capacitor effect is neglected.

The three controllers are described in the rotating dq-frame as follows

$$\underline{y}_{\mathrm{1dq}}(k)=k_{\mathrm{p1}}\left(\underline{\varepsilon}_{\mathrm{idq}}(k)+\frac{T_{\mathrm{s}}}{T_{\mathrm{i}}}\sum_{n=0}^{k}\underline{\varepsilon}_{\mathrm{idq}}(n)\right) \tag{2-29}$$

$$\underline{y}_{\mathrm{2dq}}(k)=k_{\mathrm{p2}}\,\underline{y}_{\mathrm{1dq}}(k) \tag{2-30}$$

$$\underline{u}^{*}_{\mathrm{dq}}(k+1)=\underline{u}_{\mathrm{fdq}}(k)+(R_1+\mathrm{j}\omega L_1)\underline{i}_{\mathrm{1dq}}(k)+k_{\mathrm{p3}}\,\underline{y}_{\mathrm{2dq}}(k) \tag{2-31}$$

where

$\underline{y}_{1dq}$ is the output vector of G_{c1}, which represents the change in the capacitor voltage $\underline{u}_{fdq}$;

k_{p1} is the proportional gain of G_{c1};

T_i is the integral time of G_{c1};

$\underline{y}_{2dq}$ is the output vector of G_{c2}, which represents the required change in the converter side current $\underline{i}_{1dq}$;

k_{p2} is the proportional gain of G_{c2}; and

k_{p3} is the proportional gain of G_{c3}.

The current error vector $\underline{\varepsilon}_{idq}$ is the input to the outer controller G_{c1}, and is described in the same way as in (2-8).

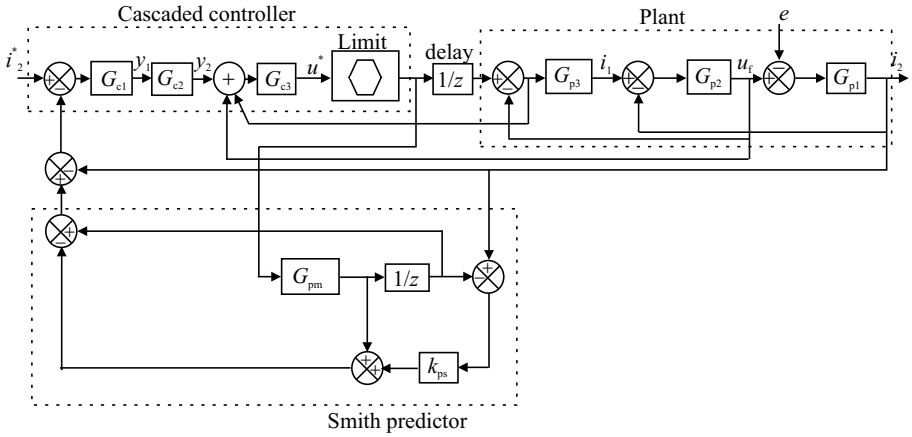

Fig. 2.10 Schematic diagram of the proposed cascaded controller (the z denotes the z transform, thus $1/z$ denotes a delay of one sample). Note that the controller is described in discrete form while the plant is described in continuous form.

The faster the inner loop is in comparison with the outer loops, the better the performance of the cascaded control system becomes in the sense of the transient response [49]. However, reduced gains for the outer controllers will reduce the overall bandwidth of the system. Hence, the inner controller gain is set to the dead-beat gain as [20]

$$k_{\mathrm{p3}} = \frac{L_1}{T_\mathrm{s}} + \frac{R_1}{2} \ . \tag{2-32}$$

The Smith predictor gain is set to a small value to stabilize the overall controller, while k_{p2} and k_{p1} are tuned by changing their values and examining the Bode plot. In Fig. 2.11 the value of k_{p2} is set to 30% of k_{p3}, while k_{p1} assumes values between 30% and 100% of k_{p2}. The same is performed in Fig. 2.12 by setting k_{p1} as 70% of k_{p2}, to achieve a high bandwidth and no overshoot, while k_{p2} is taking values between 25% and 70% of k_{p3}. It is shown by the phase plot in the figure that for k_{p2} values of 70% to 50% of k_{p1} the controller becomes unstable. Hence, the value of k_{p2} has been chosen to 30% of k_{p1}. The values used for the gains are listed in Appendix D.

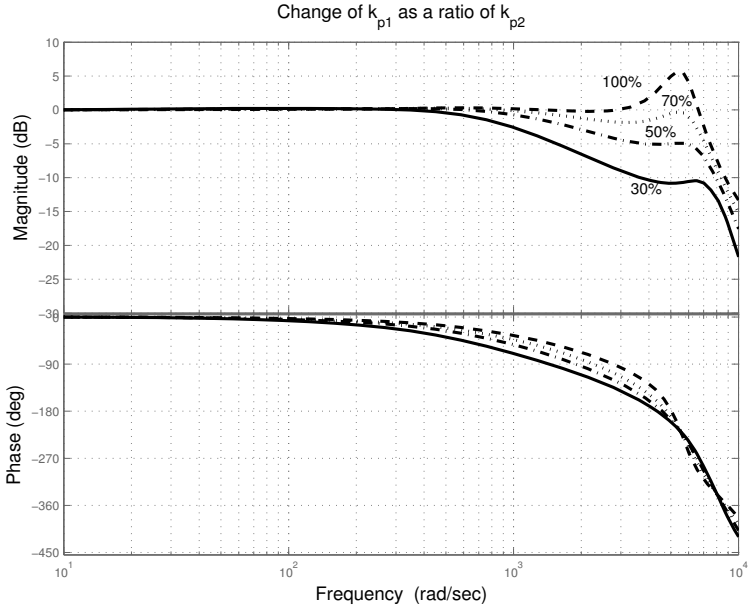

Fig. 2.11 The closed loop system frequency performance as k_{p1} is changed as a certain percentage of k_{p2}, with k_{p2} constant.

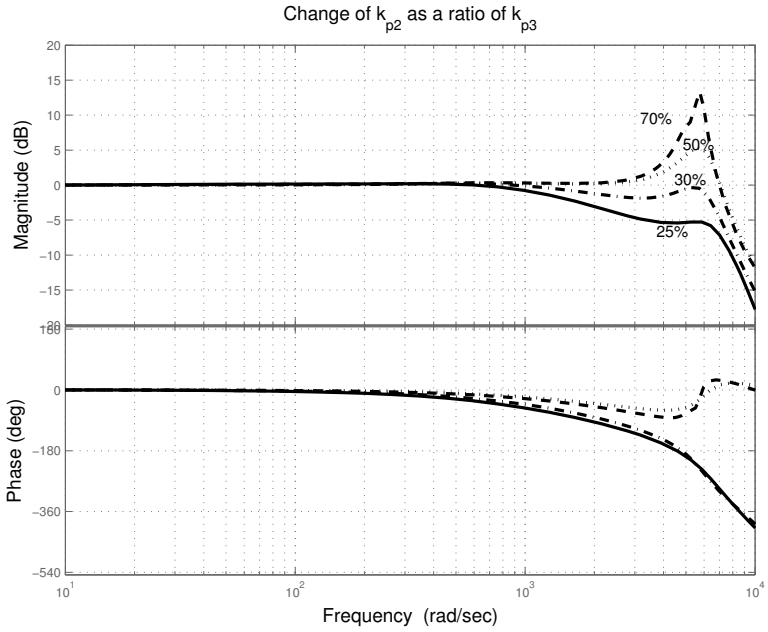

Fig. 2.12 The closed loop system frequency performance as k_{p2} is changed as a certain percentage of k_{p3}, while k_{p1} is constant.

2.7 Current reference generation with inductance-capacitance-inductance line filter

The current references are generated, in the same way as for the L-filter, as

$$\begin{bmatrix} i_{2\mathrm{d}}^{*} \\ i_{2\mathrm{q}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{d}} & e_{\mathrm{q}} \\ e_{\mathrm{q}} & -e_{\mathrm{d}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ \omega C_{\mathrm{f}} \left(u_{\mathrm{cd}}^{2} + u_{\mathrm{cq}}^{2} \right) \end{bmatrix} - \begin{bmatrix} -\omega C_{\mathrm{f}} u_{\mathrm{cq}} \\ \omega C_{\mathrm{f}} u_{\mathrm{cd}} \end{bmatrix} \quad (2\text{-}33)$$

where Δp is the active power dissipated in the filter, and is a function of the grid side and converter side currents

$$\Delta p = R_1\left(i_{1d}^2 + i_{1q}^2\right) + R_2\left(i_{1d}i_{2d} + i_{1q}i_{2q}\right) + \omega L_2\left(-i_{1d}i_{2d} + i_{1q}i_{2d}\right). \tag{2-34}$$

The current references are generated in the same manner for the DVCC[6].

2.8 Conclusions

Two distributed generation systems with a voltage source converter as a front end and two line filters; namely L-filter and LCL-filter, are considered. Vector current controllers have been proposed to control the injected grid currents for both systems. The controller for the L-filter system is based on the dead-beat control and is modified to deal with one sample time delay, integrator windup, grid voltage saturation and grid voltage imbalance. The controller shows good reference tracking even in the worst case of increased current steps. In addition, in the case of controllable DC-link voltage, the current references have been derived in such a way that a regulated DC-link voltage is provided even in the case of unbalanced grid voltage. On the other hand, a cascaded current controller has been proposed for the LCL-filter system. The current references have also been derived in the same manner as for the L-filter system.

[6] The detailed derivation is given in Appendix E and Paper C.

Chapter 3

Voltage Dips Ride-Through Capability

In this chapter, the effect of all possible voltage dips that could appear at the terminal of a converter interfaced DG unit is examined. The two distributed generation systems, described in the previous chapter, with two different line filters are compared regarding the injected grid currents and the DC-link voltage regulation. Moreover, design equations are derived to be able to predict the maximum currents that are expected to flow through the converter switches during different voltage dips.

3.1 Voltage dips definition

A voltage dip is a phenomenon that is experienced at the end user terminals mainly due to a short circuit fault at a certain point in the electrical network. It can also happen due to motor starts or overloads. It is, as defined by IEEE-std 1159-1995 [50], a decrease to between 0.1 to 0.9 p.u. in the RMS value of the voltage at the power frequency for durations of 0.5 cycle to 1 min. Using this definition, the voltage dip magnitude is referring to the remaining voltage.

In spite of the short duration, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [51]. To deeply study the effect of voltage dips on DGs with a power-electronics interface, the classification found in [52] has been adopted.

3.2 Voltage dips classification

Starting from the different types of faults that can occur in a power system, a classification of voltage dips has been accomplished in [52]. It depends on how the load is connected and how the windings of the

supplying transformer are connected. According to this classification, there are seven types of dips designated with the letters "A" to "G". The system in Fig. 3.1 has been used to quantify the magnitude of a voltage dip in a radial system. In this system, the fault occurs at a remote distance from bus 2 and the load, which could be a DG (as in the thesis), is connected at bus 3. Two impedances are connected to bus 2: the impedance of the system, denoted by Z_S, which represents Thevinin's equivalent impedance of the power system, and the fault impedance Z_F. The load is connected through a transformer to bus 2, at which the voltage, in p.u., is given by

$$V_{dip} = \frac{Z_F}{Z_F + Z_S}. \tag{3-1}$$

It is assumed that the pre-fault voltage is used as reference and is equal to 1 p.u. This typically means that voltage dips originated in the transmission system are shallow (since Z_s is small), while voltage dips originated at distribution level can be deep.

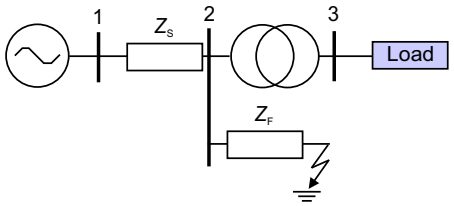

Fig. 3.1 General single-line model for dips classification.

If first it is assumed that the *X*/*R* ratio of the impedances Z_S and Z_F is the same, then V_{dip} has zero phase angle. The resulting voltage dip at bus 3 can be of type "A", which could be a result of a three-phase balanced fault, or any of the six unbalanced types denoted with letters "B" through "G" and reported in Fig. 3.2. In the figure, $E_{i,dip} = E_i V_{dip}$ where the subscript i denotes the phase sequence and takes the values 1, 2, and 3[7], and E_i represents the RMS value of the healthy phase voltage.

[7] Afterwards the three phases will be referred to as a, b, and c.

The transformer connection type has an effect of changing the voltage dip from one type to another. Still, in this work, all dip types are considered for the purpose of providing a general analysis.

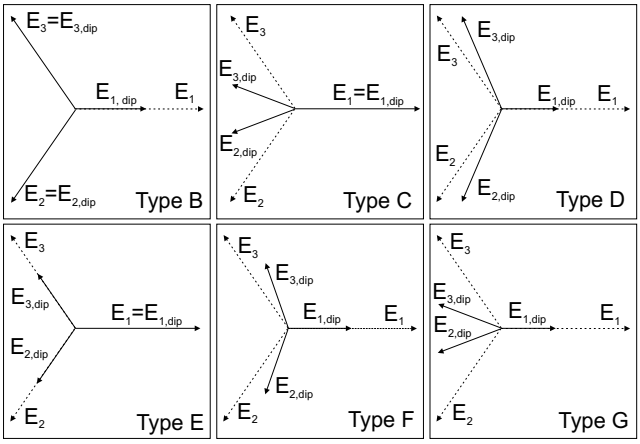

Fig. 3.2 Unbalanced voltage dip classification from "B" to "G". Phasors of three phase voltage before (dotted) and during (solid) fault are displayed. The classification is adopted from [52].

3.3 Voltage dips associated with phase angle jump

If the *X*/*R* ratio for Z_S and Z_F is different, the voltage dip seen at the terminals of the load will have a phase angle "ψ" called "phase angle jump". The impedance angle α is defined as

$$\alpha = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \tag{3-2}$$

where $Z_S = R_S + jX_S$, $Z_F = R_F + jX_F = zl$, z is the feeder impedance per unit length and l is the feeder length. The expression of the voltage dip at bus 2 will be

$$v_{dip} = \frac{\lambda e^{j\alpha}}{1 + \lambda e^{j\alpha}} = V_{dip}\angle\psi \tag{3-3}$$

where $\lambda\, e^{j\alpha} = zl / Z_S$.

The four values for the impedance angle α, that are suggested in [52], are considered: 10^o as the highest expected value for transmission system faults, 0^o as the reference value, -20^o for overhead distribution lines, and -60^o for underground distribution cables. In Fig. 3.3, the relation between the phase angle jump and different dip magnitudes at the four impedance angles is shown. The phase angle jump is larger for smaller dip magnitudes and is more sensitive to the dip magnitude when $\alpha = -60^o$.

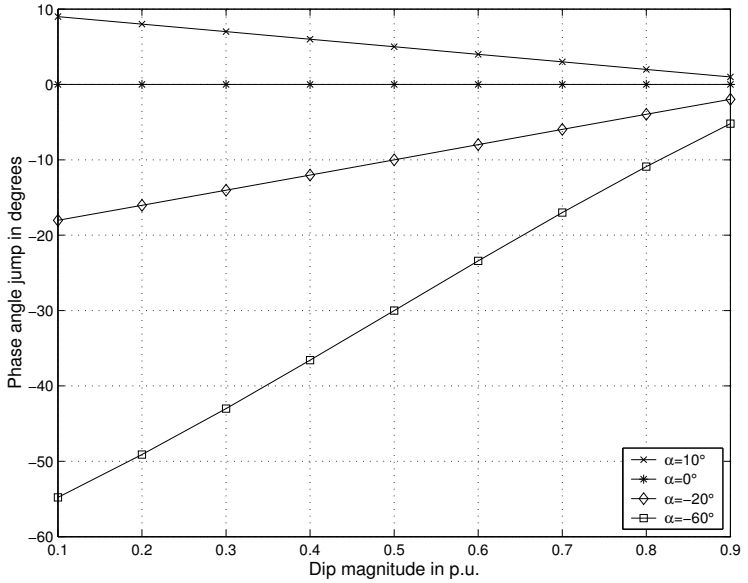

Fig. 3.3 Phase angle jump for different dip magnitudes and impedance angles.

3.4 Positive/negative sequence sub-classification

The magnitudes of the positive sequence (E_p) and the negative sequence (E_n) of the grid voltage for dip types "A" through "G" are calculated using Park transformation and summarized in Table 3-1, where E is the phase-to-phase RMS grid voltage. It shows that dips "C" and "D" have the same positive and negative sequence magnitudes. The same applies for dips "E", "F", and "G". However they may affect the system in different ways

according to Table 3-2, at which the positive and negative sequence components in the *dq*-coordinate system have been calculated. It shows that dips "C" and "D" result in different negative sequence *dq*-components. The same also holds for dip types "F" and "G", while dips "E" and "G" are exactly the same since they both result in the same positive and negative sequence components. This classification is useful in understanding the effect of unbalanced voltage dips on the system. Hence, the following study is carried out using the dual vector current controller (DVCC) that has been described in the previous chapter.

Table 3-1 Positive and negative sequence magnitudes of grid voltage for dip types "A" through "G".

Dip type	E_p	E_n
A	EV_{dip}	0
B	$\frac{E}{3}\sqrt{4+4V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
C, D	$\frac{E}{2}\sqrt{1+2V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{2}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
E, F, G	$\frac{E}{3}\sqrt{1+4V_{dip}\cos\psi+4V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$

Table 3-2 Positive and negative sequence components of the grid voltage in *dq*-coordinates for dip types "A" through "G".

Dip type	e_{dp}	e_{qp}	e_{dn}	e_{qn}
A	$EV_{dip}\cos\psi$	$EV_{dip}\sin\psi$	0	0
B	$\frac{E}{3}(2+V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
C	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{E}{2}(1-V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$
D	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{-E}{2}(1-V_{dip}\cos\psi)$	$\frac{-E}{2}V_{dip}\sin\psi$
E	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$
F	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
G	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$

3.5 Current through the voltage source converter caused by voltage dips

At the distribution level, the voltage source converter (VSC) mostly utilizes isolated gate bipolar transistors (IGBT's). An IGBT is easy to turn on and off, and has low conduction and switching losses [13]. The ratings of a single IGBT can be up to 1.2 kA and 3.3 kV. It has good switching capability (up to 100 kHz for a few kW applications), but for very high power devices and applications the frequency is limited to some kHz. On the other hand, the main drawback is poor overcurrent capability, i.e. it cannot withstand more than the peak current it is designed for, even for a short period of time. Hence, the current that would flow through the IGBTs during voltage dips could have a destructive effect if the valves are not designed to withstand this current level.

In order to calculate the required current rating of the VSC valves to ride through voltage dips occurring at the grid, the maximum current has been calculated for all the dip types. The current components in *dqp*- and *dqn*-frame are calculated using the following assumptions:

1. No switching-losses, which means that the AC active power P_1 of the converter is equal to the DC input power KP_{dc}.
2. In addition, the oscillating powers that are produced due to the imbalance are assumed to be supplied from the VSC side to simplify the calculations.
3. Furthermore, for simplicity, the phase angle jump is assumed to be zero, which results in zero *qp*- and *qn*-components of the grid voltage as seen by Table 3.2.
4. Moreover, perfect tracking is assumed, resulting in equal reference and actual currents.

Using (2-26), the grid currents are described as

$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \frac{KP_{dc}}{e_{dp}^2 - e_{dn}^2} \begin{bmatrix} e_{dp} \\ 0 \\ -e_{dn} \\ 0 \end{bmatrix} \tag{3-4}$$

where P_{dc} is the nominal input DC power and K is the ratio of the input power that is actually delivered to the DC link. The current components are then transformed back to the $\alpha\beta$-coordinates in positive- and negative-sequence frames and then into three-phase currents.

In the case of single phase faults (dip types "B" and "D"), the maximum phase current (phase *a*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp} + e_{dn}} \tag{3-5}$$

while for two phase faults (dip types "C", "E", "F", and "G"), the maximum phase current (phase *b*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp}^2 - e_{dn}^2} \sqrt{\frac{1}{4}\left(e_{dp} - e_{dn} \right)^2 + \frac{3}{4}\left(e_{dp} + e_{dn} \right)^2} \; . \tag{3-6}$$

For three phase faults (dip type "A"), the maximum phase current is

$$I_{max} = \sqrt{\frac{2}{3}} . \frac{K P_{dc}}{E \times V_{dip}} . \tag{3-7}$$

The values of e_{dp} and e_{dn}, which are the positive and negative sequence of the *d*-component of the grid voltage, are calculated using Table 3-2 for different voltage dips.

A comparison between the analytically calculated current values and the simulated ones has been performed for all dip types, in order to verify the analytical equations. For instance, the result with dip type "A" is shown in Fig. 3.4[8], where the simulation[9] has been carried out for the L-filter case. It will be shown later that the currents produced with the LCL-filter have the same amplitudes as for the L-filter, using the same value of the series inductance. As shown by the figure, the calculated curve shows overestimated current values, since the dissipated powers by the filter were

[8] Another example is shown in Paper A.

[9] The simulation has been carried out here in MatLab/Simulink.

neglected in the design equations while they were incorporated in the simulation.

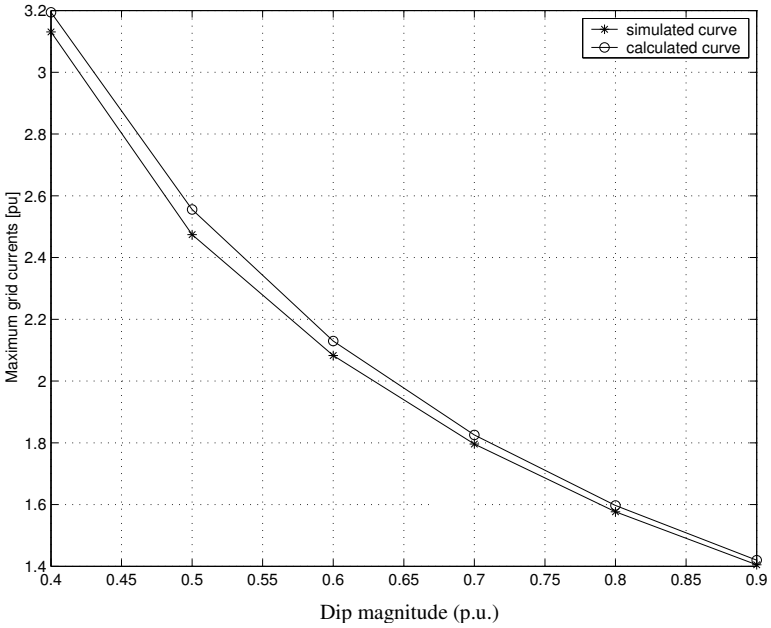

Fig. 3.4 Maximum currents due to voltage dip of type "A".

3.6 Ride-through capability for DGs with L-filter

Depending on the maximum currents that could flow during different voltage dips and using some statistical data regarding the most frequent dip types at the grid, the converter switches could be designed to withstand the increased currents. The peak-to-peak DC-link voltage in case of grid-voltage dips should also be considered in the design of the DC-link. However, the DC-link voltage ripples are found to be negligible when the oscillating powers that are resulting due to the grid-voltage imbalance, are assumed to be supplied from the grid side. This case has been found to be the optimal one for the controller design, if ride-through capability is to be considered.

The effect of all types of dips, with various magnitudes and zero phase angle jump, on the maximum grid current and DC voltage ripples is represented in Fig. 3.5. The maximum current the converter switches should

be able to hold is 3.65 p.u., which happens at 30% dip type “D”. The maximum DC voltage ripple is about 2.5% peak-to-peak and it occurs at 30% magnitude of dip type “F”.

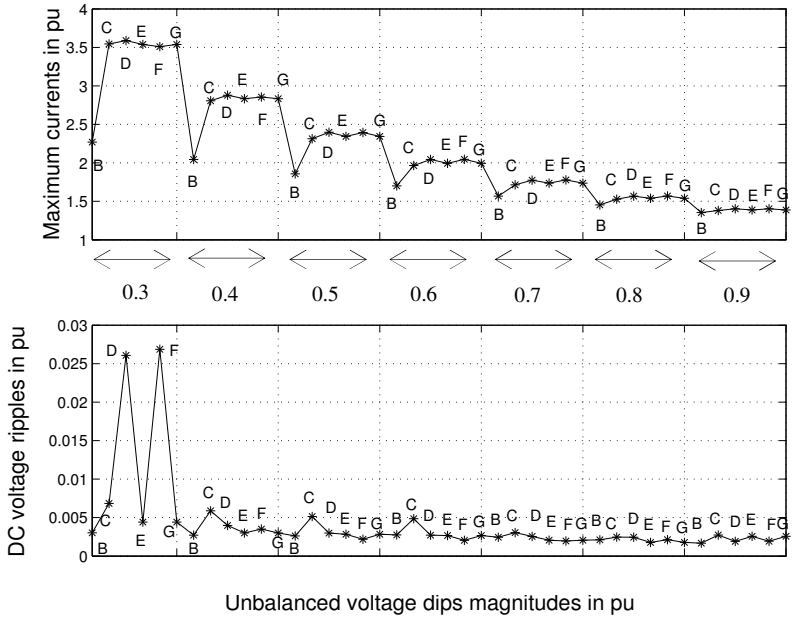

Fig. 3.5 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types.

The effect of the phase angle jump on the DC-link voltage ripples during the dip is found to be negligible. However, their effect over the maximum grid currents is more noticeable as shown in Fig. 3.6. It can be concluded that differences are very small for $\alpha = 10^{o}$ and $\alpha = -20^{o}$ while they seem to be significant when $\alpha = -60^{o}$. In that case the maximum current, with 30% magnitude of dip type “D”, is equal to 4.5 p.u. If the converter valves are designed considering the case of zero phase angle jump, they will be able to handle only 3.65 p.u. current as mentioned previously. Hence, in the case of a voltage dip with phase angle jump, the valves would most probably be destroyed or the VSC will be tripped off.

Moreover, from (3-5), (3-6), and (3-7), it is obvious that there is a direct proportionality between the maximum current and the value of the actual input power. In other words, if the input power is lowered by the ratio *K*, the maximum value of the current will also be lowered by the same ratio. Simulation results presented in Fig. 3.7 represent the effect of lowering the input power P_{in} for different dip types and magnitudes.

Therefore, if the converter switches have to be rated to ride through all dips with 30% minimum magnitude, the current rating can be decreased from about 3.5 p.u. to 3 p.u., if the input power is decreased from 90% to 70% of nominal value.

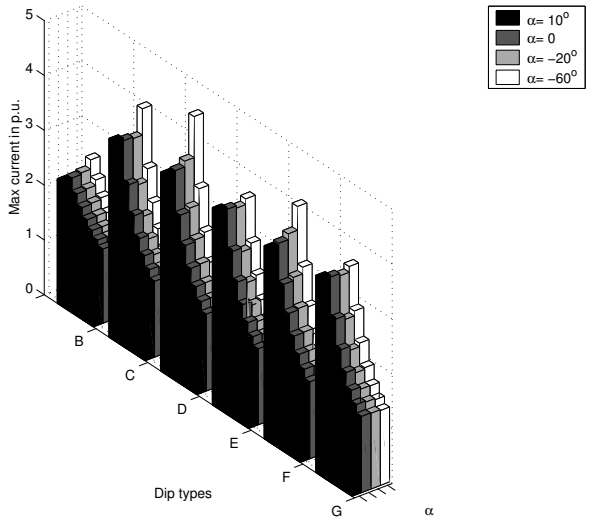

Fig. 3.6 Effect of phase angle jump on the amplitude of phase currents for different unbalanced voltage dips.

One way to optimise the design of the switches is thus to minimize the currents during the fault period, which could be established by temporarily decreasing the input power to the system (decreasing *K* in (3-5), (3-6), and (3-7)) during the fault. If this is possible or not depends on the controllability and the response time of the DC-link or the primary source. By incorporating a DC-chopper, acting as a dump load, or DC energy storage, the input power

could be reduced during the voltage dip period [9]. In addition, for some primary sources it could be possible to reduce the input energy (e.g. by changing the turbine torque reference in wind turbine systems) [36].

On the other hand, if the DC bus is powered by a source that is stochastic in nature, e.g. wind, one could argue that the probability that a dip occurs when the wind turbine is producing full power might be very low, as the turbine often runs at much lower power. Then, to optimize the design it is possible to consider a lower value of the input power, which is delivered by the turbine. This means, accepting a certain risk that the converter (thus the turbine) might still trip, but can lead to greatly reducing the size of the converter[10].

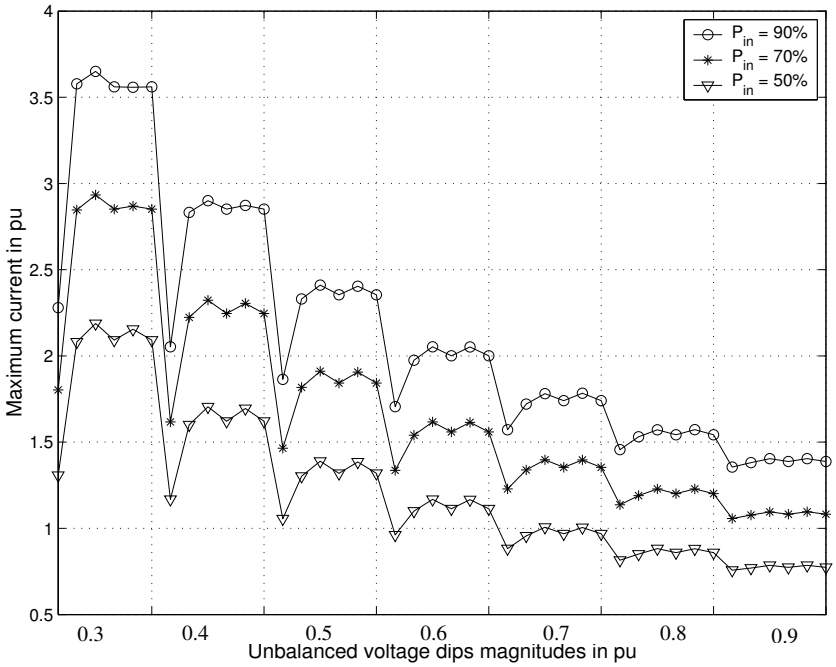

Fig. 3.7 Effect of lowering P_{in} on maximum grid currents for unbalanced voltage dips with magnitudes from 0.3 p.u. to 0.9 p.u. in steps of 0.1. The voltage dip types are shown analogously to Fig. 3.5.

[10] This is investigated numerically by the case study in Paper A.

3.7 Ride-through capability for DGs with LCL-filter

The effect of all unbalanced dips, with various magnitudes, on the maximum grid current and DC voltage ripples (in the middle of the dip period) is presented in Fig. 3.8. The base for the per unit currents is the maximum of the nominal current of the converter. Compared with the case of L-filter interface system (shown in Fig. 3.5 with a current base value equal to the RMS of the nominal current), the currents are almost the same while the DC voltage ripples are slightly increased but still within an acceptable range. This is mainly due to the part of the oscillating power consumed by the filter capacitor and not compensated for in the generated reference currents.

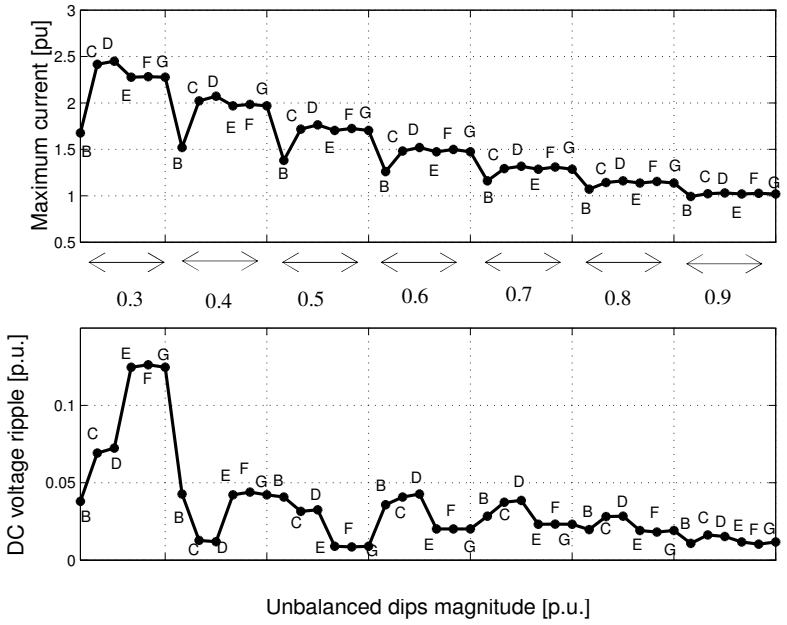

Fig. 3.8 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types and magnitudes from 0.3 to 0.9.

3.8 Conclusions

In this chapter, the effect of different voltage dips over the grid currents and DC-link voltage ripples are examined for the L-filter and the LCL-filter systems. The effect of the phase angle jump has also been examined considering the case when the grid supplies the oscillating powers. It is concluded that the phase angle jump has more effect on voltage dips with smaller magnitudes, and the worst case occurs when the impedance angle $\alpha = -60^{o}$, which corresponds to cable transmission. This effect is more significant for dip types "C" and "D". The maximum current occurs with 30% magnitude of dip type "D" and is equal to 4.5 p.u., i.e. 25% more than its value in case of zero phase angle jump. Thus, the effect of the phase angle jump should be considered when designing the converter switches to ride through all dips.

Since the two considered line filters produce almost the same current amplitudes, having the same value of series inductance, the design equations that have been derived here to calculate the required current ratings of the converter can be used for both systems. These equations give slightly over-estimated values since they are derived without considering the power dissipated in the filter. However, this over-estimation is preferred in the design stage because it gives a safety margin to the design values.

The effect of decreasing the input power has also been examined. Temporarily decreasing the input power to the system during fault reduces the currents during that period, which could be a way to decrease the ratings of the converter valves and in the same time preserving the ride-through capability. This, however, would require that the input power to the DC bus be controllable so as to be reduced very quickly.

Chapter 4

Voltage-Regulation Capability in Weak Grids

By adding a voltage-regulation capability to the DG controller, it is possible to mitigate most of the power quality problems. In addition, this is a highly attractive feature in case of the operation in weak grids. This is the topic of this chapter, where the regulation capability is examined for the mitigation of the decrease of the voltage amplitude specifically in weak grids, the voltage harmonics, and the voltage fluctuation. The DG system with a VSC as a front end and an LCL-filter is considered throughout this chapter. The voltage regulation limits are evaluated regarding the local load of the DG and the DG injected active power. Moreover, the effect of the grid voltage distortion over the phase-angle estimation and the regulation capability is studied. A phase-locked loop (PLL) synthesis based on the extraction of the fundamental component of the grid voltage has been introduced to obtain robust phase estimation.

4.1 Introduction

The term weak grid is here referring to systems where the voltage level is not constant as in a stiff (or strong) grid. Weak grids are usually found in remote areas where the feeders are long. The grids in these areas are usually designed for small loads [32]. When the design load is exceeded, the voltage level may fall below the allowed minimum and/or the thermal capacity of the feeders might be exceeded. Hence, the voltage regulation of long weak distribution lines is an important problem to be considered [30]. The connection of a DG in a weak distribution system can provide voltage support, if the voltage regulation capability is added to its controller, in addition to the main function of injecting active power into the grid. Moreover, by regulating the voltage at the PCC most of the power quality

problems could be mitigated, which might be an attractive requirement in grids with large number of disturbing (non-linear) as well as sensitive loads.

In recent publications, the voltage regulation problem is mainly tackled, in transmission or distribution systems, regarding the power electronics application, using a STATCOM (called DSTATCOM in distribution systems), which is a converter-based shunt connected reactive-power generator. The advantages of a STATCOM, compared to the other thyristor-based reactive power generators (SVCs), are its wider operating area, better performance, and greater application flexibility [75]. The implementation of the DSTATCOM has been discussed in [37], [38] and [58], [60] for voltage flicker mitigation, controlling both the active and the reactive injected powers. In [31] a DSTATCOM is used to regulate and balance the voltage at the distribution bus using only reactive power injection. The voltage regulation limits, however, have not been discussed. Although the application of a STATCOM and a DG are similar in the utilization of a converter as a front end, they are different from the point of view of the active power. STATCOMs could have controllable active power (depending on the grid needs) if they are connected to an energy storage device, while DGs are injecting constant active power that could change due to the changes in the energy source. The DG constant injected active power, consequently, puts some limits on the voltage regulation capability as will be investigated later in this chapter.

The voltage regulation using converter-interfaced DG systems, specifically with LCL-filters at the connection point to the grid, has been less introduced in literature since the emphasis is usually set on the DG technology, not from the power system point of view, and the DG system controllers. Still an example for such a system is found in [32], where a single phase VSI interface of a photovoltaic DG connected to a weak grid through an LCL-filter is considered regarding the voltage regulation purpose. The control algorithm measures the phase of the terminal voltage using Fourier extraction and then computes the required inverter voltage for the desired active and reactive power export commands. The feedback of the filter states has been used to provide the stability of the controller at higher

frequencies. The control of the real and the reactive power flow is done on a cycle-by-cycle basis. Hence, it takes several cycles for the system to settle. Although in [33] the application of a variable speed wind turbine (VSWT) system connected to a weak grid is considered, the emphasis has been placed on the control of the converters for the system and the voltage compensation has been of no interest. The compensation for grid-voltage harmonics has been the main topic of [78], where an inverter-based DG with an L-filter at the connection point to the grid has been considered. Three adaptive regulator gains have been calculated for the 5^{th}, the 7^{th} and the higher harmonics to produce the proper current commands. The focus has been put only on the voltage harmonic compensation, hence the voltage regulation is not considered and the controller takes long time to reach the steady state.

In this chapter, the cascaded controller for the DG system with an LCL-filter[11] is implemented along with a point of common coupling voltage regulator to add the voltage regulation capability. The voltage regulation capability limits are also discussed regarding the DG local load and the DG injected active and reactive powers. Since the output voltage of the VSC is synchronized with the grid voltage using an estimated phase angle, the error in this angle that is mainly due to the distorted grid voltage, should be minimal. The grid voltage phase angle is estimated using a phase locked loop (PLL), which is implemented in the *dq*-frame using a PI controller that tracks the changes in the *q*-component grid voltage by producing the necessary change in the phase angle. This PLL has been well established before [53], however it is first explained here since it will be modified in order to eliminate the effect of the grid voltage power quality problems on the estimated phase angle.

4.2 Phase locked loop (PLL)

The synthesis of the PLL that is commonly used for grid-connected three-phase power conversion systems [53] is based on the quadrature-component extraction of the grid voltage. Hence it will be referred to, here, as a Q-PLL.

[11] This controller has been explained in Chapter 2.

Assuming a balanced three-phase grid voltage at the point of common coupling (PCC)

$$u_{\mathrm{a(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\theta\,, \tag{4-1}$$

$$u_{\mathrm{b(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta - \frac{2\pi}{3}\right), \tag{4-2}$$

and

$$u_{\mathrm{c(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta + \frac{2\pi}{3}\right) \tag{4-3}$$

where U_{PCC} is the line RMS voltage at the PCC, and θ is its phase angle.

Transforming the voltage from three-phase notation into a voltage vector in a fixed $\alpha\beta$-frame, using power invariance transformation, the resulting voltage vector will be

$$\underline{u}_{\alpha\beta} = U_{\mathrm{PCC}}\left(\sin\theta + \mathrm{j}\cos\theta\right). \tag{4-4}$$

Normalizing this voltage vector and transforming it into a rotating dq-coordinate system, which rotates with the estimated angular frequency ($\hat{\omega} = \mathrm{d}\hat{\theta}/\mathrm{d}t$), the resulting normalized voltage-vector components will be

$$\underline{u}^{\mathrm{n}}_{\mathrm{dq}} = \cos\left(\theta - \hat{\theta}\right) + \mathrm{j}\sin\left(\theta - \hat{\theta}\right) \tag{4-5}$$

where $\hat{\theta}$ is the estimated phase angle.

If the estimation error ($\varepsilon = \theta - \hat{\theta}$) is very small, then $u^{\mathrm{n}}_{\mathrm{d}} \cong 1$ (the real part in (4-5)) and $u^{\mathrm{n}}_{\mathrm{q}} \cong \varepsilon$ (the imaginary part in (4-5)). Hence, the normalized q-component of the voltage can be used as an input to a PI-controller to produce a required change in the angular frequency ($\Delta\omega$) to track the changes in the phase angle. The Q-PLL main block diagram is shown in Fig. 4.1.

The on-line normalization of the voltage vector will result in nullifying the phase estimation error due to a balanced voltage amplitude change (e.g. three-phase voltage dips). However, in case of unbalanced voltage dips,

oscillations with double the fundamental frequency of the grid will be superimposed on the estimated frequency. These oscillations will result in an error in the estimated phase-angle of the grid-voltage.

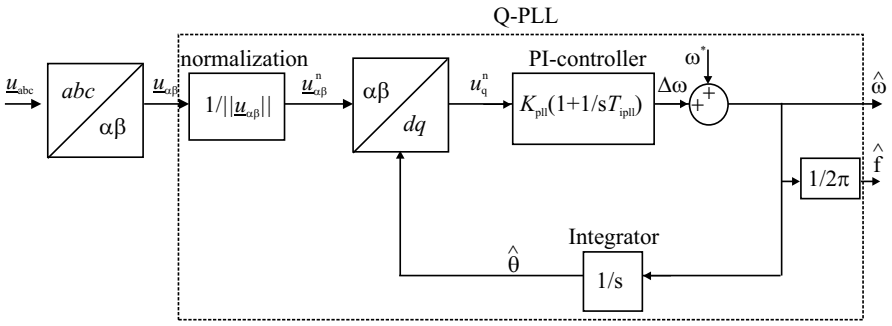

Fig. 4.1 Phase estimation using Q-PLL.

To eliminate this error, the positive sequence of the voltage-vector *q*-component is used as an input to the Q-PLL. This PLL is referred to as a positive sequence PLL (PS-PLL). This PLL is implemented in [55] and [56] by the use of low pass filters (LPF). However, a trade-off has to be made between robustness and good transient performance of the LPFs. Hence, it is instead implemented here as suggested in [57] using the delayed signal cancellation algorithm (DSC) to extract the positive sequence component of the voltage. As shown in Fig. 4.2, the three-phase voltages are measured and transformed into a vector in the stationary αβ-frame. Then the positive sequence voltage vector is extracted using the DSC algorithm, and fed into the Q-PLL that has been described in Fig. 4.1.

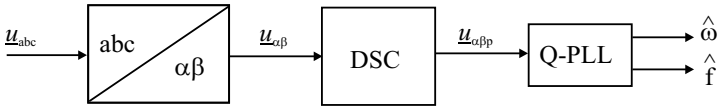

Fig. 4.2 Positive-sequence PLL.

To investigate the effect of the voltage imbalance on the PLL performance, an unbalanced voltage dip of type "C" and remaining voltage amplitude of 0.4 p.u. is applied from 0.5 s to 0.7 s. The estimated frequency

using the Q-PLL and using the PS-PLL are shown in Fig. 4.3 by the middle and lower plots respectively. The estimated frequency using PS-PLL is fairly unaffected by the unbalanced voltage dip apart from the transients at the start and the end of the dip. These transients last for one quarter of the fundamental period and they are resulting due to the implementation of the DSC.

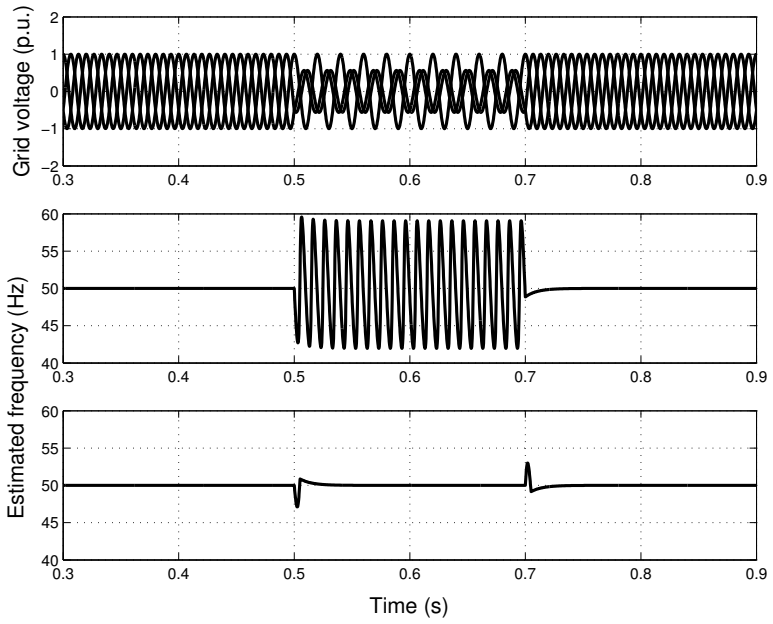

Fig. 4.3 Grid voltage (upper), and estimated frequency using Q-PLL (middle) and PS-PLL (lower).

4.3 PCC-voltage regulation limits

The voltage-regulation capability limit of a converter-interfaced DG is mainly related to the need for the DG to inject constant active power into the grid. To investigate this limit further, the simple weak grid system that is shown in Fig. 4.4 is considered. The parameters that are used for the weak-grid system are listed in Appendix C. For simplicity, it is assumed that the grid impedance Z_s is pure reactive ($Z_s = j\,X_s$). The grid is supplying a load at

the far end of the feeder, where a DG is also connected. It is assumed first that the load is disconnected and the DG is supplying both active power P_{DG} and reactive power Q_{DG} to the grid.

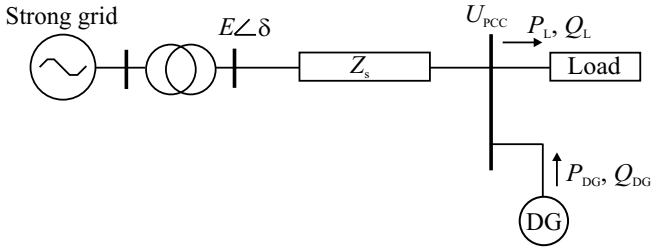

Fig. 4.4 Direction of power flow from VSC to PCC.

The power flow through the system is described by [54]

$$P_{DG} = \frac{U_{PCC}E}{X_s}\sin\delta \tag{4-6}$$

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \frac{U_{PCC}E}{X_s}\cos\delta \tag{4-7}$$

where E is the strong grid RMS line voltage, and δ is the grid voltage angle.

Using (4-6), the adjacent side for the angle δ can be calculated. Then

$$\cos\delta = \frac{\sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}}{\frac{U_{PCC}E}{X_s}}. \tag{4-8}$$

Substituting (4-8) in (4-7), Q_{DG} is obtained as

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}\ . \tag{4-9}$$

The voltage at the strong grid bus E is assumed to be equal to 1 p.u. Since the application of a DG requires injecting constant active power to the grid, the change in the reactive power leads to a change in the voltage at the PCC

(U_{PCC}) as suggested by (4-9). However, the value of the input active power affects the amount of the reactive power that is available for the compensation. A higher value of the injected active power implies that a higher value of reactive power can be injected, considering the same equation. Yet, that implies higher injected current, which could be an issue for the VSC valves capacity and protection[12], and also the increase of the DC-link voltage ripples might be another issue. An illustration of this is presented in Fig. 4.5[13], where the voltage regulation capability has been examined for a case when the grid voltage has a modulating signal with an 8% amplitude superimposed on the fundamental component. The input power from the DG source has been varied from 70% to 140% of the nominal value.

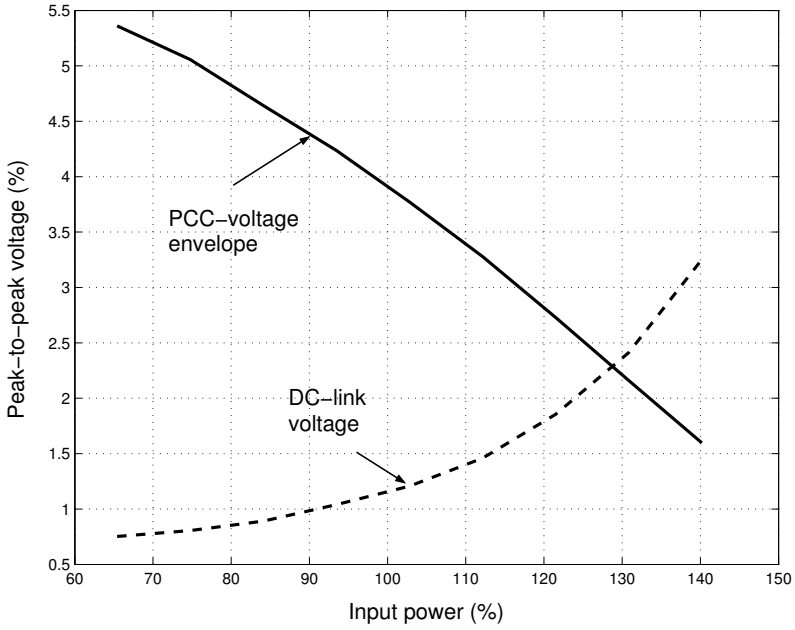

Fig. 4.5 Effect of the injected input power on the PCC voltage envelope oscillation (solid) and DC-link voltage ripples (dashed).

[12] That has been discussed in the previous chapter and in Paper A.
[13] Further details are provided in Paper E.

With the voltage regulation capability, the PCC-voltage has been better regulated at the upper value of the injected active power, where the grid voltage amplitude modulation has been reduced to 1.5%. On the other hand, the DC-link voltage ripples has increased to about 3.2% of its nominal value. Although negligible in value, in this example, the DC ripples amplitude could have a more significant value, for instance, if the amplitude of the modulating signal increases.

Equation (4-9) can be rearranged as

$$P_{\mathrm{DG}}^2 + \left(Q_{\mathrm{DG}} - \frac{U_{\mathrm{PCC}}^2}{X_{\mathrm{s}}} \right)^2 = \left(\frac{U_{\mathrm{PCC}} E}{X_{\mathrm{s}}} \right)^2 . \tag{4-10}$$

Equation (4-10) represents a circle with the radius of $U_{\mathrm{PCC}}E/X_{\mathrm{s}}$ and the centre at $(0,U^2_{\mathrm{PCC}}/X_{\mathrm{s}})$. By varying U_{PCC}, different power circles will result representing different possible operating points related to different values of the injected (or drawn) DG active and reactive powers. Those power circles have been illustrated in Fig. 4.6, where only the possible operating area has been shown (for the PCC voltage varying between 0.5 p.u. and 1 p.u.).

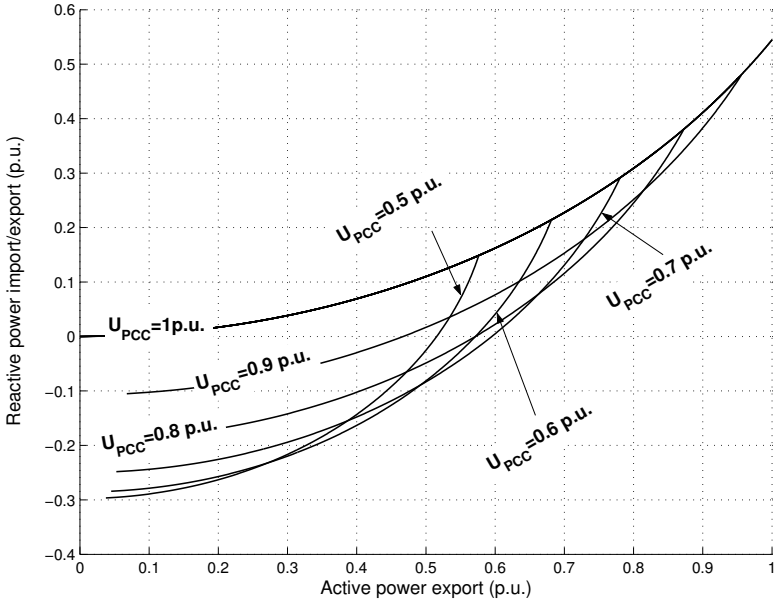

Fig. 4.6 DG import/export power with unloaded weak grid for different PCC voltages.

The figure is indicative of the amount of the reactive power to be injected by the DG at a specific value of the injected active power and a certain voltage drop over the feeder. For instance, for a PCC voltage of 0.7 p.u. and injected active power of 0.5 p.u., the injected reactive power should equal to the difference between the two values resulting from the intersection of the 0.5 p.u. power line and the two circles related to the PCC voltages of 1 p.u. and 0.7 p.u. (in this example, the injected reactive power will be about 0.2 p.u.). For the same PCC voltage (0.7 p.u.), if the DG injected power is 0.8 p.u., this operating condition will represent an unstable operation since the 0.8 p.u. power line does not intersect with the 0.7 p.u. circle.

To calculate the maximum reactive power that should be injected to regulate the voltage at the PCC with different voltage drops, (4-9) is differentiated with respect to the PCC voltage U_{PCC} and the result is set to zero. Then the resulting voltage that would acquire maximum injected reactive power is U_{limit}

$$U_{\mathrm{limit}} = X_{\mathrm{s}} \sqrt{\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2} \ . \tag{4-11}$$

The reactive power lower limit Q_{limit} that will result in maximum injected DG reactive power (to regulate the PCC voltage) is then related to the DG injected active power as

$$Q_{\mathrm{limit}} = X_{\mathrm{s}} \left(\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2 \right) - \frac{1}{2X_{\mathrm{s}}} \, . \tag{4-12}$$

Equation (4-12) is depicted in Fig. 4.7, where it shows again that the maximum power to be injected is inversely proportional to both the PCC voltage and the DG injected active power. The difference between the two curves in the figure indicates the necessary injected reactive power.

To investigate the effect of the loading on the compensation capability of the DG, it is now assumed that a static constant-power load is connected at

the PCC in Fig. 4.4. With a constant-power load, the power circles would be shifted up and/or to the right depending on the load reactive and active powers respectively. This should, in turn, increase the voltage compensation limit of the DG. However, an increased amount of the load reactive power, shifting the circles up, will imply more DG injected reactive-power to compensate for the voltage.

Assuming a constant active power load of 0.1 p.u., the operational part of the power circles relating the DG active and reactive powers to the grid voltage at the PCC is shown in Fig. 4.8. For instant, if the voltage at the PCC is 0.7 p.u. and the input DG active power is 0.8 p.u., then this will imply a stable operation with about 0.1 p.u. reactive power to be injected into the grid to regulate for the voltage.

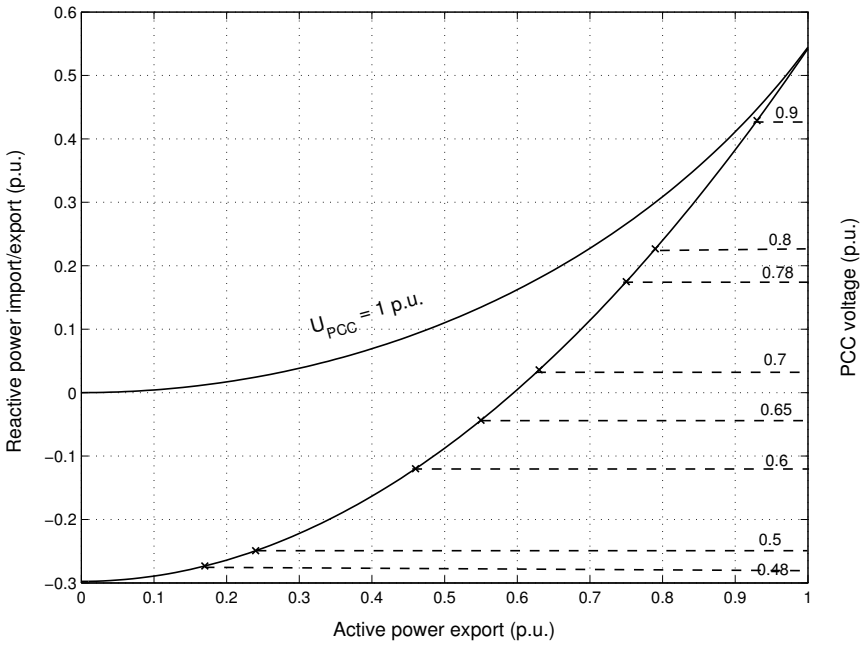

Fig. 4.7 Maximum reactive power (i.e. vertical difference between the two curves) to be injected related to the PCC voltage and the DG injected active power.

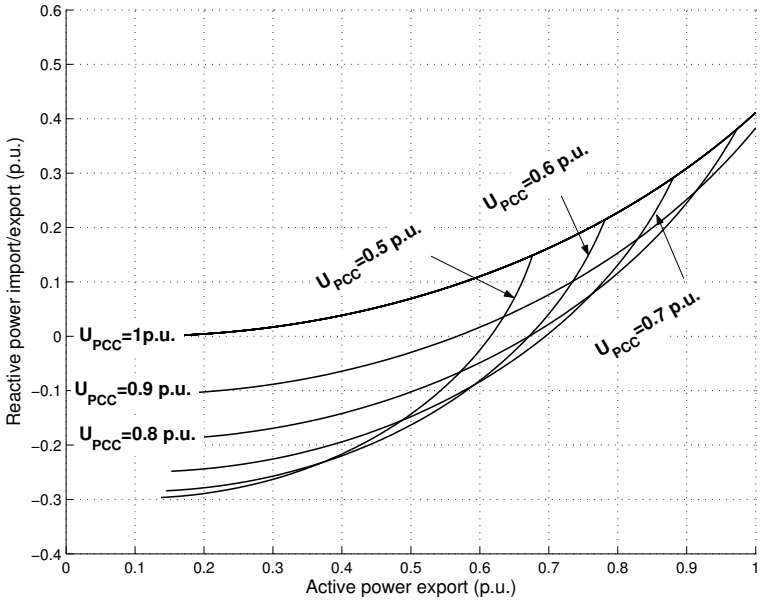

Fig. 4.8 DG import/export power with a constant power load of P_L = 0.1 p.u. and Q_L = 0.0 p.u.

It is worth noting here that the above discussion has been carried out assuming a lossless feeder. By decreasing the *X*/*R* ratio of the feeder, the resistive voltage drop will increase implying decreased PCC voltage related to the same loading condition. For instance, for a pure resistive feeder (Z_s = R_s) the equations for the active and reactive power flow through the feeder will be reversed. That means

$$Q_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}E}{R_{\mathrm{s}}}\sin\delta \tag{4-13}$$

$$P_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}^2}{R_{\mathrm{s}}} - \frac{U_{PCC}E}{R_{\mathrm{s}}}\cos\delta\,. \tag{4-14}$$

This implies that the voltage at the PCC will become more sensitive to the active power change and less sensitive to the reactive power change. This will result in an increased amount of the reactive power to regulate the

voltage compared to the case with a pure inductive feeder. Hence, the decreased *X*/*R* ratio will account for another limit for the regulation capability.

4.4 PCC-voltage regulator

The DG injected reactive power is adjusted by the PCC-voltage regulator to maintain the 1 p.u. grid voltage amplitude. The regulator has been implemented regarding the instantaneous reactive power generated by the DG at the PCC, which is described as

$$q_{(\mathrm{PCC})} = u_{\mathrm{q(PCC)}} i_{2\mathrm{d}} - u_{\mathrm{d(PCC)}} i_{2\mathrm{q}} . \tag{4-15}$$

Since the voltage-oriented synchronous-frame transformation sets the *q*-component of the voltage into zero, then $i_{2\mathrm{q}}$ is used to control the reactive power flow. Since $u_{\mathrm{d(PCC)}}$ is to be regulated, then the reactive current reference is generated to compensate the error in the voltage using a PI-controller[14], as follows

$$i_{2\mathrm{q}}^{*}(k) = k_{\mathrm{pr}} \varepsilon_{\mathrm{e}}(k) + \frac{k_{\mathrm{pr}} T_{\mathrm{s}}}{T_{\mathrm{ir}}} \sum_{n=1}^{k} \varepsilon_{\mathrm{e}}(n-1) \tag{4-16}$$

$$\varepsilon_{\mathrm{e}}(k) = u_{\mathrm{d(PCC)}}(k) - u_{\mathrm{d(PCC)}}^{*}(k) \tag{4-17}$$

where

k_{pr} is the proportional gain of the PCC-voltage regulator;

k is the sampling instant;

T_{ir} is the integral time; and

T_{s} is the sampling time.

Assuming, now, that the loading condition of the grid allows for a stable operation of the PCC-voltage regulator, the mitigation of the power quality problems at the grid is to be considered next.

[14] The controller parameters are given in Appendix D.

4.5 Compensation for grid-voltage harmonics

The effect of the voltage harmonics on the estimated phase using the PS-PLL is first discussed. If it is assumed that the voltage has a harmonic signal that is superimposed on the fundamental component, then it can be described in the αβ-frame as

$$\underline{u}_{\alpha\beta}(t) = U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \tag{4-18}$$

where

U_1 and U_h are the amplitudes of the fundamental and the h^{th} harmonic respectively;

ω is the fundamental grid-voltage angular-frequency; and

h_s is the related harmonic sequence that takes a value of either $+1$ (for positive sequence) or -1 (for negative sequence) according to [54]

$$h_s = \begin{cases} +1 & h = 3n+1 \\ -1 & h = 3n+2 \\ 0 & h = 3n \end{cases} \tag{4-19}$$

where n is a positive integer starting from zero.

The zero sequence harmonics will not be treated in this analysis due to the absence of a neutral wire.

Substituting (4-18) in (2-15), the positive-sequence vector of the grid voltage in $\alpha\beta-$frame is:

$$\begin{aligned} \underline{u}_{\alpha\beta\mathrm{p}}(t) &= \frac{1}{2}\left(U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t}\right) \\ &+ \frac{\mathrm{j}}{2}\left(U_1 e^{\mathrm{j}\omega(t-T_g/4)} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega(t-T_g/4)}\right) \end{aligned} \tag{4-20}$$

where $\dfrac{\omega T_g}{4} = \dfrac{\pi}{2}$.

The harmonic part of (4-20) can be expressed using trigonometric functions as follows

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = \frac{U_{\mathrm{h}}}{2}\left(\cos(h\omega t) + \mathrm{j}(h_{\mathrm{s}})\sin(h\omega t)\right) + \mathrm{j}\frac{U_{\mathrm{h}}}{2}\cos\left(h\omega t - h\frac{\pi}{2}\right) - (h_{\mathrm{s}})\sin\left(h\omega t - h\frac{\pi}{2}\right). \tag{4-21}$$

For the harmonics of the orders 5th and 7th, $\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}$ will be nullified since

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = -(h_{\mathrm{s}})\sin(h\omega t) \tag{4-22.a}$$

and

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = (h_{\mathrm{s}})\cos(h\omega t). \tag{4-22.b}$$

For harmonics of the orders 11th and 13th, the positive-sequence harmonic voltage vector will have the same amplitude as of the imposed harmonic signal and will rotate with the same angle. Equation (4-21) for the two harmonics will become

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = U_h e^{\mathrm{j}h_{\mathrm{s}}h\omega t}. \tag{4-23}$$

Since the 5th and 7th harmonics are the most dominant in the power system [54], it is expected that good results will be obtained using the PS-PLL in estimating the grid-voltage phase angle. Moreover, since the operation of the PS-PLL is similar to a LPF operation, the higher harmonics will be attenuated as well.

To investigate the capability of the voltage-harmonics compensation, a parallel RC-load is connected to the grid, through a diode rectifier, upstream of the DG. The phase-voltage at the PCC is shown in Fig. 4.9 before and after the connection of the DG. In addition, the harmonics content is also shown for both voltages in Fig. 4.10. The harmonics are comparatively negligible when connecting the DG, with the PCC-voltage regulation capability. For instance, the 5th harmonic component amplitude has decreased from about 9.5% without the DG to about 3% with the DG. This will result in a voltage that complies with the IEEE-std 1547-2003, which specifies the maximum harmonic voltage distortion as 4% for the harmonics' orders less than the 11th.

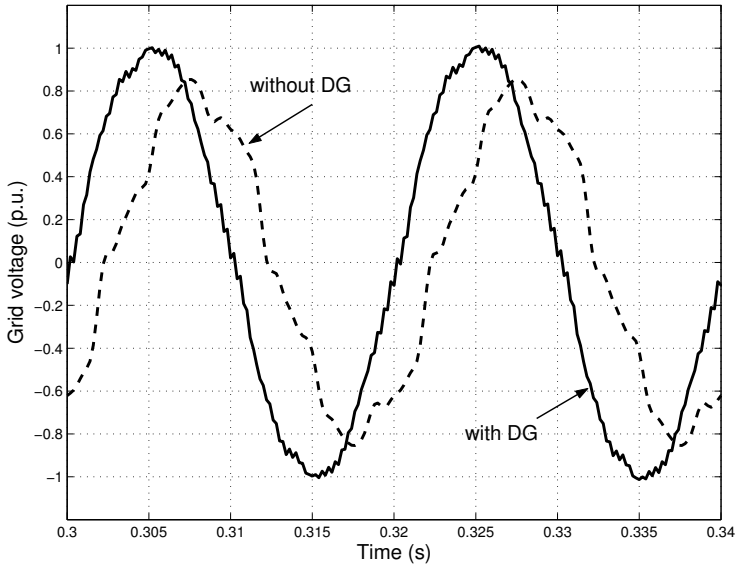

Fig. 4.9 Grid Phase-voltage with (solid) the DG and without (dashed) the DG.

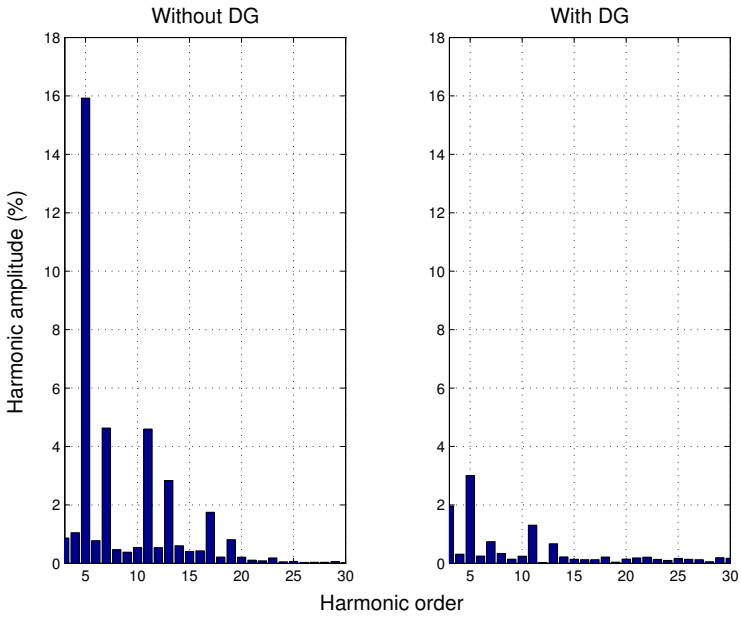

Fig. 4.10 Grid voltage harmonics content with the DG (right) and without the DG (left).

4.6 Compensation for grid-voltage fluctuation

Grid voltage amplitude fluctuations may result due to fast periodically-changing heavy loads that are connected to the grid [58]. If a distribution network is considered, one of the direct effects could be light flicker. The frequency of light flicker ranges between 0.5 Hz and 30 Hz, since this is the range of the human eye sensibility [59]. One way to mitigate this phenomenon is to compensate for the oscillating reactive power using a STATCOM [59] - [60], which is a three-phase VSC based device. The VSC-interfaced DG with the voltage compensation capability is considered here for that purpose.

Proposed PLL modification

The effect of the voltage amplitude modulation on the PS-PLL is first to be examined. For this purpose, a sinusoidal modulating signal is added to the voltage magnitude. With a variable voltage-amplitude, the q-component of the grid voltage will oscillate with the same frequency as the modulating signal. Substituting $h_s = 0$ and $h = 1/5$ (for 10 Hz amplitude modulation) in (4-21), it is obvious that the positive sequence will also be oscillating, producing an error in the estimated phase. To nullify this error and obtain a robust performance, the fundamental component of the grid voltage could be used, instead of the positive sequence component, as input to the Q-PLL. This has been implemented in [61] using two LPFs to extract both the positive-sequence and its fundamental component.

In order to cope with this situation, the adaptive linear neural network extractor (ADALINE) [62] is introduced next. A simple ADALINE consists of one neuron that has a linear input-output relationship, where each input is simply multiplied by a certain weight and all inputs are summed together to produce the output. The power of ADALINE comes from the on-line adaptation of its weights that gives it a non-linear property [62]. For this purpose, the least mean square (LMS) algorithm is used [63].

ADALINE has been implemented in [64] as a combiner to identify the voltage waveform for the classification of the power quality problems. It will

be used here in the same way, however, as an extractor to relieve the fundamental component of the source polluted voltage. The structure of ADALINE is shown in Fig. 4.11, where the discrete input vector $\mathbf{x}(k)$ is composed of sine and cosine elements of all possible frequency components that are contained in the source voltage

$$\mathbf{x}(k) = \left[\sin(\omega k T_s) \quad \cos(\omega k T_s) \quad \ldots \quad \sin(h\omega k T_s) \quad \cos(h\omega k T_s)\right]^T \tag{4-24}$$

where h is the highest harmonic order expected, k is the sampling instant, T_s is the sampling time, and the superscript T indicates the transpose of the vector. This input vector $\mathbf{x}(k)$ is then multiplied by a weight vector $\mathbf{w}(k)$ to produce the ADALINE output $u_{nn}(k)$, as follows

$$\mathbf{w}(k) = \left[w_{11} \quad w_{12} \quad w_{21} \quad w_{22} \quad \ldots \quad w_{h1} \quad w_{h2}\right] \tag{4-25}$$

$$u_{nn}(k) = \mathbf{w}(k) \cdot \mathbf{x}(k) = \sum_{i=1}^{2h} w_i x_i \tag{4-26}$$

where w_i and x_i is the i^{th} element in the vectors $\mathbf{w}$ and $\mathbf{x}$ respectively.

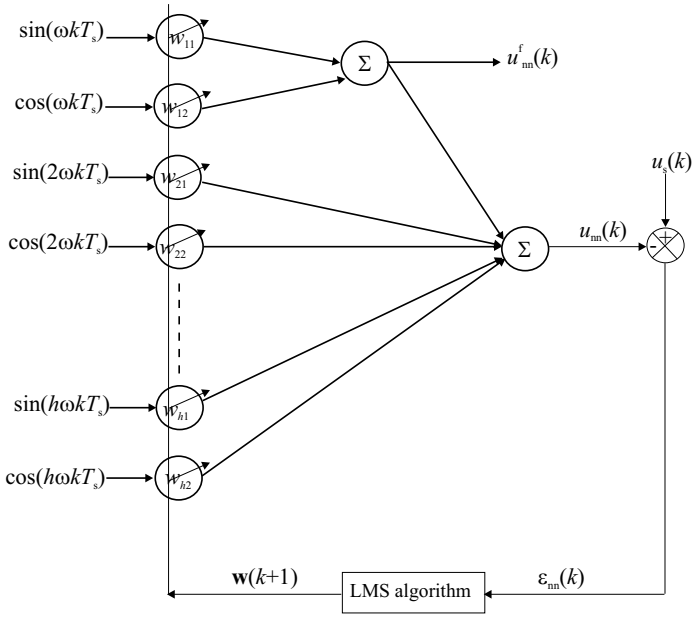

Fig. 4.11 The structure of the adaptive linear extractor (ADALINE).

The output is then compared with the measured and sampled voltage signal $u_s(k)$, where the resulting error ε_{nn} is used by the recursive algorithm to modify the weight vector according to

$$\mathbf{w}(k+1) = \mathbf{w}(k) + \lambda \frac{\mathbf{x}(k)\varepsilon_{nn}(k)}{\mathbf{x}(k)^{\mathrm{T}}\mathbf{x}(k)} \tag{4-27}$$

where λ is the learning factor. The size of λ determines how quickly old data are to be discarded. A small λ means that new data inputs will not have a significant weight and the system becomes less sensitive to disturbances, but also slower in reactions. On the other hand, a large λ makes the system react quickly, but responds more sensitively to disturbances[15].

The block diagram of the PLL implementing ADALINE (NN-PLL) is shown in Fig. 4.12. The three-phase voltage is transformed into the stationary $\alpha\beta$-frame. Then each component is fed into a separate ADALINE algorithm to extract the fundamental component that is fed into a Q-PLL.

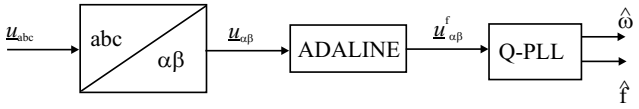

Fig. 4.12 Implementation of NN-PLL.

Performance of the proposed PLL

The performance of the NN-PLL is also compared to the PS-PLL regarding the grid voltage harmonics. The error in the estimated phase angle due to the grid voltage harmonics is shown in Fig. 4.13, using three different bandwidth values for the Q-PLL, for the two estimators. 2% amplitude of the 2nd, 4th, 5th, 7th, 11th and 13th harmonic orders has been superimposed separately on the fundamental grid-voltage. The phase error has been

[15] More discussion about the learning factor can be found in Paper E.

calculated as the peak-to-peak amplitude of the normalized quadrature-voltage.

With the PS-PLL, the error in the estimated phase-angle increases with higher values of the bandwidth. Moreover, the amplitude of the error increases with the increase of the harmonic order, excluding the case for the 5^{th} and 7^{th} harmonics at which it was proven that the error will be nullified. This can be understood by observing (4-17), where the harmonic order is in proportional relationship with the frequency of the oscillations superimposed on the fundamental grid-voltage.

Using the NN-PLL the error is nullified with all harmonic orders and all values of bandwidth, which means that it is robust and in the same time could have better dynamics. Moreover, the case of unbalanced harmonics has been examined with the same order of harmonics as before. Figure 4.14 shows that the NN-PLL is superior to the PS-PLL even when unbalanced 5^{th} and 7^{th} harmonics are present in the grid.

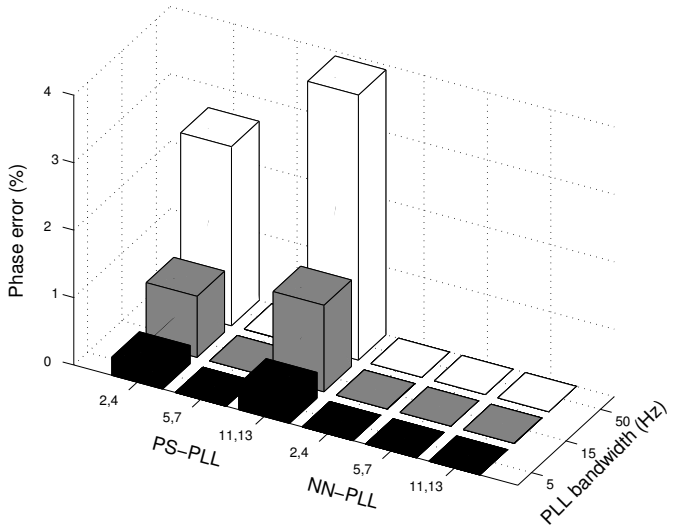

Fig. 4.13 Phase error due to different balanced harmonics using PS-PLL and NN-PLL with different BW values.

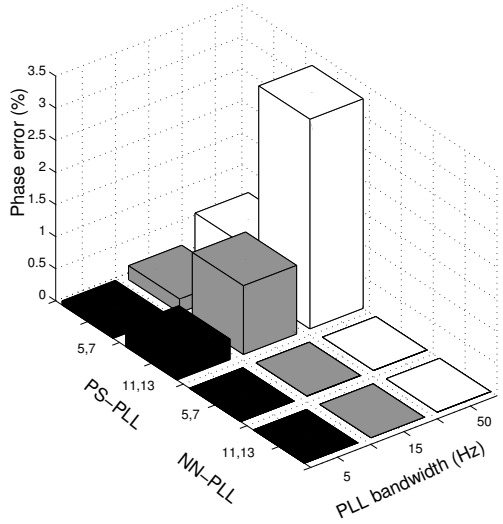

Fig. 4.14 Phase error due to different unbalanced harmonics using PS-PLL and NN-PLL with different BW values.

Mitigation of grid voltage amplitude fluctuation

The mitigation of the grid voltage fluctuation is to be examined. A fluctuating load is assumed to be connected at bus 1, in Fig. 4.4, and is further assumed to be disconnected in case of a fault at the same bus. Its effect is encountered as about 8% amplitude fluctuation of the grid voltage at bus 1 using a cosine modulation signal with a frequency of 10 Hz. In reality this modulation signal could have an infinite number of frequencies, but for the sake of clarity only a 10 Hz component is displayed here, which represents a value in the frequency band (between 2 and 15 Hz [58]) that the human eye is most sensitive to. The PCC-voltage is shown in Fig. 4.15 before the connection of the DG, and with the DG connected with the PS-PLL and the NN-PLL. From the figure, it can be concluded that the ability of the DG with an NN-PLL to mitigate the voltage fluctuation is better. The peak-to-peak voltage-envelope has been oscillating with 8% before the voltage compensation, and with 5% in case of voltage regulation using the PS-PLL and 3.5% in case of using the NN-PLL.

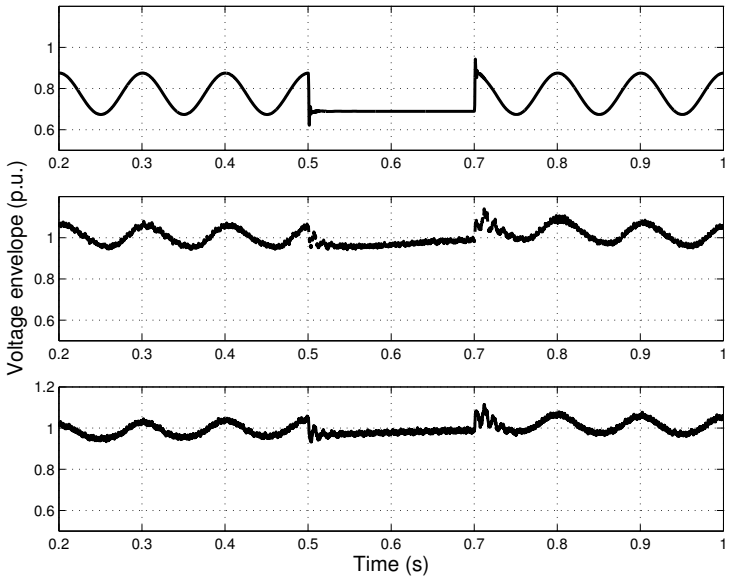

Fig. 4.15 Voltage envelop with DG disconnected (upper), DG with PS-PLL (middle), and DG with NN-PLL (lower).

Moreover, the voltage amplitude variation at the PCC has been tested with different modulation signal frequencies and the result is shown in Fig. 4.16, where the system using the NN-PLL has lower peak-to-peak value of the oscillation of the voltage envelope.

It is worth noting here that the oscillations of the voltage envelope will not be completely nullified since both the active and the reactive powers are oscillating at the grid, because of the modelling that is considered here. That means that both the injected active and reactive powers should be oscillating in order to completely compensate for the voltage fluctuation. However, this is not possible, here, since the application of the converter interfaced DG that is considered implies constant injected active power into the grid. On the other hand, the behaviour of the NN-PLL is dependent on the input-vector length, the order of harmonic frequencies used in that vector, and the initial weights' values. The input-vector length is taken, here, as 18 and the initial weight vector was set to zero. Using different setup for the ADALINE could give different results.

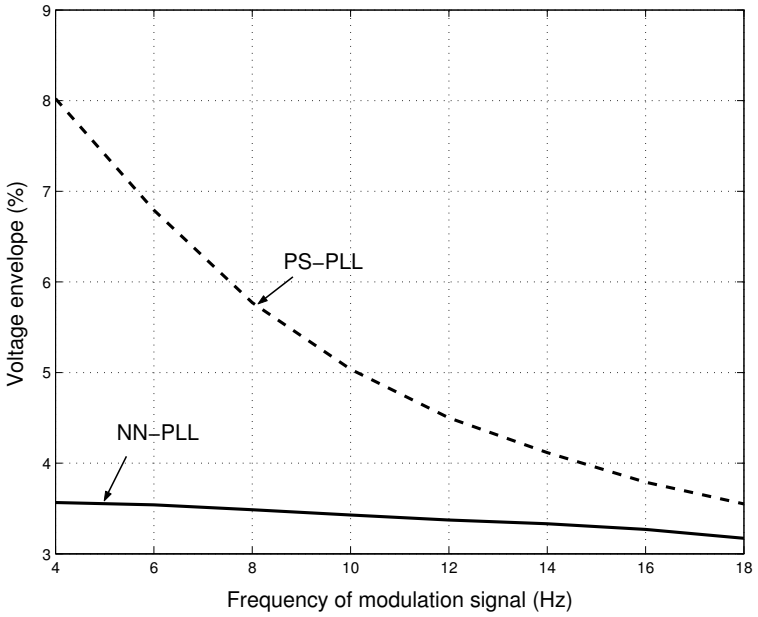

Fig. 4.16 Voltage amplitude variation owing to the change of the modulation signal frequency; with PS-PLL (dashed curve) and NN-PLL (solid curve).

4.7 Conclusions

The possibility to regulate the local voltage using a converter-interfaced DG has been discussed in this chapter. The aim is to maintain the voltage at its nominal value in case of operation in weak grids, and to mitigate the power quality problems at the point of common coupling (PCC). The voltage regulation capability has been investigated by studying the regulation limits regarding the DG injected power and the loading of the grid. The regulation capability is increased if the DG is injecting more active power into the grid and the load is mostly a constant active power load. However, this could require oversizing of the converter valves.

The PCC-voltage regulator sets the reactive current reference in such a way that the reactive power injected into the grid is controlled. The reactive current is represented by the quadrature-component of the measured current,

which is obtained through a coordinate transformation that uses an estimated angle that is obtained using a PLL. The error in the estimated angle could result in an erroneous reactive current command, which could affect the voltage compensation quality. For that purpose, the PLL algorithm has been discussed regarding the grid voltage imbalance, the grid voltage harmonics, and the grid voltage fluctuation. A neural-network based PLL (NN-PLL) has been proposed to extract the fundamental component of the grid voltage, and to estimate its phase angle. This NN-PLL has been compared with a previously investigated PLL algorithm (here referred to as PS-PLL), which estimates the phase angle of the positive-sequence component of the grid voltage. It has been shown that the NN-PLL is more robust against grid voltage harmonics. The NN-PLL has shown superiority also in the special case of unbalanced 5^{th} and 7^{th} harmonics in the grid voltage. In addition, the NN-PLL has proven to be better in case of grid-voltage fluctuation, where in a demonstrated case the oscillation of the voltage envelope has been decreased from 8% (without voltage regulation) to 3.5% (with voltage regulation and using NN-PLL), compared to 5% when using the PS-PLL.

Chapter 5

Intentional Islanding Capability

Intentional islanding refers to the case when the distributed generation (DG) is allowed to work autonomously to energize a part of the grid. For safe operation, detection methods should be applied to change the DG operating mode from grid-connected operation to island operation and vice-versa. Two different detection methods are described and examined in this chapter; namely passive and active methods. Their non-detectable zone is briefly discussed. The operation of the DG in both a strong grid and a weak grid has been examined in case of islanding.

5.1 Intentional islanding definition

Islanding refers to a condition in which a portion of the power system is energized by a local energy source, while it is electrically separated from the rest of the power system [65]. This situation, if not planned, poses a safety hazard to utility repair and maintenance personnel, and could lead to unstable island and instability problems when the utility grid is recovered [66].

Hence, islanding detection is an important aspect in DG applications. DGs should be able to detect the islanding condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, which specifies the acceptable clearing times as shown in Fig. 5.1. Yet, as recommended by the same standard, the detection could lead to an island operation of a DG, which is referred to as intentional islanding.

Besides enhancing the supply reliability for the utility grid [83] (e.g. in rural areas [4]), intentional islanding of DGs represents a required practice for some critical micro-grids [5], [84], [85]. Hence, developing reliable and robust islanding detection methods is of major importance.

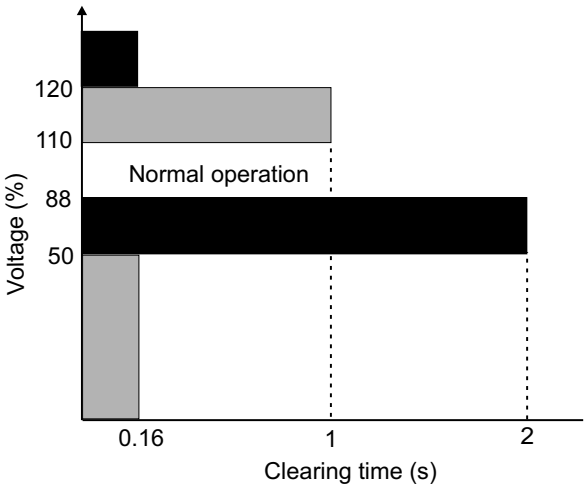

Fig. 5.1 Clearing time for a DG as described in IEEE-std 1547-2003.

5.2 Islanding detection methods

There are two types of islanding detection methods; passive and active. In passive detection algorithms, the sensed grid states (voltage, frequency … etc.) are compared with their nominal values and the deviations are used to decide on the islanding condition. For instance, in [10], the grid outage is detected using the phase angle error, between the grid voltage and the inverter voltage, which is compared to a set value to generate the disconnection signal. Then the DG operates in a stand-alone mode. When the grid is back, the increased currents are used to trip the DG. Then the DG is connected back to the grid after synchronization. Using the voltage phase-angle for islanding detection, however, may lead to false islanding in case of other power system dynamics [68]. Instead, in [40], both the voltage and the frequency are measured at the PCC to detect islanding. However, the effect of a voltage limitation, which could be incorporated in the converter controller for its safe operation, is not considered.

Although they are simple to implement, passive algorithms may fail to detect islanding if the load and generation on the island are closely matched

[67]. The active and reactive power mismatch limits that will lead to this situation are referred to as the non-detectable zone (NDZ) and they are calculated for current-controlled and power controlled DGs in [68] for different passive algorithms using an RLC-resonant load with a certain quality factor. It has been shown, in that reference, that the algorithms that are using the under/over frequency and/or the phase-angle jump are insensitive to active power mismatch. Moreover, the under/over frequency methods are, unlike the phase angle jump methods, dependent on the load quality factor. In addition, there are practical issues related to using phase-angle jump methods. Power system switching events, not resulting in islanding, can falsely trigger such schemes. When the islanding detection is delayed or not activated due to the NDZ, the DG system may lose control on its output terminal voltage, which may lead to island instability. In a way to overcome this problem and to provide seamless transfer between the grid-connected and island modes of operation, the island load (or emergency load) in [46] has been connected in parallel to the capacitor of the LCL-filter. Since the capacitor voltage is always controlled, even in the case of grid-detection failure, the load is not affected by the change of the DG operating mode, or the delay or mal-operation of the detection algorithm. However, this solution might not be feasible for all grids or loads. Another way is to decrease the NDZ by improving the detection method.

In active detection methods, the NDZ is very small [69]. Active techniques are usually incorporated within the controller, where they aim at disturbing the grid states by injecting disturbance signals. In the case of the utility supply outage, the island will be disturbed and the passive detection will succeed. In spite of the small NDZ, active methods may affect the power quality of the distribution system [39]. Moreover, in case of a weak grid system, active methods may lead to false tripping.

Hence, the passive islanding-detection method is considered first since it is the main islanding decision maker. Then, an active islanding detection method is introduced for the operation of the DG in both a strong and a weak grid.

5.3 Passive islanding-detection

A passive islanding detection algorithm has been developed to detect both the grid outage and recovery. To evaluate the grid states that could be reliable enough to be used in the detection algorithm, the grid outage is first considered.

The effect of the grid outage on the PCC-voltage

At the moment of the grid outage, the voltage at the point of common coupling (PCC) will either increase or decrease instantly depending on the sign of the power mismatch (ΔP and ΔQ in Fig. 5.2). The power mismatch represents the amount of power that the grid either delivers or absorbs in the normal operation. This power is equal to the power absorbed by the load at the PCC subtracted from the power injected by the DG, as designated in Fig. 5.2[16]. If the DG injected power is higher than the load absorbed-power, then the PCC-voltage will increase implying increased $u_{\mathrm{d(PCC)}}$. In that case, the increase of the voltage will be limited by the voltage limitation algorithm incorporated in the DG controller. Regarding the algorithm that has been implemented here, $u_{\mathrm{d(PCC)}}$ will be limited to $\frac{u_{\mathrm{dc}}}{\sqrt{2}}$ as has been shown in Section 2.2.

This case is presented in Fig. 5.3, where the grid outage occurs at 0.4 s. The DG controller that has been tested here has the PCC-voltage regulator and the DC-link voltage regulator incorporated. Hence, the *d*-component of the DG injected-current is controlled to be constant to keep the DC-link voltage constant, as shown by the lower plot in Fig. 5.3, while the *q*-component of the current starts to decrease in magnitude after the grid outage to retain the voltage at its nominal value. Since the PCC-voltage amplitude is limited (due to both the limiting algorithm and the operation of the PCC-voltage regulator), this increase in the grid voltage could also correspond to any other dynamics at the grid (e.g. load disconnection), then the over-voltage state cannot be a measure for islanding.

[16] The feeder parameters are given in Appendix C.

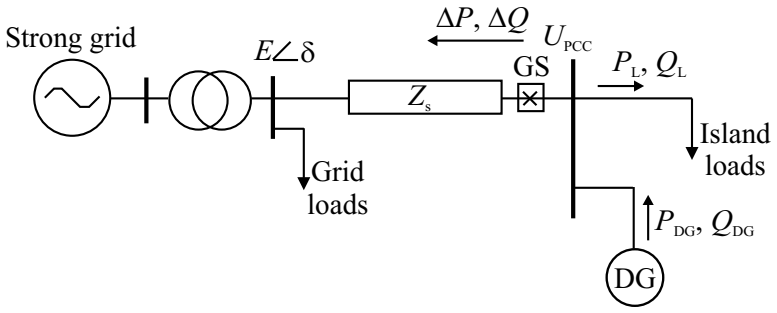

Fig. 5.2 System considered for islanding study.

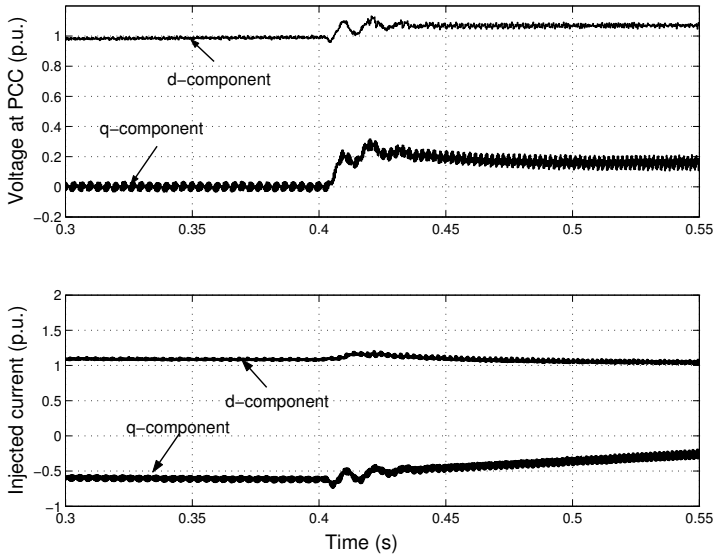

Fig. 5.3 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.4 s and $P_L < P_{DG}$.

If the load absorbed power is higher than the DG injected-power (in which case a load shedding criterion is important for a stable island operation), the PCC voltage will decrease in case of the grid outage. This case is represented in Fig. 5.4, where the grid outage occurs at 0.3 s, and the load active power is higher than the DG active power ($P_L = 1.07P_{DG}$) while the reactive power for both the load and the DG are equal. The DG controller, here, injects constant current into the grid, as shown by the lower

plot in the same figure. Since this decreased voltage could occur also due to voltage dips at the grid, hence the undervoltage is not a reliable state for islanding detection especially if the voltage dips ride-through capability is required. In other words, using the undervoltage state for the islanding detection may lead to false tripping during voltage dips.

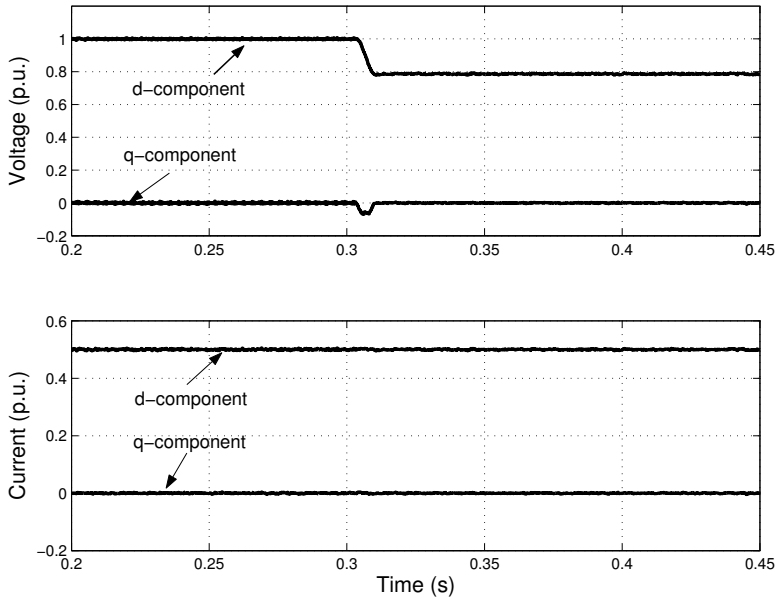

Fig. 5.4 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s and $P_L > P_{DG}$ (ΔP = -0.07 p.u.) and $Q_L = Q_{DG} = 0$.

In conclusion, an overvoltage/undervoltage islanding detection algorithm is not appropriate to be implemented. In addition, measuring other grid states (e.g. the phase angle jump) within a narrow threshold may falsely lead to islanding in case of other grid dynamics (e.g. switching events) [68].

Instead, using the signals generated within the DG controller to detect the islanding condition is considered. A disturbed signal within the controller will lead to a disturbed operation of the DG unit, and hence changing the control mode might be a good practice (even if the utility grid is not

disconnected). For instance, due to the grid outage and the reactive-power mismatch a constant nonzero value of the q-component of the voltage at the PCC will result (e.g. as shown in Fig. 5.3). This will cause an integrator windup of the PLL that in turn will result in a continuous increase (or decrease) in the estimated frequency as shown in Fig. 5.5 for a grid outage at 0.4 s. Hence, the estimated frequency signal is implemented here to detect the grid outage. This is done by assigning a threshold band for the estimated frequency. If the frequency crosses the band for a certain period of time, then the islanding condition is detected. For example, if the detection limit is set to 52 Hz then the islanding conditions are detected within 0.03 s.

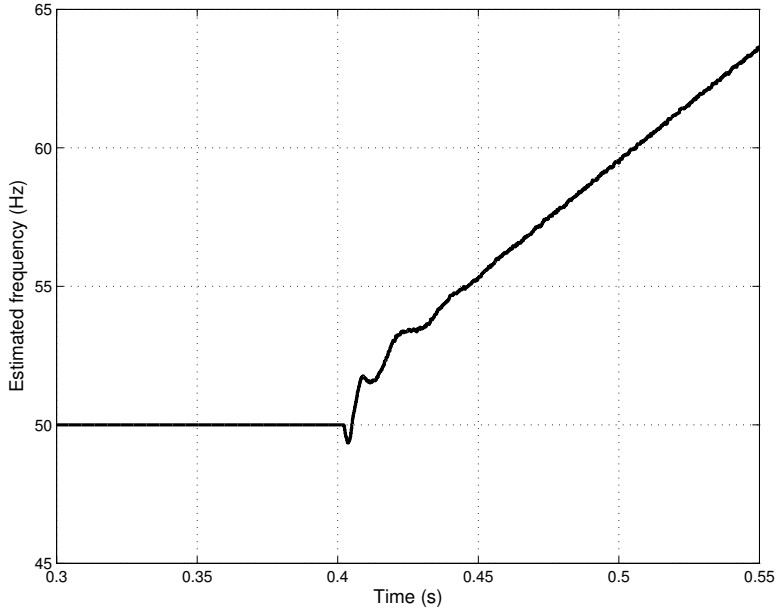

Fig. 5.5 Estimated frequency; grid outage at 0.4 s (P_L<P_{DG}).

To detect the grid recovery, the voltage measurement on the grid side of the grid switch (GS), shown in Fig. 5.2, is needed. If the voltage is back an extra PLL is used for the synchronization between the DG-output voltage and the grid voltage before connecting back the island to the grid.

Passive detection algorithm

The passive detection algorithm, which is implemented here, is shown in Fig. 5.6. Starting from the parallel (or grid-connected) operation, where the DG is aiming at controlling the active and reactive currents injected into the grid, the detection algorithm will be activated to detect the grid outage. The algorithm uses the deviation between the estimated frequency signal, which is produced by the PLL, and the nominal value. A time threshold t_s is also incorporated to avoid false tripping due to load dynamics. This time threshold is set equal to the settling time of the PLL, which could be calculated using the PLL gain as follows

$$t_s = \frac{\ln 50}{k_{pll}} \tag{5-1}$$

where the settling time is defined as the time for the PLL output to settle down to within a tolerance band of 2% of the final value [70], and k_{pll} is the proportional gain of the PLL.

Once the islanding condition is detected, the DG starts an island operation mode where its aim is to hold the voltage and frequency at their nominal values as well as to adjust the injected active and reactive powers to support the island loads. In addition, the GS is used to disconnect the utility grid from the island for safety operation. A DC chopper is also needed to consume the extra power that could be coming from the primary energy source in a way to adjust the input power to match the load needs. Moreover, in this mode, the grid recovery detection is activated where the voltage on the grid side is sensed. Once the utility grid is recovered, the synchronization between the DG voltage and grid voltage is carried out using an extra PLL on the grid side. The connection to the grid is then done by enabling the GS and disabling the DC chopper.

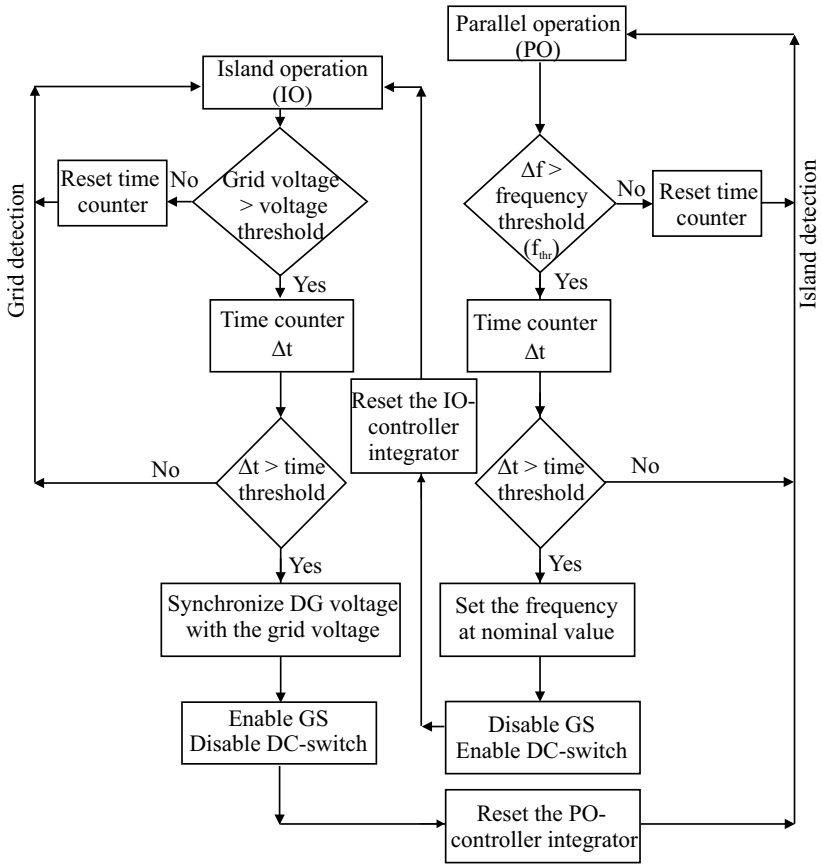

Fig. 5.6 Passive detection algorithm.

5.4 Non-detectable zone for passive detection

The non-detectable zone (NDZ) is usually described by the limits of active and reactive power mismatch (ΔP and ΔQ in Fig. 5.2) in which the detection algorithm would fail to recognize the grid outage [68]. These limits are related to the load characteristics, the detection method, and the controller of the DG.

The above described passive detection algorithm suffers from an open limit for ΔP in the NDZ. In other words, if the load reactive power exactly

matches the DG-injected reactive power, then, in case of the grid outage, the *q*-component of the PCC-voltage will not change irrespective of the amount of ΔP. This leads to undetectable islanding whatever the load active power is.

This case has been shown in Fig. 5.4, for $P_L > P_{DG}$ and constant active and reactive powers that are injected by the DG. Incorporating a PCC-voltage regulator within the DG controller, the change in the *d*-component of the PCC-voltage will lead to a change in the injected DG reactive current. Since the PCC-voltage will keep its decreased (or increased) value, due to the grid outage, the injected reactive current will keep a constant value (in case the DG is operating towards a strong grid) that will produce a reactive power mismatch and a change in the *q*-component of the PCC-voltage. This case is represented in Fig. 5.7, for the same loading condition as in Fig. 5.4. With the change in the *q*-component, an integrator windup in the PLL will result. Hence, the estimated frequency, shown in Fig. 5.8, will drop instantly leading to successful islanding-detection. As an example a frequency threshold of 48 Hz is detected within 0.01 s. This will lead to the decrease of the NDZ since either the active or reactive power mismatches will lead to a successful islanding detection.

In conclusion, combining the passive islanding-detection with the PCC-voltage regulator, described in Section 4.4, results in decreased NDZ. However, a complete match between the load and the DG unit active and reactive powers ($\Delta P = \Delta Q = 0$) would not be detected, since neither the *d*-component nor the *q*-component of the PCC-voltage would be affected by the grid outage. In this case, an active detection algorithm that injects a disturbance signal would be beneficial especially in case of a strong grid.

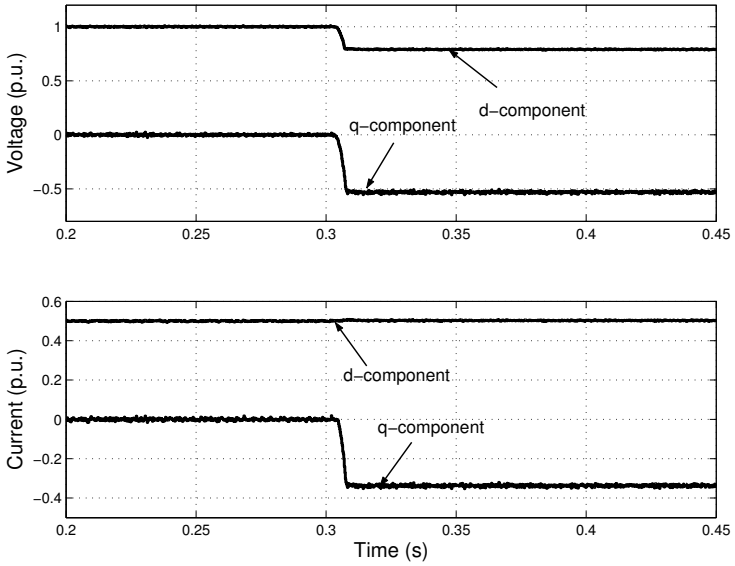

Fig. 5.7 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s; current-controlled DG with voltage regulation capability, and $P_L > P_{DG}$ ($\Delta P = -$ 0.07 p.u.).

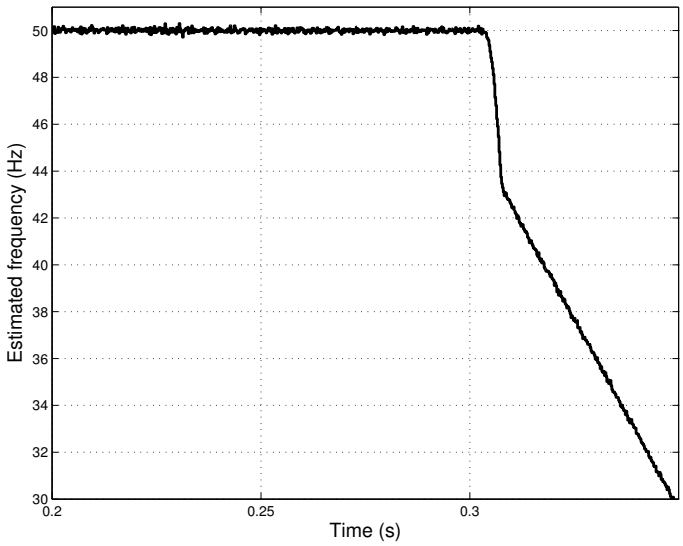

Fig. 5.8 Estimated frequency; grid outage at 0.3 s and current-controlled DG with voltage compensation capability, and ($\Delta P = -$ 0.07 p.u.).

5.5 Active Detection

The idea of the active detection is to try to disturb the grid in such a way that the passive detection will succeed to operate in the NDZ [69]. In a way to implement that, the active frequency drift method has been used in [79] and [43]. In this method, the waveform of the injected current is slightly distorted such that when islanding occurs the frequency of the phase voltage will drift up or down. Islanding is done in [43] by incorporating a washout function in the PLL that determines the change in the frequency and adds it to the frequency reference. Instead, in [39] a band pass filter is used, with the *d*-component voltage as an input, to deviate the voltage from its nominal value by changing the switching duty cycles.

In a way to optimize the design of the DG controller, the active detection is implemented here, using the PCC-voltage regulator. In case of a strong grid, the reference voltage signal in the PCC-voltage regulator is set to a value that is less than 1 p.u., while in case of a weak grid the reference voltage is set to 1 p.u.

The PCC-voltage regulator that is devoted for the operation in a strong grid is shown in Fig. 5.9. It operates in a way to produce a reactive current command i_q^* in such a way to force the voltage to deviate from its nominal value. The reference signal e_{dset} is set to a value that, when compared to the PCC-voltage e_d, produces an injected current within the maximum current limit of the DG. The limiter in the figure resets the integral part of the PI controller so that the current reference changes in a narrow band in order to decrease the current harmonics injected to the grid.

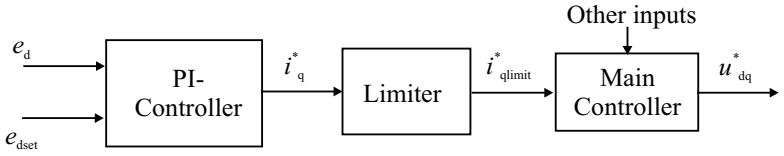

Fig. 5.9 Active islanding detection (PCC-voltage regulator).

The effect of adding the active islanding detection using the PCC-voltage controller is examined using a load that completely matches the DG power input (i.e. $\Delta P = \Delta Q = 0$). The DG injected active (*d*-component) and reactive (*q*-component) currents are shown in Fig. 5.10, without incorporating the active detection part (in the upper plot) and with incorporating it (in the lower plot), for a grid outage from 0.3 s to 0.4 s. From the figure, the increased value of the injected reactive current, in case of incorporating the active detection controller, implies producing a reactive power mismatch, in the normal operation, that in turn results in an islanding signal from the passive detection algorithm in case of grid outage.

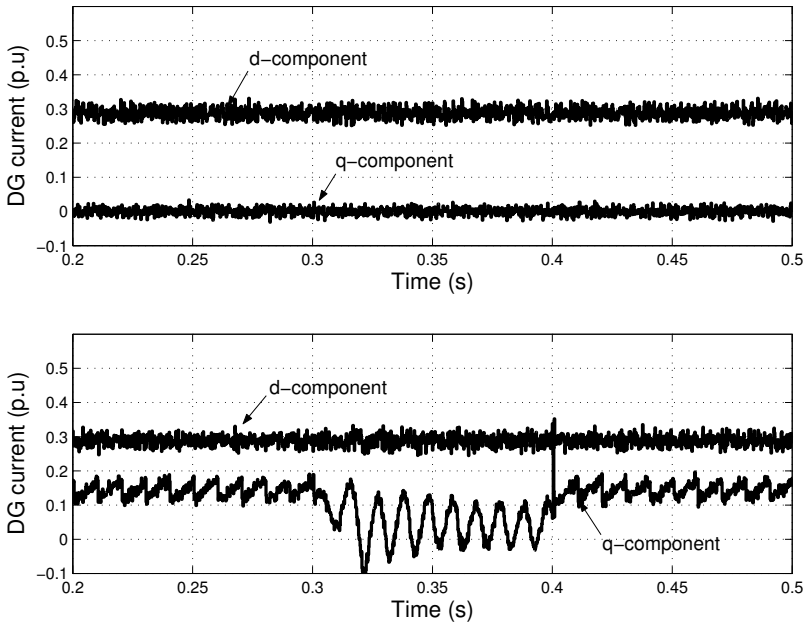

Fig. 5.10 DG injected active (d-component) and reactive (q-component) currents; without active detection controller (upper) and with active detection controller (lower) with a matching load.

The effect of using the active detection controller (i.e. the PCC-voltage controller) is also examined in case of a weak grid using a quadratic voltage dependent load that produces active power mismatch (ΔP) of 0.15 p.u. and

zero reactive power mismatch (ΔQ = 0) at the normal operation. A grid outage at 0.8 s is encountered. As shown in Fig. 5.11 (a) by the dashed line, the estimated frequency has a constant increase after 0.8 s, with the PCC-voltage regulator deactivated, due to a small change in the reactive power of the load that is in turn resulting from the increase of the PCC voltage, as shown in Fig. 5.11 (c). This increase in the estimated frequency could be relatively small and, depending on the frequency threshold set in the passive detection algorithm, it might not successfully detect the islanding condition. By activating the PCC-voltage regulator, the estimated frequency will continue to increase, as shown in Fig. 5.11 (a) by the solid line, after the grid outage at 0.8 s, due to the continuous increase in the DG injected reactive current that is shown in Fig. 5.11 (b), implying the successful detection of the islanding condition.

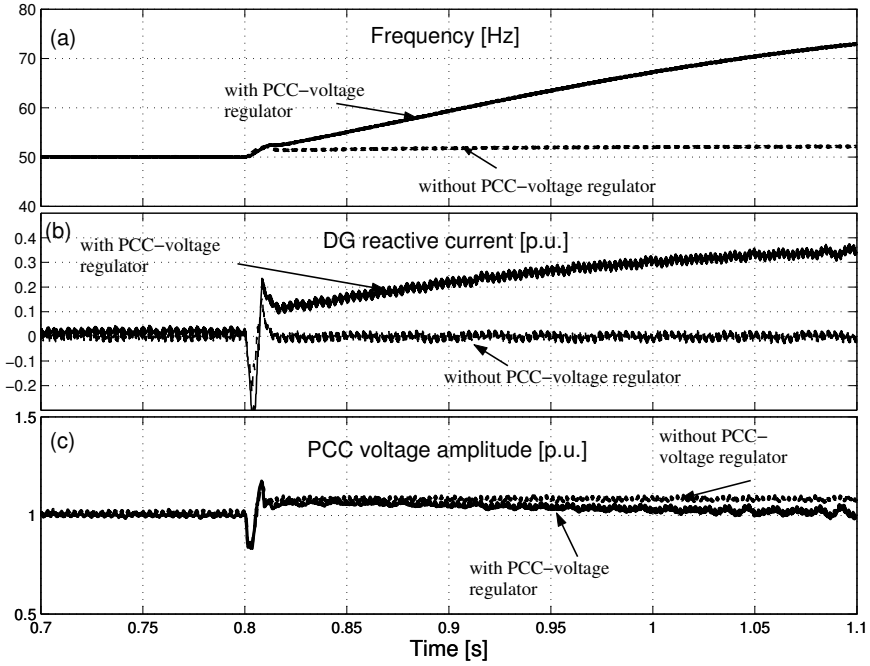

Fig. 5.11 Grid outage at 0.8 s, for ΔP = 0.15 and ΔQ = 0, with and without the PCC-voltage regulator. (a) the estimated frequency. (b) The DG injected reactive current. (c) The PCC-voltage amplitude.

The active detection method, using both the passive detection algorithm and the PCC-voltage regulator, are now to be examined.

5.6 Intentional islanding in a strong grid

A strong grid system is referring to a power system where the voltage and frequency at the load bus are kept constant, by the utility, regardless of the load dynamics. The system shown in Fig. 5.2 is considered where the PCC-voltage amplitude is kept constant at 1 p.u. during normal operation. The DG system is assumed to have an L-filter to smoothen out the current harmonics, and the DC-side is assumed to be controlled from the DG energy-source side for simplicity.

The DG controller will work on either one of the two operations; current-controlled or voltage-controlled, depending on the state of the utility grid as shown in Fig. 5.12.

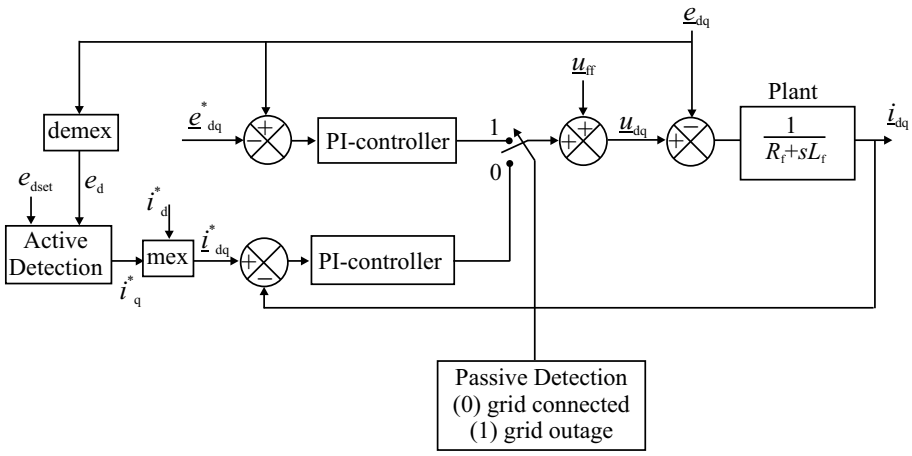

Fig. 5.12 Control transition between grid-connected and island modes.

The grid state is detected using the passive detection algorithm, shown in Fig. 5.6. In case of the grid outage, the detection algorithm will set the controller on the voltage control mode. In this mode the voltage nominal value is set as reference and compared with the measured voltage signal using a PI-controller. The output of this controller is added to the

feedforward voltage vector $\underline{u}_{ff}$. When the grid recovery occurs, the current controller will be activated. Moreover, the active detection is also incorporated in the controller in order to minimize the non-detectable zone as discussed before.

The island loads are set to draw higher power than the DG injected power, as described before for the case related to Fig. 5.4, to test the islanding detection and operation. It is assumed in this case that the energy source of the DG can inject more power to match the load in case of the occurrence of islanding (otherwise a load shedding criterion should be implemented). A grid outage has been encountered at 0.4 s, and the recovery of the grid occurred at 0.6 s. The controller has detected the outage and a transition to the voltage control mode has been performed, where the voltage has been set to 1 p.u., as shown in Fig. 5.13.

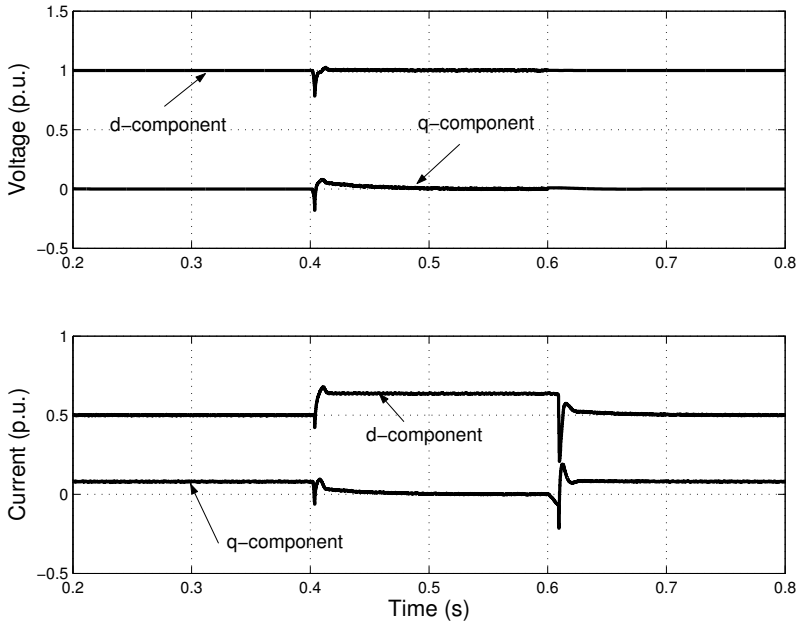

Fig. 5.13 PCC-voltage (upper), and DG injected currents (lower) in case of grid outage from 0.4 s to 0.6 s.

Before islanding, the *d*-component current has been set to 0.5 p.u., as shown by the lower trace of the same figure, while the *q*-component current i_q has been adjusted by the active detection controller to reduce the PCC-voltage *d*-component to 0.95 p.u. (i.e. e_{dset} = 0.95 p.u.). At the grid outage (at 0.4 s), i_q will start to change in a way to put the PCC-voltage amplitude to e_{dset}. However, this will change also the *q*-component of the voltage, which in turn will affect the estimated frequency as shown in Fig. 5.14 by the upper plot. This will lead to the setting of the passive detection signal, as shown in the same figure by the lower plot. Hence, the grid outage is detected and the grid switch GS is disconnected.

During the island operation, the DG injected currents will be set to match the load requirements. Moreover, the voltage angle is set to the reference value. When the grid is back, the voltage on the grid side of the GS will be sensed, and an extra PLL is used to synchronize the island back to the grid, then the GS is connected.

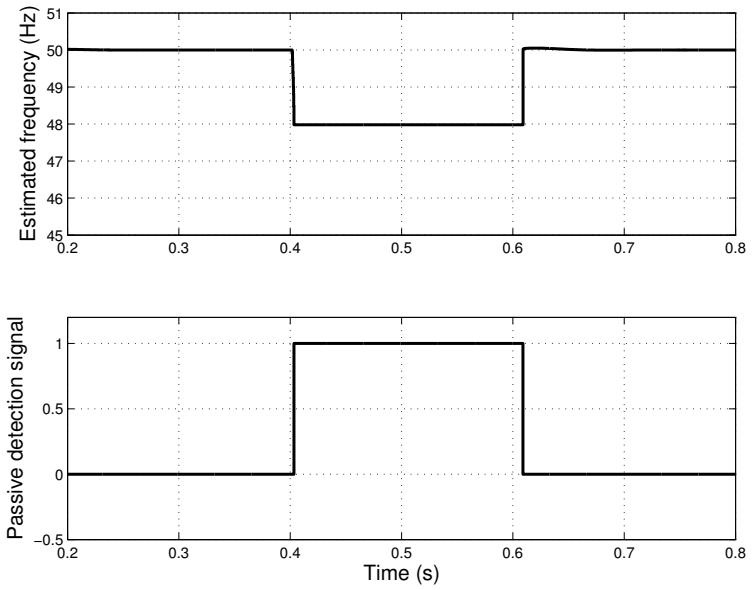

Fig. 5.14 Estimated frequency (upper), and passive detection signal (lower) in case of grid outage from 0.4 s to 0.6 s.

5.7 Intentional islanding in a weak grid

A weak grid system is referring, here, to systems where the voltage level at the load bus is not constant and is affected by the load dynamics. The system in Fig. 5.2 will be considered, where the voltage at the PCC is affected by the feeder voltage drop and the load dynamics. The island-loads are set such that their consumed power is lower than the DG-injected power. They are implemented as an aggregated quadratic voltage-dependent load, with a nominal active power mismatch (ΔP) of 0.55 p.u. and reactive power mismatch (ΔQ) of 0.2 p.u.

As has been discussed in the previous chapter, the voltage regulation capability of the DG is advantageous in the operation of weak grids since it will maintain the PCC voltage at the nominal value regardless of the load dynamics. Another advantage is highlighted here regarding the islanding. With the voltage regulation capability, the islanding non-detectable zone is reduced. This is especially important in the application of weak grids, since the active detection methods, which aim at disturbing the grid states, are not adequate for such grids since, during normal operation, the weak grid states (as opposite to strong grids) are changeable.

The DG system is considered here with the VSC as a front end and an LCL-filter to damp the line current harmonics. The grid-connected controller for this system has been described before in Section 2.6. The island-operation controller is shown in Fig. 5.15[17], where the voltage reference and the phase angle reference are set to their nominal values. A DC-link chopper is incorporated to dissipate the extra power that would come from the DG energy-source, in order to adjust the DG injected-power to match the load requirements.

The PCC-voltage is shown in Fig. 5.16, in the upper plot, for the operation of the DG before, during, and after islanding. The grid is disconnected at 0.3 s and recovered at 0.5 s.

[17] This controller has been explained in more details in Paper F.

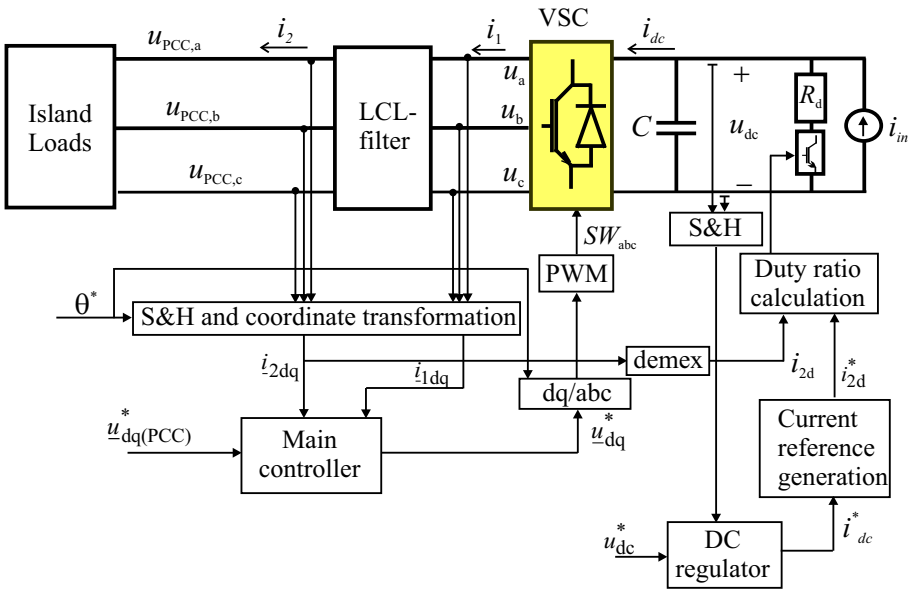

Fig. 5.15 Island operation controller for DG with LCL line filter.

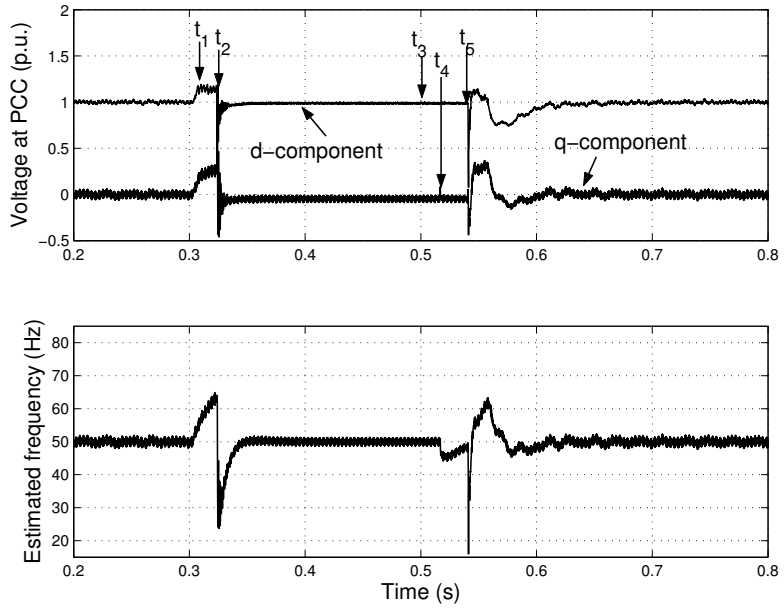

Fig. 5.16 Voltage in *dq*-frame at the PCC (upper) and estimated frequency (lower) for grid outage at 0.3 s and recovery at 0.5 s.

When the grid outage occurs at 0.3 s, the PCC voltage starts to increase in magnitude. When the *d*-component of the PCC-voltage $u_{d(PCC)}$ reaches the voltage limit, that is set by the controller, at t_1, the constant-limited value is maintained (until t_2). The frequency, which is shown by the lower plot of the same figure, will continue to increase after t_1, due to the constant value of the voltage *q*-component, until the island is detected at t_2. The detection algorithm will start to react after reaching the time threshold t_s, when the detection signal is activated (at t_2), resulting in transferring the controller from grid-connected mode to island-operation mode. At t_2 the frequency will be reset to its nominal value, and the DG injected powers, which are shown by the upper plot in Fig. 5.17, will start to adjust to match the load requirements. In consequence, the injected currents will decrease in magnitude, as shown in Fig. 5.18. Moreover, the DC-link voltage, which is shown in Fig. 5.17 by the lower plot, will maintain its nominal value in spite of the decreased injected DG-active power to the grid, since the DC chopper switch has been activated to dissipate the extra power in the chopper.

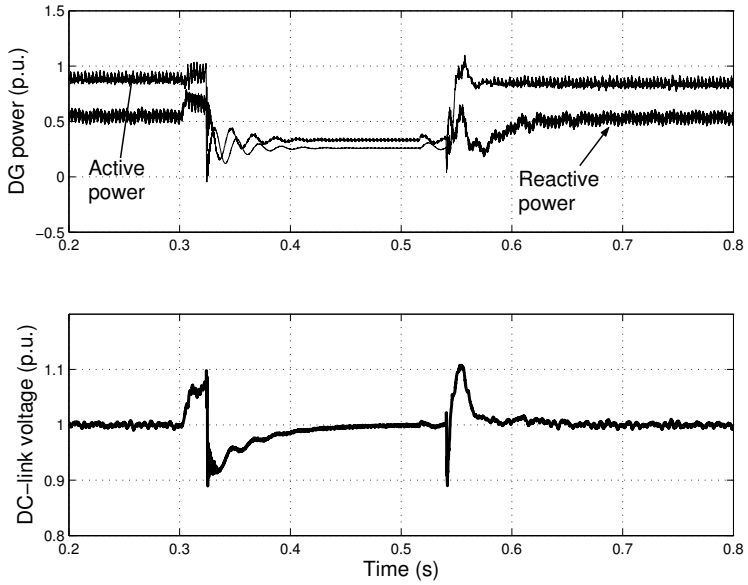

Fig. 5.17 DG injected power (upper) and DC-link voltage (lower) for grid outage at 0.3 s and recovery at 0.5 s.

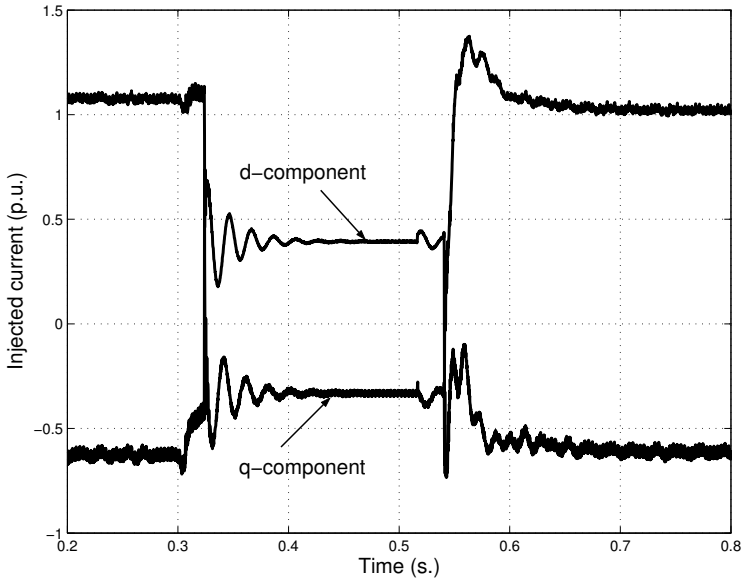

Fig. 5.18 DG injected current in dq-frame; grid outage at 0.3 s and recovery at 0.5 s.

When the grid voltage is recovered at t_3, a time threshold is also encountered before the synchronization of the grid voltage and DG voltage starts at t_4. This is done by using an extra PLL that is implemented for the voltage before the grid switch (GS in Fig. 5.2) from the utility grid side. At t_4, the phase angle of the DG voltage is set equal to the phase angle of the grid voltage. This could be seen from the change of the frequency signal in Fig. 5.16. After about one cycle of the fundamental frequency, the island is connected back to the utility grid at t_5. The DC-chopper is left in operation to buck the over-voltage that could occur at the starting of the grid-connected controller mode, until the PCC-voltage is stabilized.

At the starting of the grid-connected operation, $u_{d(PCC)}$ will drop to a value that represents its normal amplitude in case of deactivating the voltage regulator of the DG. This is mainly due to the PCC-voltage regulator transient time, which has been set long enough to stabilize the overall DG controller. In spite of the decreased value of the voltage during this time, the duration is very small compared with the clearing times that are shown in Fig. 5.1. After the transient time of the PCC-voltage regulator, the PCC-

voltage amplitude will be regained to the nominal value. In addition, the DG injected powers and currents will regain the values that are set for the grid connected operating mode.

5.8 Islanding detection reliability

Voltage dips appearing at the PCC, due to remote faults or motor starts, may lead to false tripping of the DG. The reason is that for small voltage dip amplitudes, the PCC voltage regulator may become unstable resulting in a disturbed PCC voltage that in turn will result in islanding. For instance, referring to Fig. 4.6 with a DG injected active power of 0.8 p.u. and a voltage dip magnitude of 0.7 p.u., the voltage regulator will become unstable and islanding will be detected for this case. Decreasing the DG input power would result in improving the voltage dip ride-through capability (as has been discussed in Chapter 3) and the reliability of the islanding detection.

Moreover, the effect of limiting the VSC current on the estimated frequency in case of voltage dips at the grid with induction motor loads at the PCC has been discussed in [81]. For sufficiently high current limit, the controller is able to maintain the voltage and frequency at the PCC at their nominal values. That would imply robust islanding detection.

The effect of setting a reactive current limit on the robustness of the islanding detection has been, also, discussed in Paper G, where the island loads have been implemented as an induction machine load. By setting the proper current limit, the DG unit can have the ability to ride-through voltage dips with magnitudes above a certain limit, which can be set according to the grid codes, and detect islanding for voltage dips with magnitudes lower than that limit.

5.9 Conclusions

In this chapter, the possibility of intentional islanding has been discussed. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection method should be applied. The islanding detection technique should be able to differentiate between grid dynamics and the islanding condition, and to provide the correct detection signal irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch. The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC). The NDZ, for the converter-interfaced DGs, also depends on the control method.

Two islanding methods have been introduced here; namely passive and active. An active islanding detection method has been proposed to minimize the inherent NDZ of the passive technique. In this method, the estimated frequency signal has been used to detect islanding along with the PCC-voltage regulator. This detection method is motivated by the operation of the DG in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the same method can be used by changing the reference value of the PCC-voltage regulator so as to produce a disturbing current signal in the grid.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The main focus of the thesis has been put on the study of the interface requirements and capabilities of a DG with a voltage source converter (VSC) as a front end. Two line filters have been considered at the connection point of the DG; namely an inductance line filter (L-filter) and an inductance-capacitance-inductance line filter (LCL-filter).

Vector current controller (VCC)

In the first place, **vector current controllers (VCC)** have been implemented, in the rotating synchronous *dq*-frame, for both systems. The time delay, with one sample length, that results due to the calculation time has been compensated for using a Smith predictor, which predicts the grid currents one sample ahead. In addition, the controller saturation, which could result due to high current steps, has been avoided using a voltage limiting algorithm. Besides, to avoid integrator windup, which also could result due to high current steps, the limited voltage has been used in the Smith predictor to recalculate the currents. A DC-link voltage regulator has been also incorporated in the controller to protect the capacitor on the DC-side during different load changes. Moreover, a dual vector current controller (DVCC) has been implemented, which comprises two VCCs. One of them is described in the positive rotating *dq*-frame and the other is described in the negative rotating *dq*-frame, to improve the performance in the case of unbalanced grid-voltage. Moreover, convenient current reference equations have been derived based on the power balance between the DC-side and the

AC-side of the VSC. The controllers have shown good current reference tracking even when high current steps are applied. In addition, in case of unbalanced grid-voltage, oscillating powers will be produced. When those powers are forced to be supplied from the grid side, it has been also shown that the DC-link voltage oscillations are negligible.

Voltage dips ride-through capability

Furthermore, the current-controlled converter interfaced DG has been studied in relation to different grid interface issues. First the **voltage dips ride through capability** has been discussed. For that purpose, a previously investigated voltage dips classification has been adopted to study the effect of all the possible voltage dips that could appear at the DG terminals. In addition, that classification has been modified to be implemented in the positive and negative sequence *dq*-frames. The equations of the maximum currents that would flow through the VSC valves due to all possible voltage dips have been derived. It has been shown that these analytical expressions give almost the same maximum current values as the numerical calculations based on simulation. It has been shown that if the converter-interfaced DG should ride-through the dip period there are two alternatives. One is to oversize the converter switches to withstand the increased currents. The other is to decrease the power input from the source during the dip period, so that the currents will be decreased. However, the latter would require that the input power to the DC-link be reduced very quickly, which could be an issue regarding the energy source or the control of an energy storage connected to the DC-link.

Voltage regulation capability

Thereafter, the **voltage regulation capability** has been discussed. This capability is beneficial if the compensation for the grid voltage quality problems is required. With this capability, the compensation of voltage dips, voltage harmonics, voltage amplitude modulation … etc. would be possible resulting in better power quality at the grid. Moreover, if the DG is working towards a weak grid, where the voltage level is dependable on the load

dynamics, this capability will help in maintaining the voltage level at its nominal value. However, an important issue is the voltage regulation limits, at which the voltage regulator is stable. These limits were discussed and are related to the loading at the grid. It has been shown that, the more input power coming from the DG source, the more reactive power is available to compensate for the voltage. However, in case of increased active and reactive powers, the current limit could be reached. Hence, the compensation capability is limited by the maximum current that the VSC would stand. Another limit is presented by the load that is connected at the same connection point as the DG. If the load has a low power factor, it means that more injected reactive power is needed to regulate the voltage. This in turn would increase the injected current. Another issue that could affect the voltage regulation capability is the voltage phase-angle extraction.

It has been shown that using a PLL that implements the fundamental component of the grid voltage a smaller error in the estimated phase angle would be produced and hence resulting in better grid voltage regulation. A neural-networks based PLL has (NN-PLL) been introduced for that purpose. The NN-PLL has been compared with a previously investigated PLL that extracts the angle of the positive sequence voltage, which is referred to here as PS-PLL. The NN-PLL has performed superior compared to the conventional PLL when the grid voltage harmonics are significant, and the case of grid voltage amplitude modulation.

Intentional islanding capability

Finally, the **intentional islanding capability** has been studied. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection algorithm should be applied. The islanding detection technique should be able to differentiate between grid dynamics and islanding condition, so that a correct detection signal is provided, irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch at which the detection algorithm will malfunction.

The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC).

Two islanding techniques have been examined here; namely passive and active techniques. In the passive technique, the estimated frequency signal in combination with the PCC-voltage regulator has been used to detect islanding with a minimum NDZ. That could be a beneficial application in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the active technique has shown to be beneficial. In this technique, which incorporates also the passive algorithm using the estimated frequency, a reactive current reference is set in order to change the voltage at the PCC. If the voltage changes, it will result in the detection of the island. The two islanding-detection methods have been examined for the operation of a converter-interfaced DG that is working together with both a strong grid and a weak grid. The islanding-detection technique has successfully detected the island in case of islanding condition, while it did not react during a voltage dip at the grid.

6.2 Future work

The grid interconnection capability of a converter-interfaced DG has been studied here regarding the front end converter only. The study of the whole DG system and its effect on the interface capabilities is an interesting topic and could result in setting preferable topologies for the optimal operation. For instance, the capability of voltage dips ride through has been related to the DG source input power. If this input power could be changed in a very short time, then the ride through capability could be provided without oversizing the front end converter. Moreover, providing controllable storage at the DC-link could help in storing the extra power during island operation. That could result in supporting the island for longer time duration and the stored power could be used during voltage dips to ride through the dip period.

Another interesting research point is the study of the parallel operation of converter interfaced DGs regarding the voltage regulation capability and

islanding. The parallel operation could be already motivated from the energy resource point of view. For instance the aggregated DG systems are common for wind energy applications. Using several DGs at the same connection point could increase the voltage regulation capability and provide better support in case of islanding. The design of a central controller, however, is an important issue. The controller should be designed to provide control coordination between different DG units with possibly different control aims. Sliding mode control approach could be implemented for the control of parallel converter-interfaced DGs that are operating in close proximity [72]. This control technique is based on variable structure systems (VSS), which are defined as systems where the circuit topology is intentionally changed following certain rules to improve the system behaviour in terms of speed of response, stability and robustness [12]. Hence, the operational idea of this controller could be to change the physical structure of the connected DGs to meet the physical or electrical changes on the grid.

Furthermore, since the grid outage detection algorithm plays an important role in providing a stable island by setting the DG controller into the required function, it is of great importance to develop a reliable detection algorithm. An algorithm with a negligible non-detectable zone (NDZ) implies a successful grid outage detection regardless of the loading condition of the grid or the injected power of the DG. Active islanding has been previously introduced to provide such a reliable detection. However, the equipment of active islanding can have a drawback of polluting the grid. Besides, the equipment cannot be implemented in the case of a weak grid, where the grid states are changeable even during normal operation. The use of smart sensors could present another possible and reliable way in the grid outage detection. A smart or wireless sensor is comprised of a sensor, a processor, and wireless communication all on a single chip owing to the recent advances in micro-electro-mechanical systems (MEMS) technology [73], [74]. Smart sensors could be implemented for the coordination between the controllers for islanding detection through the interaction with the protection system or the grid operator. In addition, smart sensors could be

implemented for the coordination between the controllers for parallel operating DGs.

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THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Converter-Interfaced Distributed Generation – Grid Interconnection Issues

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CHALMERS UNIVERSITY OF TECHNOLOGY
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To my family

Converter-Interfaced Distributed Generation –
Grid Interconnection Issues

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Abstract

Distributed generation (DG) with a converter interface to the grid is found in many of the green power resources applications. In this thesis, the control of a voltage source converter (VSC), as the DG front end, is in focus regarding the power quality problems that could appear at the connection point. The aims have been set to maintain a stable operation of the DG, in case of network disturbances, and to react in a corrective way during different grid operating conditions (e.g. in case of voltage dips). For this purpose, vector current controllers have been implemented with two different line filters; namely an inductance filter (L-filter) and an inductance-capacitance-inductance filter (LCL-filter). The controllers have incorporated: one sample time delay compensation, limitation of the reference voltage to avoid saturation, an integrator anti-windup, a DC-link voltage controller, a PCC voltage regulator, and an islanding detection algorithm.

The ride-through capability of the DG has been examined against a variety of possible voltage dips that could appear at the connection point. Moreover, the capability of the DG to compensate for the voltage at the connection point has been studied. Finally, the intentional islanding has been considered, where the DG is allowed to energize a part of the grid in case of the utility outage forming what is called an island.

The results found are that the effect of unbalanced voltage dips on the DC-link voltage ripple is minimized if the oscillating powers, produced during that period, are supplied by the grid side instead of the DC-side. Moreover, design equations have been derived in order to calculate the maximum currents that would flow through the VSC valves during voltage dips. These equations are to be used in designing VSC's with voltage dips ride-through capability. In addition, a neural-network based PLL, which extracts the phase angle of the fundamental component of the grid voltage, has been introduced in order to provide better performance in case of a DG with voltage compensation capability. Finally, combining the voltage regulator with the estimated frequency as a measure for islanding condition has, in this work, been found as an appropriate practice, to detect islanding, especially in the case of weak grids.

***Keywords**:* distributed generation, harmonics, intentional islanding, L-filter, LCL-filter, power quality, strong grid, vector control, voltage dips, voltage regulation, VSC, weak grid.

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At last, but not least, I would like to express my thanks to my whole family. Thanks to my father Prof. Ahmed Hassan and my mother Samia Gohar for their support and encouragement throughout my whole life. Thanks to my little two angels Mayar and Momen for filling my life with joy. And thanks Hassan for your love, patience and support.

Fainan Abdul-Magueed Hassan

Gothenburg, Sweden,

September, 2007.

Table of Contents

Chapter 1

Introduction

1.1 Motivation

The consumption of electrical energy is an ever growing need worldwide. Yet, growing in tandem to it are concerns about environmental pollution, global warming and the steady depletion of fossil fuels. Electricity generation from renewable resources might be considered as a feasible solution for the next generations [1].

Traditional power systems implement large power generation plants that produce most of the power, which then is transmitted to large consumption centres and further distributed between different customers. This power system design structure has, at some locations, started to change [2] towards new scenarios at which distributed generation (DG) units are spread throughout the distribution network, as shown in Fig. 1.1 for two possible locations. These DGs utilize renewable resources such as wind turbines, photovoltaics, biomass, small hydro-turbines … etc. Beside their environmental benefits, DGs offer a low-cost way for the energy flow into the market since they do not imply substantial transmission losses due to their location near to the customers [3]. Moreover, they could present a reliable and uninterruptible source for the customers especially in rural areas [4] and micro grids [5]. In addition, a possibility where the DG could be beneficial is if it could help to supply load during contingencies until the utility can build up additional delivery capacity [6].

More advantages are introduced using power electronics interfaced DGs [7]. For instance, converter interfaced DGs can be designed to provide ancillary services to the utility; such as reactive power support, load balancing, voltage support, and harmonic mitigation [3]. Moreover, such DGs can be more energy efficient in the sense that they can provide more

energy production, more smooth power production (less dependent on the prime source variations), and controlled energy storage [9].

In addition to the above advantages, the integration of DGs is, to a large extent, owed to political decisions in many countries. For instance, the Swedish government has introduced a legislation (2003:113), which intended to encourage and increase the proportion of electricity produced from renewable resources [8]. The objective is that the amount of electricity produced from renewable resources will provide additional power of about 6.5% of the present total production by the year 2010.

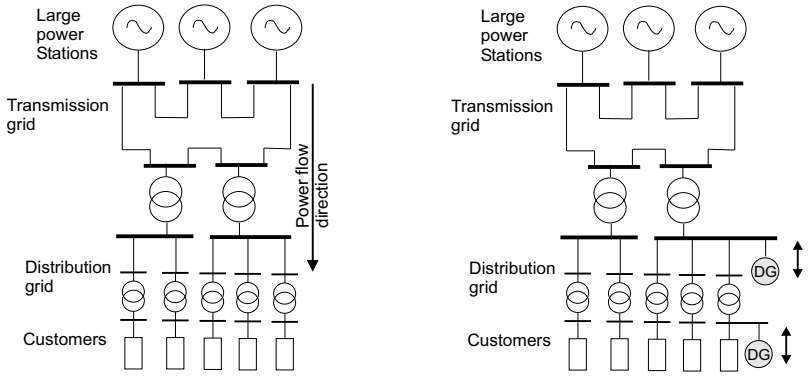

Fig. 1.1 Traditional power system (left) and penetration of distributed generation (right). The arrows present the power flow direction.

Even though large-scale implementation of DGs has several driving forces as mentioned above, there are major challenges concerning network interconnection issues that have to be solved. Grid connection of DGs is considered from two main prospects: power-system prospective and DG-technology prospective. As it is an essential part for the integration of DGs to achieve a reliable and improved performance of the power system, the DG interface to the grid is of focus in this work.

1.2 Background and related work

Background

Power conversion systems of distributed generation (DG) vary according to the nature of the input energy source. They may be implemented by using partially rated power electronics interface, as in wind turbine systems with doubly fed induction generators, or with fully rated power electronics interface [7]. The latter interface is the dominating one in applications related to fuel cells, solar cells, micro turbines and wind turbine systems [9]. There can be one or more power conversion stages in order to adjust the power of the energy source with the grid requirements, as shown in Fig. 1.2 [9]. With DC energy sources, the power electronics interface may consist of one DC/AC converter, or an intermediate DC/DC conversion stage can be added to achieve a specific goal, e.g. in order to regulate the output voltage so that the maximum available power is extracted [9]. The same is valid for AC sources, where they have to be adjusted to match the grid requirement by a DC intermediate stage. An energy storage unit could also be connected in the DC stage to adjust the energy injected into the utility grid in all operating conditions. The focus here will be on DG systems with a DC/AC power converter as a front end, where the DC-link voltage is either controllable or constant and the primary source input power is constant. The power converter to the grid enables a fast control over active and reactive power and could perform voltage and frequency control [10], [11]. Observe that, in order to control the active power, the primary source needs also to be controllable or an energy storage should be provided.

Voltage source converters (VSCs) using insulated gate bipolar transistor (IGBT) switches that are controlled by pulse width modulation (PWM) are used on the grid side at medium/high voltage due to their high controllability and low losses [12], [13], [14]. The good controllability promotes the use of the VSCs in grid connected applications to provide good power quality. An inherent part of a VSC is a filter inductor (L-filter), which is used to minimize the current harmonics injected into the grid [15] - [20].

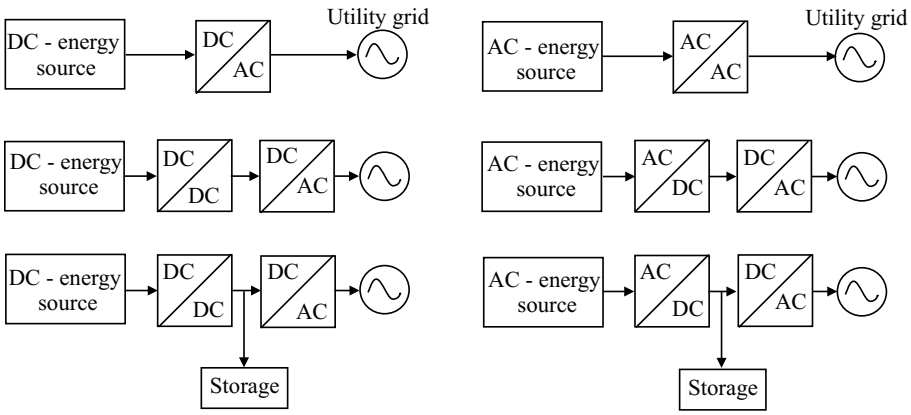

Fig. 1.2 Full-rated power electronics interfaced DG systems.

Like most of the power electronics equipment, an important drawback of using VSCs is their sensitivity to voltage disturbances, e.g. voltage dips [21]. In order to keep the DC-link voltage constant and minimize the grid current amplitude and harmonics during faults, the VSC controller is required to have two main functions: DC-link voltage regulation and current control. Most conventional current controllers have been designed under the assumption of balanced grid voltages [16]. These controllers show undesirable current control characteristics under unbalanced conditions because the current references are distorted by a second-order harmonic [16]. This is due to the negative-sequence voltage in the three-phase domain, which translates into a sinusoidal signal having a frequency of twice the grid frequency in a *dq*-frame synchronized with the positive-sequence voltage.

Related work

A comparison between different types of current controllers (CCs) for shunt-connected VSC based on their transient operation in case of voltage dips is presented in [17]. It has been shown that the dual vector current controller (DVCC) shows the best performance regarding grid current control and DC-link voltage regulation [16], [17]. This controller uses two different vector current controllers for the two sequence components,

together with a DC-link voltage controller based on the instantaneous active and reactive power theory.

Due to the PWM switching of voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [22]-[27]. Inserting an LCL-filter between the grid and the VSC eliminates high frequency harmonics even with lower switching frequency. Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. Damping methods are extensively addressed in literature. In [23] a resistance is used in series with the filter capacitor to passively damp the resonance. This resistance increases the system losses and decreases the efficiency of the filter. Instead, methods to actively damp the resonance are adopted as in [24], [25], [28]. In [25], a comparison between none-damped, passively-damped and actively-damped systems is carried out using Bode plots. It has been concluded that the active damping reduces the resonant peak as effectively as the passive damping. In [24], three cascaded controllers are used with the reference grid current generated from a DC voltage controller. The converter current and capacitor voltage are predicted. Moreover, two active resistances virtually connected in series with the filter inductor resistances are considered in the controller dead-beat gains. However, the use of these resistances is not justified. In [22], and [26] controllers with no damping are proposed. This has been proposed in [22] by controlling the grid current instead of the converter current and the proper choice of the filter parameters. However, by introducing a one sample time delay the system has been unstable acquiring the passive damping. In [26], two control loops are used: an outer current control loop and an inner capacitor voltage control loop. The latter is used to stabilize the controller and in the same time damp the resonance. The effect of adding a time delay has not been considered there as well.

The voltage compensation capability of VSCs' controllers has been also discussed in the literature to overcome the problem of having a decreased voltage at the connection point of the DG due to load/system dynamics [30]-[35], or to mitigate power quality problems [37], [38]. However, the effect of

the grid power quality on the phase locked loop (PLL), which is used to extract the grid phase angle, and on the compensation capability has not been treated in the literature. Moreover, in most of the literature the VSC is assumed to be either not injecting active power or has a controllable active power, which provides a wider compensation range.

One of the important capabilities of the DGs is to locally detect a grid outage condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, to prevent island operation. This capability has been discussed in the literature [39]- [45], where the transfer from grid-connected to island operation has been studied assuming a strong grid. The transfer from island to grid-connected mode is not much discussed. In [46], the load has been connected to the capacitor of the LCL-filter, at which its voltage is controlled in all the operating modes, to attain perfect transition without any transients. In [10], the DG was set into idle mode in case of grid recovery until the synchronization is achieved between the grid voltage and the DG voltage.

1.3 Purpose of the thesis and contributions

The main goals of the thesis and the contributions related to them are:

Goal 1: To determine the interface requirements and the capabilities of DGs with a voltage source converter (VSC) as a front end. For this purpose, two line filters are to be considered at the connection point of the DG; namely inductance line filter (L-filter) and inductance-capacitance-inductance line filter (LCL-filter). Vector current controllers are to be implemented for both systems.

Contribution 1: The derivation of the current reference generation equations, for the LCL-filter system, regarding the oscillating powers that are produced during the unbalanced grid voltage and compensating for them in two different ways. This has been presented in Section 2.5 and Paper A and Paper B.

Goal 2: To study the effect of voltage dips on the converter-interfaced DG and the requirements for ride-through capability.

Contribution 2: The study of all possible types of voltage dips that could appear at the terminals of a DG unit with both L-filter and LCL-filter systems. And, the derivation of the equations of maximum currents that would flow through the DG's converter switches. The main results of this point has been published in Paper B and explained in Section 3.5.

Goal 3: To study the effect of the other power quality problems on the DG operation, and how the DG controller could react in a corrective way to support the grid and provide better power quality at the connection point.

Contribution 3: A synthesis of a neural network based PLL has been proposed to reduce the error due to the voltage distortion, which has resulted in better compensation capability for the DG. This is shown in Paper E and in Section 4.5.

Goal 4: To study the possibility of intentional islanding for very weak grids.

Contribution 4: A passive detection algorithm that combines both the estimated frequency and the voltage regulator has been proposed to detect the islanding condition, especially in a weak grid. This has been shown in Section 5.4 and in Paper F and G, for various loads.

1.4 Thesis outline

The fundamental theory of the work is explained in details in **Chapter 2**. In that chapter the vector current controllers (VCC) for both the L-filter and the LCL-filter VSC-interfaced DG-systems are presented. The dual vector current controller (DVCC) has been implemented, for both systems, in order to achieve better current reference tracking in case of grid-voltage imbalance. Moreover, current reference equations are derived in such a way that they alleviate the DC-link ripples.

In **Chapter 3**, the voltage dips that could appear at the DG terminals are considered. An investigation of the ride-through capability is provided regarding the possible maximum currents that would flow through the VSC switches, and also regarding the DC-link voltage ripples. In addition, the maximum currents that would result during the dip period were obtained

using design equations that have been derived for various dips. Moreover, the DG system, both with the L-filter and the LCL-filter, has been examined for all possible voltage dips that could occur at its terminals. Recommendations of oversizing of the DG have been drawn as a consequence of that study.

If oversizing is not a possibility, the voltage regulation capability might appear as another possibility to correct the terminal voltage instead of riding through the voltage dip period. This is then discussed in **Chapter 4**. This capability might also be beneficial in case of operation in weak grids, where the voltage level is not constant and is dependent on the loads. Moreover, by compensating the grid voltage most of the power quality problems are mitigated. In this chapter, the voltage regulation capability is related to the performance of the phase locked loop (PLL) that estimates the phase angle of the grid voltage. A PLL that extracts the fundamental component of the grid voltage has been implemented using neural network technique.

In **Chapter 5**, the outage (and recovery) of the grid voltage has been considered, regarding the ability to keep the DG into operation to supply sensitive or critical loads. The main conclusions relating the different chapters and the possible future work considering the same topic are reported in **Chapter 6**.

1.5 Publications

The work in this thesis has resulted in eight publications, as shown in Fig. 1.3. The papers, designated in the figure from A to G, are supplemented at the end of this thesis with the same designation. The publications are also listed below with short description.

Journal papers

[J-1] F. Magueed, A. Sannino, and J. Svensson, "Design of Robust Converter Interface for Wind Power Applications," in *Wind Energy Journal, special issue on Electrical Integration of Wind Power*, vol. 8, no. 3, 2005, pp. 319 – 332.

In this paper the study of all possible voltage dips that could occur at the terminal of the DG is studied. This paper is designated as "Paper A" and supplemented at the final part of the thesis.

[J-2] F. Magueed, and T. Thiringer, "Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC," *submitted to Electrical Power Quality and Utilization Journal*.
The neural network based PLL has been presented here and compared with the positive sequence based PLL. This paper is designated as "Paper E" and supplemented at the final part of the thesis.

[J-3] F. Magueed, G. Olsson, and T. Thiringer, "Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation," *submitted to IEEE trans. on Power Delivery*.
An active islanding detection method is proposed, which consists of an under/over frequency passive detection algorithm, a PCC-voltage regulator and a DG reactive current limiter. This paper is designated as "Paper G" and supplemented at the final part of the thesis.

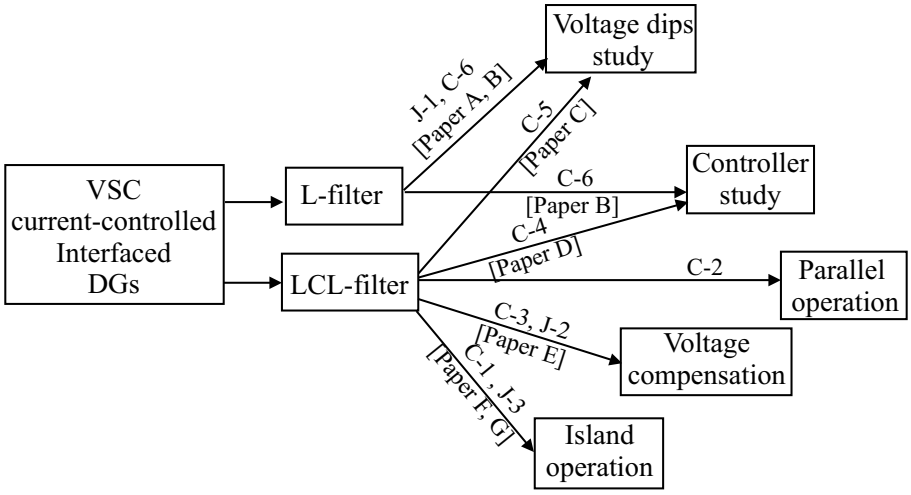

Fig. 1.3 Thesis outline with the resulting publication.

Conference papers (peer reviewed)

[C-1] F. Magueed, and J. Daalder, "Operation of Distributed Generation in Weak Grids with Local Critical Load," at *IEEE Annual Industrial*

Electronics Conference (IECON'06), Paris, France, November 7-10, 2006.

The passive islanding detection algorithm has been presented here with the focus on the operation in weak grids. This paper is designated as "Paper F" and supplemented at the final part of the thesis.

[C-2] F. Magueed, and J. Daalder, "Parallel Operation of Distributed Generation in Weak Distribution Systems," at the *12th International Power Electronics and Motion Control Conference (EPE-PEMC'06)*, Slovenia, August 30 - September 1, 2006, pp. 531 – 536.

A discussion of the voltage compensation limits and the possible parallel operation of DGs to provide better compensation capability is introduced.

[C-3] F. Magueed, and H. Awad, "Voltage Compensation in Weak Grids Using Distributed Generation with Voltage Source Converter as a Front End," at the *6th International Conference on Power Electronics and Drive Systems (PEDS'05)*, Kuala Lumpur, Malaysia, Nov 28 - Dec 1, 2005, pp. 234 – 239.

The main voltage regulator is presented here, with the capability to compensate for voltage dips at the grid.

[C-4] F. Magueed, and J. Svensson, "Control of VSC Connected to the Grid through LCL-Filter to Achieve Balanced Currents," at the *IEEE Industry Applications Society 40th Annual Meeting (IAS'05)*, Kowloon, Hong Kong, October 2-6, 2005.

The control of the VSC is presented here, in case of unbalanced voltage dips at the grid, to provide balanced DG currents. This paper is designated as "Paper D" and supplemented at the final part of the thesis.

[C-5] F. Magueed, J. Svensson, and A. Sannino, "Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage conditions," in *Proc of Power Tech Conference (PT'05)*, St. Petersburg, Russia, June 27-30, 2005.[1]

The performance of the LCL-filter system has been discussed regarding the voltage dips at the grid. This paper is designated as "Paper C" and supplemented at the final part of the thesis.

[1] This paper has been awarded ***High quality paper certificate*** for the presentation from 2005 IEEE Power Tech conference (June 27-30 2005).

[C-6] F. Magueed, A. Sannino, and J. Svensson, "Transient Performance of Voltage Source Converter under Unbalanced Voltage Dips," in *Proc. of Power Electronics Specialists Conference (PESC'04)*, Aachen, Germany, June 20-25 2004, pp. 1163 – 1168.

The study of voltage dips with phase angle jumps and the compensation of the oscillating powers using two different ways have been presented in this paper. This paper is designated as "Paper B" and supplemented at the final part of the thesis.

Chapter 2

Power Electronics Interfaced Distributed Generation – Controller Description

In this chapter, a general description of the power conversion systems, i.e. power electronics interface, for distributed generation is given. Two distributed generation systems are considered with two different line filters; namely an inductance line filter and an inductance-capacitance-inductance line filter, and a voltage source converter as a front end for the energy source. Vector current controllers are proposed for the two systems. The description of the controllers is given in details. Moreover, the generation algorithm for the current references is provided.

2.1 Current-controlled voltage source converters

Current controllers are preferred for shunt connected voltage source converters (VSCs) in order to increase stability of the closed loop and to decrease the time response in case of load transients [19]. Accordingly, a vector current controller (VCC) is considered throughout this work in order to obtain a high performance controller. In a VCC, the active and reactive currents (consequently powers) can be controlled independently. And, as indicated above, a high bandwidth controller with low cross-coupling effect between active and reactive currents can be achieved [20].

In Fig. 2.1, a scheme of the VSC system connected to the grid via a line filter along with the VCC is shown. Since the application of the distributed generation utilizing renewable resources is considered, the variation of the input current i_{in} is relatively slow compared to the response time of the controller. Hence, i_{in} is modelled as a constant current source. In addition,

the DC-link voltage should be regulated to maintain a constant voltage in case of grid voltage variations (e.g. voltage dips). The DC voltage regulator is implemented as a proportional-integral (PI) controller, where the measured DC capacitor voltage u_{dc} is compared with its reference value u_{dc}^{*} and the error signal is used to produce a reference DC current i_{dc}^{*} according to

$$i_{\mathrm{dc}}^{*} = \Delta u_{dc} k_{\mathrm{pdc}} \left(1 + \frac{1}{s T_{\mathrm{idc}}} \right) \tag{2-1}$$

where

k_{pdc}, T_{idc} are the proportional gain and integral time of the PI-controller respectively with their values as given in Appendix D;

s is the Laplace operator; and

$\Delta u_{\mathrm{dc}} = u_{\mathrm{dc}} - u_{\mathrm{dc}}^{*}$.

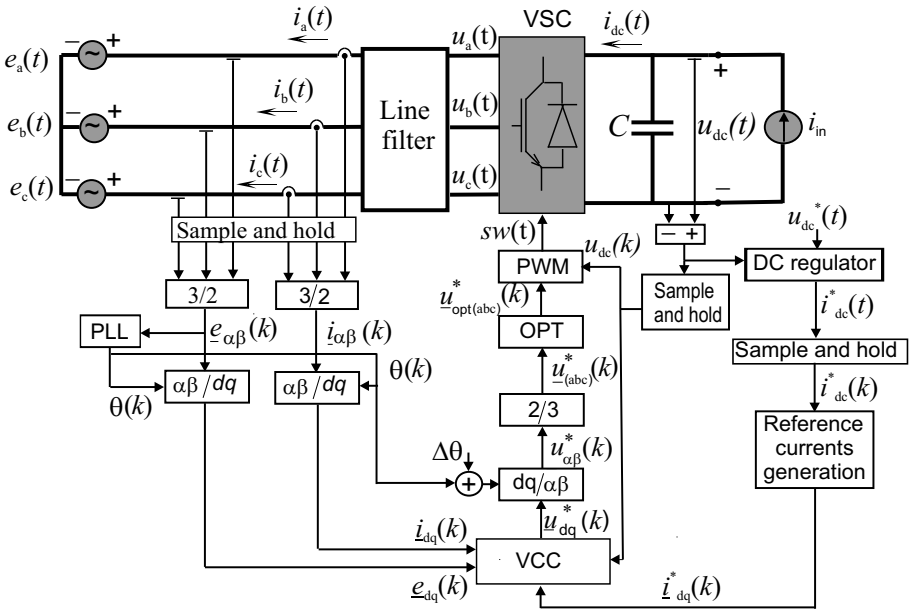

Fig. 2.1 Schematic diagram showing VSC, grid, filter and controller.

The signal flow from the power circuit to the VCC is as follows. The three-phase AC currents and voltages are first sampled and transformed into

the $\alpha\beta$-stationary frame[2]. The resulting rotating vectors $\underline{e}_{\alpha\beta}$ and $\underline{i}_{\alpha\beta}$ are then transformed into the rotating *dq*-frame that is synchronized with the grid voltage using a phase-locked-loop (PLL) that extracts the grid voltage angle θ. The *dq*-vectors of the measured voltages and currents, $\underline{e}_{\mathrm{dq}}$ and $\underline{i}_{\mathrm{dq}}$ respectively, are then used along with the reference current vector $\underline{i}^{*}_{\mathrm{dq}}$ by the VCC to produce the reference voltage vector $\underline{u}^{*}_{\mathrm{dq}}$. The different coordinate transformations are provided in Appendix A, where the *d*-component refers to the real value while the *q*-component refers to the imaginary value of a vector.

The reference currents are produced in such a way as to decrease the DC-link voltage ripple using a "reference currents generation" algorithm that uses the signal coming from the DC-link voltage regulator, and is explained later in this chapter. The reference voltage vector is then transformed to a vector in the $\alpha\beta$-frame using a transformation angle of $\theta+\Delta\theta$, where $\Delta\theta$ compensates for the transformation angle error due to one sample calculation time delay of the controller. The vector $\underline{u}^{*}_{\alpha\beta}$ is then transformed into three-phase control signals. Those signals are then used in the PWM modulator to produce the switching pattern for the VSC. The PWM is optimized to increase the maximum output voltage of the converter without increasing the DC-link voltage [12], [14]. The block "OPT" injects a zero sequence voltage into the control signals. Due to the absence of a neutral wire, the added zero sequence waveforms are cancelled out.

It should be mentioned that the design of the VCC is different for the power circuit with an inductance line filter from the power circuit with inductance-capacitance-inductance line filter, since both circuits have different time and frequency behaviors. Also the generation of reference currents is different for the two filter configurations. This is shown in the next sections.

[2] The coordinate transformation matrices are explained in Appendix A.

2.2 Vector Current Controller with inductance line filter

An inductance line filter is first considered. The plant in Fig. 2.2 represents the filter, the PWM, and the VSC. The last two, however, are assumed to be ideal, having a transfer function of 1. The plant transfer function in the *s*-domain is then represented as

$$G_{\mathrm{pl}}(s) = \frac{1}{sL_{\mathrm{f}} + R_{\mathrm{f}}} \tag{2-2}$$

where

L_{f} is the filter inductance; and

R_{f} is the filter resistance.

The controller design is based on deadbeat control. The measured voltage and current vectors are used to calculate the feedforward vector $\underline{FF}_{\mathrm{dq}}$ as

$$\underline{FF}_{\mathrm{dq}}(k) = \underline{e}_{\mathrm{dq}}(k) + \underline{i}_{\mathrm{dq}}(k)(R_{\mathrm{f}} + \mathrm{j}\omega L_{\mathrm{f}}) \tag{2-3}$$

where

ω is the angular frequency of the grid voltage;

k is the sampling instant; and

j is the imaginary unit.

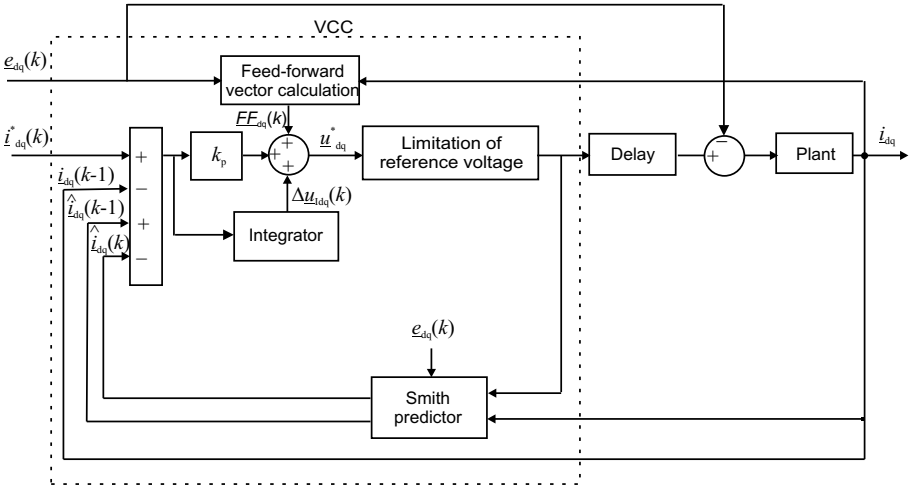

Fig. 2.2 Deadbeat based vector current controller (VCC) for DG with L-filter.

The change in the current reference is met by a change in the voltage reference that is produced by adding $\underline{FF}_{\mathrm{dq}}$ to the output of a PI-controller with a proportional gain k_p, also called here dead-beat gain. The dead-beat strategy has been described in [20]. The Dead-beat gain is given in terms of the filter parameters as

$$k_{\mathrm{p}} = \frac{L_{\mathrm{f}}}{T_{\mathrm{s}}} + \frac{R_{\mathrm{f}}}{2}. \tag{2-4}$$

An integral part $\Delta\underline{u}_{\mathrm{idq}}$ is needed to remove the static errors caused by non-linearity, noisy measurements and non-ideal components. The generated reference voltage is then calculated as

$$\underline{u}^{*}_{\mathrm{dq}}(k+1) = \underline{FF}_{\mathrm{dq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idq}}(k). \tag{2-5}$$

The integral part is implemented as

$$\Delta\underline{u}_{\mathrm{idq}}(k+1) = \Delta\underline{u}_{\mathrm{idq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{i}} \tag{2-6}$$

where k_{i} is the integration constant, which can be written as

$$k_{\mathrm{i}} = \frac{k_{\mathrm{p}}T_{\mathrm{s}}}{T_{\mathrm{i}}} \tag{2-7}$$

where T_{i} is the integral time constant, which is chosen to be equal to the L-filter time constant $T_{\mathrm{i}} = \frac{L_{\mathrm{f}}}{R_{\mathrm{f}}}$, and T_{s} is the sampling time.

The current error vector $\underline{\varepsilon}_{\mathrm{idq}}$ is described by

$$\underline{\varepsilon}_{\mathrm{idq}}(k) = \underline{i}^{*}_{\mathrm{dq}}(k) - \underline{i}_{\mathrm{dq}}(k-1) + \hat{\underline{i}}_{\mathrm{dq}}(k-1) - \hat{\underline{i}}_{\mathrm{dq}}(k) \tag{2-8}$$

which accounts for a one sample time delay in the measured current signal due to the calculation time of the digital controller. This delay has been compensated for using the estimated current $\hat{i}_{\mathrm{dq}}$ at two successive instants,

which is calculated by a Smith predictor [48], [76]. The Smith predictor is implemented in a way analogous to a state observer[3], as proposed by [20], which means running a model of the plant in parallel to the plant itself. In steady state, the estimated and actual currents should be equal, hence $\underline{i}_{\mathrm{dq}}(k-1)=\hat{\underline{i}}_{\mathrm{dq}}(k-1)$ in (2-8), which cancels the time delay effect.

The output reference voltage command is also limited to be inside the control region, which is described by a hexagon composed of six equilateral triangles with a side length of $\sqrt{2/3}u_{\mathrm{dc}}$. In this work the minimum amplitude error (MAE) limiting method has been adopted [20]. In this method a new reference voltage vector on the hexagon boundary that is closest to the original reference vector is chosen as explained by Fig. 2.3. This is done by mapping the voltage reference into new coordinates *xy*. The *xy*-coordinate position depends on the number of the sector in the hexagon that contains the voltage reference. The reference voltage vector in the new coordinates u_{xy}^{*} is obtained as

$$\underline{u}_{\mathrm{xy}}^{*}=\underline{u}_{\alpha\beta}^{*}e^{-\mathrm{j}\theta_{\mathrm{xy}}} \tag{2-9}$$

where θ_{xy} is the angle between the α-axis and the *x*-axis and is calculated as

$$\theta_{\mathrm{xy}}=\left(1+2(n-1)\right)\pi/6 \tag{2-10}$$

where *n* is the sector number at which the reference vector lies in the hexagon.

The components of the limited reference voltage vector are calculated from Fig. 2.3 as

$$u_{\mathrm{x}}=\frac{u_{\mathrm{dc}}}{\sqrt{2}} \tag{2-11}$$

[3] The use of the Smith predictor is described in more details in Paper D.

$$u_{\mathrm{y}} = \begin{cases} u_{\mathrm{y}}^{*} & \left|u_{\mathrm{y}}^{*}\right| \le \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \\ sign(u_{\mathrm{y}}^{*}) \cdot \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} & \left|u_{\mathrm{y}}^{*}\right| > \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \end{cases} . \tag{2-12}$$

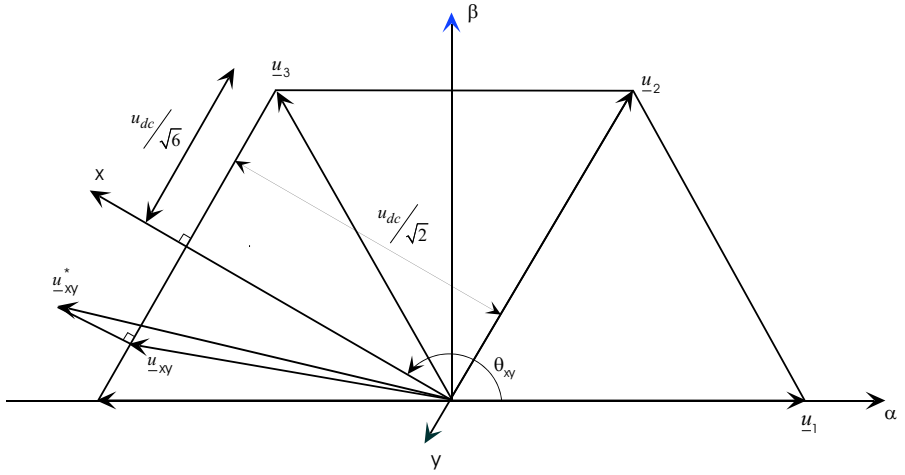

Fig. 2.3 Principle of the minimum amplitude error method.

It is worth noting here that using the limited voltage reference as an input for the Smith predictor, as shown in Fig. 2.2, is important in providing an anti-windup property for the controller, which is useful in case of increased current steps.

The time domain performance of the controller is tested in Fig. 2.4, for the case of a substantial positive active current step, which is considered the worst operational case since it leads the voltage to the saturation area. Due to the high current step of 1.5 p.u. that has been applied at 0.2 s, the controller will go into the voltage reference limitation algorithm, at which the reference voltage will be limited as shown by the same figure. Since the demanded reference voltage, required to achieve the current step, has not been reached, the dead-beat is not accomplished. Hence, it will take several samples for the current to reach its reference value. As shown by the figure, the current will accomplish the step in 2 ms. The figure also shows the cross-coupling effect

on the *q*-component of the current. To eliminate this coupling effect, i_{q}^{*} might be modified to counteract the effect of the active current step [20]. However, this will not be considered here since the reference *q*-component current will be implemented later to compensate for various power quality problems at the grid.

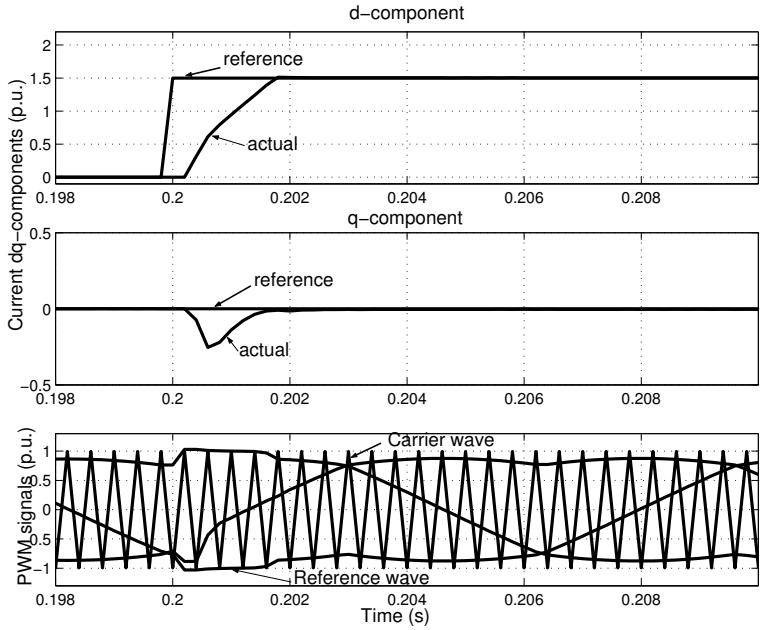

Fig. 2.4 Active current (upper), reactive current (middle), and PWM signals (lower), due to a step in i_{d}^{*} from 0 to 1.5 p.u.

2.3 Dual vector current controller (DVCC)

In case of an unbalanced grid voltage, the voltage vector in the *dq*-frame has oscillations at a frequency of twice the fundamental frequency due to the negative sequence that exists in the grid voltage. That will lead to oscillations in the injected currents to the grid. To deal with that situation a dual vector current controller (DVCC) [18] can be used. The DVCC consists

of two separate VCCs, one for controlling the positive-sequence voltage and the other for controlling the negative-sequence voltage. This controller synthesis has proved to give the best performance regarding grid current control and DC-link voltage regulation [17]. A simplified scheme for the DVCC is shown in Fig. 2.5.

The positive sequence PI-controller is described in the positive *dq*-frame (*dqp*-frame), which rotates in the positive direction, as

$$\underline{u}^{*}_{\mathrm{dqp}}(k+1) = \underline{FF}_{\mathrm{dqp}}(k) + \underline{\varepsilon}_{\mathrm{idqp}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqp}}(k) \qquad (2\text{-}13)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqp}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqp}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqp}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The negative sequence PI-controller is described in the negative *dq*-frame (*dqn*-frame), which rotates in the negative direction, as

$$\underline{u}^{*}_{\mathrm{dqn}}(k+1) = \underline{FF}_{\mathrm{dqn}}(k) + \underline{\varepsilon}_{\mathrm{idqn}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqn}}(k) \qquad (2\text{-}14)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqn}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqn}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqn}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The decomposition of the supply voltage into positive and negative sequence components is performed using the delayed signal cancellation (DSC) algorithm, which has been first proposed in [77]. This algorithm is implemented in the *dq*-frame, which rotates in the positive direction, in the same way as suggested in [17]. In this frame, the positive sequence is a constant vector (constant amplitude and fixed direction), while the negative sequence is a rotating vector, which rotates with twice the line frequency in the opposite direction, as compared with the positive sequence.

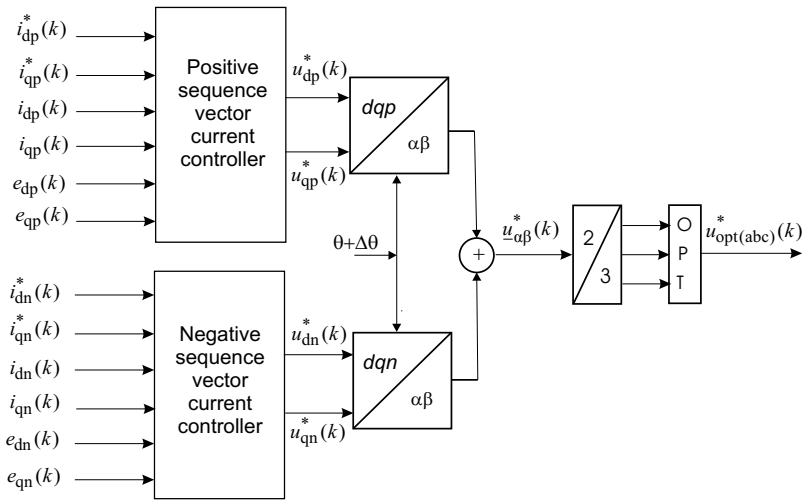

Fig. 2.5 Simplified block diagram of dual vector current controller (DVCC).

In the DSC the measured supply voltage, in the *dq*-frame, and the same signal, delayed by one-quarter of a fundamental frequency period, are considered. Delaying the signal gives a vector composed by the same positive sequence component and a negative sequence component which has equal amplitude but opposite sign. Therefore, if the signal delayed by one-fourth of period is added to the measured supply voltage, the negative sequence voltage will be removed.

The positive sequence voltage vector can thus be extracted from the measured values as

$$\underline{e}_{\mathrm{dqp}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) + \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-15}$$

where T is the period at the fundamental frequency.

The negative sequence can be obtained in the positive rotating plane, as follows

$$\underline{e}_{\mathrm{dqn}_{(\mathrm{p})}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) - \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-16}$$

which is then transformed into the negative rotating plane by transforming it into the $\alpha\beta$-frame and back into the *dqn*-frame using the opposite angle.

The time domain response of the DVCC is compared with the time domain response of the VCC when a grid voltage of 40% imbalance ratio is applied. Moreover, a step in the active current reference is applied at 0.25 s. The injected current is oscillating in the case of using the VCC, as shown in Fig. 2.6, while better tracking is achieved using the DVCC.

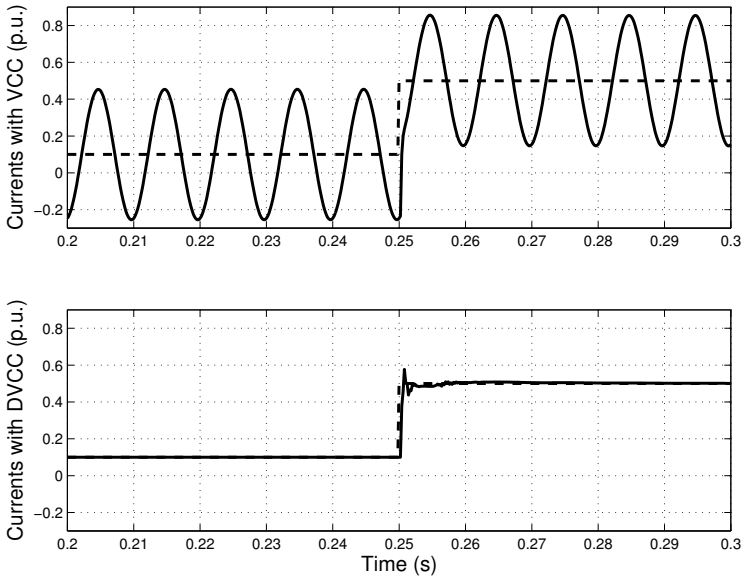

Fig. 2.6 Active grid current i_d (solid) and reference current i^*_d (dashed); with VCC (upper) and DVCC (lower).

2.4 Current reference generation with inductance line filter

In the case of a controllable DC-link voltage, proper current references should be generated in order to improve the performance of the VCC. Two performance measures are considered, which are the minimization of the DC-link voltage ripple and the decrease of the AC currents amplitudes and/or harmonics. The reference currents generation algorithm is based on

the instantaneous power theory [80]. The active power on the AC side of the converter, p_1, is considered equal to the active power on the DC side, P_{dc}, neglecting the switching losses. The power balance equation can be expressed as

$$\begin{bmatrix} p_1 \\ q_1 \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \Delta p \\ \Delta q \end{bmatrix} \tag{2-17}$$

where p_1 and q_1 are the instantaneous active and reactive powers at the AC-side of the converter respectively. The terms Δp and Δq are active and reactive powers dissipated by the filter respectively, and can be calculated instantaneously as

$$\Delta p = R_f \left(i_d^2 + i_q^2 \right) \tag{2-18}$$

$$\Delta q = \omega L_f \left(i_d^2 + i_q^2 \right). \tag{2-19}$$

The instantaneous active power p_2 and reactive power q_2 at the grid are calculated as:

$$\begin{aligned} p_2 &= e_d i_d + e_q i_q \\ q_2 &= -e_d i_q + e_q i_d \end{aligned}. \tag{2-20}$$

To achieve unity power factor, the reactive power at the grid side $q_2 = q_1 - \Delta q$ is nullified. The current references are then calculated using (2-17) as follows

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \end{bmatrix}. \tag{2-21}$$

2.5 Current reference generation for inductance line filter and unbalanced grid voltage

For the DVCC, current reference signals should be provided in the positive and the negative *dq*-coordinates. The derivation[4] is carried out in the same way as for the VCC. The current references are calculated using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ q_{\mathrm{ac},2} \\ p_{\mathrm{s}2,1} - \Delta p_{\mathrm{s}2} \\ p_{\mathrm{c}2,1} - \Delta p_{\mathrm{c}2} \end{bmatrix} \tag{2-22}$$

where the instantaneous active power p_2 and reactive power q_2 at the grid are

$$\begin{aligned} p_2(t) &= p_{\mathrm{ac},2} + p_{\mathrm{c}2,2}\cos(2\omega t) + p_{\mathrm{s}2,2}\sin(2\omega t) \\ q_2(t) &= q_{\mathrm{ac},2} + q_{\mathrm{c}2,2}\cos(2\omega t) + q_{\mathrm{s}2,2}\sin(2\omega t) \end{aligned} \tag{2-23}$$

with the following subscripts notations

ac - stands for the power at the fundamental frequency;

2 - stands for the grid side.

1 - stands for the AC converter side;

c2 - stands for the cosine component of a power that is oscillating with double the fundamental frequency; and

s2 - stands for the sine component of a power that is oscillating with double the fundamental frequency.

The power loss through the filter is encountered for in (2-22) by the terms Δp, $\Delta p_{\mathrm{s}2}$, and $\Delta p_{\mathrm{c}2}$.

Equation (2-22) has been considered in two ways, which are referred to as case 1 and case 2. The injected reactive power $q_{\mathrm{ac},2}$ to the grid is assumed to be zero in both cases.

[4] Details are given in Paper A and Paper B.

Case 1- The oscillating powers flow from the VSC side to the filter

Assuming that the converter supplies the oscillating power to the filter, and neglecting the converter losses which means $p_{ac,1}$ is equal to P_{dc}, the following equations will describe the different powers

$$P_{c2,1} = \Delta P_{c2},\ P_{c2,2} = 0 \tag{2-24}$$

$$P_{s2,1} = \Delta P_{s2},\ P_{s2,2} = 0 \quad . \tag{2-25}$$

Substituting in (2-22), the reference currents are calculated as

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qn} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{2-26}$$

Using (2-26), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.7.

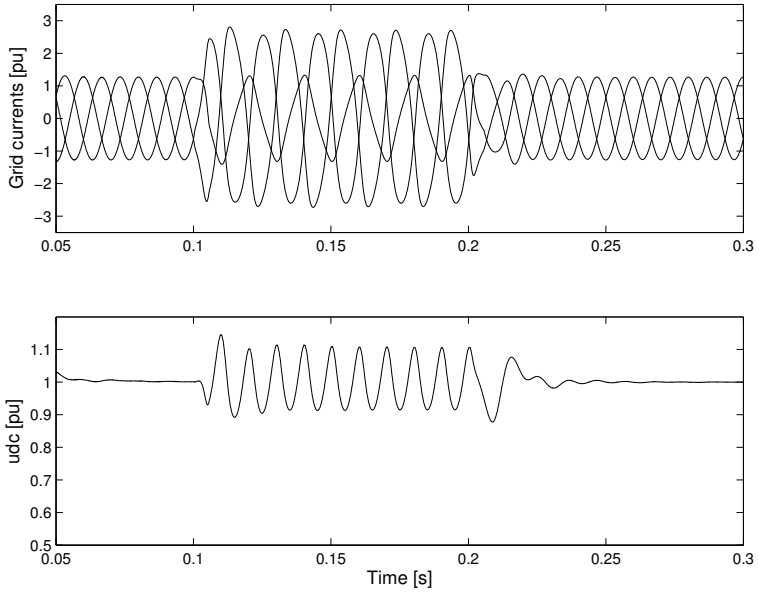

Fig. 2.7 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

Case 2- The oscillating powers flow from the grid side to the filter

In this case the grid is forced to supply the oscillating powers to the filter, by using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ 0 \\ -\Delta p_{\mathrm{s2}} \\ -\Delta p_{\mathrm{c2}} \end{bmatrix}. \qquad (2\text{-}27)$$

Using (2-27), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.8.

Comparing Fig. 2.7 and Fig. 2.8, it is concluded that it is preferred to use the current reference generation in (2-27) over (2-26) since the DC-link voltage ripples are reduced during the fault period.

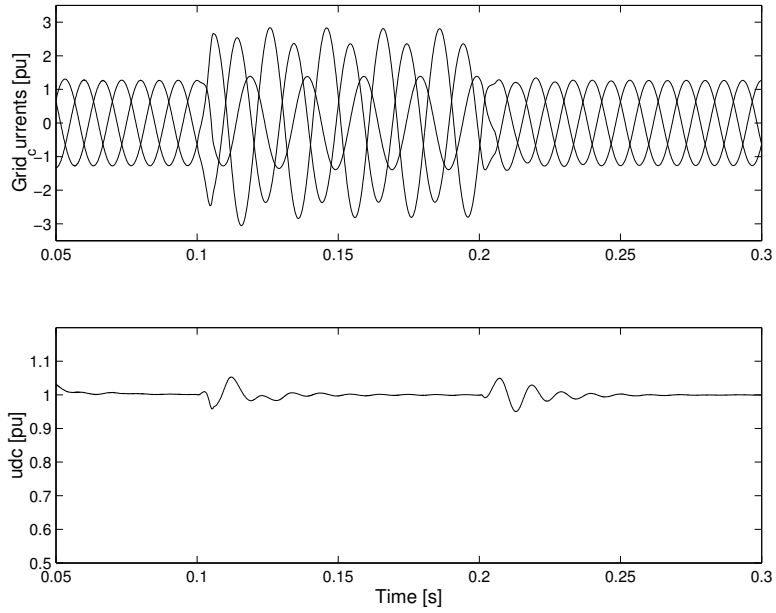

Fig. 2.8 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

2.6 Vector Current Controller with inductance-capacitance-inductance line filter

Due to the PWM switching of the voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [29]. Inserting an LCL-filter[5] between the grid and the VSC, as shown in Fig. 2.9, eliminates high frequency harmonics even with lower switching frequency.

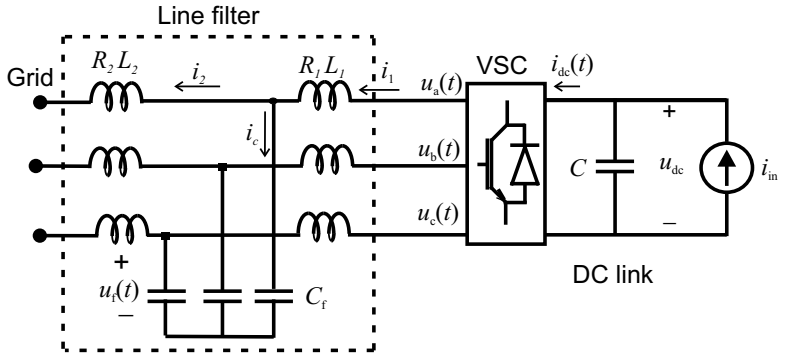

Fig. 2.9 Power circuit of DG system with VSC as a front end and an LCL-filter.

Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. In this work, a cascade control structure ([47], [48], and [49]) has been implemented to increase the stability margin and at the same time to damp oscillations at the resonant frequency of the LCL-filter. As shown in Fig. 2.10, the plant is described by three cascaded transfer functions; G_{p1}, G_{p2}, and G_{p3}, as

[5] The design of the LCL-filter parameters that are adopted here is given in Appendix B.

$$G_{\mathrm{p1}}(s)=\frac{I_2(s)}{U_{\mathrm{f}}(s)-E(s)}=\frac{1}{sL_2+R_2}$$
$$G_{\mathrm{p2}}(s)=\frac{U_{\mathrm{f}}(s)}{I_1(s)-I_2(s)}=\frac{1}{sC_{\mathrm{f}}} \tag{2-28}$$
$$G_{\mathrm{p3}}(s)=\frac{I_1(s)}{U(s)-U_{\mathrm{f}}(s)}=\frac{1}{sL_1+R_1}$$

where

$I_2(s)$ is the Laplace function of the grid side current $i_2(t)$;

$U_{\mathrm{f}}(s)$ is the Laplace function of the filter capacitor voltage $u_{\mathrm{f}}(t)$;

$E(s)$ is the Laplace function of the grid voltage $e(t)$;

$I_1(s)$ is the Laplace function of the converter side current $i_1(t)$; and

$U(s)$ is the Laplace function of the converter output voltage $u(t)$.

The inner controller G_{c3} is used for stabilization of G_{p3} and is designed using dead-beat control strategy. The two outer controllers G_{c2} and G_{c1} are used to stabilize G_{p2} and G_{p1} respectively. G_{c2} is implemented as a P-controller, while G_{c1} is implemented as a PI-controller where the integral part is added to eliminate the steady state error. With the resulting controller, shown in Fig. 2.10, the two controllers G_{c1} and G_{c2} are acting like one PI-controller. The outer controller G_{c1} is a two-degree of freedom controller, since it is using the output signal of a Smith predictor (with a compensation gain k_{ps}) to cancel the time delay effect. The time-delay free plant transfer-function G_{pm} represents the LCL-filter model in steady state, where the capacitor effect is neglected.

The three controllers are described in the rotating dq-frame as follows

$$\underline{y}_{\mathrm{1dq}}(k)=k_{\mathrm{p1}}\left(\underline{\varepsilon}_{\mathrm{idq}}(k)+\frac{T_{\mathrm{s}}}{T_{\mathrm{i}}}\sum_{n=0}^{k}\underline{\varepsilon}_{\mathrm{idq}}(n)\right) \tag{2-29}$$

$$\underline{y}_{\mathrm{2dq}}(k)=k_{\mathrm{p2}}\,\underline{y}_{\mathrm{1dq}}(k) \tag{2-30}$$

$$\underline{u}^{*}_{\mathrm{dq}}(k+1)=\underline{u}_{\mathrm{fdq}}(k)+(R_1+\mathrm{j}\omega L_1)\underline{i}_{\mathrm{1dq}}(k)+k_{\mathrm{p3}}\,\underline{y}_{\mathrm{2dq}}(k) \tag{2-31}$$

where

$\underline{y}_{1dq}$ is the output vector of G_{c1}, which represents the change in the capacitor voltage $\underline{u}_{fdq}$;

k_{p1} is the proportional gain of G_{c1};

T_i is the integral time of G_{c1};

$\underline{y}_{2dq}$ is the output vector of G_{c2}, which represents the required change in the converter side current $\underline{i}_{1dq}$;

k_{p2} is the proportional gain of G_{c2}; and

k_{p3} is the proportional gain of G_{c3}.

The current error vector $\underline{\varepsilon}_{idq}$ is the input to the outer controller G_{c1}, and is described in the same way as in (2-8).

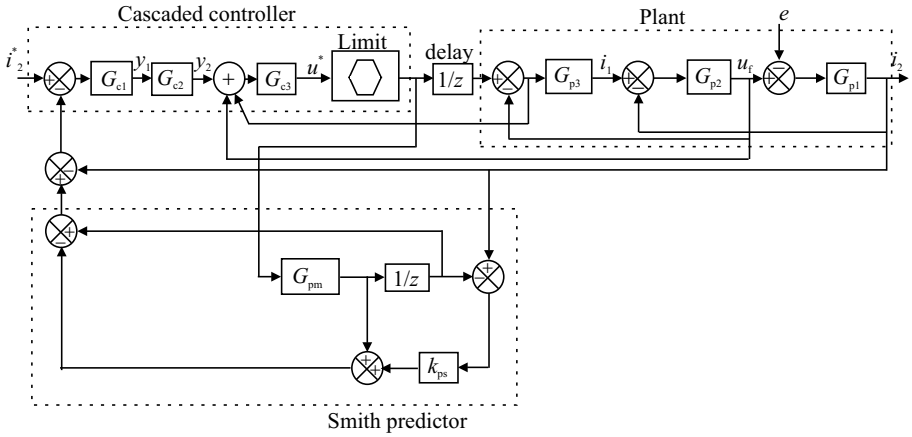

Fig. 2.10 Schematic diagram of the proposed cascaded controller (the z denotes the z transform, thus $1/z$ denotes a delay of one sample). Note that the controller is described in discrete form while the plant is described in continuous form.

The faster the inner loop is in comparison with the outer loops, the better the performance of the cascaded control system becomes in the sense of the transient response [49]. However, reduced gains for the outer controllers will reduce the overall bandwidth of the system. Hence, the inner controller gain is set to the dead-beat gain as [20]

$$k_{\mathrm{p3}} = \frac{L_1}{T_\mathrm{s}} + \frac{R_1}{2} \ . \tag{2-32}$$

The Smith predictor gain is set to a small value to stabilize the overall controller, while k_{p2} and k_{p1} are tuned by changing their values and examining the Bode plot. In Fig. 2.11 the value of k_{p2} is set to 30% of k_{p3}, while k_{p1} assumes values between 30% and 100% of k_{p2}. The same is performed in Fig. 2.12 by setting k_{p1} as 70% of k_{p2}, to achieve a high bandwidth and no overshoot, while k_{p2} is taking values between 25% and 70% of k_{p3}. It is shown by the phase plot in the figure that for k_{p2} values of 70% to 50% of k_{p1} the controller becomes unstable. Hence, the value of k_{p2} has been chosen to 30% of k_{p1}. The values used for the gains are listed in Appendix D.

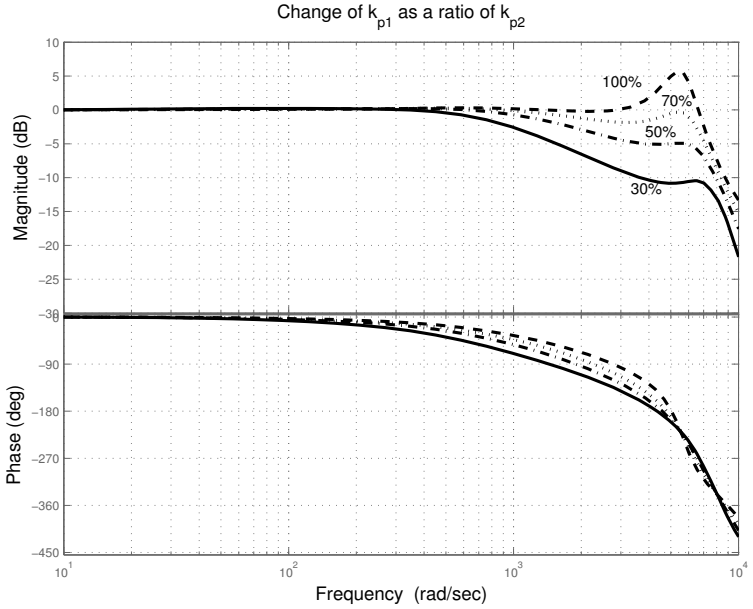

Fig. 2.11 The closed loop system frequency performance as k_{p1} is changed as a certain percentage of k_{p2}, with k_{p2} constant.

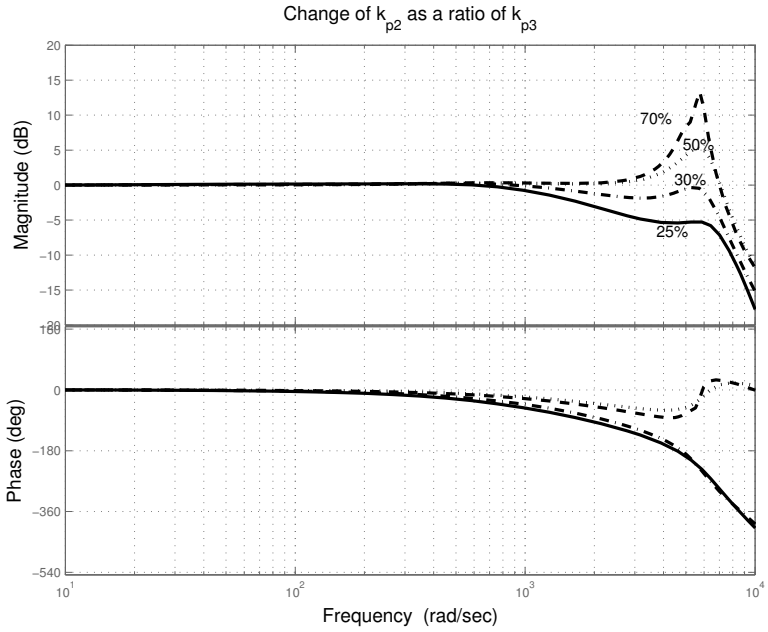

Fig. 2.12 The closed loop system frequency performance as k_{p2} is changed as a certain percentage of k_{p3}, while k_{p1} is constant.

2.7 Current reference generation with inductance-capacitance-inductance line filter

The current references are generated, in the same way as for the L-filter, as

$$\begin{bmatrix} i_{2\mathrm{d}}^{*} \\ i_{2\mathrm{q}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{d}} & e_{\mathrm{q}} \\ e_{\mathrm{q}} & -e_{\mathrm{d}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ \omega C_{\mathrm{f}} \left(u_{\mathrm{cd}}^{2} + u_{\mathrm{cq}}^{2} \right) \end{bmatrix} - \begin{bmatrix} -\omega C_{\mathrm{f}} u_{\mathrm{cq}} \\ \omega C_{\mathrm{f}} u_{\mathrm{cd}} \end{bmatrix} \quad (2\text{-}33)$$

where Δp is the active power dissipated in the filter, and is a function of the grid side and converter side currents

$$\Delta p = R_1\left(i_{1d}^2 + i_{1q}^2\right) + R_2\left(i_{1d}i_{2d} + i_{1q}i_{2q}\right) + \omega L_2\left(-i_{1d}i_{2d} + i_{1q}i_{2d}\right). \tag{2-34}$$

The current references are generated in the same manner for the DVCC[6].

2.8 Conclusions

Two distributed generation systems with a voltage source converter as a front end and two line filters; namely L-filter and LCL-filter, are considered. Vector current controllers have been proposed to control the injected grid currents for both systems. The controller for the L-filter system is based on the dead-beat control and is modified to deal with one sample time delay, integrator windup, grid voltage saturation and grid voltage imbalance. The controller shows good reference tracking even in the worst case of increased current steps. In addition, in the case of controllable DC-link voltage, the current references have been derived in such a way that a regulated DC-link voltage is provided even in the case of unbalanced grid voltage. On the other hand, a cascaded current controller has been proposed for the LCL-filter system. The current references have also been derived in the same manner as for the L-filter system.

[6] The detailed derivation is given in Appendix E and Paper C.

Chapter 3

Voltage Dips Ride-Through Capability

In this chapter, the effect of all possible voltage dips that could appear at the terminal of a converter interfaced DG unit is examined. The two distributed generation systems, described in the previous chapter, with two different line filters are compared regarding the injected grid currents and the DC-link voltage regulation. Moreover, design equations are derived to be able to predict the maximum currents that are expected to flow through the converter switches during different voltage dips.

3.1 Voltage dips definition

A voltage dip is a phenomenon that is experienced at the end user terminals mainly due to a short circuit fault at a certain point in the electrical network. It can also happen due to motor starts or overloads. It is, as defined by IEEE-std 1159-1995 [50], a decrease to between 0.1 to 0.9 p.u. in the RMS value of the voltage at the power frequency for durations of 0.5 cycle to 1 min. Using this definition, the voltage dip magnitude is referring to the remaining voltage.

In spite of the short duration, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [51]. To deeply study the effect of voltage dips on DGs with a power-electronics interface, the classification found in [52] has been adopted.

3.2 Voltage dips classification

Starting from the different types of faults that can occur in a power system, a classification of voltage dips has been accomplished in [52]. It depends on how the load is connected and how the windings of the

supplying transformer are connected. According to this classification, there are seven types of dips designated with the letters "A" to "G". The system in Fig. 3.1 has been used to quantify the magnitude of a voltage dip in a radial system. In this system, the fault occurs at a remote distance from bus 2 and the load, which could be a DG (as in the thesis), is connected at bus 3. Two impedances are connected to bus 2: the impedance of the system, denoted by Z_S, which represents Thevinin's equivalent impedance of the power system, and the fault impedance Z_F. The load is connected through a transformer to bus 2, at which the voltage, in p.u., is given by

$$V_{dip} = \frac{Z_F}{Z_F + Z_S}. \tag{3-1}$$

It is assumed that the pre-fault voltage is used as reference and is equal to 1 p.u. This typically means that voltage dips originated in the transmission system are shallow (since Z_s is small), while voltage dips originated at distribution level can be deep.

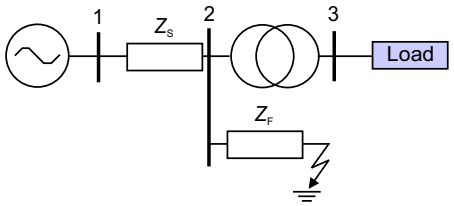

Fig. 3.1 General single-line model for dips classification.

If first it is assumed that the *X*/*R* ratio of the impedances Z_S and Z_F is the same, then V_{dip} has zero phase angle. The resulting voltage dip at bus 3 can be of type "A", which could be a result of a three-phase balanced fault, or any of the six unbalanced types denoted with letters "B" through "G" and reported in Fig. 3.2. In the figure, $E_{i,dip} = E_i V_{dip}$ where the subscript i denotes the phase sequence and takes the values 1, 2, and 3[7], and E_i represents the RMS value of the healthy phase voltage.

[7] Afterwards the three phases will be referred to as a, b, and c.

The transformer connection type has an effect of changing the voltage dip from one type to another. Still, in this work, all dip types are considered for the purpose of providing a general analysis.

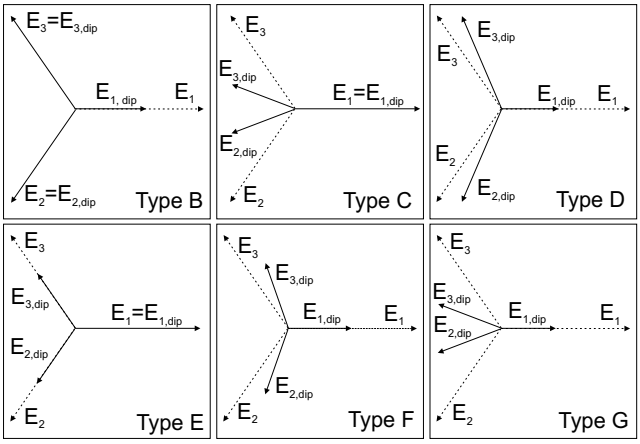

Fig. 3.2 Unbalanced voltage dip classification from "B" to "G". Phasors of three phase voltage before (dotted) and during (solid) fault are displayed. The classification is adopted from [52].

3.3 Voltage dips associated with phase angle jump

If the *X*/*R* ratio for Z_S and Z_F is different, the voltage dip seen at the terminals of the load will have a phase angle "ψ" called "phase angle jump". The impedance angle α is defined as

$$\alpha = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \tag{3-2}$$

where $Z_S = R_S + jX_S$, $Z_F = R_F + jX_F = zl$, z is the feeder impedance per unit length and l is the feeder length. The expression of the voltage dip at bus 2 will be

$$v_{dip} = \frac{\lambda e^{j\alpha}}{1 + \lambda e^{j\alpha}} = V_{dip}\angle\psi \tag{3-3}$$

where $\lambda\, e^{j\alpha} = zl / Z_S$.

The four values for the impedance angle α, that are suggested in [52], are considered: 10^o as the highest expected value for transmission system faults, 0^o as the reference value, -20^o for overhead distribution lines, and -60^o for underground distribution cables. In Fig. 3.3, the relation between the phase angle jump and different dip magnitudes at the four impedance angles is shown. The phase angle jump is larger for smaller dip magnitudes and is more sensitive to the dip magnitude when $\alpha = -60^o$.

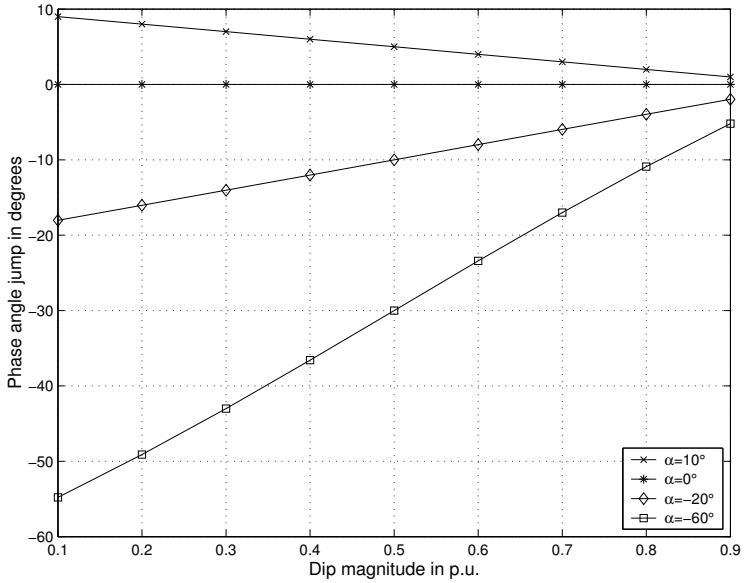

Fig. 3.3 Phase angle jump for different dip magnitudes and impedance angles.

3.4 Positive/negative sequence sub-classification

The magnitudes of the positive sequence (E_p) and the negative sequence (E_n) of the grid voltage for dip types "A" through "G" are calculated using Park transformation and summarized in Table 3-1, where E is the phase-to-phase RMS grid voltage. It shows that dips "C" and "D" have the same positive and negative sequence magnitudes. The same applies for dips "E", "F", and "G". However they may affect the system in different ways

according to Table 3-2, at which the positive and negative sequence components in the *dq*-coordinate system have been calculated. It shows that dips "C" and "D" result in different negative sequence *dq*-components. The same also holds for dip types "F" and "G", while dips "E" and "G" are exactly the same since they both result in the same positive and negative sequence components. This classification is useful in understanding the effect of unbalanced voltage dips on the system. Hence, the following study is carried out using the dual vector current controller (DVCC) that has been described in the previous chapter.

Table 3-1 Positive and negative sequence magnitudes of grid voltage for dip types "A" through "G".

Dip type	E_p	E_n
A	EV_{dip}	0
B	$\frac{E}{3}\sqrt{4+4V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
C, D	$\frac{E}{2}\sqrt{1+2V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{2}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
E, F, G	$\frac{E}{3}\sqrt{1+4V_{dip}\cos\psi+4V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$

Table 3-2 Positive and negative sequence components of the grid voltage in *dq*-coordinates for dip types "A" through "G".

Dip type	e_{dp}	e_{qp}	e_{dn}	e_{qn}
A	$EV_{dip}\cos\psi$	$EV_{dip}\sin\psi$	0	0
B	$\frac{E}{3}(2+V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
C	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{E}{2}(1-V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$
D	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{-E}{2}(1-V_{dip}\cos\psi)$	$\frac{-E}{2}V_{dip}\sin\psi$
E	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$
F	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
G	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$

3.5 Current through the voltage source converter caused by voltage dips

At the distribution level, the voltage source converter (VSC) mostly utilizes isolated gate bipolar transistors (IGBT's). An IGBT is easy to turn on and off, and has low conduction and switching losses [13]. The ratings of a single IGBT can be up to 1.2 kA and 3.3 kV. It has good switching capability (up to 100 kHz for a few kW applications), but for very high power devices and applications the frequency is limited to some kHz. On the other hand, the main drawback is poor overcurrent capability, i.e. it cannot withstand more than the peak current it is designed for, even for a short period of time. Hence, the current that would flow through the IGBTs during voltage dips could have a destructive effect if the valves are not designed to withstand this current level.

In order to calculate the required current rating of the VSC valves to ride through voltage dips occurring at the grid, the maximum current has been calculated for all the dip types. The current components in *dqp*- and *dqn*-frame are calculated using the following assumptions:

1. No switching-losses, which means that the AC active power P_1 of the converter is equal to the DC input power KP_{dc}.
2. In addition, the oscillating powers that are produced due to the imbalance are assumed to be supplied from the VSC side to simplify the calculations.
3. Furthermore, for simplicity, the phase angle jump is assumed to be zero, which results in zero *qp*- and *qn*-components of the grid voltage as seen by Table 3.2.
4. Moreover, perfect tracking is assumed, resulting in equal reference and actual currents.

Using (2-26), the grid currents are described as

$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \frac{KP_{dc}}{e_{dp}^2 - e_{dn}^2} \begin{bmatrix} e_{dp} \\ 0 \\ -e_{dn} \\ 0 \end{bmatrix} \tag{3-4}$$

where P_{dc} is the nominal input DC power and K is the ratio of the input power that is actually delivered to the DC link. The current components are then transformed back to the $\alpha\beta$-coordinates in positive- and negative-sequence frames and then into three-phase currents.

In the case of single phase faults (dip types "B" and "D"), the maximum phase current (phase *a*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp} + e_{dn}} \tag{3-5}$$

while for two phase faults (dip types "C", "E", "F", and "G"), the maximum phase current (phase *b*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp}^2 - e_{dn}^2} \sqrt{\frac{1}{4}\left(e_{dp} - e_{dn} \right)^2 + \frac{3}{4}\left(e_{dp} + e_{dn} \right)^2} \; . \tag{3-6}$$

For three phase faults (dip type "A"), the maximum phase current is

$$I_{max} = \sqrt{\frac{2}{3}} . \frac{K P_{dc}}{E \times V_{dip}} . \tag{3-7}$$

The values of e_{dp} and e_{dn}, which are the positive and negative sequence of the *d*-component of the grid voltage, are calculated using Table 3-2 for different voltage dips.

A comparison between the analytically calculated current values and the simulated ones has been performed for all dip types, in order to verify the analytical equations. For instance, the result with dip type "A" is shown in Fig. 3.4[8], where the simulation[9] has been carried out for the L-filter case. It will be shown later that the currents produced with the LCL-filter have the same amplitudes as for the L-filter, using the same value of the series inductance. As shown by the figure, the calculated curve shows overestimated current values, since the dissipated powers by the filter were

[8] Another example is shown in Paper A.

[9] The simulation has been carried out here in MatLab/Simulink.

neglected in the design equations while they were incorporated in the simulation.

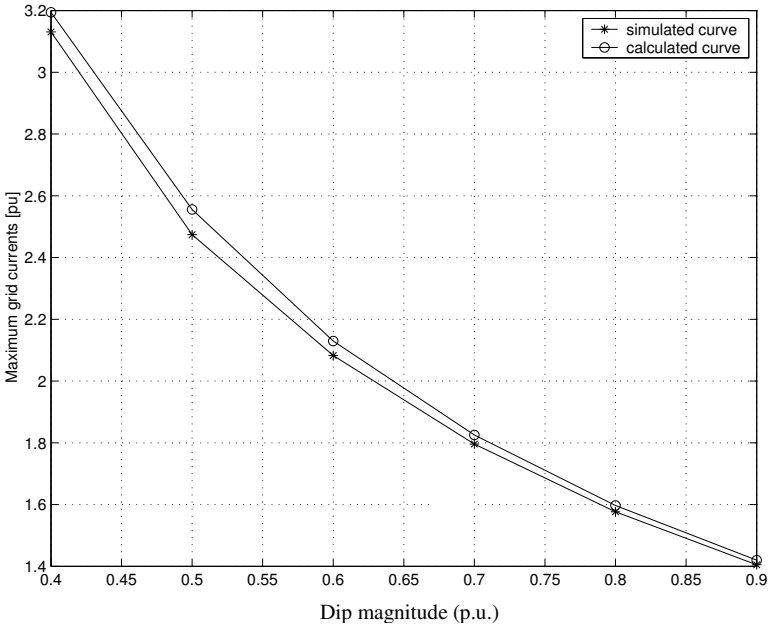

Fig. 3.4 Maximum currents due to voltage dip of type "A".

3.6 Ride-through capability for DGs with L-filter

Depending on the maximum currents that could flow during different voltage dips and using some statistical data regarding the most frequent dip types at the grid, the converter switches could be designed to withstand the increased currents. The peak-to-peak DC-link voltage in case of grid-voltage dips should also be considered in the design of the DC-link. However, the DC-link voltage ripples are found to be negligible when the oscillating powers that are resulting due to the grid-voltage imbalance, are assumed to be supplied from the grid side. This case has been found to be the optimal one for the controller design, if ride-through capability is to be considered.

The effect of all types of dips, with various magnitudes and zero phase angle jump, on the maximum grid current and DC voltage ripples is represented in Fig. 3.5. The maximum current the converter switches should

be able to hold is 3.65 p.u., which happens at 30% dip type “D”. The maximum DC voltage ripple is about 2.5% peak-to-peak and it occurs at 30% magnitude of dip type “F”.

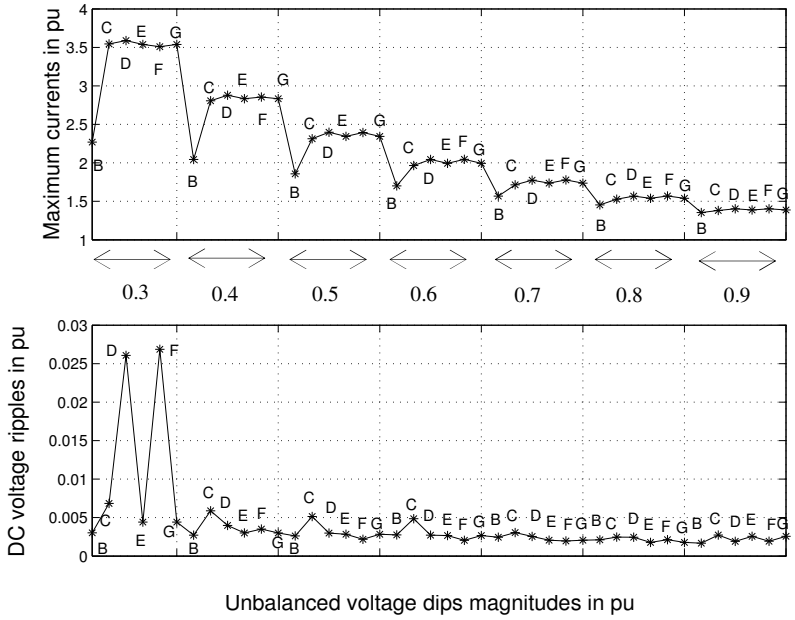

Fig. 3.5 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types.

The effect of the phase angle jump on the DC-link voltage ripples during the dip is found to be negligible. However, their effect over the maximum grid currents is more noticeable as shown in Fig. 3.6. It can be concluded that differences are very small for $\alpha = 10^{o}$ and $\alpha = -20^{o}$ while they seem to be significant when $\alpha = -60^{o}$. In that case the maximum current, with 30% magnitude of dip type “D”, is equal to 4.5 p.u. If the converter valves are designed considering the case of zero phase angle jump, they will be able to handle only 3.65 p.u. current as mentioned previously. Hence, in the case of a voltage dip with phase angle jump, the valves would most probably be destroyed or the VSC will be tripped off.

Moreover, from (3-5), (3-6), and (3-7), it is obvious that there is a direct proportionality between the maximum current and the value of the actual input power. In other words, if the input power is lowered by the ratio *K*, the maximum value of the current will also be lowered by the same ratio. Simulation results presented in Fig. 3.7 represent the effect of lowering the input power P_{in} for different dip types and magnitudes.

Therefore, if the converter switches have to be rated to ride through all dips with 30% minimum magnitude, the current rating can be decreased from about 3.5 p.u. to 3 p.u., if the input power is decreased from 90% to 70% of nominal value.

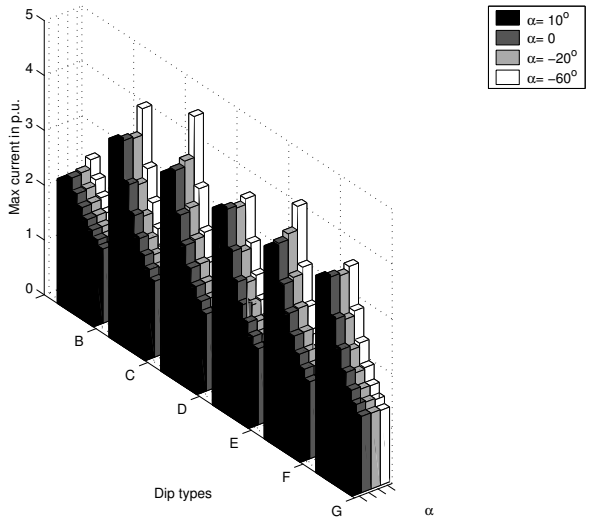

Fig. 3.6 Effect of phase angle jump on the amplitude of phase currents for different unbalanced voltage dips.

One way to optimise the design of the switches is thus to minimize the currents during the fault period, which could be established by temporarily decreasing the input power to the system (decreasing *K* in (3-5), (3-6), and (3-7)) during the fault. If this is possible or not depends on the controllability and the response time of the DC-link or the primary source. By incorporating a DC-chopper, acting as a dump load, or DC energy storage, the input power

could be reduced during the voltage dip period [9]. In addition, for some primary sources it could be possible to reduce the input energy (e.g. by changing the turbine torque reference in wind turbine systems) [36].

On the other hand, if the DC bus is powered by a source that is stochastic in nature, e.g. wind, one could argue that the probability that a dip occurs when the wind turbine is producing full power might be very low, as the turbine often runs at much lower power. Then, to optimize the design it is possible to consider a lower value of the input power, which is delivered by the turbine. This means, accepting a certain risk that the converter (thus the turbine) might still trip, but can lead to greatly reducing the size of the converter[10].

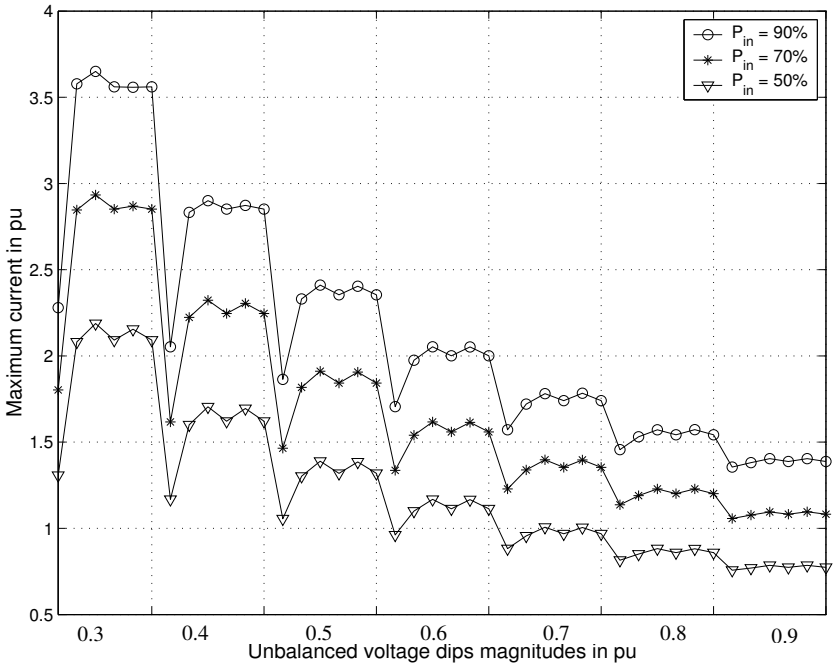

Fig. 3.7 Effect of lowering P_{in} on maximum grid currents for unbalanced voltage dips with magnitudes from 0.3 p.u. to 0.9 p.u. in steps of 0.1. The voltage dip types are shown analogously to Fig. 3.5.

[10] This is investigated numerically by the case study in Paper A.

3.7 Ride-through capability for DGs with LCL-filter

The effect of all unbalanced dips, with various magnitudes, on the maximum grid current and DC voltage ripples (in the middle of the dip period) is presented in Fig. 3.8. The base for the per unit currents is the maximum of the nominal current of the converter. Compared with the case of L-filter interface system (shown in Fig. 3.5 with a current base value equal to the RMS of the nominal current), the currents are almost the same while the DC voltage ripples are slightly increased but still within an acceptable range. This is mainly due to the part of the oscillating power consumed by the filter capacitor and not compensated for in the generated reference currents.

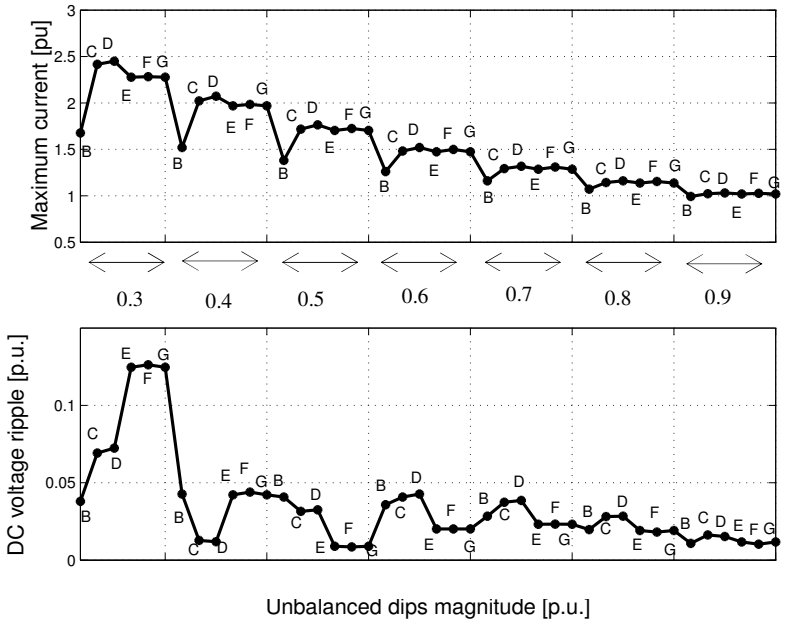

Fig. 3.8 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types and magnitudes from 0.3 to 0.9.

3.8 Conclusions

In this chapter, the effect of different voltage dips over the grid currents and DC-link voltage ripples are examined for the L-filter and the LCL-filter systems. The effect of the phase angle jump has also been examined considering the case when the grid supplies the oscillating powers. It is concluded that the phase angle jump has more effect on voltage dips with smaller magnitudes, and the worst case occurs when the impedance angle $\alpha = -60^{o}$, which corresponds to cable transmission. This effect is more significant for dip types "C" and "D". The maximum current occurs with 30% magnitude of dip type "D" and is equal to 4.5 p.u., i.e. 25% more than its value in case of zero phase angle jump. Thus, the effect of the phase angle jump should be considered when designing the converter switches to ride through all dips.

Since the two considered line filters produce almost the same current amplitudes, having the same value of series inductance, the design equations that have been derived here to calculate the required current ratings of the converter can be used for both systems. These equations give slightly over-estimated values since they are derived without considering the power dissipated in the filter. However, this over-estimation is preferred in the design stage because it gives a safety margin to the design values.

The effect of decreasing the input power has also been examined. Temporarily decreasing the input power to the system during fault reduces the currents during that period, which could be a way to decrease the ratings of the converter valves and in the same time preserving the ride-through capability. This, however, would require that the input power to the DC bus be controllable so as to be reduced very quickly.

Chapter 4

Voltage-Regulation Capability in Weak Grids

By adding a voltage-regulation capability to the DG controller, it is possible to mitigate most of the power quality problems. In addition, this is a highly attractive feature in case of the operation in weak grids. This is the topic of this chapter, where the regulation capability is examined for the mitigation of the decrease of the voltage amplitude specifically in weak grids, the voltage harmonics, and the voltage fluctuation. The DG system with a VSC as a front end and an LCL-filter is considered throughout this chapter. The voltage regulation limits are evaluated regarding the local load of the DG and the DG injected active power. Moreover, the effect of the grid voltage distortion over the phase-angle estimation and the regulation capability is studied. A phase-locked loop (PLL) synthesis based on the extraction of the fundamental component of the grid voltage has been introduced to obtain robust phase estimation.

4.1 Introduction

The term weak grid is here referring to systems where the voltage level is not constant as in a stiff (or strong) grid. Weak grids are usually found in remote areas where the feeders are long. The grids in these areas are usually designed for small loads [32]. When the design load is exceeded, the voltage level may fall below the allowed minimum and/or the thermal capacity of the feeders might be exceeded. Hence, the voltage regulation of long weak distribution lines is an important problem to be considered [30]. The connection of a DG in a weak distribution system can provide voltage support, if the voltage regulation capability is added to its controller, in addition to the main function of injecting active power into the grid. Moreover, by regulating the voltage at the PCC most of the power quality

problems could be mitigated, which might be an attractive requirement in grids with large number of disturbing (non-linear) as well as sensitive loads.

In recent publications, the voltage regulation problem is mainly tackled, in transmission or distribution systems, regarding the power electronics application, using a STATCOM (called DSTATCOM in distribution systems), which is a converter-based shunt connected reactive-power generator. The advantages of a STATCOM, compared to the other thyristor-based reactive power generators (SVCs), are its wider operating area, better performance, and greater application flexibility [75]. The implementation of the DSTATCOM has been discussed in [37], [38] and [58], [60] for voltage flicker mitigation, controlling both the active and the reactive injected powers. In [31] a DSTATCOM is used to regulate and balance the voltage at the distribution bus using only reactive power injection. The voltage regulation limits, however, have not been discussed. Although the application of a STATCOM and a DG are similar in the utilization of a converter as a front end, they are different from the point of view of the active power. STATCOMs could have controllable active power (depending on the grid needs) if they are connected to an energy storage device, while DGs are injecting constant active power that could change due to the changes in the energy source. The DG constant injected active power, consequently, puts some limits on the voltage regulation capability as will be investigated later in this chapter.

The voltage regulation using converter-interfaced DG systems, specifically with LCL-filters at the connection point to the grid, has been less introduced in literature since the emphasis is usually set on the DG technology, not from the power system point of view, and the DG system controllers. Still an example for such a system is found in [32], where a single phase VSI interface of a photovoltaic DG connected to a weak grid through an LCL-filter is considered regarding the voltage regulation purpose. The control algorithm measures the phase of the terminal voltage using Fourier extraction and then computes the required inverter voltage for the desired active and reactive power export commands. The feedback of the filter states has been used to provide the stability of the controller at higher

frequencies. The control of the real and the reactive power flow is done on a cycle-by-cycle basis. Hence, it takes several cycles for the system to settle. Although in [33] the application of a variable speed wind turbine (VSWT) system connected to a weak grid is considered, the emphasis has been placed on the control of the converters for the system and the voltage compensation has been of no interest. The compensation for grid-voltage harmonics has been the main topic of [78], where an inverter-based DG with an L-filter at the connection point to the grid has been considered. Three adaptive regulator gains have been calculated for the 5^{th}, the 7^{th} and the higher harmonics to produce the proper current commands. The focus has been put only on the voltage harmonic compensation, hence the voltage regulation is not considered and the controller takes long time to reach the steady state.

In this chapter, the cascaded controller for the DG system with an LCL-filter[11] is implemented along with a point of common coupling voltage regulator to add the voltage regulation capability. The voltage regulation capability limits are also discussed regarding the DG local load and the DG injected active and reactive powers. Since the output voltage of the VSC is synchronized with the grid voltage using an estimated phase angle, the error in this angle that is mainly due to the distorted grid voltage, should be minimal. The grid voltage phase angle is estimated using a phase locked loop (PLL), which is implemented in the *dq*-frame using a PI controller that tracks the changes in the *q*-component grid voltage by producing the necessary change in the phase angle. This PLL has been well established before [53], however it is first explained here since it will be modified in order to eliminate the effect of the grid voltage power quality problems on the estimated phase angle.

4.2 Phase locked loop (PLL)

The synthesis of the PLL that is commonly used for grid-connected three-phase power conversion systems [53] is based on the quadrature-component extraction of the grid voltage. Hence it will be referred to, here, as a Q-PLL.

[11] This controller has been explained in Chapter 2.

Assuming a balanced three-phase grid voltage at the point of common coupling (PCC)

$$u_{\mathrm{a(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\theta\,, \tag{4-1}$$

$$u_{\mathrm{b(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta - \frac{2\pi}{3}\right), \tag{4-2}$$

and

$$u_{\mathrm{c(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta + \frac{2\pi}{3}\right) \tag{4-3}$$

where U_{PCC} is the line RMS voltage at the PCC, and θ is its phase angle.

Transforming the voltage from three-phase notation into a voltage vector in a fixed $\alpha\beta$-frame, using power invariance transformation, the resulting voltage vector will be

$$\underline{u}_{\alpha\beta} = U_{\mathrm{PCC}}\left(\sin\theta + \mathrm{j}\cos\theta\right). \tag{4-4}$$

Normalizing this voltage vector and transforming it into a rotating dq-coordinate system, which rotates with the estimated angular frequency ($\hat{\omega} = \mathrm{d}\hat{\theta}/\mathrm{d}t$), the resulting normalized voltage-vector components will be

$$\underline{u}^{\mathrm{n}}_{\mathrm{dq}} = \cos\left(\theta - \hat{\theta}\right) + \mathrm{j}\sin\left(\theta - \hat{\theta}\right) \tag{4-5}$$

where $\hat{\theta}$ is the estimated phase angle.

If the estimation error ($\varepsilon = \theta - \hat{\theta}$) is very small, then $u^{\mathrm{n}}_{\mathrm{d}} \cong 1$ (the real part in (4-5)) and $u^{\mathrm{n}}_{\mathrm{q}} \cong \varepsilon$ (the imaginary part in (4-5)). Hence, the normalized q-component of the voltage can be used as an input to a PI-controller to produce a required change in the angular frequency ($\Delta\omega$) to track the changes in the phase angle. The Q-PLL main block diagram is shown in Fig. 4.1.

The on-line normalization of the voltage vector will result in nullifying the phase estimation error due to a balanced voltage amplitude change (e.g. three-phase voltage dips). However, in case of unbalanced voltage dips,

oscillations with double the fundamental frequency of the grid will be superimposed on the estimated frequency. These oscillations will result in an error in the estimated phase-angle of the grid-voltage.

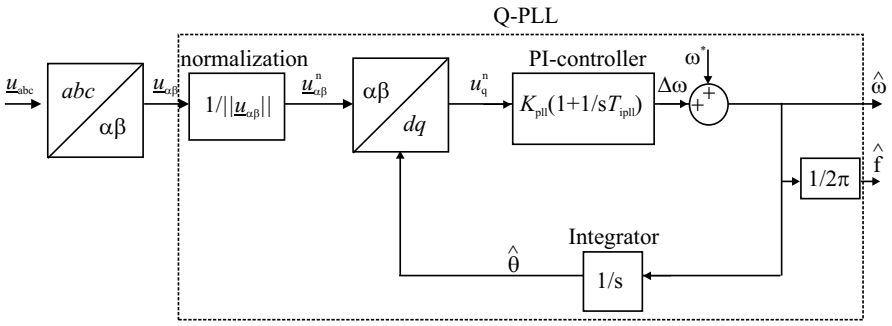

Fig. 4.1 Phase estimation using Q-PLL.

To eliminate this error, the positive sequence of the voltage-vector *q*-component is used as an input to the Q-PLL. This PLL is referred to as a positive sequence PLL (PS-PLL). This PLL is implemented in [55] and [56] by the use of low pass filters (LPF). However, a trade-off has to be made between robustness and good transient performance of the LPFs. Hence, it is instead implemented here as suggested in [57] using the delayed signal cancellation algorithm (DSC) to extract the positive sequence component of the voltage. As shown in Fig. 4.2, the three-phase voltages are measured and transformed into a vector in the stationary αβ-frame. Then the positive sequence voltage vector is extracted using the DSC algorithm, and fed into the Q-PLL that has been described in Fig. 4.1.

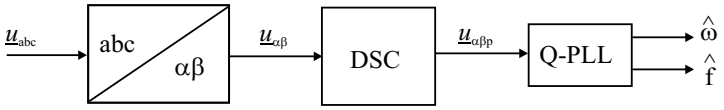

Fig. 4.2 Positive-sequence PLL.

To investigate the effect of the voltage imbalance on the PLL performance, an unbalanced voltage dip of type "C" and remaining voltage amplitude of 0.4 p.u. is applied from 0.5 s to 0.7 s. The estimated frequency

using the Q-PLL and using the PS-PLL are shown in Fig. 4.3 by the middle and lower plots respectively. The estimated frequency using PS-PLL is fairly unaffected by the unbalanced voltage dip apart from the transients at the start and the end of the dip. These transients last for one quarter of the fundamental period and they are resulting due to the implementation of the DSC.

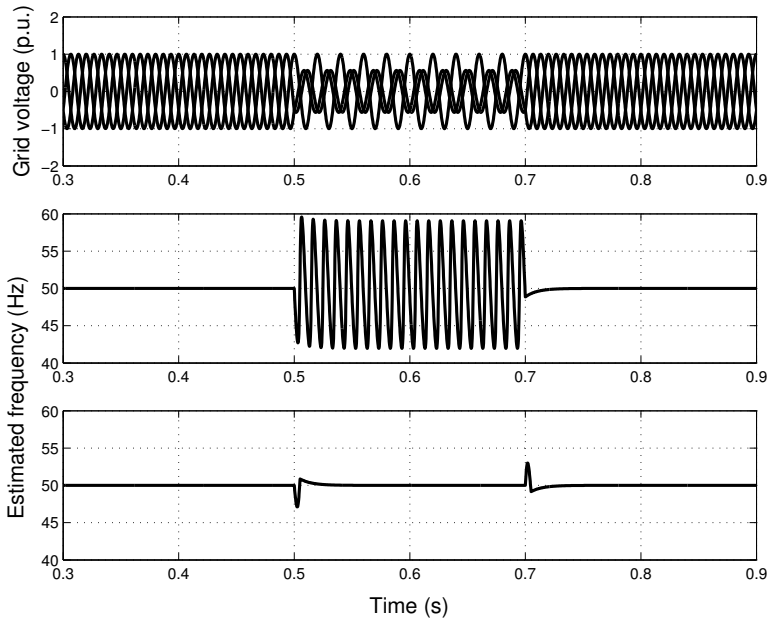

Fig. 4.3 Grid voltage (upper), and estimated frequency using Q-PLL (middle) and PS-PLL (lower).

4.3 PCC-voltage regulation limits

The voltage-regulation capability limit of a converter-interfaced DG is mainly related to the need for the DG to inject constant active power into the grid. To investigate this limit further, the simple weak grid system that is shown in Fig. 4.4 is considered. The parameters that are used for the weak-grid system are listed in Appendix C. For simplicity, it is assumed that the grid impedance Z_s is pure reactive ($Z_s = j\,X_s$). The grid is supplying a load at

the far end of the feeder, where a DG is also connected. It is assumed first that the load is disconnected and the DG is supplying both active power P_{DG} and reactive power Q_{DG} to the grid.

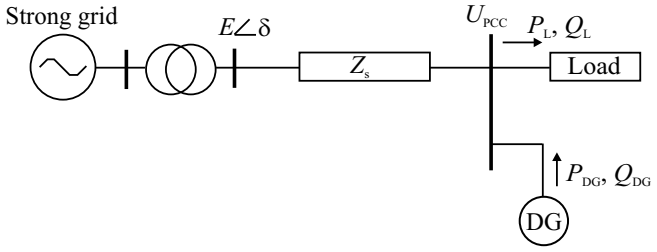

Fig. 4.4 Direction of power flow from VSC to PCC.

The power flow through the system is described by [54]

$$P_{DG} = \frac{U_{PCC}E}{X_s}\sin\delta \tag{4-6}$$

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \frac{U_{PCC}E}{X_s}\cos\delta \tag{4-7}$$

where E is the strong grid RMS line voltage, and δ is the grid voltage angle.

Using (4-6), the adjacent side for the angle δ can be calculated. Then

$$\cos\delta = \frac{\sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}}{\frac{U_{PCC}E}{X_s}}. \tag{4-8}$$

Substituting (4-8) in (4-7), Q_{DG} is obtained as

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}\ . \tag{4-9}$$

The voltage at the strong grid bus E is assumed to be equal to 1 p.u. Since the application of a DG requires injecting constant active power to the grid, the change in the reactive power leads to a change in the voltage at the PCC

(U_{PCC}) as suggested by (4-9). However, the value of the input active power affects the amount of the reactive power that is available for the compensation. A higher value of the injected active power implies that a higher value of reactive power can be injected, considering the same equation. Yet, that implies higher injected current, which could be an issue for the VSC valves capacity and protection[12], and also the increase of the DC-link voltage ripples might be another issue. An illustration of this is presented in Fig. 4.5[13], where the voltage regulation capability has been examined for a case when the grid voltage has a modulating signal with an 8% amplitude superimposed on the fundamental component. The input power from the DG source has been varied from 70% to 140% of the nominal value.

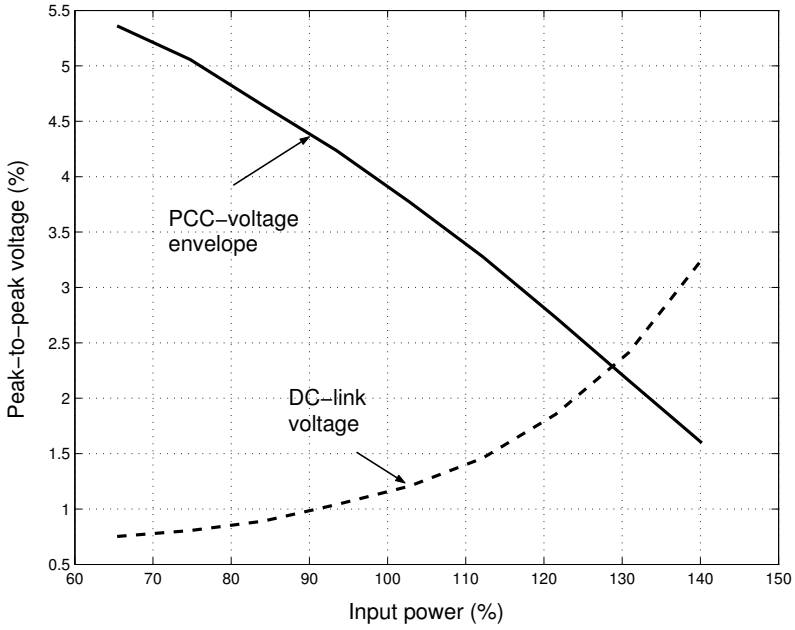

Fig. 4.5 Effect of the injected input power on the PCC voltage envelope oscillation (solid) and DC-link voltage ripples (dashed).

[12] That has been discussed in the previous chapter and in Paper A.
[13] Further details are provided in Paper E.

With the voltage regulation capability, the PCC-voltage has been better regulated at the upper value of the injected active power, where the grid voltage amplitude modulation has been reduced to 1.5%. On the other hand, the DC-link voltage ripples has increased to about 3.2% of its nominal value. Although negligible in value, in this example, the DC ripples amplitude could have a more significant value, for instance, if the amplitude of the modulating signal increases.

Equation (4-9) can be rearranged as

$$P_{\mathrm{DG}}^2 + \left(Q_{\mathrm{DG}} - \frac{U_{\mathrm{PCC}}^2}{X_{\mathrm{s}}} \right)^2 = \left(\frac{U_{\mathrm{PCC}} E}{X_{\mathrm{s}}} \right)^2 . \tag{4-10}$$

Equation (4-10) represents a circle with the radius of $U_{\mathrm{PCC}}E/X_{\mathrm{s}}$ and the centre at $(0,U^2_{\mathrm{PCC}}/X_{\mathrm{s}})$. By varying U_{PCC}, different power circles will result representing different possible operating points related to different values of the injected (or drawn) DG active and reactive powers. Those power circles have been illustrated in Fig. 4.6, where only the possible operating area has been shown (for the PCC voltage varying between 0.5 p.u. and 1 p.u.).

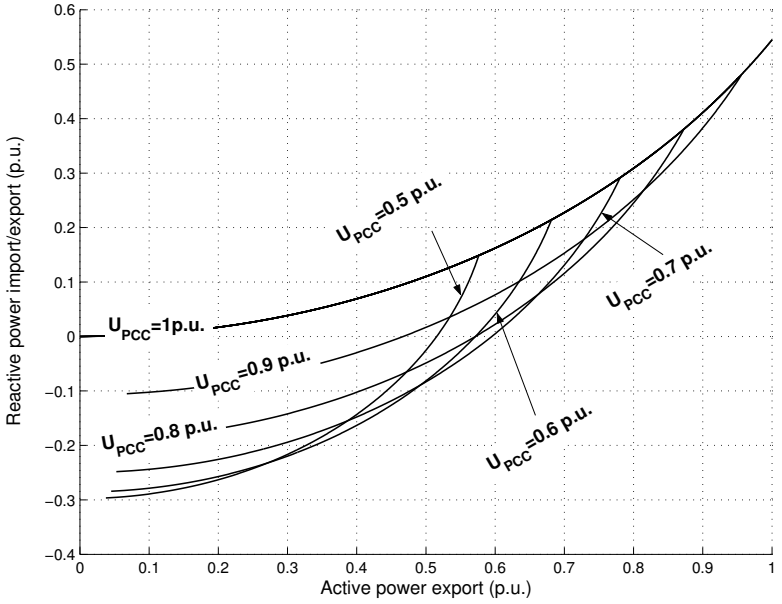

Fig. 4.6 DG import/export power with unloaded weak grid for different PCC voltages.

The figure is indicative of the amount of the reactive power to be injected by the DG at a specific value of the injected active power and a certain voltage drop over the feeder. For instance, for a PCC voltage of 0.7 p.u. and injected active power of 0.5 p.u., the injected reactive power should equal to the difference between the two values resulting from the intersection of the 0.5 p.u. power line and the two circles related to the PCC voltages of 1 p.u. and 0.7 p.u. (in this example, the injected reactive power will be about 0.2 p.u.). For the same PCC voltage (0.7 p.u.), if the DG injected power is 0.8 p.u., this operating condition will represent an unstable operation since the 0.8 p.u. power line does not intersect with the 0.7 p.u. circle.

To calculate the maximum reactive power that should be injected to regulate the voltage at the PCC with different voltage drops, (4-9) is differentiated with respect to the PCC voltage U_{PCC} and the result is set to zero. Then the resulting voltage that would acquire maximum injected reactive power is U_{limit}

$$U_{\mathrm{limit}} = X_{\mathrm{s}} \sqrt{\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2} \ . \tag{4-11}$$

The reactive power lower limit Q_{limit} that will result in maximum injected DG reactive power (to regulate the PCC voltage) is then related to the DG injected active power as

$$Q_{\mathrm{limit}} = X_{\mathrm{s}} \left(\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2 \right) - \frac{1}{2X_{\mathrm{s}}} \, . \tag{4-12}$$

Equation (4-12) is depicted in Fig. 4.7, where it shows again that the maximum power to be injected is inversely proportional to both the PCC voltage and the DG injected active power. The difference between the two curves in the figure indicates the necessary injected reactive power.

To investigate the effect of the loading on the compensation capability of the DG, it is now assumed that a static constant-power load is connected at

the PCC in Fig. 4.4. With a constant-power load, the power circles would be shifted up and/or to the right depending on the load reactive and active powers respectively. This should, in turn, increase the voltage compensation limit of the DG. However, an increased amount of the load reactive power, shifting the circles up, will imply more DG injected reactive-power to compensate for the voltage.

Assuming a constant active power load of 0.1 p.u., the operational part of the power circles relating the DG active and reactive powers to the grid voltage at the PCC is shown in Fig. 4.8. For instant, if the voltage at the PCC is 0.7 p.u. and the input DG active power is 0.8 p.u., then this will imply a stable operation with about 0.1 p.u. reactive power to be injected into the grid to regulate for the voltage.

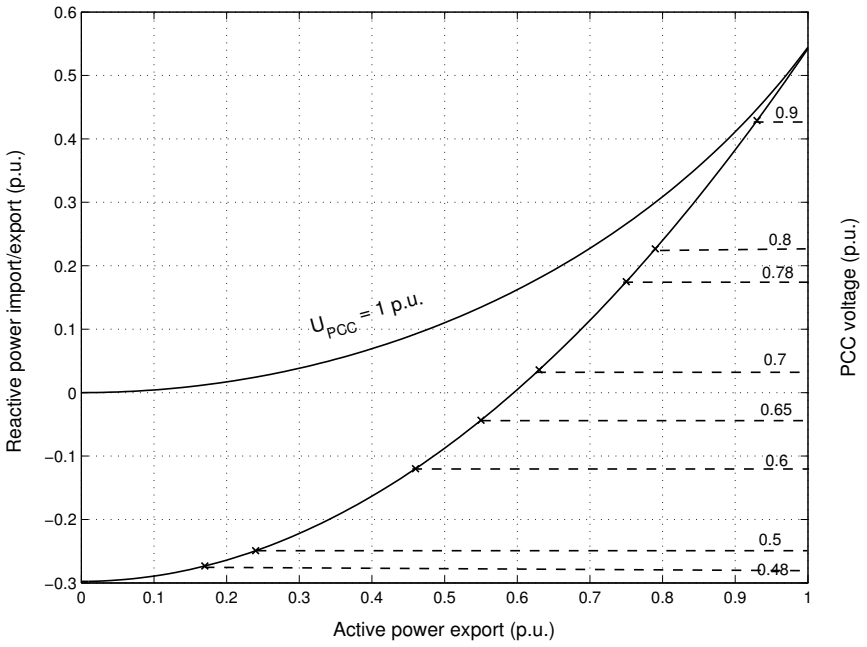

Fig. 4.7 Maximum reactive power (i.e. vertical difference between the two curves) to be injected related to the PCC voltage and the DG injected active power.

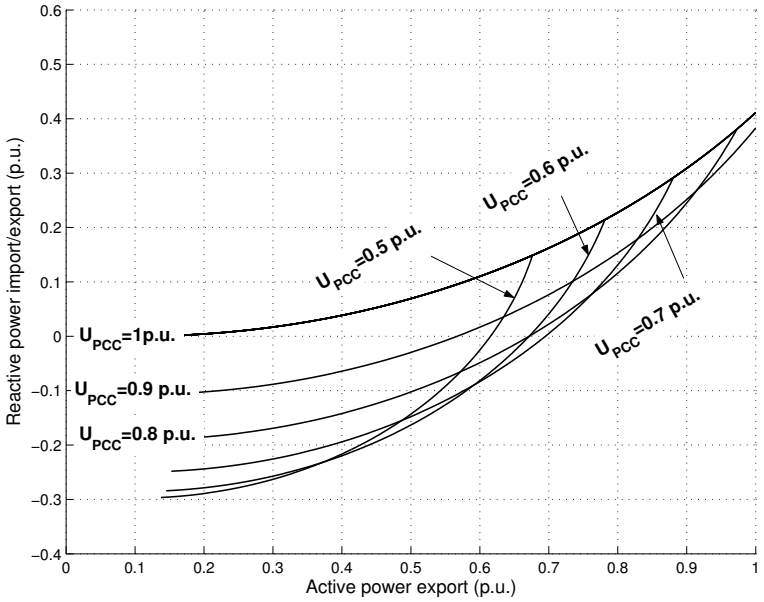

Fig. 4.8 DG import/export power with a constant power load of P_L = 0.1 p.u. and Q_L = 0.0 p.u.

It is worth noting here that the above discussion has been carried out assuming a lossless feeder. By decreasing the *X*/*R* ratio of the feeder, the resistive voltage drop will increase implying decreased PCC voltage related to the same loading condition. For instance, for a pure resistive feeder (Z_s = R_s) the equations for the active and reactive power flow through the feeder will be reversed. That means

$$Q_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}E}{R_{\mathrm{s}}}\sin\delta \tag{4-13}$$

$$P_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}^2}{R_{\mathrm{s}}} - \frac{U_{PCC}E}{R_{\mathrm{s}}}\cos\delta\,. \tag{4-14}$$

This implies that the voltage at the PCC will become more sensitive to the active power change and less sensitive to the reactive power change. This will result in an increased amount of the reactive power to regulate the

voltage compared to the case with a pure inductive feeder. Hence, the decreased *X*/*R* ratio will account for another limit for the regulation capability.

4.4 PCC-voltage regulator

The DG injected reactive power is adjusted by the PCC-voltage regulator to maintain the 1 p.u. grid voltage amplitude. The regulator has been implemented regarding the instantaneous reactive power generated by the DG at the PCC, which is described as

$$q_{(\mathrm{PCC})} = u_{\mathrm{q(PCC)}} i_{2\mathrm{d}} - u_{\mathrm{d(PCC)}} i_{2\mathrm{q}} . \tag{4-15}$$

Since the voltage-oriented synchronous-frame transformation sets the *q*-component of the voltage into zero, then $i_{2\mathrm{q}}$ is used to control the reactive power flow. Since $u_{\mathrm{d(PCC)}}$ is to be regulated, then the reactive current reference is generated to compensate the error in the voltage using a PI-controller[14], as follows

$$i_{2\mathrm{q}}^{*}(k) = k_{\mathrm{pr}} \varepsilon_{\mathrm{e}}(k) + \frac{k_{\mathrm{pr}} T_{\mathrm{s}}}{T_{\mathrm{ir}}} \sum_{n=1}^{k} \varepsilon_{\mathrm{e}}(n-1) \tag{4-16}$$

$$\varepsilon_{\mathrm{e}}(k) = u_{\mathrm{d(PCC)}}(k) - u_{\mathrm{d(PCC)}}^{*}(k) \tag{4-17}$$

where

k_{pr} is the proportional gain of the PCC-voltage regulator;

k is the sampling instant;

T_{ir} is the integral time; and

T_{s} is the sampling time.

Assuming, now, that the loading condition of the grid allows for a stable operation of the PCC-voltage regulator, the mitigation of the power quality problems at the grid is to be considered next.

[14] The controller parameters are given in Appendix D.

4.5 Compensation for grid-voltage harmonics

The effect of the voltage harmonics on the estimated phase using the PS-PLL is first discussed. If it is assumed that the voltage has a harmonic signal that is superimposed on the fundamental component, then it can be described in the αβ-frame as

$$\underline{u}_{\alpha\beta}(t) = U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \tag{4-18}$$

where

U_1 and U_h are the amplitudes of the fundamental and the h^{th} harmonic respectively;

ω is the fundamental grid-voltage angular-frequency; and

h_s is the related harmonic sequence that takes a value of either $+1$ (for positive sequence) or -1 (for negative sequence) according to [54]

$$h_s = \begin{cases} +1 & h = 3n+1 \\ -1 & h = 3n+2 \\ 0 & h = 3n \end{cases} \tag{4-19}$$

where n is a positive integer starting from zero.

The zero sequence harmonics will not be treated in this analysis due to the absence of a neutral wire.

Substituting (4-18) in (2-15), the positive-sequence vector of the grid voltage in $\alpha\beta-$frame is:

$$\begin{aligned} \underline{u}_{\alpha\beta\mathrm{p}}(t) &= \frac{1}{2}\left(U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t}\right) \\ &+ \frac{\mathrm{j}}{2}\left(U_1 e^{\mathrm{j}\omega(t-T_g/4)} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega(t-T_g/4)}\right) \end{aligned} \tag{4-20}$$

where $\dfrac{\omega T_g}{4} = \dfrac{\pi}{2}$.

The harmonic part of (4-20) can be expressed using trigonometric functions as follows

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = \frac{U_{\mathrm{h}}}{2}\left(\cos(h\omega t) + \mathrm{j}(h_{\mathrm{s}})\sin(h\omega t)\right) + \mathrm{j}\frac{U_{\mathrm{h}}}{2}\cos\left(h\omega t - h\frac{\pi}{2}\right) - (h_{\mathrm{s}})\sin\left(h\omega t - h\frac{\pi}{2}\right). \tag{4-21}$$

For the harmonics of the orders 5th and 7th, $\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}$ will be nullified since

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = -(h_{\mathrm{s}})\sin(h\omega t) \tag{4-22.a}$$

and

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = (h_{\mathrm{s}})\cos(h\omega t). \tag{4-22.b}$$

For harmonics of the orders 11th and 13th, the positive-sequence harmonic voltage vector will have the same amplitude as of the imposed harmonic signal and will rotate with the same angle. Equation (4-21) for the two harmonics will become

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = U_h e^{\mathrm{j}h_{\mathrm{s}}h\omega t}. \tag{4-23}$$

Since the 5th and 7th harmonics are the most dominant in the power system [54], it is expected that good results will be obtained using the PS-PLL in estimating the grid-voltage phase angle. Moreover, since the operation of the PS-PLL is similar to a LPF operation, the higher harmonics will be attenuated as well.

To investigate the capability of the voltage-harmonics compensation, a parallel RC-load is connected to the grid, through a diode rectifier, upstream of the DG. The phase-voltage at the PCC is shown in Fig. 4.9 before and after the connection of the DG. In addition, the harmonics content is also shown for both voltages in Fig. 4.10. The harmonics are comparatively negligible when connecting the DG, with the PCC-voltage regulation capability. For instance, the 5th harmonic component amplitude has decreased from about 9.5% without the DG to about 3% with the DG. This will result in a voltage that complies with the IEEE-std 1547-2003, which specifies the maximum harmonic voltage distortion as 4% for the harmonics' orders less than the 11th.

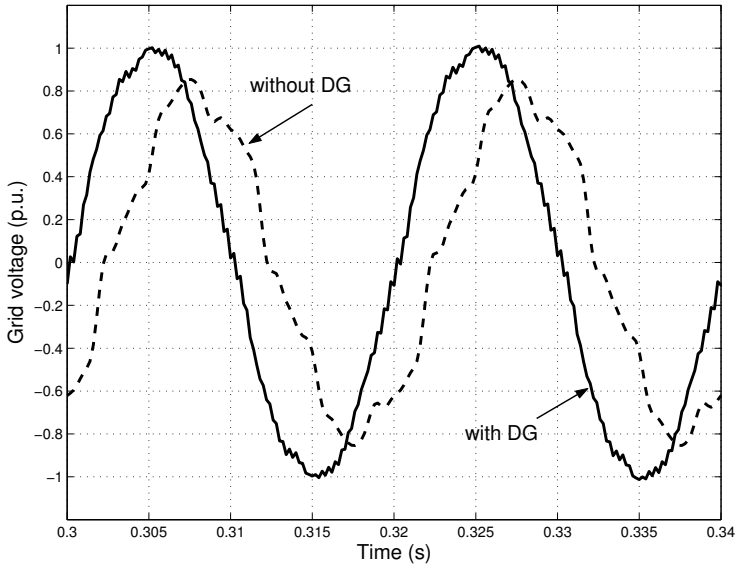

Fig. 4.9 Grid Phase-voltage with (solid) the DG and without (dashed) the DG.

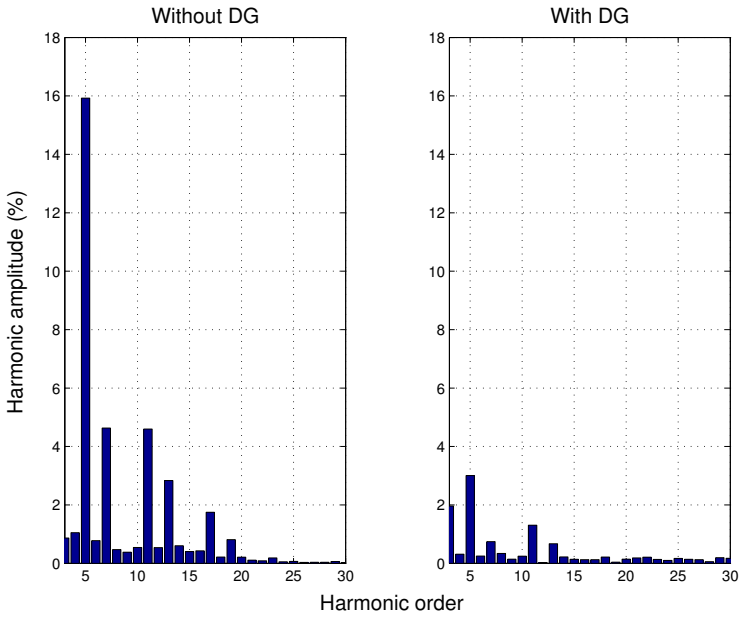

Fig. 4.10 Grid voltage harmonics content with the DG (right) and without the DG (left).

4.6 Compensation for grid-voltage fluctuation

Grid voltage amplitude fluctuations may result due to fast periodically-changing heavy loads that are connected to the grid [58]. If a distribution network is considered, one of the direct effects could be light flicker. The frequency of light flicker ranges between 0.5 Hz and 30 Hz, since this is the range of the human eye sensibility [59]. One way to mitigate this phenomenon is to compensate for the oscillating reactive power using a STATCOM [59] - [60], which is a three-phase VSC based device. The VSC-interfaced DG with the voltage compensation capability is considered here for that purpose.

Proposed PLL modification

The effect of the voltage amplitude modulation on the PS-PLL is first to be examined. For this purpose, a sinusoidal modulating signal is added to the voltage magnitude. With a variable voltage-amplitude, the q-component of the grid voltage will oscillate with the same frequency as the modulating signal. Substituting $h_s = 0$ and $h = 1/5$ (for 10 Hz amplitude modulation) in (4-21), it is obvious that the positive sequence will also be oscillating, producing an error in the estimated phase. To nullify this error and obtain a robust performance, the fundamental component of the grid voltage could be used, instead of the positive sequence component, as input to the Q-PLL. This has been implemented in [61] using two LPFs to extract both the positive-sequence and its fundamental component.

In order to cope with this situation, the adaptive linear neural network extractor (ADALINE) [62] is introduced next. A simple ADALINE consists of one neuron that has a linear input-output relationship, where each input is simply multiplied by a certain weight and all inputs are summed together to produce the output. The power of ADALINE comes from the on-line adaptation of its weights that gives it a non-linear property [62]. For this purpose, the least mean square (LMS) algorithm is used [63].

ADALINE has been implemented in [64] as a combiner to identify the voltage waveform for the classification of the power quality problems. It will

be used here in the same way, however, as an extractor to relieve the fundamental component of the source polluted voltage. The structure of ADALINE is shown in Fig. 4.11, where the discrete input vector $\mathbf{x}(k)$ is composed of sine and cosine elements of all possible frequency components that are contained in the source voltage

$$\mathbf{x}(k) = \left[\sin(\omega k T_s) \quad \cos(\omega k T_s) \quad \ldots \quad \sin(h\omega k T_s) \quad \cos(h\omega k T_s)\right]^T \tag{4-24}$$

where h is the highest harmonic order expected, k is the sampling instant, T_s is the sampling time, and the superscript T indicates the transpose of the vector. This input vector $\mathbf{x}(k)$ is then multiplied by a weight vector $\mathbf{w}(k)$ to produce the ADALINE output $u_{nn}(k)$, as follows

$$\mathbf{w}(k) = \left[w_{11} \quad w_{12} \quad w_{21} \quad w_{22} \quad \ldots \quad w_{h1} \quad w_{h2}\right] \tag{4-25}$$

$$u_{nn}(k) = \mathbf{w}(k) \cdot \mathbf{x}(k) = \sum_{i=1}^{2h} w_i x_i \tag{4-26}$$

where w_i and x_i is the i^{th} element in the vectors $\mathbf{w}$ and $\mathbf{x}$ respectively.

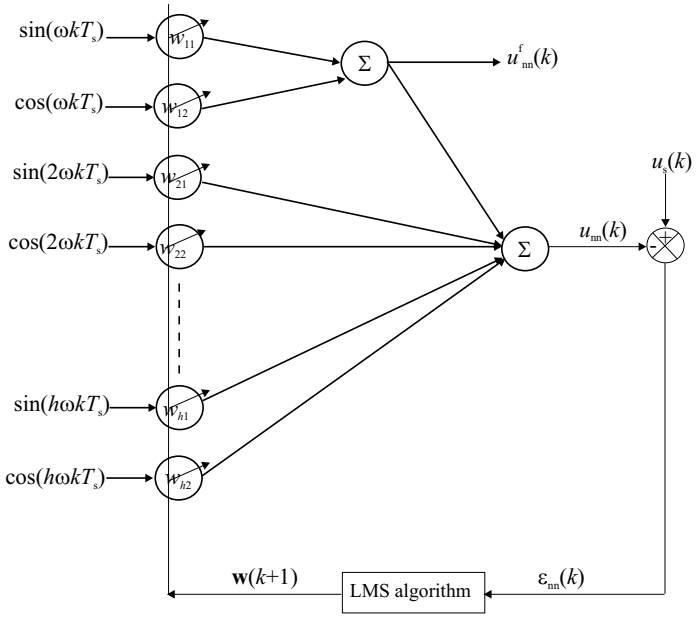

Fig. 4.11 The structure of the adaptive linear extractor (ADALINE).

The output is then compared with the measured and sampled voltage signal $u_s(k)$, where the resulting error ε_{nn} is used by the recursive algorithm to modify the weight vector according to

$$\mathbf{w}(k+1) = \mathbf{w}(k) + \lambda \frac{\mathbf{x}(k)\varepsilon_{nn}(k)}{\mathbf{x}(k)^{\mathrm{T}}\mathbf{x}(k)} \tag{4-27}$$

where λ is the learning factor. The size of λ determines how quickly old data are to be discarded. A small λ means that new data inputs will not have a significant weight and the system becomes less sensitive to disturbances, but also slower in reactions. On the other hand, a large λ makes the system react quickly, but responds more sensitively to disturbances[15].

The block diagram of the PLL implementing ADALINE (NN-PLL) is shown in Fig. 4.12. The three-phase voltage is transformed into the stationary $\alpha\beta$-frame. Then each component is fed into a separate ADALINE algorithm to extract the fundamental component that is fed into a Q-PLL.

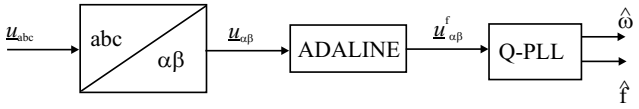

Fig. 4.12 Implementation of NN-PLL.

Performance of the proposed PLL

The performance of the NN-PLL is also compared to the PS-PLL regarding the grid voltage harmonics. The error in the estimated phase angle due to the grid voltage harmonics is shown in Fig. 4.13, using three different bandwidth values for the Q-PLL, for the two estimators. 2% amplitude of the 2nd, 4th, 5th, 7th, 11th and 13th harmonic orders has been superimposed separately on the fundamental grid-voltage. The phase error has been

[15] More discussion about the learning factor can be found in Paper E.

calculated as the peak-to-peak amplitude of the normalized quadrature-voltage.

With the PS-PLL, the error in the estimated phase-angle increases with higher values of the bandwidth. Moreover, the amplitude of the error increases with the increase of the harmonic order, excluding the case for the 5^{th} and 7^{th} harmonics at which it was proven that the error will be nullified. This can be understood by observing (4-17), where the harmonic order is in proportional relationship with the frequency of the oscillations superimposed on the fundamental grid-voltage.

Using the NN-PLL the error is nullified with all harmonic orders and all values of bandwidth, which means that it is robust and in the same time could have better dynamics. Moreover, the case of unbalanced harmonics has been examined with the same order of harmonics as before. Figure 4.14 shows that the NN-PLL is superior to the PS-PLL even when unbalanced 5^{th} and 7^{th} harmonics are present in the grid.

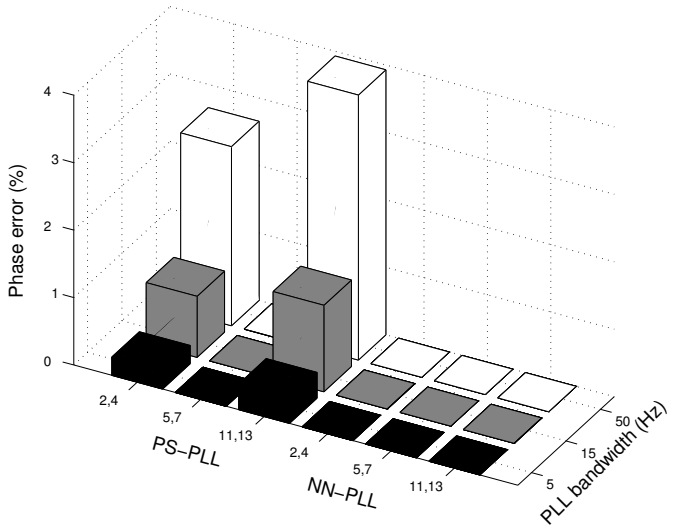

Fig. 4.13 Phase error due to different balanced harmonics using PS-PLL and NN-PLL with different BW values.

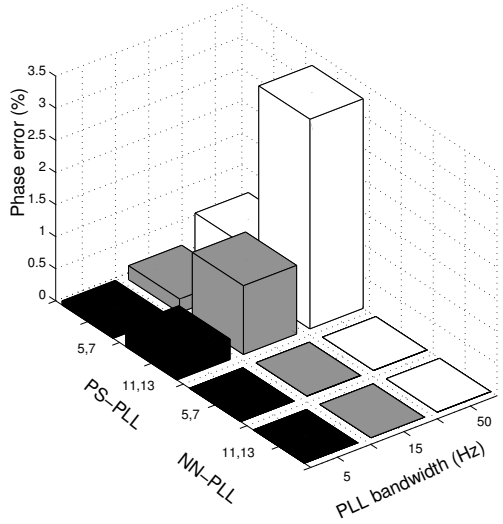

Fig. 4.14 Phase error due to different unbalanced harmonics using PS-PLL and NN-PLL with different BW values.

Mitigation of grid voltage amplitude fluctuation

The mitigation of the grid voltage fluctuation is to be examined. A fluctuating load is assumed to be connected at bus 1, in Fig. 4.4, and is further assumed to be disconnected in case of a fault at the same bus. Its effect is encountered as about 8% amplitude fluctuation of the grid voltage at bus 1 using a cosine modulation signal with a frequency of 10 Hz. In reality this modulation signal could have an infinite number of frequencies, but for the sake of clarity only a 10 Hz component is displayed here, which represents a value in the frequency band (between 2 and 15 Hz [58]) that the human eye is most sensitive to. The PCC-voltage is shown in Fig. 4.15 before the connection of the DG, and with the DG connected with the PS-PLL and the NN-PLL. From the figure, it can be concluded that the ability of the DG with an NN-PLL to mitigate the voltage fluctuation is better. The peak-to-peak voltage-envelope has been oscillating with 8% before the voltage compensation, and with 5% in case of voltage regulation using the PS-PLL and 3.5% in case of using the NN-PLL.

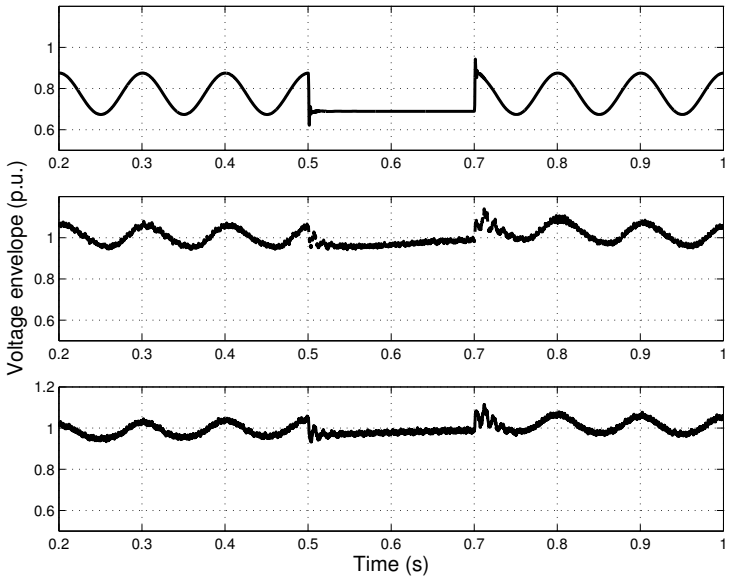

Fig. 4.15 Voltage envelop with DG disconnected (upper), DG with PS-PLL (middle), and DG with NN-PLL (lower).

Moreover, the voltage amplitude variation at the PCC has been tested with different modulation signal frequencies and the result is shown in Fig. 4.16, where the system using the NN-PLL has lower peak-to-peak value of the oscillation of the voltage envelope.

It is worth noting here that the oscillations of the voltage envelope will not be completely nullified since both the active and the reactive powers are oscillating at the grid, because of the modelling that is considered here. That means that both the injected active and reactive powers should be oscillating in order to completely compensate for the voltage fluctuation. However, this is not possible, here, since the application of the converter interfaced DG that is considered implies constant injected active power into the grid. On the other hand, the behaviour of the NN-PLL is dependent on the input-vector length, the order of harmonic frequencies used in that vector, and the initial weights' values. The input-vector length is taken, here, as 18 and the initial weight vector was set to zero. Using different setup for the ADALINE could give different results.

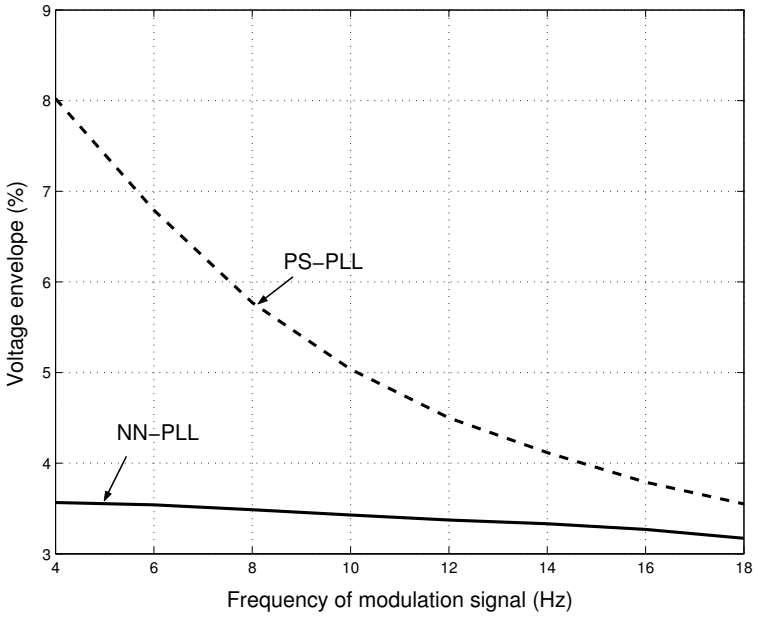

Fig. 4.16 Voltage amplitude variation owing to the change of the modulation signal frequency; with PS-PLL (dashed curve) and NN-PLL (solid curve).

4.7 Conclusions

The possibility to regulate the local voltage using a converter-interfaced DG has been discussed in this chapter. The aim is to maintain the voltage at its nominal value in case of operation in weak grids, and to mitigate the power quality problems at the point of common coupling (PCC). The voltage regulation capability has been investigated by studying the regulation limits regarding the DG injected power and the loading of the grid. The regulation capability is increased if the DG is injecting more active power into the grid and the load is mostly a constant active power load. However, this could require oversizing of the converter valves.

The PCC-voltage regulator sets the reactive current reference in such a way that the reactive power injected into the grid is controlled. The reactive current is represented by the quadrature-component of the measured current,

which is obtained through a coordinate transformation that uses an estimated angle that is obtained using a PLL. The error in the estimated angle could result in an erroneous reactive current command, which could affect the voltage compensation quality. For that purpose, the PLL algorithm has been discussed regarding the grid voltage imbalance, the grid voltage harmonics, and the grid voltage fluctuation. A neural-network based PLL (NN-PLL) has been proposed to extract the fundamental component of the grid voltage, and to estimate its phase angle. This NN-PLL has been compared with a previously investigated PLL algorithm (here referred to as PS-PLL), which estimates the phase angle of the positive-sequence component of the grid voltage. It has been shown that the NN-PLL is more robust against grid voltage harmonics. The NN-PLL has shown superiority also in the special case of unbalanced 5^{th} and 7^{th} harmonics in the grid voltage. In addition, the NN-PLL has proven to be better in case of grid-voltage fluctuation, where in a demonstrated case the oscillation of the voltage envelope has been decreased from 8% (without voltage regulation) to 3.5% (with voltage regulation and using NN-PLL), compared to 5% when using the PS-PLL.

Chapter 5

Intentional Islanding Capability

Intentional islanding refers to the case when the distributed generation (DG) is allowed to work autonomously to energize a part of the grid. For safe operation, detection methods should be applied to change the DG operating mode from grid-connected operation to island operation and vice-versa. Two different detection methods are described and examined in this chapter; namely passive and active methods. Their non-detectable zone is briefly discussed. The operation of the DG in both a strong grid and a weak grid has been examined in case of islanding.

5.1 Intentional islanding definition

Islanding refers to a condition in which a portion of the power system is energized by a local energy source, while it is electrically separated from the rest of the power system [65]. This situation, if not planned, poses a safety hazard to utility repair and maintenance personnel, and could lead to unstable island and instability problems when the utility grid is recovered [66].

Hence, islanding detection is an important aspect in DG applications. DGs should be able to detect the islanding condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, which specifies the acceptable clearing times as shown in Fig. 5.1. Yet, as recommended by the same standard, the detection could lead to an island operation of a DG, which is referred to as intentional islanding.

Besides enhancing the supply reliability for the utility grid [83] (e.g. in rural areas [4]), intentional islanding of DGs represents a required practice for some critical micro-grids [5], [84], [85]. Hence, developing reliable and robust islanding detection methods is of major importance.

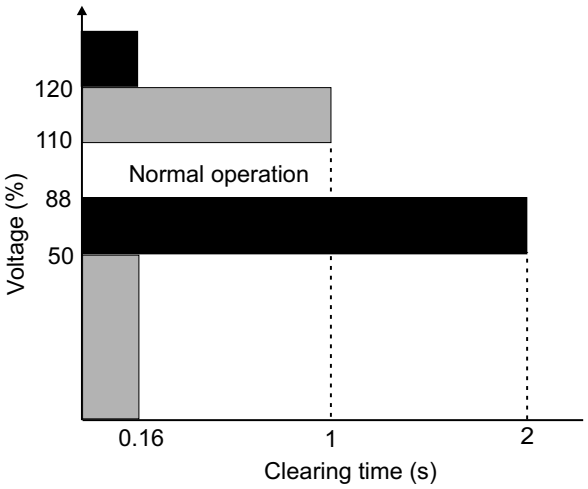

Fig. 5.1 Clearing time for a DG as described in IEEE-std 1547-2003.

5.2 Islanding detection methods

There are two types of islanding detection methods; passive and active. In passive detection algorithms, the sensed grid states (voltage, frequency … etc.) are compared with their nominal values and the deviations are used to decide on the islanding condition. For instance, in [10], the grid outage is detected using the phase angle error, between the grid voltage and the inverter voltage, which is compared to a set value to generate the disconnection signal. Then the DG operates in a stand-alone mode. When the grid is back, the increased currents are used to trip the DG. Then the DG is connected back to the grid after synchronization. Using the voltage phase-angle for islanding detection, however, may lead to false islanding in case of other power system dynamics [68]. Instead, in [40], both the voltage and the frequency are measured at the PCC to detect islanding. However, the effect of a voltage limitation, which could be incorporated in the converter controller for its safe operation, is not considered.

Although they are simple to implement, passive algorithms may fail to detect islanding if the load and generation on the island are closely matched

[67]. The active and reactive power mismatch limits that will lead to this situation are referred to as the non-detectable zone (NDZ) and they are calculated for current-controlled and power controlled DGs in [68] for different passive algorithms using an RLC-resonant load with a certain quality factor. It has been shown, in that reference, that the algorithms that are using the under/over frequency and/or the phase-angle jump are insensitive to active power mismatch. Moreover, the under/over frequency methods are, unlike the phase angle jump methods, dependent on the load quality factor. In addition, there are practical issues related to using phase-angle jump methods. Power system switching events, not resulting in islanding, can falsely trigger such schemes. When the islanding detection is delayed or not activated due to the NDZ, the DG system may lose control on its output terminal voltage, which may lead to island instability. In a way to overcome this problem and to provide seamless transfer between the grid-connected and island modes of operation, the island load (or emergency load) in [46] has been connected in parallel to the capacitor of the LCL-filter. Since the capacitor voltage is always controlled, even in the case of grid-detection failure, the load is not affected by the change of the DG operating mode, or the delay or mal-operation of the detection algorithm. However, this solution might not be feasible for all grids or loads. Another way is to decrease the NDZ by improving the detection method.

In active detection methods, the NDZ is very small [69]. Active techniques are usually incorporated within the controller, where they aim at disturbing the grid states by injecting disturbance signals. In the case of the utility supply outage, the island will be disturbed and the passive detection will succeed. In spite of the small NDZ, active methods may affect the power quality of the distribution system [39]. Moreover, in case of a weak grid system, active methods may lead to false tripping.

Hence, the passive islanding-detection method is considered first since it is the main islanding decision maker. Then, an active islanding detection method is introduced for the operation of the DG in both a strong and a weak grid.

5.3 Passive islanding-detection

A passive islanding detection algorithm has been developed to detect both the grid outage and recovery. To evaluate the grid states that could be reliable enough to be used in the detection algorithm, the grid outage is first considered.

The effect of the grid outage on the PCC-voltage

At the moment of the grid outage, the voltage at the point of common coupling (PCC) will either increase or decrease instantly depending on the sign of the power mismatch (ΔP and ΔQ in Fig. 5.2). The power mismatch represents the amount of power that the grid either delivers or absorbs in the normal operation. This power is equal to the power absorbed by the load at the PCC subtracted from the power injected by the DG, as designated in Fig. 5.2[16]. If the DG injected power is higher than the load absorbed-power, then the PCC-voltage will increase implying increased $u_{\mathrm{d(PCC)}}$. In that case, the increase of the voltage will be limited by the voltage limitation algorithm incorporated in the DG controller. Regarding the algorithm that has been implemented here, $u_{\mathrm{d(PCC)}}$ will be limited to $\frac{u_{\mathrm{dc}}}{\sqrt{2}}$ as has been shown in Section 2.2.

This case is presented in Fig. 5.3, where the grid outage occurs at 0.4 s. The DG controller that has been tested here has the PCC-voltage regulator and the DC-link voltage regulator incorporated. Hence, the *d*-component of the DG injected-current is controlled to be constant to keep the DC-link voltage constant, as shown by the lower plot in Fig. 5.3, while the *q*-component of the current starts to decrease in magnitude after the grid outage to retain the voltage at its nominal value. Since the PCC-voltage amplitude is limited (due to both the limiting algorithm and the operation of the PCC-voltage regulator), this increase in the grid voltage could also correspond to any other dynamics at the grid (e.g. load disconnection), then the over-voltage state cannot be a measure for islanding.

[16] The feeder parameters are given in Appendix C.

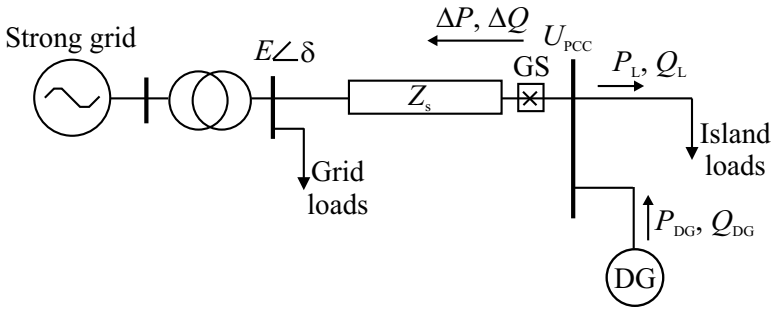

Fig. 5.2 System considered for islanding study.

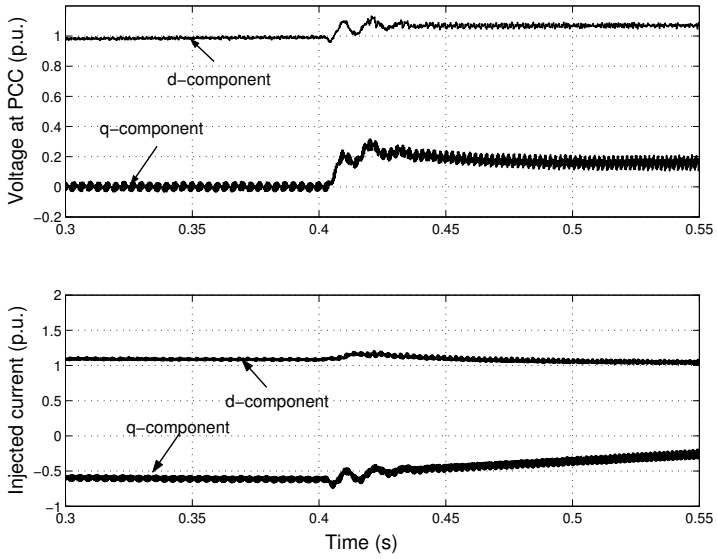

Fig. 5.3 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.4 s and $P_L < P_{DG}$.

If the load absorbed power is higher than the DG injected-power (in which case a load shedding criterion is important for a stable island operation), the PCC voltage will decrease in case of the grid outage. This case is represented in Fig. 5.4, where the grid outage occurs at 0.3 s, and the load active power is higher than the DG active power ($P_L = 1.07P_{DG}$) while the reactive power for both the load and the DG are equal. The DG controller, here, injects constant current into the grid, as shown by the lower

plot in the same figure. Since this decreased voltage could occur also due to voltage dips at the grid, hence the undervoltage is not a reliable state for islanding detection especially if the voltage dips ride-through capability is required. In other words, using the undervoltage state for the islanding detection may lead to false tripping during voltage dips.

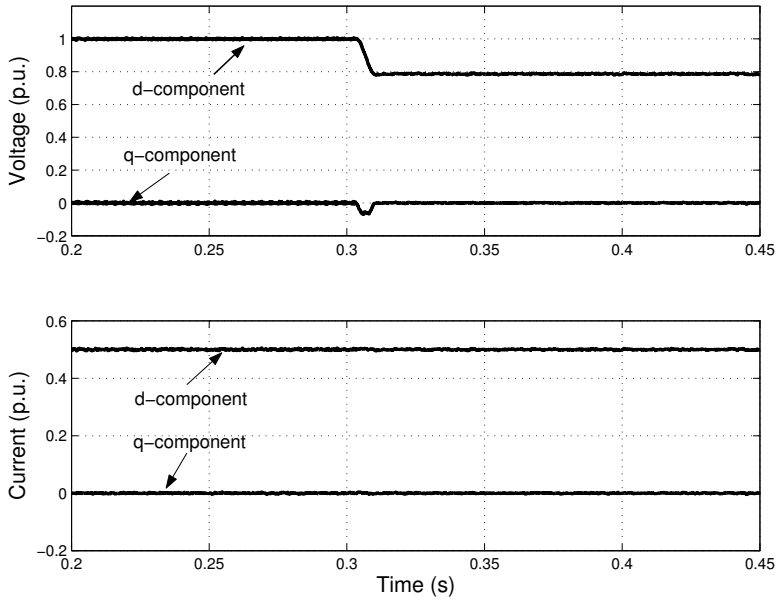

Fig. 5.4 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s and $P_L > P_{DG}$ (ΔP = -0.07 p.u.) and $Q_L = Q_{DG} = 0$.

In conclusion, an overvoltage/undervoltage islanding detection algorithm is not appropriate to be implemented. In addition, measuring other grid states (e.g. the phase angle jump) within a narrow threshold may falsely lead to islanding in case of other grid dynamics (e.g. switching events) [68].

Instead, using the signals generated within the DG controller to detect the islanding condition is considered. A disturbed signal within the controller will lead to a disturbed operation of the DG unit, and hence changing the control mode might be a good practice (even if the utility grid is not

disconnected). For instance, due to the grid outage and the reactive-power mismatch a constant nonzero value of the q-component of the voltage at the PCC will result (e.g. as shown in Fig. 5.3). This will cause an integrator windup of the PLL that in turn will result in a continuous increase (or decrease) in the estimated frequency as shown in Fig. 5.5 for a grid outage at 0.4 s. Hence, the estimated frequency signal is implemented here to detect the grid outage. This is done by assigning a threshold band for the estimated frequency. If the frequency crosses the band for a certain period of time, then the islanding condition is detected. For example, if the detection limit is set to 52 Hz then the islanding conditions are detected within 0.03 s.

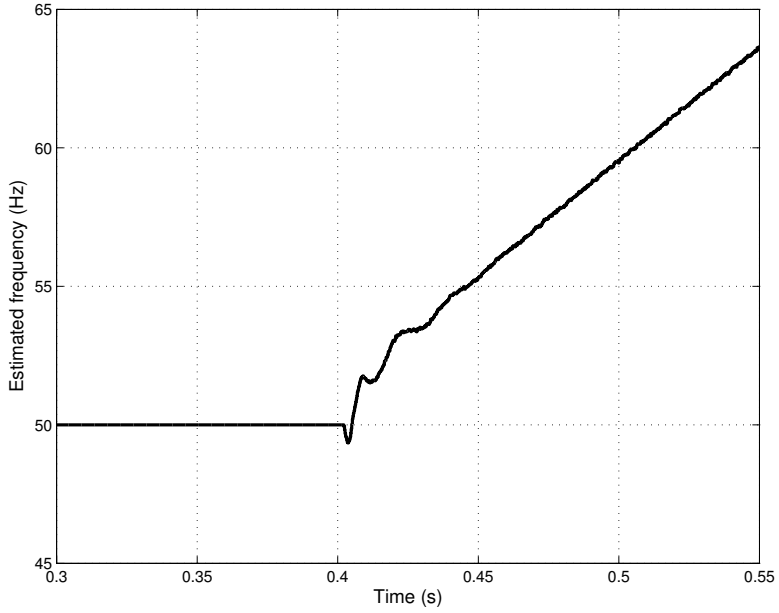

Fig. 5.5 Estimated frequency; grid outage at 0.4 s (P_L<P_{DG}).

To detect the grid recovery, the voltage measurement on the grid side of the grid switch (GS), shown in Fig. 5.2, is needed. If the voltage is back an extra PLL is used for the synchronization between the DG-output voltage and the grid voltage before connecting back the island to the grid.

Passive detection algorithm

The passive detection algorithm, which is implemented here, is shown in Fig. 5.6. Starting from the parallel (or grid-connected) operation, where the DG is aiming at controlling the active and reactive currents injected into the grid, the detection algorithm will be activated to detect the grid outage. The algorithm uses the deviation between the estimated frequency signal, which is produced by the PLL, and the nominal value. A time threshold t_s is also incorporated to avoid false tripping due to load dynamics. This time threshold is set equal to the settling time of the PLL, which could be calculated using the PLL gain as follows

$$t_s = \frac{\ln 50}{k_{pll}} \tag{5-1}$$

where the settling time is defined as the time for the PLL output to settle down to within a tolerance band of 2% of the final value [70], and k_{pll} is the proportional gain of the PLL.

Once the islanding condition is detected, the DG starts an island operation mode where its aim is to hold the voltage and frequency at their nominal values as well as to adjust the injected active and reactive powers to support the island loads. In addition, the GS is used to disconnect the utility grid from the island for safety operation. A DC chopper is also needed to consume the extra power that could be coming from the primary energy source in a way to adjust the input power to match the load needs. Moreover, in this mode, the grid recovery detection is activated where the voltage on the grid side is sensed. Once the utility grid is recovered, the synchronization between the DG voltage and grid voltage is carried out using an extra PLL on the grid side. The connection to the grid is then done by enabling the GS and disabling the DC chopper.

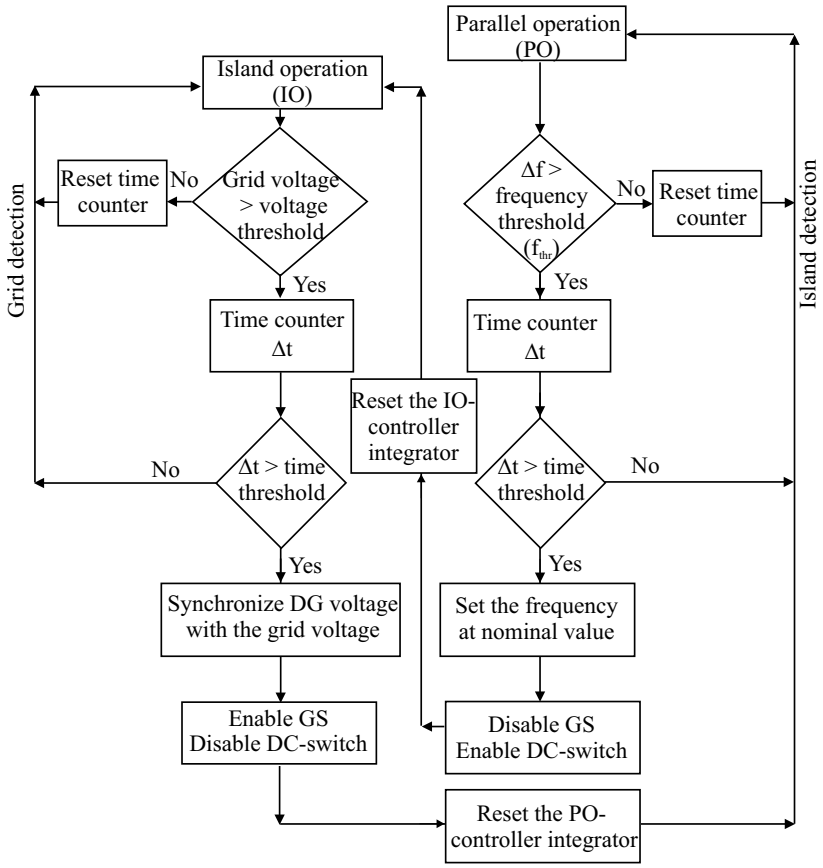

Fig. 5.6 Passive detection algorithm.

5.4 Non-detectable zone for passive detection

The non-detectable zone (NDZ) is usually described by the limits of active and reactive power mismatch (ΔP and ΔQ in Fig. 5.2) in which the detection algorithm would fail to recognize the grid outage [68]. These limits are related to the load characteristics, the detection method, and the controller of the DG.

The above described passive detection algorithm suffers from an open limit for ΔP in the NDZ. In other words, if the load reactive power exactly

matches the DG-injected reactive power, then, in case of the grid outage, the *q*-component of the PCC-voltage will not change irrespective of the amount of ΔP. This leads to undetectable islanding whatever the load active power is.

This case has been shown in Fig. 5.4, for $P_L > P_{DG}$ and constant active and reactive powers that are injected by the DG. Incorporating a PCC-voltage regulator within the DG controller, the change in the *d*-component of the PCC-voltage will lead to a change in the injected DG reactive current. Since the PCC-voltage will keep its decreased (or increased) value, due to the grid outage, the injected reactive current will keep a constant value (in case the DG is operating towards a strong grid) that will produce a reactive power mismatch and a change in the *q*-component of the PCC-voltage. This case is represented in Fig. 5.7, for the same loading condition as in Fig. 5.4. With the change in the *q*-component, an integrator windup in the PLL will result. Hence, the estimated frequency, shown in Fig. 5.8, will drop instantly leading to successful islanding-detection. As an example a frequency threshold of 48 Hz is detected within 0.01 s. This will lead to the decrease of the NDZ since either the active or reactive power mismatches will lead to a successful islanding detection.

In conclusion, combining the passive islanding-detection with the PCC-voltage regulator, described in Section 4.4, results in decreased NDZ. However, a complete match between the load and the DG unit active and reactive powers ($\Delta P = \Delta Q = 0$) would not be detected, since neither the *d*-component nor the *q*-component of the PCC-voltage would be affected by the grid outage. In this case, an active detection algorithm that injects a disturbance signal would be beneficial especially in case of a strong grid.

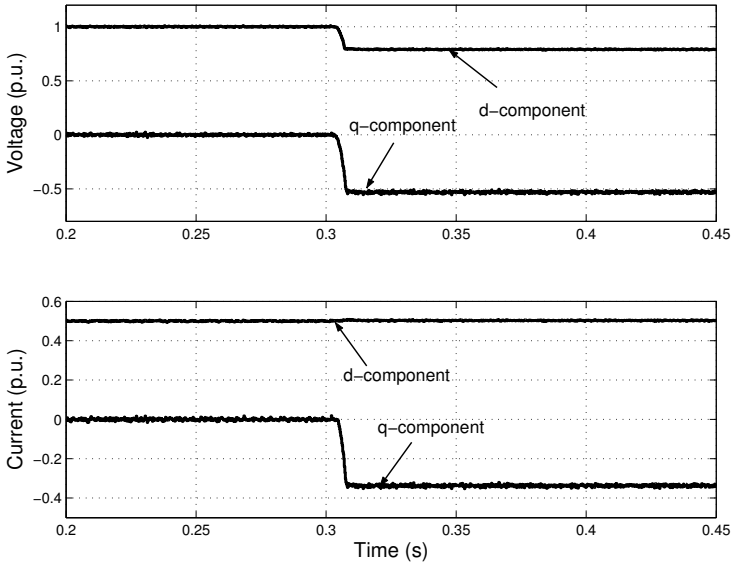

Fig. 5.7 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s; current-controlled DG with voltage regulation capability, and $P_L > P_{DG}$ ($\Delta P = -$ 0.07 p.u.).

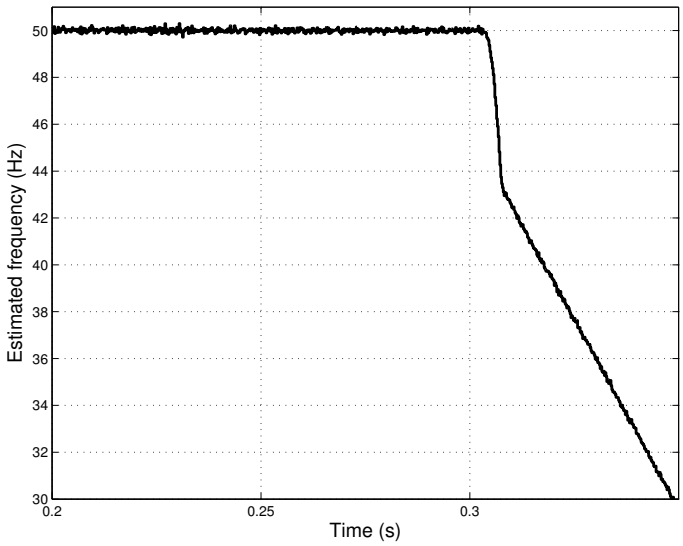

Fig. 5.8 Estimated frequency; grid outage at 0.3 s and current-controlled DG with voltage compensation capability, and ($\Delta P = -$ 0.07 p.u.).

5.5 Active Detection

The idea of the active detection is to try to disturb the grid in such a way that the passive detection will succeed to operate in the NDZ [69]. In a way to implement that, the active frequency drift method has been used in [79] and [43]. In this method, the waveform of the injected current is slightly distorted such that when islanding occurs the frequency of the phase voltage will drift up or down. Islanding is done in [43] by incorporating a washout function in the PLL that determines the change in the frequency and adds it to the frequency reference. Instead, in [39] a band pass filter is used, with the *d*-component voltage as an input, to deviate the voltage from its nominal value by changing the switching duty cycles.

In a way to optimize the design of the DG controller, the active detection is implemented here, using the PCC-voltage regulator. In case of a strong grid, the reference voltage signal in the PCC-voltage regulator is set to a value that is less than 1 p.u., while in case of a weak grid the reference voltage is set to 1 p.u.

The PCC-voltage regulator that is devoted for the operation in a strong grid is shown in Fig. 5.9. It operates in a way to produce a reactive current command i_q^* in such a way to force the voltage to deviate from its nominal value. The reference signal e_{dset} is set to a value that, when compared to the PCC-voltage e_d, produces an injected current within the maximum current limit of the DG. The limiter in the figure resets the integral part of the PI controller so that the current reference changes in a narrow band in order to decrease the current harmonics injected to the grid.

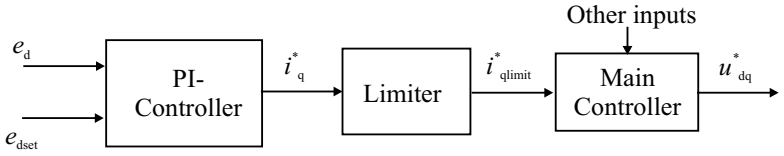

Fig. 5.9 Active islanding detection (PCC-voltage regulator).

The effect of adding the active islanding detection using the PCC-voltage controller is examined using a load that completely matches the DG power input (i.e. $\Delta P = \Delta Q = 0$). The DG injected active (*d*-component) and reactive (*q*-component) currents are shown in Fig. 5.10, without incorporating the active detection part (in the upper plot) and with incorporating it (in the lower plot), for a grid outage from 0.3 s to 0.4 s. From the figure, the increased value of the injected reactive current, in case of incorporating the active detection controller, implies producing a reactive power mismatch, in the normal operation, that in turn results in an islanding signal from the passive detection algorithm in case of grid outage.

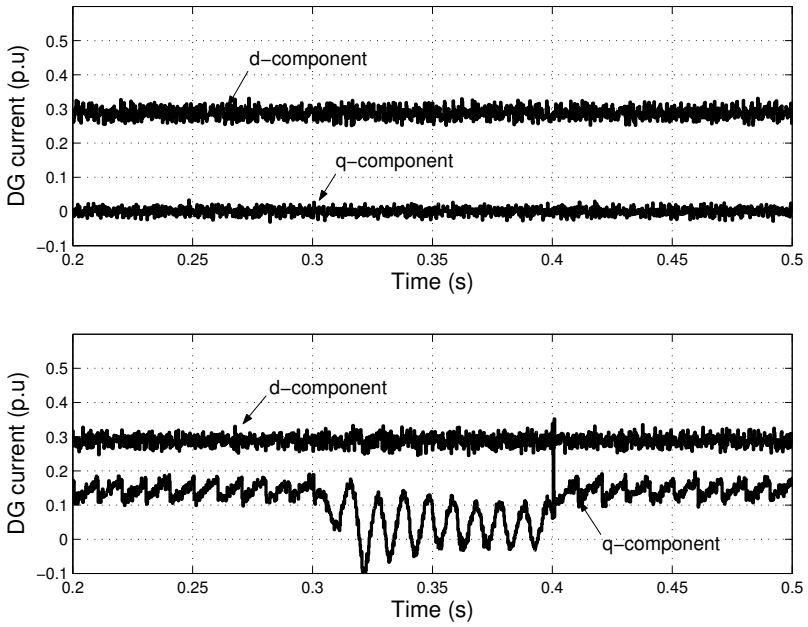

Fig. 5.10 DG injected active (d-component) and reactive (q-component) currents; without active detection controller (upper) and with active detection controller (lower) with a matching load.

The effect of using the active detection controller (i.e. the PCC-voltage controller) is also examined in case of a weak grid using a quadratic voltage dependent load that produces active power mismatch (ΔP) of 0.15 p.u. and

zero reactive power mismatch (ΔQ = 0) at the normal operation. A grid outage at 0.8 s is encountered. As shown in Fig. 5.11 (a) by the dashed line, the estimated frequency has a constant increase after 0.8 s, with the PCC-voltage regulator deactivated, due to a small change in the reactive power of the load that is in turn resulting from the increase of the PCC voltage, as shown in Fig. 5.11 (c). This increase in the estimated frequency could be relatively small and, depending on the frequency threshold set in the passive detection algorithm, it might not successfully detect the islanding condition. By activating the PCC-voltage regulator, the estimated frequency will continue to increase, as shown in Fig. 5.11 (a) by the solid line, after the grid outage at 0.8 s, due to the continuous increase in the DG injected reactive current that is shown in Fig. 5.11 (b), implying the successful detection of the islanding condition.

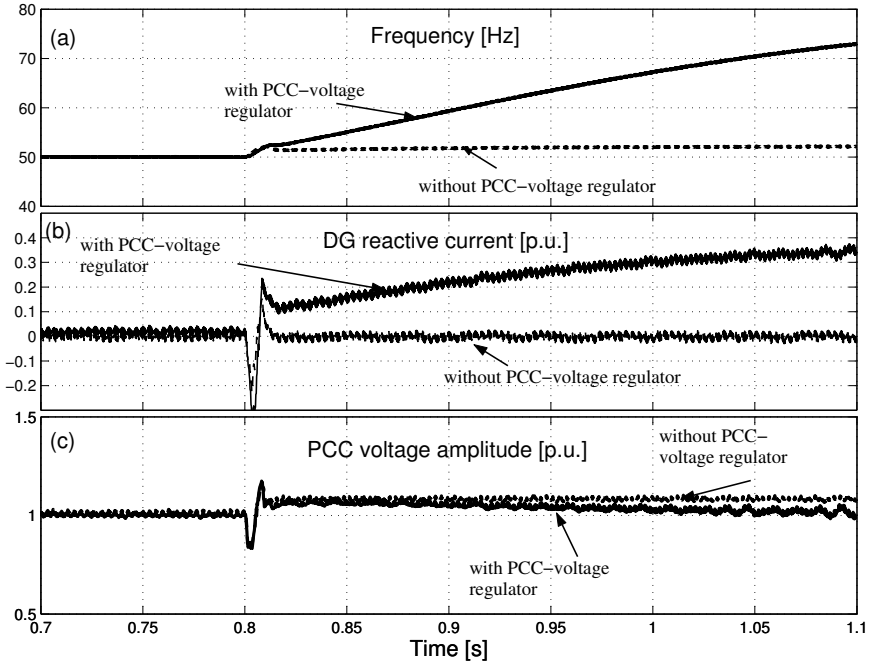

Fig. 5.11 Grid outage at 0.8 s, for ΔP = 0.15 and ΔQ = 0, with and without the PCC-voltage regulator. (a) the estimated frequency. (b) The DG injected reactive current. (c) The PCC-voltage amplitude.

The active detection method, using both the passive detection algorithm and the PCC-voltage regulator, are now to be examined.

5.6 Intentional islanding in a strong grid

A strong grid system is referring to a power system where the voltage and frequency at the load bus are kept constant, by the utility, regardless of the load dynamics. The system shown in Fig. 5.2 is considered where the PCC-voltage amplitude is kept constant at 1 p.u. during normal operation. The DG system is assumed to have an L-filter to smoothen out the current harmonics, and the DC-side is assumed to be controlled from the DG energy-source side for simplicity.

The DG controller will work on either one of the two operations; current-controlled or voltage-controlled, depending on the state of the utility grid as shown in Fig. 5.12.

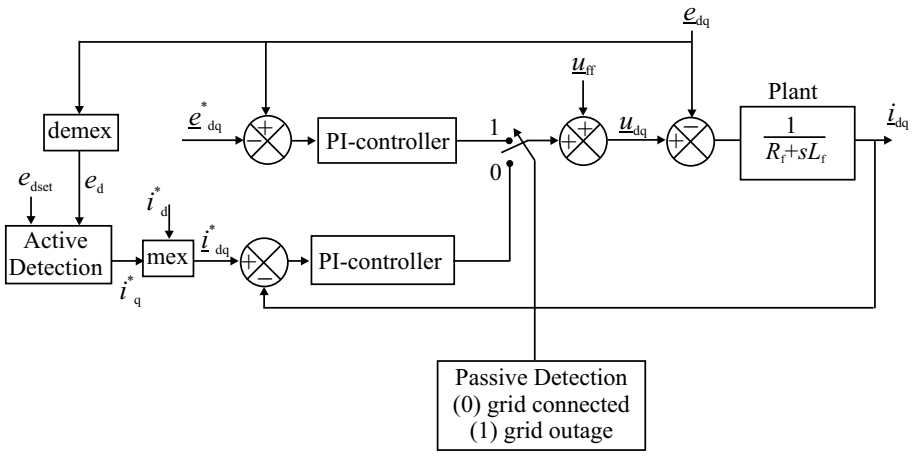

Fig. 5.12 Control transition between grid-connected and island modes.

The grid state is detected using the passive detection algorithm, shown in Fig. 5.6. In case of the grid outage, the detection algorithm will set the controller on the voltage control mode. In this mode the voltage nominal value is set as reference and compared with the measured voltage signal using a PI-controller. The output of this controller is added to the

feedforward voltage vector $\underline{u}_{ff}$. When the grid recovery occurs, the current controller will be activated. Moreover, the active detection is also incorporated in the controller in order to minimize the non-detectable zone as discussed before.

The island loads are set to draw higher power than the DG injected power, as described before for the case related to Fig. 5.4, to test the islanding detection and operation. It is assumed in this case that the energy source of the DG can inject more power to match the load in case of the occurrence of islanding (otherwise a load shedding criterion should be implemented). A grid outage has been encountered at 0.4 s, and the recovery of the grid occurred at 0.6 s. The controller has detected the outage and a transition to the voltage control mode has been performed, where the voltage has been set to 1 p.u., as shown in Fig. 5.13.

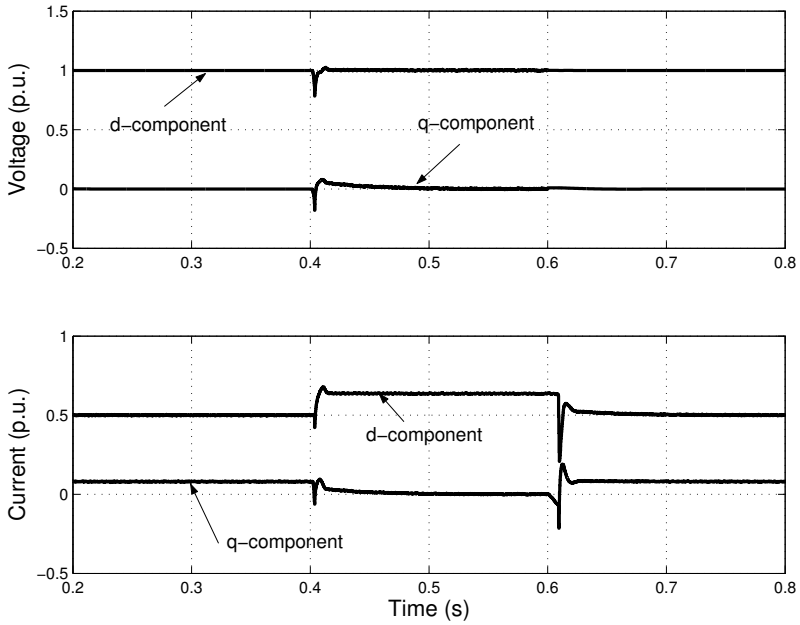

Fig. 5.13 PCC-voltage (upper), and DG injected currents (lower) in case of grid outage from 0.4 s to 0.6 s.

Before islanding, the *d*-component current has been set to 0.5 p.u., as shown by the lower trace of the same figure, while the *q*-component current i_q has been adjusted by the active detection controller to reduce the PCC-voltage *d*-component to 0.95 p.u. (i.e. e_{dset} = 0.95 p.u.). At the grid outage (at 0.4 s), i_q will start to change in a way to put the PCC-voltage amplitude to e_{dset}. However, this will change also the *q*-component of the voltage, which in turn will affect the estimated frequency as shown in Fig. 5.14 by the upper plot. This will lead to the setting of the passive detection signal, as shown in the same figure by the lower plot. Hence, the grid outage is detected and the grid switch GS is disconnected.

During the island operation, the DG injected currents will be set to match the load requirements. Moreover, the voltage angle is set to the reference value. When the grid is back, the voltage on the grid side of the GS will be sensed, and an extra PLL is used to synchronize the island back to the grid, then the GS is connected.

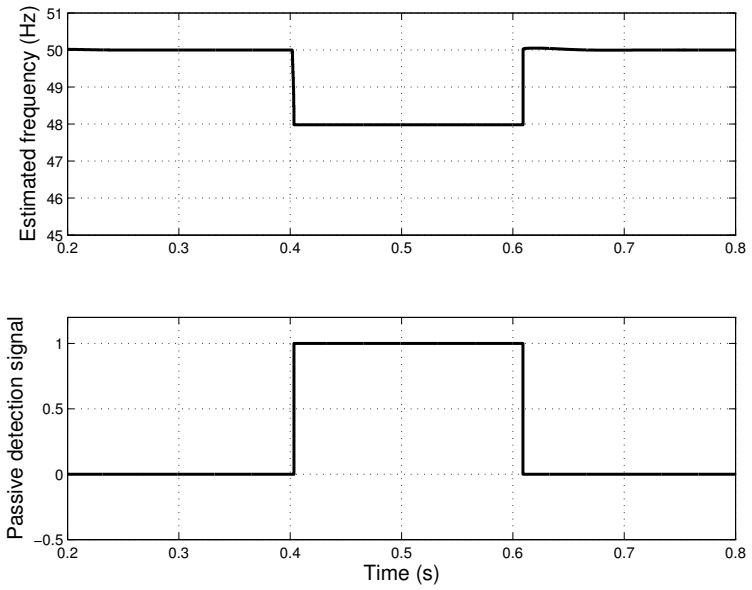

Fig. 5.14 Estimated frequency (upper), and passive detection signal (lower) in case of grid outage from 0.4 s to 0.6 s.

5.7 Intentional islanding in a weak grid

A weak grid system is referring, here, to systems where the voltage level at the load bus is not constant and is affected by the load dynamics. The system in Fig. 5.2 will be considered, where the voltage at the PCC is affected by the feeder voltage drop and the load dynamics. The island-loads are set such that their consumed power is lower than the DG-injected power. They are implemented as an aggregated quadratic voltage-dependent load, with a nominal active power mismatch (ΔP) of 0.55 p.u. and reactive power mismatch (ΔQ) of 0.2 p.u.

As has been discussed in the previous chapter, the voltage regulation capability of the DG is advantageous in the operation of weak grids since it will maintain the PCC voltage at the nominal value regardless of the load dynamics. Another advantage is highlighted here regarding the islanding. With the voltage regulation capability, the islanding non-detectable zone is reduced. This is especially important in the application of weak grids, since the active detection methods, which aim at disturbing the grid states, are not adequate for such grids since, during normal operation, the weak grid states (as opposite to strong grids) are changeable.

The DG system is considered here with the VSC as a front end and an LCL-filter to damp the line current harmonics. The grid-connected controller for this system has been described before in Section 2.6. The island-operation controller is shown in Fig. 5.15[17], where the voltage reference and the phase angle reference are set to their nominal values. A DC-link chopper is incorporated to dissipate the extra power that would come from the DG energy-source, in order to adjust the DG injected-power to match the load requirements.

The PCC-voltage is shown in Fig. 5.16, in the upper plot, for the operation of the DG before, during, and after islanding. The grid is disconnected at 0.3 s and recovered at 0.5 s.

[17] This controller has been explained in more details in Paper F.

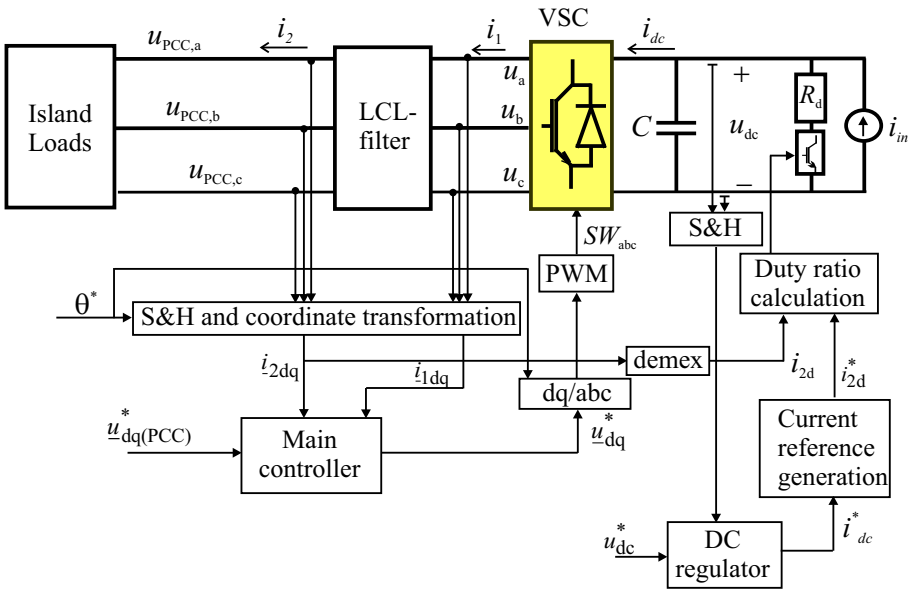

Fig. 5.15 Island operation controller for DG with LCL line filter.

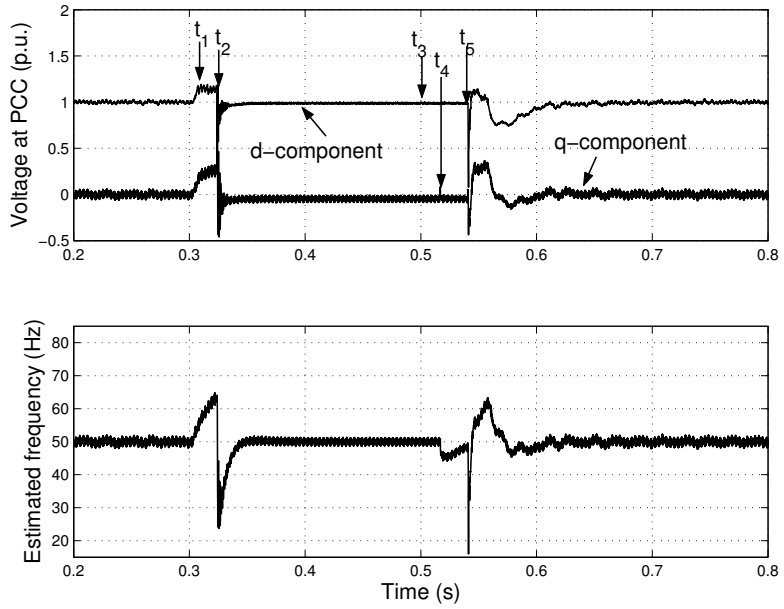

Fig. 5.16 Voltage in *dq*-frame at the PCC (upper) and estimated frequency (lower) for grid outage at 0.3 s and recovery at 0.5 s.

When the grid outage occurs at 0.3 s, the PCC voltage starts to increase in magnitude. When the *d*-component of the PCC-voltage $u_{d(PCC)}$ reaches the voltage limit, that is set by the controller, at t_1, the constant-limited value is maintained (until t_2). The frequency, which is shown by the lower plot of the same figure, will continue to increase after t_1, due to the constant value of the voltage *q*-component, until the island is detected at t_2. The detection algorithm will start to react after reaching the time threshold t_s, when the detection signal is activated (at t_2), resulting in transferring the controller from grid-connected mode to island-operation mode. At t_2 the frequency will be reset to its nominal value, and the DG injected powers, which are shown by the upper plot in Fig. 5.17, will start to adjust to match the load requirements. In consequence, the injected currents will decrease in magnitude, as shown in Fig. 5.18. Moreover, the DC-link voltage, which is shown in Fig. 5.17 by the lower plot, will maintain its nominal value in spite of the decreased injected DG-active power to the grid, since the DC chopper switch has been activated to dissipate the extra power in the chopper.

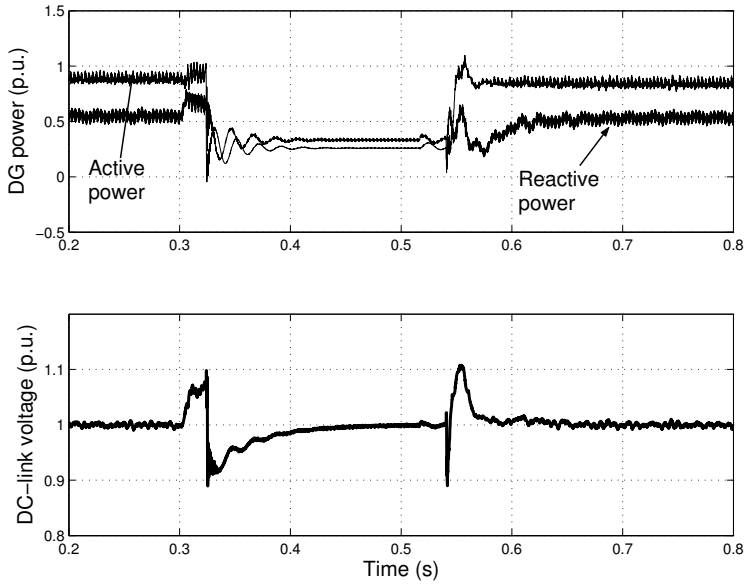

Fig. 5.17 DG injected power (upper) and DC-link voltage (lower) for grid outage at 0.3 s and recovery at 0.5 s.

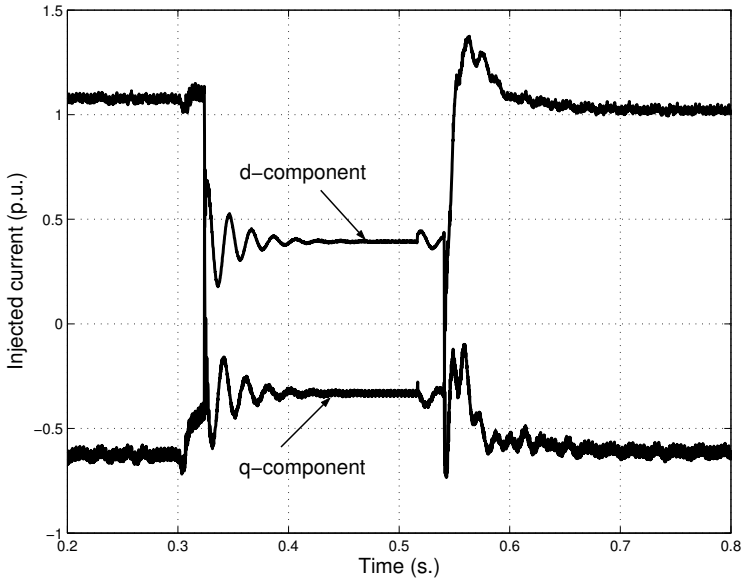

Fig. 5.18 DG injected current in dq-frame; grid outage at 0.3 s and recovery at 0.5 s.

When the grid voltage is recovered at t_3, a time threshold is also encountered before the synchronization of the grid voltage and DG voltage starts at t_4. This is done by using an extra PLL that is implemented for the voltage before the grid switch (GS in Fig. 5.2) from the utility grid side. At t_4, the phase angle of the DG voltage is set equal to the phase angle of the grid voltage. This could be seen from the change of the frequency signal in Fig. 5.16. After about one cycle of the fundamental frequency, the island is connected back to the utility grid at t_5. The DC-chopper is left in operation to buck the over-voltage that could occur at the starting of the grid-connected controller mode, until the PCC-voltage is stabilized.

At the starting of the grid-connected operation, $u_{d(PCC)}$ will drop to a value that represents its normal amplitude in case of deactivating the voltage regulator of the DG. This is mainly due to the PCC-voltage regulator transient time, which has been set long enough to stabilize the overall DG controller. In spite of the decreased value of the voltage during this time, the duration is very small compared with the clearing times that are shown in Fig. 5.1. After the transient time of the PCC-voltage regulator, the PCC-

voltage amplitude will be regained to the nominal value. In addition, the DG injected powers and currents will regain the values that are set for the grid connected operating mode.

5.8 Islanding detection reliability

Voltage dips appearing at the PCC, due to remote faults or motor starts, may lead to false tripping of the DG. The reason is that for small voltage dip amplitudes, the PCC voltage regulator may become unstable resulting in a disturbed PCC voltage that in turn will result in islanding. For instance, referring to Fig. 4.6 with a DG injected active power of 0.8 p.u. and a voltage dip magnitude of 0.7 p.u., the voltage regulator will become unstable and islanding will be detected for this case. Decreasing the DG input power would result in improving the voltage dip ride-through capability (as has been discussed in Chapter 3) and the reliability of the islanding detection.

Moreover, the effect of limiting the VSC current on the estimated frequency in case of voltage dips at the grid with induction motor loads at the PCC has been discussed in [81]. For sufficiently high current limit, the controller is able to maintain the voltage and frequency at the PCC at their nominal values. That would imply robust islanding detection.

The effect of setting a reactive current limit on the robustness of the islanding detection has been, also, discussed in Paper G, where the island loads have been implemented as an induction machine load. By setting the proper current limit, the DG unit can have the ability to ride-through voltage dips with magnitudes above a certain limit, which can be set according to the grid codes, and detect islanding for voltage dips with magnitudes lower than that limit.

5.9 Conclusions

In this chapter, the possibility of intentional islanding has been discussed. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection method should be applied. The islanding detection technique should be able to differentiate between grid dynamics and the islanding condition, and to provide the correct detection signal irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch. The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC). The NDZ, for the converter-interfaced DGs, also depends on the control method.

Two islanding methods have been introduced here; namely passive and active. An active islanding detection method has been proposed to minimize the inherent NDZ of the passive technique. In this method, the estimated frequency signal has been used to detect islanding along with the PCC-voltage regulator. This detection method is motivated by the operation of the DG in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the same method can be used by changing the reference value of the PCC-voltage regulator so as to produce a disturbing current signal in the grid.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The main focus of the thesis has been put on the study of the interface requirements and capabilities of a DG with a voltage source converter (VSC) as a front end. Two line filters have been considered at the connection point of the DG; namely an inductance line filter (L-filter) and an inductance-capacitance-inductance line filter (LCL-filter).

Vector current controller (VCC)

In the first place, **vector current controllers (VCC)** have been implemented, in the rotating synchronous *dq*-frame, for both systems. The time delay, with one sample length, that results due to the calculation time has been compensated for using a Smith predictor, which predicts the grid currents one sample ahead. In addition, the controller saturation, which could result due to high current steps, has been avoided using a voltage limiting algorithm. Besides, to avoid integrator windup, which also could result due to high current steps, the limited voltage has been used in the Smith predictor to recalculate the currents. A DC-link voltage regulator has been also incorporated in the controller to protect the capacitor on the DC-side during different load changes. Moreover, a dual vector current controller (DVCC) has been implemented, which comprises two VCCs. One of them is described in the positive rotating *dq*-frame and the other is described in the negative rotating *dq*-frame, to improve the performance in the case of unbalanced grid-voltage. Moreover, convenient current reference equations have been derived based on the power balance between the DC-side and the

AC-side of the VSC. The controllers have shown good current reference tracking even when high current steps are applied. In addition, in case of unbalanced grid-voltage, oscillating powers will be produced. When those powers are forced to be supplied from the grid side, it has been also shown that the DC-link voltage oscillations are negligible.

Voltage dips ride-through capability

Furthermore, the current-controlled converter interfaced DG has been studied in relation to different grid interface issues. First the **voltage dips ride through capability** has been discussed. For that purpose, a previously investigated voltage dips classification has been adopted to study the effect of all the possible voltage dips that could appear at the DG terminals. In addition, that classification has been modified to be implemented in the positive and negative sequence *dq*-frames. The equations of the maximum currents that would flow through the VSC valves due to all possible voltage dips have been derived. It has been shown that these analytical expressions give almost the same maximum current values as the numerical calculations based on simulation. It has been shown that if the converter-interfaced DG should ride-through the dip period there are two alternatives. One is to oversize the converter switches to withstand the increased currents. The other is to decrease the power input from the source during the dip period, so that the currents will be decreased. However, the latter would require that the input power to the DC-link be reduced very quickly, which could be an issue regarding the energy source or the control of an energy storage connected to the DC-link.

Voltage regulation capability

Thereafter, the **voltage regulation capability** has been discussed. This capability is beneficial if the compensation for the grid voltage quality problems is required. With this capability, the compensation of voltage dips, voltage harmonics, voltage amplitude modulation … etc. would be possible resulting in better power quality at the grid. Moreover, if the DG is working towards a weak grid, where the voltage level is dependable on the load

dynamics, this capability will help in maintaining the voltage level at its nominal value. However, an important issue is the voltage regulation limits, at which the voltage regulator is stable. These limits were discussed and are related to the loading at the grid. It has been shown that, the more input power coming from the DG source, the more reactive power is available to compensate for the voltage. However, in case of increased active and reactive powers, the current limit could be reached. Hence, the compensation capability is limited by the maximum current that the VSC would stand. Another limit is presented by the load that is connected at the same connection point as the DG. If the load has a low power factor, it means that more injected reactive power is needed to regulate the voltage. This in turn would increase the injected current. Another issue that could affect the voltage regulation capability is the voltage phase-angle extraction.

It has been shown that using a PLL that implements the fundamental component of the grid voltage a smaller error in the estimated phase angle would be produced and hence resulting in better grid voltage regulation. A neural-networks based PLL has (NN-PLL) been introduced for that purpose. The NN-PLL has been compared with a previously investigated PLL that extracts the angle of the positive sequence voltage, which is referred to here as PS-PLL. The NN-PLL has performed superior compared to the conventional PLL when the grid voltage harmonics are significant, and the case of grid voltage amplitude modulation.

Intentional islanding capability

Finally, the **intentional islanding capability** has been studied. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection algorithm should be applied. The islanding detection technique should be able to differentiate between grid dynamics and islanding condition, so that a correct detection signal is provided, irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch at which the detection algorithm will malfunction.

The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC).

Two islanding techniques have been examined here; namely passive and active techniques. In the passive technique, the estimated frequency signal in combination with the PCC-voltage regulator has been used to detect islanding with a minimum NDZ. That could be a beneficial application in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the active technique has shown to be beneficial. In this technique, which incorporates also the passive algorithm using the estimated frequency, a reactive current reference is set in order to change the voltage at the PCC. If the voltage changes, it will result in the detection of the island. The two islanding-detection methods have been examined for the operation of a converter-interfaced DG that is working together with both a strong grid and a weak grid. The islanding-detection technique has successfully detected the island in case of islanding condition, while it did not react during a voltage dip at the grid.

6.2 Future work

The grid interconnection capability of a converter-interfaced DG has been studied here regarding the front end converter only. The study of the whole DG system and its effect on the interface capabilities is an interesting topic and could result in setting preferable topologies for the optimal operation. For instance, the capability of voltage dips ride through has been related to the DG source input power. If this input power could be changed in a very short time, then the ride through capability could be provided without oversizing the front end converter. Moreover, providing controllable storage at the DC-link could help in storing the extra power during island operation. That could result in supporting the island for longer time duration and the stored power could be used during voltage dips to ride through the dip period.

Another interesting research point is the study of the parallel operation of converter interfaced DGs regarding the voltage regulation capability and

islanding. The parallel operation could be already motivated from the energy resource point of view. For instance the aggregated DG systems are common for wind energy applications. Using several DGs at the same connection point could increase the voltage regulation capability and provide better support in case of islanding. The design of a central controller, however, is an important issue. The controller should be designed to provide control coordination between different DG units with possibly different control aims. Sliding mode control approach could be implemented for the control of parallel converter-interfaced DGs that are operating in close proximity [72]. This control technique is based on variable structure systems (VSS), which are defined as systems where the circuit topology is intentionally changed following certain rules to improve the system behaviour in terms of speed of response, stability and robustness [12]. Hence, the operational idea of this controller could be to change the physical structure of the connected DGs to meet the physical or electrical changes on the grid.

Furthermore, since the grid outage detection algorithm plays an important role in providing a stable island by setting the DG controller into the required function, it is of great importance to develop a reliable detection algorithm. An algorithm with a negligible non-detectable zone (NDZ) implies a successful grid outage detection regardless of the loading condition of the grid or the injected power of the DG. Active islanding has been previously introduced to provide such a reliable detection. However, the equipment of active islanding can have a drawback of polluting the grid. Besides, the equipment cannot be implemented in the case of a weak grid, where the grid states are changeable even during normal operation. The use of smart sensors could present another possible and reliable way in the grid outage detection. A smart or wireless sensor is comprised of a sensor, a processor, and wireless communication all on a single chip owing to the recent advances in micro-electro-mechanical systems (MEMS) technology [73], [74]. Smart sensors could be implemented for the coordination between the controllers for islanding detection through the interaction with the protection system or the grid operator. In addition, smart sensors could be

implemented for the coordination between the controllers for parallel operating DGs.

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Appendix A
Transformations for three-phase systems

A.1 Transformation of three-phase quantities into vectors

A three-phase positive system constituted by the three quantities $x_1(t)$, $x_2(t)$ and $x_3(t)$ can be transformed into a vector in a complex reference frame, usually called $\alpha\beta$-frame, by applying the transformation defined by

$$\underline{x} = x_\alpha(t) + \mathrm{j}x_\beta(t) = \frac{2}{3}K\left[x_1(t) + x_2(t)\cdot \mathrm{e}^{\mathrm{j}\frac{2}{3}\pi} + x_3(t)\cdot \mathrm{e}^{\mathrm{j}\frac{4}{3}\pi}\right] \tag{A.1}$$

where the factor K is usually taken equal to $\sqrt{\frac{3}{2}}$ for ensuring power invariance between the two systems. Equation (A.1) can be expressed as a matrix equation:

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = \mathbf{C_{23}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.2}$$

where

$$\mathbf{C_{23}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.3}$$

The inverse transformation is given by:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{32}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \tag{A.4}$$

where

$$\mathbf{C_{32}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.5}$$

This holds under the assumption that the sum of the three quantities is zero. Otherwise, there will also be a constant (zero-sequence) component. In the latter case, (A.2) and (A.4) become

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} = \mathbf{C_{230}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.6}$$

and for the inverse transformation

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{320}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} \tag{A.7}$$

with the two matrixes given by

$$\mathbf{C_{230}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} \end{bmatrix} \tag{A.8}$$

and

$$\mathbf{C_{320}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \end{bmatrix}. \tag{A.9}$$

A.2 Transformation from fixed to rotating coordinate system

Let the vectors $\underline{v}(t)$ and $\underline{w}(t)$ rotate in the $\alpha\beta$-frame with the angular frequency $\omega(t)$ in the positive (counter-clockwise) direction. If the vector $\underline{w}(t)$ is taken as the *d*-axis of a *dq*-frame that rotates in the same direction with the same angular frequency $\omega(t)$, both vectors $\underline{v}(t)$ and $\underline{w}(t)$ will appear as fixed vectors in that frame. The components of $\underline{v}(t)$ in the *dq*-frame are thus given by the projections of the vector on the direction of $\underline{w}(t)$ and on the orthogonal direction, as illustrated in Fig. A.1.

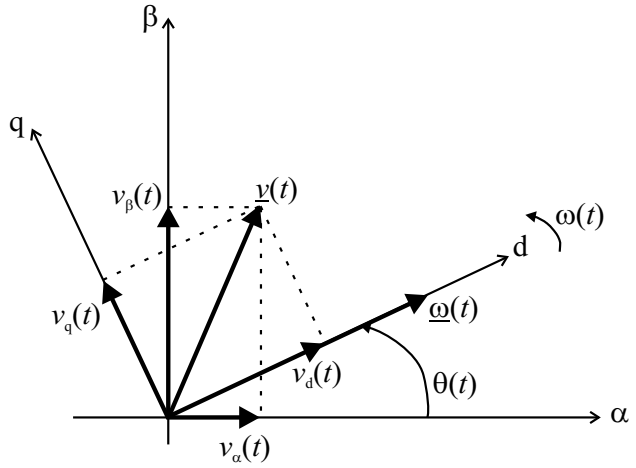

Fig. A.1 Relation between the $\alpha\beta$-frame and *dq*-frame.

The transformation can be written in vector form as:

$$\underline{v}_{\mathrm{dq}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{v}_{\alpha\beta}(t) \tag{A.10}$$

with the angle $\theta(t)$ in Fig. A.1 given by

$$\theta(t) = \theta_0(t) + \int_0^{\tau} \omega(\tau)\, d\tau \tag{A.11}$$

and the inverse transformation is defined by the expression

$$\underline{v}_{\alpha\beta}(t) = \mathrm{e}^{\mathrm{j}\theta(t)} \cdot \underline{v}_{\mathrm{dq}}(t) \tag{A.12}$$

The components in the *dq*-frame can be determined from Fig. A.1. In matrix form, the transformation from the $\alpha\beta$-frame to the *dq*-frame can be written as:

$$\begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}(-\theta(t)) \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} \tag{A.13}$$

and the inverse is given by

$$\begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} = \mathbf{R}(\theta(t)) \begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} \tag{A.14}$$

where the projection matrix is

$$\mathbf{R}(\theta(t)) = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \tag{A.15}$$

A.3 Transformations for voltage and current vectors in the *dq*-system

Suppose a symmetrical sinusoidal three-phase voltage with angular frequency $\omega(t)$ is transformed into a vector $\underline{u}(t) = u_{\alpha}(t) + \mathrm{j}u_{\beta}(t)$ in the $\alpha\beta$-frame. When transforming it further to the *dq*-frame, the *q*-axis in the *dq*-frame is normally defined as parallel to the voltage vector $\underline{u}(t)$. This definition originates from a flux vector parallel to the *d*-axis in the *dq*-frame. The voltage vector is proportional to the time derivative of the flux vector. As a consequence of the chosen reference vector, the voltage vector $\underline{u}(t)$ will only contain a *q*-component in the *dq*-frame. The transformation equation for a current vector from the $\alpha\beta$-frame to the *dq*-frame becomes, in matrix form:

$$\begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}\left(-\left(\omega t - \frac{\pi}{2}\right)\right) \cdot \begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} \tag{A.16}$$

and the inverse

$$\begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} = \mathbf{R}\left(\omega t - \frac{\pi}{2}\right) \cdot \begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} \tag{A.17}$$

The transformation from the $\alpha\beta$-frame into the dq-frame for current vectors is the same as for voltage vectors.

A.4 Voltage vectors for unsymmetrical three-phase systems

The phase voltages for a three-phase system can be written as

$$\begin{aligned} e_{\mathrm{a}}(t) &= E_{\mathrm{a}}(t)\cdot\cos(\omega t-\varphi_{\mathrm{a}}) \\ e_{\mathrm{b}}(t) &= E_{\mathrm{b}}(t)\cdot\cos(\omega t-\frac{2}{3}\pi-\varphi_{\mathrm{b}}) \\ e_{\mathrm{c}}(t) &= E_{\mathrm{c}}(t)\cdot\cos(\omega t-\frac{4}{3}\pi-\varphi_{\mathrm{c}}) \end{aligned} \tag{A.18}$$

where $E_{\mathrm{a}}(t)$, $E_{\mathrm{b}}(t)$ and $E_{\mathrm{c}}(t)$ are the amplitudes of the three-phase voltages, φ_{a}, φ_{b} and φ_{c} are the phase angles of the three-phase voltages, and ω is the angular frequency of the system.

If the amplitudes $\hat{e}_{\mathrm{a}}(t)$, $\hat{e}_{\mathrm{b}}(t)$ and $\hat{e}_{\mathrm{c}}(t)$ are unequal, the voltage vector can be written as the sum of two vectors rotating in opposite directions and interpreted as positive- and negative-sequence vectors

$$\underline{e}_{\alpha\beta}(t) = E_{\mathrm{p}}\mathrm{e}^{\mathrm{j}(\omega t+\varphi_{\mathrm{p}})} + E_{\mathrm{n}}\mathrm{e}^{-\mathrm{j}(\omega t+\varphi_{\mathrm{n}})} \tag{A.19}$$

where E_{p} and E_{n} are the amplitudes of positive- and negative-sequence vectors, respectively, and the corresponding phase angles are denoted by φ_{p} and φ_{n}. To determine amplitudes and phase angles of positive- and negative-sequence vectors in (A.19), a two-step solving technique can be used. First, the phase shifts are set to zero, so that the amplitudes E_{p} and E_{n} can easily be detected. In the next step, the phase shifts φ_{p} and φ_{n} are determined.

When transforming an unsymmetrical three-phase voltage into the dq-coordinate system, two rotating frames are used, accordingly. They are

called positive and negative synchronous reference frames and denoted by *dqp*- and *dqn*-, respectively. They can be defined by the transformations

$$\underline{e}_{\mathrm{dqp}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.20}$$

$$\underline{e}_{\mathrm{dqn}}(t) = \mathrm{e}^{+\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.21}$$

where the transformation angle $\theta(t)$ is locked to the positive phase sequence flux vector. The positive phase sequence vector in the *dqp*-coordinate system is expressed as

$$e_{\mathrm{dp}} + \mathrm{j}e_{\mathrm{qp}} = -E_{\mathrm{p}}\sin(\varphi_{\mathrm{p}}) + \mathrm{j}E_{\mathrm{p}}\cos(\varphi_{\mathrm{p}}) \tag{A.22}$$

and the negative phase sequence vector in the *dqn*-coordinate system is given by

$$e_{\mathrm{dn}} + \mathrm{j}e_{\mathrm{qn}} = -E_{\mathrm{n}}\sin(\varphi_{\mathrm{n}}) + \mathrm{j}E_{\mathrm{n}}\cos(\varphi_{\mathrm{n}})\,. \tag{A.23}$$

Appendix B
LCL-filter design

The schematic diagram of the power circuit of the VSC connected to the grid through LCL-filter has been shown in Fig. 2.9.

Assuming the grid-voltage as a disturbance and neglecting R_1 and R_2, the transfer function of the filter is then $I_2(s)$ /$U(s)$, where I_2 is the filter current on the grid side and U is the VSC output voltage, and is calculated as follows:

$$\frac{U(s)}{I_1(s)} = \frac{L_2/C_f}{\left(sL_2 + \frac{1}{sC_f}\right)} + sL_1 = \frac{sL_2 + 1/sC_f}{s^2 L_1 L_2 + \frac{(L_1 + L_2)}{C_f}} \tag{B-1}$$

Using the current divider rule, the grid-side current is

$$I_2(s) = I_1(s)\frac{1/sC_f}{sL_2 + \frac{1}{sC_f}} \tag{B-2}$$

It follows that

$$I_1(s) = I_2(s)\cdot\left(s^2 L_2 C_f + 1\right) \tag{B-3}$$

Then the transfer function becomes

$$\frac{I_2(s)}{U(s)} = \frac{1/C_f L_1 L_2}{s\left(s^2 + \frac{L_1 + L_2}{L_1 L_2 C_f}\right)} \tag{B-4}$$

The resonant frequency is then:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{B-5}$$

The filter parameters are chosen such that the following conditions are satisfied [23], [71]:

- Neglecting the filter resistances, the voltage drop across the inductances should be limited to 10% during nominal operation, which agrees with the previous design criteria for L-filter;
- The grid side inductance is a fraction of the converter side inductance, since the latter is responsible for the attenuation of most of the switching ripple;
- The capacitive value is limited by the decrease of the power factor at rated power in case of idle operation of the VSC (it will be considered as less or equal 10%);
- The resonance frequency is in the range between ten times the fundamental frequency and one half the switching frequency;
- The IEC 1000-3-4 regulation states that current harmonics above 33rd should be less than 0.6% of the nominal current;
- The resistances are taken as 10% of the value of the corresponding inductances.

According to these conditions the following equations can be used

$$L_1 + L_2 = 0.1 \text{ p.u.} \tag{B-6}$$

$$L_2 = r \cdot L_1 \tag{B-7}$$

where r is the ratio between the inductance on the grid side to the inductance on the converter side, which is less than 1.

$$C_f \leq 0.1 \quad \text{p.u.} \tag{B-8}$$

$$500 \text{ Hz} < f_{res} < 1250 \text{ Hz} \quad \text{(for sampling frequency of 5kHz)} \tag{B-9}$$

From (B-4), the gain of the system at the h harmonic is expressed as

$$\left|G(jh\omega)\right| = \frac{1/C_f L_1 L_2}{\left| jh\omega\left((jh\omega)^2 + \frac{L_1 + L_2}{L_1 L_2 C_f} \right) \right|} \leq 0.006 \text{ .} \tag{B-10}$$

Equations (B-9) and (B-10) are used as check up conditions. Using a capacitance value of 0.05 p.u., (B-9) is not satisfied for different inductance ratios (r), as shown in Fig. B.1. Increasing the capacitance value to 0.1 p.u.,

a value of r = 0.4 has been chosen to satisfy all conditions (see Fig. B.2 and Fig. B.3). The LCL-filter parameters are then calculated as reported in Appendix C.

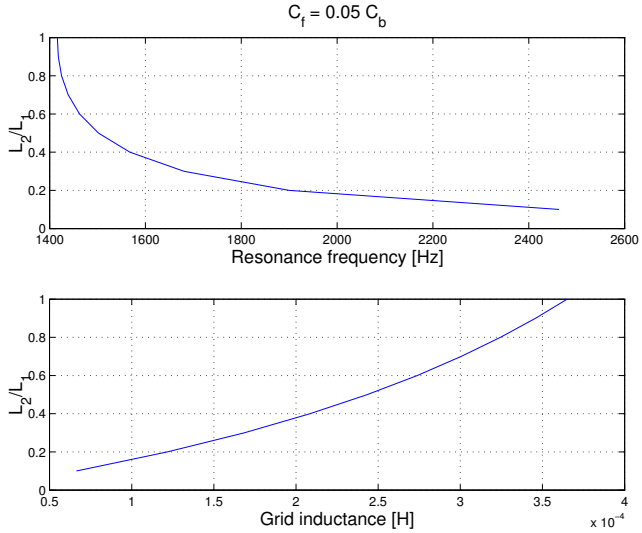

Fig. B.1 Relation between *r*, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 5% of the base value.

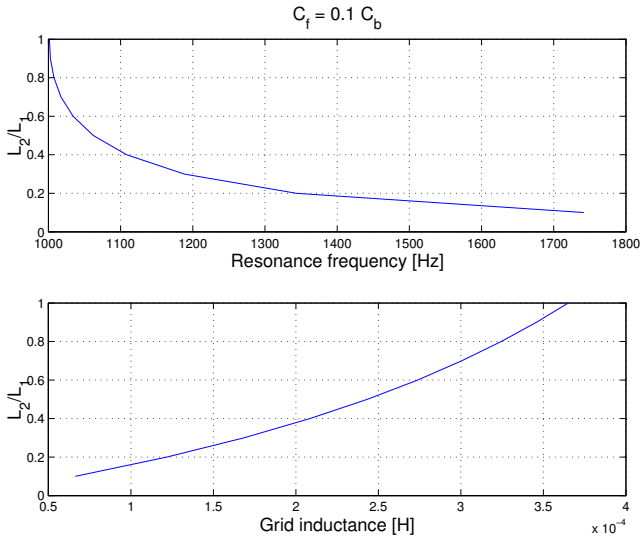

Fig. B.2 Relation between r, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 10% of the base value.

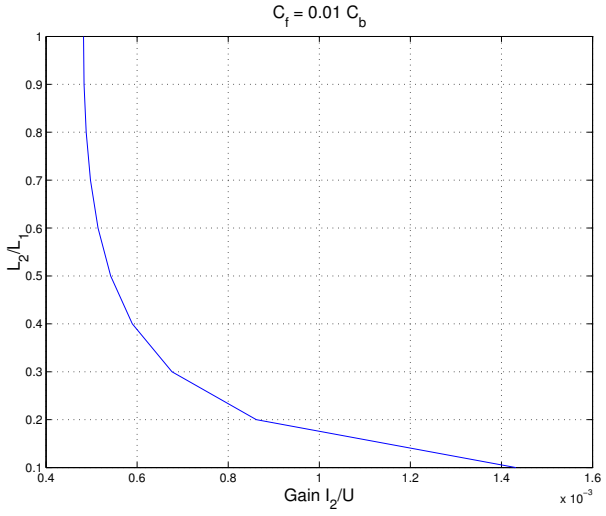

Fig. B.3 Relation between *r* and the gain filter I_2/U.

Appendix C
Power system parameters

C.1 Per-unit base values

The base values for the AC voltage and current are

$$E_{\text{base}} = 400 \text{ V} \tag{C-1}$$

$$I_{\text{base}} = 100 \text{ A} \tag{C-2}$$

The base value of the impedance is then obtained according to

$$Z_{\text{base}} = \frac{E_{\text{base}}}{\sqrt{3} I_{\text{base}}} = 2.3\Omega \tag{C-3}$$

The base values for the DC-link voltage and current are equal to

$$U_{\text{DC,base}} = 650 \text{ V} \tag{C-4}$$

$$I_{\text{DC,base}} = \frac{\sqrt{3} E_{\text{base}} I_{\text{base}}}{U_{\text{DC,base}}} = 107\text{A} \tag{C-5}$$

C.2 L-filter system data

Table C-1 System data with L-filter.

Description	Symbol	Value
Nominal RMS phase-to-phase AC voltage	E	400 V
Nominal RMS phase current	I_{n}	100 A
Nominal grid frequency	f_{n}	50 Hz
Nominal DC link voltage	U_{dc}	650 V
Nominal DC input current	I_{dc}	107 A
Filter resistance	R	23 mΩ
Filter inductance	L	0.73 mH
DC-link capacitance	C	550 µF
DC-chopper damping resistance	R_{d}	10 Ω

C.3 LCL-filter parameters

Table C-2 LCL-Filter parameters.

Parameter	p.u.	Actual
L_1	0.071	0.52 mH
R_1	0.1 L_1	1.6 mΩ
L_2	0.027	0.2 mH
R_2	0.1 L_2	0.6 mΩ
C_f	0.1	137.8 μF

C.4 Weak grid parameters

Table C-3 Weak network parameters.

Parameter	Value
V_s	400 V
R_s	3x0.05 Ω
L_s	3x2.05 mH
C_s	3x46 μF

Appendix D
Controller parameters

D.1 Parameters for VCC for L-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Dead beat gain	k_p	3.7
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.5

D.2 Parameters for VCC for LCL-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Outer controller gain	k_{p1} (0.7 k_{p2})	0.546
Second controller gain	k_{p2} (0.3 k_{p3})	0.78
Inner controller gain	k_{p3}	2.6
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.07

D.3 Parameters for DC-link voltage regulator

Table D-3 DC-link voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pdc}	0.4
Integral time	T_{idc}	0.04 s

D.4 Parameters for PCC-voltage regulator

Table D-4 PCC-voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pr}	0.5
Integral time	T_{ir}	0.05 s

Appendix E
LCL-filter current reference-generation

The power at the grid side S_2 is expressed as

$$S_2 = S_{\mathrm{ac},2} + S_{\mathrm{s}2,2} + S_{\mathrm{c}2,2} \tag{E-1}$$

where S_{ac} is the power at the fundamental frequency, $S_{\mathrm{s}2}$ and $S_{\mathrm{c}2}$ are sine and cosine components of the power at double the fundamental frequency, which are called the oscillating powers. The power is calculated in *dqp*- and *dqn*-frames as follows

$$S_2 = \left(e^{\mathrm{j}\omega t}\underline{e}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{e}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-2}$$

Expanding this equation leads to

$$\begin{aligned} S_{\mathrm{s}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{qn}} - e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dn}}i_{2\mathrm{qp}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dp}}i_{2\mathrm{dn}} - e_{\mathrm{qn}}i_{2\mathrm{qp}} - e_{\mathrm{dn}}i_{2\mathrm{dp}}\right) \end{aligned} \tag{E-3}$$

$$\begin{aligned} S_{\mathrm{c}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{dn}} + e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dn}}i_{2\mathrm{dp}} + e_{\mathrm{qn}}i_{2\mathrm{qp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dp}}i_{2\mathrm{qn}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} - e_{\mathrm{dn}}i_{2\mathrm{qp}}\right) \end{aligned} \tag{E-4}$$

The power at the converter side S_1 is expressed in the same manner and same designations as

$$S_1 = S_{\mathrm{ac},1} + S_{\mathrm{s}2,1} + S_{\mathrm{c}2,1} \tag{E-5}$$

It is calculated in *dqp*- and *dqn*- frames as follows:

$$S_1 = \left(e^{\mathrm{j}\omega t}\underline{u}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{u}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-6}$$

Expanding this equation results in the following:

$$\begin{aligned} S_{\mathrm{ac},1} &= u_{\mathrm{dp}} i_{\mathrm{1dp}} + u_{\mathrm{qp}} i_{\mathrm{1qp}} + u_{\mathrm{dn}} i_{\mathrm{1dn}} + u_{\mathrm{qn}} i_{\mathrm{1qn}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dp}} - u_{\mathrm{dp}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qn}}\right) \end{aligned} \tag{E-7}$$

$$\begin{aligned} S_{\mathrm{s}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1qn}} - u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dp}} i_{\mathrm{1dn}} - u_{\mathrm{qn}} i_{\mathrm{1qp}} - u_{\mathrm{dn}} i_{\mathrm{1dp}}\right) \end{aligned} \tag{E-8}$$

$$\begin{aligned} S_{\mathrm{c}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1dn}} + u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dn}} i_{\mathrm{1dp}} + u_{\mathrm{qn}} i_{\mathrm{1qp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dp}} i_{\mathrm{1qn}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} - u_{\mathrm{dn}} i_{\mathrm{1qp}}\right) \end{aligned} \tag{E-9}$$

Applying KVL to the outer loop of the LCL-filter

$$\underline{u}_{\mathrm{dqp}} = \underline{e}_{\mathrm{dqp}} + R_1 \underline{i}_{\mathrm{1dqp}} + \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqp}} + R_2 \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqp}} \tag{E-10}$$

$$\underline{u}_{\mathrm{dqn}} = \underline{e}_{\mathrm{dqn}} + R_1 \underline{i}_{\mathrm{1dqn}} - \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqn}} + R_2 \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqn}} \tag{E-11}$$

Applying KCL at the filter capacitor connection node

$$\underline{i}_{\mathrm{1dqp}} = \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqp}} \tag{E-12}$$

$$\underline{i}_{\mathrm{1dqn}} = \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqn}} \tag{E-13}$$

Substituting (E-10) to (E-13) in (E-7), the active power at the converter side will be

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}}\left(i_{\mathrm{2dp}} - Y_{\mathrm{c}} u_{\mathrm{cqp}}\right) + i_{\mathrm{1dp}}\left(R_1 i_{\mathrm{1dp}} - \omega L_1 i_{\mathrm{1qp}} + R_2 i_{\mathrm{2dp}} - \omega L_2 i_{\mathrm{2qp}}\right) \\ & + e_{\mathrm{qp}}\left(i_{\mathrm{2qp}} + Y_{\mathrm{c}} u_{\mathrm{cdp}}\right) + i_{\mathrm{1qp}}\left(R_1 i_{\mathrm{1qp}} + \omega L_1 i_{\mathrm{1dp}} + R_2 i_{\mathrm{2qp}} + \omega L_2 i_{\mathrm{2dp}}\right) \\ & + e_{\mathrm{dn}}\left(i_{\mathrm{2dn}} + Y_{\mathrm{c}} u_{\mathrm{cqn}}\right) + i_{\mathrm{1dn}}\left(R_1 i_{\mathrm{1dn}} + \omega L_1 i_{\mathrm{1qn}} + R_2 i_{\mathrm{2dn}} + \omega L_2 i_{\mathrm{2qn}}\right) \\ & + e_{\mathrm{qn}}\left(i_{\mathrm{2qn}} - Y_{\mathrm{c}} u_{\mathrm{cdn}}\right) + i_{\mathrm{1qn}}\left(R_1 i_{\mathrm{1qn}} - \omega L_1 i_{\mathrm{1dn}} + R_2 i_{\mathrm{2qn}} - \omega L_2 i_{\mathrm{2dn}}\right) \end{aligned} \tag{E-14}$$

where $Y_{\mathrm{c}} = \omega C_{\mathrm{f}}$. This reduces to

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}} i_{\mathrm{2dp}} + e_{\mathrm{qp}} i_{\mathrm{2qp}} + e_{\mathrm{dn}} i_{\mathrm{2dn}} + e_{\mathrm{qn}} i_{\mathrm{2qn}} \\ & + R_1\left(i_{\mathrm{1dp}}^2 + i_{\mathrm{1qp}}^2 + i_{\mathrm{1dn}}^2 + i_{\mathrm{1qn}}^2\right) \\ & + R_2\left(i_{\mathrm{2dp}} i_{\mathrm{1dp}} + i_{\mathrm{2qp}} i_{\mathrm{1qp}} + i_{\mathrm{2dn}} i_{\mathrm{1dn}} + i_{\mathrm{2qn}} i_{\mathrm{1qn}}\right) \\ & + \omega L_2\left(-i_{\mathrm{2qp}} i_{\mathrm{1dp}} + i_{\mathrm{2dp}} i_{\mathrm{1qp}} + i_{\mathrm{2qn}} i_{\mathrm{1dn}} - i_{\mathrm{2dn}} i_{\mathrm{1qn}}\right) \\ & + Y_{\mathrm{c}}\left(-u_{\mathrm{cqp}} e_{\mathrm{dp}} + u_{\mathrm{cdp}} e_{\mathrm{qp}} + u_{\mathrm{cqn}} e_{\mathrm{dn}} - u_{\mathrm{cdn}} e_{\mathrm{qn}}\right) \end{aligned} \tag{E-15}$$

which can be separated into three different parts as follows

$$P_{\mathrm{ac},1} = P_{\mathrm{ac},2} + \Delta P(i) + \Delta P(e) \tag{E-16}$$

where $\Delta P(i)$ is the active power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta P(e)$ is the active power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

In the same way, the reactive power at the converter side is calculated as

$$\begin{aligned} Q_{\mathrm{ac},1} = {} & e_{\mathrm{qp}} i_{2\mathrm{dp}} - e_{\mathrm{dp}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qn}} \\ & + \omega L_1 \left(i_{1\mathrm{dp}}^2 + i_{1\mathrm{qp}}^2 - i_{1\mathrm{dn}}^2 - i_{1\mathrm{qn}}^2 \right) \\ & + R_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{dp}} - i_{2\mathrm{dp}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qn}} \right) \\ & + \omega L_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{dp}} + i_{2\mathrm{qp}} i_{1\mathrm{qp}} - i_{2\mathrm{dn}} i_{1\mathrm{dn}} - i_{2\mathrm{qn}} i_{1\mathrm{qn}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cqp}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dp}} + u_{\mathrm{cqn}} e_{\mathrm{qn}} + u_{\mathrm{cdn}} e_{\mathrm{dn}} \right) \end{aligned} \tag{E-17}$$

which can be separated into three different parts, as follows

$$Q_{\mathrm{ac},1} = Q_{\mathrm{ac},2} + \Delta Q(i) + \Delta Q(e) \tag{E-18}$$

where $\Delta Q(i)$ is the reactive power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta Q(e)$ is the reactive power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

The sine and cosine components of the active oscillating power are derived as

$$\begin{aligned} P_{\mathrm{s}2,1} = {} & e_{\mathrm{dp}} i_{2\mathrm{qn}} - e_{\mathrm{qp}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dp}} \\ & + 2R_1 \left(i_{1\mathrm{dp}} i_{1\mathrm{qn}} - i_{1\mathrm{qp}} i_{1\mathrm{dn}} \right) \\ & - 2\omega L_1 \left(i_{1\mathrm{qp}} i_{1\mathrm{qn}} + i_{1\mathrm{dp}} i_{1\mathrm{dn}} \right) \\ & + R_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{qn}} - i_{2\mathrm{qp}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dp}} \right) \\ & - \omega L_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{qn}} + i_{2\mathrm{dp}} i_{1\mathrm{dn}} + i_{2\mathrm{qn}} i_{1\mathrm{qp}} + i_{2\mathrm{dn}} i_{1\mathrm{dp}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cdn}} e_{\mathrm{dp}} - u_{\mathrm{cqn}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dn}} - u_{\mathrm{cqp}} e_{\mathrm{qn}} \right) \end{aligned} \tag{E-19}$$

$$P_{s2,1} = P_{s2,2} + \Delta P_{s2}(i) + \Delta P_{s2}(e) \tag{E-20}$$

$$\begin{aligned} P_{c2,1} = {} & e_{dp} i_{2dn} + e_{qp} i_{2qn} + e_{dn} i_{2dp} + e_{qn} i_{2qp} \\ & + 2R_1 \left(i_{1dp} i_{1dn} + i_{1qp} i_{1qn} \right) \\ & + 2\omega L_1 \left(i_{1dp} i_{1qn} - i_{1dn} i_{1qp} \right) \\ & + R_2 \left(i_{2dp} i_{1dn} + i_{2qp} i_{1qn} + i_{2dn} i_{1dp} + i_{2qn} i_{1qp} \right) \\ & + \omega L_2 \left(-i_{2qp} i_{1dn} + i_{2dp} i_{1qn} + i_{2qn} i_{1dp} - i_{2dn} i_{1qp} \right) \\ & + Y_c \left(u_{cqn} e_{dp} - u_{cdn} e_{qp} - u_{cqp} e_{dn} + u_{cdp} e_{qn} \right) \end{aligned} \tag{E-21}$$

$$P_{c2,1} = P_{c2,2} + \Delta P_{c2}(i) + \Delta P_{c2}(e) \tag{E-22}$$

Expressing (E-15) to (E-21) in matrix form will result in

$$\begin{aligned} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} = {} & \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \begin{bmatrix} i_{2dp} \\ i_{2qp} \\ i_{2dn} \\ i_{2qn} \end{bmatrix} \\ & + \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \end{aligned} \tag{E-23}$$

The current references are then calculated using the following matrix

$$\begin{bmatrix} i_{2dp}^* \\ i_{2qp}^* \\ i_{2dn}^* \\ i_{2qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} - Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \tag{E-24}$$

The oscillating power, which is consumed by the filter inductors, is compensated by the power flow from the VSC side. Hence

$$P_{s2,1} = \Delta P_{s2}(i) \tag{E-25}$$

$$P_{c2,1} = \Delta P_{c2}(i) \tag{E-26}$$

Moreover, the active power at the VSC side is assumed to be equal to the power at the DC side of the converter.

$$P_{ac,1} = u_{dc}^{*} i_{v}^{*} \tag{E-27}$$

To achieve zero reactive power at the grid, $Q_{ac,1}$ should supply the reactive power consumed by the filter. Hence

$$Q_{ac,1} = \Delta Q(i) + \Delta Q_{c} \tag{E-28}$$

where ΔQ_{c} is the power loss in the filter capacitor, which is calculated as

$$\Delta Q_{c} = \omega C_{f} \left(u_{cdp}^{2} + u_{cqp}^{2} + u_{cdn}^{2} + u_{cqn}^{2} \right) \tag{E-29}$$

Paper A

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Design of Robust Converter Interface for Wind Power Applications

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Key words:
wind power;
distributed generation;
voltage source converter (VSC);
control;
power electronics;
voltage dips (sags)

As the amount of wind power and other distributed generation with power electronic interface in the grid grows, it becomes unacceptable to disconnect generating units every time a disturbance occurs, as was common practice in the past. Keeping the voltage source converter on-line during unbalanced voltage dips thus becomes a very critical issue. In this article the design of a robust converter interface for wind turbines is investigated. Based on the classification of unbalanced faults that can occur in the grid, resulting in voltage dips at the bus where the turbine is connected, the maximum current that the converter valves must be able to withstand is calculated. The effect of phase angle jumps during faults is also investigated. It is demonstrated that, ultimately, the converter design can be optimized by using statistics of voltage dips and the wind speed distribution for the specific site considered. This is shown by a design example. Copyright © 2005 John Wiley & Sons, Ltd.

Introduction

Integration of distributed generation (DG) in the utility grid offers a number of technical, environmental and economic benefits, both from the utility and the end-user point of view,[1–3] and is therefore becoming more and more popular. The amount of wind power installed in the grid is especially predicted to grow in the coming years.

For variable speed wind turbines, like many other DG technologies, a power electronic interface is used to connect the DG system to the utility grid, with the main function of adapting the characteristics of the active power supplied from the DG to the grid. This power electronic interface usually comprises a current-controlled voltage source converter (VSC) based on IGBT valves, which can be controlled with pulse width modulation (PWM) techniques with high switching frequencies to achieve high controllability and power quality.

The drawback of using a VSC is its sensitivity to voltage disturbances, e.g. voltage dips. A voltage dip is a short-duration drop in voltage that is normally due to a fault.[4] For a VSC a sudden decrease in grid voltage normally causes an increase in current as the control attempts to maintain the power to the DC-link constant. This can lead to tripping of the VSC because of overcurrent in order to protect the IGBTs. Moreover, most faults are unbalanced and result in unbalanced dips, which produce undesirable power oscillations of low-order frequencies resulting in current harmonics and poor DC-link voltage regulation.[5] Ultimately, this can also lead to tripping of the VSC due to DC overvoltage. The common practice in the past has been to disconnect the unit when a fault occurs. However, as the amount of DG with power electronic interface in the grid grows, it becomes unacceptable to lose generating units every time a disturbance occurs. Keeping the VSC on-line during unbalanced voltage dips thus becomes a very critical issue.

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The VSC controller is required to have two main functions: current control and DC-link voltage regulation. A comparison between different types of current controllers for a shunt-connected VSC presented in Reference 6 has proved that the dual vector current controller (DVCC), first proposed in Reference 7, is capable of providing sinusoidal grid currents and regulated DC-link voltage during unbalanced faults. However, an increase in the VSC rating is unavoidable if ride-through capability is desired.

In this article the design of a robust VSC interface for wind turbines is investigated. The performance of the investigated controller during unbalanced dips is demonstrated. Based on the assumption of constant active power flow and the classification of unbalanced faults that can occur in the grid, resulting in voltage dips at the bus where the turbine is connected, the maximum current that the VSC must be able to withstand is calculated. The effect of phase angle jumps during faults is also investigated. It is demonstrated that, ultimately, the VSC design can be optimized by using statistics of voltage dips and the wind speed distribution for the specific site considered. This is shown by a design example.

Voltage Dip Classification

A voltage dip is the voltage experienced at the end-user terminals normally owing to a short-circuit fault somewhere in the grid. In spite of their short duration, between 1 cycle and several seconds, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices. The classification of voltage dips defined by Bollen[4] and reported in Figure 1 is used in this article to quantify the unbalanced voltage dips at the VSC bus. Owing to a fault at bus 3 in Figure 2, a voltage dip occurs at bus 1, which can be either balanced (due to a three-phase fault and called type A) or one of the six unbalanced types in Figure 1.

According to the transformer type, the dip that occurs at bus 1 may change from one type to another, as seen by the VSC connected at bus 2. This transformer (TR) can be one of the following types.

- Type 1: transformers that do not change anything to voltages (e.g. star grounded/star grounded).
- Type 2: transformers that block the zero-sequence voltage (e.g. Y/Y with at least one not grounded or D/Z).
- Type 3: transformers that swap line and phase voltages (e.g. D/Y, Y/D, Y/Z).

The transfer from one dip type to another is listed in Table I. Since this transformer is mainly D/Y (type 3), dips at the equipment terminals are normally of the following five types.

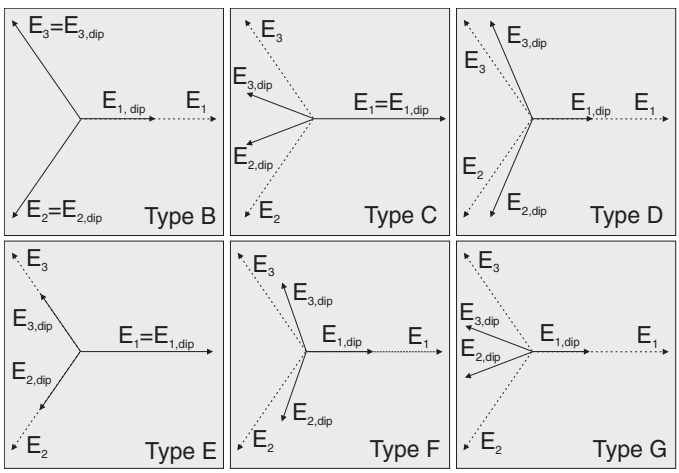

Figure 1. Classification of unbalanced voltage dips from B to G. Phasors of three-phase voltage before (dotted lines) and during fault (full lines) are displayed

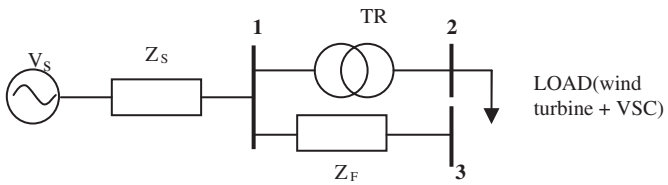

Figure 2. Single-line diagram for dip classification

Table I. Transformation of dip types due to different transformers

Dip type at primary side	A	B	C	D	E	F	G
	Dip type at secondary side						
TR type 1	A	B	C	D	E	F	G
TR type 2	A	D*	C	D	G	F	G
TR type 3	A	C*	D	C	F	G	F

* Indicates that the dip magnitude is not equal to V_{dip} but equal to $\frac{1}{3}+\frac{2}{3}V_{dip}$.

- Type A, due to three-phase faults.
- Types C and D, due to single-phase and double-phase faults.
- Types F and G, due to double-phase-to-ground faults.

Note, however, that the load can in principle be subjected to dips of types B and E if the fault occurs at the same voltage level as the load or if the transformer is of type 1. Therefore we will still consider all seven dip types in the following analysis. In Figure 2, if the X/R ratios for supply impedance Z_S and feeder impedance Z_F are different, the voltage during the fault seen at the terminals of the VSC will have in general a different phase angle as compared with the pre-fault voltage. The impedance angle γ is defined as

$$\gamma = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \tag{1}$$

with $Z_S = R_S + jX_S$ and $Z_F = R_F + jX_F = zl$, where z is the feeder impedance per unit length and l is the feeder length. The expression of the dip voltage at bus 1 will be

$$v_{dip} = \frac{\lambda e^{j\gamma}}{1+\lambda e^{j\gamma}} = V_{dip}\angle\psi \tag{2}$$

where $\lambda e^{j\gamma} = zl/Z_S$, V_{dip} is the dip magnitude and ψ is the phase angle jump. Reference 4 suggests considering four values for the impedance angle γ: 10° as the highest expected value for transmission system faults, 0° as the reference value, −20° for overhead distribution lines and −60° for underground distribution cables. In Figure 3 the relation between the phase angle jump and different dip magnitudes at the four impedance angles is shown. The phase angle jump is bigger for smaller dip magnitudes and is more significant when $\gamma = -60°$.

Investigated System

The investigated system is shown in Figure 4. The VSC is connected to the grid via filter inductors. The three-phase grid currents and voltages are sampled and transformed into dq-vectors via the transformation angle $\theta(k)$ obtained by using a phase-locked loop, which is assumed here to be slow and not to react during faults. The

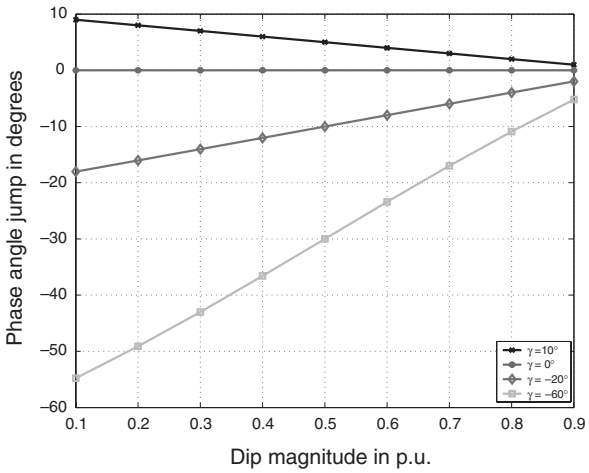

Figure 3. Phase angle jump for different dip magnitudes and impedance angles γ

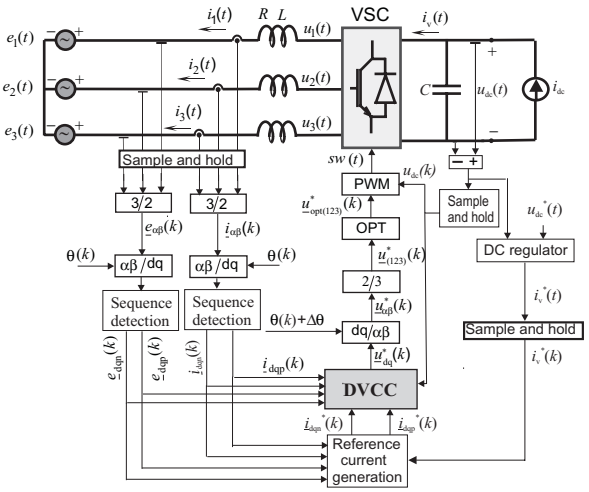

Figure 4. Scheme of investigated system with controller

dq-components of currents and voltages are then used along with the reference current signals in the DVCC to produce the reference voltage signals for the PWM modulator. The voltage across the DC-link capacitor is regulated by using a PI controller, and the output of the DC-link voltage regulator is used to generate the reference currents in order to minimize the ripple of the DC-link voltage by using the algorithm explained later. The reference voltage signals in the *dq*-frame are transformed to three-phase quantities using the angle $\theta(k) + \Delta\theta(k)$, where $\Delta\theta(k)$ compensates for the phase delay due to the execution time of the control computer. The three-phase control signals are then used in the PWM to produce the switching pattern for the VSC. The PWM is optimized to increase the maximum output voltage of the VSC without increasing the DC-link voltage. The block 'OPT' adds a zero-sequence voltage to the control signals. Owing to the absence of a neutral wire, the added zero-sequence waveforms do not result in zero-sequence currents in the grid.

Sequence Detection

The decomposition of the supply voltage into positive and negative sequences is performed in the $\alpha\beta$-frame using the technique proposed in Reference 6. By delaying the measured supply voltage by one-fourth of the

line period T, a vector composed of the same positive-sequence component and a negative-sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative-sequence voltage will be removed. The positive-sequence voltage component can thus be extracted from the measured values as

$$\mathbf{e}_{\mathrm{Pos}}^{(\alpha\beta)} = \frac{1}{2}\left[\mathbf{e}^{(\alpha\beta)}(t) + \mathrm{j}\mathbf{e}^{(\alpha\beta)}\left(t - \frac{T}{4}\right)\right] \tag{3}$$

The negative sequence can be calculated as

$$\mathbf{e}_{\mathrm{neg}}^{(\alpha\beta)} = \frac{1}{2}\left[\mathbf{e}^{(\alpha\beta)}(t) - \mathrm{j}\mathbf{e}^{(\alpha\beta)}\left(t - \frac{T}{4}\right)\right] \tag{4}$$

Then the positive-sequence voltage in the positive-rotating co-ordinate (dqp) is

$$\mathbf{e}_{dq\mathrm{p}} = e^{-\mathrm{j}\theta}\mathbf{e}_{\mathrm{Pos}}^{(\alpha\beta)} \tag{5}$$

and the negative-sequence voltage in the negative-rotating co-ordinate (dqn) is

$$\mathbf{e}_{dq\mathrm{n}} = e^{\mathrm{j}\theta}\mathbf{e}_{\mathrm{neg}}^{(\alpha\beta)} \tag{6}$$

The latter will be seen as a constant signal in the negative-rotating plane dqn, which utilizes the opposite angle for the dq-transformation.

Implementing the DVCC

The DVCC consists of two PI controllers that control the positive- and negative-sequence currents separately, as shown in Figure 5. Since all unbalanced faults contain positive- and negative-sequence components, the DVCC has proved to give better performance than only one controller implemented in the positive dq-frame concerning the grid current harmonics and DC voltage ripples.[6]

The positive-sequence current controller is described for a sampling instant k in the dqp-frame by the equation

$$\mathbf{u}_{dq\mathrm{p}}^{*}(k+1) = \mathbf{e}_{dq\mathrm{p}}(k) + R\mathbf{i}_{dq\mathrm{p}}(k) + \mathrm{j}\omega L\mathbf{i}_{dq\mathrm{p}}(k) + 0.7k_{\mathrm{p}}(\mathbf{i}_{dq\mathrm{p}}^{*}(k)\mathbf{i}_{dq\mathrm{p}}(k)) - \Delta\mathbf{u}_{\mathrm{I},dq\mathrm{p}}(k) \tag{7}$$

where $\mathbf{i}_{dq\mathrm{p}}(k)$ is the positive-sequence grid dq-current, $\mathbf{i}^{*}_{dq\mathrm{p}}(k)$ is the positive-sequence reference dq-current and k_{p} is the dead-beat gain. The integration term $\Delta\mathbf{u}_{\mathrm{I},dq\mathrm{p}}(k)$ is defined as

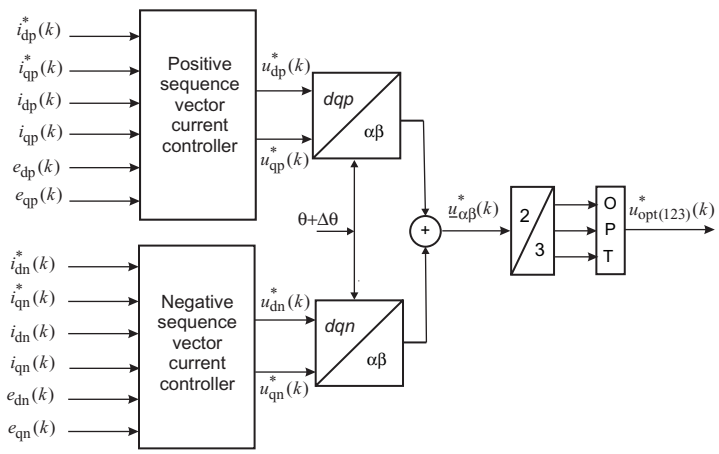

Figure 5. Block scheme of DVCC

$$\Delta\mathbf{u}_{\mathrm{I},dqp}(k+1) = \Delta\mathbf{u}_{\mathrm{I},dqp}(k) + k_{\mathrm{I}}\left(\mathbf{i}^{*}_{dqp}(k-1) - \mathbf{i}_{dqp}(k)\right) \tag{8}$$

With analogous notation the negative-sequence current controller is described by the equation

$$\mathbf{e}^{*}_{dqn}(k+1) = \mathbf{e}_{dqn}(k) + R\mathbf{i}_{dqn}(k) - \mathrm{j}\omega L\mathbf{i}_{dqn}(k) + 0.7k_p\left(\mathbf{i}^{*}_{dqn}(k) - \mathbf{i}_{dqn}(k)\right) + \Delta\mathbf{u}_{\mathrm{I},dqn}(k) \tag{9}$$

and is implemented in the *dq*n-frame.

Reference Current Generation

In order to generate proper current references, consider the complex apparent power from the grid

$$\mathbf{S}_{\mathrm{g}} = \left(\mathbf{e}_{dqp}e^{\mathrm{j}\omega t} + \mathbf{e}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)\left(\mathbf{i}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \mathbf{i}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)^{\mathrm{conj}} \tag{10}$$

which is the sum of a constant apparent power and two terms in sine and cosine, oscillating with double the grid frequency. By expanding equation 10, the following expression in matrix form can be written:

$$\begin{bmatrix} P_{\mathrm{g}} \\ Q_{\mathrm{g}} \\ P_{\mathrm{S2g}} \\ P_{\mathrm{c2g}} \end{bmatrix} = \begin{bmatrix} e_{d\mathrm{p}} & e_{q\mathrm{p}} & e_{d\mathrm{n}} & e_{q\mathrm{n}} \\ e_{q\mathrm{p}} & -e_{d\mathrm{p}} & e_{q\mathrm{n}} & -e_{d\mathrm{n}} \\ e_{q\mathrm{n}} & -e_{d\mathrm{n}} & -e_{q\mathrm{p}} & e_{d\mathrm{p}} \\ e_{d\mathrm{n}} & e_{q\mathrm{n}} & e_{d\mathrm{p}} & e_{q\mathrm{p}} \end{bmatrix} \begin{bmatrix} i_{d\mathrm{p}} \\ i_{q\mathrm{p}} \\ i_{d\mathrm{n}} \\ i_{q\mathrm{n}} \end{bmatrix} \tag{11}$$

where P_{g} and Q_{g} are the constant active and reactive powers respectively and P_{s2g} and P_{c2g} represent the second-harmonic sine and cosine components of the active power respectively. These are the oscillating powers due to the imbalance in the grid voltages. The fluctuating reactive powers are not considered since they do not affect the DC-link voltage and its control.

Calculating the apparent power $\mathbf{S}_{\mathrm{ac}}$ at the VSC terminals as in (10), but with the VSC voltages in place of the grid voltages, and considering that $\mathbf{S}_{\mathrm{ac}}$ is the sum of the apparent power from the grid ($\mathbf{S}_{\mathrm{g}}$) and the apparent power dissipated in the filter ($\Delta\mathbf{S}$), i.e.

$$\mathbf{S}_{\mathrm{ac}} = \mathbf{S}_{\mathrm{g}} + \Delta\mathbf{S} \tag{12}$$

the reference currents can be calculated as

$$\begin{bmatrix} i^{*}_{d\mathrm{p}} \\ i^{*}_{q\mathrm{p}} \\ i^{*}_{d\mathrm{n}} \\ i^{*}_{q\mathrm{n}} \end{bmatrix} = \begin{bmatrix} e_{d\mathrm{p}} & e_{q\mathrm{p}} & e_{d\mathrm{n}} & e_{q\mathrm{n}} \\ e_{d\mathrm{p}} & -e_{q\mathrm{p}} & e_{q\mathrm{n}} & -e_{d\mathrm{n}} \\ e_{q\mathrm{n}} & -e_{d\mathrm{n}} & -e_{q\mathrm{p}} & e_{d\mathrm{p}} \\ e_{d\mathrm{n}} & e_{q\mathrm{n}} & e_{d\mathrm{p}} & e_{q\mathrm{p}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta P \\ 0 \\ -\Delta P_{\mathrm{s2}} \\ -\Delta P_{\mathrm{c2}} \end{bmatrix} \tag{13}$$

where P_{dc} is the power at the DC side of the converter, which is considered equal to the active power at the AC terminals neglecting the losses, and ΔP, ΔP_{c2} and ΔP_{s2} are the active powers dissipated in the filter, given by

$$\Delta P = R(i^2_{d\mathrm{p}} + i^2_{q\mathrm{p}} + i^2_{d\mathrm{n}} + i^2_{q\mathrm{n}}) \tag{14}$$

$$\Delta P_{\mathrm{c2}} = 2R(i_{d\mathrm{p}}i_{d\mathrm{n}} + i_{q\mathrm{p}}i_{q\mathrm{n}}) + 2\omega L(i_{d\mathrm{p}}i_{q\mathrm{n}} - i_{q\mathrm{p}}i_{d\mathrm{n}}) \tag{15}$$

$$\Delta P_{\mathrm{s2}} = 2R(i_{d\mathrm{p}}i_{d\mathrm{n}} - i_{q\mathrm{p}}i_{d\mathrm{n}}) + 2\omega L(-i_{d\mathrm{p}}i_{d\mathrm{n}} - i_{q\mathrm{p}}i_{q\mathrm{n}}) \tag{16}$$

DC-link Voltage Regulator

In variable speed wind turbine systems the DC-link voltage cannot be considered constant. It should be regulated to ensure correct operation of the VSC and to avoid damage to the valves and the DC-link capacitor. The current from the DG source to the DC-link is also not constant, but its variations can be assumed to be much

slower than the time range of the transient phenomena considered here. Therefore the DC-link is modelled as a capacitor with a current source in parallel. A simple PI controller is implemented, where the measured DC capacitor voltage u_{dc} is compared with its reference value u^*_{dc} and the error signal is used to produce a reference DC current signal i^*_v according to

$$i_v^*(s) = -k_{pdc}\left(1 + \frac{1}{sT_{idc}}\right)\left(u_{dc}^*(s) - u_{dc}(s)\right) \tag{17}$$

where k_{pdc} and T_{idc} are the proportional gain and integral time constant of the DC PI controller respectively and s is the Laplace operator.

DC-link Capacitor Design

The instantaneous active power difference between the AC and DC side is stored in the capacitor, which causes the DC link voltage to vary. Hence the size of the capacitor can be determined from the constraint on the maximum allowed DC-link voltage ripple Δu_{dc}. The design expression for the DC-link capacitor size, which has been derived based on a simplified analysis of the instantaneous active power flow in Reference 8, is

$$C = \frac{S_n}{u_{dc}^* \Delta u_{dc}} \frac{1}{2\omega_n} \tag{18}$$

where S_n and ω_n are the rated power of the VSC and the fundamental angular frequency of the grid respectively. The allowed Δu_{dc} is considered as ±5% of the rated voltage, resulting in a DC capacitance of 5.2 mF. However, owing to the high performance of the DC-link voltage controller along with DVCC, the size of the capacitance is reduced to 550 μF.

Performance Analysis

Response to Unbalanced Dips

For the investigated system, all six unbalanced dip types with magnitude varying between 0.3 and 0.9 pu in steps of 0.1 pu have been simulated using Matlab/Simulink. The dip starts at 0.1 s and ends at 0.2 s. System data and controller data are shown in Tables II and III, respectively.

As an example, the grid currents in the three-phase domain and the DC-link voltage are shown in Figure 6 for a dip of type C with magnitude 40%. During the dip the grid currents increase to about 3 pu. The DC voltage shows a variation during the transients at the beginning and end of the dip. However, the ripple during the transient is not bigger than 10% peak-to-peak and is quite quickly damped to almost zero.

Table II. System data

Constant	Symbol	Value	Value in pu
Nominal AC voltage	E	400 V	1.0
Nominal phase current	I_n	100 A	1.0
Nominal grid frequency	f_n	50 Hz	
Nominal DC voltage	U_{dc}	650 V	1.0 (DC)
Nominal DC current	I_{dc}	107 A	1.0 (DC)
Filter resistance	R	23 mΩ	0.01
Filter inductance	L	0.73 mH	0.1
DC-link capacitance	C	550 μF	τ = 1.7 ms

Table III. Controller data

Constant	Symbol	Value/equation
Sampling frequency	f_S	5 kHz
Sampling time	T_S	200 μs
Dead-beat gain	K_p	$\frac{L}{T_S}+\frac{R}{2}=3.7$
Integration time constant	T_i	0.03
DC controller proportional gain	k_{pdc}	0.2
DC controller integral constant	T_{idc}	$\frac{4\zeta^2}{K_{pdc}}C$
DC controller damping ratio	ζ	0.7

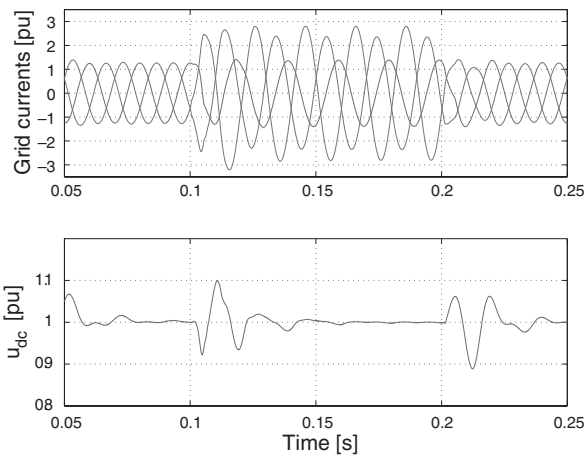

Figure 6. Grid currents (top) and DC voltage (bottom) for 40% dip type C

Maximum grid current and peak-to-peak DC voltage ripple during the dip are shown for all dip types with varying magnitudes in Figure 7. In order to ride through dips with a minimum retained voltage of 30%, the VSC valves should be able to carry a maximum current of 3.65 pu. The maximum DC voltage ripple is ±0.5% around the nominal value for dip magnitudes higher than 30%.

Effect of the Phase Angle Jump

The four values of impedance angle $\gamma = 10°, 0°, -20°$ and $-60°$ are used. Again for a dip of type C with retained voltage 40%, Figure 8 shows that only in the case of $\gamma = -60°$ does the phase angle jump seem to have an effect on the DC voltage ripple. The effect of the phase angle jump on the maximum grid current is represented in Figure 9 for all unbalanced dip types.

No noticeable effect can be seen for $\gamma = 10°$ or $\gamma = -20°$, where the maximum grid current is the same as without phase angle jump. On the other hand, for $\gamma = -60°$ the current is higher and the effect is more significant as the dip magnitude decreases. The absolute maximum current is found for dip type D with magnitude 30% and is equal to 4.5 pu, which is significantly higher than the corresponding value found with zero phase angle jump (3.65 pu). It might therefore be deemed necessary to consider the phase angle jump explicitly in the design.

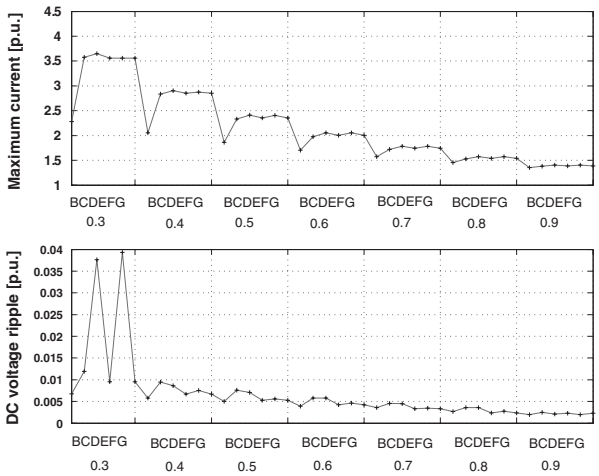

Figure 7. Maximum grid current (top) and DC voltage ripple (bottom) for all unbalanced dip types with magnitude between 0.3 and 0.9 pu

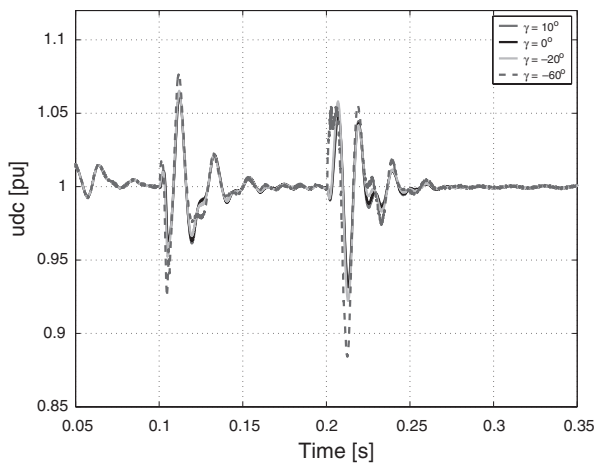

Figure 8. DC-link voltage for 40% dip type C

Converter Design

Design Equations of Maximum Current

In order to calculate the required current rating of the VSC valves to ride through voltage dips in the grid, the maximum current has been calculated for unbalanced faults. Equation (13) has been used to calculate the current components in the *dq*p- and *dq*n-frame assuming zero oscillating powers. Furthermore, the phase angle jump is assumed to be zero, which result in zero *q*p- and *q*n-components of the grid voltage according to Table IV. The grid current is then described as

$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \frac{KP_{dc}}{e_{dp}^2 - e_{dn}^2} \begin{bmatrix} e_{dp} \\ 0 \\ -e_{dn} \\ 0 \end{bmatrix} \tag{19}$$

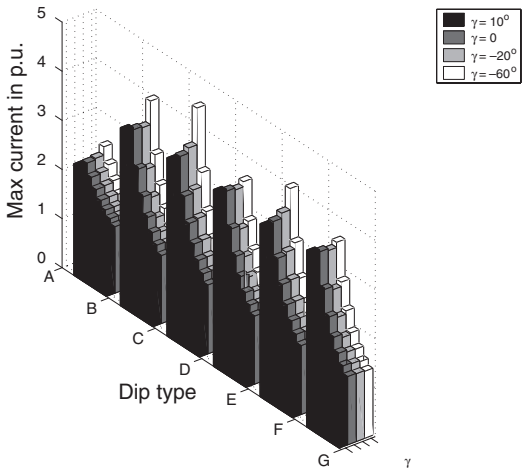

Figure 9. Effect of phase angle jump on maximum grid current for all unbalanced dips (types B–G) with magnitude between 30% and 90% (dip magnitude increases for each type going from left to right)

Table IV. Positive- and negative-sequence *dq*-components of grid voltage for unbalanced voltage dips with phase angle jump

Dip	e_{dp}	e_{qp}	e_{dn}	e_{qn}
A	$EV_{\text{dip}}\cos\psi$	$EV_{\text{dip}}\sin\psi$	0	0
B	$\frac{E}{3}(2+V_{\text{dip}}\cos\psi)$	$\frac{E}{3}V_{\text{dip}}\sin\psi$	$\frac{-E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{-E}{3}V_{\text{dip}}\sin\psi$
C	$\frac{E}{2}(1+V_{\text{dip}}\cos\psi)$	$\frac{E}{2}V_{\text{dip}}\sin\psi$	$\frac{E}{2}(1-V_{\text{dip}}\cos\psi)$	$\frac{E}{2}V_{\text{dip}}\sin\psi$
D	$\frac{E}{2}(1+V_{\text{dip}}\cos\psi)$	$\frac{E}{2}V_{\text{dip}}\sin\psi$	$\frac{-E}{2}(1-V_{\text{dip}}\cos\psi)$	$\frac{-E}{2}V_{\text{dip}}\sin\psi$
E	$\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$	$\frac{2E}{3}V_{\text{dip}}\sin\psi$	$\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{E}{3}V_{\text{dip}}\sin\psi$
F	$\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$	$\frac{2E}{3}V_{\text{dip}}\sin\psi$	$\frac{-E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{-E}{3}V_{\text{dip}}\sin\psi$
G	$\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$	$\frac{2E}{3}V_{\text{dip}}\sin\psi$	$\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$	$\frac{E}{3}V_{\text{dip}}\sin\psi$

where P_{dc} is the nominal input DC power and K is the ratio of the input power actually delivered to the DC-link. The current components are then transformed back into three-phase quantities in positive and negative-sequence frames and then into three-phase current using the Park transformation.

In the case of single-phase faults (dip types B and D) the maximum phase current (phase *a*) is calculated as

$$I_{\max}=\sqrt{\frac{2}{3}}\frac{KP_{\text{dc}}}{e_{dp}+e_{dn}} \tag{20}$$

while for two-phase faults (dip types C, E, F and G) the maximum phase current (phase *b*) is calculated as

$$I_{\max}=\sqrt{\frac{2}{3}}\frac{KP_{dc}}{e_{dp}^2-e_{dn}^2}\sqrt{\frac{1}{4}(e_{dp}-e_{dn})^2+\frac{3}{4}(e_{dp}+e_{dn})^2} \tag{21}$$

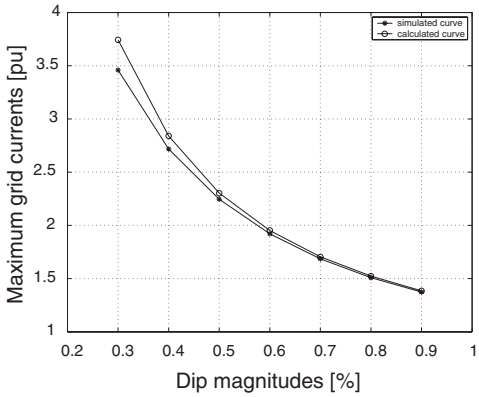

Figure 10. Maximum current for dip type C: simulated (asterisks) and calculated (circles)

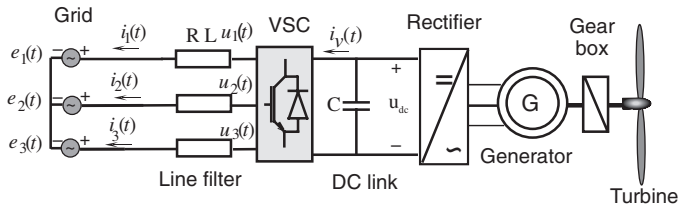

Figure 11. Wind turbine system

The values of $e_{d\mathrm{p}}$ and $e_{d\mathrm{n}}$, which are the positive and negative sequences of the d-component of the grid voltage respectively, are calculated using Table IV for different voltage dips (where E is the phase-to-phase RMS grid voltage, V_{dip} is the dip magnitude and ψ is the phase angle jump). Note that since the dips have zero phase angle jump, the d-components correspond to the magnitudes of their sequence voltages.

A comparison between the calculated and simulated maximum current values has been performed for all dip types. The calculated values are slightly overestimated, as shown in Figure 10 for dip type C. However, the error, which is mostly due to not considering the oscillating powers dissipated in the filter in the calculations, is considered acceptable. The overestimation gives a safety margin to the design.

Design Example

The system in Figure 4 is to be implemented in a wind turbine system (Figure 11) with turbine rated power 180 kW, turbine speed $\omega_{\mathrm{S}} = 42$ rpm, gearbox ratio 23.75 and blade radius $R = 11.5$ m. The mechanical efficiency of the turbine, C_{P}, which measures how efficiently the turbine converts the energy in the wind to electricity, has its largest value of 44% at a wind speed around 9 m s^{-1}.[9]

The conversion from wind speed to mechanical power is described by

$$P = \frac{\pi \rho \omega_{\mathrm{S}}^3 R^2}{2} C_{\mathrm{P}}(\omega_{\mathrm{S}}) \tag{22}$$

where ρ is the air density, which is set to 1.225 kg m^{-3}. Using the given data, the power curve for the turbine is obtained as in Figure 12. The power is expressed in per unit of the rated power of the turbine. The efficiency of the electrical generator is set to 100%. The wind variation of a typical site can be described using the Weibull distribution, as displayed in Figure 13, which shows the probability density for the wind speed at two sites

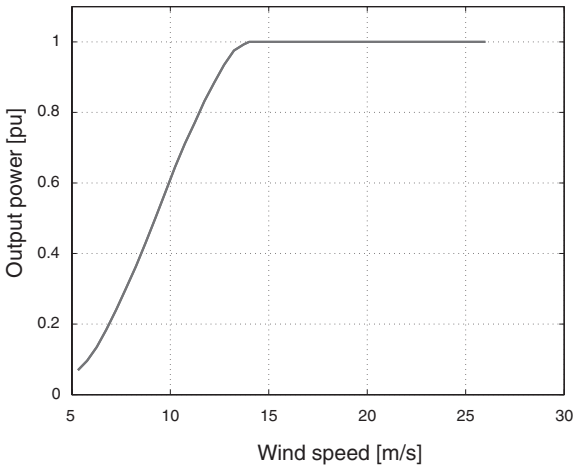

Figure 12. Electrical power output of turbine as a function of wind speed

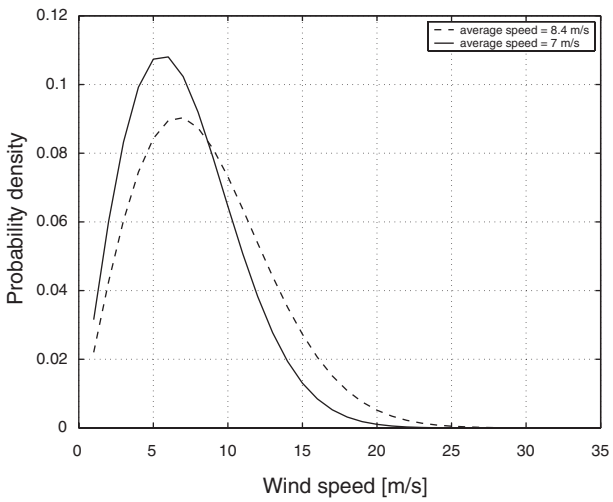

Figure 13. Weibull distribution for a site with average wind speed 8.4 m s^{-1} (broken line) and 7 m s^{-1} (full line)

with average speeds of 8.4 and 7 m s^{-1}, respectively. The shape parameter for the two curves is set to 2.[10] By integrating the probability density in Figure 13 and combining it with the power curve in Figure 12, the curve in Figure 14 is obtained. This represents the probability that a given maximum output power is produced.

Assume now that it is required to keep the system on-line for 80% of the time during a year. This means that the maximum power that can be obtained statistically is about 0.86 pu for a site with an average wind speed of 8.4 m s^{-1}. For a site with an average wind speed of 7 m s^{-1}, a maximum power of 0.61 pu is obtained. The maximum VSC currents for these two power levels for all unbalanced voltage dips are plotted in Figure 15.

From Figure 15 it is concluded that the VSC will stay in operation in the case of dips with magnitude higher than 80% for the first site and 50% for the second site. If the VSC must ride through all dips starting with magnitude higher than 30%, it must be rated 2.4 pu for the first site and about 1.8 pu for the second site. The same figures can be calculated using the design equations derived previously.

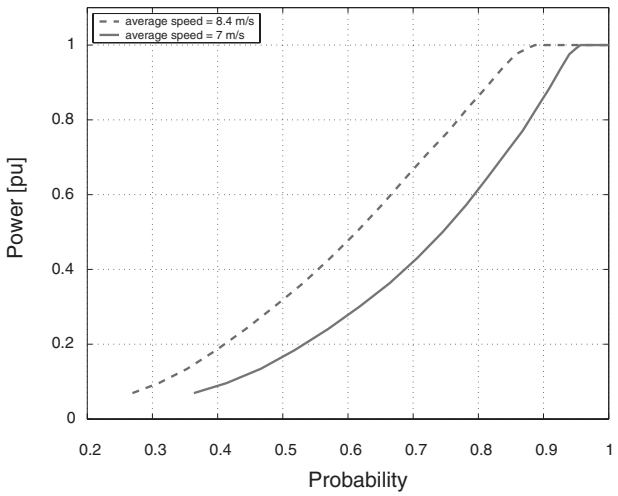

Figure 14. Probability of output power production from wind turbine

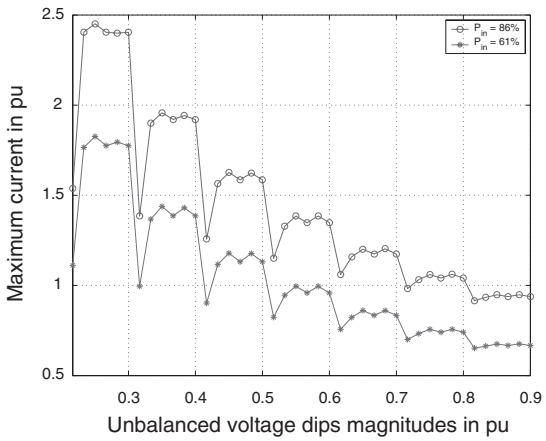

Figure 15. Maximum grid current for unbalanced voltage dips with magnitudes 0.3–0.9 pu with VSC input power P_{in} = 86% and 61%

By considering the statistical character of the wind power output, it becomes clear that, even without oversizing the VSC interface, some limited ride-through capability is ensured. However, if a higher ride-through capability is required, some overrating of the VSC will be necessary. This can be limited by accepting a certain risk of tripping (in the given example the risk would be 20%).

Conclusions

In this article, the design of a robust voltage source converter (VSC) interface for a wind turbine with a VSC has been investigated. The performance of the dual vector current controller (DVCC) has been presented for all unbalanced voltage dips that can occur at the point of connection of the wind turbine. Attention is focused

on the DC-link voltage ripple, which should be minimized, and on the maximum grid current during the dip, which determines the ride-through capability for the whole wind turbine system.

Based on the classification of unbalanced faults that can occur in the grid, resulting in voltage dips at the bus where the turbine is connected, the maximum current that the VSC must be able to withstand has been calculated. The effect of phase angle jumps during faults has also been investigated. It is demonstrated that, ultimately, the VSC design can be optimized by using statistics of wind speed distribution for the specific site considered. This is shown by a design example.

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Paper B

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Transient Performance of Voltage Source Converter under Unbalanced Voltage Dips

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***Abstract*- Robust operation of Voltage Source Converters under unbalanced voltage dips can be obtained by controlling the positive and negative-sequence currents separately with a Dual Vector Current Controller (DVCC). In this paper, the performance of the DVCC is investigated under all voltage dips that can affect the converter. Two different methods for taking into account the oscillating powers dissipated in the filter are presented, tested and compared. The effect of the phase-angle jump of the dip is also studied.**

***Index Terms*- Voltage Source Converter (VSC), current controller, voltage dip (sag), unbalance.**

I. Introduction

The three-phase Voltage Source Converter (VSC) is the basic component of most new FACTS and custom power equipment because of its good controllability and power quality. It is also used as interface to dispersed or distributed generation or in electric drive applications. In many of these applications, the voltage across the DC-link capacitor must be regulated.

A drawback of using VSC is its sensitivity to voltage disturbances, e.g. voltage dips. For a VSC, a sudden decrease in the grid voltage normally causes an increase in current, as the control attempts at maintaining the power to the DC-link constant, which can cause the VSC to trip to protect the valves. Moreover, most dips are due to unbalanced faults propagating in the grid. The resulting unbalanced voltages produce undesirable power oscillations of low order frequencies, which result in current harmonics and poor DC-link voltage regulation. The latter can also lead to tripping of the converter to avoid damage to the equipment due to DC overvoltage. In order to keep the VSC working adequately in these conditions, a robust control scheme should be developed.

A comparison between different types of vector current controllers (VCCs) for shunt connected VSC presented in [1] has proved that the Dual Vector Current Controller (DVCC) shows the best performance regarding grid currents and DC-link voltage during faults. This controller, which was first proposed in [2], uses two different VCCs for positive and negative sequence components, together with a DC-link voltage controller based on the instantaneous active and reactive power theory. However, in reference [2] the oscillating powers that are dissipated in the filter are neglected. In reference [3] these oscillating powers are considered compensated by the filter, but the performance of the controller is shown only in two unbalance cases. Moreover, both [2] and [3] only show results in steady-state conditions. When the VSC is subjected to voltage dips, the speed of response becomes critical. The method for sequence separation applied in [3] implies a delay of 2/3 of period, which will greatly impact the transient performance.

In this paper, the performance of the DVCC is investigated under all voltage dips that can affect the VSC. Two different methods for taking into account the oscillating powers dissipated in the filter are presented, tested and compared. The effect of the phase-angle jump of the dip is also studied.

II. Voltage Dips

A voltage dip is the voltage experienced at the end user terminals due to a short-circuit fault at a certain point in the electrical network. It can also happen due to motor starting or overloads. In spite of their short duration, between one cycle and several seconds, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [4] [5].

A. Voltage Dip Classification

The voltage dip classification defined by Bollen [6] and reported in Fig.1 has been used in this paper to quantify the unbalanced voltage dips at the VSC bus. The magnitude, indicated as E_{dip} or V_{dip}, is equal to the retained voltage for a single-phase dip. For a three-phase dip, the expressions of the three phase voltages for given dip magnitude and type are given in [6]. Due to a fault at bus 3 in Fig.2, a voltage dip occurs at bus 1, which can be balanced (due to a three-phase fault, and called type A), or of any of the six unbalanced types in Fig.1. According to the transformer (TRF) type, the dip that occurs at bus 1 may change from one type to another, as seen by the VSC connected at bus 2. This transformer can be: Type 1, which does not change anything to voltages (e.g. star grounded/star grounded); Type 2, which removes the zero-sequence voltage (e.g. Y/Y with at least one side not grounded or D/Z); Type 3, which swaps line and phase voltages (e.g. D/Y, Y/D, Y/Z). The transformation from one type to another is listed in Table 1. Since distribution transformers are often D/Y (Type 3), we normally find five types at the equipment terminals: Type A, due to three-phase faults; Type C and D, due to single-phase and double-phase faults; Type F and G, due to double-phase to ground faults. Note, however, that the load can in principle be subjected to dips of type B and E if the fault occurs at the same voltage level as the load or if the transformer is type 1.

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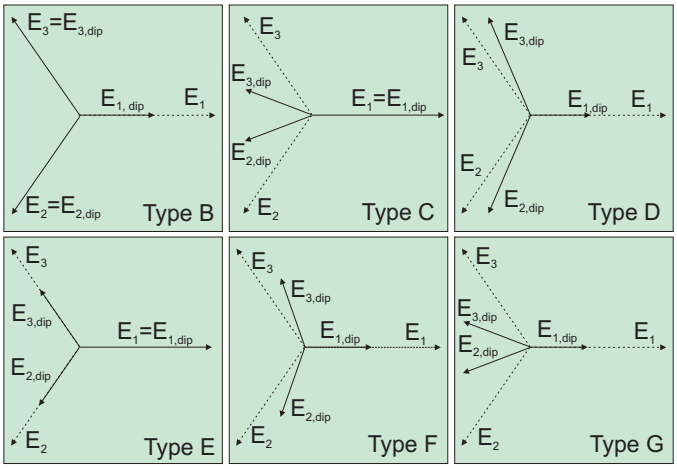

Fig.1. Voltage dip classification from B to G. Phasors of three phase voltage before (dotted) and during fault (solid) are displayed.

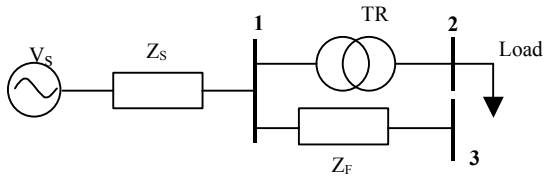

Fig.2. One-line model for dip analysis.

TABLE 1
TRANSFORMATION OF VOLTAGE DIPS THROUGH TRF

	Dip on the primary side						
Dip type	A	B	C	D	E	F	G
TRF type1	A	B	C	D	E	F	G
TRF type2	A	D*	C	D	G	F	G
TRF type3	A	C*	D	C	F	G	F

The superscript * indicates that the dip magnitude is equal to $\frac{1}{3}+\frac{2}{3}V_{dip}$.

B. Phase-angle jump

In Fig.2, if the X/R ratio for Z_S and Z_F is different, the voltage seen at the VSC terminals during the fault will have a different phase angle as compared to the pre-fault voltage. If the impedance angle α is defined as:

$$\alpha = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \quad (1)$$

where $Z_S = R_S + jX_S$, $Z_F = R_F + jX_F = zl$, z is the feeder impedance per unit length and l is the feeder length, the expression of the dip voltage at bus 1 will be:

$$v_{dip} = \frac{\lambda e^{j\alpha}}{1+\lambda e^{j\alpha}} = V_{dip}\angle\psi \quad (2)$$

where $\lambda e^{j\alpha} = zl / Z_S$, V_{dip} is the dip magnitude and ψ the "phase angle jump". In Fig.3 the relation between dip magnitude and phase angle jump for different impedance angles is shown.

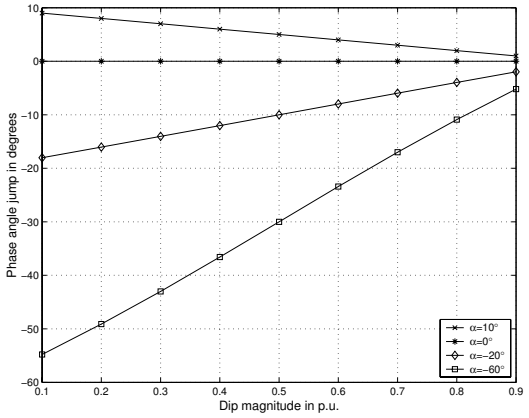

Fig.3. Phase angle jump for different dip magnitudes and impedance angles.

Four values for the angle α suggested by reference [6] are considered: 10^o as the highest expected value for transmission system faults, 0^o as the reference value, -20^o for overhead distribution lines, and -60^o for underground distribution cables. The phase angle jump is bigger for smaller dip magnitudes and is more significant when $\alpha = -60^o$.

III. INVESTIGATED SYSTEM

A scheme of the investigated system is shown in Fig.4. The VSC of rated power 69KVA is connected to the 400 V grid via a filter inductor. The DC side has a constant input DC current, while the DC voltage across the capacitor is regulated.

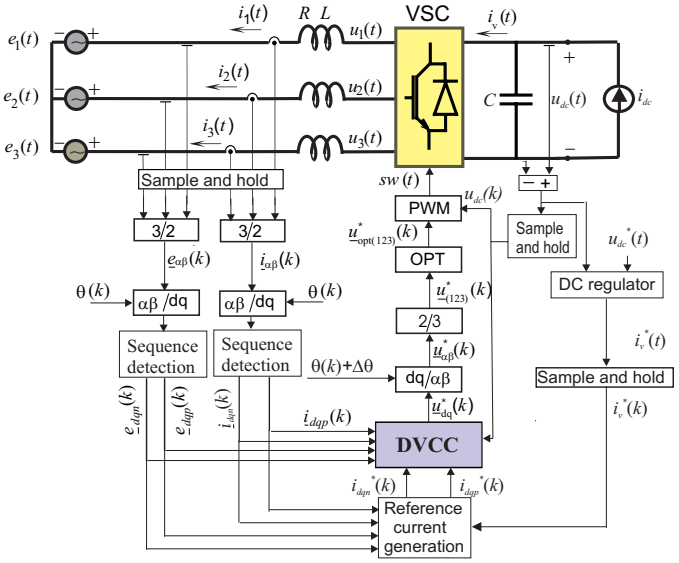

Fig.4. Scheme of investigated system.

The three-phase grid currents and voltages are sampled and transformed into vectors in the fixed $\alpha\beta$-frame and then into a rotating dq-frame synchronized with the grid voltage. This is done by using the transformation angle $\theta(k)$ obtained by using a PLL, which is assumed here to be slow and not to react during faults. The dq-components of currents and voltages are then separated into their positive and negative

sequence components, which are used along with the reference current signals in the DVCC to produce the reference voltage signals for the PWM modulator. The reference currents are produced by the "reference current generation algorithm" explained later, which uses the signal coming from the DC voltage regulator. The reference voltage signals in the *dq*-frame are transformed to three-phase quantities using the angle $\theta(k)+\Delta\theta(k)$, where $\Delta\theta(k)$ compensates for the error due to the calculation time. The three-phase control signals are then used in the PWM modulator to produce the switching pattern for the VSC. The PWM is optimized by adding a zero sequence voltage to the control signals in the block "OPT," in order to increase the maximum output voltage of the converter without increasing the DC-link voltage.

The different parts of the controller are described in more detail in the following.

A. Sequence detection

The decomposition of the supply voltage into positive and negative-sequence is performed in a *dq*-frame synchronised with the positive sequence (indicated as *dqp*), with the technique proposed in [7]. By delaying the *dq*-vector of the measured supply voltage by one fourth of the period *T* at the fundamental frequency, a vector composed of the same positive sequence component and a negative sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative sequence voltage will be removed. The positive sequence voltage component can thus be extracted from the measured values as

$$\underline{e}_{dqp} = \frac{1}{2}\left(\underline{e}_{dq}(t) + \underline{e}_{dq}\left(t - \frac{T}{4} \right) \right) \tag{3}$$

The negative sequence can be calculated as

$$\underline{e}_{dqn} = \frac{1}{2}\left(\underline{e}_{dq}(t) - \underline{e}_{dq}\left(t - \frac{T}{4} \right) \right) \tag{4}$$

The latter will be seen as a constant signal in the negative rotating plane *dqn*, which utilizes the opposite angle for the *dq*-transformation.

B. Implementing DVCC

The DVCC consists of two separate PI-controllers, for controlling the positive-sequence and the negative-sequence currents separately, as shown in Fig.5. The positive-sequence VCC is described for a sampling instant *k* in the *dqp*-frame by the following equation:

$$\begin{aligned} \underline{u}^{*}_{dqp}(k) = {} & \underline{e}_{dqp}(k) + R \cdot \underline{i}_{dqp}(k) + \mathrm{j}\omega L \cdot \underline{i}_{dqp}(k) + \\ & k_p \cdot \left(\underline{i}^{*}_{dqp}(k) - \underline{i}_{dqp}(k) \right) + \Delta \underline{u}_{I,dqp}(k) \end{aligned} \tag{5}$$

where $\underline{i}_{dqp}(k)$ is the positive sequence grid *dq*-current, $\underline{i}^{*}_{dqp}(k)$ is the positive sequence reference *dq*-current, k_p is the dead beat gain. The integration term $\Delta \underline{u}_{I,dqp}(k)$ is defined as

$$\Delta \underline{u}_{I,dqp}(k+1) = \Delta \underline{u}_{I,dqp}(k) + k_I \cdot \left(\underline{i}^{*}_{dqp}(k-1) - \underline{i}_{dqp}(k) \right) \tag{6}$$

With analogous notations, the negative sequence VCC is described by the following equation

$$\begin{aligned} \underline{u}^{*}_{dqp}(k) = {} & \underline{e}_{dqn}(k) + R \cdot \underline{i}_{dqn}(k) - \mathrm{j}\omega L \cdot \underline{i}_{dqn}(k) + \\ & k_p \cdot \left(\underline{i}^{*}_{dqn}(k) - \underline{i}_{dqn}(k) \right) + \Delta \underline{u}_{I,dqn}(k) \end{aligned} \tag{7}$$

and is implemented in the *dqn*-frame.

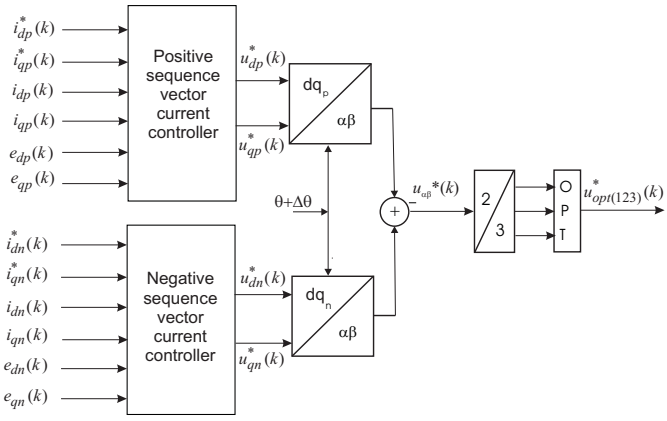

Fig.5. Simplified block scheme for DVCC.

C. DC-link voltage regulator

In many applications, e.g. drive systems and variable-speed wind turbines, the DC-link voltage cannot be considered constant. However, it should be regulated to insure correct operation of the VSC and to avoid damage to the power electronic switches and DC-link capacitor. Also the current to the DC-link is not constant. But its variations can be assumed to be much slower than the time range of the transient phenomena considered here. Therefore the DC-link is modeled as a capacitor with a current source in parallel.

A simple PI-controller is implemented, where the measured DC capacitor voltage u_{dc} is compared with its reference value u^{*}_{dc} and the error signal is used to produce a reference DC current signal i^{*}_{v} according to

$$i^{*}_{v} = -k_{pdc} \cdot \left(1 + \frac{1}{sT_{idc}} \right) \left(u^{*}_{dc} - u_{dc} \right) \tag{8}$$

where k_{pdc}, T_{idc} are the proportional gain and integral time constant of the DC PI-controller respectively, and *s* is Laplace operator.

D. Generation of current references

Proper current references should be generated in order to minimize the DC ripple and decrease the AC current

magnitude and harmonics content. Consider the apparent power from the grid

$$\underline{S}_g = \left(\underline{e}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{e}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)\cdot\left(\underline{i}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{i}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)^{conj} \quad (9)$$

which is the sum of a constant apparent power and two terms in sine and cosine, oscillating with double the grid frequency. By expanding Eq.(9), the following expression in matrix form can be written

$$\begin{bmatrix} P_g \\ Q_g \\ P_{s2g} \\ P_{c2g} \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \cdot \begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} \quad (10)$$

where P_g and Q_g are the constant active and reactive power, respectively, while P_{s2g} and P_{c2g} represent the second-harmonic sine and cosine component of the active power. These are the oscillating powers due to the unbalance in the grid voltages.

The apparent power at the converter terminals is

$$\underline{S}_{ac} = \left(\underline{u}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{u}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)\cdot\left(\underline{i}_{dqp}\mathrm{e}^{\mathrm{j}\omega t} + \underline{i}_{dqn}\mathrm{e}^{-\mathrm{j}\omega t}\right)^{conj} \quad (11)$$

and the following expression gives the power balance at the converter terminals

$$\underline{S}_{ac} = \underline{S}_g + \Delta\underline{S} \quad (12)$$

where ΔS is the apparent power dissipated in the filter. This contains also constant active and reactive power and two sine and cosine components oscillating with double the grid frequency. By substituting Eq.(12) in Eq.(11) and expressing the converter output voltages in terms of grid voltages by applying KVL, the following expressions for the active powers dissipated in the filter are obtained:

$$\Delta P = R\cdot\left(i_{dp}^2 + i_{qp}^2 + i_{dn}^2 + i_{qn}^2\right) \quad (13)$$

$$\Delta P_{c2} = 2R\left(i_{dp}\cdot i_{dn} + i_{qp}\cdot i_{qn}\right) + 2\omega L\left(i_{dp}\cdot i_{qn} - i_{qp}\cdot i_{dn}\right) \quad (14)$$

$$\Delta P_{s2} = 2R\left(i_{dp}\cdot i_{qn} - i_{qp}\cdot i_{dn}\right) + 2\omega L\left(-i_{dp}\cdot i_{dn} - i_{qp}\cdot i_{qn}\right) \quad (15)$$

where ΔP is the constant term of the active power dissipated in the filter, while ΔP_{c2} and ΔP_{s2} are the cosine and sine oscillating components of the active power, respectively. The current references are then calculated by nullifying Q_g, to achieve average unity power factor. The converter losses are neglected, so that $P_{ac} = P_{dc}$ which is the DC-link power.

Two different methods are used here for considering the oscillating powers. In the first case (Case I), the DC side of the converter supplies the oscillating power to the filter, which means that the oscillating power is set to zero on the grid side, i.e. $P_{c2g} = P_{s2g} = 0$. The reference currents from Eq.(10) can thus be expressed as:

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (16)$$

In the second case (Case II), the oscillating powers flow from the grid into the filter, i.e. the oscillating powers are forced to zero at the converter terminals, $P_{c2g} = -\Delta P_{c2}$ and $P_{s2g} = -\Delta P_{s2}$. The reference currents for the DVCC are

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ 0 \\ -\Delta P_{s2} \\ -\Delta P_{c2} \end{bmatrix} \quad (17)$$

In both Eq.(16) and Eq.(17), the filter powers are non-linear combinations of the grid currents. This can be solved on line with mathematical iterative methods as done in [3]. However, this will make the controller quite complex and increase the calculation time. Here, the actual values of the grid currents sampled one time step back are used.

IV. Simulation Results

To test the controller, simulations have been run with all six unbalanced dip types mentioned previously and with magnitudes varying from 0.1 pu to 0.9 pu in steps of 0.1 pu using Matlab/Simulink for the two algorithms mentioned as case I and case II. System data and main controller data are shown in Table 2 and, respectively.

If only one VCC implemented in the *dqp*-frame is used, current harmonics appear during faults, as shown in Fig. 6 for a dip type C with magnitude 40%. This is due to the negative sequence component in the unbalanced grid voltage, which also causes ripple in the DC-link voltage, also shown in Fig. 6, equal to 6.5%. Separating the sequences and using the algorithm of case I to generate the current references smoothes out the currents, as shown in Fig. 7. However, the DC side supplies the oscillating powers and the DC ripple increases to 20%. With the oscillating powers supplied by the grid in case II, the DC voltage is significantly smoothed out, apart from the transients at the beginning and end of the dip, see Fig. 8. The currents are almost the same in magnitude in both cases, however they are more smoothed in case II.

TABLE 2
SYSTEM DATA

Constant	Symbol	Actual value	Value in pu
Nominal line AC voltage	E	400 V	1.0
Nominal phase current	I_n	100 A	1.0
Nominal grid frequency	f_n	50 Hz	
Nominal DC-link voltage	U_{dc}	650 V	1.0 (dc)
Nominal DC input current	I_{dc}	107 A	1.0 (dc)
Filter resistance	R	23 mΩ	0.01
Filter inductance	L	0.73 mH	0.1
DC link capacitance	C	550 µF	τ=1.7 ms

TABLE 3
MAIN CONTROLLER DATA

Constant	Symbol	Value
Sampling frequency	f_S	5 kHz
Sampling time	T_S	200 µs
Proportional gain (dead-beat)	K_P	$L/T_S + R/2 = 3.7$
Integration time constant	T_i	0.03 s

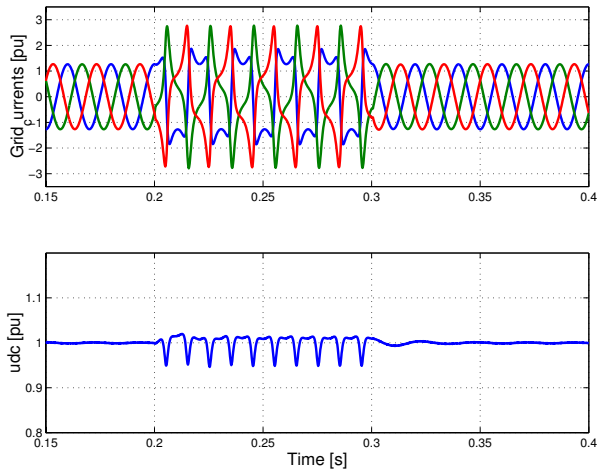

Fig. 6 Grid currents (top) and DC voltage (bottom) for 40% dip type C, with VCC.

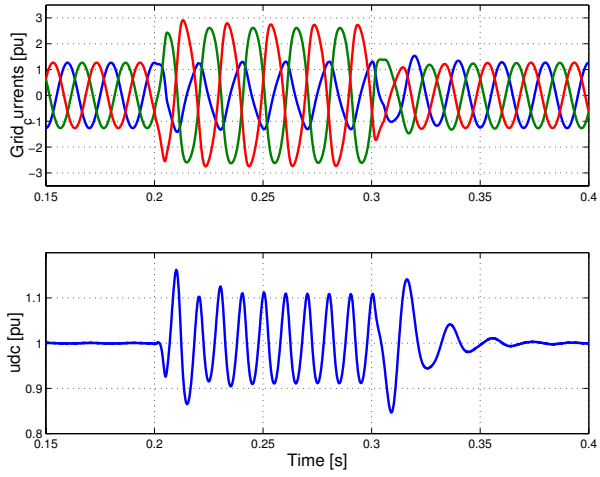

Fig. 7 Grid currents (top) and DC voltage (bottom) for 40% dip type C, with DVCC in case I.

The effect of all types of dips in both cases, with magnitude between 0.3 and 0.9 pu, on the maximum grid current and peak-to-peak DC-voltage ripple measured in the middle of the dip is represented in Fig. 9. The maximum current the valves should be able to hold is reduced in case II to 3.65 pu. The maximum DC voltage ripple is about ± 1.6 V around the nominal value. The maximum DC voltage ripple during the transient for all dips is less than 1.1 pu for case II, compared to about 1.13 pu in case I. The required rating of the converter is reduced in case II and also the performance of the system is improved.

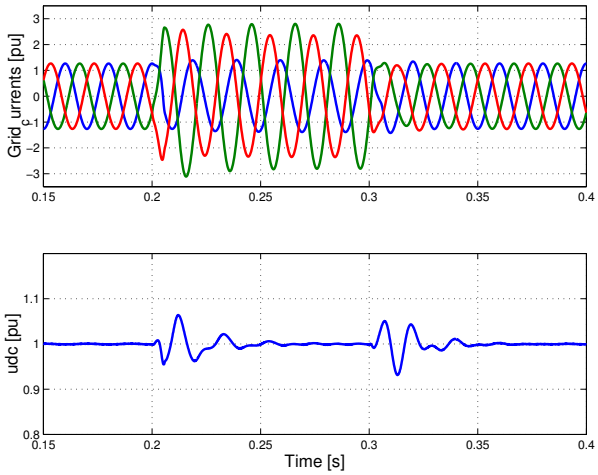

Fig. 8 Grid currents (top) and DC voltage (bottom) for 40% dip type C, with DVCC in case II.

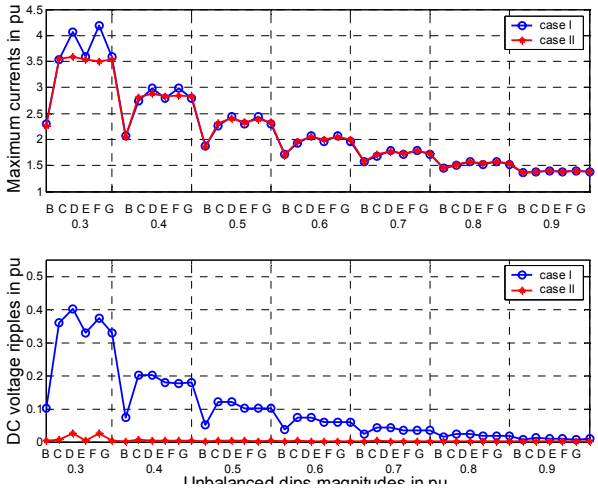

Fig. 9 Maximum grid current (top) and DC voltage ripple (bottom) in pu for different unbalanced dip types and magnitudes between 0.3 and 0.9 for case I (circle marked) and case II (asterisk marked).

V. EFFECT OF PHASE ANGLE JUMP

The system is further examined considering the phase angle jump. Four values of the impedance angles α specified in [6], which are 10°, 0, −20° and −60°, are used in the simulations. For 40% dip type C, Fig. 10 show that changing the phase angle jump has a negligible effect on the DC-voltage ripples. The effect of various phase angle jumps for the different unbalanced dip types and different impedance angles has been simulated and shown in Fig. 11. The dip magnitude increases for each dip type going from left to right. The phase angle jump appears to have more effect on the maximum grid currents in case of smaller dip magnitudes There is practically no difference for α = 0°, +10°, or −20°, but a significant increase in current occurs when α equals −60°. In that case the maximum current, with 30% magnitude of dip type D, is equal to 4.5 pu. This is significantly higher than in case of zero phase-angle jump (3.65 pu). If the converter switches are designed for a minimum dip magnitude considering the case of zero phase angle jump, they will be damaged if the same dip with a significant phase angle jump occurs.

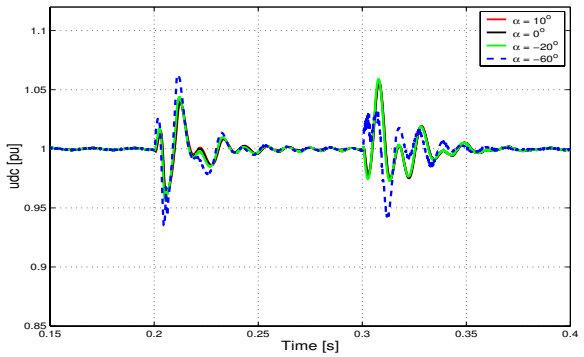

Fig. 10 DC ripple in pu for a 40% dip types C, $\alpha = 10^o, 0^o, -20^o, -60^o$.

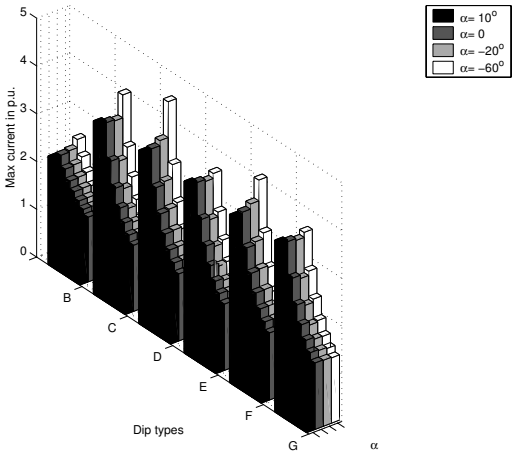

Fig. 11 Effect of phase angle jump on amplitude of phase currents for different unbalanced dips each from 30% to 90% dip magnitude.

VI. Conclusion

In this paper, the transient performance of a voltage source converter subject to unbalanced voltage dips has been treated. The Dual Vector Current Controller (DVCC) has been implemented and tested exhaustively through simulations of all voltage dips that can occur at the converter terminals.

Two methods for generation of the current references have been implemented and compared, in which the instantaneous active and reactive powers are controlled at the grid side and the converter terminals, respectively. In the latter case, it has been shown that the grid currents are slightly decreased and the DC voltage is significantly smoothed out.

Dips with significant phase angle jumps, corresponding to an impedance angle $\alpha = -60^o$, are characterized by an increase of maximum grid currents and DC-link voltage ripple, and this effect is more significant at lower dip magnitudes. This effect should be taken into account when designing converters with high ride-through capability for voltage dips.

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Paper C

F. Magueed, J. Svensson, and A. Sannino, "Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage conditions," in *Proc of Power Tech Conference (PT'05)*, St. Petersburg, Russia, June 27-30, 2005.

Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage Conditions

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***Abstract*-- Grid-connected voltage source converters (VSC's) are used in many applications with power quality concerns due to good controllability and output power quality. However, the major drawback is their sensitivity to grid disturbances, e.g. voltage dips. Moreover, when VSCs are used in distributed generation (DG) applications, voltage imbalance may be intolerant. The VSC may trip due to current imbalance or due to overcurrent. In this paper, dual vector current controller is adopted for the VSC connected to the grid through LCL-filter to achieve sinusoidal grid currents with no harmonics and smooth DC-link voltage during voltage dips. The LCL-filter resonance is damped by adjusting the controller gain. Proper current references are generated using a signal command from the DC-link voltage controller and compensates for oscillating powers produced in fault cases. The controller is examined for all types of unbalanced dips.**

***Index Terms*-- DG, LCL-filter, power quality, VSC, vector current control, voltage dips.**

I. Introduction

Integration of Distributed Generation (DG) in the utility grid offers a number of technical, environmental and economical benefits, both from the utility and the end-user point of view ([1], [2], and [3]), and is therefore becoming more and more popular. In variable-speed wind turbines, like many other DG technologies, a power-electronic interface is used to connect the DG system to the utility grid. This power electronics interface usually comprises a current-controlled voltage source converter (VSC), which has the advantages of good controllability (controls active and reactive power independently) and power quality (no low-frequency harmonics). The grid-connected VSC is used to control the active power flow to the grid by keeping the DC-link voltage constant independently of the operation of the generation part of the DG. This is done by using a cascade controller, where the outer-loop controller tracks the DC-link voltage reference and sets the reference current to the inner vector-current controller, which controls the instantaneous active and reactive current.

The drawback of using VSCs is their sensitivity to voltage disturbances, e.g. voltage dips. A voltage dip is a short duration drop in voltage that is normally due to a fault [4]. For a VSC, a sudden decrease in grid voltage normally causes an increase in current, as the control attempts at maintaining the power to the DC link constant. This can lead to tripping of the VSC because of over-current, in order to protect the valves. Moreover, most faults are unbalanced and result in unbalanced dips, which produce undesirable power oscillations of low-order frequencies resulting in current harmonics and poor DC-link voltage regulation [5]. Ultimately, this can also lead to tripping of the VSC due to DC over-voltage. When a large amount of DGs are installed in the grid it becomes unacceptable to disconnect generating units every time a disturbance occurs. Hence, a robust controller should be developed to enhance the transient performance of a DG.

In references [4], [5], and [6] investigations have been carried out in order to improve the controllability of the VSC connected to the grid through L-filter for unbalanced voltages of the grid. Dual vector current controller (DVCC) has proved to perform adequately concerning the grid current. An advanced DC-link voltage controller has been introduced in order to reduce the voltage ripple on the DC-link when running the VSC on unbalanced grids.

However, to eliminate the grid current harmonics an LCL-filter is inserted between the grid and the VSC due to its higher attenuation ability of current harmonics at higher frequencies compared with the L-filter. Implementing LCL- filter may lead to instability problem that could occur at the resonance frequency of the filter. Damping methods are extensively addressed in literature [7]-[12], where the high gain at the resonance frequency of the filter is either passively or actively damped. In passive damping method, a resistor is connected in series with the filter capacitor. Although this method is easy to implement, it increases the system losses and decreases the efficiency of the filter. Instead, methods to actively damp the resonance are adopted ([8], [11] and [12]), which increases the control system complexity.

In this paper, the DVCC is adopted for the VSC connected to the grid through LCL-filter to achieve sinusoidal grid currents with no harmonics and smooth DC-link voltage during different voltage dips. The LCL-filter resonance is damped by

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adjusting the cascaded controller gains. Proper current references are generated using a signal command from a DC-link voltage controller and compensating for the oscillating powers produced in fault cases. The controller is examined for all types of unbalanced dips.

II. System Description

A scheme of the investigated system using VSC with LCL-filter is shown in Fig. 1. The generating part of the DG is modeled by a constant DC current source, while the DC voltage across the capacitor is regulated. The system data are shown in Table 1 and the filter parameters are shown in Table 2.

The grid currents and voltages, the VSC currents, the capacitor voltages and the DC-link voltage are measured and fed into the cascaded controller. The outer controller (PI1) tracks the reference current of the grid i_2^* and the output is the reference capacitor voltage u_c^*, which is the reference for the second controller (P2). In P2 the measured capacitor voltage u_c is compared with the reference command using a proportional controller, which produces the reference current i_1^* for the third controller (P3). The third controller is also a proportional controller, which output is the reference voltage u^* to the PWM-block to generate the proper switching pattern (SW_{123}) necessary for the operation of the VSC.

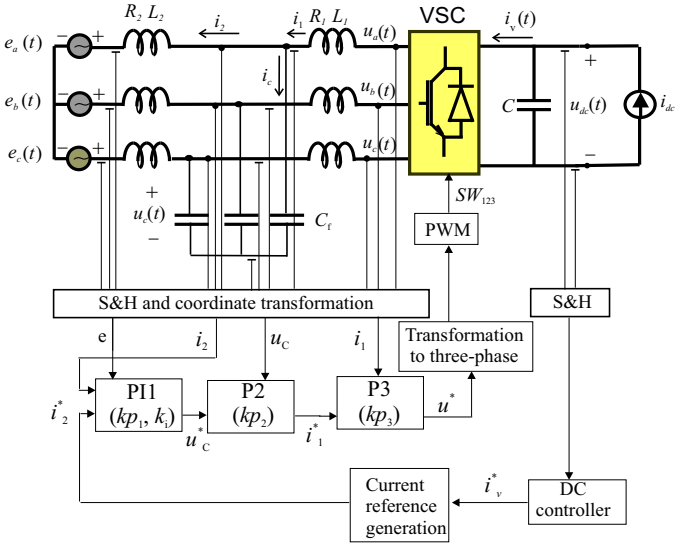

Fig. 1 Investigated system schematic diagram.

The controller equations in *dq*-frame, which is synchronized with the grid voltage by a PLL, are derived. A time delay of one sample is considered in the inner controller (P3) to model the inherited time delay resulting from the calculation time in practical systems and an integral part is used in the outer controller (PI1) to eliminate steady-state error.

TABLE 1
SYSTEM DATA

Description	Symbol	Value
Nominal (base) rms phase-to-phase AC voltage	E	400 V
Nominal (base) rms phase current	I_n	100 A
Nominal (base) grid frequency	f_n	50 Hz
Nominal (base) DC link voltage	U_{dc}	650 V
Nominal (base) DC input current	I_{dc}	107 A
DC link capacitance	C	550 µF

TABLE 2
FILTER PARAMETERS

Description	Parameter	Value
VSC-side inductance	L_1	0.52 mH
VSC-side resistance	R_1	1.6 mΩ
Grid-side inductance	L_2	0.2 mH
Grid-side resistance	R_2	0.6 mΩ
Filter capacitance	C_f	137.83 µF

The controller equations are:

$$\underline{u}_{cdq}^*(k) = \underline{e}_{dq}(k) + (R_2 + j\omega L_2)\underline{i}_{2dq}(k) + kp_1\left(\underline{i}_{2dq}^*(k) - \underline{i}_{2dq}(k)\right) + \underline{\Delta u}_{idq}(k) \quad (1)$$

$$\underline{i}_{1dq}^*(k) = \underline{i}_{2dq}(k) + j\omega C_f \underline{u}_{cdq}(k) + kp_2\left(\underline{u}_{cdq}^*(k) - \underline{u}_{cdq}(k)\right) \quad (2)$$

$$\underline{u}_{dq}^*(k+1) = \underline{u}_{cdq}(k) + (R_1 + j\omega L_1)\underline{i}_{1dq}(k) + kp_3\left(\underline{i}_{1dq}^*(k) - \hat{\underline{i}}_{1dq}(k)\right) \quad (3)$$

where $\underline{e}_{dq}$ is the grid voltage vector, kp_1, kp_2, and kp_3 are the controller proportional gains that are fractions of the corresponding dead-beat gains, k_{DB1}, k_{DB2}, and k_{DB3}, as explained by the following equations:

$$kp_1 = k_1 k_{DB1} = k_1\left(\frac{L_2}{T_s} + \frac{R_2}{2}\right)$$
$$kp_2 = k_2 k_{DB2} = k_2\left(\frac{C_f}{T_s}\right) \quad (4)$$
$$kp_3 = k_3 k_{DB3} = k_3\left(\frac{L_1}{T_s} + \frac{R_1}{2}\right)$$

where T_s is the sampling time. The integral part is calculated as:

$$\underline{\Delta u}_{idq}(k+1) = \underline{\Delta u}_{idq}(k) + k_i\left(\underline{i}_{2dq}^*(k-1) - \underline{i}_{2dq}(k)\right) \quad (5)$$

where k_i is the integrator gain.

Predicting the VSC current one sample ahead instead of

using the delayed measured current in P3 compensates for the time delay. The predicted current equation is:

$$\hat{\underline{i}}_{1dq}(k+1)=\frac{T_s}{L_1}\left(\underline{u}^*_{dq}(k)-\underline{u}_{cdq}(k)\right)+\left(1-\frac{R_1}{L_1}-j\omega T_s\right)\hat{\underline{i}}_{1dq}(k)$$
$$+kp_s\left(\underline{i}_{1dq}(k)-\hat{\underline{i}}_{1dq}(k-1)\right) \quad (6)$$

where kp_s is a proportional gain that compensates for the error between the actual and the estimated current.

Theoretically, choosing dead-beat gains for the controller should result in fast transient response. However, this is not possible in cascaded controllers, since the operation of the controllers should be decoupled. In another sense, the voltage reference (output of P3) is not modified after one sample and then the actual grid current is not able to follow its reference within one sample. To choose the proper gains, the stability of the complete system has been examined looking at the pole locations on the unit disc, shown in Fig. 2. The two poles near the upper bound of the unit disc (and their conjugates at the lower bound) are fast moving poles depending on the gain of P3. They move into the unit disc as kp_3 takes values less than 30% of the dead-beat gain. However, increased values of kp_3 decrease the peak value in the gain from grid voltage to grid-side current (i_{2d}/e_d in Fig. 3) insuring proper transient response at high frequencies. Hence, a trade-off should be considered to choose the controller gains. The transient response for the controller, using the gains that are reported in Table 3, is shown in Fig. 4. The settling time in i_{2d} is about 0.02 s for a step in the active component of the reference current i^*_{2d}, while it is about 0.015 s for a step in the active component of the grid voltage e_d. Moreover, the effect of a step in i^*_{2d} over i_{2q}, which is called the cross-coupling effect, is negligible.

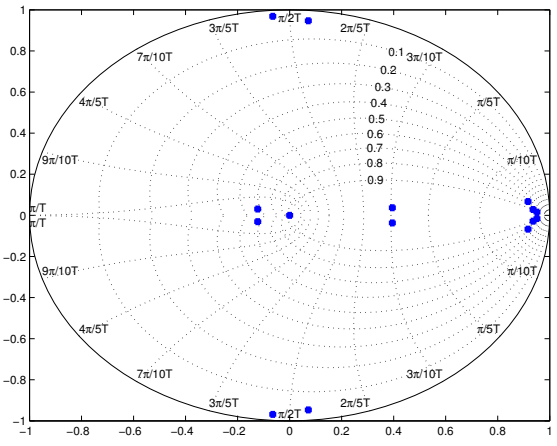

Fig. 2 System poles.

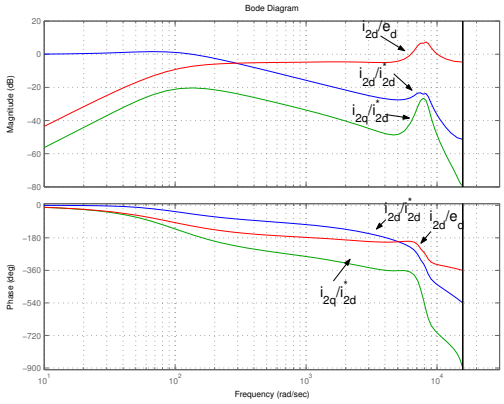

Fig. 3 Bode plot for the controller.

TABLE 3
CONTROLLER PARAMETERS

kp_1	k_{DB1}	kp_s	0.5
T_i	10 ms	f_s	5 kHz
kp_2	k_{DB2}	k_{pdc}	0.2
kp_3	$0.2k_{DB3}$	T_{idc}	5 ms

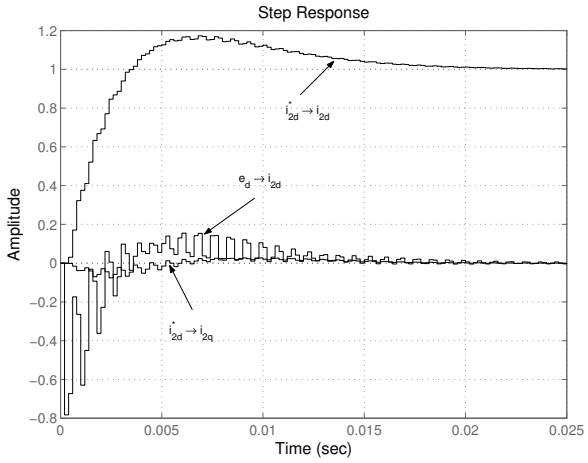

Fig. 4 Transient response for the controller.

III. VOLTAGE DIPS

A voltage dip is the voltage experienced at the end user terminals due to a short-circuit fault at a certain point in the electrical network. It can also happen due to motor starting or overloads. In spite of their short duration, between one cycle and several seconds, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [13], [14].

The voltage dip classification defined by Bollen [20] and reported in Fig.5 has been used in this paper to quantify the unbalanced voltage dips at the VSC bus. The magnitude, indicated as E_{dip} or V_{dip}, is equal to the retained voltage for a single-phase dip. For a three-phase dip, the expressions of the three phase voltages for a given dip magnitude and type are given in [20]. Due to a fault at bus 3 in Fig. 6, a voltage dip

occurs at bus 1, which can be balanced (due to a three-phase fault, and called type A), or of any of the six unbalanced types in Fig.5. According to the transformer (TR) type, the dip that occurs at bus 1 may change from one type to another, as seen by the VSC connected at bus 2. This transformer can be: Type 1, which does not change anything to voltages (e.g. star grounded/star grounded); Type 2, which removes the zero-sequence voltage (e.g. Y/Y with at least one side not grounded or D/Z); Type 3, which swaps line and phase voltages (e.g. D/Y, Y/D, Y/Z). The transformation from one type to another is listed in Table 4. Since distribution transformers are often D/Y (Type 3), we normally find five types at the equipment terminals: Type A, due to three-phase faults; Type C and D, due to single-phase and double-phase faults; Type F and G, due to double-phase to ground faults. Note, however, that the load can in principle be subjected to dips of type B and E if the fault occurs at the same voltage level as the load or if the transformer is type 1.

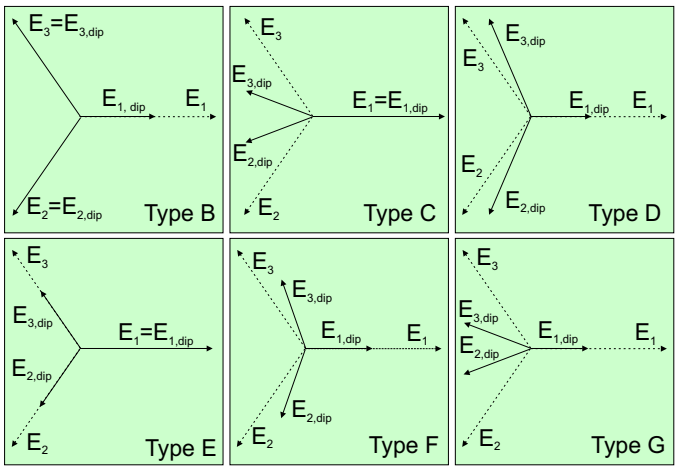

Fig.5. Voltage dip classification from B to G. Phasors of three phase voltage before (dotted) and during fault (solid) are displayed.

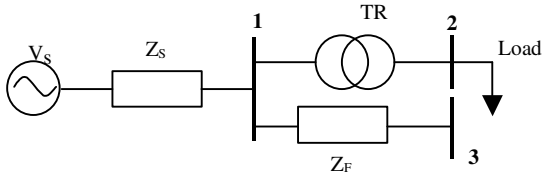

Fig. 6 One-line model for dip analysis.

TABLE 4
TRANSFORMATION OF VOLTAGE DIPS THROUGH TR

	Dip on the primary side						
Dip type	A	B	C	D	E	F	G
TRF type1	A	B	C	D	E	F	G
TRF type2	A	D*	C	D	G	F	G
TRF type3	A	C*	D	C	F	G	F

The superscript * indicates that the dip magnitude is equal to $\frac{1}{3}+\frac{2}{3}V_{dip}$.

IV. PERFORMANCE DURING UNBALANCED VOLTAGE DIPS

To examine the performance of the controller in case of unbalanced voltage dips on the grid side, proper current references should be generated. The active current reference should be produced in such a way to keep the DC-link voltage constant. Hence, the current reference generation block in Fig. 1 is commanded using the output signal of the DC-link voltage controller.

A. DC-link voltage controller

In many applications, e.g. drive systems and variable-speed wind turbines, the DC-link voltage cannot be considered constant. However, it should be regulated to insure correct operation of the VSC and to avoid damage to the power electronic switches and DC-link capacitor. Also the current to the DC-link is not constant. But its variations can be assumed to be much slower than the time range of the transient phenomena considered here. Therefore the DC-link is modeled as a capacitor with a current source in parallel.

A simple PI-controller is implemented, where the measured DC capacitor voltage u_{dc} is compared with its reference value u_{dc}^{*} and the error signal is used to produce a reference DC current signal i_{v}^{*} according to

$$i_{\mathrm{v}}^{*}=-k_{\mathrm{pdc}}\cdot\left(1+\frac{1}{sT_{\mathrm{idc}}}\right)\left(u_{\mathrm{dc}}^{*}-u_{\mathrm{dc}}\right) \tag{7}$$

where k_{pdc}, T_{idc} are the proportional gain and integral time constant of the DC PI-controller respectively, and s is Laplace operator.

B. Current reference generation

The current references are then generated to keep power balance through the system, neglecting the power loss in VSC switches. The power at the VSC side is:

$$S_1=\underline{u}_{\mathrm{dq}}\underline{i}_{\mathrm{1dq}}^{\mathrm{conj}} \tag{8}$$

which is expanded as follows:

$$S_1=u_{\mathrm{d}}i_{\mathrm{1d}}+u_{\mathrm{q}}i_{\mathrm{1q}}+\mathrm{j}\left(u_{\mathrm{q}}i_{\mathrm{1d}}-u_{\mathrm{d}}i_{\mathrm{1q}}\right) \tag{9}$$

Applying KVL and KCL, we get:

$$\underline{u}_{\mathrm{dq}}=\underline{e}_{\mathrm{dq}}+R_1\underline{i}_{\mathrm{1dq}}+\mathrm{j}\omega L_1\underline{i}_{\mathrm{1dq}}+R_2\underline{i}_{\mathrm{2dq}}+\mathrm{j}\omega L_2\underline{i}_{\mathrm{2dq}} \tag{10}$$

$$\underline{i}_{\mathrm{1dq}}=\underline{i}_{\mathrm{2dq}}+\mathrm{j}\omega C_{\mathrm{f}}\underline{u}_{\mathrm{cdq}} \tag{11}$$

Substituting in (9) and expressing the equation in matrix form:

$$\begin{bmatrix}P_1\\Q_1\end{bmatrix}=\begin{bmatrix}e_{\mathrm{d}} & e_{\mathrm{q}}\\ e_{\mathrm{q}} & -e_{\mathrm{d}}\end{bmatrix}\begin{bmatrix}i_{\mathrm{2d}}\\ i_{\mathrm{2q}}\end{bmatrix}+\begin{bmatrix}\Delta P(i)\\ \Delta Q(i)\end{bmatrix}+\begin{bmatrix}\Delta P(e)\\ \Delta Q(e)\end{bmatrix}$$

where, P_1 and Q_1 are active and reactive powers at the VSC

side, $\Delta P(i)$ and $\Delta Q(i)$ are active and reactive powers consumed in the filter inductors and expressed as functions in grid-current and VSC-current, and $\Delta P(e)$ and $\Delta Q(e)$ are active and reactive powers consumed by the filter capacitor and expressed as function in the grid voltage.

To achieve zero reactive power at the grid, Q_1 should supply the reactive power consumed by the filter. In equation:

$$Q_1 = \Delta Q(i) + \Delta Q_c \tag{12}$$

where ΔQ_c is the power loss in the filter capacitor, it is calculated as:

$$\Delta Q_c = \omega C_f \left(u_{cd}^2 + u_{cq}^2\right) \tag{13}$$

Moreover, neglecting the switching losses, the active power at the VSC side is considered equal to the power at the DC side. The current references are then generated as:

$$\begin{bmatrix} i_{2d}^* \\ i_{2q}^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} u_{dc} i_v^* - \Delta P(i) \\ \Delta Q_c \end{bmatrix} - \begin{bmatrix} -\omega C_f u_{cq} \\ \omega C_f u_{cd} \end{bmatrix} \tag{14}$$

where

$$\begin{aligned} \Delta P(i) = {} & R_1 \left(i_{1d}^2 + i_{1q}^2\right) + R_2 \left(i_{1d} i_{2d} + i_{1q} i_{2q}\right) \\ & + \omega L_2 \left(-i_{1d} i_{2q} + i_{1q} i_{2d}\right) \end{aligned} \tag{15}$$

C. Performance

The controller that has been described above has been examined in case of unbalanced voltage dips. A dip, resulting from two-phase fault (dip type C), is applied at the grid side. The dip starts at 0.2 s for duration of 0.1s with a remaining voltage of 40%. The grid currents are distorted during the dip, as shown in Fig. 7, and the DC-link voltage contains about 20% peak-to-peak ripples.

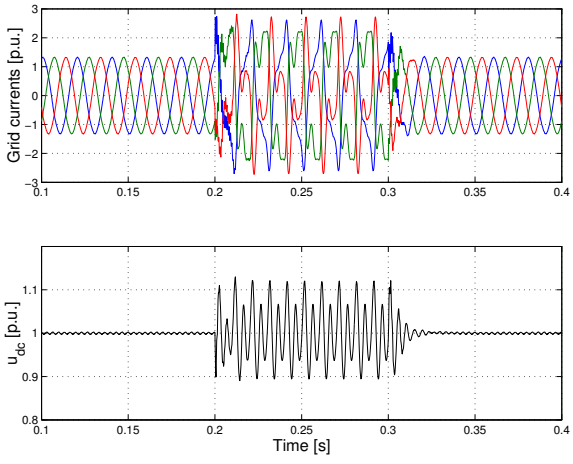

Fig. 7 Grid currents (upper) and DC-link voltage (lower) in case of voltage dip.

V. Dual Vector Current Controller (DVCC)

To improve the transient response during voltage dips, DVCC is implemented. It consists of two separate controllers for controlling the positive and negative sequences.

The decomposition of the supply voltage (and all measured signals) into positive and negative-sequence is performed in the *dq*-frame synchronized with the positive sequence (indicated as *dqp*), with the technique proposed in [21]. By delaying the *dq*-vector of the measured supply voltage by one fourth of the period T at the fundamental frequency, a vector composed of the same positive sequence component and a negative sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative sequence voltage will be removed. The positive sequence voltage component can thus be extracted from the measured values as

$$\underline{e}_{dqp} = \frac{1}{2}\left(\underline{e}_{dq}(t) + \underline{e}_{dq}\left(t - \frac{T}{4}\right)\right) \tag{16}$$

The negative sequence can be calculated as

$$\underline{e}_{dqn} = \frac{1}{2}\left(\underline{e}_{dq}(t) - \underline{e}_{dq}\left(t - \frac{T}{4}\right)\right) \tag{17}$$

The latter will be seen as a constant signal in the negative rotating plane *dqn*, which utilizes the opposite angle for the *dq*-transformation.

Equations (1) to (3) are then expressed in the positive sequence frame (*dqp*-frame) and negative sequence frame (*dqn*-frame) as follows:

$$\begin{aligned} \underline{u}_{cdqp}^*(k) = {} & \underline{e}_{dqp}(k) + (R_2 + j\omega L_2)\underline{i}_{2dqp}(k) \\ & + kp_1\left(\underline{i}_{2dqp}^*(k) - \underline{i}_{2dqp}(k)\right) + \underline{\Delta u}_{idqp}(k) \end{aligned} \tag{18}$$

$$\begin{aligned} \underline{u}_{cdqn}^*(k) = {} & \underline{e}_{dqn}(k) + (R_2 - j\omega L_2)\underline{i}_{2dqn}(k) \\ & + kp_1\left(\underline{i}_{2dqn}^*(k) - \underline{i}_{2dqn}(k)\right) + \underline{\Delta u}_{idqn}(k) \end{aligned} \tag{19}$$

$$\begin{aligned} \underline{i}_{1dqp}^*(k) = {} & \underline{i}_{2dqp}(k) + j\omega C_f \underline{u}_{cdqp}(k) \\ & + kp_2\left(\underline{u}_{cdqp}^*(k) - \underline{u}_{cdqp}(k)\right) \end{aligned} \tag{20}$$

$$\begin{aligned} \underline{i}_{1dqn}^*(k) = {} & \underline{i}_{2dqn}(k) - j\omega C_f \underline{u}_{cdqn}(k) \\ & + kp_2\left(\underline{u}_{cdqn}^*(k) - \underline{u}_{cdqn}(k)\right) \end{aligned} \tag{21}$$

$$\begin{aligned} \underline{u}_{dqp}^*(k+1) = {} & \underline{u}_{cdqp}(k) + (R_1 + j\omega L_1)\underline{i}_{1dqp}(k) \\ & + kp_3\left(\underline{i}_{1dqp}^*(k) - \hat{\underline{i}}_{1dqp}(k)\right) \end{aligned} \tag{22}$$

$$\underline{u}^{*}_{\mathrm{dqn}}(k+1)=\underline{u}_{\mathrm{cdqn}}(k)+(R_1-\mathrm{j}\omega L_1)\underline{i}_{\mathrm{1dqn}}(k)+kp_3\left(\underline{i}^{*}_{\mathrm{1dqn}}(k)-\underline{\hat{i}}_{\mathrm{1dqn}}(k)\right) \tag{23}$$

A. *Current reference generation*

The power at the VSC side is expressed as:

$$S_1=\left(e^{\mathrm{j}\omega t}\underline{u}_{\mathrm{dqp}}+e^{-\mathrm{j}\omega t}\underline{u}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{\mathrm{1dqp}}+e^{-\mathrm{j}\omega t}\underline{i}_{\mathrm{1dqn}}\right)^{\mathrm{conj}} \tag{24}$$

Expressing (10) and (11) in *dqp-* and *dqn-* frames, and substituting in (24) results in the following matrix to generate the current references:

$$\begin{bmatrix} i^{*}_{2\mathrm{dp}} \\ i^{*}_{2\mathrm{qp}} \\ i^{*}_{2\mathrm{dn}} \\ i^{*}_{2\mathrm{qn}} \end{bmatrix}=\begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qp}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1}\begin{bmatrix} u_{\mathrm{dc}}i^{*}_{\mathrm{v}}-\Delta P(i) \\ \Delta Q_{\mathrm{c}} \\ P_{\mathrm{s}2}-\Delta P_{\mathrm{s}2}(i) \\ P_{\mathrm{c}2}-\Delta P_{\mathrm{c}2}(i) \end{bmatrix}-Y_c\begin{bmatrix} -u_{\mathrm{cqp}} \\ u_{\mathrm{cdp}} \\ u_{\mathrm{cqn}} \\ -u_{\mathrm{cdn}} \end{bmatrix} \tag{25}$$

where $Y_{\mathrm{c}}=\omega C_{\mathrm{f}}$, $\Delta P(i)$ is the power consumed by the filter inductors that is read as:

$$\begin{aligned}\Delta P(i)=&R_1\left(i^2_{1dp}+i^2_{1qp}+i^2_{1dn}+i^2_{1qn}\right)\\&+R_2\left(i_{2dp}i_{1dp}+i_{2qp}i_{1qp}+i_{2dn}i_{1dn}+i_{2qn}i_{1qn}\right)\\&+\omega L_2\left(-i_{2qp}i_{1dp}+i_{2dp}i_{1qp}+i_{2qn}i_{1dn}-i_{2dn}i_{1qn}\right)\end{aligned} \tag{26}$$

$$, \Delta Q_{\mathrm{c}}=Y_{\mathrm{c}}\left(u^2_{\mathrm{cdp}}+u^2_{\mathrm{cqp}}+u^2_{\mathrm{cdn}}+u^2_{\mathrm{cqn}}\right) \tag{27}$$

, and $P_{\mathrm{s}2}$ and $P_{\mathrm{c}2}$ are sine and cosine components of the active power generated from the VSC at double the fundamental frequency (which is called the oscillating power) while $\Delta P_{\mathrm{s}2}$ and $\Delta P_{\mathrm{c}2}$ are the oscillating power consumed by the filter inductors and will be compensated by the power from the VSC side. Hence:

$$P_{\mathrm{s}2}=\Delta P_{\mathrm{s}2}(i) \tag{28}$$

$$P_{\mathrm{c}2}=\Delta P_{\mathrm{c}2}(i) \tag{29}$$

B. *Results*

An unbalanced voltage dip, resulting from two-phase fault (dip type C), is applied at the grid side. The dip starts at 0.2 s for duration of 0.1s with a remaining voltage of 40%. The resulting grid currents and DC-link voltage are shown in Fig. 8. The grid currents are sinusoidal during the voltage dip and the DC-link voltage is almost constant with no ripples. The transient at the start and end of the dip is mainly due to the delay in the sequence detection algorithm.

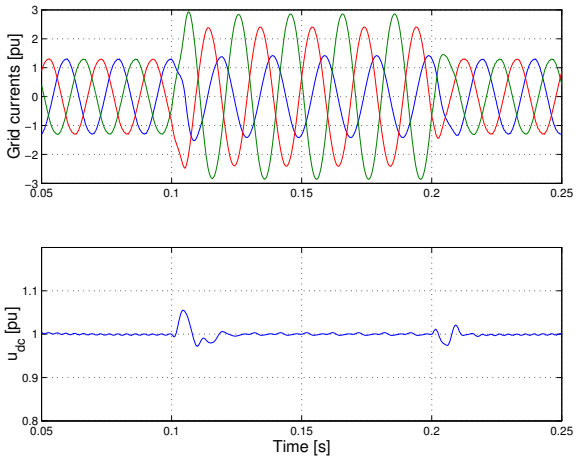

Fig. 8 Grid currents (upper) and DC-link voltage (lower) in case of voltage dip for DVCC.

All dips shown in Fig.5 are then tested. The instantaneous maximum current referred to the maximum of the nominal current and DC-link voltage peak-to-peak ripples referred to nominal DC voltage during the dip period are shown in Fig. 9 for all dips. For remaining voltage (V_{dip}) of 40% and higher, the maximum current that can occur is about 2 p.u. and maximum peak-to-peak DC ripples is about 0.05 p.u. (5% of nominal voltage).

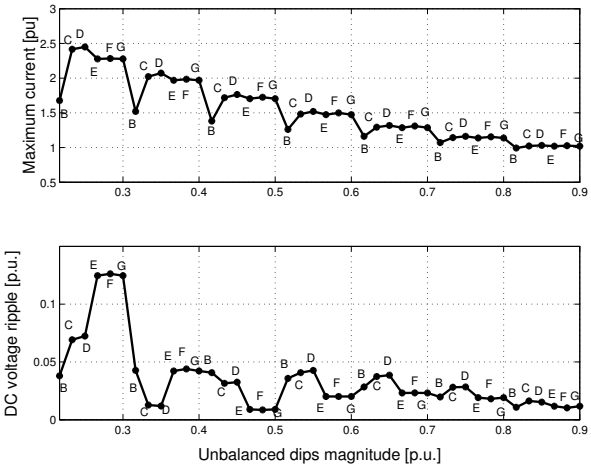

Fig. 9 Maximum grid current (upper), and DC-link voltage peak-to-peak ripples (lower) during different unbalanced dips.

VI. Conclusions

A dual vector current controller (DVCC) has been developed for the VSC connected to the grid through LCL-filter. The controller different gains have been adjusted to enhance the transient operation at higher frequencies. Proper current references are generated using a signal command from a DC-link voltage controller and compensating for the oscillating power produced in fault cases. The controller is examined and compared with a regular vector controller in

case of unbalanced voltage dips. It has proved to give better performance considering the grid current, which is sinusoidal, and DC-link voltage, which is smooth, during the dip period.

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VIII. BIOGRAPHIES

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Paper D

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Control of VSC connected to the grid through LCL-filter to achieve balanced currents

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Abstract— **Grid-connected voltage source converters (VSCs) are the heart of many applications with power quality concerns due to their reactive power controllability. However, the major drawback is their sensitivity to grid disturbances. Moreover, when VSCs are used in DG applications, voltage unbalance may be intolerant. The current protection may trip due to current unbalance or due to overcurrent. In this paper, a vector current controller for VSC connected to the grid through LCL-filter is developed with the main focus on producing symmetrical and balanced currents in case of unbalanced voltage dips. Implementing this controller helps the VSC system not to trip during voltage dips.**

Keywords- DG, LCL-filter, power quality, VSC, vector current control, voltage dips.

I. INTRODUCTION

Voltage source converters (VSCs) are now widely used in many grid-connected applications including STATCOMs, UPFCs, DVRs and as active interfaces for distributed generation (DG) systems (for instance photovoltaics, wind, fuel cells and microturbines). Benefits of using a VSC are sinusoidal grid currents and high controllability of both active and reactive power. To make the VSC operating towards the grid, an inductor is needed in each phase to limit and to control the currents. For DG systems, the output voltage of the grid-connected VSC needs often to be stepped up to the distribution level. Therefore, a step-up transformer should be used and the leakage inductance of the transformer will be equivalent to the needed series inductance. However, high frequency current harmonics are generated due to PWM switching of the VSC, which may affect the EMC sensitive loads connected to the same bus. The isolation of transformers is sensitive to high dv/dt. Therefore, the VSC voltages should be filtered. This can be done by inserting a reactor (inductor) towards the VSC and shunt-connected capacitors between the reactor and the transformer. Hence, LCL-filters are utilized to interface the VSC to the grid, which have the potential of improved grid current harmonics [1]-[4].

The major drawback of using VSC is its sensitivity to voltage disturbances, e.g. voltage dips. A voltage dip is a short duration drop in voltage that is normally due to a fault. For a VSC, a sudden decrease in grid voltage normally causes an increase in the current, as the control attempts at maintaining the power to the DC link constant. This can lead to tripping of the VSC because of overcurrent, in order to protect the IGBTs. Moreover, most faults are unbalanced and result in unbalanced voltage dips, which produce current harmonics and unbalance that also cause current protection to trip.

Many controllers have been developed to deal with grid voltage unbalance for a VSC system connected to the grid through L-filter [5] - [8]. In [9], LCL-filter is considered along with grid voltage unbalance. Moreover, a dual controller, that comprises one controller in the positive and one controller in the negative sequence frame, has been implemented. The reference negative sequence currents are set to zero. One case of voltage unbalance has been discussed showing the response only in the grid current.

In this paper, a vector current controller for VSC connected to the grid through LCL-filter is developed with the main focus on reducing current unbalance in case of different unbalanced voltage dips. The idea of implementing the controller in positive synchronous reference frame with feed-forward of negative voltage (first introduced in [7]) is adopted and modified for the system with LCL-filter. The performance of this controller is compared with a dual vector controller (DVC) regarding the VSC side current unbalance and the grid side current unbalance. This comparison is done by calculating the amount of unbalance, which is the ratio of negative sequence to positive sequence components, for each current and for different types of unbalanced voltage dips at the grid.

II. SYSTEM DESCRIPTION

A scheme of the investigated system is shown in Fig. 1. The VSC of rated power 69 kVA is connected to 400 V grid via LCL-filter, which has the parameters provided in Table I. The inductor on the grid side represents the leakage inductance of the transformer needed to match the grid requirement. Its inductance value is a ratio of the inductance at the VSC side. The ratio is higher than one in order to limit the high frequency harmonics in the VSC current. The choice of the LCL-filter parameters depends on the system rating. The criterion that is described in [4] and [10] has been used to choose the parameters. In this paper, the DC side has been assumed to have a constant DC voltage equal to 650 V. This assumption is reasonable if the DC capacitance C_{dc} is high [2].

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The LCL-filter is described in the instantaneous time domain and with single-phase notation, using KVL in the outer loop and KCL at the capacitor connection bus, as follows:

$$\frac{di_1}{dt} = \frac{-R_1}{L_1} i_1 - \frac{1}{L_1} u_c + \frac{1}{L_1} u \tag{1}$$

$$\frac{di_2}{dt} = \frac{-R_2}{L_2} i_2 + \frac{1}{L_2} u_c - \frac{1}{L_2} e \tag{2}$$

$$\frac{du_c}{dt} = \frac{1}{C_f} i_1 - \frac{1}{C_f} i_2 \tag{3}$$

where

i_1 is the phase current on the VSC side;
i_2 is the phase current on the grid side;
u_c is the capacitor phase voltage;
u is the VSC phase voltage;
e is the grid phase voltage.

Using the foregoing equations, the frequency response from the VSC voltage to the grid current is calculated and shown in Fig. 2. The figure shows that the LCL-filter has harmonic attenuation of 60 dB/decade at frequencies above the resonance peak equal to 1.1 kHz, thus eliminating the PWM switching current harmonics. The switching frequency is set to 2.5 kHz. The drawback of the LCL-filter is its peak gain at the resonance frequency, which implies an oscillatory behavior and consequently controller instability. Hence, this resonant peak should be damped actively within the controller.

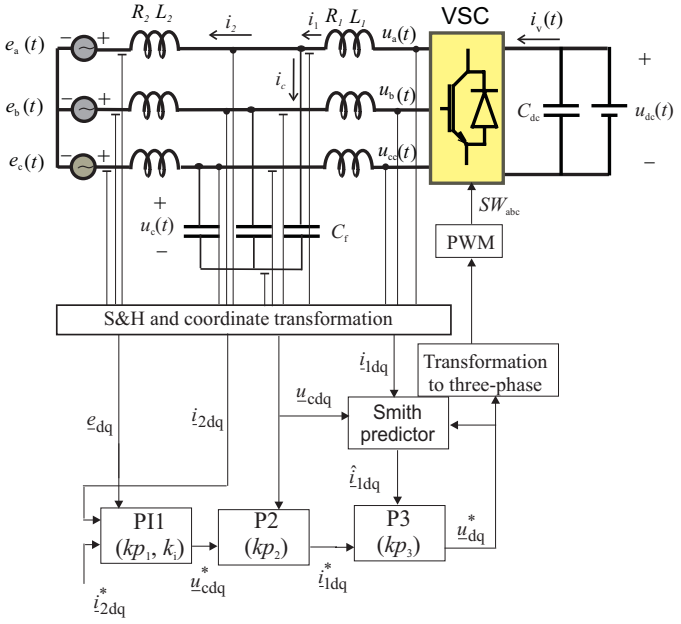

Figure 1. Power circuit along with main controller blocks.

TABLE I. LCL FILTER PARAMETERS (BASE IMPEDANCE IS ZBASE =2.3Ω).

Parameter	Description	pu
L_1	VSC side inductance	0.071
R_1	VSC side inductor resistance	0.1 L_1
L_2	Grid side inductance	0.027
R_2	Grid side inductor resistance	0.1 L_2
C_f	Filter capacitance	0.1

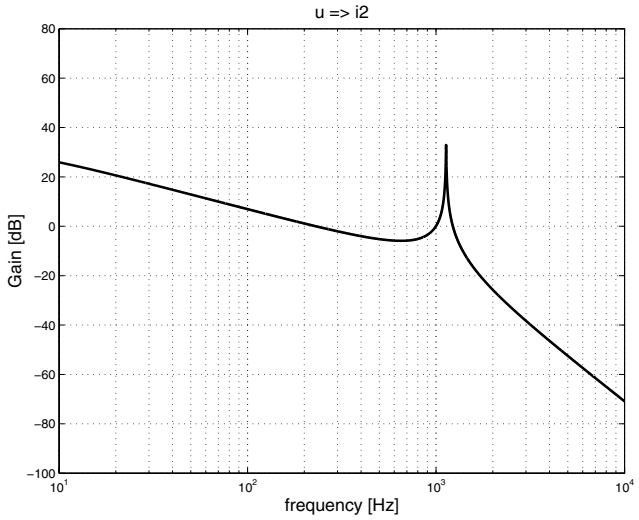

Figure 2. LCL-filter frequency response from VSC voltage to grid current.

III. CONTROLLER DESCRIPTION

A. Basic controller

The basic controller block diagram is shown in Fig. 1. The three-phase grid currents and voltages, VSC currents and voltages, and capacitor three phase voltages, are all measured and sampled with 5 kHz sampling frequency. All signals are then transformed into vectors in the fixed $\alpha\beta$-frame and then in the rotating dq-frame synchronized with the grid voltage. This is done by using the transformation angle θ obtained by using a PLL, which is assumed here to be slow and not to react on voltage dips. To increase the stability limits and in the same time damping oscillations at resonant frequency, three cascaded controllers are applied [13]. The outer controller (PI1) tracks the reference grid current vector $\underline{i}^*_{2dq}$ and the output is the reference capacitor voltage vector $\underline{u}^*_{cdq}$, which is the reference for the second controller (P2). In P2 the measured capacitor voltage vector $\underline{u}_{cdq}$ is compared with the reference command using a proportional controller, which produces the reference VSC current vector $\underline{i}^*_{1dq}$ for the third controller (P3). The third controller is also a proportional controller, which outputs the reference voltage vector $\underline{u}^*_{dq}$. The equations describing the cascaded controller in the dq-frame in the discrete time domain are:

$$\underline{u}^{*}_{\mathrm{cdq}}(k)=\underline{e}_{\mathrm{dq}}(k)+(R_2+\mathrm{j}\omega L_2)\underline{i}_{2\mathrm{dq}}(k)+k_{\mathrm{p1}}\left(\underline{i}^{*}_{2\mathrm{dq}}(k)-\underline{i}_{2\mathrm{dq}}(k)\right)+\underline{\Delta u}_{\mathrm{idq}}(k) \quad (4)$$

$$\underline{i}^{*}_{1\mathrm{dq}}(k)=\underline{i}_{2\mathrm{dq}}(k)+\mathrm{j}\omega C_{\mathrm{f}}\underline{u}_{\mathrm{cdq}}(k)+k_{\mathrm{p2}}\left(\underline{u}^{*}_{\mathrm{cdq}}(k)-\underline{u}_{\mathrm{cdq}}(k)\right) \quad (5)$$

where k is a sampling instant, $\underline{e}_{\mathrm{dq}}$ is the grid voltage vector in dq-frame, $\Delta\underline{u}_{\mathrm{idq}}$ is the integration part that eliminates steady state errors and finally ω is the angular frequency of the grid voltage. The integration part is calculated using the following equation:

$$\underline{\Delta u}_{\mathrm{idq}}(k+1)=\underline{\Delta u}_{\mathrm{idq}}(k)+k_{\mathrm{i}}\left(\underline{i}^{*}_{2\mathrm{dq}}(k)-\underline{i}_{2\mathrm{dq}}(k)\right) \quad (6)$$

where $k_{\mathrm{i}}=k_{\mathrm{p1}}T_{\mathrm{s}}/T_{\mathrm{i}}$, T_{i} and T_{s} are the integral time constant and the sampling time respectively. The reference voltage is then generated as:

$$\underline{u}^{*}_{\mathrm{dq}}(k+1)=\underline{u}_{\mathrm{cdq}}(k)+(R_1+\mathrm{j}\omega L_1)\underline{i}_{1\mathrm{dq}}(k)+k_{\mathrm{p3}}\left(\underline{i}^{*}_{1\mathrm{dq}}(k)-\underline{\hat{i}}_{1\mathrm{dq}}(k-1)\right) \quad (7)$$

The controller constants k_{p1}, k_{p2}, and k_{p3} are fractions of the corresponding dead-beat gains, k_{DB1}, k_{DB2}, and k_{DB3}, as

$$\begin{aligned}k_{\mathrm{p1}}&=k_1k_{\mathrm{DB1}}=k_1\left(\frac{L_2}{T_{\mathrm{s}}}+\frac{R_2}{2}\right)\\ k_{\mathrm{p2}}&=k_2k_{\mathrm{DB2}}=k_2\left(\frac{C_{\mathrm{f}}}{T_{\mathrm{s}}}\right)\\ k_{\mathrm{p3}}&=k_3k_{\mathrm{DB3}}=k_3\left(\frac{L_1}{T_{\mathrm{s}}}+\frac{R_1}{2}\right)\end{aligned} \quad (8)$$

To compensate for the time delay due to the calculation time, Smith predictor is used [14], which attempts to remove the effect of the delay time from the closed loop control system so that the controller can be designed as if no time delay was present. Hence, the Smith predictor is implemented in a way analogous to a state observer, which means running a model of the plant parallel to the plant itself. The predicted current equation is then calculated in the dq-frame as:

$$\hat{\underline{i}}_{1\mathrm{dq}}(k+1)=\frac{T_{\mathrm{s}}}{L_1}\left(\underline{u}^{*}_{\mathrm{dq}}(k)-\underline{u}_{\mathrm{cdq}}(k)\right)+\left(1-\frac{R_1}{L_1}-\mathrm{j}\omega T_{\mathrm{s}}\right)\hat{\underline{i}}_{1\mathrm{dq}}(k)+k_{\mathrm{ps}}\left(\underline{i}_{1\mathrm{dq}}(k)-\hat{\underline{i}}_{1\mathrm{dq}}(k-1)\right) \quad (9)$$

where k_{ps} is the observer gain that compensates for the error between the actual and the predicted currents.

Theoretically, choosing dead-beat gains for the controller should result in fast transient response. However, this is not possible in cascaded controllers, since the operation of the controllers should be decoupled. To choose the proper gains, the stability of the complete system has been examined looking at the pole location on the unit disc [13]. The controller parameters stated in Table II are chosen to produce an adequate response considering the overshoot, the rise time and the damping at the resonance frequency.

TABLE II. LCL-CONTROLLER PARAMETERS.

k_1	1
k_2	1
k_3	0.2
T_{i}	0.01 s
k_{ps}	0.07

B. Performance in case of grid voltage unbalance

To be able to analyze the grid voltage unbalance, the decomposition of the voltage vector into positive and negative-sequence is needed. This is performed in a *dqp*-frame with the technique proposed in [8], which originates from [15]. By delaying the voltage vector by one fourth of the grid cycle T, a vector composed of the same positive sequence component and a negative sequence component with equal amplitude and opposite sign is obtained. Therefore, if this vector is added to the measured supply voltage vector, the negative sequence voltage will be removed. The positive sequence voltage component can, thus, be extracted from the measured values as

$$\underline{e}_{dqp}(t)=\tfrac{1}{2}\left(\underline{e}_{dq}(t)+\underline{e}_{dqp}(t-T/4)\right) \quad (10)$$

The negative sequence, in *dqp*-frame, can be calculated as

$$\underline{e}_{dqn(p)}(t)=\tfrac{1}{2}\left(\underline{e}_{dq}(t)-\underline{e}_{dqp}(t-T/4)\right) \quad (11)$$

The latter will be seen as a constant signal in the negative rotating plane *dqn*, which utilizes the opposite angle for the *dq*-transformation. This technique is applied to the current vectors as well, to be able to look at positive and negative sequence currents resulting due to the voltage imbalance.

The voltage imbalance due to unbalanced voltage dips is considered here. Three different dips are applied; one is due to a single phase fault, another is due to double phase fault, and the third is due to double phase to ground fault. The phasor diagram of voltage dips resulting from the three different faults is shown in Fig. 3. The dip magnitude E_{dip}, which is the magnitude of the remaining voltage during the dip, is chosen such that all dips have the same positive sequence component. The active current reference is chosen to be 1 pu while the reactive current reference is set to zero to produce unity power factor at the grid side. The resulting positive sequence current is shown in Fig. 4. This current is the same for all dips apart from the transients at the start and the end of the dip. This transient time is produced mainly due to the delay introduced by the sequence detection algorithm.

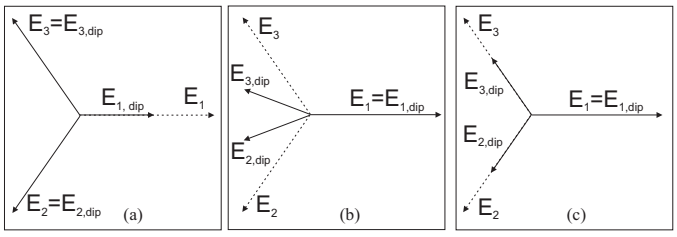

Figure 3. Voltage dips due to (a) single phase fault, (b) double phase fault, and (c) double phase to ground fault.

A dip due to a single phase fault with 10 % remaining voltage has been applied at 0.2 s for duration of 0.1 s, as shown in Fig. 5. The resulting negative sequence currents, on the VSC and grid sides, in *dq*-frame will be as shown in Fig. 6. The amount of imbalance, which is the ratio of negative sequence to positive sequence components at fundamental frequency [12], given by

$$r_i = \frac{\sqrt{i_{2\mathrm{dn}}^2 + i_{2\mathrm{qn}}^2}}{\sqrt{i_{2\mathrm{dp}}^2 + i_{2\mathrm{qp}}^2}} \times 100 \qquad (12)$$

is 132 % in this case. For a dip due to double phase fault with 40% remaining voltage, shown in Fig. 7, $r_i = 89$ %. In this case, the negative sequence currents are shown in Fig. 8. For the last case, which is a dip due to double phase to ground fault, $r_i = 69$ %. The voltage and negative sequence current are shown in Fig. 9 and Fig. 10, respectively.

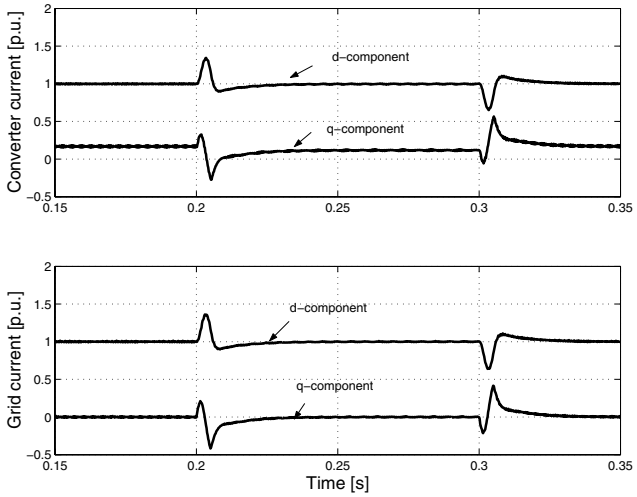

Figure 4. Positive sequence VSC current (upper) and grid current (lower) in *dq*-frame.

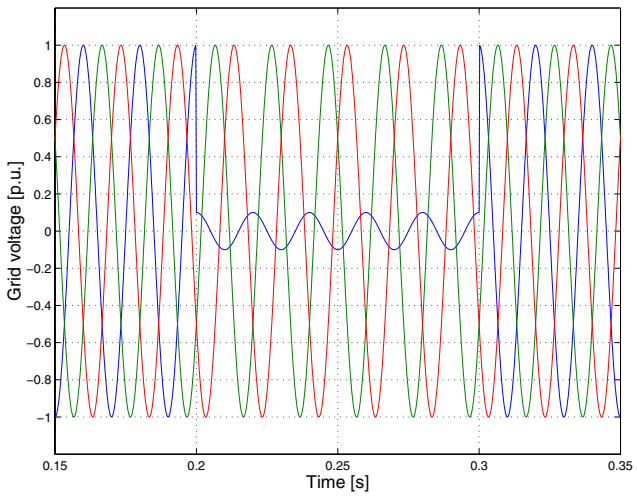

Figure 5. Grid voltage: 10 % voltage dip due to single phase fault.

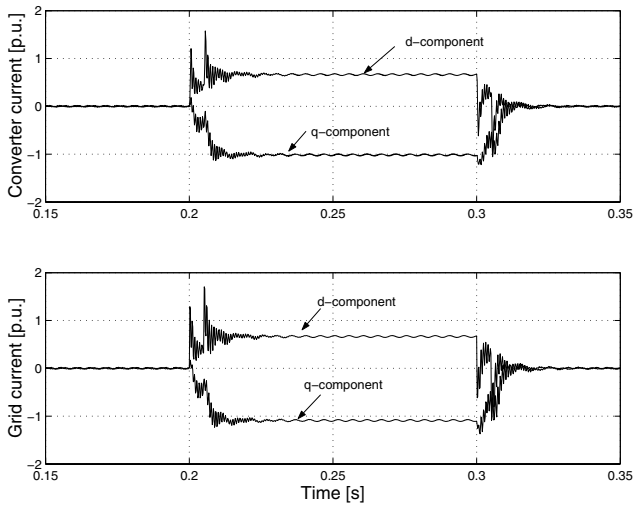

Figure 6. Negative sequence of VSC current (upper) and grid current (lower): 10 % voltage dip due to single phase fault.

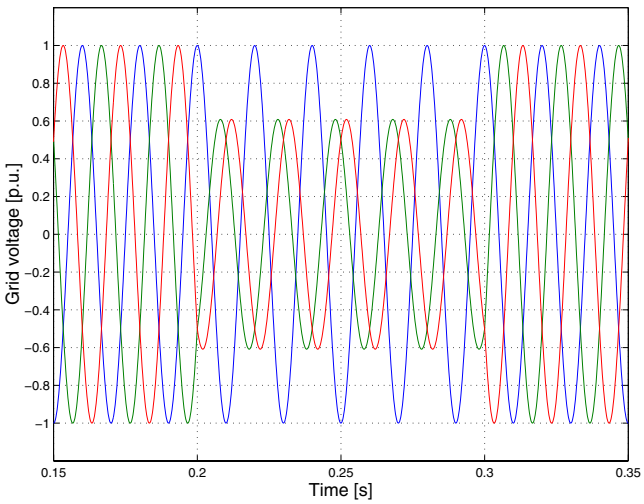

Figure 7. Grid voltage: 40 % voltage dip due to double phase fault.

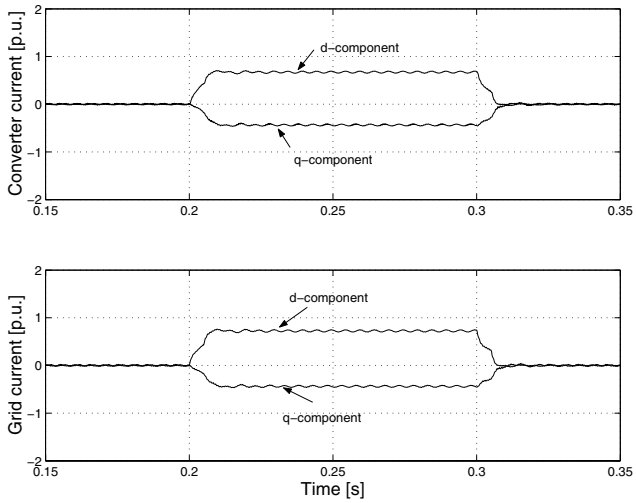

Figure 8. Negative sequence of VSC current (upper) and grid current (lower): 40 % voltage dip due to double phase fault.

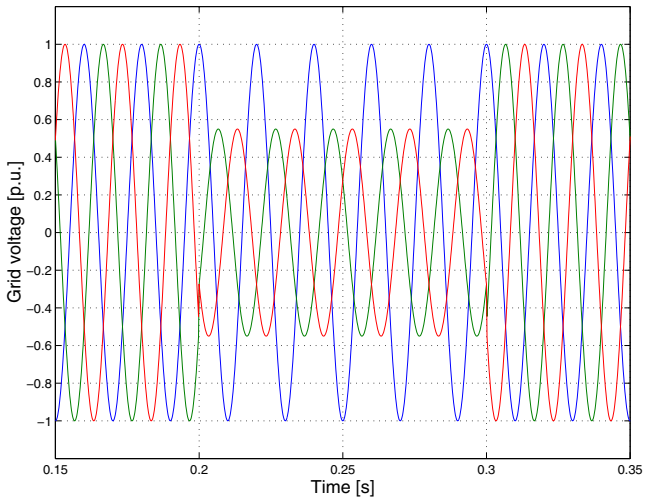

Figure 9. Grid voltage: 55 % voltage dip due to double phase to ground fault.

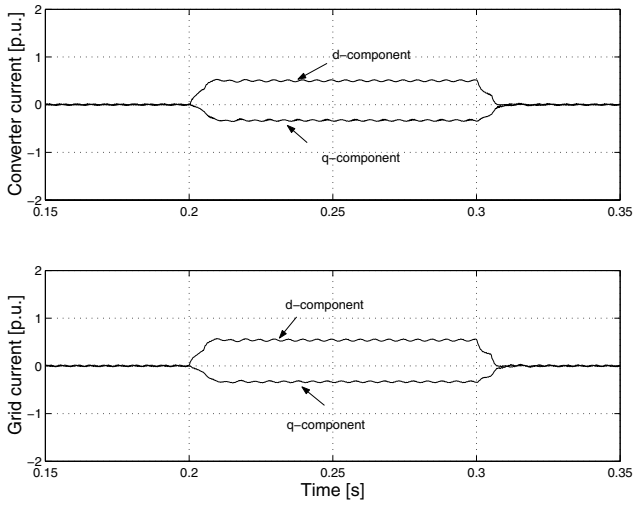

Figure 10. Negative sequence of VSC current (upper) and grid current (lower): 55 % voltage dip due to double phase to ground fault.

IV. Proposed Controller for Balanced Currents

A. *One controller in the positive sequence frame with feed forward for the negative sequence (NSFF)*

Since the main interest of the controller is to deal with voltage imbalance, the LCL-filter should be described in positive and negative sequence synchronous frames (*dqp*- and *dqn*- frames) to derive relevant control laws. The *dqp*-frame is synchronized with the grid voltage with the same direction of rotation, while *dqn*-frame rotates in the opposite direction.

The LCL-filter equations (1) to (3), is described in the *dqp*-frame as follows:

$$\frac{d}{dt}\underline{i}_{1dq} = -j\omega\underline{i}_{1dq} - \frac{R_1}{L_1}\underline{i}_{1dq} - \frac{1}{L_1}\underline{u}_{cdq} + \frac{1}{L_1}\underline{u}_{dq} \tag{13}$$

$$\frac{d}{dt}\underline{i}_{2dq} = \frac{-R_2}{L_2}\underline{i}_{2dq} - j\omega\underline{i}_{2dq} + \frac{1}{L_2}\underline{u}_{cdq} - \frac{1}{L_2}\underline{e}_{dq} \tag{14}$$

$$\frac{d}{dt}\underline{u}_{cdq} = \frac{1}{C_f}\underline{i}_{1dq} - \frac{1}{C_f}\underline{i}_{2dq} + j\omega\underline{u}_{cdq} \tag{15}$$

In steady state and *dqn*-frame, the foregoing equations are read as follows:

$$\frac{-R_1}{L_1}\underline{i}_{1dqn} + j\omega\underline{i}_{1dqn} - \frac{1}{L_1}\underline{u}_{cdqn} + \frac{1}{L_1}\underline{u}_{dqn} = 0 \tag{16}$$

$$\frac{-R_2}{L_2}\underline{i}_{2dqn} + j\omega\underline{i}_{2dqn} - \frac{1}{L_2}\underline{u}_{cdqn} + \frac{1}{L_2}\underline{e}_{dqn} = 0 \tag{17}$$

$$\frac{1}{C_f}\underline{i}_{1dqn} - \frac{1}{C_f}\underline{i}_{2dqn} - j\omega\underline{u}_{cdqn} = 0 \tag{18}$$

For the grid currents to be symmetrical, the negative sequence components in *dq*-frame should be nullified; i.e. $\underline{i}_{2dqn}=0$. That should be achieved by adjusting the reference VSC voltage vector described in (7). Substituting with $\underline{i}_{2dqn}=0$ in (18) and using the result in (16) yields

$$\underline{u}^*_{dqn} = \underline{u}_{cdqn}\left(1+\omega^2 C_f L_1\right) + jR_1\omega C_f\,\underline{u}_{cdqn} \tag{19}$$

This is implemented using positive sequence grid and capacitor voltage vectors within the controller equations and the negative sequence capacitor voltage vector is fed-forward to calculate the negative part of the VSC reference voltage vector, as suggested in Fig. 11.

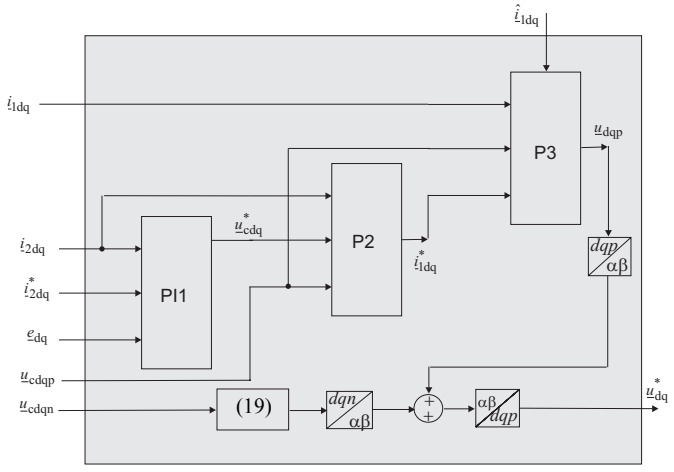

Figure 11. Schematic diagram for the controller for balanced currents.

However, recalculating (19) with the specified filter parameters, yields

$$\underline{u}^*_{dqn} \approx \underline{u}_{cdqn} \tag{20}$$

which is the condition for balanced converter currents. With this algorithm, the VSC currents are forced to be balanced, which reduces the ratio of imbalance in the grid currents.

Moreover, substituting $\underline{i}_{1dqn} = 0$ and $\underline{i}_{2dqn} = 0$ in (17) results in $\underline{u}^*_{cdqn} = \underline{e}_{dqn}$ and in (18) results in $\underline{u}^*_{cdqn} = 0$. Since these conditions contradict with each other, it is not possible to achieve symmetrical grid and VSC currents simultaneously.

B. Dual vector controller (DVC)

The controller equations (4) to (9) can be described in *dqp*-frame and *dqn*-frame, and then two parallel controllers, one for each frame, can be implemented as shown in Fig. 12 [8]. To achieve symmetrical grid currents during grid voltage unbalance, the reference negative sequence currents are set to zero. This controller cannot achieve symmetrical VSC current, since there is no direct access to the VSC current reference.

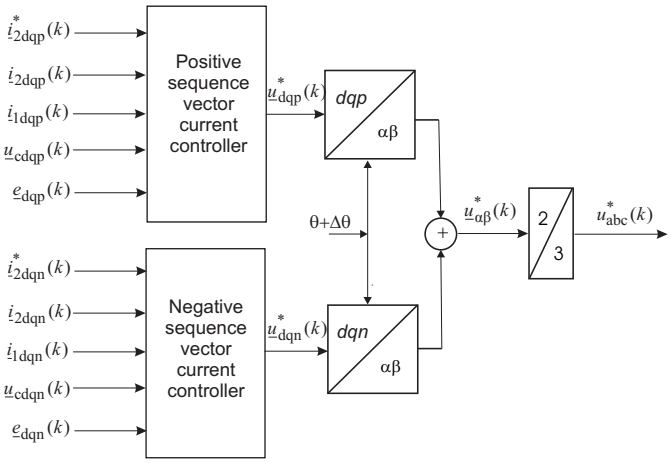

Figure 12. Dual vector controller.

C. Results

The first proposed controller, to achieve balanced currents in case of grid voltage unbalance, using the feed forward of the negative sequence capacitor voltage (NSFF) is tested in case of unbalanced voltage dips. The VSC negative sequence current is nullified, for the three introduced different voltage dips, while the negative sequence grid current is significantly reduced. This is shown for the dip due to single phase fault, since it produces the most amount of imbalance, in Fig. 13. This amount of unbalance is reduced from 132 % to less than 5 % when applying the current balancing algorithm. The three phase VSC and grid currents are also shown in Fig. 14. When the dual controller, DVC, is implemented with the same voltage dip, the resulting negative sequence in the grid and VSC currents is as shown in Fig. 15. The negative sequence of the grid current is nullified during the dip, while the negative sequence of the VSC current is reduced to less that 5 %.

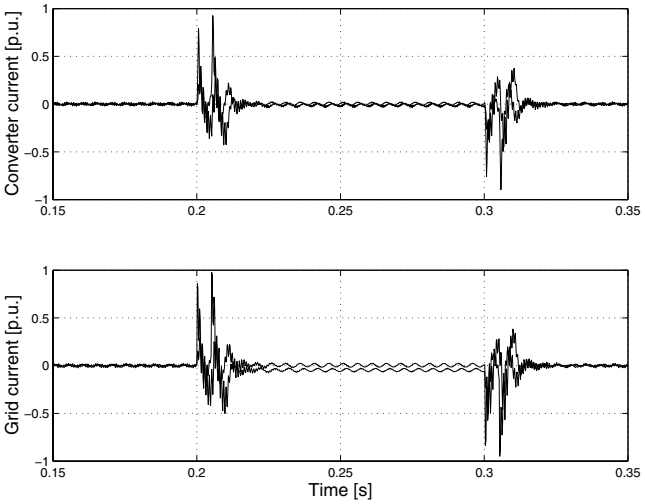

Figure 13. Negative sequence of VSC current (upper) and grid current (lower): NSFF and 10 % voltage dip due to single phase to ground fault.

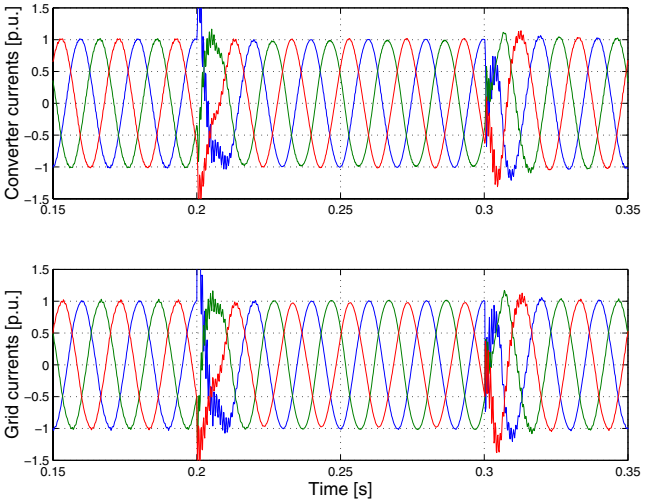

Figure 14. VSC current phasors (upper) and grid current phasors (lower) balanced current control.

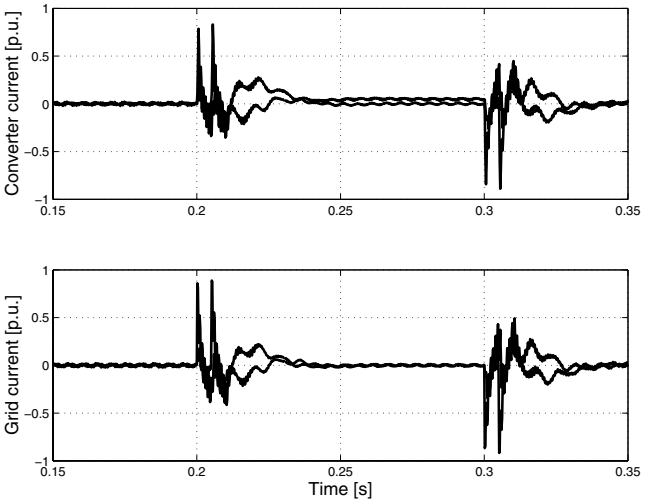

Figure 15. Negative sequence of VSC current (upper) and grid current (lower): DVC and 10 % voltage dip due to single phase to ground fault.

V. CONCLUSIONS

A vector current controller for VSC connected to the grid through LCL-filter is developed with the main focus on reducing current imbalance in case of unbalanced voltage dips at the grid. The controller is applied in the positive sequence frame and the negative sequence capacitor voltage vector is fed-forward with relevant relations that are derived here. Implementing this controller the currents on the VSC side are symmetrical while the amount of imbalance in the current on the grid side is reduced from 132 % to 5 % in case of a voltage dip due to a single phase fault with 10 % remaining voltage. The controller has been tested also for dips due to double phase fault and double phase to ground fault. The grid currents are almost symmetrical during the different voltage dips, which results in protecting the VSC from tripping due to overcurrents or current imbalance during the dip period. This controller has been compared with a dual vector controller (DVC) that is composed of two controllers; one is implemented in the positive sequence frame and the other is implemented in the negative sequence frame. The DVC has been tested with the same cases of grid voltage imbalance. The resulting grid side current is balanced while the VSC side current has an amount of imbalance of less than 5 %.

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Paper E

F. Magueed, and T. Thiringer, “Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC,” *submitted to Electrical Power Quality and Utilization Journal.*

Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC

Fainan Magueed, *Member, IEEE*, and Torbjörn Thiringer, *Member, IEEE*

***Abstract*— The phase locked loop (PLL) is an important part of the current-controlled grid-connected converter. Its job is to estimate the phase angle of the grid voltage. If the PLL is not robust, the grid-voltage distortion will lead to an error in the estimated phase leading to a degradable performance of the converter's function. In this paper, the effect of the PLL on the operation of a current-controlled voltage-source converter is examined. A PLL synthesis is proposed, to track the phase angle of the distorted grid voltage, and compared with a previously investigated PLL. The result found is that the proposed synthesis of the PLL is superior in case of grid voltage harmonics other than the 5th and the 7th orders. Moreover, the capability of compensating for the voltage amplitude modulation was improved using the proposed PLL. The amplitude oscillation has been reduced from 8% to 3%, with the proposed PLL, compared to from 8% to 5% with the previously investigated PLL.**

***Index Terms*— Amplitude modulation, Distributed generation, harmonics, phase locked loop, light flicker, power quality, voltage dips, voltage source converters.**

I. Introduction

Grid-connected voltage-source converters (VSCs) are the basic elements of most new FACTS, custom power equipment and HVDC systems due to their good controllability [1]. They are also used as an interface for distributed generation systems and in adjustable speed drives applications. To keep their control goals, which are dependent on the instantaneous state of the grid, a good estimation of the grid phase angle is needed. This is usually done using a software phase locked loop (PLL) instead of a classical hardware PLL to reduce the controller cost and provide the flexibility to modify the PLL's parameters to match a specific control requirement.

In three-phase systems, the PLL algorithm is usually implemented in a rotating reference frame (*dq*-frame) that is synchronized with the grid voltage using the estimated phase angle [2]. This type of PLL will be referred to as Q-PLL, since its major input is the quadrature (*q*) component of the voltage vector. The latter reflects the error between the estimated and the actual phase. When this error is fed into a PI controller, the estimated angle will change in a way to eliminate this error. The Q-PLL yields good results during non-disturbed conditions. However, in the presence of grid-voltage harmonics, imbalance, or voltage amplitude change, an error in the estimated phase will occur [2]. In order to make the PLL robust towards this polluted voltage and to recover the correct phase angle, the use of low pass filters (LPF) has been proposed in [3] and [4]. The aim of using an LPF is to extract the positive sequence of the grid voltage in the *q*-direction, in which the negative sequence should not appear. In this way the effect of the grid voltage imbalance on the estimated phase is negligible. However, a trade-off has to be made between robustness and good transient performance of the LPFs [5]. Lower cut-off frequency of the filters results in less distortion in the estimated phase, yet slower dynamics will occur. In order to overcome this problem, a second order generalized integrator has been proposed in [6] to extract the positive sequence of the grid voltage. The task of this integrator is to produce a 90^{o} delayed signal, which is adaptive to the change of the grid fundamental frequency. However, the need for tuning the integrator is adding to the complexity of the PLL-design. On the other hand, for the grid-connected applications considered here, the frequency change is assumed to be kept within the allowed limits (e.g. in Sweden $\pm$ 0.5 Hz is respected according to the Swedish standard SS EN-50160:2000) by the strong grid.

The purpose of this paper is to investigate the effect of the PLL on the operation of a current-controlled power-electronics interfaced distributed-generation with a voltage source converter as a front end. This is done through the implementation of two PLL configurations, considering the case of a distorted grid voltage. The previously investigated PLL, which uses the positive-sequence of the quadrature component of the grid voltage to extract the angle, is compared with a proposed PLL synthesis based upon the neural networks application. The two PLL configurations have been evaluated regarding the voltage quality at the connection point of the VSC, where the VSC controller is aiming at regulating the terminal voltage in addition to its original task, which is injecting active power to the grid.

II. Phase Locked Loop (PLL)

The output voltage of a grid-connected VSC is synchronized with the grid voltage using a PLL. The estimated phase output of the PLL could also be used for the detection of an islanding condition to protect the VSC and the system that is connected

through it, in case of severe voltage changes in the grid [7]. Hence, for proper operation of the controller, the error in the estimated phase should be minimal. Two PLL algorithms will be evaluated regarding their performance to handle the voltage disturbaces. Since the quadrature component PLL is the basic building element for both, it will be explained first.

A. Quadrature-Component Based PLL (Q-PLL)

This type of PLL has been investigated previously in [2], for instance, and is shown here in Fig. 1. The measured grid voltage is transformed from three-phase notation into a voltage vector in a fixed $\alpha\beta$-frame, using power invariance transformation. This voltage vector is then normalized and transformed into a vector in a rotating *dq*-coordinate, which rotates with the estimated angular frequency $\hat{\omega} = \mathrm{d}\hat{\theta}/\mathrm{d}t$, where $\hat{\theta}$ is the estimated phase angle. The normalized *q*-component of the voltage is then used as an input to a PI-controller to produce a required change in the angular frequency ($\Delta\omega$) to track the changes in the phase angle.

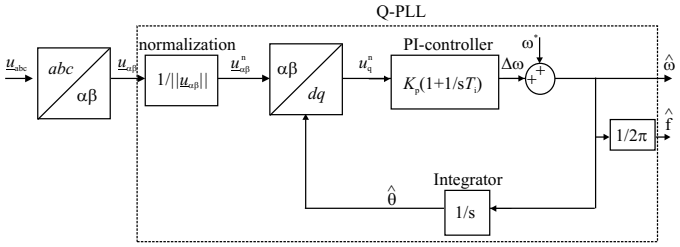

Fig. 1 Phase estimation using Q-PLL.

The normalization of the voltage vector results in nullifying the phase estimation error due to a balanced voltage amplitude change (e.g. three-phase voltage dips). However, in case of an unbalanced voltage amplitude variation (e.g. an unbalanced voltage dips), oscillations having the frequency of twice the fundamental frequency will be superimposed in the *q*-component voltage due to the introduced negative sequence that rotates in the opposite direction [2].

B. Positive Sequence Frame PLL (PS-PLL)

To reduce the error in the estimated phase-angle due to the existence of the negative sequence in case of an unbalanced grid voltage, a PS-PLL is implemented. As shown in Fig. 2, the three-phase voltages are measured and transformed into a vector in the stationary $\alpha\beta$-frame. Then the positive sequence voltage vector is extracted using the DSC algorithm, and fed into the Q-PLL that has been described in Fig. 1.

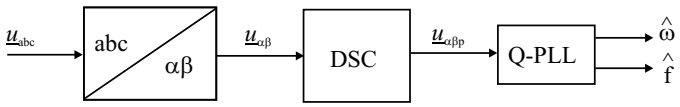

Fig. 2 PS-PLL.

1) The delayed signal cancellation method (DSC)

The method of DSC, which has been proposed in [8], is adopted here for the decomposition of the supply voltage into the positive and the negative sequences. It is defined in the $\alpha\beta$-plane by the following expressions:

$$\underline{u}_{\alpha\beta\mathrm{p}}(t) = \frac{1}{2}\left(\underline{u}_{\alpha\beta}(t) + \mathrm{j}\underline{u}_{\alpha\beta}(t - \frac{T_g}{4})\right) \tag{1}$$

$$\underline{u}_{\alpha\beta\mathrm{n}}(t) = \frac{1}{2}\left(\underline{u}_{\alpha\beta}(t) - \mathrm{j}\underline{u}_{\alpha\beta}(t - \frac{T_g}{4})\right) \tag{2}$$

where T_g is the fundamental period of the grid voltage;
$\underline{u}_{\alpha\beta\mathrm{p}}$ is the positive sequence voltage vector in the $\alpha\beta$-frame; and
$\underline{u}_{\alpha\beta\mathrm{n}}$ is the negative sequence voltage vector in the $\alpha\beta$-frame.

2) DSC effect on grid voltage harmonics

It is assumed that the grid voltage has an h^{th} harmonic component superimposed on its fundamental component. In the stationary $\alpha\beta$ −frame, this will be expressed in the time domain as follows:

$$\underline{u}_{\alpha\beta}(t) = U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \tag{3}$$

where U_1 and U_h are the amplitudes of the fundamental and the h^{th} harmonic respectively, ω is the fundamental grid-voltage angular-frequency, and h_s is the related harmonic sequence that takes a value of either +1 (for positive sequence) or -1 (for negative sequence) according to [9]:

$$h_s = \begin{cases} +1 & h = 3n+1 \\ -1 & h = 3n+2 \\ 0 & h = 3n \end{cases} \tag{4}$$

where n is any number starting from zero.

The zero sequence harmonics will not be regarded in this analysis, since the VSC is normally connected to the grid through a Y/D transformer that eliminates the triplet harmonics.

Substituting (3) in (1), the positive-sequence vector of the grid voltage in $\alpha\beta$ −frame is:

$$\underline{u}_{\alpha\beta\mathrm{p}}(t) = \frac{1}{2}\begin{pmatrix} U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \\ + \mathrm{j}\left(U_1 e^{\mathrm{j}\omega(t - T_g/4)} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega(t - T_g/4)}\right) \end{pmatrix} \tag{5}$$

where $\dfrac{\omega T_g}{4} = \dfrac{\pi}{2}$.

The harmonic part of (5) can be expressed using trigonometric functions as follows:

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = \frac{U_\mathrm{h}}{2}\begin{pmatrix} \cos(h\omega t) + \mathrm{j}(h_\mathrm{s})\sin(h\omega t) \\ + \mathrm{j}\cos\left(h\omega t - h\dfrac{\pi}{2}\right) - (h_\mathrm{s})\sin\left(h\omega t - h\dfrac{\pi}{2}\right) \end{pmatrix} \tag{6}$$

For the odd harmonics of orders less than 11^{th} (i.e. 5^{th} and 7^{th}), $\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}$ will be nullified since:

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = -(h_\mathrm{s})\sin(h\omega t) \tag{7.a}$$

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = (h_s)\cos(h\omega t) \quad (7.b)$$

However, opposite signs will appear in (7) for higher harmonics (e.g. the 11th), implying the existence of such harmonics superimposed on the positive sequence voltage.

For the even harmonics of orders less than the 10th, the following will hold:

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = (h_s)\cos(h\omega t) \quad (8.a)$$

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = -(h_s)\sin(h\omega t) \quad (8.b),$$

which implies the existence of these harmonics superimposed on the fundamental component in the positive sequence frame. In spite of the opposed sign in (8) for higher harmonics (more than the 10th), they will still exist in the positive sequence as (6) suggests.

Yet, since the 5th and 7th harmonics are the most dominant in the power system [9], it is expected that using the PS-PLL in estimating the grid-voltage phase angle will give good results as it will be shown later in the case study.

3) DSC effect on grid-voltage amplitude modulation

Grid voltage amplitude modulation is a result of fast periodically-changing heavy loads that are connected at the grid. If a distribution network is considered, one of the direct effects would be the light flicker. The frequency of light flicker ranges between 0.5 Hz and 30 Hz, since this is the range of the human eye sensibility [10]. One way to mitigate this phenomenon is to compensate for the oscillating reactive power using a STATCOM [10], which is a three-phase VSC.

If the VSC controller is aimed at mitigating the voltage-amplitude modulation, the *q*-component of the grid voltage will be forced to oscillate with the same frequency as the modulating function. Substituting $h_s = 0$ and $h = 1/5$ (for a 10 Hz amplitude modulation) in (6), will show that the positive sequence will also be oscillating, producing an error in the estimated phase. To nullify this error, a bandwidth less than the frequency of the amplitude-modulating signal should be adopted. However, this will affect the transient performance of the VSC.

C. Neural-Network Fundamental-Extractor Based PLL (NN-PLL)

To nullify the phase-estimation error produced due to the harmonics and amplitude modulation of the grid voltage and in the same time to obtain a good dynamic performance, the implementation of an adaptive linear neural-network is proposed. The advantages are the easy synthesis and programming, the adaptation capability to the change in the grid voltage, and the fast response.

1) Adaptive linear neural-network extractor (ADALINE)

ADALINE is one of the earliest neural network models that was proposed in [11]. A simple ADALINE consists of one neuron that has a linear input-output relationship, where each input is simply multiplied by a certain weight and all inputs are summed together to produce the output. The power of ADALINE, though, comes from the on-line adaptation of its weights that gives it a non-linear property. For this purpose, the least mean square (LMS) algorithm is used [12].

ADALINE has been implemented in [13] as a combiner to identify the voltage waveform for the classification of power quality issue. It will be used here in the same way, however, as an extractor to relieve the fundamental component of the source polluted voltage. ADALINE is shown in Fig. 3, where the discrete input vector $\mathbf{x}(k)$ is composed of sine and cosine elements of all possible frequency components that could be contained in the source voltage

$$\mathbf{x}(k) = \left[\sin(\omega k T_s) \quad \cos(\omega k T_s) \quad \ldots \quad \sin(h\omega k T_s) \quad \cos(h\omega k T_s)\right]^T \quad (9)$$

where h is the highest harmonic order expected, k is the sampling instant, T_s is the sampling time, and the superscript T indicates the transpose of the vector. This input vector $\mathbf{x}(k)$ is then multiplied by a weight vector $\mathbf{w}(k)$ to produce the ADALINE output $u_{nn}(k)$.

$$\mathbf{w}(k) = \left[w_{11} \quad w_{12} \quad w_{21} \quad w_{22} \quad \ldots \quad w_{h1} \quad w_{h2}\right] \quad (10)$$

$$u_{nn}(k) = \mathbf{w}(k)\cdot\mathbf{x}(k) = \sum_{i=1}^{2h} w_i x_i \quad (11)$$

where w_i and x_i is the i^{th} element in the vectors $\mathbf{w}$ and $\mathbf{x}$ respectively.

The output is then compared with the measured and sampled voltage signal $u_s(k)$, where the resulting error $\varepsilon_{nn}(k)$ is used by the LMS algorithm to modify the weight vector according to

$$\mathbf{w}(k+1) = \mathbf{w}(k) + \lambda\frac{\mathbf{x}(k)\varepsilon_{nn}(k)}{\mathbf{x}(k)^T\mathbf{x}(k)} \quad (12),$$

where λ is the learning factor.

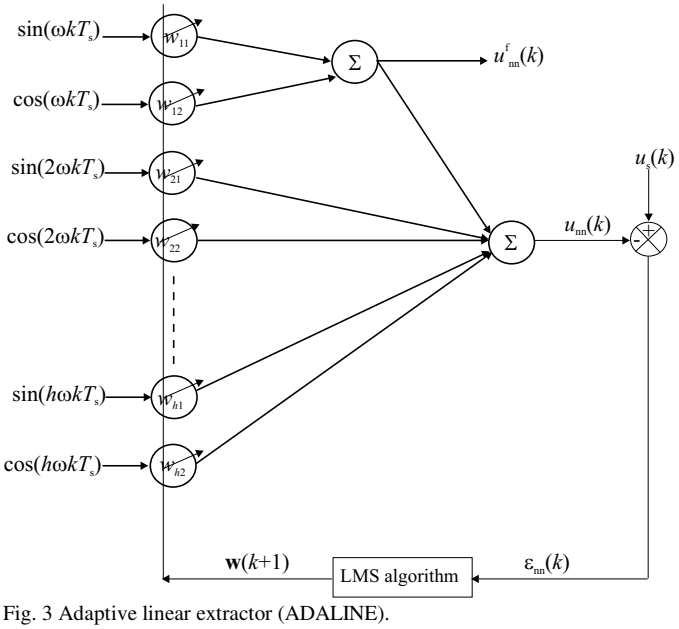

Fig. 3 Adaptive linear extractor (ADALINE).

The learning factor λ is given a value between 0 and 1, where this value specifies the speed of the correction of the error ε_{nn} [14]. The upper limit value of 1 corrects the error within one iteration, while decreasing this value will increase the number of iterations used for the correction. This is evaluated applying an input sinusoidal signal with a 5% magnitude of the 5th harmonic and a 3% magnitude of the 7th harmonic and a 30% voltage decrease at 0.6 s with a phase-angle jump of -60°. The output of ADALINE is examined using two different learning rates: 0.07 and 0.7. The tracking signal u_{nn} and the fundamental signal u_{nn}^{f} are shown for λ = 0.07 in Fig. 4, whereas counterpart signals corresponding to $\lambda = 0.7$ are shown in Fig. 5. As expected, the tracking is faster with the higher learning rate. However, the fundamental wave is distorted in the transient period and an overshoot occurs due to the fast change in the weight vector. With lower λ, the change in the weight vector is slower and hence the fundamental wave will ride-through the transient period keeping its sinusoidal shape and implying better performance of the PLL.

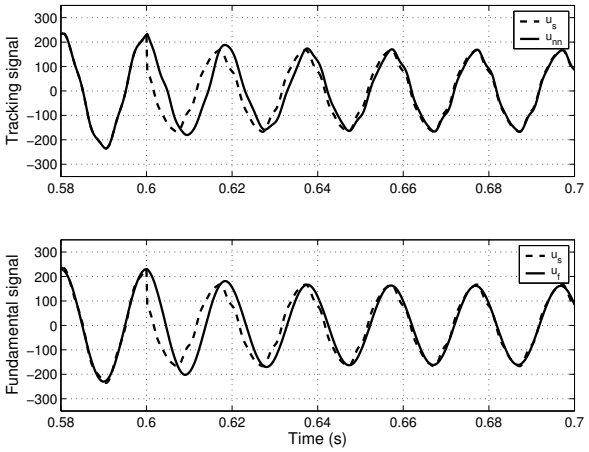

Fig. 4 ADALINE tracking signal (upper) and fundamental signal (lower) with λ =0.07.

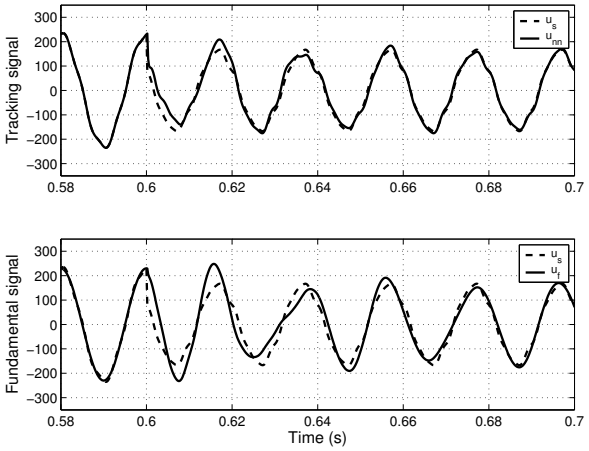

Fig. 5 ADALINE tracking signal (upper) and fundamental signal (lower) with λ =0.7.

The block diagram of the PLL implementing ADALINE (NN-PLL) is shown in fig. 6. The three-phase voltage is transformed into the stationary $\alpha\beta$-frame. Then each component is fed into a separate ADALINE algorithm, shown in Fig. 3, to extract the fundamental component that is fed into a Q-PLL. The effect of changing the learning rate is reexamined regarding the overshoot in the estimated-phase due to an unbalanced voltage dip with about -45° phase angle jump. The result is shown in Fig. 7, indicating the increase of the overshoot as the learning rate increases. This is again justifies the use of lower value for the learning rate.

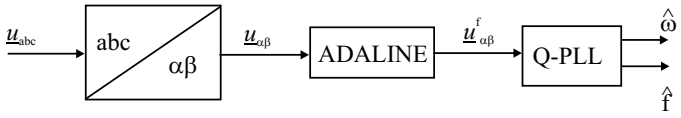

Fig. 6 NN-PLL.

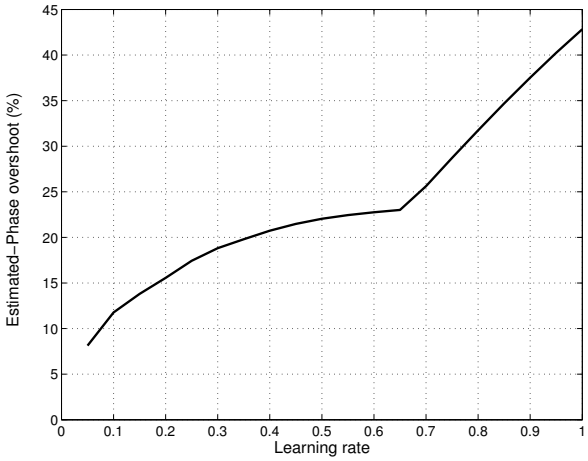

Fig. 7 Estimated-phase overshoot due to unbalanced voltage dip with phase angle jump.

III. The Performance of PS-PLL, and NN-PLL

The performance of PS-PLL and NN-PLL has been tested in MatLab/Simulink regarding the harmonics effect and the dynamic behavior.

The error in the estimated phase angle due to the presence of the grid voltage harmonics is shown in Fig. 8, with a three different bandwidth values for the Q-PLL, for the two estimators. A 2% amplitude of the 2nd, 4th, 5th, 7th, 11th and 13th harmonic orders has been superimposed separately on the fundamental grid-voltage. The phase error has been calculated as the peak-to-peak amplitude of the normalized quadrature-voltage.

With the PS-PLL, the error in the estimated phase-angle increases using higher values of the bandwidth. Moreover, the amplitude of the error increases with the increase of the harmonic order, excluding the case for the 5th and 7th harmonics at which it was proven that the error is nullified. This can be understood by inspecting (6), where the harmonic order is in proportional relationship with the frequency of the

oscillations superimposed on the fundamental grid voltage.

Using the NN-PLL the error is nullified for all harmonic orders and all values of bandwidth, which means that it is robust and in the same time provides a better dynamics.

To study the dynamical behavior, a balanced voltage dip having a -40° phase angle jump has been applied at the grid as shown in Fig. 9. The dip starts at 0.4 s and ends at 0.6 s. The actual phase angle of the grid voltage is shown by the solid line while the estimated phase angle is shown by the dashed line for PS-PLL and dash-dotted line for NN-PLL. The NN-PLL has been implemented using a bandwidth of 50 Hz, while the PS-PLL has a bandwidth of 5 Hz since it should be slow to be robust against the grid voltage harmonics. As expected, using the NN-PLL results in the fast tracking of the phase angle of the grid voltage, implying a better dynamic performance.

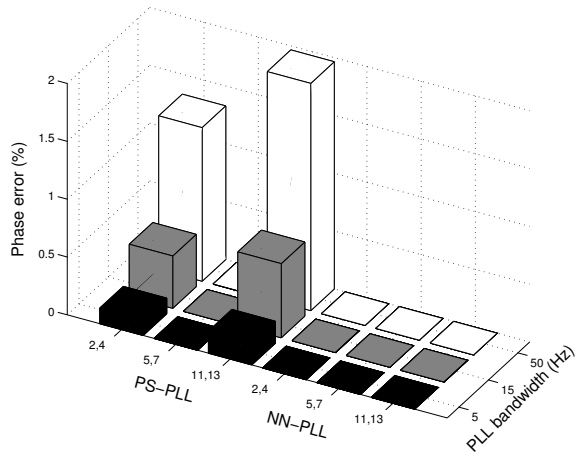

Fig. 8 Estimated-phase error due to different harmonics and in case of bandwidth of 5, 15, and 50 Hz.

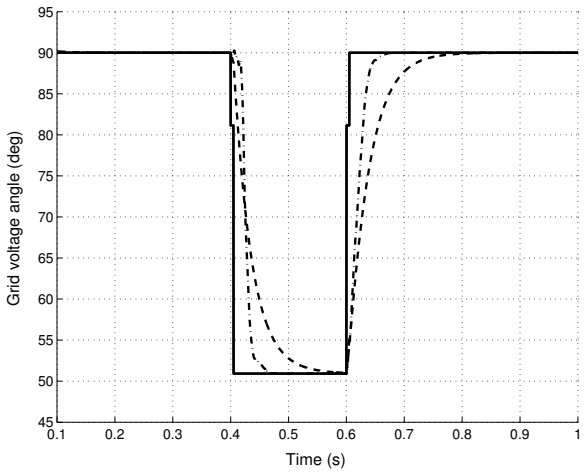

Fig. 9 Grid voltage angle; actual (solid), estimated using PS-PLL with small bandwidth (dashed), and estimated using NN-PLL with large bandwidth (dash-dotted).

IV. Case Study: Grid Connected VSC as an Interface for Distributed Generation

A distributed generation (DG) unit is considered in this case study, in which the EMTDC is used for the simulation, to evaluate the effect of the two previously discussed PLL algorithms on its controller's performance. The mitigation of grid voltage amplitude modulation and voltage dips with phase angle jumps are considered here.

A. System Model

In Fig. 10 an example part of a distribution system with a DG is presented. A fluctuating load is assumed to be connected at bus 1, and is further assumed to be disconnected in case of a fault at the same bus. Its effect is encountered as an 8% amplitude modulation of the grid voltage at bus 1 using a cosine modulating signal with a frequency of 10 Hz. In reality this modulating signal could have an infinite number of frequencies, but for the sake of clarity only the 10 Hz component is displayed here. A distributed generation unit is connected at bus 3, where a sensitive load is also connected. The latter is assumed to be a static inductive load that requires the voltage to be maintained at 1 p.u. all the time at the point of common coupling (bus 3) with a good power quality.

The DG unit could represent a small wind turbine, a photovoltaic unit, or a fuel cell system. Since the energy source is not the issue here, it has been assumed that its dynamics are slower than that of the control system. Hence, the energy source is modeled as a constant current source i_{in}, as shown in Fig. 11. The injected power, coming from the energy source, is transferred through a DC-link and adjusted to match the grid-connection requirements using a controlled voltage source converter (VSC). Moreover, an LCL-filter is used in order to eliminate the higher grid-side current harmonics caused by the PWM switching of the VSC [15]. The grid side inductance, which is connected to the PCC, represents the leakage inductance of a step-up transformer.

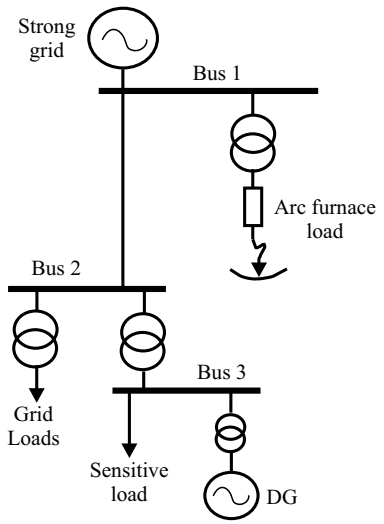

Fig. 10 Distribution system for the case study.

B. Controller description and targets

The main task of the controller of the DG is to inject active power into the grid. In addition, using the power electronics system with the controller, shown in Fig. 11, it can mitigate power quality problems. Accordingly, in grids with large industrial loads (polluting the grid with harmonics, voltage

fluctuations, voltage dips … etc.) and sensitive loads (requiring a certain level of power quality), the DG should maintain a controlled operation and in the same time grid power quality improving. For this purpose, a PCC-voltage regulator is used to provide the ability to inject reactive power at the PCC to maintain the voltage at its nominal value and condition. Hence, the DG controller is composed of the following parts.

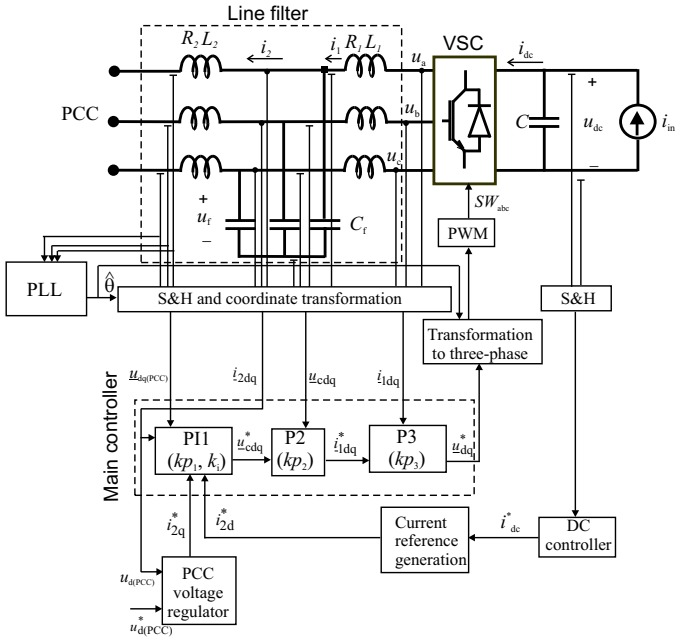

Fig. 11 Power electronics converter-interfaced DG system with robust controller.

1) Main Controller

The control system for the DG unit is implemented in a rotating *dq*-frame that is synchronized with the voltage at the PCC using a phase locked loop (PLL).

The main controller, which is shown in Fig. 11, consists of three cascaded controllers to obtain proper dynamics and at the same time to damp the oscillations at the resonance frequency of the LCL-filter as explained in [15]. The three-cascaded controllers are: an outer current controller, a capacitor voltage controller, and an inner current controller. The outer controller (PI1) tracks the reference current of the grid $\underline{i}^*_{2\mathrm{dq}}$ and its output is the reference capacitor voltage $\underline{u}^*_{\mathrm{fdq}}$, which is fed to the capacitor voltage controller (P2). In P2, the measured (or estimated) capacitor voltage $\underline{u}_{\mathrm{fdq}}$ is compared with its reference command using a proportional controller, which produces the reference current $\underline{i}^*_{1\mathrm{dq}}$ for the inner current controller (P3). The latter is also a proportional controller, which generates the reference voltage $\underline{u}^*_{\mathrm{dq}}$. This reference voltage is then transformed into a three-phase voltage vector to be used in the PWM as a reference signal to generate the proper switching commands. This controller is explained in more details in [15].

2) DC-regulator

In the case of grid voltage variations, the DC-link voltage should be regulated to maintain a constant value in order to protect the DC capacitor and maintain the correct operation of the VSC.

The DC regulator is a PI-controller that generates a DC current reference i^*_{dc}. Then, the active current reference $i^*_{2\mathrm{d}}$ is generated (current reference generation block in Fig. 11), based on the power balance between the AC and DC side of the VSC, to maintain the DC voltage at its nominal value during voltage disturbances at the PCC.

3) PCC-voltage regulator

Since the *q*-component of the PCC voltage is set to zero using the coordinate transformation, the *d*-component $u_{\mathrm{d(PCC)}}$, should be regulated to maintain the PCC voltage at its nominal value $u^*_{\mathrm{d(PCC)}}$. The reactive current reference $i^*_{2\mathrm{q}}$ is generated to compensate for the error in the PCC voltage using a PI-controller. More details of the control system are given in [16].

C. Operation in case of voltage amplitude modulation, and voltage dips

Due to the loads connected to the grid, a voltage amplitude modulating signal is superimposed on the fundamental grid voltage. Moreover, a voltage dip with a phase angle jump will appear at the PCC, from 0.5 s to 0.7 s, caused by a three phase fault at bus 1. In addition, due to the voltage drop through the feeder, the voltage at the PCC will decrease in amplitude. All these phenomena should be compensated for locally at the PCC by the DG injected power, which is adjusted by the controller. The impact of the two PLL algorithms on the controller performance is now to be investigated.

1) Using the PS-PLL

With the voltage compensation capability of the DG, the voltage at the PCC should be regulated to 1 p.u. However, the error in the phase estimation, due to the polluted voltage, will result in an error in the value of the current command $i^*_{2\mathrm{q}}$ leading to uncompensated oscillations in e_{d}. Moreover, regarding the equation of the instantaneous reactive power injected by the DG at PCC [16]

$$q_{(\mathrm{PCC})} = u_{\mathrm{q(PCC)}} i_{2\mathrm{d}} - u_{\mathrm{d(PCC)}} i_{2\mathrm{q}} \quad (13),$$

and since the active power is regulated using the DC-regulator, which implies regulated $i_{2\mathrm{d}}$, the *q*-component voltage $u_{\mathrm{q(PCC)}}$ will oscillate in consequence of the oscillating $q_{(\mathrm{PCC})}$. Though, due to the phase estimation error, it is unavoidable that the oscillations will increase in amplitude. Hence, the three-phase voltage-envelope will oscillate around the nominal value.

This is shown in Fig. 12, where the voltage envelope at the PCC is shown in the upper trace for the case of no DG installed. The middle trace in the same figure represents the case for using the PS-PLL with a 15 Hz bandwidth. The amplitude modulation still exists, with about 5% peak-to-peak value, due to the high bandwidth of the PLL compared to the

frequency of the modulating signal.

2) Using NN-PLL

The three-phase voltage-envelope at the PCC is shown, in this case, by the lower trace of Fig. 12. The peak-to-peak value of the oscillation is reduced to 3% using the same bandwidth as before. Moreover, the dynamic behavior is better, which is obvious regarding the amplitude of the overshoot during and after the voltage dip.

The estimated frequency is shown in Fig. 13 for the two PLL configurations.

Moreover, the voltage amplitude variation at PCC has been tested with different modulating signal frequencies and the result is shown in Fig. 14, where it can be noted that the system with NN-PLL has a lower peak-to-peak value of the oscillation of the voltage envelope.

It is worth noting here that the oscillations of the voltage envelope will not be completely nullified since both active and reactive powers are oscillating, due to the modeling that is considered here, which means that both injected active and reactive powers should be oscillating in order to compensate for it. However, this is not possible since the application of a DG implies constant injected active power into the grid. Moreover, the behavior of the NN-PLL is dependent on the input-vector length, the order of harmonic frequencies used in that vector, and the initial weights values. The input-vector length is taken, here, as 18 and the initial weight vector was set to zero.

In addition, regarding the application considered here, which is DG systems, it is assumed that there is an injected active power to the grid. The value of this active power, though, affects the voltage compensation capability. More injected active power implies more available reactive power to be injected. Yet, the current amplitude will increase leading to increased DC-link voltage ripples, as shown in Fig. 15. Hence, if a current limiter is applied, to protect the VSC valves and improve the DC-link voltage regulation, it will mean limiting the voltage compensation capability.

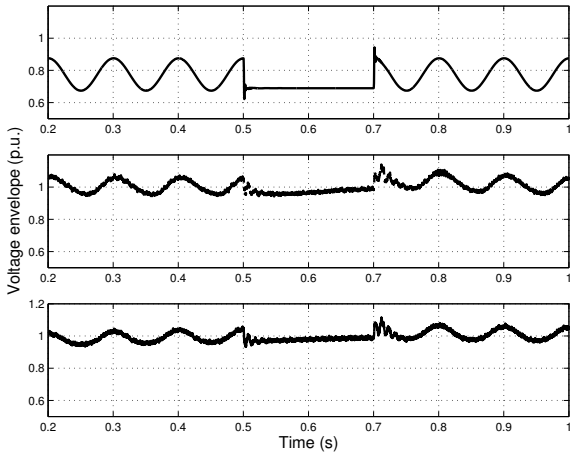

Fig. 12 Voltage envelop with DG not connected (upper), DG with PS-PLL (middle), and DG with NN-PLL (lower).

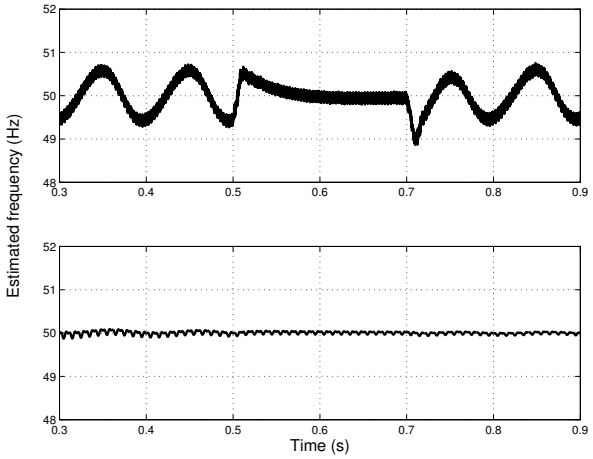

Fig. 13 Estimated frequency using: PS-PLL (upper), and NN-PLL (lower) with 15 Hz bandwidth.

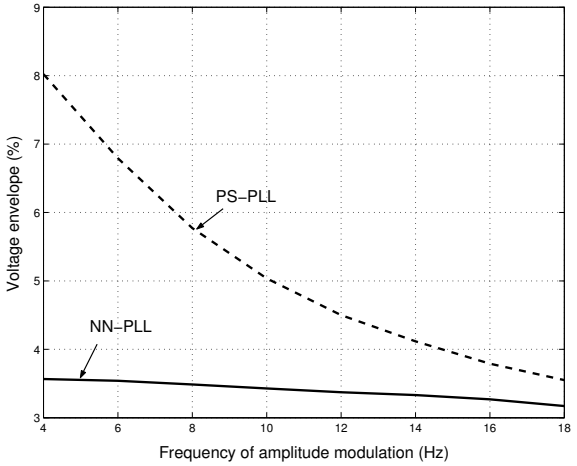

Fig. 14 Voltage amplitude variation due to changing the modulating signal frequency; with PS-PLL (dashed curve) and NN-PLL (solid curve).

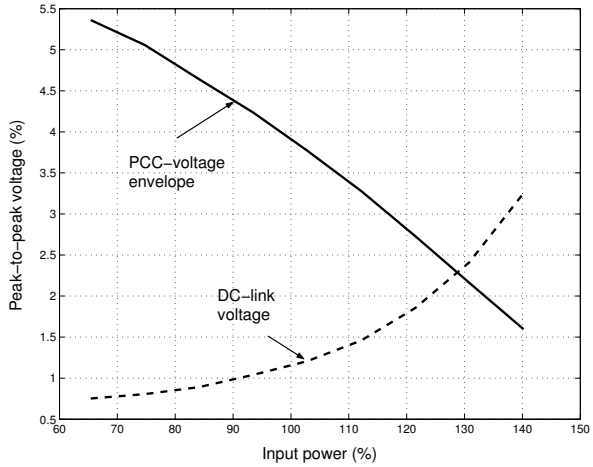

Fig. 15 Effect of the input power on PCC voltage envelope oscillation (solid), and DC-link voltage ripples (dashed).

V. CONCLUSIONS

The error in the phase estimation of the grid voltage affects the performance of the current-controlled grid-connected voltage source converters (VSC). In this paper, a neural network phase locked loop (NN-PLL) estimator has been compared with a previously investigated PLL, which extracts the phase angle from the positive-sequence quadrature-component of the grid voltage. It was shown in this paper that, the proposed PLL synthesis is more robust against grid voltage harmonics, is better in handling the transients, and can improve the voltage compensation function of the VSC.

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Paper G

F. Magueed, G. Olsson, and T. Thiringer, “Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation,” submitted to *IEEE trans. on Power Delivery.*

Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation

Fainan Magueed, *Member, IEEE,* Gustaf Olsson, *Member, IEEE,* Torbjörn Thiringer, *Member, IEEE*

***Abstract*—Islanding of a voltage source converter (VSC) equipped DG unit connected to a weak grid is considered in this paper. The islanding detection using over/under voltage, which is commonly used for passive detection methods, is not adequate due to the voltage limitation that is incorporated in the DG controller for its safe operation. Hence, the estimated frequency of the grid voltage along with a point of common coupling (PCC) voltage regulator, with a reactive current reference limiter incorporated, is proposed for islanding detection algorithm. Using a PCC-voltage regulator adds the active, or dynamic, property for the detection algorithm and increases its reliability. Moreover, using the current limiter increases its robustness, which has been tested for the case of voltage dips at the grid. By setting the proper current limit, the DG unit can have the ability to ride-through voltage dips with magnitudes above a certain limit, which can be set according to the grid codes, and detect islanding for voltage dips with magnitudes lower than that limit. This has been tested for the case of island motor load, which is considered as a difficult type of load since it affects the grid states in the case of islanding.**

***Index Terms*—Distributed generation, Intentional islanding, LCL-filter, PLL, Voltage source converters, Vector control, weak grid.**

I. Introduction

Although the integration of distributed generation (DG) has many driving forces, it still has many challenges [1]. Islanding, due to utility outage, is one of the problems that can cause improper operation of a DG unit, and its connected loads, if it is not detected.

There are two types of islanding detection techniques; passive and active [2]. In the passive techniques, the sensed grid states (voltage, frequency …etc.) are compared with their nominal values and the deviations are used to identify the islanding condition. Although they are simple to implement, the passive techniques suffer from a certain non detectible zone (NDZ), which represents the amount of the active and reactive power mismatch between the DG and its local loads at which the passive detection algorithm fails [2], [3]. Incorporating the active detection techniques, the NDZ becomes negligible. An active detection technique could typically be incorporated in the main controller of the DG, using active disturbance injection into the grid [4]. If the grid is disturbed, the passive detection starts to react to identify the islanding condition.

The problem of islanding can be more crucial with the application of the DG in a weak grid, where the grid states are not robust [5]. That implies that the active detection techniques that tend to disturb the grid are not adequate. Instead, active techniques that tend to improve the power quality at the grid might be more adequate.

The steady state performance of different passive detection algorithms regarding the reduction of the non-detectible zone (NDZ) has been studied in literature [2] - [3]. The under/over frequency has been found to have an NDZ that is independent on the active power mismatch and dependent on the quality factor of the load. To overcome this dependency, an under/over frequency passive detection algorithm has, in this paper, been incorporated in an active detection technique. The detection technique consists of three parts; a passive detection algorithm, a PCC voltage regulator, and a reactive current limiter. The dynamic performance and robustness of the proposed active islanding detection are studied regarding the voltage dips at the grid and the load dynamics.

II. System Description

A. Investigated network

A weak grid system is, here, referring to a rural electric feeder where the voltage level at the load bus is not constant and is affected by the load dynamics. The system in Fig. 1 will be considered, where the voltage at the point of common coupling (PCC) is affected by the feeder voltage drop and the load dynamics. The feeder has an X/R ratio of 10, and its inductance is 6.15 mH per phase. The island-loads consume power that is assumed to be lower than the DG-injected power, implying the directions of the active and reactive power mismatches (ΔP and ΔQ) as designated in the same figure. The island loads will be set (models and parameters) later in order to investigate the ability of the islanding detection method for various cases.

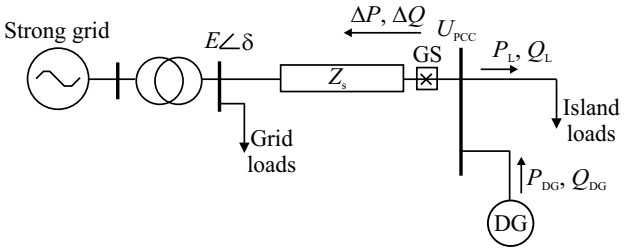

Fig. 1. System considred for islanding study.

The grid loads are assumed to be static loads that have rated power of 0.2 p.u. based on the DG nominal settings. The DG unit is an inverter based system that is connected through an LCL-filter to the PCC. The data of the DG unit are reported in Table I.

TABLE I
DG SYSTEM DATA

Symbol	Quantity	Value
E_{DG}	Nominal RMS line AC voltage	0.4 kV
I_{DG}	Nominal RMS phase current	0.1 kA
f	Nominal grid frequency	50 Hz
U_{dc}	Nominal DC link voltage	0.65 kV
I_{dc}	Nominal DC current	0.107 kA
L_1	Converter-side LCL-filter inductance	0.52 mH
R_1	Converter-side LCL inductor resistance	1.6 mΩ
L_2	Grid-side LCL-filter inductance	0.2 mH
R_2	Grid-side LCL-filter inductor resistance	0.6 mΩ
C_f	LCL-filter capacitance	138 μF
R_d	DC-chopper damping resistance	10 Ω

The main part of the DG system, which is considered here, is a PWM voltage source converter (VSC), which represents the front end of an energy source. The latter is modeled as a constant current source i_{in} (in Fig. 2), since the variations in the input power are considered slow compared to the transient response of the VSC controller. The LCL-filter is implemented on the AC-side of the VSC to prevent harmonic current injection into the grid.

B. DG main controller

The DG controller is implemented in a rotating *dq*-frame that is synchronized with the grid-voltage angular-frequency using a phase locked loop (PLL). The PLL estimates the angular frequency of the grid voltage $\hat{\theta}$ using a PI-controller [6]. In the case of island operation the output of the PLL is set to the reference angular frequency θ^*. As shown in Fig. 2, the grid states (voltages and currents) are measured and transformed into vectors in the *dq*-frame. The transformation matrices set the *q*-component of the grid voltage to zero, while the *d*-component represents the amplitude of the line voltage. A DC-link voltage regulator is also incorporated to maintain a constant DC voltage value in order to protect the DC-capacitor and maintain correct operation of the VSC. The DC-regulator is implemented as a PI-controller that outputs a DC current reference i^*_{dc}, which is then used to generate the active current reference i^*_{2d}. The latter is generated based on the power balance between the AC-side and the DC-side of the VSC. The current i^*_{2d} is fed to the VSC controller in the case of grid connected operation. In the case of island operation, i^*_{2d} is used to determine the duty ratio of the DC-chopper switch that is only activated in this case. The DC-chopper is incorporated in the DC-side of the VSC in order to dissipate the extra power that is produced during island operation by the energy source.

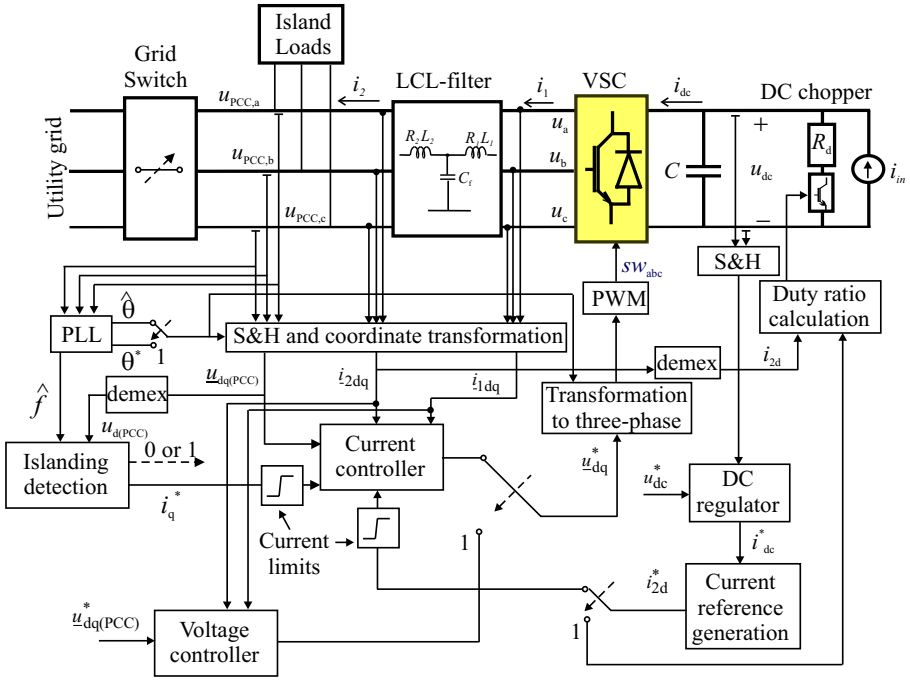

Fig. 2. System as seen by the DG. The dashed lines in the controller denote the islanding detection status.

Neglecting the switching losses of the VSC, the plant to be controlled is mainly the LCL-filter. It is described using three transfer functions; G_{p1}, G_{p2}, and G_{p3}, as

$$G_{p1}(s)=\frac{I_2(s)}{U_f(s)-U_{PCC}(s)}=\frac{1}{sL_2+R_2}$$
$$G_{p2}(s)=\frac{U_f(s)}{I_1(s)-I_2(s)}=\frac{1}{sC_f} \quad (1)$$
$$G_{p3}(s)=\frac{I_1(s)}{U(s)-U_f(s)}=\frac{1}{sL_1+R_1}$$

where s is the Laplace operator and U_f is the voltage over the filter's capacitor in the s-domain.

The DG main controller is the vector current controller that is shown in Fig. 3, which is devoted to the grid connected operation and is then modified as a voltage controller in case of island operation.

1) Vector current controller:

The current controller consists of three cascaded controllers. The inner controller G_{c3} is used for stabilization of G_{p3} and is designed based on dead-beat control. The two outer controllers G_{c2} and G_{c1} are used to stabilize G_{p2} and G_{p1} respectively. G_{c2} is implemented as a P-controller, while G_{c1} is implemented as a PI-controller where the integral part is added to eliminate the steady state error. G_{c1} is a two-degree of freedom controller, since it exploits the output signal of a Smith predictor (with a compensation gain k_{ps}) to cancel the time delay effect. The time-delay free plant transfer-function G_{pm} (incorporated in the Smith predictor) represents the LCL-filter model in steady state.

The three controllers are implemented in discrete form and described in the rotating dq-frame as follows

$$\underline{y}_{1dq}(k)=k_{p1}\left(\underline{\varepsilon}_{idq}(k)+\frac{T_s}{T_i}\sum_{n=0}^{k}\underline{\varepsilon}_{idq}(n)\right) \quad (2)$$

$$\underline{y}_{2dq}(k)=k_{p2}\,\underline{y}_{1dq}(k) \quad (3)$$

$$\underline{u}^{*}_{dq}(k+1)=\underline{u}_{fdq}(k)+(R_1+j\omega L_1)\underline{i}_{1dq}(k)+k_{p3}\,\underline{y}_{2dq}(k) \quad (4)$$

where

$\underline{y}_{1dq}$ is the output vector of G_{c1}, which represents the change in the capacitor voltage $\underline{u}_{fdq}$;

k is the sampling instant;

k_{p1} is the proportional gain of G_{c1};

T_i is the integral time of G_{c1};

$\underline{y}_{2dq}$ is the output vector of G_{c2}, which represents the required change in the converter side current $\underline{i}_{1dq}$;

k_{p2} is the proportional gain of G_{c2};

k_{p3} is the proportional gain of G_{c3}; and

$\underline{\varepsilon}_{idq}$ is the current error vector.

The faster the inner loop is in comparison with the outer loops, the better is the performance of the cascaded control system in the sense of the transient response. However, reduced gains for the outer controllers will reduce the overall bandwidth of the system. Hence, the inner controller gain is set to the dead-beat gain as

$$k_{p3}=\frac{L_1}{T_s}+\frac{R_1}{2} \quad (5)$$

And the inner controller parameters are given as ratios of k_{p3}, as reported in Table II.

TABLE II
DG MAIN CONTROLLER PARAMETERS

Symbol	Quantity	Value
f_s	Sampling frequency	5 kHz
k_{p1}	Outer controller gain	0.55
k_{p2}	Second controller gain	0.78
k_{p3}	Inner controller gain	2.6
T_i	Integral time	0.03 s
k_{ps}	Smith predictor gain	0.07

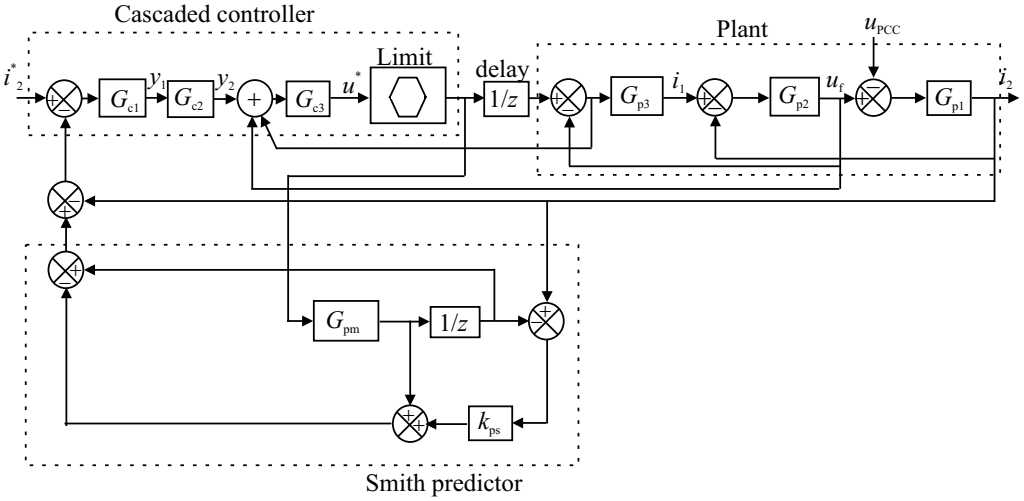

Fig. 3. Schematic diagram of the main current controller (z denotes the z-transform, thus $1/z$ denotes a delay of one sample).

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Converter-Interfaced Distributed Generation – Grid Interconnection Issues

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Göteborg, Sweden 2007

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Grid Interconnection Issues

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To my family

Converter-Interfaced Distributed Generation –
Grid Interconnection Issues

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Abstract

Distributed generation (DG) with a converter interface to the grid is found in many of the green power resources applications. In this thesis, the control of a voltage source converter (VSC), as the DG front end, is in focus regarding the power quality problems that could appear at the connection point. The aims have been set to maintain a stable operation of the DG, in case of network disturbances, and to react in a corrective way during different grid operating conditions (e.g. in case of voltage dips). For this purpose, vector current controllers have been implemented with two different line filters; namely an inductance filter (L-filter) and an inductance-capacitance-inductance filter (LCL-filter). The controllers have incorporated: one sample time delay compensation, limitation of the reference voltage to avoid saturation, an integrator anti-windup, a DC-link voltage controller, a PCC voltage regulator, and an islanding detection algorithm.

The ride-through capability of the DG has been examined against a variety of possible voltage dips that could appear at the connection point. Moreover, the capability of the DG to compensate for the voltage at the connection point has been studied. Finally, the intentional islanding has been considered, where the DG is allowed to energize a part of the grid in case of the utility outage forming what is called an island.

The results found are that the effect of unbalanced voltage dips on the DC-link voltage ripple is minimized if the oscillating powers, produced during that period, are supplied by the grid side instead of the DC-side. Moreover, design equations have been derived in order to calculate the maximum currents that would flow through the VSC valves during voltage dips. These equations are to be used in designing VSC's with voltage dips ride-through capability. In addition, a neural-network based PLL, which extracts the phase angle of the fundamental component of the grid voltage, has been introduced in order to provide better performance in case of a DG with voltage compensation capability. Finally, combining the voltage regulator with the estimated frequency as a measure for islanding condition has, in this work, been found as an appropriate practice, to detect islanding, especially in the case of weak grids.

***Keywords**:* distributed generation, harmonics, intentional islanding, L-filter, LCL-filter, power quality, strong grid, vector control, voltage dips, voltage regulation, VSC, weak grid.

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Fainan Abdul-Magueed Hassan

Gothenburg, Sweden,

September, 2007.

Table of Contents

Chapter 1

Introduction

1.1 Motivation

The consumption of electrical energy is an ever growing need worldwide. Yet, growing in tandem to it are concerns about environmental pollution, global warming and the steady depletion of fossil fuels. Electricity generation from renewable resources might be considered as a feasible solution for the next generations [1].

Traditional power systems implement large power generation plants that produce most of the power, which then is transmitted to large consumption centres and further distributed between different customers. This power system design structure has, at some locations, started to change [2] towards new scenarios at which distributed generation (DG) units are spread throughout the distribution network, as shown in Fig. 1.1 for two possible locations. These DGs utilize renewable resources such as wind turbines, photovoltaics, biomass, small hydro-turbines … etc. Beside their environmental benefits, DGs offer a low-cost way for the energy flow into the market since they do not imply substantial transmission losses due to their location near to the customers [3]. Moreover, they could present a reliable and uninterruptible source for the customers especially in rural areas [4] and micro grids [5]. In addition, a possibility where the DG could be beneficial is if it could help to supply load during contingencies until the utility can build up additional delivery capacity [6].

More advantages are introduced using power electronics interfaced DGs [7]. For instance, converter interfaced DGs can be designed to provide ancillary services to the utility; such as reactive power support, load balancing, voltage support, and harmonic mitigation [3]. Moreover, such DGs can be more energy efficient in the sense that they can provide more

energy production, more smooth power production (less dependent on the prime source variations), and controlled energy storage [9].

In addition to the above advantages, the integration of DGs is, to a large extent, owed to political decisions in many countries. For instance, the Swedish government has introduced a legislation (2003:113), which intended to encourage and increase the proportion of electricity produced from renewable resources [8]. The objective is that the amount of electricity produced from renewable resources will provide additional power of about 6.5% of the present total production by the year 2010.

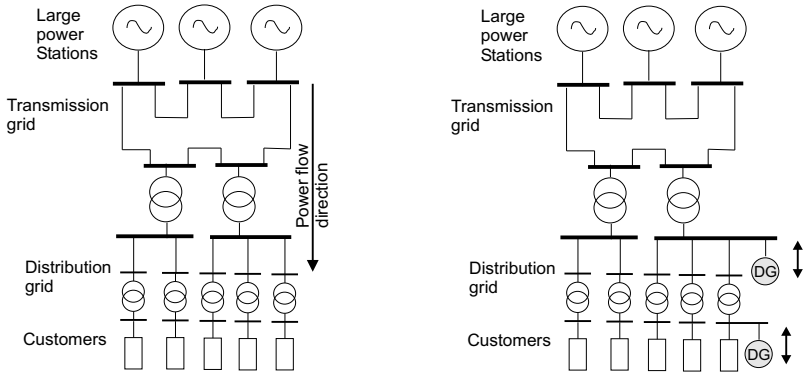

Fig. 1.1 Traditional power system (left) and penetration of distributed generation (right). The arrows present the power flow direction.

Even though large-scale implementation of DGs has several driving forces as mentioned above, there are major challenges concerning network interconnection issues that have to be solved. Grid connection of DGs is considered from two main prospects: power-system prospective and DG-technology prospective. As it is an essential part for the integration of DGs to achieve a reliable and improved performance of the power system, the DG interface to the grid is of focus in this work.

1.2 Background and related work

Background

Power conversion systems of distributed generation (DG) vary according to the nature of the input energy source. They may be implemented by using partially rated power electronics interface, as in wind turbine systems with doubly fed induction generators, or with fully rated power electronics interface [7]. The latter interface is the dominating one in applications related to fuel cells, solar cells, micro turbines and wind turbine systems [9]. There can be one or more power conversion stages in order to adjust the power of the energy source with the grid requirements, as shown in Fig. 1.2 [9]. With DC energy sources, the power electronics interface may consist of one DC/AC converter, or an intermediate DC/DC conversion stage can be added to achieve a specific goal, e.g. in order to regulate the output voltage so that the maximum available power is extracted [9]. The same is valid for AC sources, where they have to be adjusted to match the grid requirement by a DC intermediate stage. An energy storage unit could also be connected in the DC stage to adjust the energy injected into the utility grid in all operating conditions. The focus here will be on DG systems with a DC/AC power converter as a front end, where the DC-link voltage is either controllable or constant and the primary source input power is constant. The power converter to the grid enables a fast control over active and reactive power and could perform voltage and frequency control [10], [11]. Observe that, in order to control the active power, the primary source needs also to be controllable or an energy storage should be provided.

Voltage source converters (VSCs) using insulated gate bipolar transistor (IGBT) switches that are controlled by pulse width modulation (PWM) are used on the grid side at medium/high voltage due to their high controllability and low losses [12], [13], [14]. The good controllability promotes the use of the VSCs in grid connected applications to provide good power quality. An inherent part of a VSC is a filter inductor (L-filter), which is used to minimize the current harmonics injected into the grid [15] - [20].

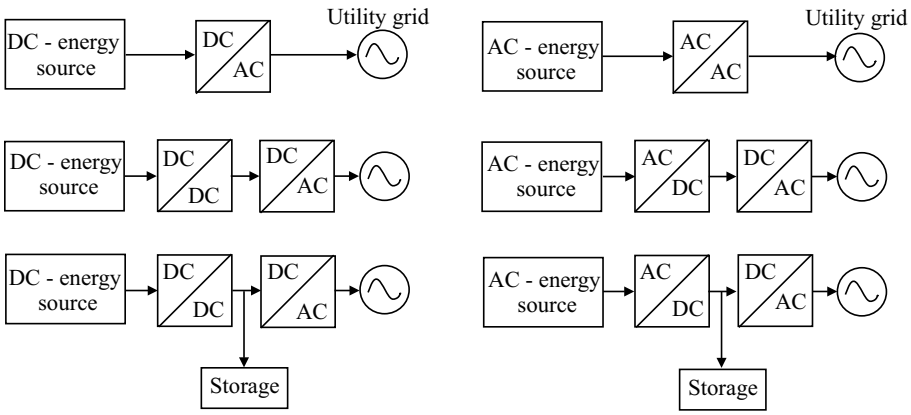

Fig. 1.2 Full-rated power electronics interfaced DG systems.

Like most of the power electronics equipment, an important drawback of using VSCs is their sensitivity to voltage disturbances, e.g. voltage dips [21]. In order to keep the DC-link voltage constant and minimize the grid current amplitude and harmonics during faults, the VSC controller is required to have two main functions: DC-link voltage regulation and current control. Most conventional current controllers have been designed under the assumption of balanced grid voltages [16]. These controllers show undesirable current control characteristics under unbalanced conditions because the current references are distorted by a second-order harmonic [16]. This is due to the negative-sequence voltage in the three-phase domain, which translates into a sinusoidal signal having a frequency of twice the grid frequency in a *dq*-frame synchronized with the positive-sequence voltage.

Related work

A comparison between different types of current controllers (CCs) for shunt-connected VSC based on their transient operation in case of voltage dips is presented in [17]. It has been shown that the dual vector current controller (DVCC) shows the best performance regarding grid current control and DC-link voltage regulation [16], [17]. This controller uses two different vector current controllers for the two sequence components,

together with a DC-link voltage controller based on the instantaneous active and reactive power theory.

Due to the PWM switching of voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [22]-[27]. Inserting an LCL-filter between the grid and the VSC eliminates high frequency harmonics even with lower switching frequency. Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. Damping methods are extensively addressed in literature. In [23] a resistance is used in series with the filter capacitor to passively damp the resonance. This resistance increases the system losses and decreases the efficiency of the filter. Instead, methods to actively damp the resonance are adopted as in [24], [25], [28]. In [25], a comparison between none-damped, passively-damped and actively-damped systems is carried out using Bode plots. It has been concluded that the active damping reduces the resonant peak as effectively as the passive damping. In [24], three cascaded controllers are used with the reference grid current generated from a DC voltage controller. The converter current and capacitor voltage are predicted. Moreover, two active resistances virtually connected in series with the filter inductor resistances are considered in the controller dead-beat gains. However, the use of these resistances is not justified. In [22], and [26] controllers with no damping are proposed. This has been proposed in [22] by controlling the grid current instead of the converter current and the proper choice of the filter parameters. However, by introducing a one sample time delay the system has been unstable acquiring the passive damping. In [26], two control loops are used: an outer current control loop and an inner capacitor voltage control loop. The latter is used to stabilize the controller and in the same time damp the resonance. The effect of adding a time delay has not been considered there as well.

The voltage compensation capability of VSCs' controllers has been also discussed in the literature to overcome the problem of having a decreased voltage at the connection point of the DG due to load/system dynamics [30]-[35], or to mitigate power quality problems [37], [38]. However, the effect of

the grid power quality on the phase locked loop (PLL), which is used to extract the grid phase angle, and on the compensation capability has not been treated in the literature. Moreover, in most of the literature the VSC is assumed to be either not injecting active power or has a controllable active power, which provides a wider compensation range.

One of the important capabilities of the DGs is to locally detect a grid outage condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, to prevent island operation. This capability has been discussed in the literature [39]- [45], where the transfer from grid-connected to island operation has been studied assuming a strong grid. The transfer from island to grid-connected mode is not much discussed. In [46], the load has been connected to the capacitor of the LCL-filter, at which its voltage is controlled in all the operating modes, to attain perfect transition without any transients. In [10], the DG was set into idle mode in case of grid recovery until the synchronization is achieved between the grid voltage and the DG voltage.

1.3 Purpose of the thesis and contributions

The main goals of the thesis and the contributions related to them are:

Goal 1: To determine the interface requirements and the capabilities of DGs with a voltage source converter (VSC) as a front end. For this purpose, two line filters are to be considered at the connection point of the DG; namely inductance line filter (L-filter) and inductance-capacitance-inductance line filter (LCL-filter). Vector current controllers are to be implemented for both systems.

Contribution 1: The derivation of the current reference generation equations, for the LCL-filter system, regarding the oscillating powers that are produced during the unbalanced grid voltage and compensating for them in two different ways. This has been presented in Section 2.5 and Paper A and Paper B.

Goal 2: To study the effect of voltage dips on the converter-interfaced DG and the requirements for ride-through capability.

Contribution 2: The study of all possible types of voltage dips that could appear at the terminals of a DG unit with both L-filter and LCL-filter systems. And, the derivation of the equations of maximum currents that would flow through the DG's converter switches. The main results of this point has been published in Paper B and explained in Section 3.5.

Goal 3: To study the effect of the other power quality problems on the DG operation, and how the DG controller could react in a corrective way to support the grid and provide better power quality at the connection point.

Contribution 3: A synthesis of a neural network based PLL has been proposed to reduce the error due to the voltage distortion, which has resulted in better compensation capability for the DG. This is shown in Paper E and in Section 4.5.

Goal 4: To study the possibility of intentional islanding for very weak grids.

Contribution 4: A passive detection algorithm that combines both the estimated frequency and the voltage regulator has been proposed to detect the islanding condition, especially in a weak grid. This has been shown in Section 5.4 and in Paper F and G, for various loads.

1.4 Thesis outline

The fundamental theory of the work is explained in details in **Chapter 2**. In that chapter the vector current controllers (VCC) for both the L-filter and the LCL-filter VSC-interfaced DG-systems are presented. The dual vector current controller (DVCC) has been implemented, for both systems, in order to achieve better current reference tracking in case of grid-voltage imbalance. Moreover, current reference equations are derived in such a way that they alleviate the DC-link ripples.

In **Chapter 3**, the voltage dips that could appear at the DG terminals are considered. An investigation of the ride-through capability is provided regarding the possible maximum currents that would flow through the VSC switches, and also regarding the DC-link voltage ripples. In addition, the maximum currents that would result during the dip period were obtained

using design equations that have been derived for various dips. Moreover, the DG system, both with the L-filter and the LCL-filter, has been examined for all possible voltage dips that could occur at its terminals. Recommendations of oversizing of the DG have been drawn as a consequence of that study.

If oversizing is not a possibility, the voltage regulation capability might appear as another possibility to correct the terminal voltage instead of riding through the voltage dip period. This is then discussed in **Chapter 4**. This capability might also be beneficial in case of operation in weak grids, where the voltage level is not constant and is dependent on the loads. Moreover, by compensating the grid voltage most of the power quality problems are mitigated. In this chapter, the voltage regulation capability is related to the performance of the phase locked loop (PLL) that estimates the phase angle of the grid voltage. A PLL that extracts the fundamental component of the grid voltage has been implemented using neural network technique.

In **Chapter 5**, the outage (and recovery) of the grid voltage has been considered, regarding the ability to keep the DG into operation to supply sensitive or critical loads. The main conclusions relating the different chapters and the possible future work considering the same topic are reported in **Chapter 6**.

1.5 Publications

The work in this thesis has resulted in eight publications, as shown in Fig. 1.3. The papers, designated in the figure from A to G, are supplemented at the end of this thesis with the same designation. The publications are also listed below with short description.

Journal papers

[J-1] F. Magueed, A. Sannino, and J. Svensson, "Design of Robust Converter Interface for Wind Power Applications," in *Wind Energy Journal, special issue on Electrical Integration of Wind Power*, vol. 8, no. 3, 2005, pp. 319 – 332.

In this paper the study of all possible voltage dips that could occur at the terminal of the DG is studied. This paper is designated as "Paper A" and supplemented at the final part of the thesis.

[J-2] F. Magueed, and T. Thiringer, "Comparison of Two PLL Configurations for Grid-Connected Current-Controlled Three-Phase VSC," *submitted to Electrical Power Quality and Utilization Journal*.
The neural network based PLL has been presented here and compared with the positive sequence based PLL. This paper is designated as "Paper E" and supplemented at the final part of the thesis.

[J-3] F. Magueed, G. Olsson, and T. Thiringer, "Active Islanding Detection Method in a Weak Grid using a Converter Interfaced Distributed Generation," *submitted to IEEE trans. on Power Delivery*.
An active islanding detection method is proposed, which consists of an under/over frequency passive detection algorithm, a PCC-voltage regulator and a DG reactive current limiter. This paper is designated as "Paper G" and supplemented at the final part of the thesis.

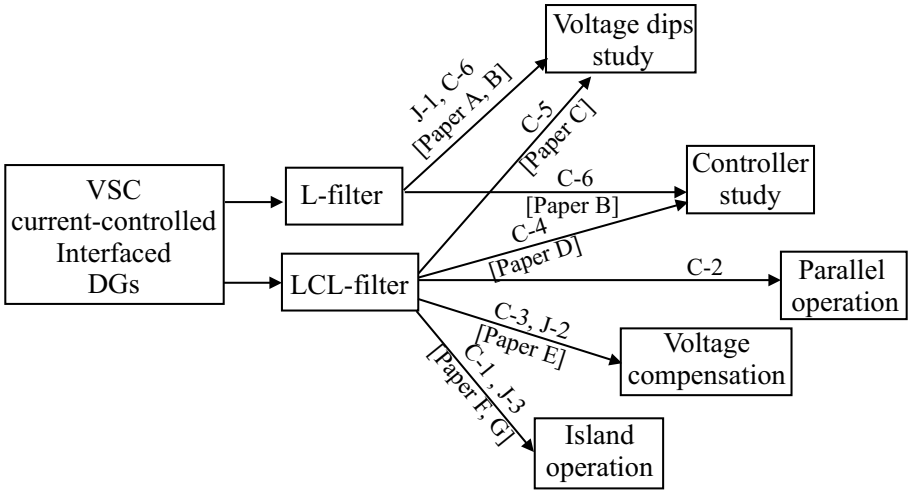

Fig. 1.3 Thesis outline with the resulting publication.

Conference papers (peer reviewed)

[C-1] F. Magueed, and J. Daalder, "Operation of Distributed Generation in Weak Grids with Local Critical Load," at *IEEE Annual Industrial*

Electronics Conference (IECON'06), Paris, France, November 7-10, 2006.

The passive islanding detection algorithm has been presented here with the focus on the operation in weak grids. This paper is designated as "Paper F" and supplemented at the final part of the thesis.

[C-2] F. Magueed, and J. Daalder, "Parallel Operation of Distributed Generation in Weak Distribution Systems," at the *12th International Power Electronics and Motion Control Conference (EPE-PEMC'06)*, Slovenia, August 30 - September 1, 2006, pp. 531 – 536.

A discussion of the voltage compensation limits and the possible parallel operation of DGs to provide better compensation capability is introduced.

[C-3] F. Magueed, and H. Awad, "Voltage Compensation in Weak Grids Using Distributed Generation with Voltage Source Converter as a Front End," at the *6th International Conference on Power Electronics and Drive Systems (PEDS'05)*, Kuala Lumpur, Malaysia, Nov 28 - Dec 1, 2005, pp. 234 – 239.

The main voltage regulator is presented here, with the capability to compensate for voltage dips at the grid.

[C-4] F. Magueed, and J. Svensson, "Control of VSC Connected to the Grid through LCL-Filter to Achieve Balanced Currents," at the *IEEE Industry Applications Society 40th Annual Meeting (IAS'05)*, Kowloon, Hong Kong, October 2-6, 2005.

The control of the VSC is presented here, in case of unbalanced voltage dips at the grid, to provide balanced DG currents. This paper is designated as "Paper D" and supplemented at the final part of the thesis.

[C-5] F. Magueed, J. Svensson, and A. Sannino, "Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage conditions," in *Proc of Power Tech Conference (PT'05)*, St. Petersburg, Russia, June 27-30, 2005.[1]

The performance of the LCL-filter system has been discussed regarding the voltage dips at the grid. This paper is designated as "Paper C" and supplemented at the final part of the thesis.

[1] This paper has been awarded ***High quality paper certificate*** for the presentation from 2005 IEEE Power Tech conference (June 27-30 2005).

[C-6] F. Magueed, A. Sannino, and J. Svensson, "Transient Performance of Voltage Source Converter under Unbalanced Voltage Dips," in *Proc. of Power Electronics Specialists Conference (PESC'04)*, Aachen, Germany, June 20-25 2004, pp. 1163 – 1168.

The study of voltage dips with phase angle jumps and the compensation of the oscillating powers using two different ways have been presented in this paper. This paper is designated as "Paper B" and supplemented at the final part of the thesis.

Chapter 2

Power Electronics Interfaced Distributed Generation – Controller Description

In this chapter, a general description of the power conversion systems, i.e. power electronics interface, for distributed generation is given. Two distributed generation systems are considered with two different line filters; namely an inductance line filter and an inductance-capacitance-inductance line filter, and a voltage source converter as a front end for the energy source. Vector current controllers are proposed for the two systems. The description of the controllers is given in details. Moreover, the generation algorithm for the current references is provided.

2.1 Current-controlled voltage source converters

Current controllers are preferred for shunt connected voltage source converters (VSCs) in order to increase stability of the closed loop and to decrease the time response in case of load transients [19]. Accordingly, a vector current controller (VCC) is considered throughout this work in order to obtain a high performance controller. In a VCC, the active and reactive currents (consequently powers) can be controlled independently. And, as indicated above, a high bandwidth controller with low cross-coupling effect between active and reactive currents can be achieved [20].

In Fig. 2.1, a scheme of the VSC system connected to the grid via a line filter along with the VCC is shown. Since the application of the distributed generation utilizing renewable resources is considered, the variation of the input current i_{in} is relatively slow compared to the response time of the controller. Hence, i_{in} is modelled as a constant current source. In addition,

the DC-link voltage should be regulated to maintain a constant voltage in case of grid voltage variations (e.g. voltage dips). The DC voltage regulator is implemented as a proportional-integral (PI) controller, where the measured DC capacitor voltage u_{dc} is compared with its reference value u_{dc}^{*} and the error signal is used to produce a reference DC current i_{dc}^{*} according to

$$i_{\mathrm{dc}}^{*} = \Delta u_{dc} k_{\mathrm{pdc}} \left(1 + \frac{1}{s T_{\mathrm{idc}}} \right) \tag{2-1}$$

where

k_{pdc}, T_{idc} are the proportional gain and integral time of the PI-controller respectively with their values as given in Appendix D;

s is the Laplace operator; and

$\Delta u_{\mathrm{dc}} = u_{\mathrm{dc}} - u_{\mathrm{dc}}^{*}$.

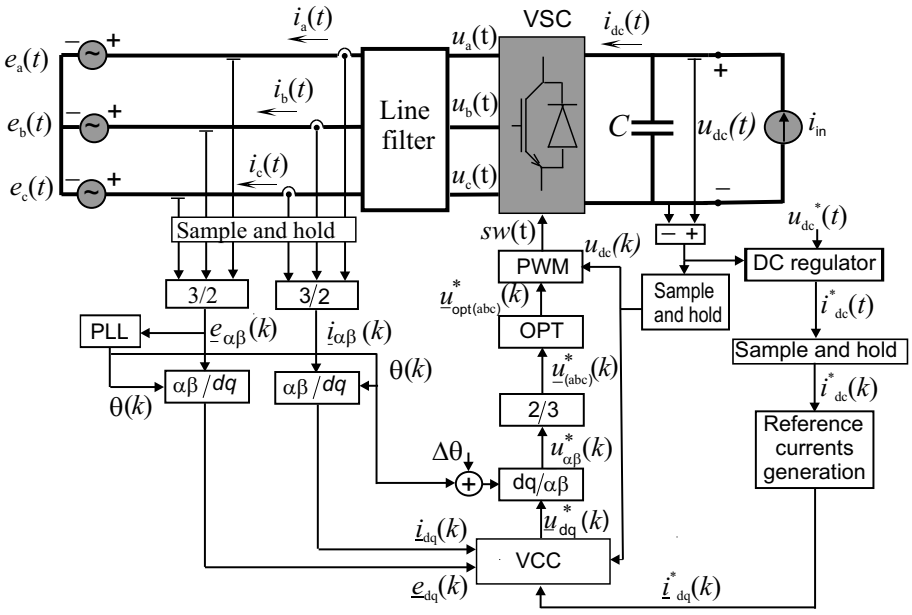

Fig. 2.1 Schematic diagram showing VSC, grid, filter and controller.

The signal flow from the power circuit to the VCC is as follows. The three-phase AC currents and voltages are first sampled and transformed into

the $\alpha\beta$-stationary frame[2]. The resulting rotating vectors $\underline{e}_{\alpha\beta}$ and $\underline{i}_{\alpha\beta}$ are then transformed into the rotating *dq*-frame that is synchronized with the grid voltage using a phase-locked-loop (PLL) that extracts the grid voltage angle θ. The *dq*-vectors of the measured voltages and currents, $\underline{e}_{\mathrm{dq}}$ and $\underline{i}_{\mathrm{dq}}$ respectively, are then used along with the reference current vector $\underline{i}^{*}_{\mathrm{dq}}$ by the VCC to produce the reference voltage vector $\underline{u}^{*}_{\mathrm{dq}}$. The different coordinate transformations are provided in Appendix A, where the *d*-component refers to the real value while the *q*-component refers to the imaginary value of a vector.

The reference currents are produced in such a way as to decrease the DC-link voltage ripple using a "reference currents generation" algorithm that uses the signal coming from the DC-link voltage regulator, and is explained later in this chapter. The reference voltage vector is then transformed to a vector in the $\alpha\beta$-frame using a transformation angle of $\theta+\Delta\theta$, where $\Delta\theta$ compensates for the transformation angle error due to one sample calculation time delay of the controller. The vector $\underline{u}^{*}_{\alpha\beta}$ is then transformed into three-phase control signals. Those signals are then used in the PWM modulator to produce the switching pattern for the VSC. The PWM is optimized to increase the maximum output voltage of the converter without increasing the DC-link voltage [12], [14]. The block "OPT" injects a zero sequence voltage into the control signals. Due to the absence of a neutral wire, the added zero sequence waveforms are cancelled out.

It should be mentioned that the design of the VCC is different for the power circuit with an inductance line filter from the power circuit with inductance-capacitance-inductance line filter, since both circuits have different time and frequency behaviors. Also the generation of reference currents is different for the two filter configurations. This is shown in the next sections.

[2] The coordinate transformation matrices are explained in Appendix A.

2.2 Vector Current Controller with inductance line filter

An inductance line filter is first considered. The plant in Fig. 2.2 represents the filter, the PWM, and the VSC. The last two, however, are assumed to be ideal, having a transfer function of 1. The plant transfer function in the *s*-domain is then represented as

$$G_{\mathrm{pl}}(s) = \frac{1}{sL_{\mathrm{f}} + R_{\mathrm{f}}} \tag{2-2}$$

where

L_{f} is the filter inductance; and

R_{f} is the filter resistance.

The controller design is based on deadbeat control. The measured voltage and current vectors are used to calculate the feedforward vector $\underline{FF}_{\mathrm{dq}}$ as

$$\underline{FF}_{\mathrm{dq}}(k) = \underline{e}_{\mathrm{dq}}(k) + \underline{i}_{\mathrm{dq}}(k)(R_{\mathrm{f}} + \mathrm{j}\omega L_{\mathrm{f}}) \tag{2-3}$$

where

ω is the angular frequency of the grid voltage;

k is the sampling instant; and

j is the imaginary unit.

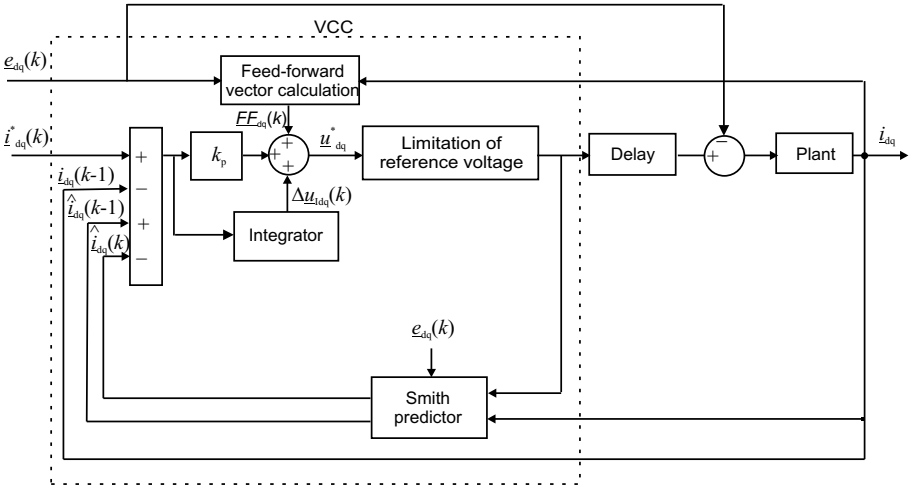

Fig. 2.2 Deadbeat based vector current controller (VCC) for DG with L-filter.

The change in the current reference is met by a change in the voltage reference that is produced by adding $\underline{FF}_{\mathrm{dq}}$ to the output of a PI-controller with a proportional gain k_p, also called here dead-beat gain. The dead-beat strategy has been described in [20]. The Dead-beat gain is given in terms of the filter parameters as

$$k_{\mathrm{p}} = \frac{L_{\mathrm{f}}}{T_{\mathrm{s}}} + \frac{R_{\mathrm{f}}}{2}. \tag{2-4}$$

An integral part $\Delta\underline{u}_{\mathrm{idq}}$ is needed to remove the static errors caused by non-linearity, noisy measurements and non-ideal components. The generated reference voltage is then calculated as

$$\underline{u}^{*}_{\mathrm{dq}}(k+1) = \underline{FF}_{\mathrm{dq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idq}}(k). \tag{2-5}$$

The integral part is implemented as

$$\Delta\underline{u}_{\mathrm{idq}}(k+1) = \Delta\underline{u}_{\mathrm{idq}}(k) + \underline{\varepsilon}_{\mathrm{idq}}(k)k_{\mathrm{i}} \tag{2-6}$$

where k_{i} is the integration constant, which can be written as

$$k_{\mathrm{i}} = \frac{k_{\mathrm{p}}T_{\mathrm{s}}}{T_{\mathrm{i}}} \tag{2-7}$$

where T_{i} is the integral time constant, which is chosen to be equal to the L-filter time constant $T_{\mathrm{i}} = \frac{L_{\mathrm{f}}}{R_{\mathrm{f}}}$, and T_{s} is the sampling time.

The current error vector $\underline{\varepsilon}_{\mathrm{idq}}$ is described by

$$\underline{\varepsilon}_{\mathrm{idq}}(k) = \underline{i}^{*}_{\mathrm{dq}}(k) - \underline{i}_{\mathrm{dq}}(k-1) + \hat{\underline{i}}_{\mathrm{dq}}(k-1) - \hat{\underline{i}}_{\mathrm{dq}}(k) \tag{2-8}$$

which accounts for a one sample time delay in the measured current signal due to the calculation time of the digital controller. This delay has been compensated for using the estimated current $\hat{i}_{\mathrm{dq}}$ at two successive instants,

which is calculated by a Smith predictor [48], [76]. The Smith predictor is implemented in a way analogous to a state observer[3], as proposed by [20], which means running a model of the plant in parallel to the plant itself. In steady state, the estimated and actual currents should be equal, hence $\underline{i}_{\mathrm{dq}}(k-1)=\hat{\underline{i}}_{\mathrm{dq}}(k-1)$ in (2-8), which cancels the time delay effect.

The output reference voltage command is also limited to be inside the control region, which is described by a hexagon composed of six equilateral triangles with a side length of $\sqrt{2/3}u_{\mathrm{dc}}$. In this work the minimum amplitude error (MAE) limiting method has been adopted [20]. In this method a new reference voltage vector on the hexagon boundary that is closest to the original reference vector is chosen as explained by Fig. 2.3. This is done by mapping the voltage reference into new coordinates *xy*. The *xy*-coordinate position depends on the number of the sector in the hexagon that contains the voltage reference. The reference voltage vector in the new coordinates u_{xy}^{*} is obtained as

$$\underline{u}_{\mathrm{xy}}^{*}=\underline{u}_{\alpha\beta}^{*}e^{-\mathrm{j}\theta_{\mathrm{xy}}} \tag{2-9}$$

where θ_{xy} is the angle between the α-axis and the *x*-axis and is calculated as

$$\theta_{\mathrm{xy}}=\left(1+2(n-1)\right)\pi/6 \tag{2-10}$$

where *n* is the sector number at which the reference vector lies in the hexagon.

The components of the limited reference voltage vector are calculated from Fig. 2.3 as

$$u_{\mathrm{x}}=\frac{u_{\mathrm{dc}}}{\sqrt{2}} \tag{2-11}$$

[3] The use of the Smith predictor is described in more details in Paper D.

$$u_{\mathrm{y}} = \begin{cases} u_{\mathrm{y}}^{*} & \left|u_{\mathrm{y}}^{*}\right| \le \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \\ sign(u_{\mathrm{y}}^{*}) \cdot \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} & \left|u_{\mathrm{y}}^{*}\right| > \dfrac{u_{\mathrm{dc}}}{\sqrt{6}} \end{cases} . \tag{2-12}$$

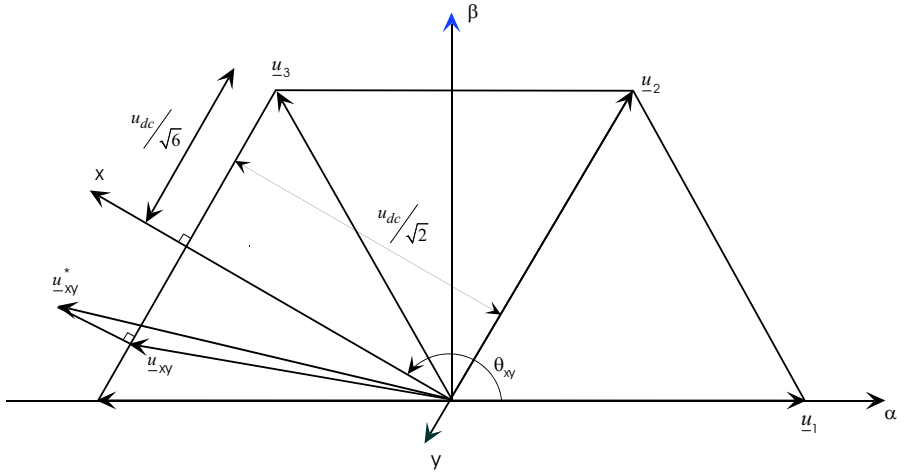

Fig. 2.3 Principle of the minimum amplitude error method.

It is worth noting here that using the limited voltage reference as an input for the Smith predictor, as shown in Fig. 2.2, is important in providing an anti-windup property for the controller, which is useful in case of increased current steps.

The time domain performance of the controller is tested in Fig. 2.4, for the case of a substantial positive active current step, which is considered the worst operational case since it leads the voltage to the saturation area. Due to the high current step of 1.5 p.u. that has been applied at 0.2 s, the controller will go into the voltage reference limitation algorithm, at which the reference voltage will be limited as shown by the same figure. Since the demanded reference voltage, required to achieve the current step, has not been reached, the dead-beat is not accomplished. Hence, it will take several samples for the current to reach its reference value. As shown by the figure, the current will accomplish the step in 2 ms. The figure also shows the cross-coupling effect

on the *q*-component of the current. To eliminate this coupling effect, i_{q}^{*} might be modified to counteract the effect of the active current step [20]. However, this will not be considered here since the reference *q*-component current will be implemented later to compensate for various power quality problems at the grid.

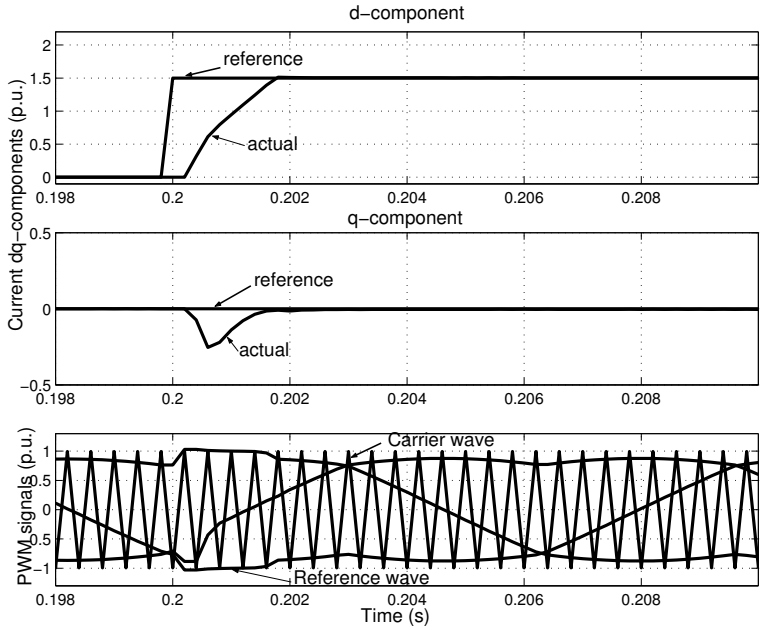

Fig. 2.4 Active current (upper), reactive current (middle), and PWM signals (lower), due to a step in i_{d}^{*} from 0 to 1.5 p.u.

2.3 Dual vector current controller (DVCC)

In case of an unbalanced grid voltage, the voltage vector in the *dq*-frame has oscillations at a frequency of twice the fundamental frequency due to the negative sequence that exists in the grid voltage. That will lead to oscillations in the injected currents to the grid. To deal with that situation a dual vector current controller (DVCC) [18] can be used. The DVCC consists

of two separate VCCs, one for controlling the positive-sequence voltage and the other for controlling the negative-sequence voltage. This controller synthesis has proved to give the best performance regarding grid current control and DC-link voltage regulation [17]. A simplified scheme for the DVCC is shown in Fig. 2.5.

The positive sequence PI-controller is described in the positive *dq*-frame (*dqp*-frame), which rotates in the positive direction, as

$$\underline{u}^{*}_{\mathrm{dqp}}(k+1) = \underline{FF}_{\mathrm{dqp}}(k) + \underline{\varepsilon}_{\mathrm{idqp}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqp}}(k) \qquad (2\text{-}13)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqp}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqp}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqp}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The negative sequence PI-controller is described in the negative *dq*-frame (*dqn*-frame), which rotates in the negative direction, as

$$\underline{u}^{*}_{\mathrm{dqn}}(k+1) = \underline{FF}_{\mathrm{dqn}}(k) + \underline{\varepsilon}_{\mathrm{idqn}}(k)k_{\mathrm{p}} + \Delta\underline{u}_{\mathrm{idqn}}(k) \qquad (2\text{-}14)$$

where the feedforward vector $\underline{FF}_{\mathrm{dqn}}$, the error vector $\underline{\varepsilon}_{\mathrm{dqn}}$ and the integral vector $\Delta\underline{u}_{\mathrm{idqn}}$ are defined in a way analogous to (2-3), (2-8), and (2-6) respectively.

The decomposition of the supply voltage into positive and negative sequence components is performed using the delayed signal cancellation (DSC) algorithm, which has been first proposed in [77]. This algorithm is implemented in the *dq*-frame, which rotates in the positive direction, in the same way as suggested in [17]. In this frame, the positive sequence is a constant vector (constant amplitude and fixed direction), while the negative sequence is a rotating vector, which rotates with twice the line frequency in the opposite direction, as compared with the positive sequence.

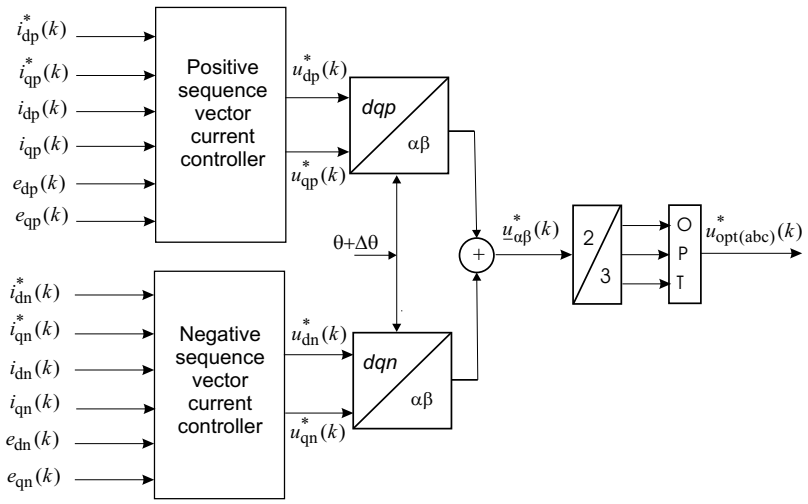

Fig. 2.5 Simplified block diagram of dual vector current controller (DVCC).

In the DSC the measured supply voltage, in the *dq*-frame, and the same signal, delayed by one-quarter of a fundamental frequency period, are considered. Delaying the signal gives a vector composed by the same positive sequence component and a negative sequence component which has equal amplitude but opposite sign. Therefore, if the signal delayed by one-fourth of period is added to the measured supply voltage, the negative sequence voltage will be removed.

The positive sequence voltage vector can thus be extracted from the measured values as

$$\underline{e}_{\mathrm{dqp}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) + \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-15}$$

where T is the period at the fundamental frequency.

The negative sequence can be obtained in the positive rotating plane, as follows

$$\underline{e}_{\mathrm{dqn}_{(\mathrm{p})}}(t) = \frac{1}{2} \cdot \left(\underline{e}_{\mathrm{dq}}(t) - \underline{e}_{\mathrm{dq}}\left(t - \frac{T}{4} \right) \right) \tag{2-16}$$

which is then transformed into the negative rotating plane by transforming it into the $\alpha\beta$-frame and back into the *dqn*-frame using the opposite angle.

The time domain response of the DVCC is compared with the time domain response of the VCC when a grid voltage of 40% imbalance ratio is applied. Moreover, a step in the active current reference is applied at 0.25 s. The injected current is oscillating in the case of using the VCC, as shown in Fig. 2.6, while better tracking is achieved using the DVCC.

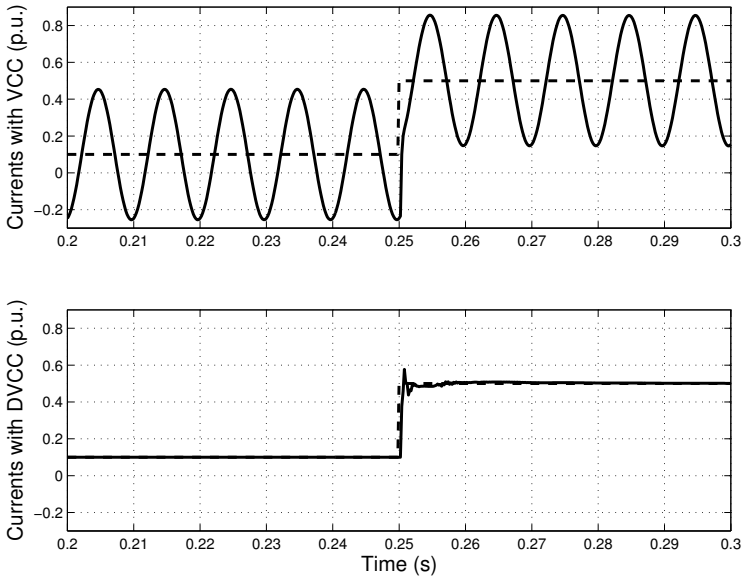

Fig. 2.6 Active grid current i_d (solid) and reference current i^*_d (dashed); with VCC (upper) and DVCC (lower).

2.4 Current reference generation with inductance line filter

In the case of a controllable DC-link voltage, proper current references should be generated in order to improve the performance of the VCC. Two performance measures are considered, which are the minimization of the DC-link voltage ripple and the decrease of the AC currents amplitudes and/or harmonics. The reference currents generation algorithm is based on

the instantaneous power theory [80]. The active power on the AC side of the converter, p_1, is considered equal to the active power on the DC side, P_{dc}, neglecting the switching losses. The power balance equation can be expressed as

$$\begin{bmatrix} p_1 \\ q_1 \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \Delta p \\ \Delta q \end{bmatrix} \tag{2-17}$$

where p_1 and q_1 are the instantaneous active and reactive powers at the AC-side of the converter respectively. The terms Δp and Δq are active and reactive powers dissipated by the filter respectively, and can be calculated instantaneously as

$$\Delta p = R_f \left(i_d^2 + i_q^2 \right) \tag{2-18}$$

$$\Delta q = \omega L_f \left(i_d^2 + i_q^2 \right). \tag{2-19}$$

The instantaneous active power p_2 and reactive power q_2 at the grid are calculated as:

$$\begin{aligned} p_2 &= e_d i_d + e_q i_q \\ q_2 &= -e_d i_q + e_q i_d \end{aligned}. \tag{2-20}$$

To achieve unity power factor, the reactive power at the grid side $q_2 = q_1 - \Delta q$ is nullified. The current references are then calculated using (2-17) as follows

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \end{bmatrix}. \tag{2-21}$$

2.5 Current reference generation for inductance line filter and unbalanced grid voltage

For the DVCC, current reference signals should be provided in the positive and the negative *dq*-coordinates. The derivation[4] is carried out in the same way as for the VCC. The current references are calculated using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ q_{\mathrm{ac},2} \\ p_{\mathrm{s}2,1} - \Delta p_{\mathrm{s}2} \\ p_{\mathrm{c}2,1} - \Delta p_{\mathrm{c}2} \end{bmatrix} \tag{2-22}$$

where the instantaneous active power p_2 and reactive power q_2 at the grid are

$$\begin{aligned} p_2(t) &= p_{\mathrm{ac},2} + p_{\mathrm{c}2,2}\cos(2\omega t) + p_{\mathrm{s}2,2}\sin(2\omega t) \\ q_2(t) &= q_{\mathrm{ac},2} + q_{\mathrm{c}2,2}\cos(2\omega t) + q_{\mathrm{s}2,2}\sin(2\omega t) \end{aligned} \tag{2-23}$$

with the following subscripts notations

ac - stands for the power at the fundamental frequency;

2 - stands for the grid side.

1 - stands for the AC converter side;

c2 - stands for the cosine component of a power that is oscillating with double the fundamental frequency; and

s2 - stands for the sine component of a power that is oscillating with double the fundamental frequency.

The power loss through the filter is encountered for in (2-22) by the terms Δp, $\Delta p_{\mathrm{s}2}$, and $\Delta p_{\mathrm{c}2}$.

Equation (2-22) has been considered in two ways, which are referred to as case 1 and case 2. The injected reactive power $q_{\mathrm{ac},2}$ to the grid is assumed to be zero in both cases.

[4] Details are given in Paper A and Paper B.

Case 1- The oscillating powers flow from the VSC side to the filter

Assuming that the converter supplies the oscillating power to the filter, and neglecting the converter losses which means $p_{ac,1}$ is equal to P_{dc}, the following equations will describe the different powers

$$P_{c2,1} = \Delta P_{c2},\ P_{c2,2} = 0 \tag{2-24}$$

$$P_{s2,1} = \Delta P_{s2},\ P_{s2,2} = 0 \quad . \tag{2-25}$$

Substituting in (2-22), the reference currents are calculated as

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qn} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{dc} - \Delta p \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{2-26}$$

Using (2-26), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.7.

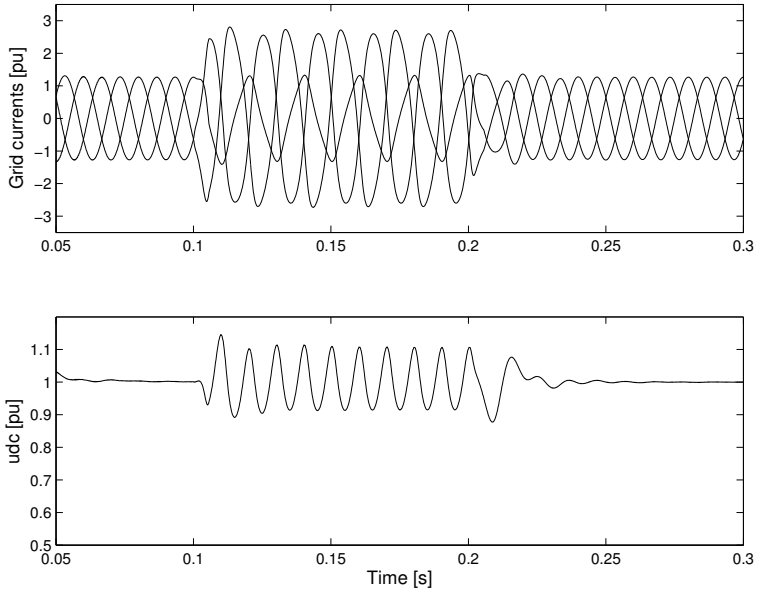

Fig. 2.7 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

Case 2- The oscillating powers flow from the grid side to the filter

In this case the grid is forced to supply the oscillating powers to the filter, by using the following equation

$$\begin{bmatrix} i_{\mathrm{dp}}^{*} \\ i_{\mathrm{qp}}^{*} \\ i_{\mathrm{dn}}^{*} \\ i_{\mathrm{qn}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{dp}} & e_{\mathrm{qp}} & e_{\mathrm{dn}} & e_{\mathrm{qn}} \\ e_{\mathrm{qp}} & -e_{\mathrm{dp}} & e_{\mathrm{qn}} & -e_{\mathrm{dn}} \\ e_{\mathrm{qn}} & -e_{\mathrm{dn}} & -e_{\mathrm{qn}} & e_{\mathrm{dp}} \\ e_{\mathrm{dn}} & e_{\mathrm{qn}} & e_{\mathrm{dp}} & e_{\mathrm{qp}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ 0 \\ -\Delta p_{\mathrm{s2}} \\ -\Delta p_{\mathrm{c2}} \end{bmatrix}. \qquad (2\text{-}27)$$

Using (2-27), with a grid-voltage imbalance (due to a double-phase fault at a remote location) from 0.1 s to 0.2 s, the resulting grid currents and the DC-link voltage are shown in Fig. 2.8.

Comparing Fig. 2.7 and Fig. 2.8, it is concluded that it is preferred to use the current reference generation in (2-27) over (2-26) since the DC-link voltage ripples are reduced during the fault period.

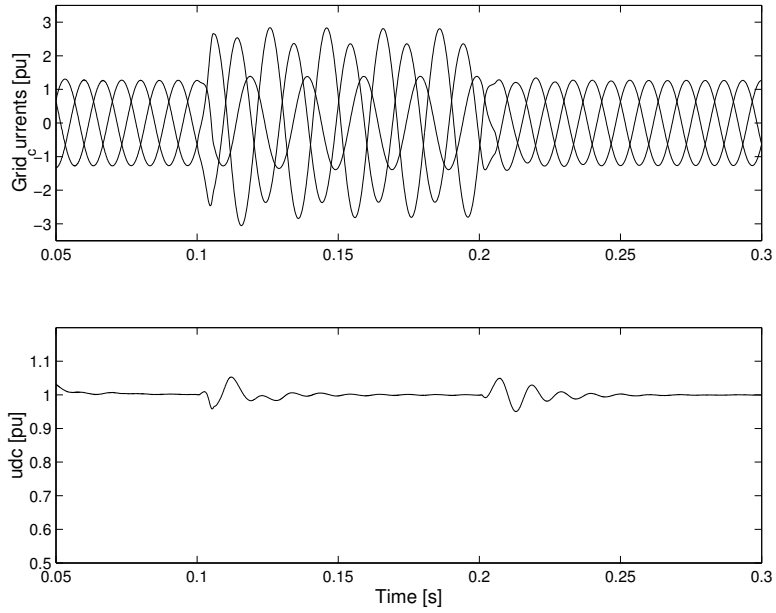

Fig. 2.8 Grid-currents (upper) and DC-link voltages (lower) due to a double phase fault at the grid lasting from 0.1 s to 0.2 s.

2.6 Vector Current Controller with inductance-capacitance-inductance line filter

Due to the PWM switching of the voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [29]. Inserting an LCL-filter[5] between the grid and the VSC, as shown in Fig. 2.9, eliminates high frequency harmonics even with lower switching frequency.

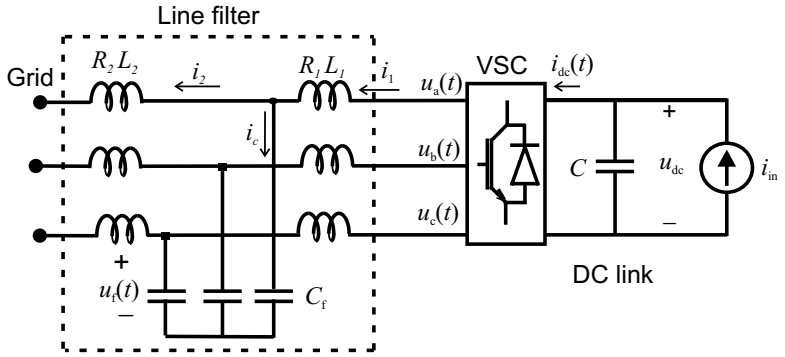

Fig. 2.9 Power circuit of DG system with VSC as a front end and an LCL-filter.

Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. In this work, a cascade control structure ([47], [48], and [49]) has been implemented to increase the stability margin and at the same time to damp oscillations at the resonant frequency of the LCL-filter. As shown in Fig. 2.10, the plant is described by three cascaded transfer functions; G_{p1}, G_{p2}, and G_{p3}, as

[5] The design of the LCL-filter parameters that are adopted here is given in Appendix B.

$$G_{\mathrm{p1}}(s)=\frac{I_2(s)}{U_{\mathrm{f}}(s)-E(s)}=\frac{1}{sL_2+R_2}$$
$$G_{\mathrm{p2}}(s)=\frac{U_{\mathrm{f}}(s)}{I_1(s)-I_2(s)}=\frac{1}{sC_{\mathrm{f}}} \tag{2-28}$$
$$G_{\mathrm{p3}}(s)=\frac{I_1(s)}{U(s)-U_{\mathrm{f}}(s)}=\frac{1}{sL_1+R_1}$$

where

$I_2(s)$ is the Laplace function of the grid side current $i_2(t)$;

$U_{\mathrm{f}}(s)$ is the Laplace function of the filter capacitor voltage $u_{\mathrm{f}}(t)$;

$E(s)$ is the Laplace function of the grid voltage $e(t)$;

$I_1(s)$ is the Laplace function of the converter side current $i_1(t)$; and

$U(s)$ is the Laplace function of the converter output voltage $u(t)$.

The inner controller G_{c3} is used for stabilization of G_{p3} and is designed using dead-beat control strategy. The two outer controllers G_{c2} and G_{c1} are used to stabilize G_{p2} and G_{p1} respectively. G_{c2} is implemented as a P-controller, while G_{c1} is implemented as a PI-controller where the integral part is added to eliminate the steady state error. With the resulting controller, shown in Fig. 2.10, the two controllers G_{c1} and G_{c2} are acting like one PI-controller. The outer controller G_{c1} is a two-degree of freedom controller, since it is using the output signal of a Smith predictor (with a compensation gain k_{ps}) to cancel the time delay effect. The time-delay free plant transfer-function G_{pm} represents the LCL-filter model in steady state, where the capacitor effect is neglected.

The three controllers are described in the rotating dq-frame as follows

$$\underline{y}_{\mathrm{1dq}}(k)=k_{\mathrm{p1}}\left(\underline{\varepsilon}_{\mathrm{idq}}(k)+\frac{T_{\mathrm{s}}}{T_{\mathrm{i}}}\sum_{n=0}^{k}\underline{\varepsilon}_{\mathrm{idq}}(n)\right) \tag{2-29}$$

$$\underline{y}_{\mathrm{2dq}}(k)=k_{\mathrm{p2}}\,\underline{y}_{\mathrm{1dq}}(k) \tag{2-30}$$

$$\underline{u}^{*}_{\mathrm{dq}}(k+1)=\underline{u}_{\mathrm{fdq}}(k)+(R_1+\mathrm{j}\omega L_1)\underline{i}_{\mathrm{1dq}}(k)+k_{\mathrm{p3}}\,\underline{y}_{\mathrm{2dq}}(k) \tag{2-31}$$

where

$\underline{y}_{1dq}$ is the output vector of G_{c1}, which represents the change in the capacitor voltage $\underline{u}_{fdq}$;

k_{p1} is the proportional gain of G_{c1};

T_i is the integral time of G_{c1};

$\underline{y}_{2dq}$ is the output vector of G_{c2}, which represents the required change in the converter side current $\underline{i}_{1dq}$;

k_{p2} is the proportional gain of G_{c2}; and

k_{p3} is the proportional gain of G_{c3}.

The current error vector $\underline{\varepsilon}_{idq}$ is the input to the outer controller G_{c1}, and is described in the same way as in (2-8).

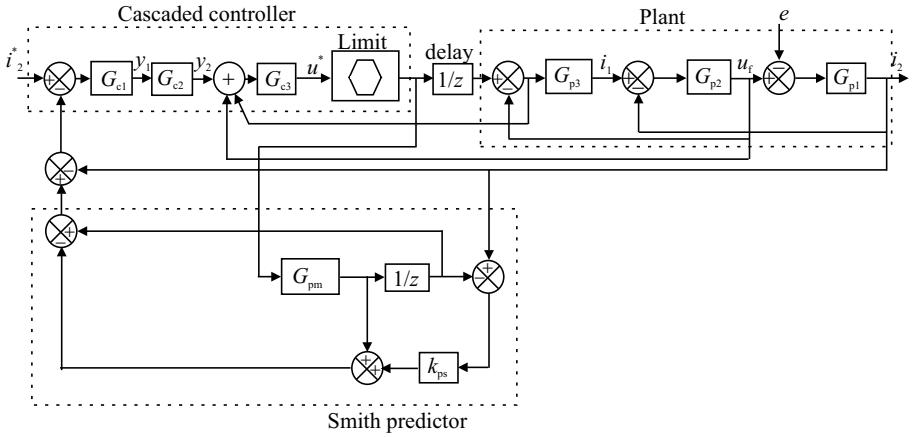

Fig. 2.10 Schematic diagram of the proposed cascaded controller (the z denotes the z transform, thus $1/z$ denotes a delay of one sample). Note that the controller is described in discrete form while the plant is described in continuous form.

The faster the inner loop is in comparison with the outer loops, the better the performance of the cascaded control system becomes in the sense of the transient response [49]. However, reduced gains for the outer controllers will reduce the overall bandwidth of the system. Hence, the inner controller gain is set to the dead-beat gain as [20]

$$k_{\mathrm{p3}} = \frac{L_1}{T_\mathrm{s}} + \frac{R_1}{2} \ . \tag{2-32}$$

The Smith predictor gain is set to a small value to stabilize the overall controller, while k_{p2} and k_{p1} are tuned by changing their values and examining the Bode plot. In Fig. 2.11 the value of k_{p2} is set to 30% of k_{p3}, while k_{p1} assumes values between 30% and 100% of k_{p2}. The same is performed in Fig. 2.12 by setting k_{p1} as 70% of k_{p2}, to achieve a high bandwidth and no overshoot, while k_{p2} is taking values between 25% and 70% of k_{p3}. It is shown by the phase plot in the figure that for k_{p2} values of 70% to 50% of k_{p1} the controller becomes unstable. Hence, the value of k_{p2} has been chosen to 30% of k_{p1}. The values used for the gains are listed in Appendix D.

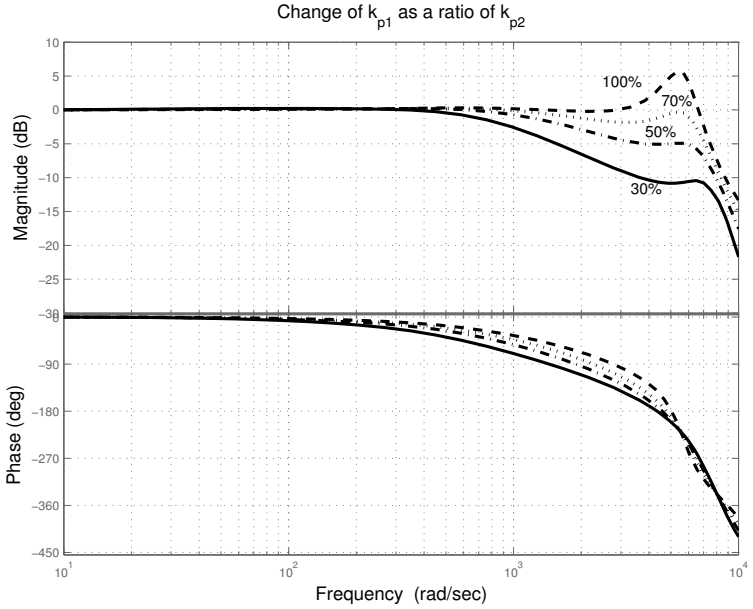

Fig. 2.11 The closed loop system frequency performance as k_{p1} is changed as a certain percentage of k_{p2}, with k_{p2} constant.

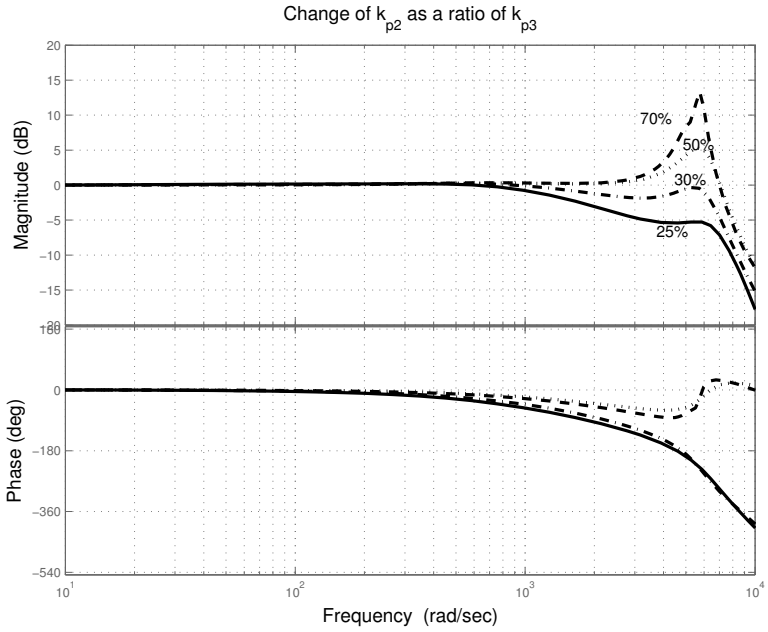

Fig. 2.12 The closed loop system frequency performance as k_{p2} is changed as a certain percentage of k_{p3}, while k_{p1} is constant.

2.7 Current reference generation with inductance-capacitance-inductance line filter

The current references are generated, in the same way as for the L-filter, as

$$\begin{bmatrix} i_{2\mathrm{d}}^{*} \\ i_{2\mathrm{q}}^{*} \end{bmatrix} = \begin{bmatrix} e_{\mathrm{d}} & e_{\mathrm{q}} \\ e_{\mathrm{q}} & -e_{\mathrm{d}} \end{bmatrix}^{-1} \begin{bmatrix} P_{\mathrm{dc}} - \Delta p \\ \omega C_{\mathrm{f}} \left(u_{\mathrm{cd}}^{2} + u_{\mathrm{cq}}^{2} \right) \end{bmatrix} - \begin{bmatrix} -\omega C_{\mathrm{f}} u_{\mathrm{cq}} \\ \omega C_{\mathrm{f}} u_{\mathrm{cd}} \end{bmatrix} \quad (2\text{-}33)$$

where Δp is the active power dissipated in the filter, and is a function of the grid side and converter side currents

$$\Delta p = R_1\left(i_{1d}^2 + i_{1q}^2\right) + R_2\left(i_{1d}i_{2d} + i_{1q}i_{2q}\right) + \omega L_2\left(-i_{1d}i_{2d} + i_{1q}i_{2d}\right). \tag{2-34}$$

The current references are generated in the same manner for the DVCC[6].

2.8 Conclusions

Two distributed generation systems with a voltage source converter as a front end and two line filters; namely L-filter and LCL-filter, are considered. Vector current controllers have been proposed to control the injected grid currents for both systems. The controller for the L-filter system is based on the dead-beat control and is modified to deal with one sample time delay, integrator windup, grid voltage saturation and grid voltage imbalance. The controller shows good reference tracking even in the worst case of increased current steps. In addition, in the case of controllable DC-link voltage, the current references have been derived in such a way that a regulated DC-link voltage is provided even in the case of unbalanced grid voltage. On the other hand, a cascaded current controller has been proposed for the LCL-filter system. The current references have also been derived in the same manner as for the L-filter system.

[6] The detailed derivation is given in Appendix E and Paper C.

Chapter 3

Voltage Dips Ride-Through Capability

In this chapter, the effect of all possible voltage dips that could appear at the terminal of a converter interfaced DG unit is examined. The two distributed generation systems, described in the previous chapter, with two different line filters are compared regarding the injected grid currents and the DC-link voltage regulation. Moreover, design equations are derived to be able to predict the maximum currents that are expected to flow through the converter switches during different voltage dips.

3.1 Voltage dips definition

A voltage dip is a phenomenon that is experienced at the end user terminals mainly due to a short circuit fault at a certain point in the electrical network. It can also happen due to motor starts or overloads. It is, as defined by IEEE-std 1159-1995 [50], a decrease to between 0.1 to 0.9 p.u. in the RMS value of the voltage at the power frequency for durations of 0.5 cycle to 1 min. Using this definition, the voltage dip magnitude is referring to the remaining voltage.

In spite of the short duration, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [51]. To deeply study the effect of voltage dips on DGs with a power-electronics interface, the classification found in [52] has been adopted.

3.2 Voltage dips classification

Starting from the different types of faults that can occur in a power system, a classification of voltage dips has been accomplished in [52]. It depends on how the load is connected and how the windings of the

supplying transformer are connected. According to this classification, there are seven types of dips designated with the letters "A" to "G". The system in Fig. 3.1 has been used to quantify the magnitude of a voltage dip in a radial system. In this system, the fault occurs at a remote distance from bus 2 and the load, which could be a DG (as in the thesis), is connected at bus 3. Two impedances are connected to bus 2: the impedance of the system, denoted by Z_S, which represents Thevinin's equivalent impedance of the power system, and the fault impedance Z_F. The load is connected through a transformer to bus 2, at which the voltage, in p.u., is given by

$$V_{dip} = \frac{Z_F}{Z_F + Z_S}. \tag{3-1}$$

It is assumed that the pre-fault voltage is used as reference and is equal to 1 p.u. This typically means that voltage dips originated in the transmission system are shallow (since Z_s is small), while voltage dips originated at distribution level can be deep.

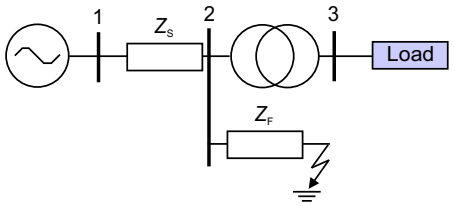

Fig. 3.1 General single-line model for dips classification.

If first it is assumed that the *X*/*R* ratio of the impedances Z_S and Z_F is the same, then V_{dip} has zero phase angle. The resulting voltage dip at bus 3 can be of type "A", which could be a result of a three-phase balanced fault, or any of the six unbalanced types denoted with letters "B" through "G" and reported in Fig. 3.2. In the figure, $E_{i,dip} = E_i V_{dip}$ where the subscript i denotes the phase sequence and takes the values 1, 2, and 3[7], and E_i represents the RMS value of the healthy phase voltage.

[7] Afterwards the three phases will be referred to as a, b, and c.

The transformer connection type has an effect of changing the voltage dip from one type to another. Still, in this work, all dip types are considered for the purpose of providing a general analysis.

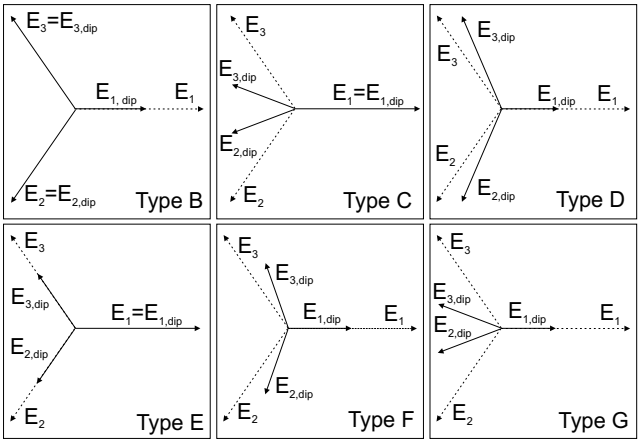

Fig. 3.2 Unbalanced voltage dip classification from "B" to "G". Phasors of three phase voltage before (dotted) and during (solid) fault are displayed. The classification is adopted from [52].

3.3 Voltage dips associated with phase angle jump

If the *X*/*R* ratio for Z_S and Z_F is different, the voltage dip seen at the terminals of the load will have a phase angle "ψ" called "phase angle jump". The impedance angle α is defined as

$$\alpha = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \tag{3-2}$$

where $Z_S = R_S + jX_S$, $Z_F = R_F + jX_F = zl$, z is the feeder impedance per unit length and l is the feeder length. The expression of the voltage dip at bus 2 will be

$$v_{dip} = \frac{\lambda e^{j\alpha}}{1 + \lambda e^{j\alpha}} = V_{dip}\angle\psi \tag{3-3}$$

where $\lambda\, e^{j\alpha} = zl / Z_S$.

The four values for the impedance angle α, that are suggested in [52], are considered: 10^o as the highest expected value for transmission system faults, 0^o as the reference value, -20^o for overhead distribution lines, and -60^o for underground distribution cables. In Fig. 3.3, the relation between the phase angle jump and different dip magnitudes at the four impedance angles is shown. The phase angle jump is larger for smaller dip magnitudes and is more sensitive to the dip magnitude when $\alpha = -60^o$.

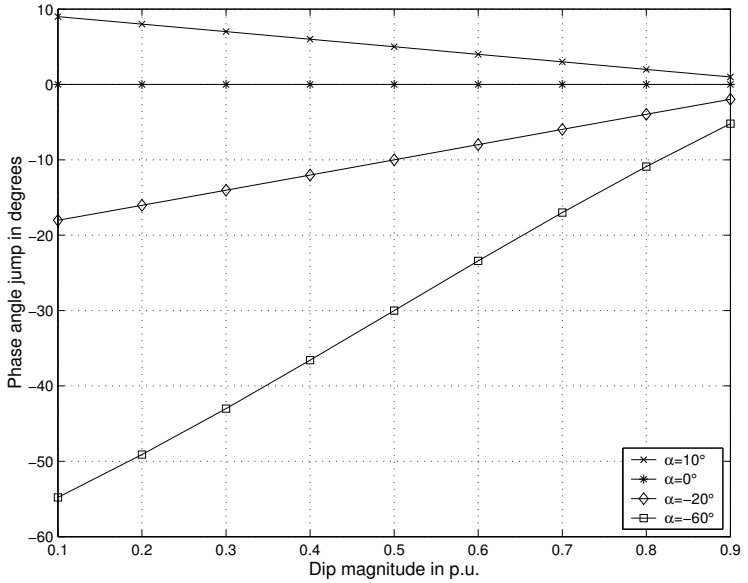

Fig. 3.3 Phase angle jump for different dip magnitudes and impedance angles.

3.4 Positive/negative sequence sub-classification

The magnitudes of the positive sequence (E_p) and the negative sequence (E_n) of the grid voltage for dip types "A" through "G" are calculated using Park transformation and summarized in Table 3-1, where E is the phase-to-phase RMS grid voltage. It shows that dips "C" and "D" have the same positive and negative sequence magnitudes. The same applies for dips "E", "F", and "G". However they may affect the system in different ways

according to Table 3-2, at which the positive and negative sequence components in the *dq*-coordinate system have been calculated. It shows that dips "C" and "D" result in different negative sequence *dq*-components. The same also holds for dip types "F" and "G", while dips "E" and "G" are exactly the same since they both result in the same positive and negative sequence components. This classification is useful in understanding the effect of unbalanced voltage dips on the system. Hence, the following study is carried out using the dual vector current controller (DVCC) that has been described in the previous chapter.

Table 3-1 Positive and negative sequence magnitudes of grid voltage for dip types "A" through "G".

Dip type	E_p	E_n
A	EV_{dip}	0
B	$\frac{E}{3}\sqrt{4+4V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
C, D	$\frac{E}{2}\sqrt{1+2V_{dip}\cos\psi+V_{dip}^2}$	$\frac{E}{2}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$
E, F, G	$\frac{E}{3}\sqrt{1+4V_{dip}\cos\psi+4V_{dip}^2}$	$\frac{E}{3}\sqrt{1-2V_{dip}\cos\psi+V_{dip}^2}$

Table 3-2 Positive and negative sequence components of the grid voltage in *dq*-coordinates for dip types "A" through "G".

Dip type	e_{dp}	e_{qp}	e_{dn}	e_{qn}
A	$EV_{dip}\cos\psi$	$EV_{dip}\sin\psi$	0	0
B	$\frac{E}{3}(2+V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
C	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{E}{2}(1-V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$
D	$\frac{E}{2}(1+V_{dip}\cos\psi)$	$\frac{E}{2}V_{dip}\sin\psi$	$\frac{-E}{2}(1-V_{dip}\cos\psi)$	$\frac{-E}{2}V_{dip}\sin\psi$
E	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$
F	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{-E}{3}(1-V_{dip}\cos\psi)$	$\frac{-E}{3}V_{dip}\sin\psi$
G	$\frac{E}{3}(1+2V_{dip}\cos\psi)$	$\frac{2E}{3}V_{dip}\sin\psi$	$\frac{E}{3}(1-V_{dip}\cos\psi)$	$\frac{E}{3}V_{dip}\sin\psi$

3.5 Current through the voltage source converter caused by voltage dips

At the distribution level, the voltage source converter (VSC) mostly utilizes isolated gate bipolar transistors (IGBT's). An IGBT is easy to turn on and off, and has low conduction and switching losses [13]. The ratings of a single IGBT can be up to 1.2 kA and 3.3 kV. It has good switching capability (up to 100 kHz for a few kW applications), but for very high power devices and applications the frequency is limited to some kHz. On the other hand, the main drawback is poor overcurrent capability, i.e. it cannot withstand more than the peak current it is designed for, even for a short period of time. Hence, the current that would flow through the IGBTs during voltage dips could have a destructive effect if the valves are not designed to withstand this current level.

In order to calculate the required current rating of the VSC valves to ride through voltage dips occurring at the grid, the maximum current has been calculated for all the dip types. The current components in *dqp*- and *dqn*-frame are calculated using the following assumptions:

1. No switching-losses, which means that the AC active power P_1 of the converter is equal to the DC input power KP_{dc}.
2. In addition, the oscillating powers that are produced due to the imbalance are assumed to be supplied from the VSC side to simplify the calculations.
3. Furthermore, for simplicity, the phase angle jump is assumed to be zero, which results in zero *qp*- and *qn*-components of the grid voltage as seen by Table 3.2.
4. Moreover, perfect tracking is assumed, resulting in equal reference and actual currents.

Using (2-26), the grid currents are described as

$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \frac{KP_{dc}}{e_{dp}^2 - e_{dn}^2} \begin{bmatrix} e_{dp} \\ 0 \\ -e_{dn} \\ 0 \end{bmatrix} \tag{3-4}$$

where P_{dc} is the nominal input DC power and K is the ratio of the input power that is actually delivered to the DC link. The current components are then transformed back to the $\alpha\beta$-coordinates in positive- and negative-sequence frames and then into three-phase currents.

In the case of single phase faults (dip types "B" and "D"), the maximum phase current (phase *a*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp} + e_{dn}} \tag{3-5}$$

while for two phase faults (dip types "C", "E", "F", and "G"), the maximum phase current (phase *b*) is calculated as follows

$$I_{max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp}^2 - e_{dn}^2} \sqrt{\frac{1}{4}\left(e_{dp} - e_{dn} \right)^2 + \frac{3}{4}\left(e_{dp} + e_{dn} \right)^2} \; . \tag{3-6}$$

For three phase faults (dip type "A"), the maximum phase current is

$$I_{max} = \sqrt{\frac{2}{3}} . \frac{K P_{dc}}{E \times V_{dip}} . \tag{3-7}$$

The values of e_{dp} and e_{dn}, which are the positive and negative sequence of the *d*-component of the grid voltage, are calculated using Table 3-2 for different voltage dips.

A comparison between the analytically calculated current values and the simulated ones has been performed for all dip types, in order to verify the analytical equations. For instance, the result with dip type "A" is shown in Fig. 3.4[8], where the simulation[9] has been carried out for the L-filter case. It will be shown later that the currents produced with the LCL-filter have the same amplitudes as for the L-filter, using the same value of the series inductance. As shown by the figure, the calculated curve shows overestimated current values, since the dissipated powers by the filter were

[8] Another example is shown in Paper A.

[9] The simulation has been carried out here in MatLab/Simulink.

neglected in the design equations while they were incorporated in the simulation.

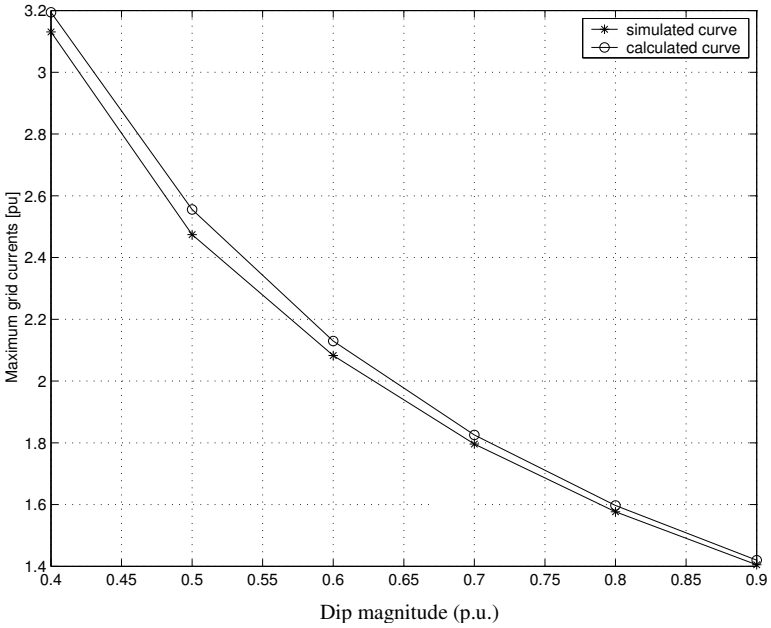

Fig. 3.4 Maximum currents due to voltage dip of type "A".

3.6 Ride-through capability for DGs with L-filter

Depending on the maximum currents that could flow during different voltage dips and using some statistical data regarding the most frequent dip types at the grid, the converter switches could be designed to withstand the increased currents. The peak-to-peak DC-link voltage in case of grid-voltage dips should also be considered in the design of the DC-link. However, the DC-link voltage ripples are found to be negligible when the oscillating powers that are resulting due to the grid-voltage imbalance, are assumed to be supplied from the grid side. This case has been found to be the optimal one for the controller design, if ride-through capability is to be considered.

The effect of all types of dips, with various magnitudes and zero phase angle jump, on the maximum grid current and DC voltage ripples is represented in Fig. 3.5. The maximum current the converter switches should

be able to hold is 3.65 p.u., which happens at 30% dip type “D”. The maximum DC voltage ripple is about 2.5% peak-to-peak and it occurs at 30% magnitude of dip type “F”.

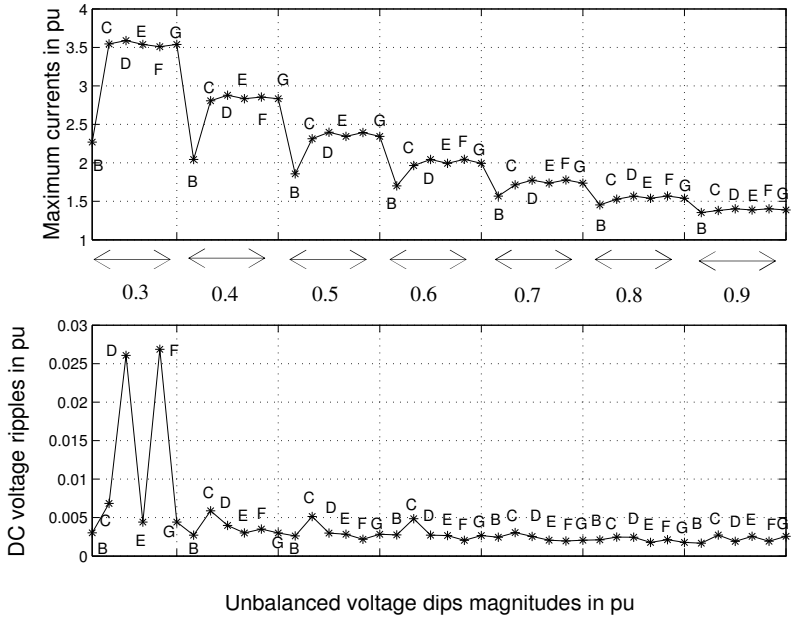

Fig. 3.5 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types.

The effect of the phase angle jump on the DC-link voltage ripples during the dip is found to be negligible. However, their effect over the maximum grid currents is more noticeable as shown in Fig. 3.6. It can be concluded that differences are very small for $\alpha = 10^{o}$ and $\alpha = -20^{o}$ while they seem to be significant when $\alpha = -60^{o}$. In that case the maximum current, with 30% magnitude of dip type “D”, is equal to 4.5 p.u. If the converter valves are designed considering the case of zero phase angle jump, they will be able to handle only 3.65 p.u. current as mentioned previously. Hence, in the case of a voltage dip with phase angle jump, the valves would most probably be destroyed or the VSC will be tripped off.

Moreover, from (3-5), (3-6), and (3-7), it is obvious that there is a direct proportionality between the maximum current and the value of the actual input power. In other words, if the input power is lowered by the ratio *K*, the maximum value of the current will also be lowered by the same ratio. Simulation results presented in Fig. 3.7 represent the effect of lowering the input power P_{in} for different dip types and magnitudes.

Therefore, if the converter switches have to be rated to ride through all dips with 30% minimum magnitude, the current rating can be decreased from about 3.5 p.u. to 3 p.u., if the input power is decreased from 90% to 70% of nominal value.

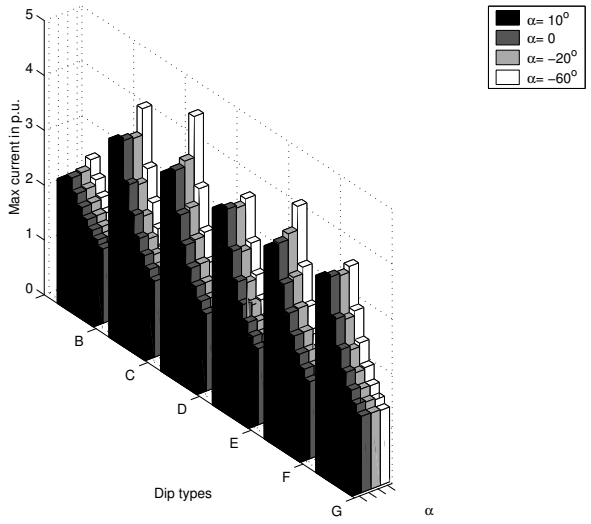

Fig. 3.6 Effect of phase angle jump on the amplitude of phase currents for different unbalanced voltage dips.

One way to optimise the design of the switches is thus to minimize the currents during the fault period, which could be established by temporarily decreasing the input power to the system (decreasing *K* in (3-5), (3-6), and (3-7)) during the fault. If this is possible or not depends on the controllability and the response time of the DC-link or the primary source. By incorporating a DC-chopper, acting as a dump load, or DC energy storage, the input power

could be reduced during the voltage dip period [9]. In addition, for some primary sources it could be possible to reduce the input energy (e.g. by changing the turbine torque reference in wind turbine systems) [36].

On the other hand, if the DC bus is powered by a source that is stochastic in nature, e.g. wind, one could argue that the probability that a dip occurs when the wind turbine is producing full power might be very low, as the turbine often runs at much lower power. Then, to optimize the design it is possible to consider a lower value of the input power, which is delivered by the turbine. This means, accepting a certain risk that the converter (thus the turbine) might still trip, but can lead to greatly reducing the size of the converter[10].

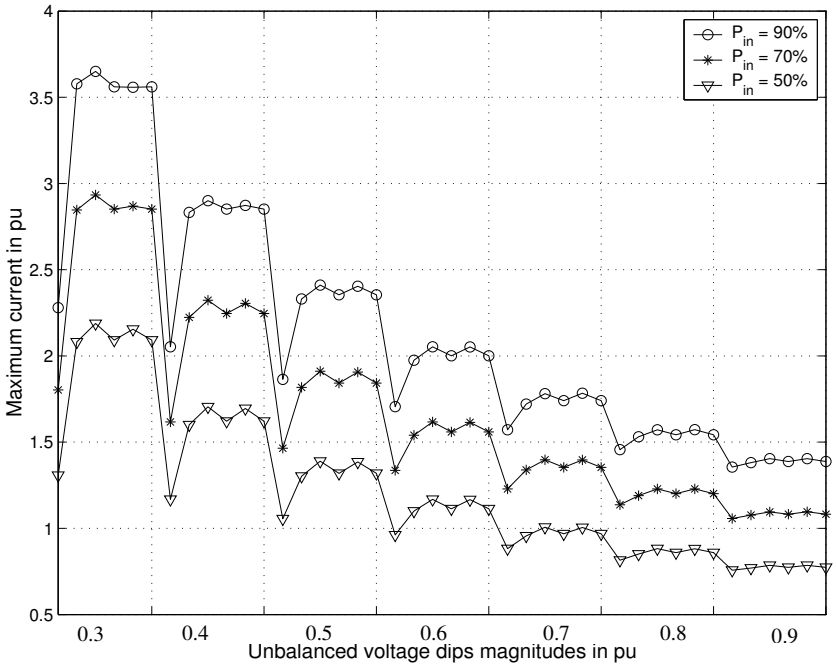

Fig. 3.7 Effect of lowering P_{in} on maximum grid currents for unbalanced voltage dips with magnitudes from 0.3 p.u. to 0.9 p.u. in steps of 0.1. The voltage dip types are shown analogously to Fig. 3.5.

[10] This is investigated numerically by the case study in Paper A.

3.7 Ride-through capability for DGs with LCL-filter

The effect of all unbalanced dips, with various magnitudes, on the maximum grid current and DC voltage ripples (in the middle of the dip period) is presented in Fig. 3.8. The base for the per unit currents is the maximum of the nominal current of the converter. Compared with the case of L-filter interface system (shown in Fig. 3.5 with a current base value equal to the RMS of the nominal current), the currents are almost the same while the DC voltage ripples are slightly increased but still within an acceptable range. This is mainly due to the part of the oscillating power consumed by the filter capacitor and not compensated for in the generated reference currents.

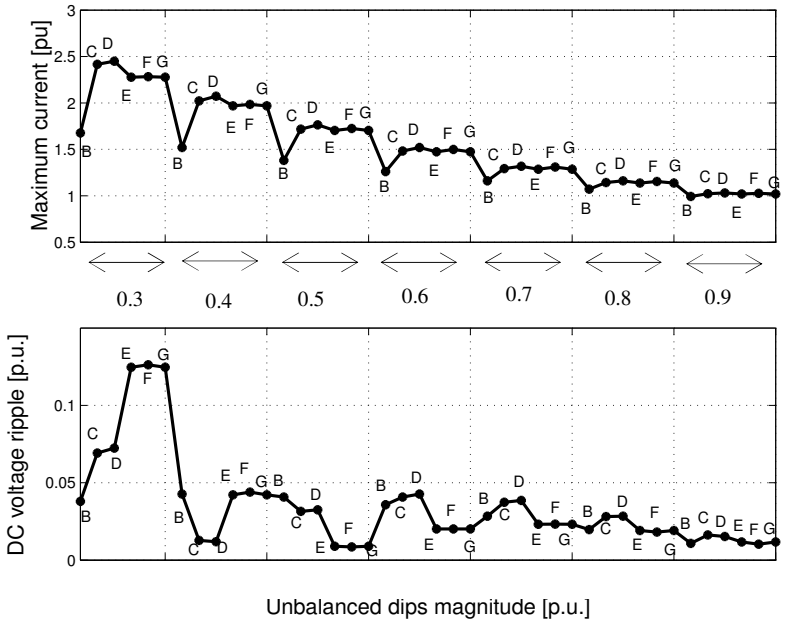

Fig. 3.8 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types and magnitudes from 0.3 to 0.9.

3.8 Conclusions

In this chapter, the effect of different voltage dips over the grid currents and DC-link voltage ripples are examined for the L-filter and the LCL-filter systems. The effect of the phase angle jump has also been examined considering the case when the grid supplies the oscillating powers. It is concluded that the phase angle jump has more effect on voltage dips with smaller magnitudes, and the worst case occurs when the impedance angle $\alpha = -60^{o}$, which corresponds to cable transmission. This effect is more significant for dip types "C" and "D". The maximum current occurs with 30% magnitude of dip type "D" and is equal to 4.5 p.u., i.e. 25% more than its value in case of zero phase angle jump. Thus, the effect of the phase angle jump should be considered when designing the converter switches to ride through all dips.

Since the two considered line filters produce almost the same current amplitudes, having the same value of series inductance, the design equations that have been derived here to calculate the required current ratings of the converter can be used for both systems. These equations give slightly over-estimated values since they are derived without considering the power dissipated in the filter. However, this over-estimation is preferred in the design stage because it gives a safety margin to the design values.

The effect of decreasing the input power has also been examined. Temporarily decreasing the input power to the system during fault reduces the currents during that period, which could be a way to decrease the ratings of the converter valves and in the same time preserving the ride-through capability. This, however, would require that the input power to the DC bus be controllable so as to be reduced very quickly.

Chapter 4

Voltage-Regulation Capability in Weak Grids

By adding a voltage-regulation capability to the DG controller, it is possible to mitigate most of the power quality problems. In addition, this is a highly attractive feature in case of the operation in weak grids. This is the topic of this chapter, where the regulation capability is examined for the mitigation of the decrease of the voltage amplitude specifically in weak grids, the voltage harmonics, and the voltage fluctuation. The DG system with a VSC as a front end and an LCL-filter is considered throughout this chapter. The voltage regulation limits are evaluated regarding the local load of the DG and the DG injected active power. Moreover, the effect of the grid voltage distortion over the phase-angle estimation and the regulation capability is studied. A phase-locked loop (PLL) synthesis based on the extraction of the fundamental component of the grid voltage has been introduced to obtain robust phase estimation.

4.1 Introduction

The term weak grid is here referring to systems where the voltage level is not constant as in a stiff (or strong) grid. Weak grids are usually found in remote areas where the feeders are long. The grids in these areas are usually designed for small loads [32]. When the design load is exceeded, the voltage level may fall below the allowed minimum and/or the thermal capacity of the feeders might be exceeded. Hence, the voltage regulation of long weak distribution lines is an important problem to be considered [30]. The connection of a DG in a weak distribution system can provide voltage support, if the voltage regulation capability is added to its controller, in addition to the main function of injecting active power into the grid. Moreover, by regulating the voltage at the PCC most of the power quality

problems could be mitigated, which might be an attractive requirement in grids with large number of disturbing (non-linear) as well as sensitive loads.

In recent publications, the voltage regulation problem is mainly tackled, in transmission or distribution systems, regarding the power electronics application, using a STATCOM (called DSTATCOM in distribution systems), which is a converter-based shunt connected reactive-power generator. The advantages of a STATCOM, compared to the other thyristor-based reactive power generators (SVCs), are its wider operating area, better performance, and greater application flexibility [75]. The implementation of the DSTATCOM has been discussed in [37], [38] and [58], [60] for voltage flicker mitigation, controlling both the active and the reactive injected powers. In [31] a DSTATCOM is used to regulate and balance the voltage at the distribution bus using only reactive power injection. The voltage regulation limits, however, have not been discussed. Although the application of a STATCOM and a DG are similar in the utilization of a converter as a front end, they are different from the point of view of the active power. STATCOMs could have controllable active power (depending on the grid needs) if they are connected to an energy storage device, while DGs are injecting constant active power that could change due to the changes in the energy source. The DG constant injected active power, consequently, puts some limits on the voltage regulation capability as will be investigated later in this chapter.

The voltage regulation using converter-interfaced DG systems, specifically with LCL-filters at the connection point to the grid, has been less introduced in literature since the emphasis is usually set on the DG technology, not from the power system point of view, and the DG system controllers. Still an example for such a system is found in [32], where a single phase VSI interface of a photovoltaic DG connected to a weak grid through an LCL-filter is considered regarding the voltage regulation purpose. The control algorithm measures the phase of the terminal voltage using Fourier extraction and then computes the required inverter voltage for the desired active and reactive power export commands. The feedback of the filter states has been used to provide the stability of the controller at higher

frequencies. The control of the real and the reactive power flow is done on a cycle-by-cycle basis. Hence, it takes several cycles for the system to settle. Although in [33] the application of a variable speed wind turbine (VSWT) system connected to a weak grid is considered, the emphasis has been placed on the control of the converters for the system and the voltage compensation has been of no interest. The compensation for grid-voltage harmonics has been the main topic of [78], where an inverter-based DG with an L-filter at the connection point to the grid has been considered. Three adaptive regulator gains have been calculated for the 5^{th}, the 7^{th} and the higher harmonics to produce the proper current commands. The focus has been put only on the voltage harmonic compensation, hence the voltage regulation is not considered and the controller takes long time to reach the steady state.

In this chapter, the cascaded controller for the DG system with an LCL-filter[11] is implemented along with a point of common coupling voltage regulator to add the voltage regulation capability. The voltage regulation capability limits are also discussed regarding the DG local load and the DG injected active and reactive powers. Since the output voltage of the VSC is synchronized with the grid voltage using an estimated phase angle, the error in this angle that is mainly due to the distorted grid voltage, should be minimal. The grid voltage phase angle is estimated using a phase locked loop (PLL), which is implemented in the *dq*-frame using a PI controller that tracks the changes in the *q*-component grid voltage by producing the necessary change in the phase angle. This PLL has been well established before [53], however it is first explained here since it will be modified in order to eliminate the effect of the grid voltage power quality problems on the estimated phase angle.

4.2 Phase locked loop (PLL)

The synthesis of the PLL that is commonly used for grid-connected three-phase power conversion systems [53] is based on the quadrature-component extraction of the grid voltage. Hence it will be referred to, here, as a Q-PLL.

[11] This controller has been explained in Chapter 2.

Assuming a balanced three-phase grid voltage at the point of common coupling (PCC)

$$u_{\mathrm{a(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\theta\,, \tag{4-1}$$

$$u_{\mathrm{b(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta - \frac{2\pi}{3}\right), \tag{4-2}$$

and

$$u_{\mathrm{c(PCC)}} = \sqrt{\frac{2}{3}} U_{\mathrm{PCC}} \cos\left(\theta + \frac{2\pi}{3}\right) \tag{4-3}$$

where U_{PCC} is the line RMS voltage at the PCC, and θ is its phase angle.

Transforming the voltage from three-phase notation into a voltage vector in a fixed $\alpha\beta$-frame, using power invariance transformation, the resulting voltage vector will be

$$\underline{u}_{\alpha\beta} = U_{\mathrm{PCC}}\left(\sin\theta + \mathrm{j}\cos\theta\right). \tag{4-4}$$

Normalizing this voltage vector and transforming it into a rotating dq-coordinate system, which rotates with the estimated angular frequency ($\hat{\omega} = \mathrm{d}\hat{\theta}/\mathrm{d}t$), the resulting normalized voltage-vector components will be

$$\underline{u}^{\mathrm{n}}_{\mathrm{dq}} = \cos\left(\theta - \hat{\theta}\right) + \mathrm{j}\sin\left(\theta - \hat{\theta}\right) \tag{4-5}$$

where $\hat{\theta}$ is the estimated phase angle.

If the estimation error ($\varepsilon = \theta - \hat{\theta}$) is very small, then $u^{\mathrm{n}}_{\mathrm{d}} \cong 1$ (the real part in (4-5)) and $u^{\mathrm{n}}_{\mathrm{q}} \cong \varepsilon$ (the imaginary part in (4-5)). Hence, the normalized q-component of the voltage can be used as an input to a PI-controller to produce a required change in the angular frequency ($\Delta\omega$) to track the changes in the phase angle. The Q-PLL main block diagram is shown in Fig. 4.1.

The on-line normalization of the voltage vector will result in nullifying the phase estimation error due to a balanced voltage amplitude change (e.g. three-phase voltage dips). However, in case of unbalanced voltage dips,

oscillations with double the fundamental frequency of the grid will be superimposed on the estimated frequency. These oscillations will result in an error in the estimated phase-angle of the grid-voltage.

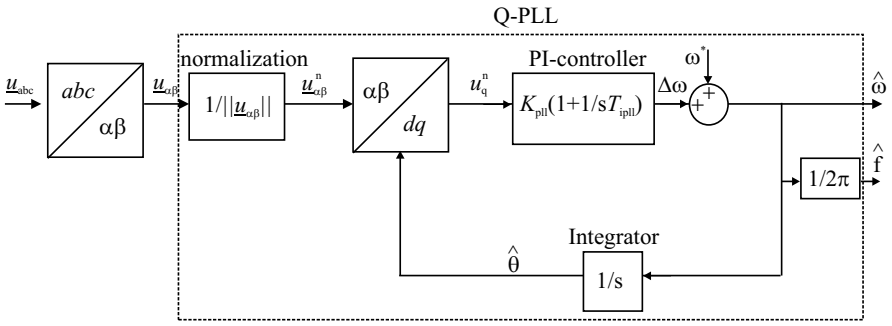

Fig. 4.1 Phase estimation using Q-PLL.

To eliminate this error, the positive sequence of the voltage-vector *q*-component is used as an input to the Q-PLL. This PLL is referred to as a positive sequence PLL (PS-PLL). This PLL is implemented in [55] and [56] by the use of low pass filters (LPF). However, a trade-off has to be made between robustness and good transient performance of the LPFs. Hence, it is instead implemented here as suggested in [57] using the delayed signal cancellation algorithm (DSC) to extract the positive sequence component of the voltage. As shown in Fig. 4.2, the three-phase voltages are measured and transformed into a vector in the stationary αβ-frame. Then the positive sequence voltage vector is extracted using the DSC algorithm, and fed into the Q-PLL that has been described in Fig. 4.1.

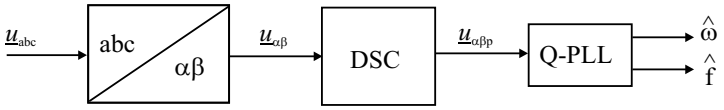

Fig. 4.2 Positive-sequence PLL.

To investigate the effect of the voltage imbalance on the PLL performance, an unbalanced voltage dip of type "C" and remaining voltage amplitude of 0.4 p.u. is applied from 0.5 s to 0.7 s. The estimated frequency

using the Q-PLL and using the PS-PLL are shown in Fig. 4.3 by the middle and lower plots respectively. The estimated frequency using PS-PLL is fairly unaffected by the unbalanced voltage dip apart from the transients at the start and the end of the dip. These transients last for one quarter of the fundamental period and they are resulting due to the implementation of the DSC.

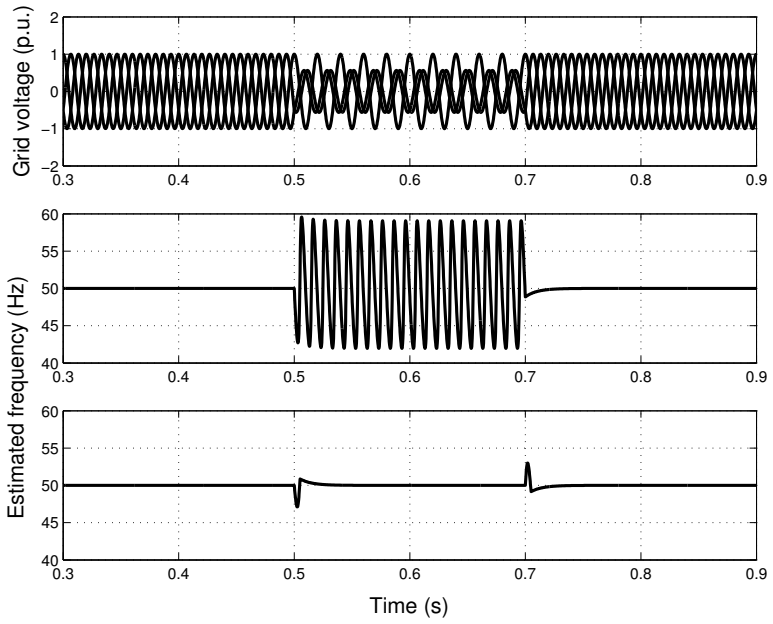

Fig. 4.3 Grid voltage (upper), and estimated frequency using Q-PLL (middle) and PS-PLL (lower).

4.3 PCC-voltage regulation limits

The voltage-regulation capability limit of a converter-interfaced DG is mainly related to the need for the DG to inject constant active power into the grid. To investigate this limit further, the simple weak grid system that is shown in Fig. 4.4 is considered. The parameters that are used for the weak-grid system are listed in Appendix C. For simplicity, it is assumed that the grid impedance Z_s is pure reactive ($Z_s = j\,X_s$). The grid is supplying a load at

the far end of the feeder, where a DG is also connected. It is assumed first that the load is disconnected and the DG is supplying both active power P_{DG} and reactive power Q_{DG} to the grid.

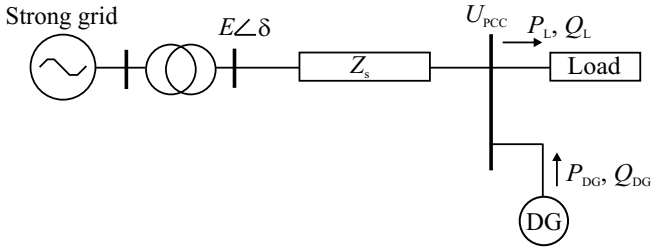

Fig. 4.4 Direction of power flow from VSC to PCC.

The power flow through the system is described by [54]

$$P_{DG} = \frac{U_{PCC}E}{X_s}\sin\delta \tag{4-6}$$

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \frac{U_{PCC}E}{X_s}\cos\delta \tag{4-7}$$

where E is the strong grid RMS line voltage, and δ is the grid voltage angle.

Using (4-6), the adjacent side for the angle δ can be calculated. Then

$$\cos\delta = \frac{\sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}}{\frac{U_{PCC}E}{X_s}}. \tag{4-8}$$

Substituting (4-8) in (4-7), Q_{DG} is obtained as

$$Q_{DG} = \frac{U_{PCC}^2}{X_s} - \sqrt{\left(\frac{U_{PCC}E}{X_s}\right)^2 - P_{DG}^2}\ . \tag{4-9}$$

The voltage at the strong grid bus E is assumed to be equal to 1 p.u. Since the application of a DG requires injecting constant active power to the grid, the change in the reactive power leads to a change in the voltage at the PCC

(U_{PCC}) as suggested by (4-9). However, the value of the input active power affects the amount of the reactive power that is available for the compensation. A higher value of the injected active power implies that a higher value of reactive power can be injected, considering the same equation. Yet, that implies higher injected current, which could be an issue for the VSC valves capacity and protection[12], and also the increase of the DC-link voltage ripples might be another issue. An illustration of this is presented in Fig. 4.5[13], where the voltage regulation capability has been examined for a case when the grid voltage has a modulating signal with an 8% amplitude superimposed on the fundamental component. The input power from the DG source has been varied from 70% to 140% of the nominal value.

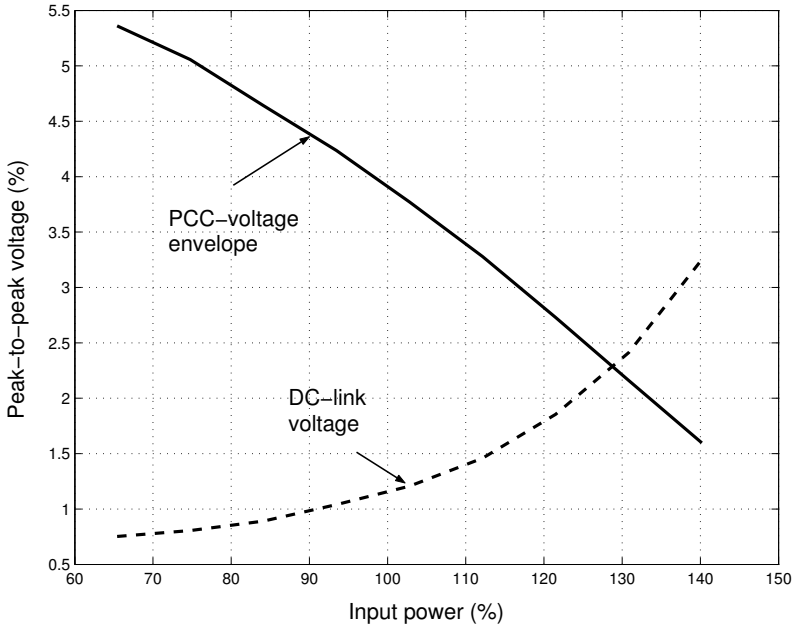

Fig. 4.5 Effect of the injected input power on the PCC voltage envelope oscillation (solid) and DC-link voltage ripples (dashed).

[12] That has been discussed in the previous chapter and in Paper A.
[13] Further details are provided in Paper E.

With the voltage regulation capability, the PCC-voltage has been better regulated at the upper value of the injected active power, where the grid voltage amplitude modulation has been reduced to 1.5%. On the other hand, the DC-link voltage ripples has increased to about 3.2% of its nominal value. Although negligible in value, in this example, the DC ripples amplitude could have a more significant value, for instance, if the amplitude of the modulating signal increases.

Equation (4-9) can be rearranged as

$$P_{\mathrm{DG}}^2 + \left(Q_{\mathrm{DG}} - \frac{U_{\mathrm{PCC}}^2}{X_{\mathrm{s}}} \right)^2 = \left(\frac{U_{\mathrm{PCC}} E}{X_{\mathrm{s}}} \right)^2 . \tag{4-10}$$

Equation (4-10) represents a circle with the radius of $U_{\mathrm{PCC}}E/X_{\mathrm{s}}$ and the centre at $(0,U^2_{\mathrm{PCC}}/X_{\mathrm{s}})$. By varying U_{PCC}, different power circles will result representing different possible operating points related to different values of the injected (or drawn) DG active and reactive powers. Those power circles have been illustrated in Fig. 4.6, where only the possible operating area has been shown (for the PCC voltage varying between 0.5 p.u. and 1 p.u.).

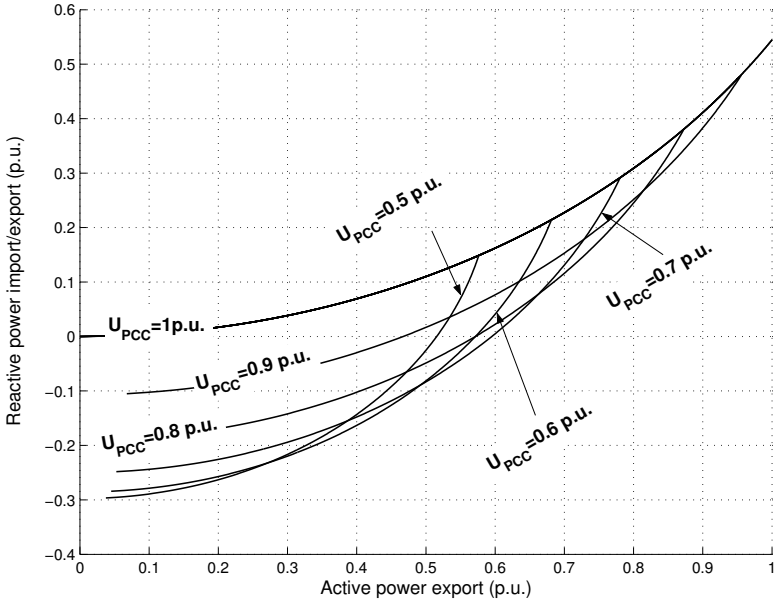

Fig. 4.6 DG import/export power with unloaded weak grid for different PCC voltages.

The figure is indicative of the amount of the reactive power to be injected by the DG at a specific value of the injected active power and a certain voltage drop over the feeder. For instance, for a PCC voltage of 0.7 p.u. and injected active power of 0.5 p.u., the injected reactive power should equal to the difference between the two values resulting from the intersection of the 0.5 p.u. power line and the two circles related to the PCC voltages of 1 p.u. and 0.7 p.u. (in this example, the injected reactive power will be about 0.2 p.u.). For the same PCC voltage (0.7 p.u.), if the DG injected power is 0.8 p.u., this operating condition will represent an unstable operation since the 0.8 p.u. power line does not intersect with the 0.7 p.u. circle.

To calculate the maximum reactive power that should be injected to regulate the voltage at the PCC with different voltage drops, (4-9) is differentiated with respect to the PCC voltage U_{PCC} and the result is set to zero. Then the resulting voltage that would acquire maximum injected reactive power is U_{limit}

$$U_{\mathrm{limit}} = X_{\mathrm{s}} \sqrt{\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2} \ . \tag{4-11}$$

The reactive power lower limit Q_{limit} that will result in maximum injected DG reactive power (to regulate the PCC voltage) is then related to the DG injected active power as

$$Q_{\mathrm{limit}} = X_{\mathrm{s}} \left(\frac{1}{4X_{\mathrm{s}}^2} + P_{\mathrm{DG}}^2 \right) - \frac{1}{2X_{\mathrm{s}}} \, . \tag{4-12}$$

Equation (4-12) is depicted in Fig. 4.7, where it shows again that the maximum power to be injected is inversely proportional to both the PCC voltage and the DG injected active power. The difference between the two curves in the figure indicates the necessary injected reactive power.

To investigate the effect of the loading on the compensation capability of the DG, it is now assumed that a static constant-power load is connected at

the PCC in Fig. 4.4. With a constant-power load, the power circles would be shifted up and/or to the right depending on the load reactive and active powers respectively. This should, in turn, increase the voltage compensation limit of the DG. However, an increased amount of the load reactive power, shifting the circles up, will imply more DG injected reactive-power to compensate for the voltage.

Assuming a constant active power load of 0.1 p.u., the operational part of the power circles relating the DG active and reactive powers to the grid voltage at the PCC is shown in Fig. 4.8. For instant, if the voltage at the PCC is 0.7 p.u. and the input DG active power is 0.8 p.u., then this will imply a stable operation with about 0.1 p.u. reactive power to be injected into the grid to regulate for the voltage.

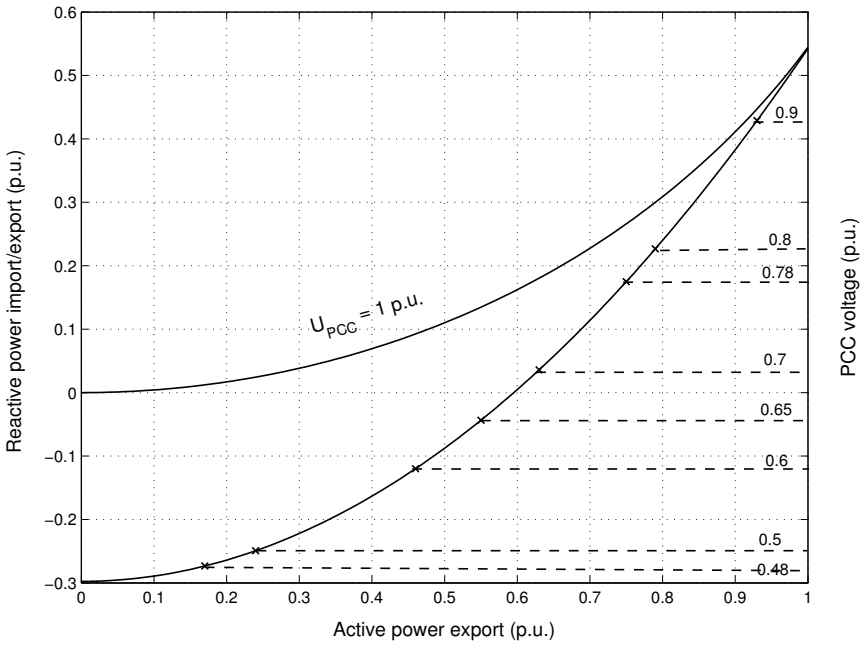

Fig. 4.7 Maximum reactive power (i.e. vertical difference between the two curves) to be injected related to the PCC voltage and the DG injected active power.

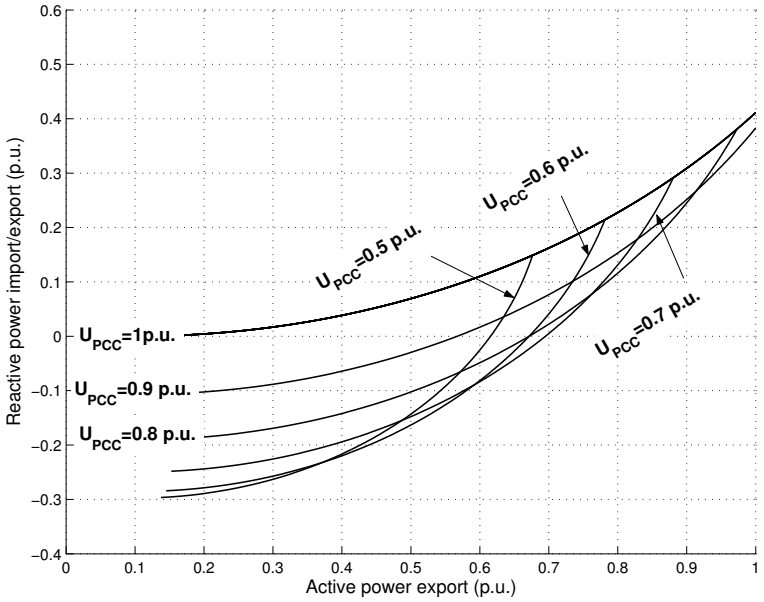

Fig. 4.8 DG import/export power with a constant power load of P_L = 0.1 p.u. and Q_L = 0.0 p.u.

It is worth noting here that the above discussion has been carried out assuming a lossless feeder. By decreasing the *X*/*R* ratio of the feeder, the resistive voltage drop will increase implying decreased PCC voltage related to the same loading condition. For instance, for a pure resistive feeder (Z_s = R_s) the equations for the active and reactive power flow through the feeder will be reversed. That means

$$Q_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}E}{R_{\mathrm{s}}}\sin\delta \tag{4-13}$$

$$P_{\mathrm{DG}} = \frac{U_{\mathrm{PCC}}^2}{R_{\mathrm{s}}} - \frac{U_{PCC}E}{R_{\mathrm{s}}}\cos\delta\,. \tag{4-14}$$

This implies that the voltage at the PCC will become more sensitive to the active power change and less sensitive to the reactive power change. This will result in an increased amount of the reactive power to regulate the

voltage compared to the case with a pure inductive feeder. Hence, the decreased *X*/*R* ratio will account for another limit for the regulation capability.

4.4 PCC-voltage regulator

The DG injected reactive power is adjusted by the PCC-voltage regulator to maintain the 1 p.u. grid voltage amplitude. The regulator has been implemented regarding the instantaneous reactive power generated by the DG at the PCC, which is described as

$$q_{(\mathrm{PCC})} = u_{\mathrm{q(PCC)}} i_{2\mathrm{d}} - u_{\mathrm{d(PCC)}} i_{2\mathrm{q}} . \tag{4-15}$$

Since the voltage-oriented synchronous-frame transformation sets the *q*-component of the voltage into zero, then $i_{2\mathrm{q}}$ is used to control the reactive power flow. Since $u_{\mathrm{d(PCC)}}$ is to be regulated, then the reactive current reference is generated to compensate the error in the voltage using a PI-controller[14], as follows

$$i_{2\mathrm{q}}^{*}(k) = k_{\mathrm{pr}} \varepsilon_{\mathrm{e}}(k) + \frac{k_{\mathrm{pr}} T_{\mathrm{s}}}{T_{\mathrm{ir}}} \sum_{n=1}^{k} \varepsilon_{\mathrm{e}}(n-1) \tag{4-16}$$

$$\varepsilon_{\mathrm{e}}(k) = u_{\mathrm{d(PCC)}}(k) - u_{\mathrm{d(PCC)}}^{*}(k) \tag{4-17}$$

where

k_{pr} is the proportional gain of the PCC-voltage regulator;

k is the sampling instant;

T_{ir} is the integral time; and

T_{s} is the sampling time.

Assuming, now, that the loading condition of the grid allows for a stable operation of the PCC-voltage regulator, the mitigation of the power quality problems at the grid is to be considered next.

[14] The controller parameters are given in Appendix D.

4.5 Compensation for grid-voltage harmonics

The effect of the voltage harmonics on the estimated phase using the PS-PLL is first discussed. If it is assumed that the voltage has a harmonic signal that is superimposed on the fundamental component, then it can be described in the αβ-frame as

$$\underline{u}_{\alpha\beta}(t) = U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t} \tag{4-18}$$

where

U_1 and U_h are the amplitudes of the fundamental and the h^{th} harmonic respectively;

ω is the fundamental grid-voltage angular-frequency; and

h_s is the related harmonic sequence that takes a value of either $+1$ (for positive sequence) or -1 (for negative sequence) according to [54]

$$h_s = \begin{cases} +1 & h = 3n+1 \\ -1 & h = 3n+2 \\ 0 & h = 3n \end{cases} \tag{4-19}$$

where n is a positive integer starting from zero.

The zero sequence harmonics will not be treated in this analysis due to the absence of a neutral wire.

Substituting (4-18) in (2-15), the positive-sequence vector of the grid voltage in $\alpha\beta-$frame is:

$$\begin{aligned} \underline{u}_{\alpha\beta\mathrm{p}}(t) &= \frac{1}{2}\left(U_1 e^{\mathrm{j}\omega t} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega t}\right) \\ &+ \frac{\mathrm{j}}{2}\left(U_1 e^{\mathrm{j}\omega(t-T_g/4)} + U_\mathrm{h} e^{(h_\mathrm{s})\mathrm{j}h\omega(t-T_g/4)}\right) \end{aligned} \tag{4-20}$$

where $\dfrac{\omega T_g}{4} = \dfrac{\pi}{2}$.

The harmonic part of (4-20) can be expressed using trigonometric functions as follows

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = \frac{U_{\mathrm{h}}}{2}\left(\cos(h\omega t) + \mathrm{j}(h_{\mathrm{s}})\sin(h\omega t)\right) + \mathrm{j}\frac{U_{\mathrm{h}}}{2}\cos\left(h\omega t - h\frac{\pi}{2}\right) - (h_{\mathrm{s}})\sin\left(h\omega t - h\frac{\pi}{2}\right). \tag{4-21}$$

For the harmonics of the orders 5th and 7th, $\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}$ will be nullified since

$$\cos\left(h\omega t - h\frac{\pi}{2}\right) = -(h_{\mathrm{s}})\sin(h\omega t) \tag{4-22.a}$$

and

$$\sin\left(h\omega t - h\frac{\pi}{2}\right) = (h_{\mathrm{s}})\cos(h\omega t). \tag{4-22.b}$$

For harmonics of the orders 11th and 13th, the positive-sequence harmonic voltage vector will have the same amplitude as of the imposed harmonic signal and will rotate with the same angle. Equation (4-21) for the two harmonics will become

$$\underline{u}^{\mathrm{h}}_{\alpha\beta\mathrm{p}}(t) = U_h e^{\mathrm{j}h_{\mathrm{s}}h\omega t}. \tag{4-23}$$

Since the 5th and 7th harmonics are the most dominant in the power system [54], it is expected that good results will be obtained using the PS-PLL in estimating the grid-voltage phase angle. Moreover, since the operation of the PS-PLL is similar to a LPF operation, the higher harmonics will be attenuated as well.

To investigate the capability of the voltage-harmonics compensation, a parallel RC-load is connected to the grid, through a diode rectifier, upstream of the DG. The phase-voltage at the PCC is shown in Fig. 4.9 before and after the connection of the DG. In addition, the harmonics content is also shown for both voltages in Fig. 4.10. The harmonics are comparatively negligible when connecting the DG, with the PCC-voltage regulation capability. For instance, the 5th harmonic component amplitude has decreased from about 9.5% without the DG to about 3% with the DG. This will result in a voltage that complies with the IEEE-std 1547-2003, which specifies the maximum harmonic voltage distortion as 4% for the harmonics' orders less than the 11th.

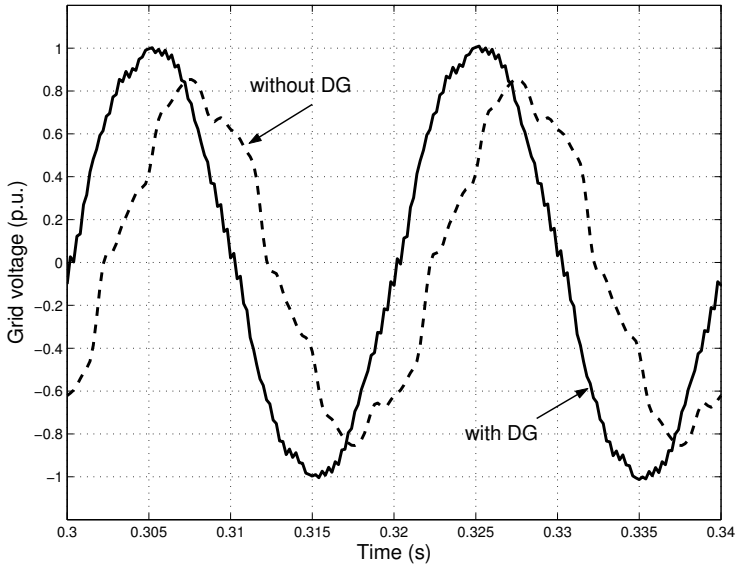

Fig. 4.9 Grid Phase-voltage with (solid) the DG and without (dashed) the DG.

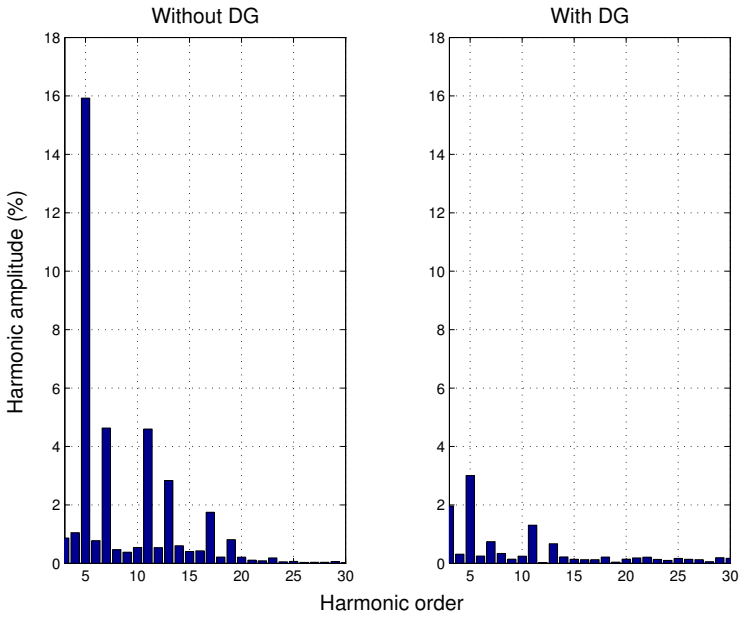

Fig. 4.10 Grid voltage harmonics content with the DG (right) and without the DG (left).

4.6 Compensation for grid-voltage fluctuation

Grid voltage amplitude fluctuations may result due to fast periodically-changing heavy loads that are connected to the grid [58]. If a distribution network is considered, one of the direct effects could be light flicker. The frequency of light flicker ranges between 0.5 Hz and 30 Hz, since this is the range of the human eye sensibility [59]. One way to mitigate this phenomenon is to compensate for the oscillating reactive power using a STATCOM [59] - [60], which is a three-phase VSC based device. The VSC-interfaced DG with the voltage compensation capability is considered here for that purpose.

Proposed PLL modification

The effect of the voltage amplitude modulation on the PS-PLL is first to be examined. For this purpose, a sinusoidal modulating signal is added to the voltage magnitude. With a variable voltage-amplitude, the q-component of the grid voltage will oscillate with the same frequency as the modulating signal. Substituting $h_s = 0$ and $h = 1/5$ (for 10 Hz amplitude modulation) in (4-21), it is obvious that the positive sequence will also be oscillating, producing an error in the estimated phase. To nullify this error and obtain a robust performance, the fundamental component of the grid voltage could be used, instead of the positive sequence component, as input to the Q-PLL. This has been implemented in [61] using two LPFs to extract both the positive-sequence and its fundamental component.

In order to cope with this situation, the adaptive linear neural network extractor (ADALINE) [62] is introduced next. A simple ADALINE consists of one neuron that has a linear input-output relationship, where each input is simply multiplied by a certain weight and all inputs are summed together to produce the output. The power of ADALINE comes from the on-line adaptation of its weights that gives it a non-linear property [62]. For this purpose, the least mean square (LMS) algorithm is used [63].

ADALINE has been implemented in [64] as a combiner to identify the voltage waveform for the classification of the power quality problems. It will

be used here in the same way, however, as an extractor to relieve the fundamental component of the source polluted voltage. The structure of ADALINE is shown in Fig. 4.11, where the discrete input vector $\mathbf{x}(k)$ is composed of sine and cosine elements of all possible frequency components that are contained in the source voltage

$$\mathbf{x}(k) = \left[\sin(\omega k T_s) \quad \cos(\omega k T_s) \quad \ldots \quad \sin(h\omega k T_s) \quad \cos(h\omega k T_s)\right]^T \tag{4-24}$$

where h is the highest harmonic order expected, k is the sampling instant, T_s is the sampling time, and the superscript T indicates the transpose of the vector. This input vector $\mathbf{x}(k)$ is then multiplied by a weight vector $\mathbf{w}(k)$ to produce the ADALINE output $u_{nn}(k)$, as follows

$$\mathbf{w}(k) = \left[w_{11} \quad w_{12} \quad w_{21} \quad w_{22} \quad \ldots \quad w_{h1} \quad w_{h2}\right] \tag{4-25}$$

$$u_{nn}(k) = \mathbf{w}(k) \cdot \mathbf{x}(k) = \sum_{i=1}^{2h} w_i x_i \tag{4-26}$$

where w_i and x_i is the i^{th} element in the vectors $\mathbf{w}$ and $\mathbf{x}$ respectively.

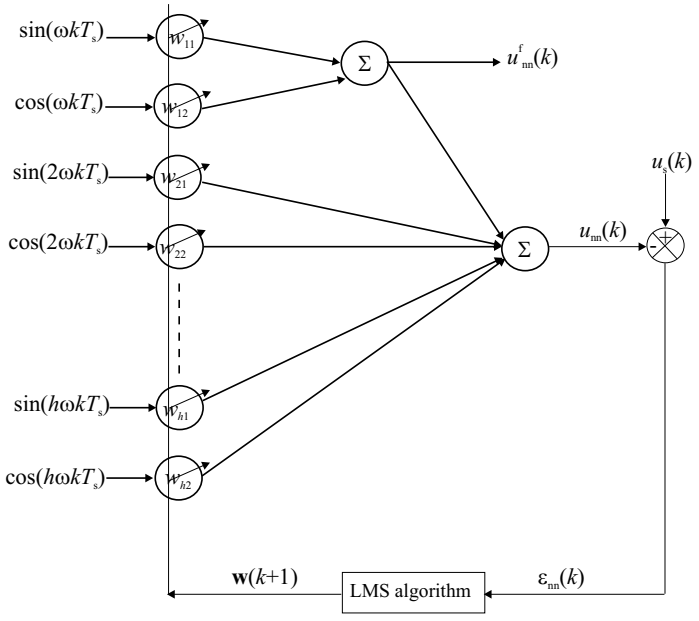

Fig. 4.11 The structure of the adaptive linear extractor (ADALINE).

The output is then compared with the measured and sampled voltage signal $u_s(k)$, where the resulting error ε_{nn} is used by the recursive algorithm to modify the weight vector according to

$$\mathbf{w}(k+1) = \mathbf{w}(k) + \lambda \frac{\mathbf{x}(k)\varepsilon_{nn}(k)}{\mathbf{x}(k)^{\mathrm{T}}\mathbf{x}(k)} \tag{4-27}$$

where λ is the learning factor. The size of λ determines how quickly old data are to be discarded. A small λ means that new data inputs will not have a significant weight and the system becomes less sensitive to disturbances, but also slower in reactions. On the other hand, a large λ makes the system react quickly, but responds more sensitively to disturbances[15].

The block diagram of the PLL implementing ADALINE (NN-PLL) is shown in Fig. 4.12. The three-phase voltage is transformed into the stationary $\alpha\beta$-frame. Then each component is fed into a separate ADALINE algorithm to extract the fundamental component that is fed into a Q-PLL.

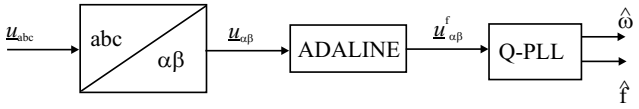

Fig. 4.12 Implementation of NN-PLL.

Performance of the proposed PLL

The performance of the NN-PLL is also compared to the PS-PLL regarding the grid voltage harmonics. The error in the estimated phase angle due to the grid voltage harmonics is shown in Fig. 4.13, using three different bandwidth values for the Q-PLL, for the two estimators. 2% amplitude of the 2nd, 4th, 5th, 7th, 11th and 13th harmonic orders has been superimposed separately on the fundamental grid-voltage. The phase error has been

[15] More discussion about the learning factor can be found in Paper E.

calculated as the peak-to-peak amplitude of the normalized quadrature-voltage.

With the PS-PLL, the error in the estimated phase-angle increases with higher values of the bandwidth. Moreover, the amplitude of the error increases with the increase of the harmonic order, excluding the case for the 5^{th} and 7^{th} harmonics at which it was proven that the error will be nullified. This can be understood by observing (4-17), where the harmonic order is in proportional relationship with the frequency of the oscillations superimposed on the fundamental grid-voltage.

Using the NN-PLL the error is nullified with all harmonic orders and all values of bandwidth, which means that it is robust and in the same time could have better dynamics. Moreover, the case of unbalanced harmonics has been examined with the same order of harmonics as before. Figure 4.14 shows that the NN-PLL is superior to the PS-PLL even when unbalanced 5^{th} and 7^{th} harmonics are present in the grid.

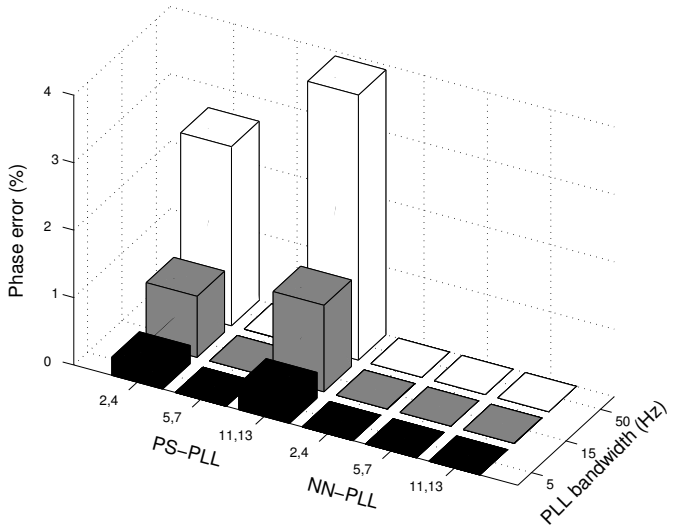

Fig. 4.13 Phase error due to different balanced harmonics using PS-PLL and NN-PLL with different BW values.

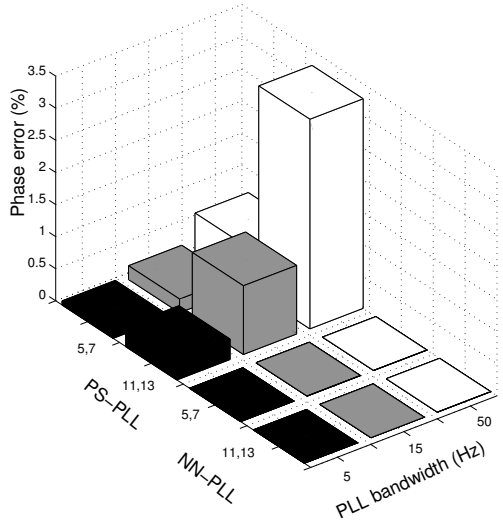

Fig. 4.14 Phase error due to different unbalanced harmonics using PS-PLL and NN-PLL with different BW values.

Mitigation of grid voltage amplitude fluctuation

The mitigation of the grid voltage fluctuation is to be examined. A fluctuating load is assumed to be connected at bus 1, in Fig. 4.4, and is further assumed to be disconnected in case of a fault at the same bus. Its effect is encountered as about 8% amplitude fluctuation of the grid voltage at bus 1 using a cosine modulation signal with a frequency of 10 Hz. In reality this modulation signal could have an infinite number of frequencies, but for the sake of clarity only a 10 Hz component is displayed here, which represents a value in the frequency band (between 2 and 15 Hz [58]) that the human eye is most sensitive to. The PCC-voltage is shown in Fig. 4.15 before the connection of the DG, and with the DG connected with the PS-PLL and the NN-PLL. From the figure, it can be concluded that the ability of the DG with an NN-PLL to mitigate the voltage fluctuation is better. The peak-to-peak voltage-envelope has been oscillating with 8% before the voltage compensation, and with 5% in case of voltage regulation using the PS-PLL and 3.5% in case of using the NN-PLL.

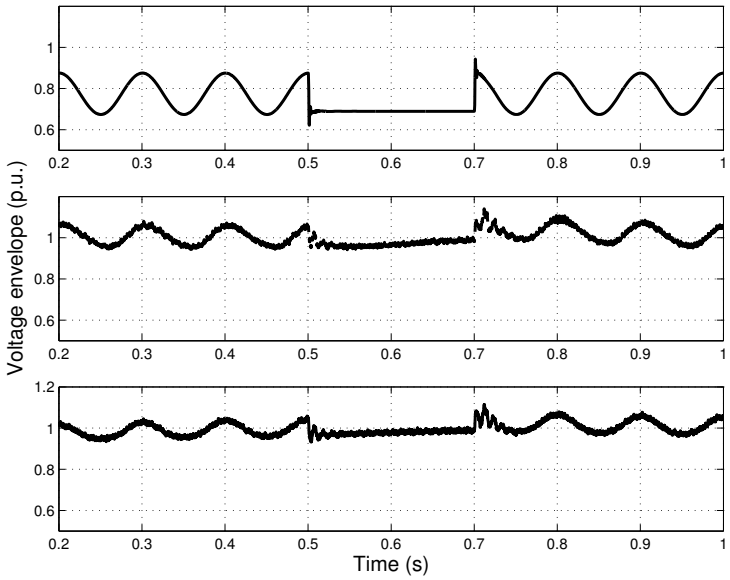

Fig. 4.15 Voltage envelop with DG disconnected (upper), DG with PS-PLL (middle), and DG with NN-PLL (lower).

Moreover, the voltage amplitude variation at the PCC has been tested with different modulation signal frequencies and the result is shown in Fig. 4.16, where the system using the NN-PLL has lower peak-to-peak value of the oscillation of the voltage envelope.

It is worth noting here that the oscillations of the voltage envelope will not be completely nullified since both the active and the reactive powers are oscillating at the grid, because of the modelling that is considered here. That means that both the injected active and reactive powers should be oscillating in order to completely compensate for the voltage fluctuation. However, this is not possible, here, since the application of the converter interfaced DG that is considered implies constant injected active power into the grid. On the other hand, the behaviour of the NN-PLL is dependent on the input-vector length, the order of harmonic frequencies used in that vector, and the initial weights' values. The input-vector length is taken, here, as 18 and the initial weight vector was set to zero. Using different setup for the ADALINE could give different results.

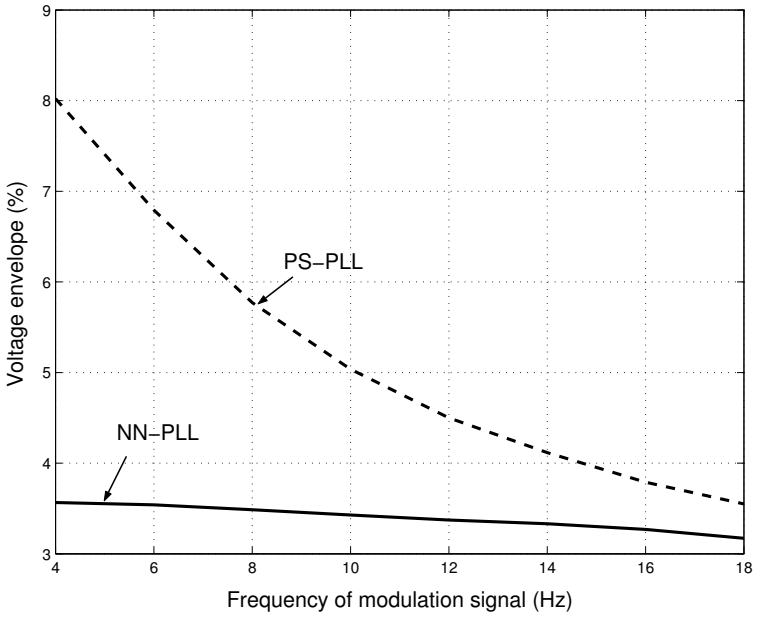

Fig. 4.16 Voltage amplitude variation owing to the change of the modulation signal frequency; with PS-PLL (dashed curve) and NN-PLL (solid curve).

4.7 Conclusions

The possibility to regulate the local voltage using a converter-interfaced DG has been discussed in this chapter. The aim is to maintain the voltage at its nominal value in case of operation in weak grids, and to mitigate the power quality problems at the point of common coupling (PCC). The voltage regulation capability has been investigated by studying the regulation limits regarding the DG injected power and the loading of the grid. The regulation capability is increased if the DG is injecting more active power into the grid and the load is mostly a constant active power load. However, this could require oversizing of the converter valves.

The PCC-voltage regulator sets the reactive current reference in such a way that the reactive power injected into the grid is controlled. The reactive current is represented by the quadrature-component of the measured current,

which is obtained through a coordinate transformation that uses an estimated angle that is obtained using a PLL. The error in the estimated angle could result in an erroneous reactive current command, which could affect the voltage compensation quality. For that purpose, the PLL algorithm has been discussed regarding the grid voltage imbalance, the grid voltage harmonics, and the grid voltage fluctuation. A neural-network based PLL (NN-PLL) has been proposed to extract the fundamental component of the grid voltage, and to estimate its phase angle. This NN-PLL has been compared with a previously investigated PLL algorithm (here referred to as PS-PLL), which estimates the phase angle of the positive-sequence component of the grid voltage. It has been shown that the NN-PLL is more robust against grid voltage harmonics. The NN-PLL has shown superiority also in the special case of unbalanced 5^{th} and 7^{th} harmonics in the grid voltage. In addition, the NN-PLL has proven to be better in case of grid-voltage fluctuation, where in a demonstrated case the oscillation of the voltage envelope has been decreased from 8% (without voltage regulation) to 3.5% (with voltage regulation and using NN-PLL), compared to 5% when using the PS-PLL.

Chapter 5

Intentional Islanding Capability

Intentional islanding refers to the case when the distributed generation (DG) is allowed to work autonomously to energize a part of the grid. For safe operation, detection methods should be applied to change the DG operating mode from grid-connected operation to island operation and vice-versa. Two different detection methods are described and examined in this chapter; namely passive and active methods. Their non-detectable zone is briefly discussed. The operation of the DG in both a strong grid and a weak grid has been examined in case of islanding.

5.1 Intentional islanding definition

Islanding refers to a condition in which a portion of the power system is energized by a local energy source, while it is electrically separated from the rest of the power system [65]. This situation, if not planned, poses a safety hazard to utility repair and maintenance personnel, and could lead to unstable island and instability problems when the utility grid is recovered [66].

Hence, islanding detection is an important aspect in DG applications. DGs should be able to detect the islanding condition within a specified clearing time and to stop to energize the grid according to the IEEE-std 1547-2003, which specifies the acceptable clearing times as shown in Fig. 5.1. Yet, as recommended by the same standard, the detection could lead to an island operation of a DG, which is referred to as intentional islanding.

Besides enhancing the supply reliability for the utility grid [83] (e.g. in rural areas [4]), intentional islanding of DGs represents a required practice for some critical micro-grids [5], [84], [85]. Hence, developing reliable and robust islanding detection methods is of major importance.

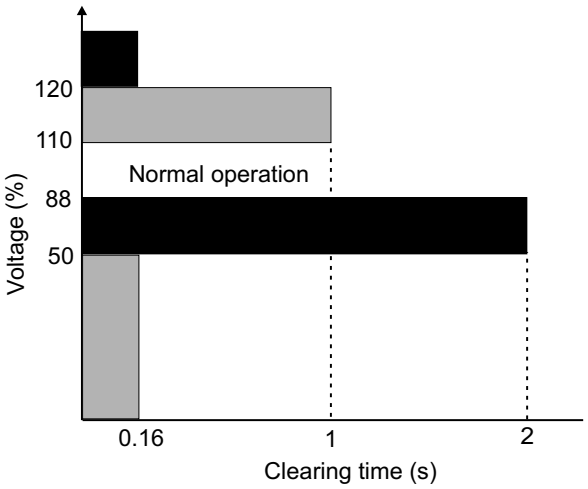

Fig. 5.1 Clearing time for a DG as described in IEEE-std 1547-2003.

5.2 Islanding detection methods

There are two types of islanding detection methods; passive and active. In passive detection algorithms, the sensed grid states (voltage, frequency … etc.) are compared with their nominal values and the deviations are used to decide on the islanding condition. For instance, in [10], the grid outage is detected using the phase angle error, between the grid voltage and the inverter voltage, which is compared to a set value to generate the disconnection signal. Then the DG operates in a stand-alone mode. When the grid is back, the increased currents are used to trip the DG. Then the DG is connected back to the grid after synchronization. Using the voltage phase-angle for islanding detection, however, may lead to false islanding in case of other power system dynamics [68]. Instead, in [40], both the voltage and the frequency are measured at the PCC to detect islanding. However, the effect of a voltage limitation, which could be incorporated in the converter controller for its safe operation, is not considered.

Although they are simple to implement, passive algorithms may fail to detect islanding if the load and generation on the island are closely matched

[67]. The active and reactive power mismatch limits that will lead to this situation are referred to as the non-detectable zone (NDZ) and they are calculated for current-controlled and power controlled DGs in [68] for different passive algorithms using an RLC-resonant load with a certain quality factor. It has been shown, in that reference, that the algorithms that are using the under/over frequency and/or the phase-angle jump are insensitive to active power mismatch. Moreover, the under/over frequency methods are, unlike the phase angle jump methods, dependent on the load quality factor. In addition, there are practical issues related to using phase-angle jump methods. Power system switching events, not resulting in islanding, can falsely trigger such schemes. When the islanding detection is delayed or not activated due to the NDZ, the DG system may lose control on its output terminal voltage, which may lead to island instability. In a way to overcome this problem and to provide seamless transfer between the grid-connected and island modes of operation, the island load (or emergency load) in [46] has been connected in parallel to the capacitor of the LCL-filter. Since the capacitor voltage is always controlled, even in the case of grid-detection failure, the load is not affected by the change of the DG operating mode, or the delay or mal-operation of the detection algorithm. However, this solution might not be feasible for all grids or loads. Another way is to decrease the NDZ by improving the detection method.

In active detection methods, the NDZ is very small [69]. Active techniques are usually incorporated within the controller, where they aim at disturbing the grid states by injecting disturbance signals. In the case of the utility supply outage, the island will be disturbed and the passive detection will succeed. In spite of the small NDZ, active methods may affect the power quality of the distribution system [39]. Moreover, in case of a weak grid system, active methods may lead to false tripping.

Hence, the passive islanding-detection method is considered first since it is the main islanding decision maker. Then, an active islanding detection method is introduced for the operation of the DG in both a strong and a weak grid.

5.3 Passive islanding-detection

A passive islanding detection algorithm has been developed to detect both the grid outage and recovery. To evaluate the grid states that could be reliable enough to be used in the detection algorithm, the grid outage is first considered.

The effect of the grid outage on the PCC-voltage

At the moment of the grid outage, the voltage at the point of common coupling (PCC) will either increase or decrease instantly depending on the sign of the power mismatch (ΔP and ΔQ in Fig. 5.2). The power mismatch represents the amount of power that the grid either delivers or absorbs in the normal operation. This power is equal to the power absorbed by the load at the PCC subtracted from the power injected by the DG, as designated in Fig. 5.2[16]. If the DG injected power is higher than the load absorbed-power, then the PCC-voltage will increase implying increased $u_{\mathrm{d(PCC)}}$. In that case, the increase of the voltage will be limited by the voltage limitation algorithm incorporated in the DG controller. Regarding the algorithm that has been implemented here, $u_{\mathrm{d(PCC)}}$ will be limited to $\frac{u_{\mathrm{dc}}}{\sqrt{2}}$ as has been shown in Section 2.2.

This case is presented in Fig. 5.3, where the grid outage occurs at 0.4 s. The DG controller that has been tested here has the PCC-voltage regulator and the DC-link voltage regulator incorporated. Hence, the *d*-component of the DG injected-current is controlled to be constant to keep the DC-link voltage constant, as shown by the lower plot in Fig. 5.3, while the *q*-component of the current starts to decrease in magnitude after the grid outage to retain the voltage at its nominal value. Since the PCC-voltage amplitude is limited (due to both the limiting algorithm and the operation of the PCC-voltage regulator), this increase in the grid voltage could also correspond to any other dynamics at the grid (e.g. load disconnection), then the over-voltage state cannot be a measure for islanding.

[16] The feeder parameters are given in Appendix C.

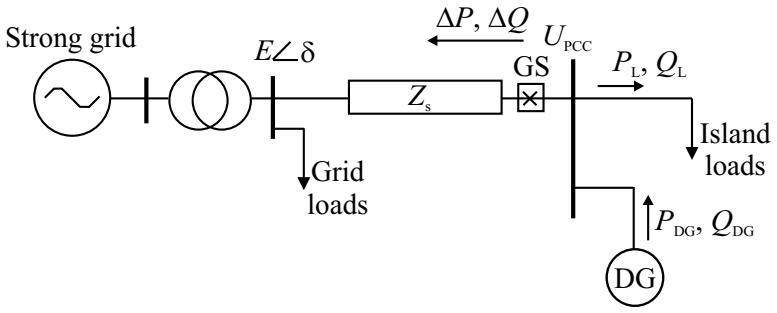

Fig. 5.2 System considered for islanding study.

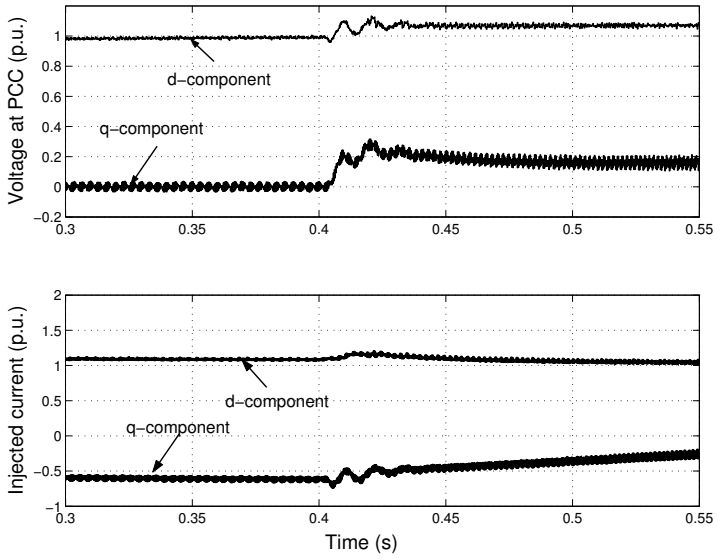

Fig. 5.3 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.4 s and $P_L < P_{DG}$.

If the load absorbed power is higher than the DG injected-power (in which case a load shedding criterion is important for a stable island operation), the PCC voltage will decrease in case of the grid outage. This case is represented in Fig. 5.4, where the grid outage occurs at 0.3 s, and the load active power is higher than the DG active power ($P_L = 1.07P_{DG}$) while the reactive power for both the load and the DG are equal. The DG controller, here, injects constant current into the grid, as shown by the lower

plot in the same figure. Since this decreased voltage could occur also due to voltage dips at the grid, hence the undervoltage is not a reliable state for islanding detection especially if the voltage dips ride-through capability is required. In other words, using the undervoltage state for the islanding detection may lead to false tripping during voltage dips.

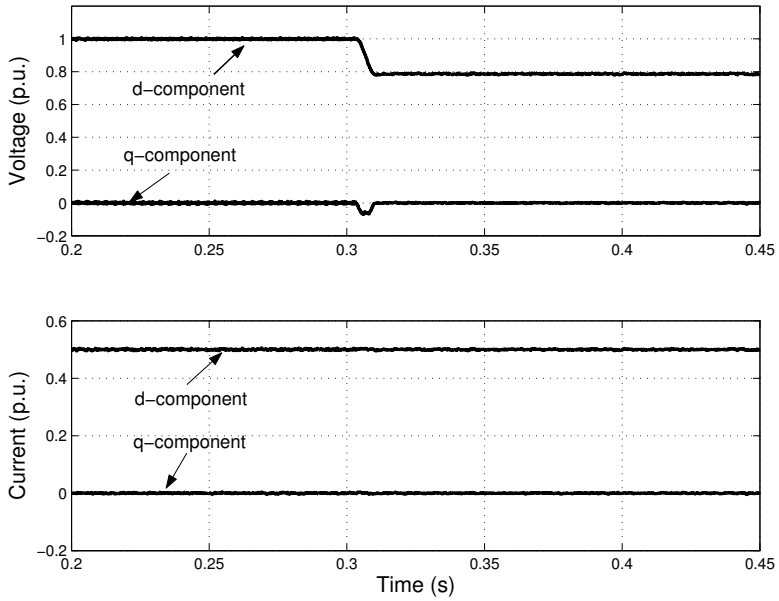

Fig. 5.4 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s and $P_L > P_{DG}$ (ΔP = -0.07 p.u.) and $Q_L = Q_{DG} = 0$.

In conclusion, an overvoltage/undervoltage islanding detection algorithm is not appropriate to be implemented. In addition, measuring other grid states (e.g. the phase angle jump) within a narrow threshold may falsely lead to islanding in case of other grid dynamics (e.g. switching events) [68].

Instead, using the signals generated within the DG controller to detect the islanding condition is considered. A disturbed signal within the controller will lead to a disturbed operation of the DG unit, and hence changing the control mode might be a good practice (even if the utility grid is not

disconnected). For instance, due to the grid outage and the reactive-power mismatch a constant nonzero value of the q-component of the voltage at the PCC will result (e.g. as shown in Fig. 5.3). This will cause an integrator windup of the PLL that in turn will result in a continuous increase (or decrease) in the estimated frequency as shown in Fig. 5.5 for a grid outage at 0.4 s. Hence, the estimated frequency signal is implemented here to detect the grid outage. This is done by assigning a threshold band for the estimated frequency. If the frequency crosses the band for a certain period of time, then the islanding condition is detected. For example, if the detection limit is set to 52 Hz then the islanding conditions are detected within 0.03 s.

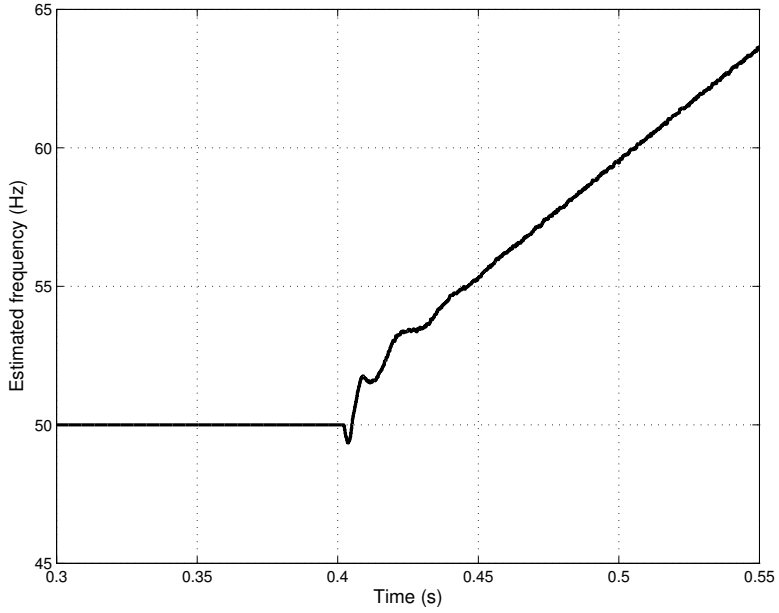

Fig. 5.5 Estimated frequency; grid outage at 0.4 s (P_L<P_{DG}).

To detect the grid recovery, the voltage measurement on the grid side of the grid switch (GS), shown in Fig. 5.2, is needed. If the voltage is back an extra PLL is used for the synchronization between the DG-output voltage and the grid voltage before connecting back the island to the grid.

Passive detection algorithm

The passive detection algorithm, which is implemented here, is shown in Fig. 5.6. Starting from the parallel (or grid-connected) operation, where the DG is aiming at controlling the active and reactive currents injected into the grid, the detection algorithm will be activated to detect the grid outage. The algorithm uses the deviation between the estimated frequency signal, which is produced by the PLL, and the nominal value. A time threshold t_s is also incorporated to avoid false tripping due to load dynamics. This time threshold is set equal to the settling time of the PLL, which could be calculated using the PLL gain as follows

$$t_s = \frac{\ln 50}{k_{pll}} \tag{5-1}$$

where the settling time is defined as the time for the PLL output to settle down to within a tolerance band of 2% of the final value [70], and k_{pll} is the proportional gain of the PLL.

Once the islanding condition is detected, the DG starts an island operation mode where its aim is to hold the voltage and frequency at their nominal values as well as to adjust the injected active and reactive powers to support the island loads. In addition, the GS is used to disconnect the utility grid from the island for safety operation. A DC chopper is also needed to consume the extra power that could be coming from the primary energy source in a way to adjust the input power to match the load needs. Moreover, in this mode, the grid recovery detection is activated where the voltage on the grid side is sensed. Once the utility grid is recovered, the synchronization between the DG voltage and grid voltage is carried out using an extra PLL on the grid side. The connection to the grid is then done by enabling the GS and disabling the DC chopper.

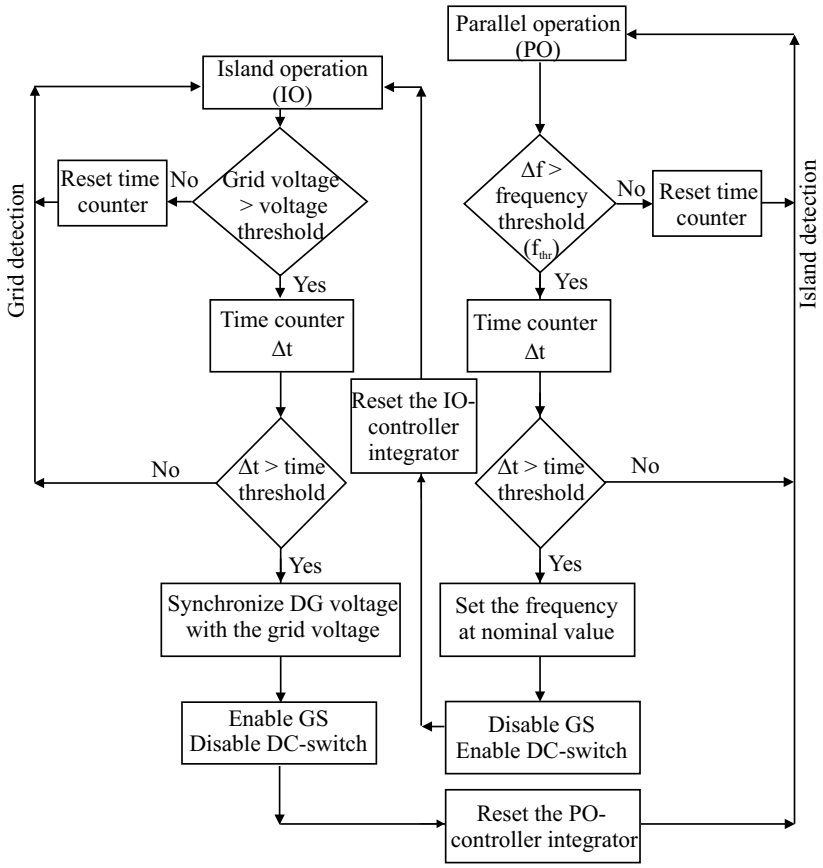

Fig. 5.6 Passive detection algorithm.

5.4 Non-detectable zone for passive detection

The non-detectable zone (NDZ) is usually described by the limits of active and reactive power mismatch (ΔP and ΔQ in Fig. 5.2) in which the detection algorithm would fail to recognize the grid outage [68]. These limits are related to the load characteristics, the detection method, and the controller of the DG.

The above described passive detection algorithm suffers from an open limit for ΔP in the NDZ. In other words, if the load reactive power exactly

matches the DG-injected reactive power, then, in case of the grid outage, the *q*-component of the PCC-voltage will not change irrespective of the amount of ΔP. This leads to undetectable islanding whatever the load active power is.

This case has been shown in Fig. 5.4, for $P_L > P_{DG}$ and constant active and reactive powers that are injected by the DG. Incorporating a PCC-voltage regulator within the DG controller, the change in the *d*-component of the PCC-voltage will lead to a change in the injected DG reactive current. Since the PCC-voltage will keep its decreased (or increased) value, due to the grid outage, the injected reactive current will keep a constant value (in case the DG is operating towards a strong grid) that will produce a reactive power mismatch and a change in the *q*-component of the PCC-voltage. This case is represented in Fig. 5.7, for the same loading condition as in Fig. 5.4. With the change in the *q*-component, an integrator windup in the PLL will result. Hence, the estimated frequency, shown in Fig. 5.8, will drop instantly leading to successful islanding-detection. As an example a frequency threshold of 48 Hz is detected within 0.01 s. This will lead to the decrease of the NDZ since either the active or reactive power mismatches will lead to a successful islanding detection.

In conclusion, combining the passive islanding-detection with the PCC-voltage regulator, described in Section 4.4, results in decreased NDZ. However, a complete match between the load and the DG unit active and reactive powers ($\Delta P = \Delta Q = 0$) would not be detected, since neither the *d*-component nor the *q*-component of the PCC-voltage would be affected by the grid outage. In this case, an active detection algorithm that injects a disturbance signal would be beneficial especially in case of a strong grid.

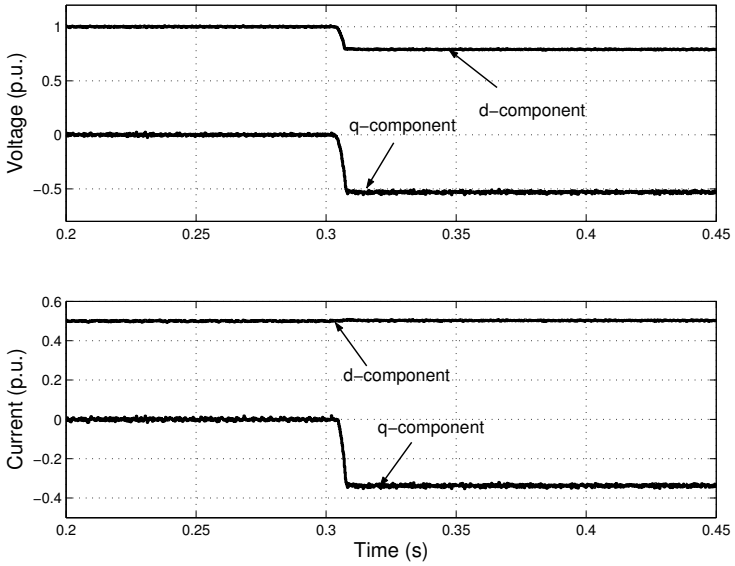

Fig. 5.7 Voltage at PCC (upper) and DG-injected currents (lower), with grid outage at 0.3 s; current-controlled DG with voltage regulation capability, and $P_L > P_{DG}$ ($\Delta P = -$ 0.07 p.u.).

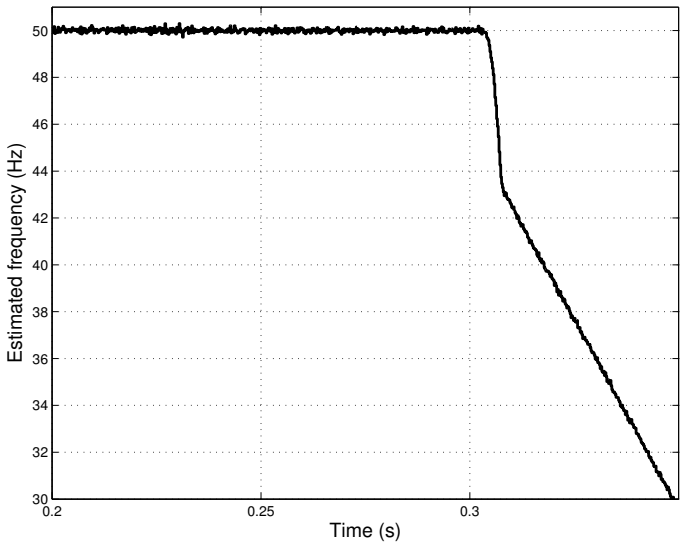

Fig. 5.8 Estimated frequency; grid outage at 0.3 s and current-controlled DG with voltage compensation capability, and ($\Delta P = -$ 0.07 p.u.).

5.5 Active Detection

The idea of the active detection is to try to disturb the grid in such a way that the passive detection will succeed to operate in the NDZ [69]. In a way to implement that, the active frequency drift method has been used in [79] and [43]. In this method, the waveform of the injected current is slightly distorted such that when islanding occurs the frequency of the phase voltage will drift up or down. Islanding is done in [43] by incorporating a washout function in the PLL that determines the change in the frequency and adds it to the frequency reference. Instead, in [39] a band pass filter is used, with the *d*-component voltage as an input, to deviate the voltage from its nominal value by changing the switching duty cycles.

In a way to optimize the design of the DG controller, the active detection is implemented here, using the PCC-voltage regulator. In case of a strong grid, the reference voltage signal in the PCC-voltage regulator is set to a value that is less than 1 p.u., while in case of a weak grid the reference voltage is set to 1 p.u.

The PCC-voltage regulator that is devoted for the operation in a strong grid is shown in Fig. 5.9. It operates in a way to produce a reactive current command i_q^* in such a way to force the voltage to deviate from its nominal value. The reference signal e_{dset} is set to a value that, when compared to the PCC-voltage e_d, produces an injected current within the maximum current limit of the DG. The limiter in the figure resets the integral part of the PI controller so that the current reference changes in a narrow band in order to decrease the current harmonics injected to the grid.

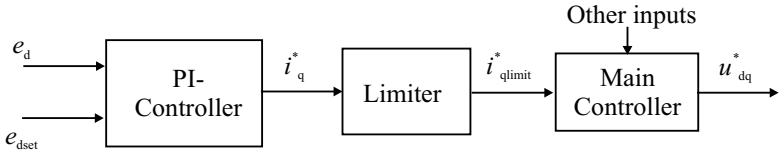

Fig. 5.9 Active islanding detection (PCC-voltage regulator).

The effect of adding the active islanding detection using the PCC-voltage controller is examined using a load that completely matches the DG power input (i.e. $\Delta P = \Delta Q = 0$). The DG injected active (*d*-component) and reactive (*q*-component) currents are shown in Fig. 5.10, without incorporating the active detection part (in the upper plot) and with incorporating it (in the lower plot), for a grid outage from 0.3 s to 0.4 s. From the figure, the increased value of the injected reactive current, in case of incorporating the active detection controller, implies producing a reactive power mismatch, in the normal operation, that in turn results in an islanding signal from the passive detection algorithm in case of grid outage.

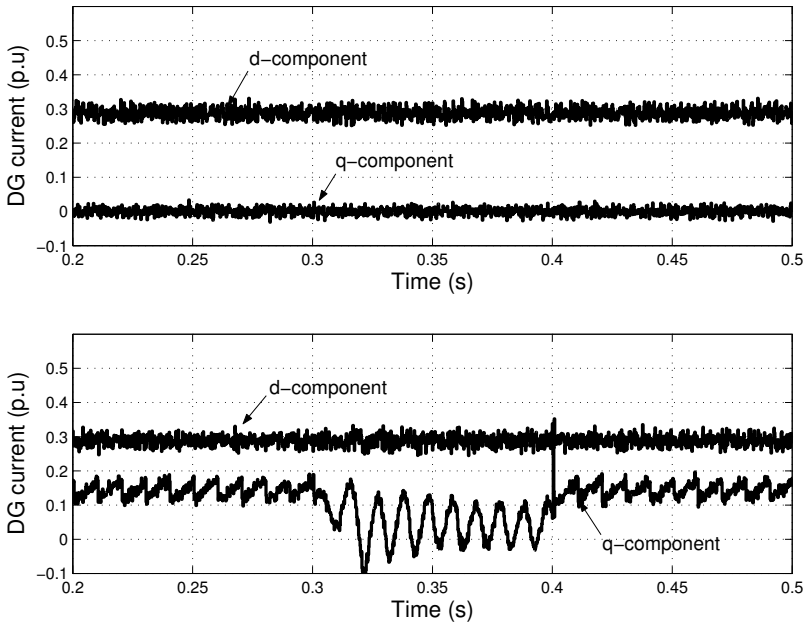

Fig. 5.10 DG injected active (d-component) and reactive (q-component) currents; without active detection controller (upper) and with active detection controller (lower) with a matching load.

The effect of using the active detection controller (i.e. the PCC-voltage controller) is also examined in case of a weak grid using a quadratic voltage dependent load that produces active power mismatch (ΔP) of 0.15 p.u. and

zero reactive power mismatch (ΔQ = 0) at the normal operation. A grid outage at 0.8 s is encountered. As shown in Fig. 5.11 (a) by the dashed line, the estimated frequency has a constant increase after 0.8 s, with the PCC-voltage regulator deactivated, due to a small change in the reactive power of the load that is in turn resulting from the increase of the PCC voltage, as shown in Fig. 5.11 (c). This increase in the estimated frequency could be relatively small and, depending on the frequency threshold set in the passive detection algorithm, it might not successfully detect the islanding condition. By activating the PCC-voltage regulator, the estimated frequency will continue to increase, as shown in Fig. 5.11 (a) by the solid line, after the grid outage at 0.8 s, due to the continuous increase in the DG injected reactive current that is shown in Fig. 5.11 (b), implying the successful detection of the islanding condition.

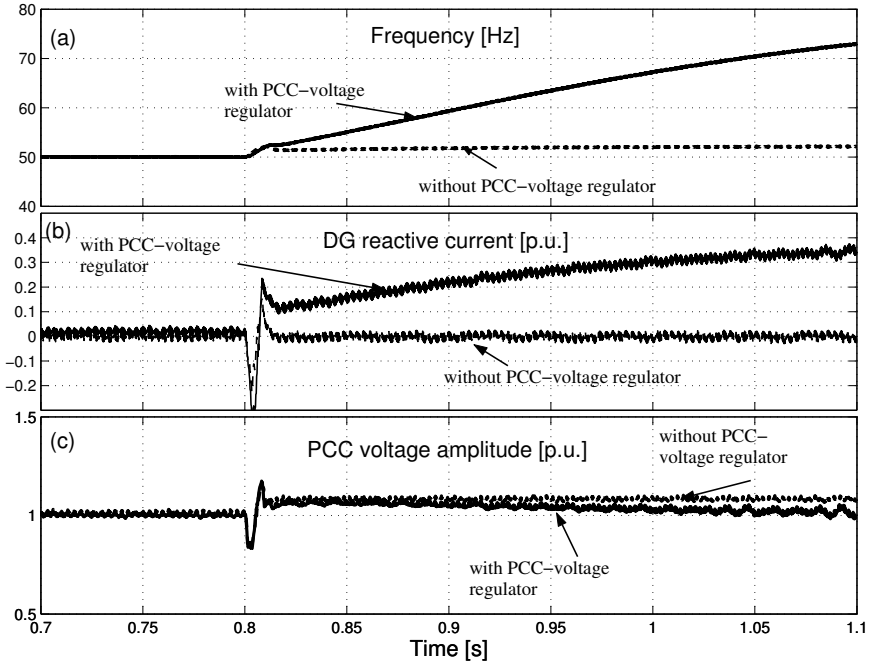

Fig. 5.11 Grid outage at 0.8 s, for ΔP = 0.15 and ΔQ = 0, with and without the PCC-voltage regulator. (a) the estimated frequency. (b) The DG injected reactive current. (c) The PCC-voltage amplitude.

The active detection method, using both the passive detection algorithm and the PCC-voltage regulator, are now to be examined.

5.6 Intentional islanding in a strong grid

A strong grid system is referring to a power system where the voltage and frequency at the load bus are kept constant, by the utility, regardless of the load dynamics. The system shown in Fig. 5.2 is considered where the PCC-voltage amplitude is kept constant at 1 p.u. during normal operation. The DG system is assumed to have an L-filter to smoothen out the current harmonics, and the DC-side is assumed to be controlled from the DG energy-source side for simplicity.

The DG controller will work on either one of the two operations; current-controlled or voltage-controlled, depending on the state of the utility grid as shown in Fig. 5.12.

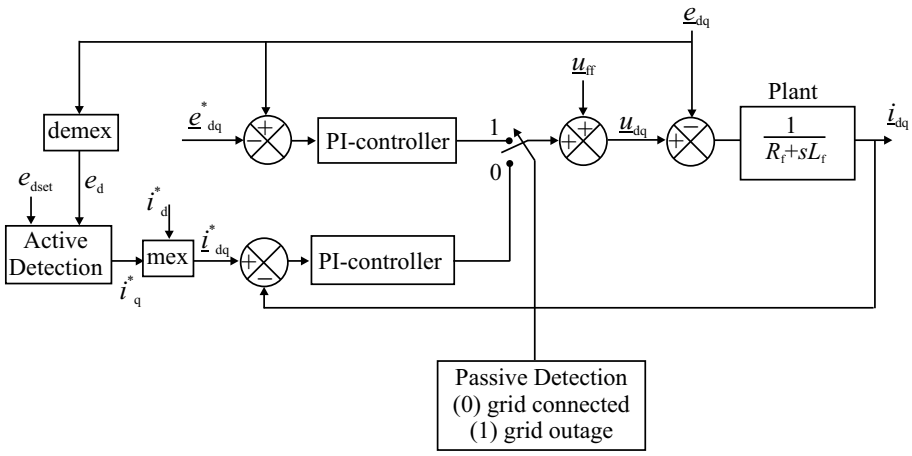

Fig. 5.12 Control transition between grid-connected and island modes.

The grid state is detected using the passive detection algorithm, shown in Fig. 5.6. In case of the grid outage, the detection algorithm will set the controller on the voltage control mode. In this mode the voltage nominal value is set as reference and compared with the measured voltage signal using a PI-controller. The output of this controller is added to the

feedforward voltage vector $\underline{u}_{ff}$. When the grid recovery occurs, the current controller will be activated. Moreover, the active detection is also incorporated in the controller in order to minimize the non-detectable zone as discussed before.

The island loads are set to draw higher power than the DG injected power, as described before for the case related to Fig. 5.4, to test the islanding detection and operation. It is assumed in this case that the energy source of the DG can inject more power to match the load in case of the occurrence of islanding (otherwise a load shedding criterion should be implemented). A grid outage has been encountered at 0.4 s, and the recovery of the grid occurred at 0.6 s. The controller has detected the outage and a transition to the voltage control mode has been performed, where the voltage has been set to 1 p.u., as shown in Fig. 5.13.

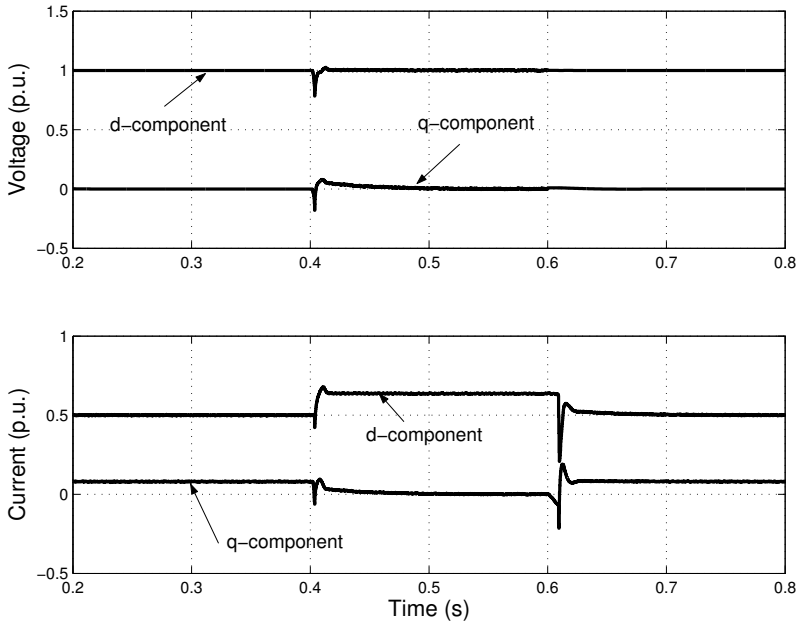

Fig. 5.13 PCC-voltage (upper), and DG injected currents (lower) in case of grid outage from 0.4 s to 0.6 s.

Before islanding, the *d*-component current has been set to 0.5 p.u., as shown by the lower trace of the same figure, while the *q*-component current i_q has been adjusted by the active detection controller to reduce the PCC-voltage *d*-component to 0.95 p.u. (i.e. e_{dset} = 0.95 p.u.). At the grid outage (at 0.4 s), i_q will start to change in a way to put the PCC-voltage amplitude to e_{dset}. However, this will change also the *q*-component of the voltage, which in turn will affect the estimated frequency as shown in Fig. 5.14 by the upper plot. This will lead to the setting of the passive detection signal, as shown in the same figure by the lower plot. Hence, the grid outage is detected and the grid switch GS is disconnected.

During the island operation, the DG injected currents will be set to match the load requirements. Moreover, the voltage angle is set to the reference value. When the grid is back, the voltage on the grid side of the GS will be sensed, and an extra PLL is used to synchronize the island back to the grid, then the GS is connected.

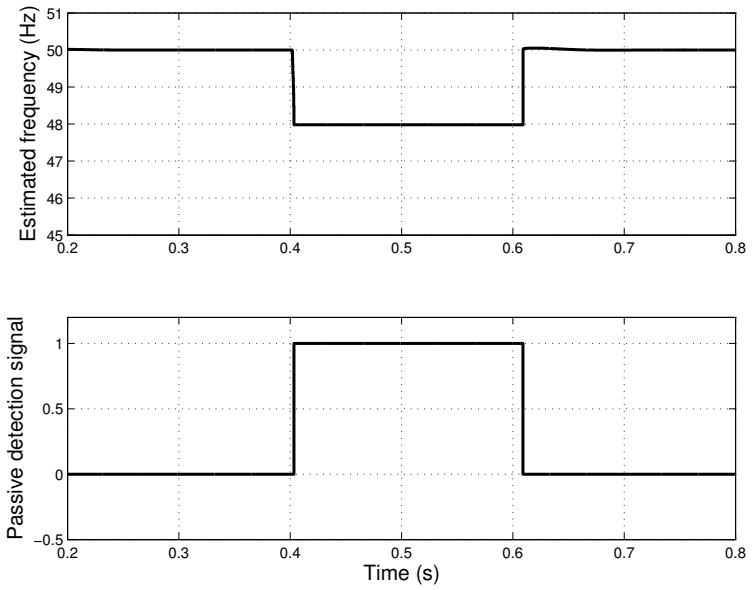

Fig. 5.14 Estimated frequency (upper), and passive detection signal (lower) in case of grid outage from 0.4 s to 0.6 s.

5.7 Intentional islanding in a weak grid

A weak grid system is referring, here, to systems where the voltage level at the load bus is not constant and is affected by the load dynamics. The system in Fig. 5.2 will be considered, where the voltage at the PCC is affected by the feeder voltage drop and the load dynamics. The island-loads are set such that their consumed power is lower than the DG-injected power. They are implemented as an aggregated quadratic voltage-dependent load, with a nominal active power mismatch (ΔP) of 0.55 p.u. and reactive power mismatch (ΔQ) of 0.2 p.u.

As has been discussed in the previous chapter, the voltage regulation capability of the DG is advantageous in the operation of weak grids since it will maintain the PCC voltage at the nominal value regardless of the load dynamics. Another advantage is highlighted here regarding the islanding. With the voltage regulation capability, the islanding non-detectable zone is reduced. This is especially important in the application of weak grids, since the active detection methods, which aim at disturbing the grid states, are not adequate for such grids since, during normal operation, the weak grid states (as opposite to strong grids) are changeable.

The DG system is considered here with the VSC as a front end and an LCL-filter to damp the line current harmonics. The grid-connected controller for this system has been described before in Section 2.6. The island-operation controller is shown in Fig. 5.15[17], where the voltage reference and the phase angle reference are set to their nominal values. A DC-link chopper is incorporated to dissipate the extra power that would come from the DG energy-source, in order to adjust the DG injected-power to match the load requirements.

The PCC-voltage is shown in Fig. 5.16, in the upper plot, for the operation of the DG before, during, and after islanding. The grid is disconnected at 0.3 s and recovered at 0.5 s.

[17] This controller has been explained in more details in Paper F.

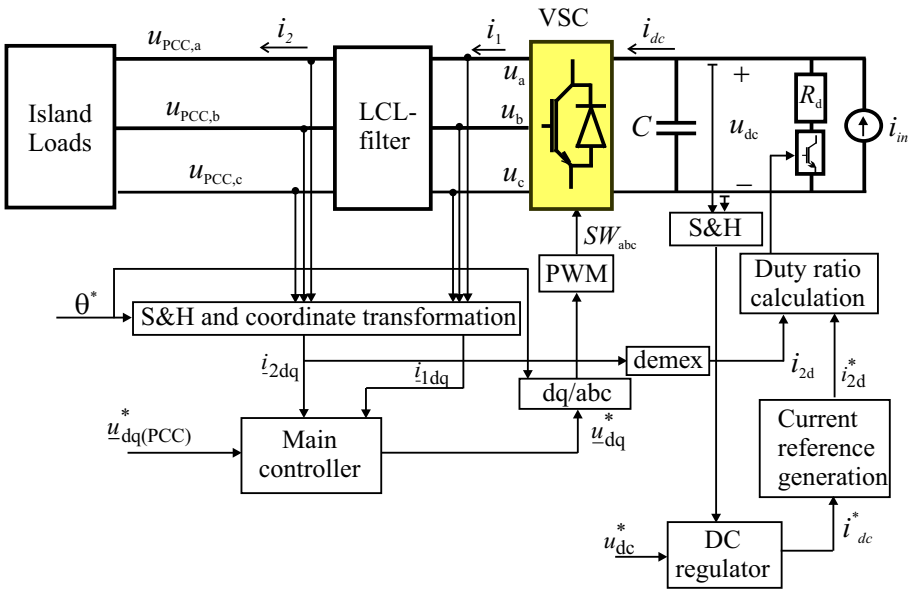

Fig. 5.15 Island operation controller for DG with LCL line filter.

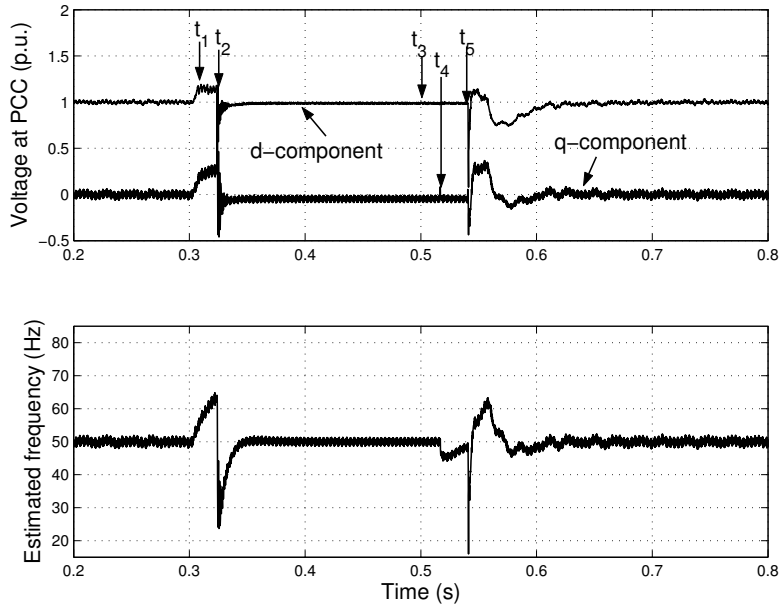

Fig. 5.16 Voltage in *dq*-frame at the PCC (upper) and estimated frequency (lower) for grid outage at 0.3 s and recovery at 0.5 s.

When the grid outage occurs at 0.3 s, the PCC voltage starts to increase in magnitude. When the *d*-component of the PCC-voltage $u_{d(PCC)}$ reaches the voltage limit, that is set by the controller, at t_1, the constant-limited value is maintained (until t_2). The frequency, which is shown by the lower plot of the same figure, will continue to increase after t_1, due to the constant value of the voltage *q*-component, until the island is detected at t_2. The detection algorithm will start to react after reaching the time threshold t_s, when the detection signal is activated (at t_2), resulting in transferring the controller from grid-connected mode to island-operation mode. At t_2 the frequency will be reset to its nominal value, and the DG injected powers, which are shown by the upper plot in Fig. 5.17, will start to adjust to match the load requirements. In consequence, the injected currents will decrease in magnitude, as shown in Fig. 5.18. Moreover, the DC-link voltage, which is shown in Fig. 5.17 by the lower plot, will maintain its nominal value in spite of the decreased injected DG-active power to the grid, since the DC chopper switch has been activated to dissipate the extra power in the chopper.

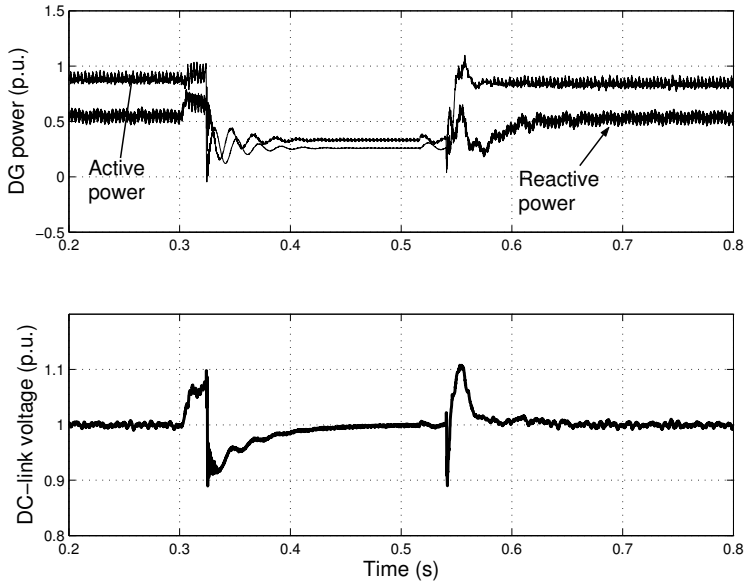

Fig. 5.17 DG injected power (upper) and DC-link voltage (lower) for grid outage at 0.3 s and recovery at 0.5 s.

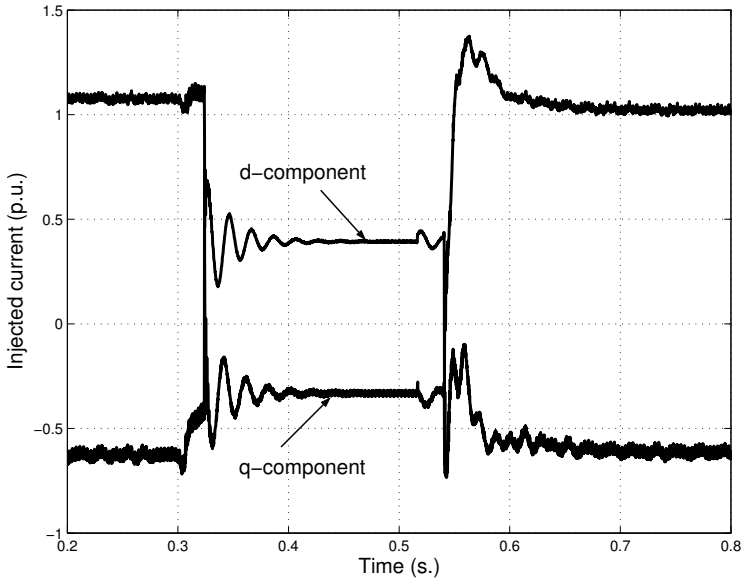

Fig. 5.18 DG injected current in dq-frame; grid outage at 0.3 s and recovery at 0.5 s.

When the grid voltage is recovered at t_3, a time threshold is also encountered before the synchronization of the grid voltage and DG voltage starts at t_4. This is done by using an extra PLL that is implemented for the voltage before the grid switch (GS in Fig. 5.2) from the utility grid side. At t_4, the phase angle of the DG voltage is set equal to the phase angle of the grid voltage. This could be seen from the change of the frequency signal in Fig. 5.16. After about one cycle of the fundamental frequency, the island is connected back to the utility grid at t_5. The DC-chopper is left in operation to buck the over-voltage that could occur at the starting of the grid-connected controller mode, until the PCC-voltage is stabilized.

At the starting of the grid-connected operation, $u_{d(PCC)}$ will drop to a value that represents its normal amplitude in case of deactivating the voltage regulator of the DG. This is mainly due to the PCC-voltage regulator transient time, which has been set long enough to stabilize the overall DG controller. In spite of the decreased value of the voltage during this time, the duration is very small compared with the clearing times that are shown in Fig. 5.1. After the transient time of the PCC-voltage regulator, the PCC-

voltage amplitude will be regained to the nominal value. In addition, the DG injected powers and currents will regain the values that are set for the grid connected operating mode.

5.8 Islanding detection reliability

Voltage dips appearing at the PCC, due to remote faults or motor starts, may lead to false tripping of the DG. The reason is that for small voltage dip amplitudes, the PCC voltage regulator may become unstable resulting in a disturbed PCC voltage that in turn will result in islanding. For instance, referring to Fig. 4.6 with a DG injected active power of 0.8 p.u. and a voltage dip magnitude of 0.7 p.u., the voltage regulator will become unstable and islanding will be detected for this case. Decreasing the DG input power would result in improving the voltage dip ride-through capability (as has been discussed in Chapter 3) and the reliability of the islanding detection.

Moreover, the effect of limiting the VSC current on the estimated frequency in case of voltage dips at the grid with induction motor loads at the PCC has been discussed in [81]. For sufficiently high current limit, the controller is able to maintain the voltage and frequency at the PCC at their nominal values. That would imply robust islanding detection.

The effect of setting a reactive current limit on the robustness of the islanding detection has been, also, discussed in Paper G, where the island loads have been implemented as an induction machine load. By setting the proper current limit, the DG unit can have the ability to ride-through voltage dips with magnitudes above a certain limit, which can be set according to the grid codes, and detect islanding for voltage dips with magnitudes lower than that limit.

5.9 Conclusions

In this chapter, the possibility of intentional islanding has been discussed. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection method should be applied. The islanding detection technique should be able to differentiate between grid dynamics and the islanding condition, and to provide the correct detection signal irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch. The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC). The NDZ, for the converter-interfaced DGs, also depends on the control method.

Two islanding methods have been introduced here; namely passive and active. An active islanding detection method has been proposed to minimize the inherent NDZ of the passive technique. In this method, the estimated frequency signal has been used to detect islanding along with the PCC-voltage regulator. This detection method is motivated by the operation of the DG in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the same method can be used by changing the reference value of the PCC-voltage regulator so as to produce a disturbing current signal in the grid.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The main focus of the thesis has been put on the study of the interface requirements and capabilities of a DG with a voltage source converter (VSC) as a front end. Two line filters have been considered at the connection point of the DG; namely an inductance line filter (L-filter) and an inductance-capacitance-inductance line filter (LCL-filter).

Vector current controller (VCC)

In the first place, **vector current controllers (VCC)** have been implemented, in the rotating synchronous *dq*-frame, for both systems. The time delay, with one sample length, that results due to the calculation time has been compensated for using a Smith predictor, which predicts the grid currents one sample ahead. In addition, the controller saturation, which could result due to high current steps, has been avoided using a voltage limiting algorithm. Besides, to avoid integrator windup, which also could result due to high current steps, the limited voltage has been used in the Smith predictor to recalculate the currents. A DC-link voltage regulator has been also incorporated in the controller to protect the capacitor on the DC-side during different load changes. Moreover, a dual vector current controller (DVCC) has been implemented, which comprises two VCCs. One of them is described in the positive rotating *dq*-frame and the other is described in the negative rotating *dq*-frame, to improve the performance in the case of unbalanced grid-voltage. Moreover, convenient current reference equations have been derived based on the power balance between the DC-side and the

AC-side of the VSC. The controllers have shown good current reference tracking even when high current steps are applied. In addition, in case of unbalanced grid-voltage, oscillating powers will be produced. When those powers are forced to be supplied from the grid side, it has been also shown that the DC-link voltage oscillations are negligible.

Voltage dips ride-through capability

Furthermore, the current-controlled converter interfaced DG has been studied in relation to different grid interface issues. First the **voltage dips ride through capability** has been discussed. For that purpose, a previously investigated voltage dips classification has been adopted to study the effect of all the possible voltage dips that could appear at the DG terminals. In addition, that classification has been modified to be implemented in the positive and negative sequence *dq*-frames. The equations of the maximum currents that would flow through the VSC valves due to all possible voltage dips have been derived. It has been shown that these analytical expressions give almost the same maximum current values as the numerical calculations based on simulation. It has been shown that if the converter-interfaced DG should ride-through the dip period there are two alternatives. One is to oversize the converter switches to withstand the increased currents. The other is to decrease the power input from the source during the dip period, so that the currents will be decreased. However, the latter would require that the input power to the DC-link be reduced very quickly, which could be an issue regarding the energy source or the control of an energy storage connected to the DC-link.

Voltage regulation capability

Thereafter, the **voltage regulation capability** has been discussed. This capability is beneficial if the compensation for the grid voltage quality problems is required. With this capability, the compensation of voltage dips, voltage harmonics, voltage amplitude modulation … etc. would be possible resulting in better power quality at the grid. Moreover, if the DG is working towards a weak grid, where the voltage level is dependable on the load

dynamics, this capability will help in maintaining the voltage level at its nominal value. However, an important issue is the voltage regulation limits, at which the voltage regulator is stable. These limits were discussed and are related to the loading at the grid. It has been shown that, the more input power coming from the DG source, the more reactive power is available to compensate for the voltage. However, in case of increased active and reactive powers, the current limit could be reached. Hence, the compensation capability is limited by the maximum current that the VSC would stand. Another limit is presented by the load that is connected at the same connection point as the DG. If the load has a low power factor, it means that more injected reactive power is needed to regulate the voltage. This in turn would increase the injected current. Another issue that could affect the voltage regulation capability is the voltage phase-angle extraction.

It has been shown that using a PLL that implements the fundamental component of the grid voltage a smaller error in the estimated phase angle would be produced and hence resulting in better grid voltage regulation. A neural-networks based PLL has (NN-PLL) been introduced for that purpose. The NN-PLL has been compared with a previously investigated PLL that extracts the angle of the positive sequence voltage, which is referred to here as PS-PLL. The NN-PLL has performed superior compared to the conventional PLL when the grid voltage harmonics are significant, and the case of grid voltage amplitude modulation.

Intentional islanding capability

Finally, the **intentional islanding capability** has been studied. Intentional islanding refers to the situation of having a planned island in case of a grid outage. To start the island operation, a reliable islanding detection algorithm should be applied. The islanding detection technique should be able to differentiate between grid dynamics and islanding condition, so that a correct detection signal is provided, irrespective of the loading at the grid. A common measure for the different islanding techniques is their related non-detectable zone (NDZ), which refers to the amplitude of the active and reactive power mismatch at which the detection algorithm will malfunction.

The power mismatch is the difference between the power consumed by the load and injected by the DG at the point of common coupling (PCC).

Two islanding techniques have been examined here; namely passive and active techniques. In the passive technique, the estimated frequency signal in combination with the PCC-voltage regulator has been used to detect islanding with a minimum NDZ. That could be a beneficial application in weak grids, where the regulation capability is required to maintain the PCC-voltage at its nominal value during normal operation. On the other hand, if the DG is operating in a strong grid, the active technique has shown to be beneficial. In this technique, which incorporates also the passive algorithm using the estimated frequency, a reactive current reference is set in order to change the voltage at the PCC. If the voltage changes, it will result in the detection of the island. The two islanding-detection methods have been examined for the operation of a converter-interfaced DG that is working together with both a strong grid and a weak grid. The islanding-detection technique has successfully detected the island in case of islanding condition, while it did not react during a voltage dip at the grid.

6.2 Future work

The grid interconnection capability of a converter-interfaced DG has been studied here regarding the front end converter only. The study of the whole DG system and its effect on the interface capabilities is an interesting topic and could result in setting preferable topologies for the optimal operation. For instance, the capability of voltage dips ride through has been related to the DG source input power. If this input power could be changed in a very short time, then the ride through capability could be provided without oversizing the front end converter. Moreover, providing controllable storage at the DC-link could help in storing the extra power during island operation. That could result in supporting the island for longer time duration and the stored power could be used during voltage dips to ride through the dip period.

Another interesting research point is the study of the parallel operation of converter interfaced DGs regarding the voltage regulation capability and

islanding. The parallel operation could be already motivated from the energy resource point of view. For instance the aggregated DG systems are common for wind energy applications. Using several DGs at the same connection point could increase the voltage regulation capability and provide better support in case of islanding. The design of a central controller, however, is an important issue. The controller should be designed to provide control coordination between different DG units with possibly different control aims. Sliding mode control approach could be implemented for the control of parallel converter-interfaced DGs that are operating in close proximity [72]. This control technique is based on variable structure systems (VSS), which are defined as systems where the circuit topology is intentionally changed following certain rules to improve the system behaviour in terms of speed of response, stability and robustness [12]. Hence, the operational idea of this controller could be to change the physical structure of the connected DGs to meet the physical or electrical changes on the grid.

Furthermore, since the grid outage detection algorithm plays an important role in providing a stable island by setting the DG controller into the required function, it is of great importance to develop a reliable detection algorithm. An algorithm with a negligible non-detectable zone (NDZ) implies a successful grid outage detection regardless of the loading condition of the grid or the injected power of the DG. Active islanding has been previously introduced to provide such a reliable detection. However, the equipment of active islanding can have a drawback of polluting the grid. Besides, the equipment cannot be implemented in the case of a weak grid, where the grid states are changeable even during normal operation. The use of smart sensors could present another possible and reliable way in the grid outage detection. A smart or wireless sensor is comprised of a sensor, a processor, and wireless communication all on a single chip owing to the recent advances in micro-electro-mechanical systems (MEMS) technology [73], [74]. Smart sensors could be implemented for the coordination between the controllers for islanding detection through the interaction with the protection system or the grid operator. In addition, smart sensors could be

implemented for the coordination between the controllers for parallel operating DGs.

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Appendix A
Transformations for three-phase systems

A.1 Transformation of three-phase quantities into vectors

A three-phase positive system constituted by the three quantities $x_1(t)$, $x_2(t)$ and $x_3(t)$ can be transformed into a vector in a complex reference frame, usually called $\alpha\beta$-frame, by applying the transformation defined by

$$\underline{x} = x_\alpha(t) + \mathrm{j}x_\beta(t) = \frac{2}{3}K\left[x_1(t) + x_2(t)\cdot \mathrm{e}^{\mathrm{j}\frac{2}{3}\pi} + x_3(t)\cdot \mathrm{e}^{\mathrm{j}\frac{4}{3}\pi}\right] \tag{A.1}$$

where the factor K is usually taken equal to $\sqrt{\frac{3}{2}}$ for ensuring power invariance between the two systems. Equation (A.1) can be expressed as a matrix equation:

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = \mathbf{C_{23}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.2}$$

where

$$\mathbf{C_{23}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.3}$$

The inverse transformation is given by:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{32}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \tag{A.4}$$

where

$$\mathbf{C_{32}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.5}$$

This holds under the assumption that the sum of the three quantities is zero. Otherwise, there will also be a constant (zero-sequence) component. In the latter case, (A.2) and (A.4) become

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} = \mathbf{C_{230}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.6}$$

and for the inverse transformation

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{320}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} \tag{A.7}$$

with the two matrixes given by

$$\mathbf{C_{230}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} \end{bmatrix} \tag{A.8}$$

and

$$\mathbf{C_{320}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \end{bmatrix}. \tag{A.9}$$

A.2 Transformation from fixed to rotating coordinate system

Let the vectors $\underline{v}(t)$ and $\underline{w}(t)$ rotate in the $\alpha\beta$-frame with the angular frequency $\omega(t)$ in the positive (counter-clockwise) direction. If the vector $\underline{w}(t)$ is taken as the *d*-axis of a *dq*-frame that rotates in the same direction with the same angular frequency $\omega(t)$, both vectors $\underline{v}(t)$ and $\underline{w}(t)$ will appear as fixed vectors in that frame. The components of $\underline{v}(t)$ in the *dq*-frame are thus given by the projections of the vector on the direction of $\underline{w}(t)$ and on the orthogonal direction, as illustrated in Fig. A.1.

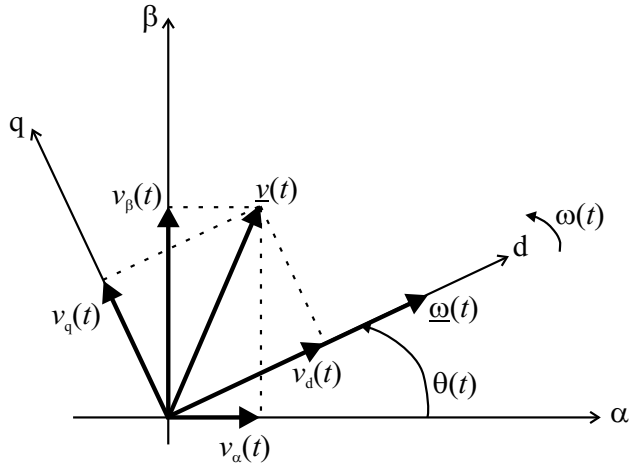

Fig. A.1 Relation between the $\alpha\beta$-frame and *dq*-frame.

The transformation can be written in vector form as:

$$\underline{v}_{\mathrm{dq}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{v}_{\alpha\beta}(t) \tag{A.10}$$

with the angle $\theta(t)$ in Fig. A.1 given by

$$\theta(t) = \theta_0(t) + \int_0^{\tau} \omega(\tau)\, d\tau \tag{A.11}$$

and the inverse transformation is defined by the expression

$$\underline{v}_{\alpha\beta}(t) = \mathrm{e}^{\mathrm{j}\theta(t)} \cdot \underline{v}_{\mathrm{dq}}(t) \tag{A.12}$$

The components in the *dq*-frame can be determined from Fig. A.1. In matrix form, the transformation from the $\alpha\beta$-frame to the *dq*-frame can be written as:

$$\begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}(-\theta(t)) \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} \tag{A.13}$$

and the inverse is given by

$$\begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} = \mathbf{R}(\theta(t)) \begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} \tag{A.14}$$

where the projection matrix is

$$\mathbf{R}(\theta(t)) = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \tag{A.15}$$

A.3 Transformations for voltage and current vectors in the *dq*-system

Suppose a symmetrical sinusoidal three-phase voltage with angular frequency $\omega(t)$ is transformed into a vector $\underline{u}(t) = u_{\alpha}(t) + \mathrm{j}u_{\beta}(t)$ in the $\alpha\beta$-frame. When transforming it further to the *dq*-frame, the *q*-axis in the *dq*-frame is normally defined as parallel to the voltage vector $\underline{u}(t)$. This definition originates from a flux vector parallel to the *d*-axis in the *dq*-frame. The voltage vector is proportional to the time derivative of the flux vector. As a consequence of the chosen reference vector, the voltage vector $\underline{u}(t)$ will only contain a *q*-component in the *dq*-frame. The transformation equation for a current vector from the $\alpha\beta$-frame to the *dq*-frame becomes, in matrix form:

$$\begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}\left(-\left(\omega t - \frac{\pi}{2}\right)\right) \cdot \begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} \tag{A.16}$$

and the inverse

$$\begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} = \mathbf{R}\left(\omega t - \frac{\pi}{2}\right) \cdot \begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} \tag{A.17}$$

The transformation from the $\alpha\beta$-frame into the dq-frame for current vectors is the same as for voltage vectors.

A.4 Voltage vectors for unsymmetrical three-phase systems

The phase voltages for a three-phase system can be written as

$$\begin{aligned} e_{\mathrm{a}}(t) &= E_{\mathrm{a}}(t)\cdot\cos(\omega t-\varphi_{\mathrm{a}}) \\ e_{\mathrm{b}}(t) &= E_{\mathrm{b}}(t)\cdot\cos(\omega t-\frac{2}{3}\pi-\varphi_{\mathrm{b}}) \\ e_{\mathrm{c}}(t) &= E_{\mathrm{c}}(t)\cdot\cos(\omega t-\frac{4}{3}\pi-\varphi_{\mathrm{c}}) \end{aligned} \tag{A.18}$$

where $E_{\mathrm{a}}(t)$, $E_{\mathrm{b}}(t)$ and $E_{\mathrm{c}}(t)$ are the amplitudes of the three-phase voltages, φ_{a}, φ_{b} and φ_{c} are the phase angles of the three-phase voltages, and ω is the angular frequency of the system.

If the amplitudes $\hat{e}_{\mathrm{a}}(t)$, $\hat{e}_{\mathrm{b}}(t)$ and $\hat{e}_{\mathrm{c}}(t)$ are unequal, the voltage vector can be written as the sum of two vectors rotating in opposite directions and interpreted as positive- and negative-sequence vectors

$$\underline{e}_{\alpha\beta}(t) = E_{\mathrm{p}}\mathrm{e}^{\mathrm{j}(\omega t+\varphi_{\mathrm{p}})} + E_{\mathrm{n}}\mathrm{e}^{-\mathrm{j}(\omega t+\varphi_{\mathrm{n}})} \tag{A.19}$$

where E_{p} and E_{n} are the amplitudes of positive- and negative-sequence vectors, respectively, and the corresponding phase angles are denoted by φ_{p} and φ_{n}. To determine amplitudes and phase angles of positive- and negative-sequence vectors in (A.19), a two-step solving technique can be used. First, the phase shifts are set to zero, so that the amplitudes E_{p} and E_{n} can easily be detected. In the next step, the phase shifts φ_{p} and φ_{n} are determined.

When transforming an unsymmetrical three-phase voltage into the dq-coordinate system, two rotating frames are used, accordingly. They are

called positive and negative synchronous reference frames and denoted by *dqp*- and *dqn*-, respectively. They can be defined by the transformations

$$\underline{e}_{\mathrm{dqp}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.20}$$

$$\underline{e}_{\mathrm{dqn}}(t) = \mathrm{e}^{+\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.21}$$

where the transformation angle $\theta(t)$ is locked to the positive phase sequence flux vector. The positive phase sequence vector in the *dqp*-coordinate system is expressed as

$$e_{\mathrm{dp}} + \mathrm{j}e_{\mathrm{qp}} = -E_{\mathrm{p}}\sin(\varphi_{\mathrm{p}}) + \mathrm{j}E_{\mathrm{p}}\cos(\varphi_{\mathrm{p}}) \tag{A.22}$$

and the negative phase sequence vector in the *dqn*-coordinate system is given by

$$e_{\mathrm{dn}} + \mathrm{j}e_{\mathrm{qn}} = -E_{\mathrm{n}}\sin(\varphi_{\mathrm{n}}) + \mathrm{j}E_{\mathrm{n}}\cos(\varphi_{\mathrm{n}})\,. \tag{A.23}$$

Appendix B
LCL-filter design

The schematic diagram of the power circuit of the VSC connected to the grid through LCL-filter has been shown in Fig. 2.9.

Assuming the grid-voltage as a disturbance and neglecting R_1 and R_2, the transfer function of the filter is then $I_2(s)$ /$U(s)$, where I_2 is the filter current on the grid side and U is the VSC output voltage, and is calculated as follows:

$$\frac{U(s)}{I_1(s)} = \frac{L_2/C_f}{\left(sL_2 + \frac{1}{sC_f}\right)} + sL_1 = \frac{sL_2 + 1/sC_f}{s^2 L_1 L_2 + \frac{(L_1 + L_2)}{C_f}} \tag{B-1}$$

Using the current divider rule, the grid-side current is

$$I_2(s) = I_1(s)\frac{1/sC_f}{sL_2 + \frac{1}{sC_f}} \tag{B-2}$$

It follows that

$$I_1(s) = I_2(s)\cdot\left(s^2 L_2 C_f + 1\right) \tag{B-3}$$

Then the transfer function becomes

$$\frac{I_2(s)}{U(s)} = \frac{1/C_f L_1 L_2}{s\left(s^2 + \frac{L_1 + L_2}{L_1 L_2 C_f}\right)} \tag{B-4}$$

The resonant frequency is then:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{B-5}$$

The filter parameters are chosen such that the following conditions are satisfied [23], [71]:

- Neglecting the filter resistances, the voltage drop across the inductances should be limited to 10% during nominal operation, which agrees with the previous design criteria for L-filter;
- The grid side inductance is a fraction of the converter side inductance, since the latter is responsible for the attenuation of most of the switching ripple;
- The capacitive value is limited by the decrease of the power factor at rated power in case of idle operation of the VSC (it will be considered as less or equal 10%);
- The resonance frequency is in the range between ten times the fundamental frequency and one half the switching frequency;
- The IEC 1000-3-4 regulation states that current harmonics above 33rd should be less than 0.6% of the nominal current;
- The resistances are taken as 10% of the value of the corresponding inductances.

According to these conditions the following equations can be used

$$L_1 + L_2 = 0.1 \text{ p.u.} \tag{B-6}$$

$$L_2 = r \cdot L_1 \tag{B-7}$$

where r is the ratio between the inductance on the grid side to the inductance on the converter side, which is less than 1.

$$C_f \leq 0.1 \quad \text{p.u.} \tag{B-8}$$

$$500 \text{ Hz} < f_{res} < 1250 \text{ Hz} \quad \text{(for sampling frequency of 5kHz)} \tag{B-9}$$

From (B-4), the gain of the system at the h harmonic is expressed as

$$\left|G(jh\omega)\right| = \frac{1/C_f L_1 L_2}{\left| jh\omega\left((jh\omega)^2 + \frac{L_1 + L_2}{L_1 L_2 C_f} \right) \right|} \leq 0.006 \text{ .} \tag{B-10}$$

Equations (B-9) and (B-10) are used as check up conditions. Using a capacitance value of 0.05 p.u., (B-9) is not satisfied for different inductance ratios (r), as shown in Fig. B.1. Increasing the capacitance value to 0.1 p.u.,

a value of r = 0.4 has been chosen to satisfy all conditions (see Fig. B.2 and Fig. B.3). The LCL-filter parameters are then calculated as reported in Appendix C.

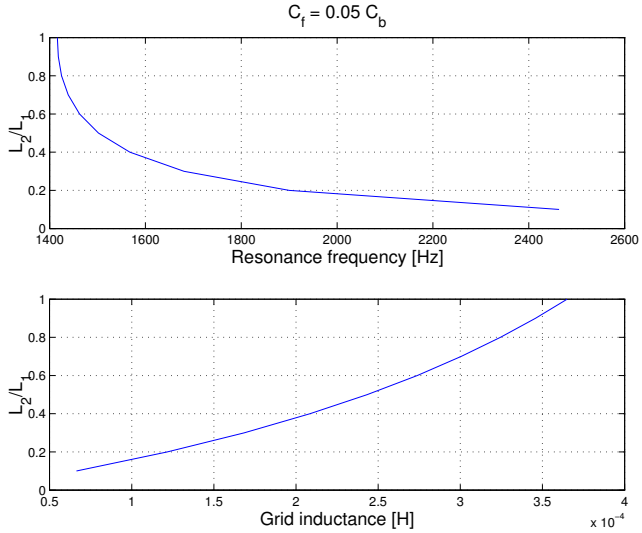

Fig. B.1 Relation between *r*, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 5% of the base value.

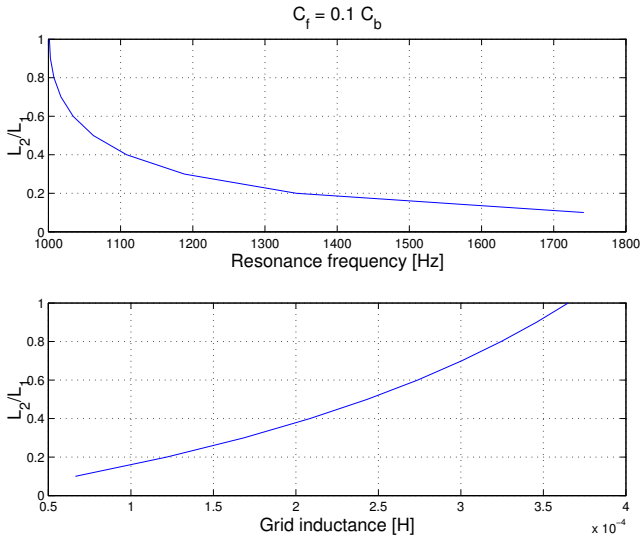

Fig. B.2 Relation between r, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 10% of the base value.

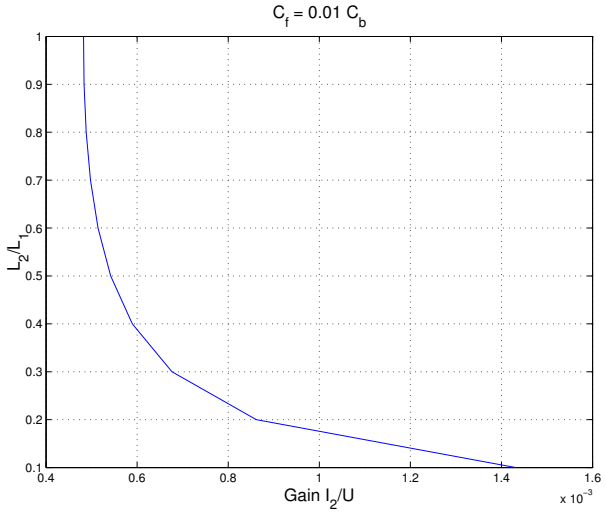

Fig. B.3 Relation between *r* and the gain filter I_2/U.

Appendix C
Power system parameters

C.1 Per-unit base values

The base values for the AC voltage and current are

$$E_{\text{base}} = 400 \text{ V} \tag{C-1}$$

$$I_{\text{base}} = 100 \text{ A} \tag{C-2}$$

The base value of the impedance is then obtained according to

$$Z_{\text{base}} = \frac{E_{\text{base}}}{\sqrt{3} I_{\text{base}}} = 2.3\Omega \tag{C-3}$$

The base values for the DC-link voltage and current are equal to

$$U_{\text{DC,base}} = 650 \text{ V} \tag{C-4}$$

$$I_{\text{DC,base}} = \frac{\sqrt{3} E_{\text{base}} I_{\text{base}}}{U_{\text{DC,base}}} = 107\text{A} \tag{C-5}$$

C.2 L-filter system data

Table C-1 System data with L-filter.

Description	Symbol	Value
Nominal RMS phase-to-phase AC voltage	E	400 V
Nominal RMS phase current	I_{n}	100 A
Nominal grid frequency	f_{n}	50 Hz
Nominal DC link voltage	U_{dc}	650 V
Nominal DC input current	I_{dc}	107 A
Filter resistance	R	23 mΩ
Filter inductance	L	0.73 mH
DC-link capacitance	C	550 µF
DC-chopper damping resistance	R_{d}	10 Ω

C.3 LCL-filter parameters

Table C-2 LCL-Filter parameters.

Parameter	p.u.	Actual
L_1	0.071	0.52 mH
R_1	0.1 L_1	1.6 mΩ
L_2	0.027	0.2 mH
R_2	0.1 L_2	0.6 mΩ
C_f	0.1	137.8 μF

C.4 Weak grid parameters

Table C-3 Weak network parameters.

Parameter	Value
V_s	400 V
R_s	3x0.05 Ω
L_s	3x2.05 mH
C_s	3x46 μF

Appendix D
Controller parameters

D.1 Parameters for VCC for L-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Dead beat gain	k_p	3.7
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.5

D.2 Parameters for VCC for LCL-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Outer controller gain	k_{p1} (0.7 k_{p2})	0.546
Second controller gain	k_{p2} (0.3 k_{p3})	0.78
Inner controller gain	k_{p3}	2.6
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.07

D.3 Parameters for DC-link voltage regulator

Table D-3 DC-link voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pdc}	0.4
Integral time	T_{idc}	0.04 s

D.4 Parameters for PCC-voltage regulator

Table D-4 PCC-voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pr}	0.5
Integral time	T_{ir}	0.05 s

Appendix E
LCL-filter current reference-generation

The power at the grid side S_2 is expressed as

$$S_2 = S_{\mathrm{ac},2} + S_{\mathrm{s}2,2} + S_{\mathrm{c}2,2} \tag{E-1}$$

where S_{ac} is the power at the fundamental frequency, $S_{\mathrm{s}2}$ and $S_{\mathrm{c}2}$ are sine and cosine components of the power at double the fundamental frequency, which are called the oscillating powers. The power is calculated in *dqp*- and *dqn*-frames as follows

$$S_2 = \left(e^{\mathrm{j}\omega t}\underline{e}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{e}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-2}$$

Expanding this equation leads to

$$\begin{aligned} S_{\mathrm{s}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{qn}} - e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dn}}i_{2\mathrm{qp}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dp}}i_{2\mathrm{dn}} - e_{\mathrm{qn}}i_{2\mathrm{qp}} - e_{\mathrm{dn}}i_{2\mathrm{dp}}\right) \end{aligned} \tag{E-3}$$

$$\begin{aligned} S_{\mathrm{c}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{dn}} + e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dn}}i_{2\mathrm{dp}} + e_{\mathrm{qn}}i_{2\mathrm{qp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dp}}i_{2\mathrm{qn}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} - e_{\mathrm{dn}}i_{2\mathrm{qp}}\right) \end{aligned} \tag{E-4}$$

The power at the converter side S_1 is expressed in the same manner and same designations as

$$S_1 = S_{\mathrm{ac},1} + S_{\mathrm{s}2,1} + S_{\mathrm{c}2,1} \tag{E-5}$$

It is calculated in *dqp*- and *dqn*- frames as follows:

$$S_1 = \left(e^{\mathrm{j}\omega t}\underline{u}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{u}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-6}$$

Expanding this equation results in the following:

$$\begin{aligned} S_{\mathrm{ac},1} &= u_{\mathrm{dp}} i_{\mathrm{1dp}} + u_{\mathrm{qp}} i_{\mathrm{1qp}} + u_{\mathrm{dn}} i_{\mathrm{1dn}} + u_{\mathrm{qn}} i_{\mathrm{1qn}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dp}} - u_{\mathrm{dp}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qn}}\right) \end{aligned} \tag{E-7}$$

$$\begin{aligned} S_{\mathrm{s}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1qn}} - u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dp}} i_{\mathrm{1dn}} - u_{\mathrm{qn}} i_{\mathrm{1qp}} - u_{\mathrm{dn}} i_{\mathrm{1dp}}\right) \end{aligned} \tag{E-8}$$

$$\begin{aligned} S_{\mathrm{c}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1dn}} + u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dn}} i_{\mathrm{1dp}} + u_{\mathrm{qn}} i_{\mathrm{1qp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dp}} i_{\mathrm{1qn}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} - u_{\mathrm{dn}} i_{\mathrm{1qp}}\right) \end{aligned} \tag{E-9}$$

Applying KVL to the outer loop of the LCL-filter

$$\underline{u}_{\mathrm{dqp}} = \underline{e}_{\mathrm{dqp}} + R_1 \underline{i}_{\mathrm{1dqp}} + \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqp}} + R_2 \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqp}} \tag{E-10}$$

$$\underline{u}_{\mathrm{dqn}} = \underline{e}_{\mathrm{dqn}} + R_1 \underline{i}_{\mathrm{1dqn}} - \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqn}} + R_2 \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqn}} \tag{E-11}$$

Applying KCL at the filter capacitor connection node

$$\underline{i}_{\mathrm{1dqp}} = \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqp}} \tag{E-12}$$

$$\underline{i}_{\mathrm{1dqn}} = \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqn}} \tag{E-13}$$

Substituting (E-10) to (E-13) in (E-7), the active power at the converter side will be

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}}\left(i_{\mathrm{2dp}} - Y_{\mathrm{c}} u_{\mathrm{cqp}}\right) + i_{\mathrm{1dp}}\left(R_1 i_{\mathrm{1dp}} - \omega L_1 i_{\mathrm{1qp}} + R_2 i_{\mathrm{2dp}} - \omega L_2 i_{\mathrm{2qp}}\right) \\ & + e_{\mathrm{qp}}\left(i_{\mathrm{2qp}} + Y_{\mathrm{c}} u_{\mathrm{cdp}}\right) + i_{\mathrm{1qp}}\left(R_1 i_{\mathrm{1qp}} + \omega L_1 i_{\mathrm{1dp}} + R_2 i_{\mathrm{2qp}} + \omega L_2 i_{\mathrm{2dp}}\right) \\ & + e_{\mathrm{dn}}\left(i_{\mathrm{2dn}} + Y_{\mathrm{c}} u_{\mathrm{cqn}}\right) + i_{\mathrm{1dn}}\left(R_1 i_{\mathrm{1dn}} + \omega L_1 i_{\mathrm{1qn}} + R_2 i_{\mathrm{2dn}} + \omega L_2 i_{\mathrm{2qn}}\right) \\ & + e_{\mathrm{qn}}\left(i_{\mathrm{2qn}} - Y_{\mathrm{c}} u_{\mathrm{cdn}}\right) + i_{\mathrm{1qn}}\left(R_1 i_{\mathrm{1qn}} - \omega L_1 i_{\mathrm{1dn}} + R_2 i_{\mathrm{2qn}} - \omega L_2 i_{\mathrm{2dn}}\right) \end{aligned} \tag{E-14}$$

where $Y_{\mathrm{c}} = \omega C_{\mathrm{f}}$. This reduces to

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}} i_{\mathrm{2dp}} + e_{\mathrm{qp}} i_{\mathrm{2qp}} + e_{\mathrm{dn}} i_{\mathrm{2dn}} + e_{\mathrm{qn}} i_{\mathrm{2qn}} \\ & + R_1\left(i_{\mathrm{1dp}}^2 + i_{\mathrm{1qp}}^2 + i_{\mathrm{1dn}}^2 + i_{\mathrm{1qn}}^2\right) \\ & + R_2\left(i_{\mathrm{2dp}} i_{\mathrm{1dp}} + i_{\mathrm{2qp}} i_{\mathrm{1qp}} + i_{\mathrm{2dn}} i_{\mathrm{1dn}} + i_{\mathrm{2qn}} i_{\mathrm{1qn}}\right) \\ & + \omega L_2\left(-i_{\mathrm{2qp}} i_{\mathrm{1dp}} + i_{\mathrm{2dp}} i_{\mathrm{1qp}} + i_{\mathrm{2qn}} i_{\mathrm{1dn}} - i_{\mathrm{2dn}} i_{\mathrm{1qn}}\right) \\ & + Y_{\mathrm{c}}\left(-u_{\mathrm{cqp}} e_{\mathrm{dp}} + u_{\mathrm{cdp}} e_{\mathrm{qp}} + u_{\mathrm{cqn}} e_{\mathrm{dn}} - u_{\mathrm{cdn}} e_{\mathrm{qn}}\right) \end{aligned} \tag{E-15}$$

which can be separated into three different parts as follows

$$P_{\mathrm{ac},1} = P_{\mathrm{ac},2} + \Delta P(i) + \Delta P(e) \tag{E-16}$$

where $\Delta P(i)$ is the active power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta P(e)$ is the active power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

In the same way, the reactive power at the converter side is calculated as

$$\begin{aligned} Q_{\mathrm{ac},1} = {} & e_{\mathrm{qp}} i_{2\mathrm{dp}} - e_{\mathrm{dp}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qn}} \\ & + \omega L_1 \left(i_{1\mathrm{dp}}^2 + i_{1\mathrm{qp}}^2 - i_{1\mathrm{dn}}^2 - i_{1\mathrm{qn}}^2 \right) \\ & + R_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{dp}} - i_{2\mathrm{dp}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qn}} \right) \\ & + \omega L_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{dp}} + i_{2\mathrm{qp}} i_{1\mathrm{qp}} - i_{2\mathrm{dn}} i_{1\mathrm{dn}} - i_{2\mathrm{qn}} i_{1\mathrm{qn}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cqp}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dp}} + u_{\mathrm{cqn}} e_{\mathrm{qn}} + u_{\mathrm{cdn}} e_{\mathrm{dn}} \right) \end{aligned} \tag{E-17}$$

which can be separated into three different parts, as follows

$$Q_{\mathrm{ac},1} = Q_{\mathrm{ac},2} + \Delta Q(i) + \Delta Q(e) \tag{E-18}$$

where $\Delta Q(i)$ is the reactive power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta Q(e)$ is the reactive power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

The sine and cosine components of the active oscillating power are derived as

$$\begin{aligned} P_{\mathrm{s}2,1} = {} & e_{\mathrm{dp}} i_{2\mathrm{qn}} - e_{\mathrm{qp}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dp}} \\ & + 2R_1 \left(i_{1\mathrm{dp}} i_{1\mathrm{qn}} - i_{1\mathrm{qp}} i_{1\mathrm{dn}} \right) \\ & - 2\omega L_1 \left(i_{1\mathrm{qp}} i_{1\mathrm{qn}} + i_{1\mathrm{dp}} i_{1\mathrm{dn}} \right) \\ & + R_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{qn}} - i_{2\mathrm{qp}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dp}} \right) \\ & - \omega L_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{qn}} + i_{2\mathrm{dp}} i_{1\mathrm{dn}} + i_{2\mathrm{qn}} i_{1\mathrm{qp}} + i_{2\mathrm{dn}} i_{1\mathrm{dp}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cdn}} e_{\mathrm{dp}} - u_{\mathrm{cqn}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dn}} - u_{\mathrm{cqp}} e_{\mathrm{qn}} \right) \end{aligned} \tag{E-19}$$

$$P_{s2,1} = P_{s2,2} + \Delta P_{s2}(i) + \Delta P_{s2}(e) \tag{E-20}$$

$$\begin{aligned} P_{c2,1} = {} & e_{dp} i_{2dn} + e_{qp} i_{2qn} + e_{dn} i_{2dp} + e_{qn} i_{2qp} \\ & + 2R_1 \left(i_{1dp} i_{1dn} + i_{1qp} i_{1qn} \right) \\ & + 2\omega L_1 \left(i_{1dp} i_{1qn} - i_{1dn} i_{1qp} \right) \\ & + R_2 \left(i_{2dp} i_{1dn} + i_{2qp} i_{1qn} + i_{2dn} i_{1dp} + i_{2qn} i_{1qp} \right) \\ & + \omega L_2 \left(-i_{2qp} i_{1dn} + i_{2dp} i_{1qn} + i_{2qn} i_{1dp} - i_{2dn} i_{1qp} \right) \\ & + Y_c \left(u_{cqn} e_{dp} - u_{cdn} e_{qp} - u_{cqp} e_{dn} + u_{cdp} e_{qn} \right) \end{aligned} \tag{E-21}$$

$$P_{c2,1} = P_{c2,2} + \Delta P_{c2}(i) + \Delta P_{c2}(e) \tag{E-22}$$

Expressing (E-15) to (E-21) in matrix form will result in

$$\begin{aligned} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} = {} & \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \begin{bmatrix} i_{2dp} \\ i_{2qp} \\ i_{2dn} \\ i_{2qn} \end{bmatrix} \\ & + \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \end{aligned} \tag{E-23}$$

The current references are then calculated using the following matrix

$$\begin{bmatrix} i_{2dp}^* \\ i_{2qp}^* \\ i_{2dn}^* \\ i_{2qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} - Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \tag{E-24}$$

The oscillating power, which is consumed by the filter inductors, is compensated by the power flow from the VSC side. Hence

$$P_{s2,1} = \Delta P_{s2}(i) \tag{E-25}$$

$$P_{c2,1} = \Delta P_{c2}(i) \tag{E-26}$$

Moreover, the active power at the VSC side is assumed to be equal to the power at the DC side of the converter.

$$P_{ac,1} = u_{dc}^{*} i_{v}^{*} \tag{E-27}$$

To achieve zero reactive power at the grid, $Q_{ac,1}$ should supply the reactive power consumed by the filter. Hence

$$Q_{ac,1} = \Delta Q(i) + \Delta Q_{c} \tag{E-28}$$

where ΔQ_{c} is the power loss in the filter capacitor, which is calculated as

$$\Delta Q_{c} = \omega C_{f} \left(u_{cdp}^{2} + u_{cqp}^{2} + u_{cdn}^{2} + u_{cqn}^{2} \right) \tag{E-29}$$

Paper A

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Paper B

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Paper C

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Paper D

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Paper E

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Paper G

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Appendix A
Transformations for three-phase systems

A.1 Transformation of three-phase quantities into vectors

A three-phase positive system constituted by the three quantities $x_1(t)$, $x_2(t)$ and $x_3(t)$ can be transformed into a vector in a complex reference frame, usually called $\alpha\beta$-frame, by applying the transformation defined by

$$\underline{x} = x_\alpha(t) + \mathrm{j}x_\beta(t) = \frac{2}{3}K\left[x_1(t) + x_2(t)\cdot \mathrm{e}^{\mathrm{j}\frac{2}{3}\pi} + x_3(t)\cdot \mathrm{e}^{\mathrm{j}\frac{4}{3}\pi}\right] \tag{A.1}$$

where the factor K is usually taken equal to $\sqrt{\frac{3}{2}}$ for ensuring power invariance between the two systems. Equation (A.1) can be expressed as a matrix equation:

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = \mathbf{C_{23}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.2}$$

where

$$\mathbf{C_{23}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.3}$$

The inverse transformation is given by:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{32}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \tag{A.4}$$

where

$$\mathbf{C_{32}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.5}$$

This holds under the assumption that the sum of the three quantities is zero. Otherwise, there will also be a constant (zero-sequence) component. In the latter case, (A.2) and (A.4) become

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} = \mathbf{C_{230}} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \tag{A.6}$$

and for the inverse transformation

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C_{320}} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} \tag{A.7}$$

with the two matrixes given by

$$\mathbf{C_{230}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} \end{bmatrix} \tag{A.8}$$

and

$$\mathbf{C_{320}} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \end{bmatrix}. \tag{A.9}$$

A.2 Transformation from fixed to rotating coordinate system

Let the vectors $\underline{v}(t)$ and $\underline{w}(t)$ rotate in the $\alpha\beta$-frame with the angular frequency $\omega(t)$ in the positive (counter-clockwise) direction. If the vector $\underline{w}(t)$ is taken as the *d*-axis of a *dq*-frame that rotates in the same direction with the same angular frequency $\omega(t)$, both vectors $\underline{v}(t)$ and $\underline{w}(t)$ will appear as fixed vectors in that frame. The components of $\underline{v}(t)$ in the *dq*-frame are thus given by the projections of the vector on the direction of $\underline{w}(t)$ and on the orthogonal direction, as illustrated in Fig. A.1.

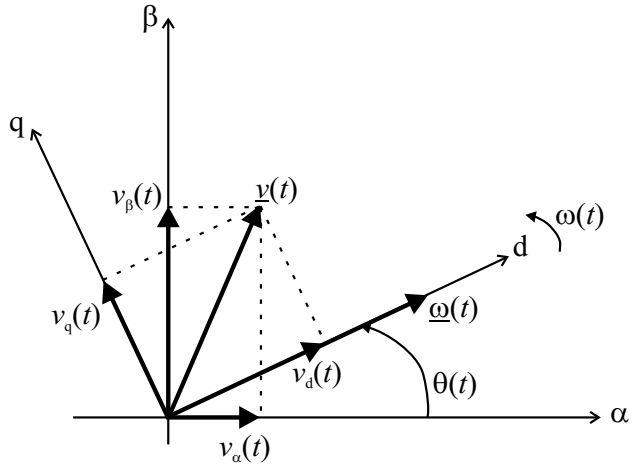

Fig. A.1 Relation between the $\alpha\beta$-frame and *dq*-frame.

The transformation can be written in vector form as:

$$\underline{v}_{\mathrm{dq}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{v}_{\alpha\beta}(t) \tag{A.10}$$

with the angle $\theta(t)$ in Fig. A.1 given by

$$\theta(t) = \theta_0(t) + \int_0^{\tau} \omega(\tau)\, d\tau \tag{A.11}$$

and the inverse transformation is defined by the expression

$$\underline{v}_{\alpha\beta}(t) = \mathrm{e}^{\mathrm{j}\theta(t)} \cdot \underline{v}_{\mathrm{dq}}(t) \tag{A.12}$$

The components in the *dq*-frame can be determined from Fig. A.1. In matrix form, the transformation from the $\alpha\beta$-frame to the *dq*-frame can be written as:

$$\begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}(-\theta(t)) \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} \tag{A.13}$$

and the inverse is given by

$$\begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} = \mathbf{R}(\theta(t)) \begin{bmatrix} v_{\mathrm{d}}(t) \\ v_{\mathrm{q}}(t) \end{bmatrix} \tag{A.14}$$

where the projection matrix is

$$\mathbf{R}(\theta(t)) = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \tag{A.15}$$

A.3 Transformations for voltage and current vectors in the *dq*-system

Suppose a symmetrical sinusoidal three-phase voltage with angular frequency $\omega(t)$ is transformed into a vector $\underline{u}(t) = u_{\alpha}(t) + \mathrm{j}u_{\beta}(t)$ in the $\alpha\beta$-frame. When transforming it further to the *dq*-frame, the *q*-axis in the *dq*-frame is normally defined as parallel to the voltage vector $\underline{u}(t)$. This definition originates from a flux vector parallel to the *d*-axis in the *dq*-frame. The voltage vector is proportional to the time derivative of the flux vector. As a consequence of the chosen reference vector, the voltage vector $\underline{u}(t)$ will only contain a *q*-component in the *dq*-frame. The transformation equation for a current vector from the $\alpha\beta$-frame to the *dq*-frame becomes, in matrix form:

$$\begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} = \mathbf{R}\left(-\left(\omega t - \frac{\pi}{2}\right)\right) \cdot \begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} \tag{A.16}$$

and the inverse

$$\begin{bmatrix} u_{\alpha}(t) \\ u_{\beta}(t) \end{bmatrix} = \mathbf{R}\left(\omega t - \frac{\pi}{2}\right) \cdot \begin{bmatrix} u_{\mathrm{d}}(t) \\ u_{\mathrm{q}}(t) \end{bmatrix} \tag{A.17}$$

The transformation from the $\alpha\beta$-frame into the dq-frame for current vectors is the same as for voltage vectors.

A.4 Voltage vectors for unsymmetrical three-phase systems

The phase voltages for a three-phase system can be written as

$$\begin{aligned} e_{\mathrm{a}}(t) &= E_{\mathrm{a}}(t)\cdot\cos(\omega t-\varphi_{\mathrm{a}}) \\ e_{\mathrm{b}}(t) &= E_{\mathrm{b}}(t)\cdot\cos(\omega t-\frac{2}{3}\pi-\varphi_{\mathrm{b}}) \\ e_{\mathrm{c}}(t) &= E_{\mathrm{c}}(t)\cdot\cos(\omega t-\frac{4}{3}\pi-\varphi_{\mathrm{c}}) \end{aligned} \tag{A.18}$$

where $E_{\mathrm{a}}(t)$, $E_{\mathrm{b}}(t)$ and $E_{\mathrm{c}}(t)$ are the amplitudes of the three-phase voltages, φ_{a}, φ_{b} and φ_{c} are the phase angles of the three-phase voltages, and ω is the angular frequency of the system.

If the amplitudes $\hat{e}_{\mathrm{a}}(t)$, $\hat{e}_{\mathrm{b}}(t)$ and $\hat{e}_{\mathrm{c}}(t)$ are unequal, the voltage vector can be written as the sum of two vectors rotating in opposite directions and interpreted as positive- and negative-sequence vectors

$$\underline{e}_{\alpha\beta}(t) = E_{\mathrm{p}}\mathrm{e}^{\mathrm{j}(\omega t+\varphi_{\mathrm{p}})} + E_{\mathrm{n}}\mathrm{e}^{-\mathrm{j}(\omega t+\varphi_{\mathrm{n}})} \tag{A.19}$$

where E_{p} and E_{n} are the amplitudes of positive- and negative-sequence vectors, respectively, and the corresponding phase angles are denoted by φ_{p} and φ_{n}. To determine amplitudes and phase angles of positive- and negative-sequence vectors in (A.19), a two-step solving technique can be used. First, the phase shifts are set to zero, so that the amplitudes E_{p} and E_{n} can easily be detected. In the next step, the phase shifts φ_{p} and φ_{n} are determined.

When transforming an unsymmetrical three-phase voltage into the dq-coordinate system, two rotating frames are used, accordingly. They are

called positive and negative synchronous reference frames and denoted by *dqp*- and *dqn*-, respectively. They can be defined by the transformations

$$\underline{e}_{\mathrm{dqp}}(t) = \mathrm{e}^{-\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.20}$$

$$\underline{e}_{\mathrm{dqn}}(t) = \mathrm{e}^{+\mathrm{j}\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \tag{A.21}$$

where the transformation angle $\theta(t)$ is locked to the positive phase sequence flux vector. The positive phase sequence vector in the *dqp*-coordinate system is expressed as

$$e_{\mathrm{dp}} + \mathrm{j}e_{\mathrm{qp}} = -E_{\mathrm{p}}\sin(\varphi_{\mathrm{p}}) + \mathrm{j}E_{\mathrm{p}}\cos(\varphi_{\mathrm{p}}) \tag{A.22}$$

and the negative phase sequence vector in the *dqn*-coordinate system is given by

$$e_{\mathrm{dn}} + \mathrm{j}e_{\mathrm{qn}} = -E_{\mathrm{n}}\sin(\varphi_{\mathrm{n}}) + \mathrm{j}E_{\mathrm{n}}\cos(\varphi_{\mathrm{n}})\,. \tag{A.23}$$

Appendix B
LCL-filter design

The schematic diagram of the power circuit of the VSC connected to the grid through LCL-filter has been shown in Fig. 2.9.

Assuming the grid-voltage as a disturbance and neglecting R_1 and R_2, the transfer function of the filter is then $I_2(s)$ /$U(s)$, where I_2 is the filter current on the grid side and U is the VSC output voltage, and is calculated as follows:

$$\frac{U(s)}{I_1(s)} = \frac{L_2/C_f}{\left(sL_2 + \frac{1}{sC_f}\right)} + sL_1 = \frac{sL_2 + 1/sC_f}{s^2 L_1 L_2 + \frac{(L_1 + L_2)}{C_f}} \tag{B-1}$$

Using the current divider rule, the grid-side current is

$$I_2(s) = I_1(s)\frac{1/sC_f}{sL_2 + \frac{1}{sC_f}} \tag{B-2}$$

It follows that

$$I_1(s) = I_2(s)\cdot\left(s^2 L_2 C_f + 1\right) \tag{B-3}$$

Then the transfer function becomes

$$\frac{I_2(s)}{U(s)} = \frac{1/C_f L_1 L_2}{s\left(s^2 + \frac{L_1 + L_2}{L_1 L_2 C_f}\right)} \tag{B-4}$$

The resonant frequency is then:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{B-5}$$

The filter parameters are chosen such that the following conditions are satisfied [23], [71]:

- Neglecting the filter resistances, the voltage drop across the inductances should be limited to 10% during nominal operation, which agrees with the previous design criteria for L-filter;
- The grid side inductance is a fraction of the converter side inductance, since the latter is responsible for the attenuation of most of the switching ripple;
- The capacitive value is limited by the decrease of the power factor at rated power in case of idle operation of the VSC (it will be considered as less or equal 10%);
- The resonance frequency is in the range between ten times the fundamental frequency and one half the switching frequency;
- The IEC 1000-3-4 regulation states that current harmonics above 33rd should be less than 0.6% of the nominal current;
- The resistances are taken as 10% of the value of the corresponding inductances.

According to these conditions the following equations can be used

$$L_1 + L_2 = 0.1 \text{ p.u.} \tag{B-6}$$

$$L_2 = r \cdot L_1 \tag{B-7}$$

where r is the ratio between the inductance on the grid side to the inductance on the converter side, which is less than 1.

$$C_f \leq 0.1 \quad \text{p.u.} \tag{B-8}$$

$$500 \text{ Hz} < f_{res} < 1250 \text{ Hz} \quad \text{(for sampling frequency of 5kHz)} \tag{B-9}$$

From (B-4), the gain of the system at the h harmonic is expressed as

$$\left|G(jh\omega)\right| = \frac{1/C_f L_1 L_2}{\left| jh\omega\left((jh\omega)^2 + \frac{L_1 + L_2}{L_1 L_2 C_f} \right) \right|} \leq 0.006 \text{ .} \tag{B-10}$$

Equations (B-9) and (B-10) are used as check up conditions. Using a capacitance value of 0.05 p.u., (B-9) is not satisfied for different inductance ratios (r), as shown in Fig. B.1. Increasing the capacitance value to 0.1 p.u.,

a value of r = 0.4 has been chosen to satisfy all conditions (see Fig. B.2 and Fig. B.3). The LCL-filter parameters are then calculated as reported in Appendix C.

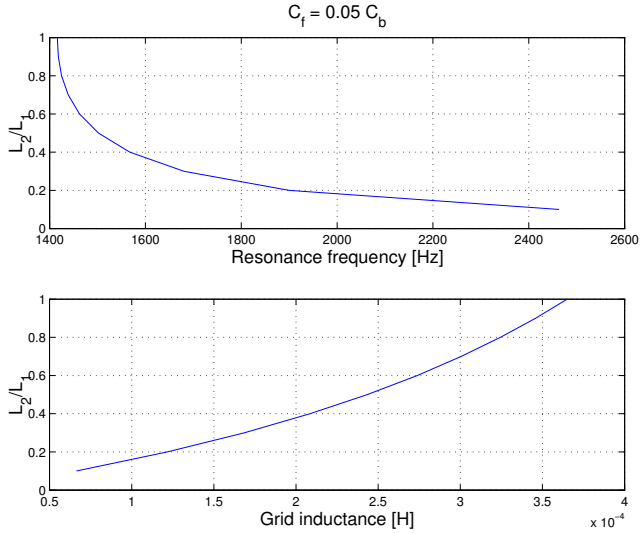

Fig. B.1 Relation between *r*, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 5% of the base value.

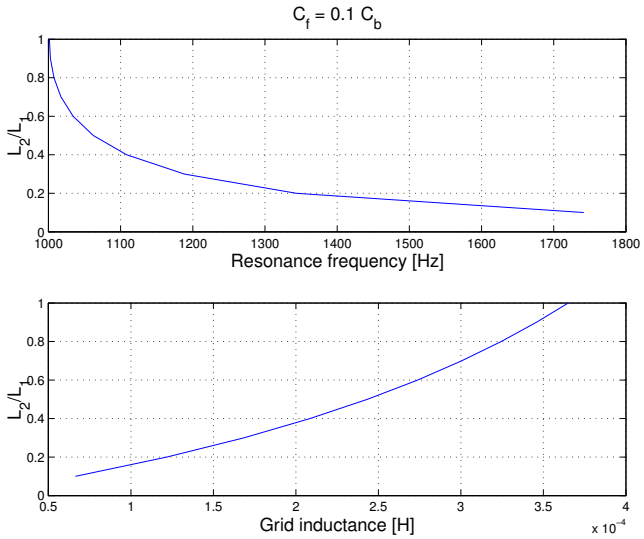

Fig. B.2 Relation between r, which is described in (B-7), and the resonance frequency (upper), and the grid inductance (lower) for a filter capacitance of 10% of the base value.

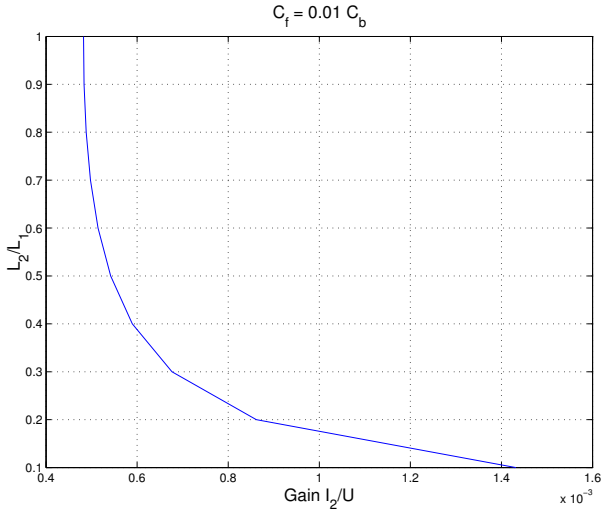

Fig. B.3 Relation between *r* and the gain filter I_2/U.

Appendix C
Power system parameters

C.1 Per-unit base values

The base values for the AC voltage and current are

$$E_{\text{base}} = 400 \text{ V} \tag{C-1}$$

$$I_{\text{base}} = 100 \text{ A} \tag{C-2}$$

The base value of the impedance is then obtained according to

$$Z_{\text{base}} = \frac{E_{\text{base}}}{\sqrt{3} I_{\text{base}}} = 2.3\Omega \tag{C-3}$$

The base values for the DC-link voltage and current are equal to

$$U_{\text{DC,base}} = 650 \text{ V} \tag{C-4}$$

$$I_{\text{DC,base}} = \frac{\sqrt{3} E_{\text{base}} I_{\text{base}}}{U_{\text{DC,base}}} = 107\text{A} \tag{C-5}$$

C.2 L-filter system data

Table C-1 System data with L-filter.

Description	Symbol	Value
Nominal RMS phase-to-phase AC voltage	E	400 V
Nominal RMS phase current	I_{n}	100 A
Nominal grid frequency	f_{n}	50 Hz
Nominal DC link voltage	U_{dc}	650 V
Nominal DC input current	I_{dc}	107 A
Filter resistance	R	23 mΩ
Filter inductance	L	0.73 mH
DC-link capacitance	C	550 µF
DC-chopper damping resistance	R_{d}	10 Ω

C.3 LCL-filter parameters

Table C-2 LCL-Filter parameters.

Parameter	p.u.	Actual
L_1	0.071	0.52 mH
R_1	0.1 L_1	1.6 mΩ
L_2	0.027	0.2 mH
R_2	0.1 L_2	0.6 mΩ
C_f	0.1	137.8 μF

C.4 Weak grid parameters

Table C-3 Weak network parameters.

Parameter	Value
V_s	400 V
R_s	3x0.05 Ω
L_s	3x2.05 mH
C_s	3x46 μF

Appendix D
Controller parameters

D.1 Parameters for VCC for L-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Dead beat gain	k_p	3.7
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.5

D.2 Parameters for VCC for LCL-filter system

Table D-2 VCC for L-filter parameters.

Description	Symbol	Value
Sampling frequency	f_s	5 kHz
Sampling time	T_s	200 μs
Outer controller gain	k_{p1} (0.7 k_{p2})	0.546
Second controller gain	k_{p2} (0.3 k_{p3})	0.78
Inner controller gain	k_{p3}	2.6
Integral time	T_i	0.03 s
Smith predictor gain	k_{ps}	0.07

D.3 Parameters for DC-link voltage regulator

Table D-3 DC-link voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pdc}	0.4
Integral time	T_{idc}	0.04 s

D.4 Parameters for PCC-voltage regulator

Table D-4 PCC-voltage regulator parameters.

Description	Symbol	Value
Proportional gain	k_{pr}	0.5
Integral time	T_{ir}	0.05 s

Appendix E
LCL-filter current reference-generation

The power at the grid side S_2 is expressed as

$$S_2 = S_{\mathrm{ac},2} + S_{\mathrm{s}2,2} + S_{\mathrm{c}2,2} \tag{E-1}$$

where S_{ac} is the power at the fundamental frequency, $S_{\mathrm{s}2}$ and $S_{\mathrm{c}2}$ are sine and cosine components of the power at double the fundamental frequency, which are called the oscillating powers. The power is calculated in *dqp*- and *dqn*-frames as follows

$$S_2 = \left(e^{\mathrm{j}\omega t}\underline{e}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{e}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{2\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-2}$$

Expanding this equation leads to

$$\begin{aligned} S_{\mathrm{s}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{qn}} - e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dn}}i_{2\mathrm{qp}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dp}}i_{2\mathrm{dn}} - e_{\mathrm{qn}}i_{2\mathrm{qp}} - e_{\mathrm{dn}}i_{2\mathrm{dp}}\right) \end{aligned} \tag{E-3}$$

$$\begin{aligned} S_{\mathrm{c}2,2} = {} & e_{\mathrm{dp}}i_{2\mathrm{dn}} + e_{\mathrm{qp}}i_{2\mathrm{qn}} + e_{\mathrm{dn}}i_{2\mathrm{dp}} + e_{\mathrm{qn}}i_{2\mathrm{qp}} \\ & + \mathrm{j}\left(e_{\mathrm{qp}}i_{2\mathrm{dn}} - e_{\mathrm{dp}}i_{2\mathrm{qn}} + e_{\mathrm{qn}}i_{2\mathrm{dp}} - e_{\mathrm{dn}}i_{2\mathrm{qp}}\right) \end{aligned} \tag{E-4}$$

The power at the converter side S_1 is expressed in the same manner and same designations as

$$S_1 = S_{\mathrm{ac},1} + S_{\mathrm{s}2,1} + S_{\mathrm{c}2,1} \tag{E-5}$$

It is calculated in *dqp*- and *dqn*- frames as follows:

$$S_1 = \left(e^{\mathrm{j}\omega t}\underline{u}_{\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{u}_{\mathrm{dqn}}\right)\left(e^{\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqp}} + e^{-\mathrm{j}\omega t}\underline{i}_{1\mathrm{dqn}}\right)^{\mathrm{conj}} \tag{E-6}$$

Expanding this equation results in the following:

$$\begin{aligned} S_{\mathrm{ac},1} &= u_{\mathrm{dp}} i_{\mathrm{1dp}} + u_{\mathrm{qp}} i_{\mathrm{1qp}} + u_{\mathrm{dn}} i_{\mathrm{1dn}} + u_{\mathrm{qn}} i_{\mathrm{1qn}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dp}} - u_{\mathrm{dp}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qn}}\right) \end{aligned} \tag{E-7}$$

$$\begin{aligned} S_{\mathrm{s}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1qn}} - u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dn}} i_{\mathrm{1qp}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dp}} i_{\mathrm{1dn}} - u_{\mathrm{qn}} i_{\mathrm{1qp}} - u_{\mathrm{dn}} i_{\mathrm{1dp}}\right) \end{aligned} \tag{E-8}$$

$$\begin{aligned} S_{\mathrm{c}2,1} &= u_{\mathrm{dp}} i_{\mathrm{1dn}} + u_{\mathrm{qp}} i_{\mathrm{1qn}} + u_{\mathrm{dn}} i_{\mathrm{1dp}} + u_{\mathrm{qn}} i_{\mathrm{1qp}} \\ &\quad + \mathrm{j}\left(u_{\mathrm{qp}} i_{\mathrm{1dn}} - u_{\mathrm{dp}} i_{\mathrm{1qn}} + u_{\mathrm{qn}} i_{\mathrm{1dp}} - u_{\mathrm{dn}} i_{\mathrm{1qp}}\right) \end{aligned} \tag{E-9}$$

Applying KVL to the outer loop of the LCL-filter

$$\underline{u}_{\mathrm{dqp}} = \underline{e}_{\mathrm{dqp}} + R_1 \underline{i}_{\mathrm{1dqp}} + \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqp}} + R_2 \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqp}} \tag{E-10}$$

$$\underline{u}_{\mathrm{dqn}} = \underline{e}_{\mathrm{dqn}} + R_1 \underline{i}_{\mathrm{1dqn}} - \mathrm{j}\omega L_1 \underline{i}_{\mathrm{1dqn}} + R_2 \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega L_2 \underline{i}_{\mathrm{2dqn}} \tag{E-11}$$

Applying KCL at the filter capacitor connection node

$$\underline{i}_{\mathrm{1dqp}} = \underline{i}_{\mathrm{2dqp}} + \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqp}} \tag{E-12}$$

$$\underline{i}_{\mathrm{1dqn}} = \underline{i}_{\mathrm{2dqn}} - \mathrm{j}\omega C_{\mathrm{f}}\, \underline{u}_{\mathrm{cdqn}} \tag{E-13}$$

Substituting (E-10) to (E-13) in (E-7), the active power at the converter side will be

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}}\left(i_{\mathrm{2dp}} - Y_{\mathrm{c}} u_{\mathrm{cqp}}\right) + i_{\mathrm{1dp}}\left(R_1 i_{\mathrm{1dp}} - \omega L_1 i_{\mathrm{1qp}} + R_2 i_{\mathrm{2dp}} - \omega L_2 i_{\mathrm{2qp}}\right) \\ & + e_{\mathrm{qp}}\left(i_{\mathrm{2qp}} + Y_{\mathrm{c}} u_{\mathrm{cdp}}\right) + i_{\mathrm{1qp}}\left(R_1 i_{\mathrm{1qp}} + \omega L_1 i_{\mathrm{1dp}} + R_2 i_{\mathrm{2qp}} + \omega L_2 i_{\mathrm{2dp}}\right) \\ & + e_{\mathrm{dn}}\left(i_{\mathrm{2dn}} + Y_{\mathrm{c}} u_{\mathrm{cqn}}\right) + i_{\mathrm{1dn}}\left(R_1 i_{\mathrm{1dn}} + \omega L_1 i_{\mathrm{1qn}} + R_2 i_{\mathrm{2dn}} + \omega L_2 i_{\mathrm{2qn}}\right) \\ & + e_{\mathrm{qn}}\left(i_{\mathrm{2qn}} - Y_{\mathrm{c}} u_{\mathrm{cdn}}\right) + i_{\mathrm{1qn}}\left(R_1 i_{\mathrm{1qn}} - \omega L_1 i_{\mathrm{1dn}} + R_2 i_{\mathrm{2qn}} - \omega L_2 i_{\mathrm{2dn}}\right) \end{aligned} \tag{E-14}$$

where $Y_{\mathrm{c}} = \omega C_{\mathrm{f}}$. This reduces to

$$\begin{aligned} P_{\mathrm{ac},1} = {} & e_{\mathrm{dp}} i_{\mathrm{2dp}} + e_{\mathrm{qp}} i_{\mathrm{2qp}} + e_{\mathrm{dn}} i_{\mathrm{2dn}} + e_{\mathrm{qn}} i_{\mathrm{2qn}} \\ & + R_1\left(i_{\mathrm{1dp}}^2 + i_{\mathrm{1qp}}^2 + i_{\mathrm{1dn}}^2 + i_{\mathrm{1qn}}^2\right) \\ & + R_2\left(i_{\mathrm{2dp}} i_{\mathrm{1dp}} + i_{\mathrm{2qp}} i_{\mathrm{1qp}} + i_{\mathrm{2dn}} i_{\mathrm{1dn}} + i_{\mathrm{2qn}} i_{\mathrm{1qn}}\right) \\ & + \omega L_2\left(-i_{\mathrm{2qp}} i_{\mathrm{1dp}} + i_{\mathrm{2dp}} i_{\mathrm{1qp}} + i_{\mathrm{2qn}} i_{\mathrm{1dn}} - i_{\mathrm{2dn}} i_{\mathrm{1qn}}\right) \\ & + Y_{\mathrm{c}}\left(-u_{\mathrm{cqp}} e_{\mathrm{dp}} + u_{\mathrm{cdp}} e_{\mathrm{qp}} + u_{\mathrm{cqn}} e_{\mathrm{dn}} - u_{\mathrm{cdn}} e_{\mathrm{qn}}\right) \end{aligned} \tag{E-15}$$

which can be separated into three different parts as follows

$$P_{\mathrm{ac},1} = P_{\mathrm{ac},2} + \Delta P(i) + \Delta P(e) \tag{E-16}$$

where $\Delta P(i)$ is the active power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta P(e)$ is the active power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

In the same way, the reactive power at the converter side is calculated as

$$\begin{aligned} Q_{\mathrm{ac},1} = {} & e_{\mathrm{qp}} i_{2\mathrm{dp}} - e_{\mathrm{dp}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qn}} \\ & + \omega L_1 \left(i_{1\mathrm{dp}}^2 + i_{1\mathrm{qp}}^2 - i_{1\mathrm{dn}}^2 - i_{1\mathrm{qn}}^2 \right) \\ & + R_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{dp}} - i_{2\mathrm{dp}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qn}} \right) \\ & + \omega L_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{dp}} + i_{2\mathrm{qp}} i_{1\mathrm{qp}} - i_{2\mathrm{dn}} i_{1\mathrm{dn}} - i_{2\mathrm{qn}} i_{1\mathrm{qn}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cqp}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dp}} + u_{\mathrm{cqn}} e_{\mathrm{qn}} + u_{\mathrm{cdn}} e_{\mathrm{dn}} \right) \end{aligned} \tag{E-17}$$

which can be separated into three different parts, as follows

$$Q_{\mathrm{ac},1} = Q_{\mathrm{ac},2} + \Delta Q(i) + \Delta Q(e) \tag{E-18}$$

where $\Delta Q(i)$ is the reactive power consumed by filter inductors as a function in the grid-side current and the converter-side current, and $\Delta Q(e)$ is the reactive power consumed by filter inductors as a function in the grid voltage and the capacitor voltage.

The sine and cosine components of the active oscillating power are derived as

$$\begin{aligned} P_{\mathrm{s}2,1} = {} & e_{\mathrm{dp}} i_{2\mathrm{qn}} - e_{\mathrm{qp}} i_{2\mathrm{dn}} - e_{\mathrm{dn}} i_{2\mathrm{qp}} + e_{\mathrm{qn}} i_{2\mathrm{dp}} \\ & + 2R_1 \left(i_{1\mathrm{dp}} i_{1\mathrm{qn}} - i_{1\mathrm{qp}} i_{1\mathrm{dn}} \right) \\ & - 2\omega L_1 \left(i_{1\mathrm{qp}} i_{1\mathrm{qn}} + i_{1\mathrm{dp}} i_{1\mathrm{dn}} \right) \\ & + R_2 \left(i_{2\mathrm{dp}} i_{1\mathrm{qn}} - i_{2\mathrm{qp}} i_{1\mathrm{dn}} - i_{2\mathrm{dn}} i_{1\mathrm{qp}} + i_{2\mathrm{qn}} i_{1\mathrm{dp}} \right) \\ & - \omega L_2 \left(i_{2\mathrm{qp}} i_{1\mathrm{qn}} + i_{2\mathrm{dp}} i_{1\mathrm{dn}} + i_{2\mathrm{qn}} i_{1\mathrm{qp}} + i_{2\mathrm{dn}} i_{1\mathrm{dp}} \right) \\ & + Y_{\mathrm{c}} \left(-u_{\mathrm{cdn}} e_{\mathrm{dp}} - u_{\mathrm{cqn}} e_{\mathrm{qp}} - u_{\mathrm{cdp}} e_{\mathrm{dn}} - u_{\mathrm{cqp}} e_{\mathrm{qn}} \right) \end{aligned} \tag{E-19}$$

$$P_{s2,1} = P_{s2,2} + \Delta P_{s2}(i) + \Delta P_{s2}(e) \tag{E-20}$$

$$\begin{aligned} P_{c2,1} = {} & e_{dp} i_{2dn} + e_{qp} i_{2qn} + e_{dn} i_{2dp} + e_{qn} i_{2qp} \\ & + 2R_1 \left(i_{1dp} i_{1dn} + i_{1qp} i_{1qn} \right) \\ & + 2\omega L_1 \left(i_{1dp} i_{1qn} - i_{1dn} i_{1qp} \right) \\ & + R_2 \left(i_{2dp} i_{1dn} + i_{2qp} i_{1qn} + i_{2dn} i_{1dp} + i_{2qn} i_{1qp} \right) \\ & + \omega L_2 \left(-i_{2qp} i_{1dn} + i_{2dp} i_{1qn} + i_{2qn} i_{1dp} - i_{2dn} i_{1qp} \right) \\ & + Y_c \left(u_{cqn} e_{dp} - u_{cdn} e_{qp} - u_{cqp} e_{dn} + u_{cdp} e_{qn} \right) \end{aligned} \tag{E-21}$$

$$P_{c2,1} = P_{c2,2} + \Delta P_{c2}(i) + \Delta P_{c2}(e) \tag{E-22}$$

Expressing (E-15) to (E-21) in matrix form will result in

$$\begin{aligned} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} = {} & \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \begin{bmatrix} i_{2dp} \\ i_{2qp} \\ i_{2dn} \\ i_{2qn} \end{bmatrix} \\ & + \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \end{aligned} \tag{E-23}$$

The current references are then calculated using the following matrix

$$\begin{bmatrix} i_{2dp}^* \\ i_{2qp}^* \\ i_{2dn}^* \\ i_{2qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} - Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \tag{E-24}$$

The oscillating power, which is consumed by the filter inductors, is compensated by the power flow from the VSC side. Hence

$$P_{s2,1} = \Delta P_{s2}(i) \tag{E-25}$$

$$P_{c2,1} = \Delta P_{c2}(i) \tag{E-26}$$

Moreover, the active power at the VSC side is assumed to be equal to the power at the DC side of the converter.

$$P_{ac,1} = u_{dc}^{*} i_{v}^{*} \tag{E-27}$$

To achieve zero reactive power at the grid, $Q_{ac,1}$ should supply the reactive power consumed by the filter. Hence

$$Q_{ac,1} = \Delta Q(i) + \Delta Q_{c} \tag{E-28}$$

where ΔQ_{c} is the power loss in the filter capacitor, which is calculated as

$$\Delta Q_{c} = \omega C_{f} \left(u_{cdp}^{2} + u_{cqp}^{2} + u_{cdn}^{2} + u_{cqn}^{2} \right) \tag{E-29}$$

Paper A

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Paper B

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Paper C

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Paper E

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Paper G

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