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Radar and communication signal processing algorithm and implementation using OFDM based waveform

Master's thesis in Embedded Electronic System Design

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CHALMERS UNIVERSITY OF TECHNOLOGY
UNIVERSITY OF GOTHENBURG
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MASTER'S THESIS 2018

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Abstract

With the development of radar systems, a platform that can support high estimation accuracy and multiple target tracking is required. OFDM is widely used in communication engineering due to the high spectrum efficiency. In this thesis, an algorithm of OFDM estimation method is developed based on the "RadCom" concept with data transmission and radar sensor. The algorithm is verified in hardware with 80 GHz carrier frequency. A novel approach on fractional step length estimation is demonstrated and tested for the improvement of radar estimation accuracy, improving the resolution for single target estimation beyond what is possible with the traditional integer step length method. Beside the OFDM-based "RadCom" system, this thesis presents a single-carrier radar system, which is developed using the tool suite DSP Builder and verified on an Arria V FPGA board.

Keywords: OFDM, RadCom, radar, resolution, FPGA, DSP builder

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Contents

1

Introduction

Radar has been widely used in a number of areas including automobile, production automation, quality monitoring, etc. Traditional frequency-modulated continuous-wave (FMCW) radar is widely used due to its structure simplicity. However, when several radars are installed in close proximity to each other, there is a chance they would interference with each other. Orthogonal frequency-division multiplexing (OFDM) technology is well-known used in multi-user systems such as Wi-Fi and cellular networks. Since one of the properties of OFDM technology is each sub carrier is orthogonal, adopting OFDM concept into radar will not only eliminate unwanted multi-user interference, but also support a system which has both radar and communication functionalities. Such system is referred to as "RadCom" [1]. To realize "RadCom" digital signal processing, algorithms need to be investigated considering practical implementations. In this thesis work, algorithms specifically for "RadCom" OFDM will be studied.

Doppler frequency shift happens when a target is moving relative to the observer. This frequency shift can be used to estimate relative radial velocity in radar processing. Furthermore, the radar should have the ability to estimate the ranges and velocities of multiple targets independently and simultaneously. To determine the direction of the target is also an important task of a radar system. A technique combined with multiple-input-multiple-output (MIMO) and digital beam-forming (DBF) in communication and radar processing areas is supposed to achieve high performance azimuth position estimation [2].

Estimation accuracy translates to the resulting range resolution in a radar system. For radars with modulated signals, the accuracy is determined by the bandwidth. The wider the bandwidth of transmitted signal is, the higher resolution will be achieved. In [3], the authors used multiple signal characterization (MUSIC) algorithm to offer high spectral resolution in traditional FMCW radar. Considering a "RadCom" system, the signal should have a suitable bandwidth that provides high performance in terms of bit error rate (BER) and signal to noise ratio (SNR). But minimum bandwidth limitation for a radar processing should be considered as well.

1.1 Motivation

There are several benefits of OFDM, such as high tolerance of Doppler frequency shifting, simultaneous information transmission and high flexibility in system design. Compared to the correlation estimation method the drawback of baseband signal processing can be solved by applying OFDM technique, which is discussed in [4] [5]. As for multiple targets estimation, OFDM radar processing provides good performance. Algorithms of range and Doppler measurements for multiple targets are developed in [6]. Carrier wave is one concern of OFDM. The performance of OFDM radar system in 6 GHz and 24 GHz carrier frequencies is discussed in [7]. Higher carrier frequency has its benefit in saving hardware and improving range resolution. The performance in 73.5 to 83.5 GHz should be explored in this report. Another approach of OFDM radar estimation is Maximum Likelihood (ML) estimation, which is

presented in [8]. All the parameters in OFDM should be modified to accommodate radar application. In [9], the authors have discussed parameters applied in vehicle to vehicle "RadCom" system. Considering range resolution, meter-level radar system has been researched in [1]. To improve range resolution to millimeter or, even more challenging, to micrometer is a problem that needs to be addressed.

1.2 Applications

In terms of intelligent transportation system, an effective communication system is necessary in vehicle-to-vehicle communication on the condition that several transceiver partners are on the road. It is not enough to support autonomous driving techniques since the surroundings could affect the vehicle movement. In the joint "RadCom" system, radar sensor and communication system would share information to each other to increase the detection accuracy and efficiency. While the communication system plays the role as "ears" and "mouth", the radar sensor, as the "eyes", observes the surroundings. With a suitable joint platform, this system can be used to handle most cases on the road.

Another application of radar sensing is in micro-motion estimation. Resolutions of a radar system determine the accuracy of estimations. In [10], the authors provided a novel solution using a high-resolution range profile (HRRP)-based method. As for an OFDM radar system, detection accuracy can be improved by average calculation of each sub carrier. However, in the sample based algorithm, resolutions are limited by integer samples. To achieve a high resolution OFDM radar system, fractional parts should be involved to make the estimation more accurate.

1.3 Goals

There are two final aims in this thesis work. The first one is to develop and evaluate an OFDM based "RadCom" system to detect range and velocity of targets. The algorithm will be tested by a radio frequency (RF) setup including oscilloscope and arbitrary waveform generator (AWG). The system is supposed to have compatibility for different applications such as automotive radar and thickness measurement. The second goal is to build the radar transceiver model and verify it on hardware. Simulink with Intel DSP builder will be used to build the system model and field programmable gate array (FPGA) will be used as hardware platform for implementation and verification. In this thesis work, an Altera Arria V generation FPGA board [11] and THDB-ADA-HSMC card [12][13] with the functions of analog to digital convention and digital to analog convention will be used to test range with a narrow bandwidth.

1.4 Thesis outline

To read this thesis work report, the readers are supposed to have some basic knowledge of radar sensor and communication system. Chapter 2 gives a background of "RadCom" related techniques. Furthermore, this chapters introduces the OFDM algorithm development, including the novel estimation algorithm and presents some simulation results of channel estimation and multiple targets. In chapter 3, system setup and FPGA implementation will be discussed. Model based radar transceiver design will be shown and verified in Simulink platform. Implementation based on FPGA will be completed with hardware dynamic feedback. In chapter 4, the measurement of OFDM radar system will be focused on. The evaluation will be carried out on a static target to improve distance estimation resolution with 80GHz setup. Our findings and some remaining issues will be discussed in the conclusion in chapter 5.

2

OFDM Radar Signal Processing

To realize a “RadCom” system, the radar estimation and communication systems should be developed as the basic functionality modules. In this chapter, we will discuss the theory of target detection and range and velocity estimation with OFDM technique. Three stages are used to illustrate this theory, which are OFDM signal construction, OFDM signal transmission and OFDM signal radar estimation. To begin with, the OFDM signal construction is discussed briefly with showing the time domain and frequency domain matrix concept. In the transmission part, the signal operation in transceiver including modulation and demodulation is shown as a flow diagram. At last, the estimation theory is explained in detail with basic channel influence and the mathematic demonstration. In the last section of this part, a novel demodulation algorithm is provided to get higher estimation accuracy.

With the understanding of OFDM radar estimation method, the algorithm development is introduced in the next step. Simulation result of OFDM radar algorithm can be found in the last section of this chapter. The simulation starts with channel response in communication and ends with multiple target estimation.

2.1 OFDM signal construction

OFDM modulation is widely used in the communication area due to the orthogonal property. Figure 2.1 shows the spectrum of OFDM signal with 4 sub carriers. *Sinc(x)* function in frequency domain stands for an OFDM sub carrier. In the max amplitude of each sub carrier, the other sub carrier’s amplitude is 0, which means that the sub carriers don’t affect each other.

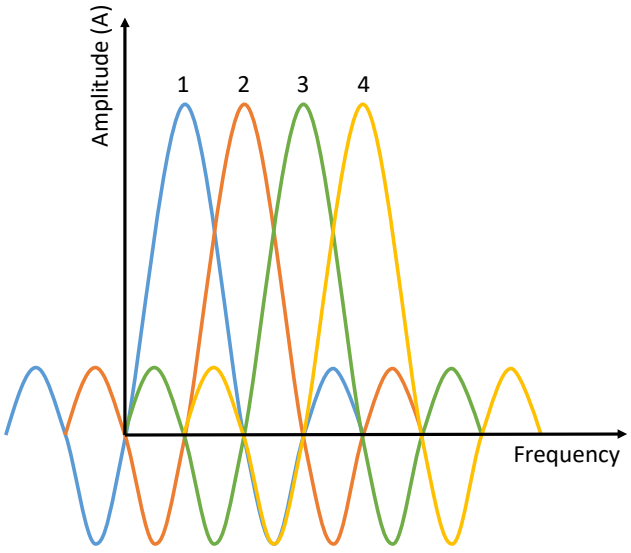


Figure 2.1. Spectrum of OFDM

An OFDM signal is generated in two dimensions. The sub carriers are generate along the frequency domain, while along the time domain, there are OFDM symbols with a duration time which is equal to the reciprocal of sub carrier frequency interval. An illustrative diagram of the OFDM signal's properties is shown in figure 2.2.

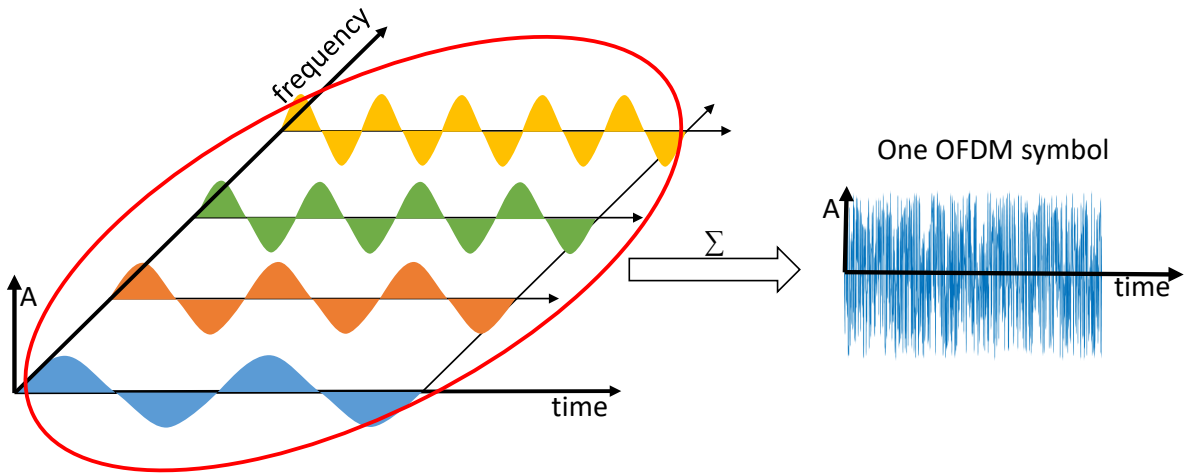


Figure 2.2. OFDM signal construction

2.2 OFDM transmission

In the OFDM transmission, as shown in figure 2.3, the first step is to generate modulated symbols. After inverse discrete Fourier transform (IDFT) to each symbol, a cyclic prefix is added for each OFDM symbol to avoid inter symbol interference (ISI). Then the matrix is changed to serial signal for the transmission. In the receiver part, the signal is changed back to parallel. After removing cyclic prefix, discrete Fourier transform (DFT) is calculated for each OFDM symbol.

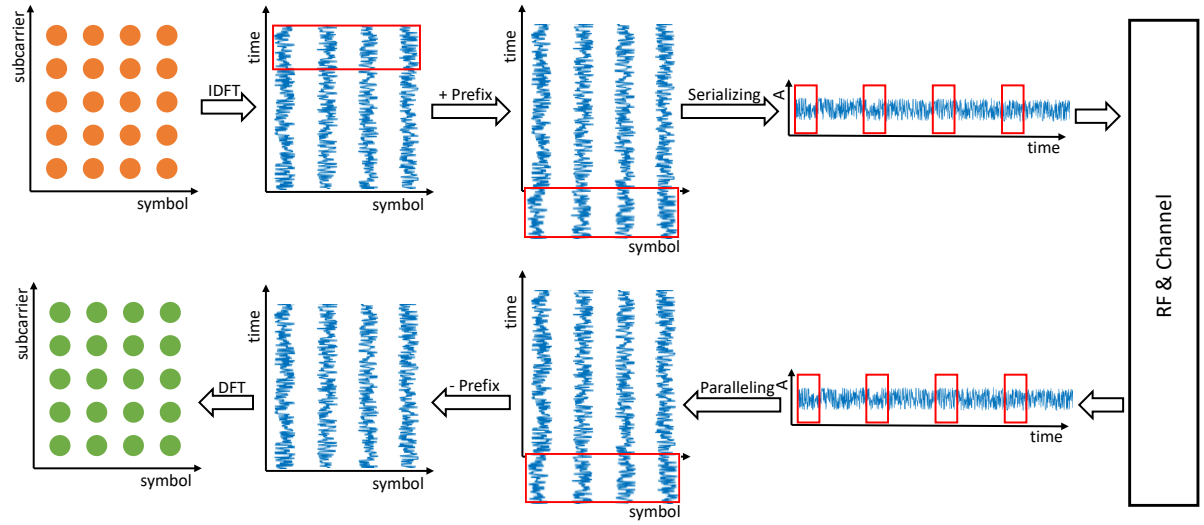


Figure 2.3. OFDM transmission

2.3 OFDM radar estimation

2.3.1 Synchronization based on cross-correlation method

The time delay caused by propagation from the radar platform to the target object is shown below

$$t_d = \frac{2 * R}{c_o}$$

In practice, it is hard to use this equation to estimate range due to the small sampling time offset that cannot be avoided.

The similarity of transmitted and received signals can be calculated by cross-correlation method. The diagram of it is shown in figure 2.4. By this calculation, a coherent peak will show up. By knowing the position of coherent peak, time delay t_d can be calculated.

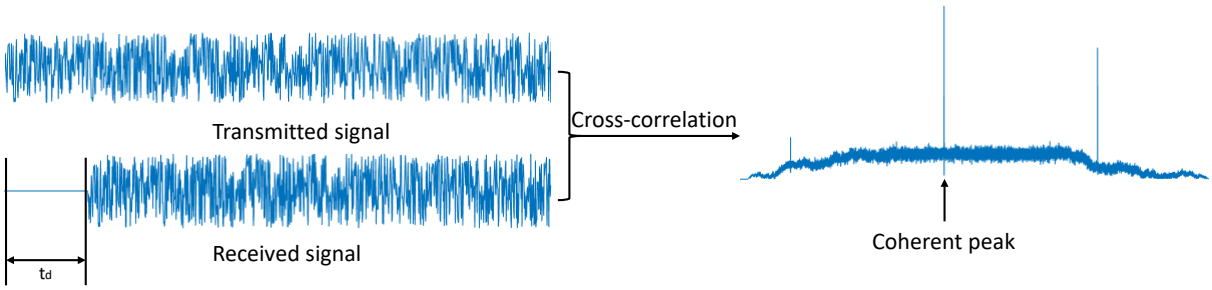


Figure 2.4. Diagram illustration for Cross-correlation method

When the time delay is figured out, the estimated distance can be induced straightforwardly by

$$d = \left(\frac{t_d}{f_s}\right) * c_o$$

In the equation, c_o stands for the speed of light. This estimation has the only variable index which is sampling frequency (f_s). It means that the higher sampling frequency is, the better distance resolution could be.

There is a drawback in cross-correlation estimation method. If there are several targets that needed to be detected and estimated, this method cannot work due to the received signals will be overlaid according to their different time delay.

2.3.2 Radial velocity and range detection

According to Doppler theory, frequency shift is expected between radar platform and reflecting objects. If the relative velocity is v_{rel}, the Doppler frequency shift f_D is

$$f_{D,comm} = \frac{v_{rel}}{\lambda} = \frac{v_{rel} * f_c}{c_o}$$

In this equation, λ is the wavelength and f_c is the carrier frequency. In the radar process, Doppler frequency shifting is doubled caused by two-way propagation

$$f_{D,radar} = \frac{2 * v_{rel}}{\lambda} = \frac{2 * v_{rel} * f_c}{c_o}$$

To detect radial velocity, the Doppler frequency shift should be observed from receiver. However, this frequency is very small compared to signal carrier frequency. So, to calculate the phase shifting caused by Doppler frequency could be a better solution to estimate radial velocity.

2.3.3 Estimation theory of OFDM radar processing

Instead of dealing with baseband signals, the OFDM radar technique provides a solution in operating two-dimensional modulation symbols. The general estimation idea of OFDM is shown in figure 2.5. The variable *S* stands for modulated symbols. Each column represents one OFDM symbol while each row represents one sub carrier. In the demodulation, for each row, IDFT is calculated to estimate the range, and in each column, DFT is calculated for the velocity estimation. The following part of this section will illustrate OFDM estimation theory in detail.

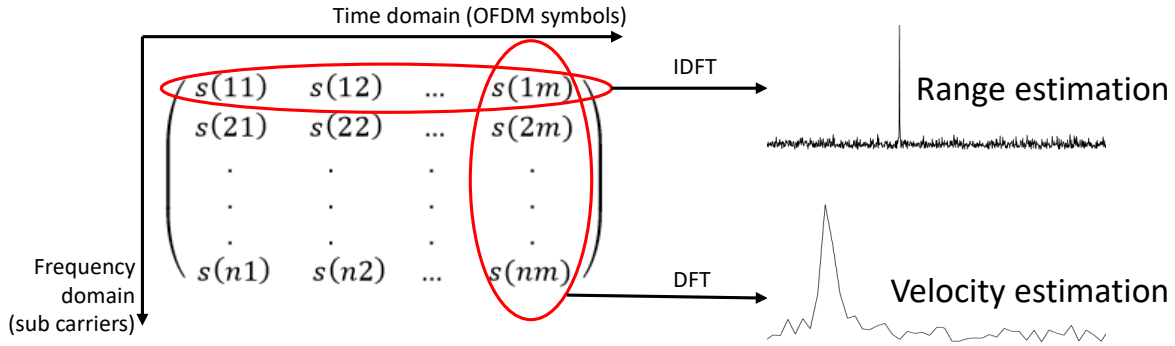


Figure 2.5. Diagram illustration for OFDM method

Time delay transfers into frequency domain as phase offset, while frequency offset transfers into time domain as phase shift according to Fourier theory. It means that to get correct estimation of range and velocity, only the phase information is needed. Therefore, as shown in figure 2.6, the first step of OFDM radar processing is to remove the information of transmitted signal in the received signal. With this division, only the phase information is left in the symbols.

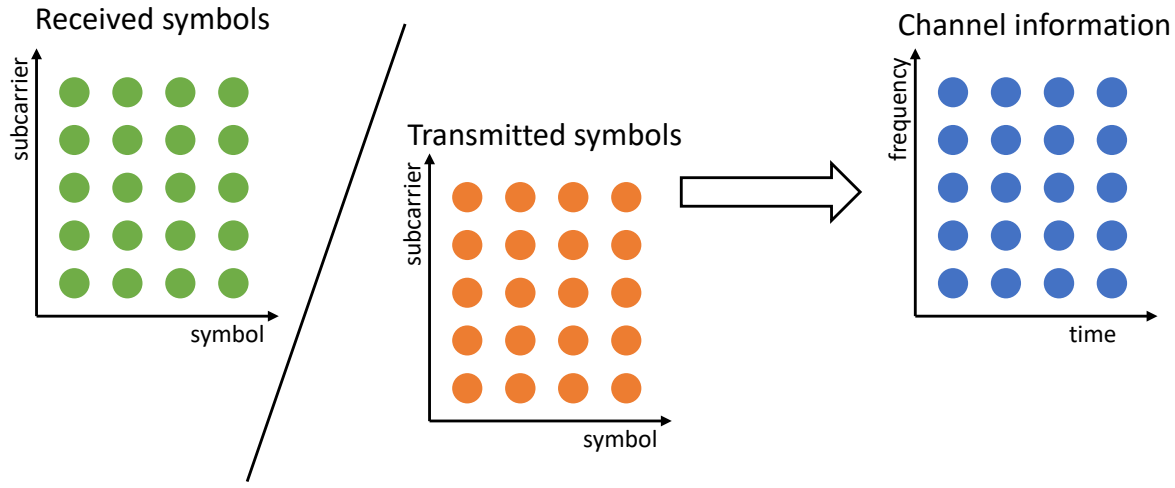


Figure 2.6. Division between received and transmitted symbols

This method mainly follows the algorithm introduced by [5]. After the division, the channel information is received, and can be described in a matrix as below.

$$D = \begin{pmatrix} d(1) & d(N_c+1) & \dots & d\big((N_{sym}-1)*N_c+1\big) \\ d(2) & d(N_c+2) & \dots & d\big((N_{sym}-1)*N_c+2\big) \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ d(N_c) & d(2N_c) & \dots & d\big(N_{sym}N_c\big) \end{pmatrix}$$

N_c represents the number of sub carriers and N_{sym} represents the number of symbols in each sub carrier. To be clearer, along the column, we can regard the symbols in frequency domain while along the row, symbols are in the time domain.

Since the range and the velocity are estimated from phase shift caused by time delay and Doppler frequency, other information in the receiver side is useless. So, the first step is to remove transmitted information from receiver, then the information left just has the components of attenuation and phase shift. The signal can be represented as $\vec{k}_R(n) * \vec{k}_D(m)$, $n = 1, \dots, N_c$ and $m = 1, \dots, N_{sym}$. The * stands for elements multiplication in vector. In the equations below, parameter R stands for range while v_{rel} stands for relative velocity.

$$\vec{k}_R(n) = \exp(-j2\pi n f_{spa}\frac{2R}{c_o})$$

$$\vec{k}_D(m) = \exp(-j2\pi m\frac{2v_{rel}f_c}{f_{spa}c_o})$$

Frequency spacing is represented by f_{spa}, which is the frequency between each sub carrier.

To estimate the range, we compute IDFT for each column. In one OFDM symbol, frequency offset caused by time delay is different, due to different frequencies in every sub carriers. Since other information is removed from receiver, the time delay corresponds to an impulse in the time domain. Equation below shows mathematical proof of it.

$$\begin{aligned} \mathrm{r}(k) = IDFT[k_R(n)] &= \frac{1}{N_c}\sum_{n=1}^{N_c}\exp\left(-j2\pi n f_{spa}\frac{2R}{c_o}\right)\exp\left(j\frac{2\pi}{N_c}nk\right) \\ &= \frac{1}{N_c}\sum_{n=1}^{N_c}\exp\left(j2\pi\left(\frac{n}{N_c}k - nf_{spa}\frac{2R}{c_o}\right)\right) \end{aligned}$$

In this equation, two exponential components cancel each other under the condition

$$k = \frac{2Rf_{spa}N_c}{c_o}, \qquad (k = 0, \dots, N_c - 1)$$

It means that at this certain point in the time response, a peak will occur.

To estimate the radial velocity, the approach is similar to range estimation. We calculate DFT for each row, then the frequency shifting is represented as a peak in the Fourier domain.

$$\mathrm{v}(l) = DFT[k_D(m)] = \sum_{m=1}^{N_{sym}} \exp\left(j2\pi m \frac{2v_{rel}f_c}{f_{spa}c_o}\right) \exp\left(-j\frac{2\pi}{N_{sym}} ml\right)$$
$$= \sum_{m=1}^{N_{sym}} \exp\left(j2\pi\left(m\frac{2v_{rel}f_c}{f_{spa}c_o} - \frac{m}{N_{sym}}l\right)\right)$$

Cancellation happens under the condition

$$l = \frac{2v_{rel}f_cN_{sym}}{f_{spa}c_o}, \qquad (l = 0, \ldots, N_{sym} - 1)$$

2.3.4 High resolution demodulation solution

As shown in figure 2.7, the range estimation is based on the cancelation after IDFT operation. The resolution in this case depends on index *k*. Since IDFT is a sample based calculation, index *k* should be integer, which sets a limitation on estimation resolution. The practical distance may correspond to a fractional value of index *k*. Therefore, a novel demodulation is introduced in this section. Instead of operating IDFT for each symbols, we design a loop calculation by fractional increase of index *k*. Here, index *k* can be regarded as step length of measurement. It is easy to understand that smaller step length can get better accuracy.

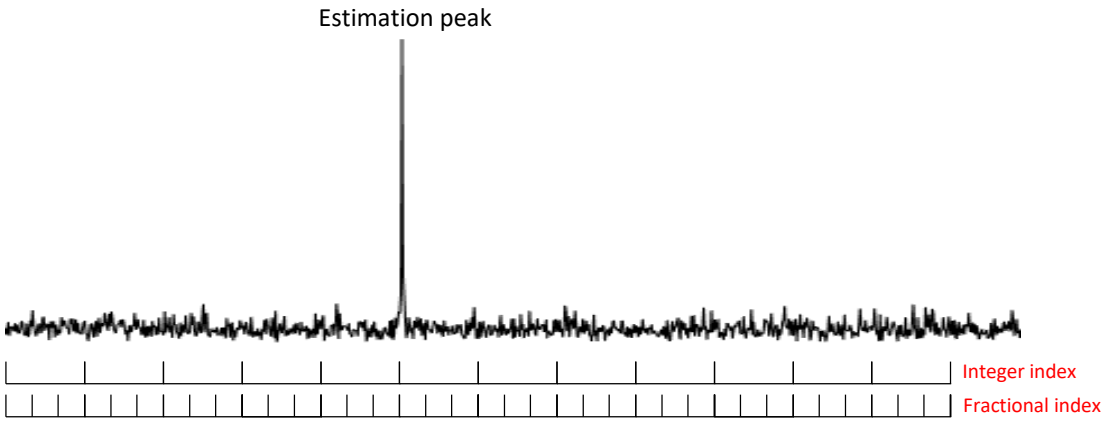


Figure 2.7. Comparison of two measurement step lengths

As discussed in last section, the range estimation equation is

$$\mathrm{r}(k) = \frac{1}{N_c}\sum_{n=1}^{N_c} \exp\left(-j2\pi n f_{spa}\frac{2R}{c_o}\right) \exp\left(j\frac{2\pi}{N_c}nk\right)$$

In this equation, two exponential components cancel each other under the condition

$$k = \frac{2Rf_{spa}N_c}{c_o}, \qquad (k = 0, 0+m, 0+2m, \ldots, N_c - m)$$

In this case, *k* changes *m* ($m < 1$) in a step-wise fashion.

2.4 OFDM algorithm development

The general idea is we want to apply OFDM signal in a “RadCom” system to achieve range and velocity detection and estimation. The algorithm development is shown in figure 2.8. A random bit sequence is

used as a raw signal. Quadrature phase-shift keying (QPSK) modulation is used in this case. QPSK symbols are reshaped in two dimensional matrix. IFFT is operated for QPSK symbols to generate OFDM symbols. After that, cyclic prefix is added to avoid inter symbol interference (ISI). Then the signal is serialized for transmission. In the receiver part, at first, synchronization is completed between received signal and transmitted signal by cross-correlation method. The phase offset in each symbols won't be affected by the time domain synchronization. After that, the signal is reshaped in matrix. Cyclic prefix should be removed before demodulation. Then FFT is calculated to demodulate OFDM signal. The transmitted signal should be removed from received signal, due to the needed information for estimation is only the phase shift. As shown in last section, IFFT along the time domain is used for range estimation, while FFT along the frequency domain is for velocity estimation.

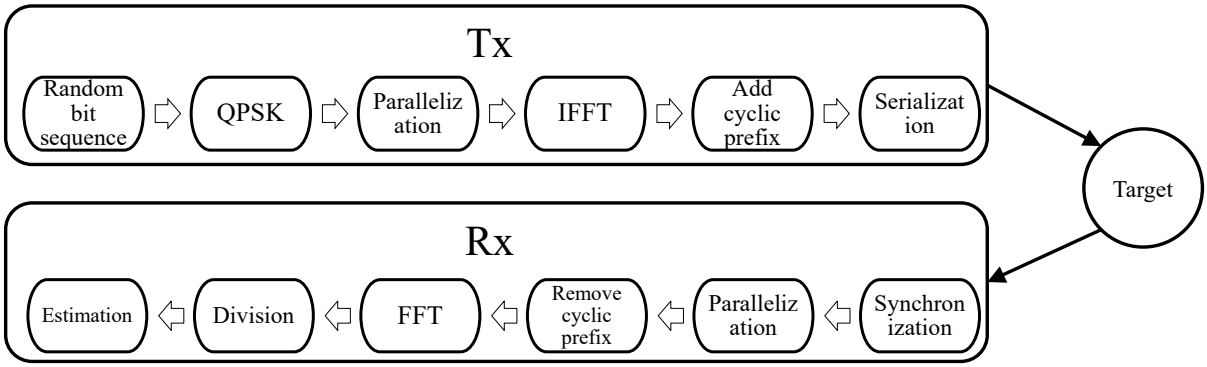


Figure 2.8. Flow schematic of OFDM algorithm

2.5 OFDM radar performance simulation

2.5.1 Channel response

In this section, the influence of frequency offset, time offset, phase noise and time delay are evaluated. Constellation in each case is shown in figure below. Frequency offset is set to 4000 Hz in this case. As shown in figure 2.9(a), the symbols in constellation are rotated by different degrees. This is because frequency offset changes phase in time domain. Similarly, in the case of time offset, which is shown in figure 2.9(b), phase shift of every symbols is the same. Compared to carrier frequency, frequency changing between sub carriers is too small to be calculated. The linewidth of phase noise in this case is set to 500 kHz as shown in figure 2.9(c). Cyclic prefix is adding to avoid ISI, which has the length of 128 symbols in this case. Time delay is set to $0.008*10^{-9}$ s. From the constellation in figure 2.9(d), it is clear that no ISI occurs.

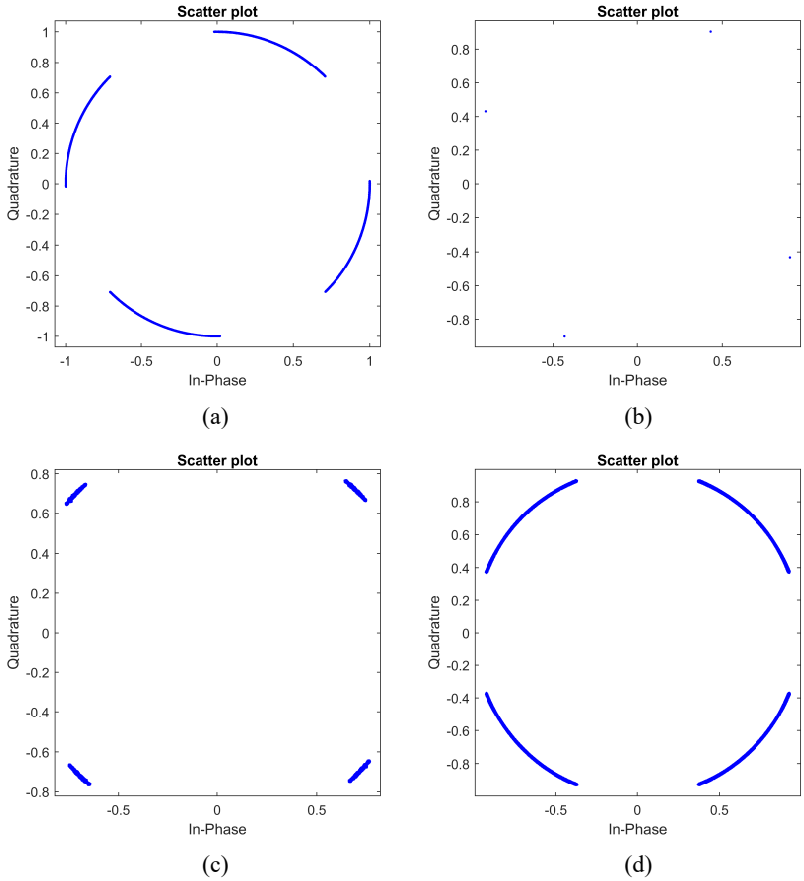


Figure 2.9. Constellations of (a) frequency offset, (b) time offset, (c) phase noise, (d) time delay

2.5.2 Single target

In this simulation, the target is in the position of 40 m away from radar, and has the radial velocity 10 m/s. According to theory section, two peaks in the figure 2.10 represent the estimated range and radial velocity. Noise is of no concern in this case. QPSK modulation is used, and the sampling frequency is 1 GHz, which means the signal has bandwidth of 500 MHz. A 2048k bit sequence is transmitted with 1024 sub carriers. Small variation in the figure is caused by range and frequency resolution. In this case, the range resolution is

$$r_d = \frac{c_o}{2 * f_{spa} * N_c} = 0.3 \text{ m}$$

and the velocity resolution is

$$r_v = \frac{f_{spa} * c_0}{2 * f_{car} * N_{sym}} = 0.8772 \text{ m/s}$$

Carrier frequency in this case is 83.5 GHz.

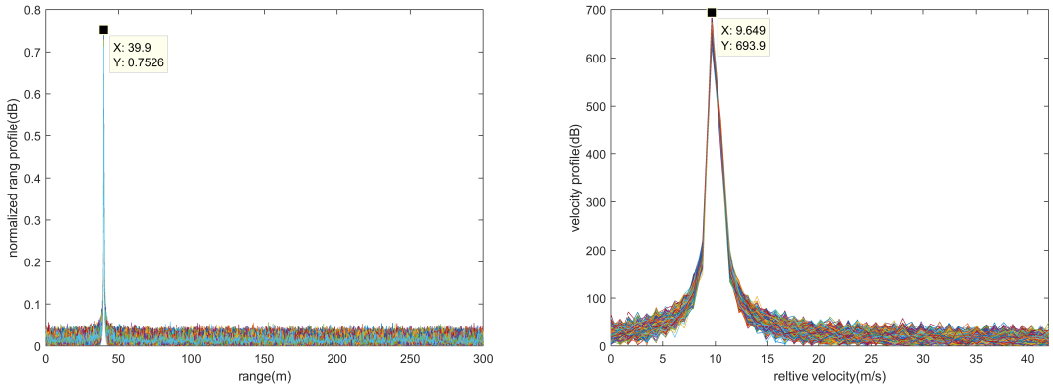
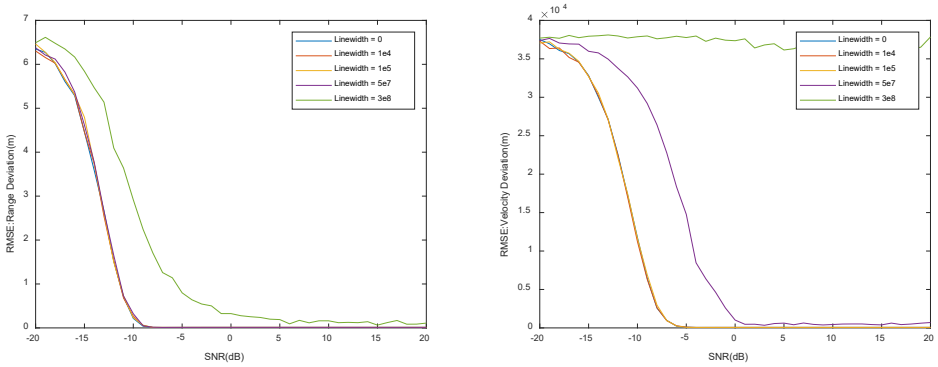


Figure 2.10. Range and radial velocity estimation

Additive white Gaussian noise (AWGN) channel is used to evaluate the algorithm in the next stage. In the channel, phase noise is also added to see the tolerance of this system. From the figure below, it is shown that when SNR is larger than -5 dB, no error appears, even when the phase noise with a linewidth of 10 kHz or 100 kHz is added. When the linewidth of phase noise is up to 50 MHz, which will not happen in reality, the range estimation still has good performance. This is because phase noise mainly affects phase of transmitted signal, which is in the time domain. When it is set to 300 MHz, the system cannot be used to detect velocity.

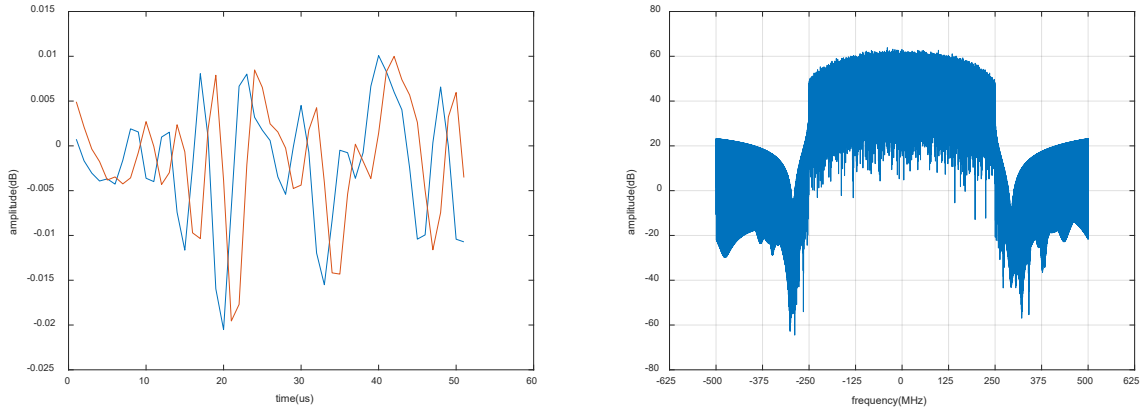


(a) (b)

Figure 2.11. Effect of phase noise in AWGN channel (a) range estimation deviation (b) velocity estimation deviation

2.5.3 Multiple targets

In this case, estimation of two targets will be investigated. Figure 2.12 shows the received signals in time domain and frequency domain. In time domain, different time delay caused by different distance of targets. In the spectrum, attenuation appears due to the influence of Doppler frequency. In the middle, the signal overlap lead to power increase. In terms of constellation, symbols in 128 sub carriers are shown in figure 2.13. We can see that the curve of constellation is not tending to be a circle any more. It is because the power changed by overlap and the Doppler frequency shifting of received signals.



(a) (b)

Figure 2.12. Simulation of two targets: (a) signals in time domain (b) spectrum

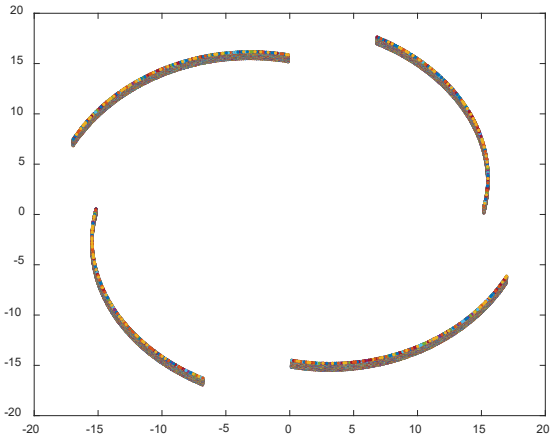


Figure 2.13. Constellation of 128 sub carriers

As shown in figure 2.14, two peaks are shown in both range and velocity estimation. The first target has the distance 110 m away with radial velocity 10 m/s, while the second target is 5 m away with radial velocity 30 m/s. The limitation of multiple targets is dependent on range and velocity resolution.

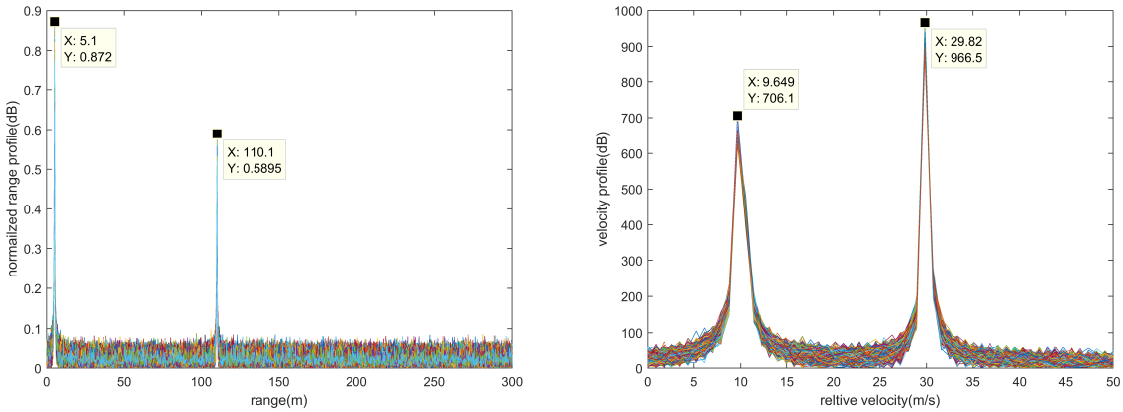


Figure 2.14. Estimation of two targets

2.5.4 Fractional step length

As demonstrated in section 2.3.4, the estimation resolution can be improved by fractional step length estimation method. In this simulation, the signal bandwidth is 500MHz as before. Range estimation is taken as an example and the target is set 2.16 meters away. In the integer estimation, the target cannot be detected very accurately due to the resolution limitation. In the fractional method, the step length is set to 0.1, which provides the resolution 0.03 meter. In figure 2.15 (b), the estimation is exactly in 2.16 meters as the expectation.

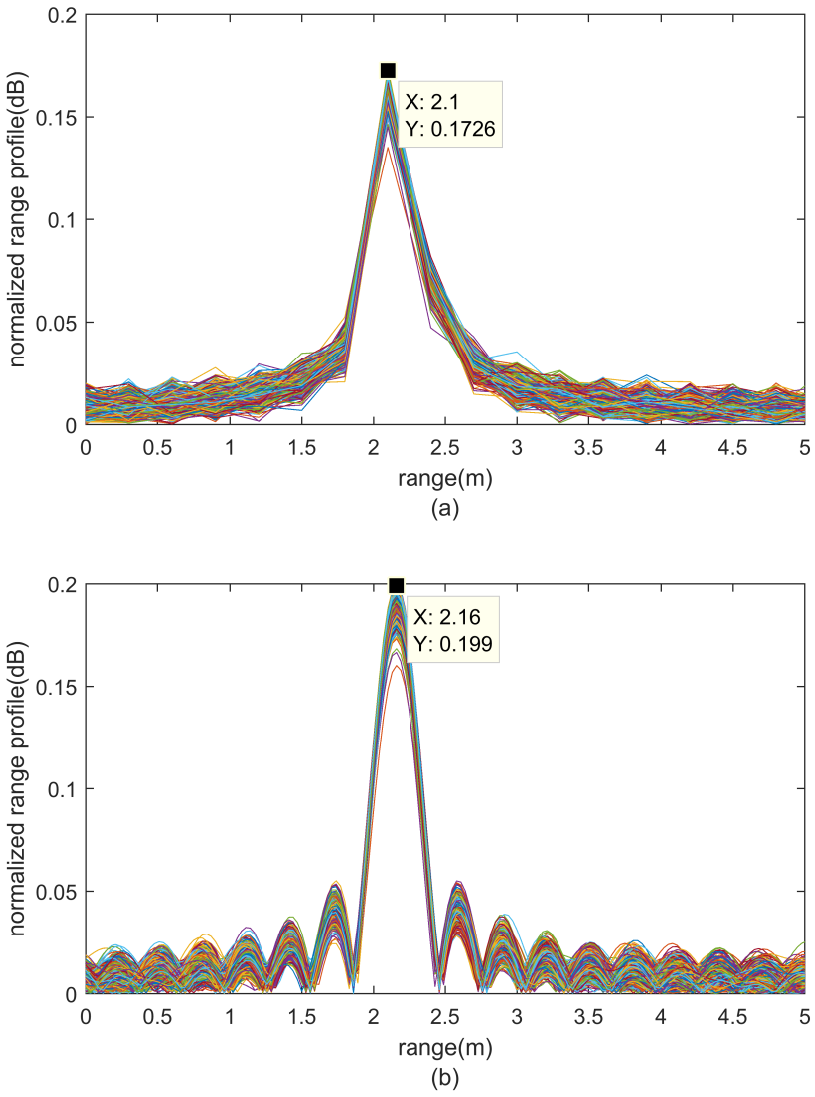


Figure 2.15. Comparison of IFFT and fractional step length estimation (a) Sample based IFFT estimation (b) Fractional step length estimation

Then multiple target estimation is simulated in fractional step length method as well. Two targets are used in this case. The first one is 2.16 meters, while the other is 2.76 meters away. The estimation peak is shown in figure 2.16. In figure 2.16 (b), the estimation peaks occur around the target ranges but with one sampling point shift. This is because the side-lobe of one target influences the main-lobe of other target. To solve this problem, a curve of *sinc* function can be generated for the more accurate estimation

by cross-correlation operation between a known *sinc* function and the estimation peak. This idea needs more research work and won't be discussed in this thesis.

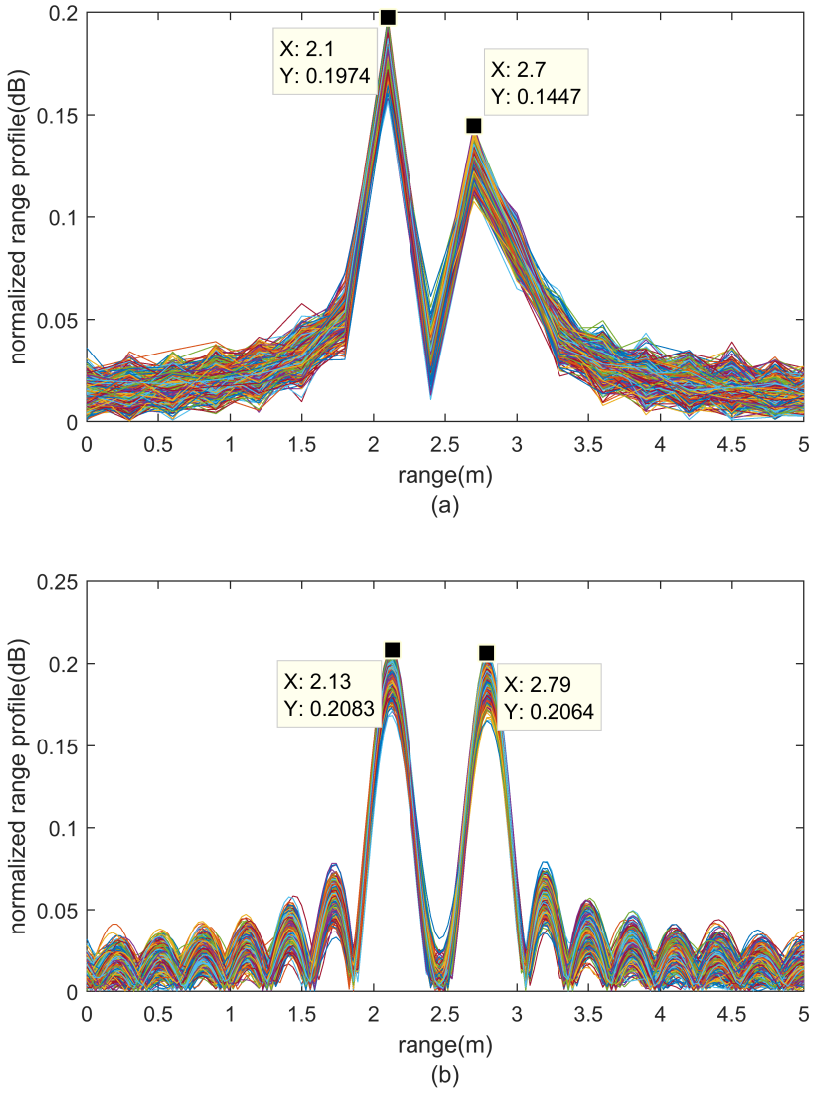


Figure 2.16. Comparison of IFFT and fractional step length estimation in multiple target (a) Sample based IFFT estimation (b) Fractional step length estimation

3

DSP builder implementation

In this chapter, three stages of the DSP builder system design are discussed, namely system development, hardware implementation and system verification. A single carrier demonstration is used to show the work flow. In the system development, DSP builder software for Intel FPGAs is introduced [14]. The system design of transceiver is shown step by step. Some simulation results are shown to confirm the functionality of the system. In the implementation section, the FPGA board and the signal converter card are first introduced. Then, Quartus Prime software including embedded IP components and tools are introduced [15]. In the final stage, the setup is shown by several pictures and the verification results are shown based on the results in SignalTap Logic Analyzer.

3.1 Intel DSP builder introduction

Intel DSP builder combined with Simulink environment will be used to generate hardware description language (HDL) algorithm for FPGA. In the areas of radar and wireless communication digital signal processing, DSP builder software provides sufficient solutions in model development with diverse functionality blocks. In this thesis work, DSP builder advanced blockset will be used to generate the whole system and Quartus Prime software with SignalTap Logic Analyzer will be used to compile, configure and verify the design.

3.2 Software cooperation

As shown in figure 3.1, the system design is completed in three stages, which are system development, hardware implementation and system verification. In the system development, Matlab signal resource is used as the simulation input signal. DSP builder advanced blockset is used to build the module in Simulink platform. After the simulation, DSP builder can generate an IP core for hardware implementation. In the Quartus Prime software, several embedded hardware IP components are designed and used in the hardware implementation. Timing constraints and pin planning are set according to the hardware specification. In the verification stage, the SignalTap Logic Analyzer is used to verify the transmitted and received signals in every stage. With this tool, we can watch the signals in real-time to get dynamic feedback from hardware performance.

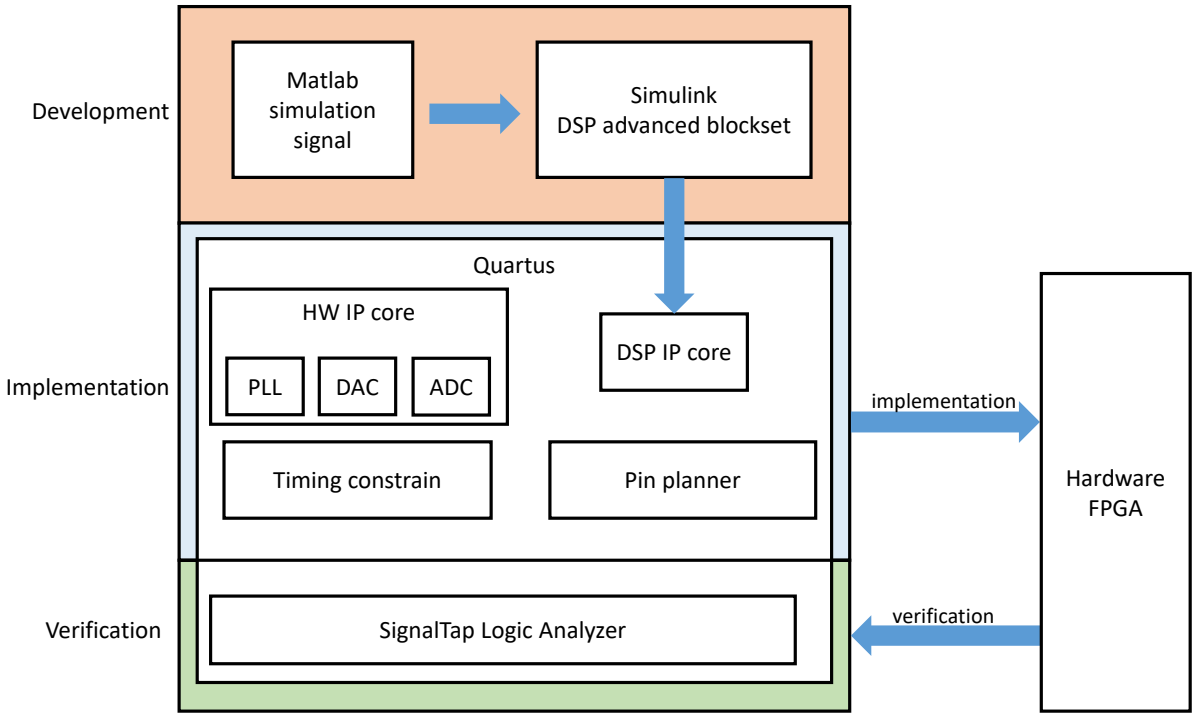


Figure 3.1 Software cooperation

3.3 System development of single carrier demonstration

3.3.1 System introduction

The system design flow is shown in figure 3.2. An initial bit sequence is generated with 14 bits to adapt hardware requirements. The filter in the transmitter combines the two functions of interpolation and signal shaping. A numerical controlled oscillator (NCO) is designed to generate a 12MHz sinusoidal. After a mixer, the baseband signal is up converted into 12MHz, which is the intermediate frequency used in the system. The bit shift block is designed to make sure that distortion won't occur in the output signal. In the receiver part, a selector is designed to select sampling point since sampling rate of analog to digital converter (ADC) is half of the digital to analog converter (DAC). After the mixer in receiver, signal is down converted to baseband. Two filters are used serially for three times decimation and signal shaping. A qualifier is designed to set the optimal sampling point after the demodulation. Every block will be explained in detail in this section.

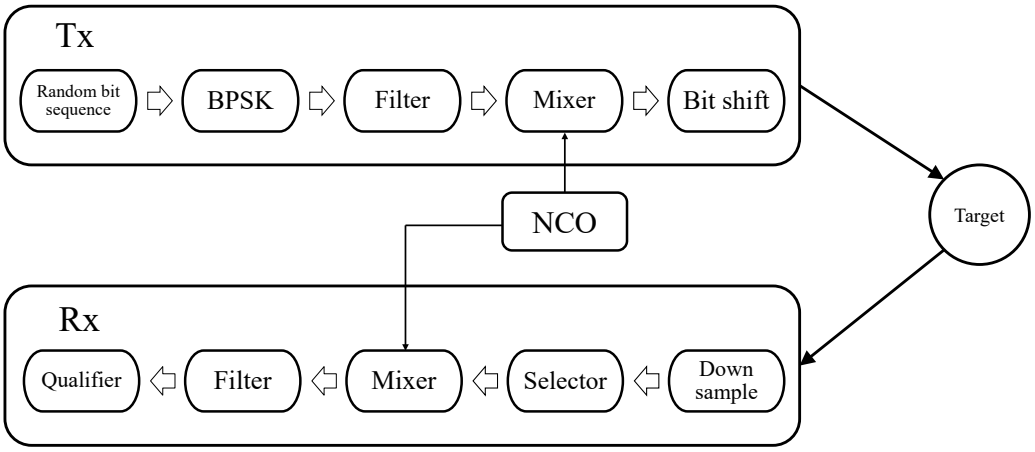


Figure 3.2. Radar communication system design diagram

3.3.2 Transceiver development

As shown in figures below, the whole system model built in Simulink is presented. In figure 3.3, we can see the completed idea of transmitter development. A memory sub system is built to generate an input signal sequence and store the data. When we run the system, the input data will be sent out periodically from this sub system. The input signal we used is a random data sequence with BPSK modulation. The symbol rate is 1 MBaud while the sampling rate is 120 MHz in this case. An interpolating FIR filter is designed to interpolate 120 times for the initial BPSK symbols. This filter block also implements another filter design function: A root raised cosine (RRC) filter is designed and embedded into this block to shape the signal. Then, the data signal is connected to a real-valued mixer block after a scaling block. All the scaling blocks are used to remove redundant signal bits. The NCO block is used to generate carrier waveform. In this case, sinusoid with frequency 12 MHz is the output result of NCO block. After the mixer, we use a mux block to multiply channel I and channel Q. A bit shift sub system is developed to ensure that the output data has the full amplitude with unsigned signal type.

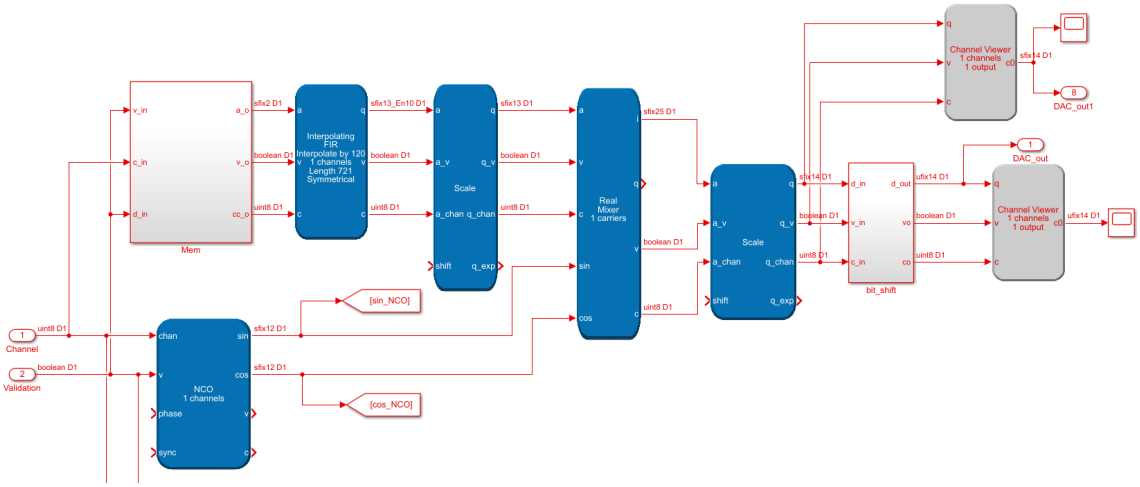


Figure 3.3. Transmitter model in Simulink

The receiver model is shown in figure 3.4. When the data is exported from SignalTap Logic Analyzer, it will be read by Simulink. The input data goes to a real-valued mixer with the same sinusoid signal generated from NCO block to remove the carrier wave. The output signal of mixer goes to the demodulation sub system and after demodulation, an eye diagram block and a constellation diagram block are connected to allow for verification of the results.

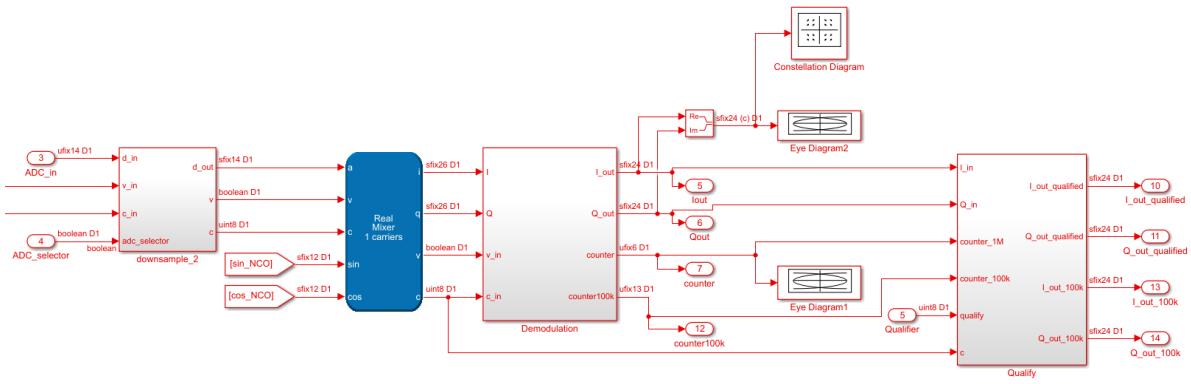


Figure 3.4. Receiver model in Simulink

In figure 3.5, the demodulation sub system is shown. The methods for I and Q are the same, so a mux Simulink operation block is used to simplify the system structure. Two filters are used in serial. At first, a decimating FIR filter helps us to decimate the data by three times to save resource in hardware. The embedded function of this filter is a low pass filter which is used to filter out the mirrored signals out of the bandwidth. The second filter is designed as another RRC filter with the same parameter in the transmitter for signal shaping. By multiplication of two RRC filter, a raised cosine filter function will be achieved, which means the system uses raised cosine filter as pulse shaping method to minimize the ISI. In the left bottom corner, there are two counters. The top one counts from 1 to 60 based on Simulink sample based calculation. This is used as a qualifier to make data store at the optimal sampling point. The details of qualifier are shown in figure 3.7. The bottom counter from 0 to 6000 is used for the future work with lower frequency, which will be discussed in the final chapter.

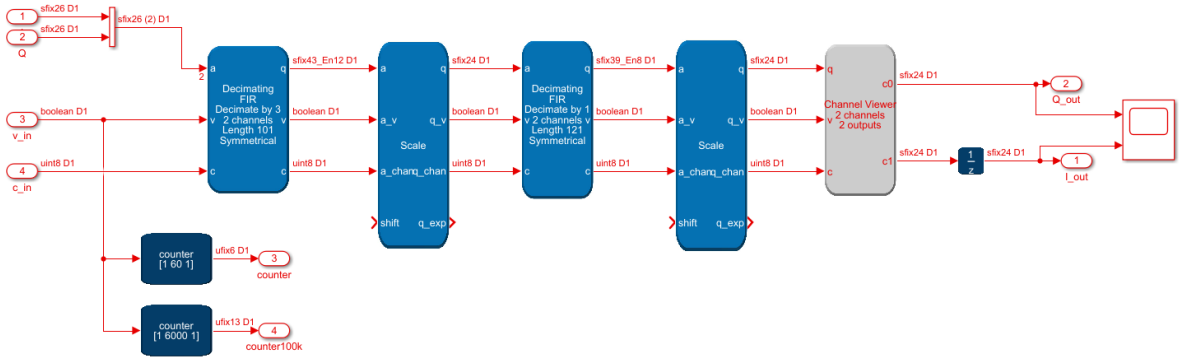


Figure 3.5. Demodulation method

As shown in figure below, two comparators are used to select optimal sampling point. If the optimal sampling point is selected, the output of comparator will be '1' to the validation port, which means that only at this point, the data could be stored.

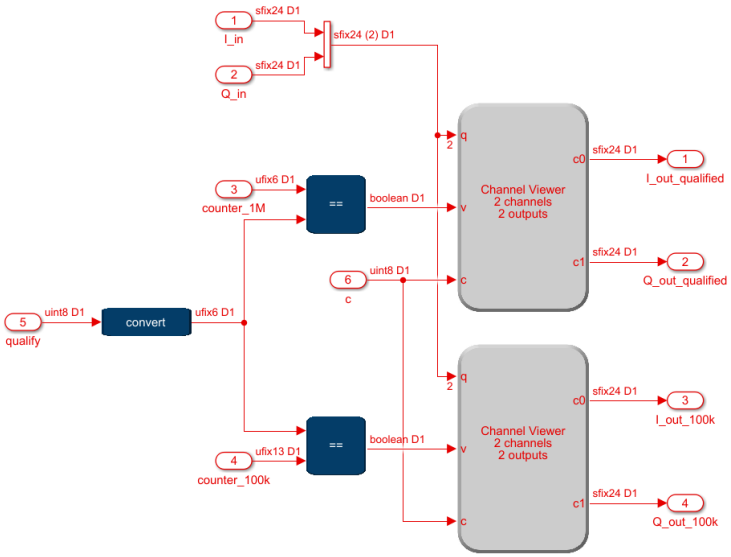


Figure 3.6. Qualifier design

3.3.3 Simulation result

The modulated signal generated by DSP builder system will be sent out from transmitter by DAC. In figure 3.7, the waveform of DAC output signal in the simulation is shown. The signal has 14 bits unsigned amplitude with no attenuation.

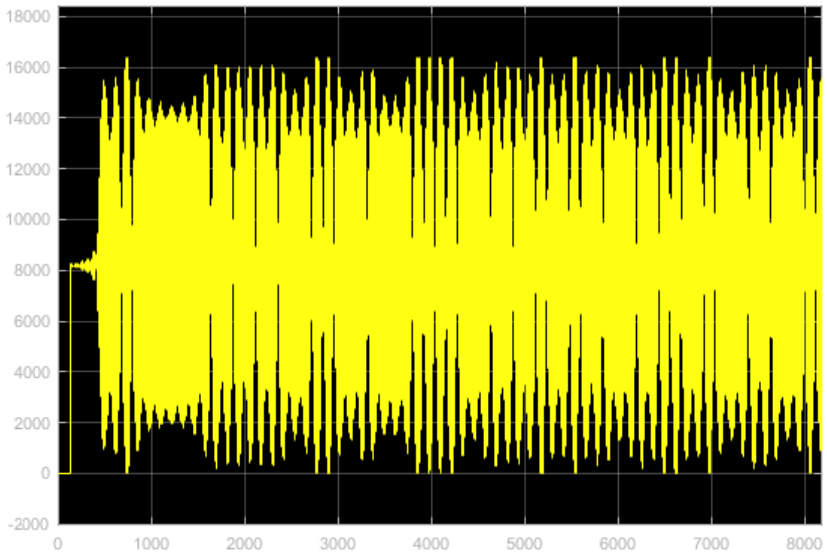


Figure 3.7 Transmitted signal waveform in simulation

After demodulation, the constellation and eye diagrams are shown in figure 3.8. A phase rotation is corresponding to sample delay which is expected. I and Q channels in the eye diagram are in a very good quality as expected.

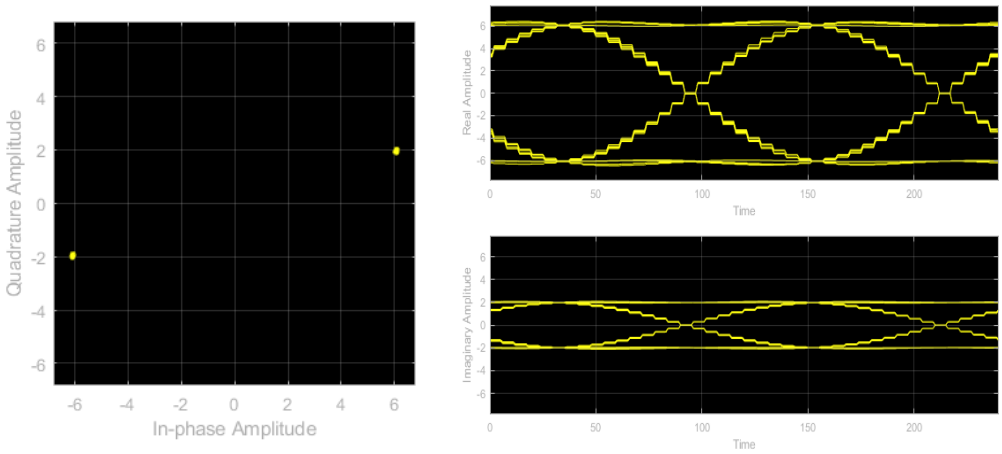
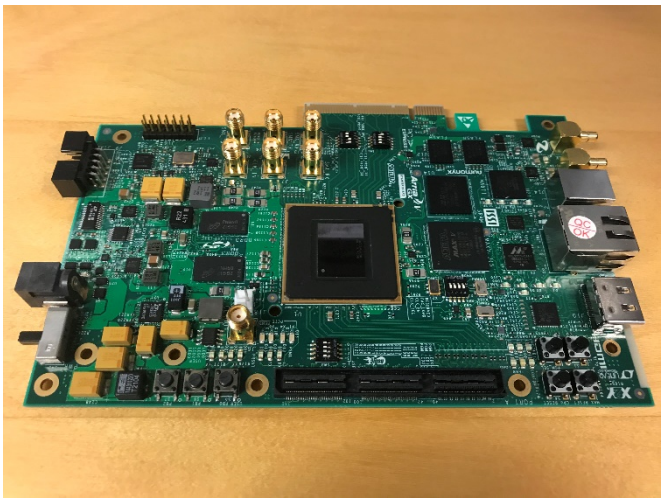


Figure 3.8. Constellation and eye diagram in simulation

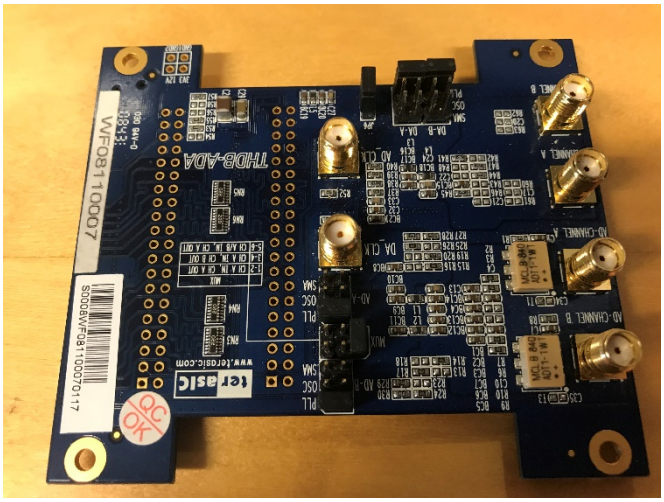
3.4 Hardware implementation

3.4.1 Hardware platform introduction

As shown in figure 3.9, the Arria V generation FPGA board and THDB-ADA-HSMC (AD/DA) card are used in this project. One high-speed mezzanine card (HSMC) connector on FPGA board is used to make the connection of them.



(a) Altera Arria V FPGA board



(b) THDB-ADA-HSMC card

Figure 3.9. Pictures of hardware used in this project

3.4.2 Arria V generation FPGA platform

3.4.2.1 Board overview

Arria V generation FPGA board is a starter board for developing and prototyping low-power, high-performance, and logic-intensive designs [11]. In Arria V GX 5AGXFB3H4F35C4N FPGA, there are 17,260 Kbit on-die block memory blocks, 24 high-speed transceiver blocks, 2,090 18x19 multiplier blocks and 544 general purpose inputs and outputs [11]. The board running mode can be controlled by DIP switches. Four push buttons are used for central processing unit (CPU) reset, system reset, program

load and program selected. The general user push buttons are defined as ADC amplitude controller, ADC sampling point selector and Phase-locked loop (PLL) reset.

3.4.2.2 Clock circuit

The starter board includes programmable oscillators with multiple frequencies, which is shown in figure 3.10. In this project, we use 50 MHz fixed oscillator to generate the clock signal.

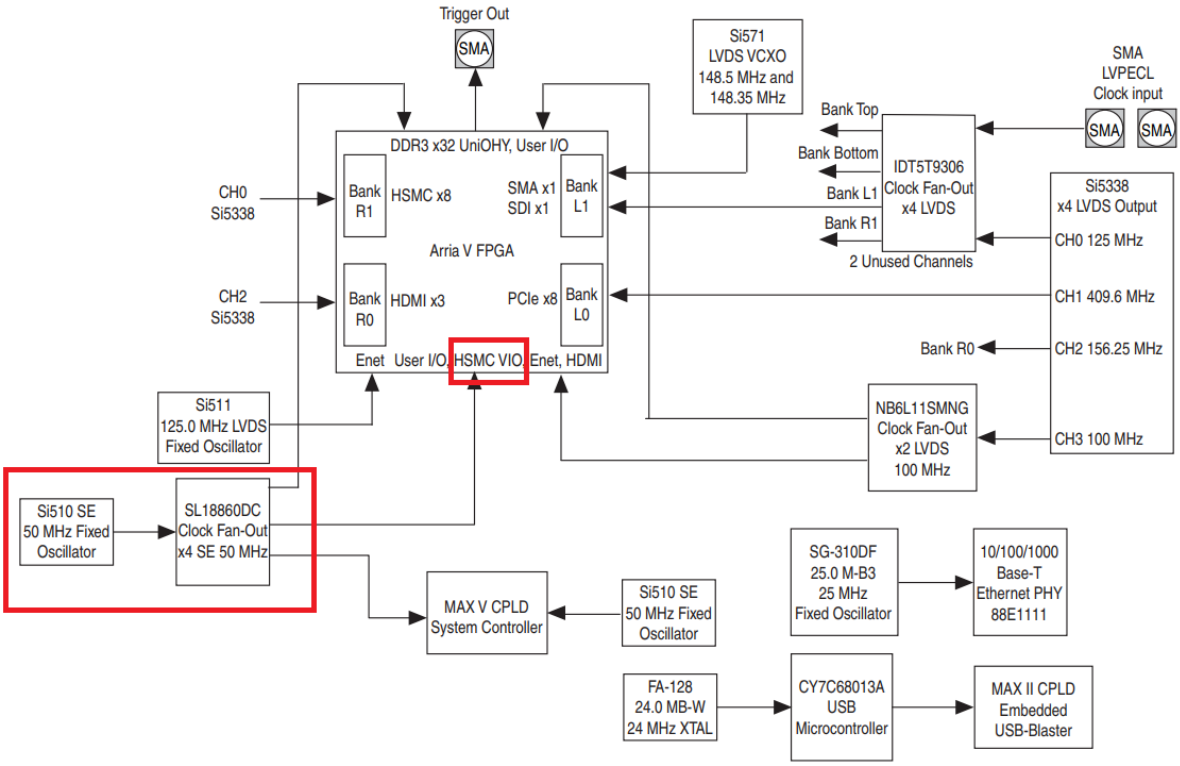


Figure 3.10. Oscillators and the I/O standards on Arria V FPGA board [11]

3.4.3 DAC

Dual-port and interleaved are two DAC timing modes in this card. One DIP switch is used to control it. Since the system only requires one data output signal, the interleaved mode is more complicated for it. We use dual-port timing mode in this system. The timing sequence of dual port mode is shown in figure 3.11. The DAC clock signal should not be later than the WRT signal while the data out signal should have a propagation delay between rising edge of WRT and data output signals. WRT signal here is the initial enable signal of DAC.

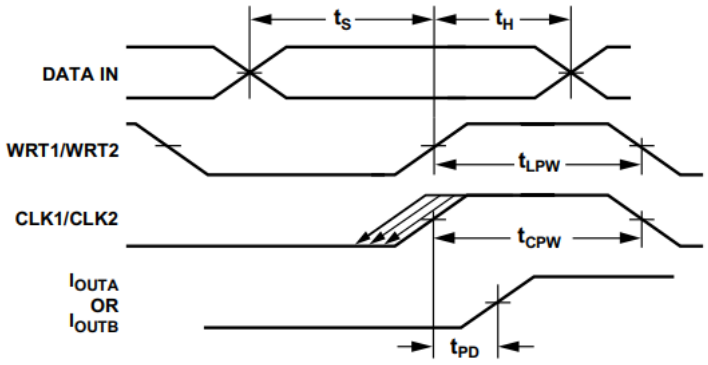


Figure 3.11. DAC timing in dual-port model [12]

3.4.4 ADC

The timing sequence in ADC is shown in figure 3.12. Data output will have a seven clock cycles pipeline delay. The propagation delay between clock and data is limited between 2 ns to 6 ns.

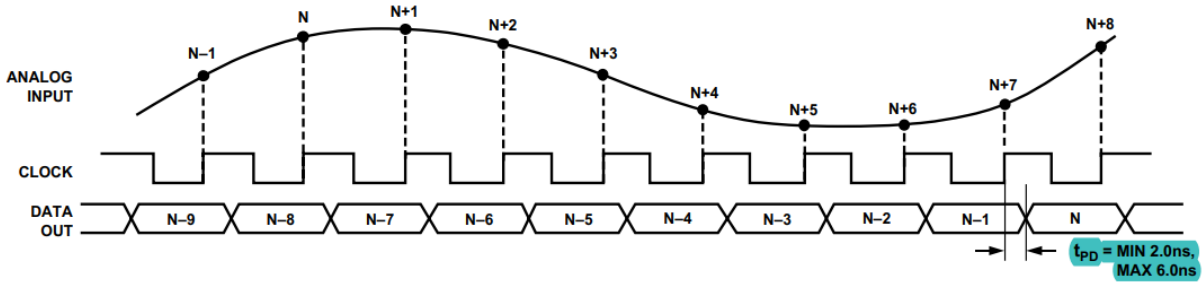


Figure 3.12. ADC timing [13]

3.4.5 Phase-locked loop and clock generator

The clock generated by local oscillator on FPGA is 50 MHz, and the clock frequencies of DAC and ADC are 120 MHz and 60 MHz respectively. In this project, a phase-locked loop (PLL) is used to generate clock signals for different devices. 50 MHz FPGA clock is the input baseline clock signal. Since a WRT signal is required in DAC, the output clock should be two 120 MHz clock signals for DAC clock signal and WRT signal, and one 60 MHz clock signal for ADC clock. Figure 3.13 illustrates PLL working theory.

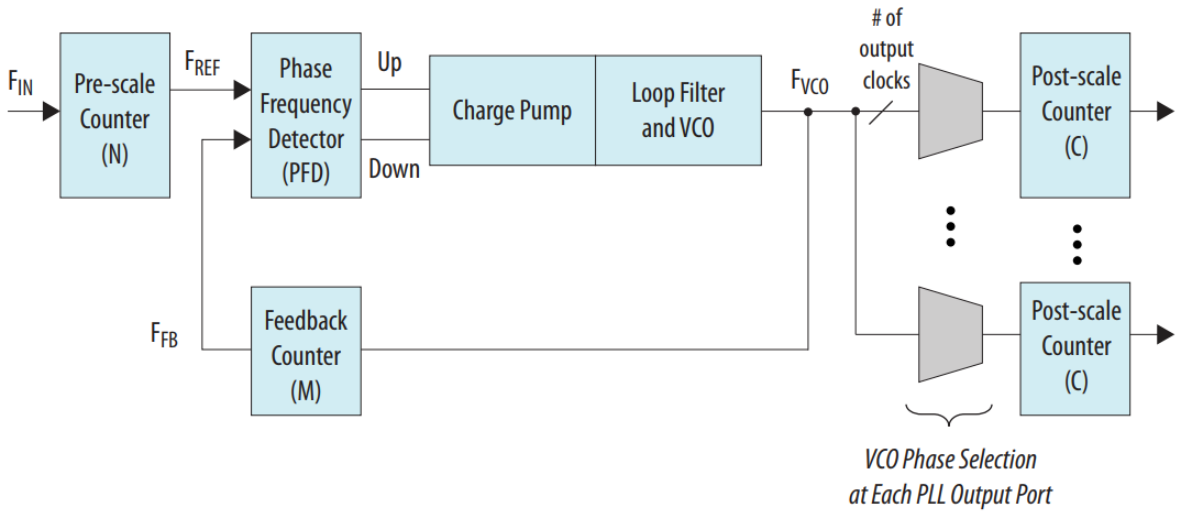


Figure 3.13. Phase-locked loop (PLL) architecture [16]

The flow of data and clock signals is shown in figure 3.14. The clock signal is generated by FPGA local oscillator and sent to PLL to generate DAC and ADC clock signals. DSP builder uses the same clock as DAC to emulate the real situation. Inside DSP builder, as discussed in section 3.3.2, a down sampling sub system is designed for the demodulation due to different clock frequencies between DAC and ADC. The data generated by DSP builder is sent out by DAC, after the target reflection, it is acquired by ADC and sent back to DSP builder system for the demodulation signal processing.

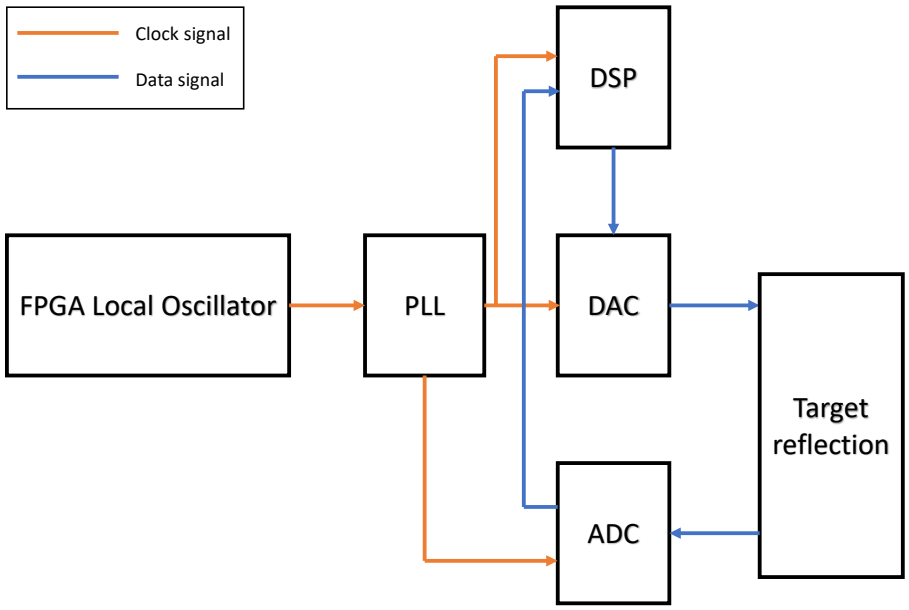


Figure 3.14. Clock and data signals flow

3.4.6 Structure design in Quartus Prime

The schematic of top level is shown in figure 3.15. The top level is programmed in VHDL (Very high-speed integrated circuit Hardware Description Language) and complied in Quartus software. PLL and RAM (Random Access Memory) are two IP components in this project. DAC clock signal is used in

RAM component and DSP builder component. A RAM component stores the sampling point information for the qualifier. With the RAM, sampling point can be easily changed during the system running. Reference clock signal from FPGA oscillator and data acquired by ADC are two input signals for the system. After the demodulation, I and Q signals are captured with the information of phase and amplitude, which will be used in the estimation.

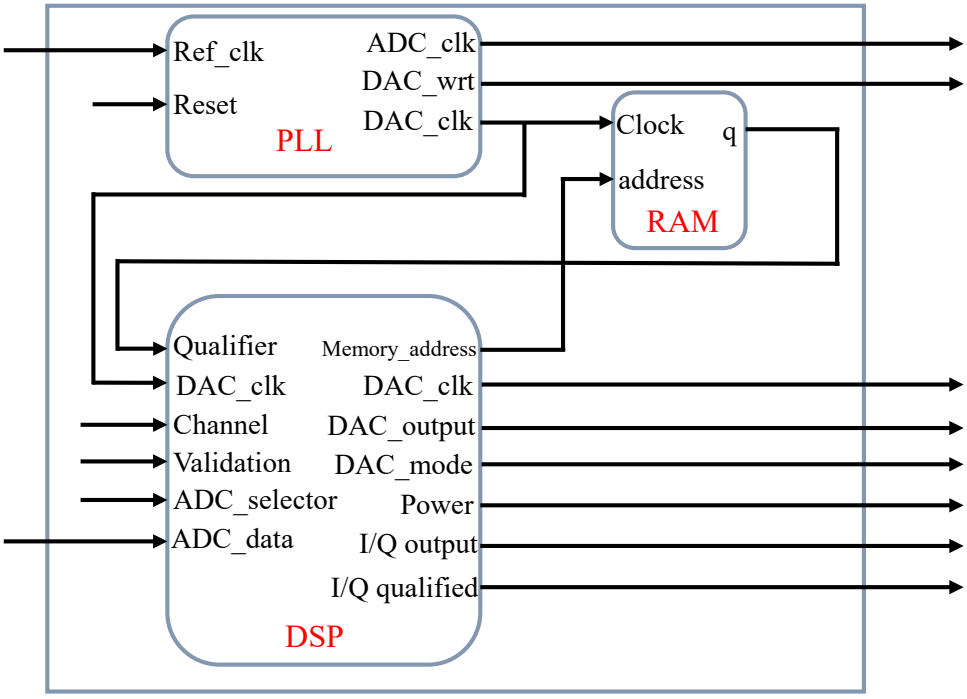


Figure 3.15. Top level schematic diagram

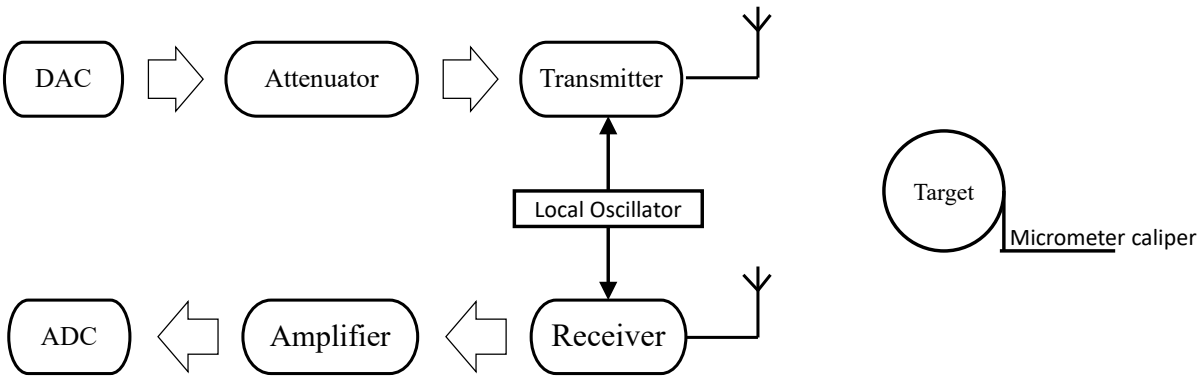
In figure 3.16, the work flow in Quartus software is shown. The pin planner tool provides a platform for pins setting. With the correct pin connection, the system can be completely complied and programmed into FPGA. SignalTap Logic Analyzer is used to observe signals in real time. The memory editor tool is used for RAM IP component to read and write values into a selected address.

Figure 3.16. Implementation in Quartus tools working flow

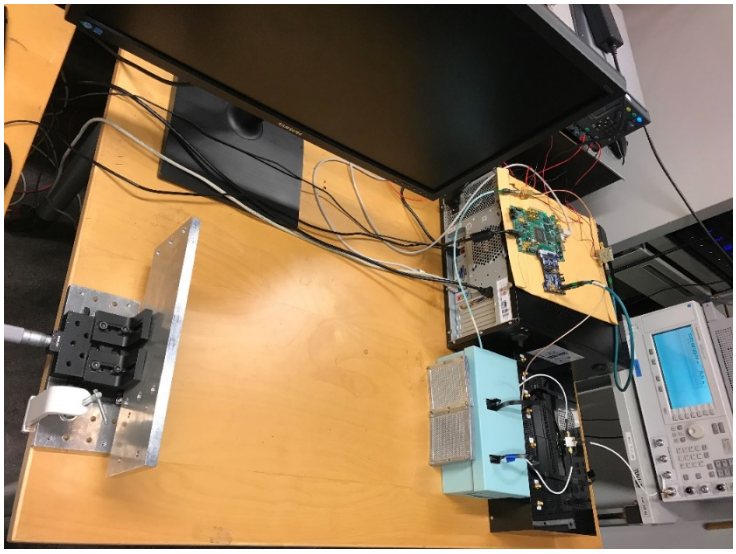
3.5 System verification

3.5.1 Transceiver setup

The whole setup including transceiver, antennas, target, FPGA and AD/DA convertor is shown in figure 3.17. The input I and Q signals to the receiver are not split out in this case. A spiral micrometer caliper is used to change the target distance. A local oscillator with 10 GHz is used to generate RF carrier. The transceiver box has a six-fold frequency mixer, which means the carrier signal has the frequency of 60 GHz.



(a) Block daigram of setup



(b) Transceiver and hardware platform setup

Figure 3.17. Schematic and picture of hardware setup

Since this setup may be used in Chalmers DSP course, a transceiver box is made to protect dies inside, which is shown in figure 3.18.

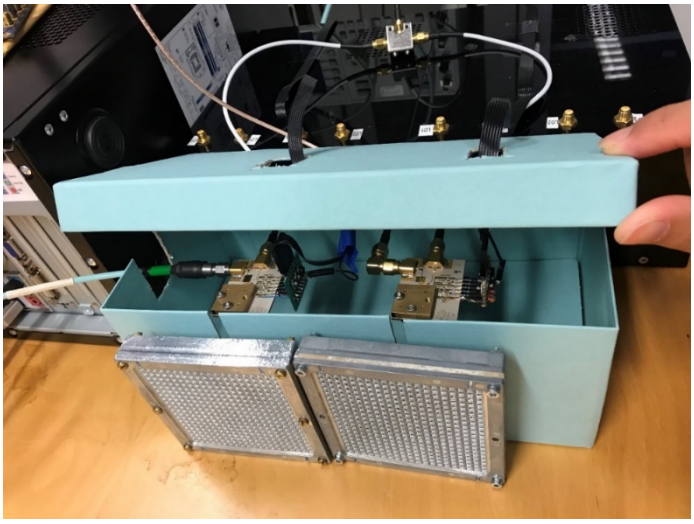
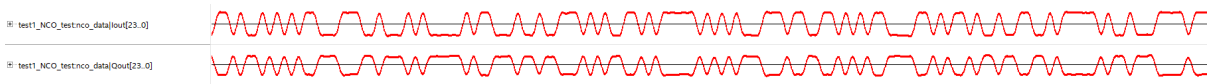


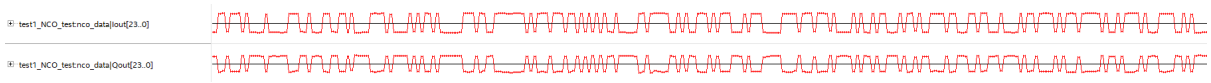
Figure 3.18. Handmade transceiver box

3.5.2 Verification result

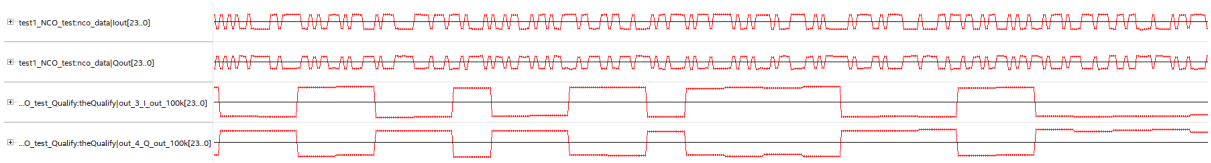
After the implementation on hardware, the SignalTap Logic Analyzer is used to observe channel I and channel Q. As shown in figure 3.19 (a), the waveforms of I and Q signals are the same as simulation result. In this tool, it is easy to see the waveform and amplitude changing. After the qualifier, in figure 3.19 (b), we set the optimal sampling point for I and Q signals. In each symbol, only the highest or the lowest values are selected and remained. The result here is as our expected. A little vibration occurs due to the channel noise. In figure 3.19 (c), the signal is decimated by 10 times. In this case, the symbol rate will decrease to 100k symbol per second, which may be used in the future work.



(a) I and Q signals in SignalTap Logic Analyzer



(b) I and Q signals after qualifier



(c) I and Q signals with 10 times lower frequency

Figure 3.19. I and Q signals in different cases

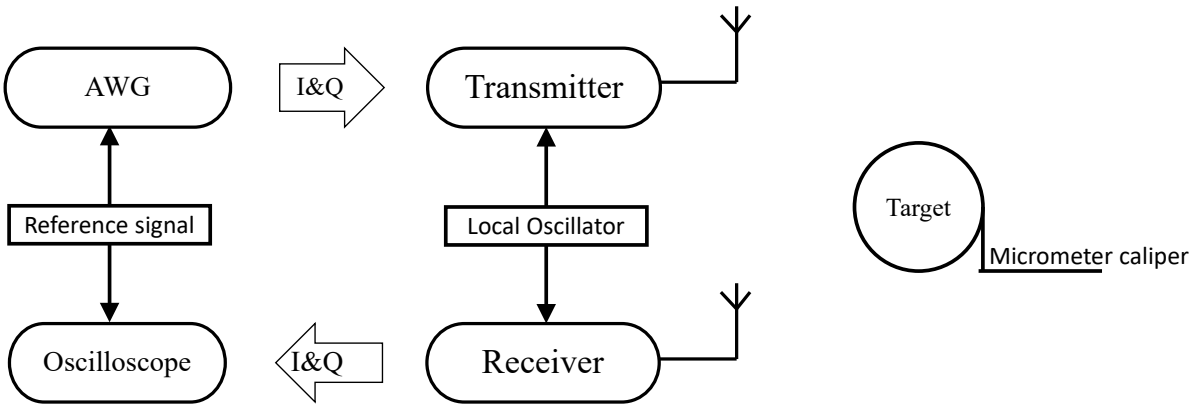
4

OFDM Experiment

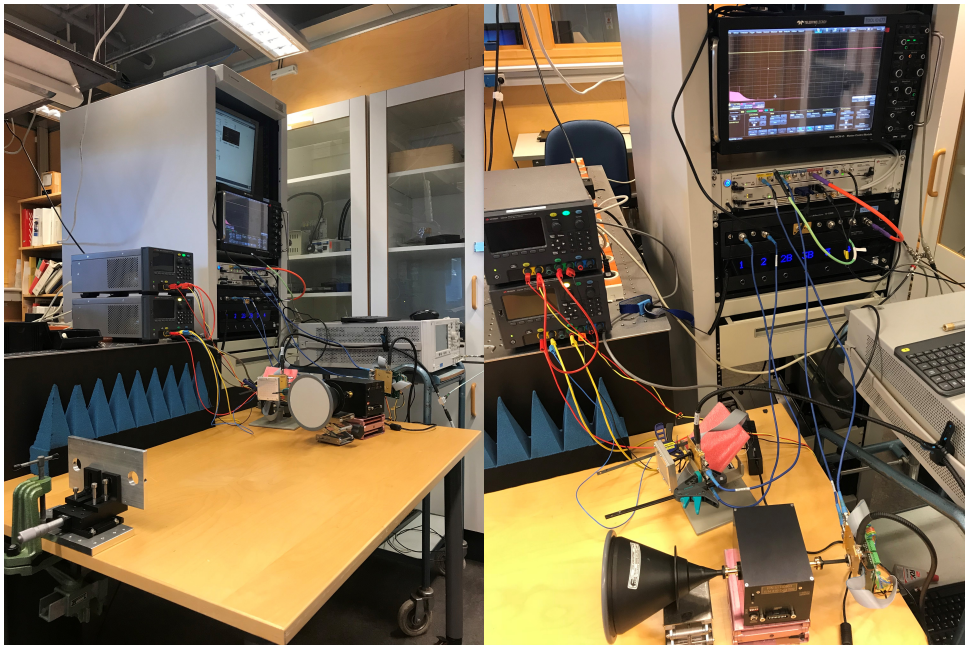
In this chapter, the experiment of OFDM "RadCom" system will be introduced in the lab setup and the final results. This measurement is completed with 80 GHz radio frequency equipment including the transmitter and receiver set up at Microwave Electronics Lab at Chalmers University of Technology. The purpose of this measurement is to demonstrate the improved range resolution in "RadCom" system with OFDM techniques.

4.1 Measurement setup

Keysight M8195A 65Gsa/s arbitrary waveform generator controlled by Matlab, where the baseband transmitter is implemented, is used to generate OFDM QPSK signal. In the experiment, 128 sub carriers with 8GHz bandwidth in total are used. At the receiver, Teledyne Lecroy 100 GHz oscilloscope is used to capture the baseband received signal. Subsequent signal processing is implemented offline in Matlab. Gotmic's E-band transmitter and receiver with integrated mixer, frequency multiplier, and amplifiers are used. With integrated 6 times multiplier in the transmitter and receiver, the RF carrier wave is able to reach 80 GHz. The setup is shown in figure 4.1.



(a) Block diagram of setup



(b) Lab measurement setup

Figure 4.1. Setup pictures and diagram

As shown in figure 4.2, a spiral micrometer caliper is used to vary the distance of the target. With this spiral micrometer, the distance between the target and the transceiver antennas can be varied with offset from 0mm to 25mm. Then the distance can be changed from 0mm to 50mm due to the round-trip transmission.

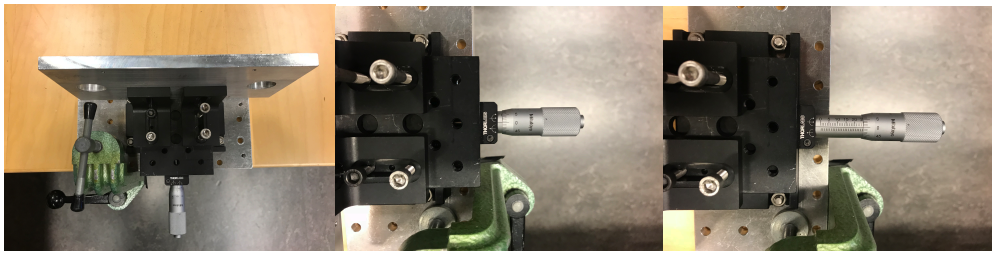


Figure 4.2, Spiral micrometer caliper for distance changing (distance variation from 0mm to 25mm)

4.2 Results

There are three estimation stages of the range. The first stage relies on cross-correlation of transmitted and received signals. The second stage relies on the OFDM algorithm. The last one is based on fractional increase of demodulation index.

In the first stage, the time delay of the transmitted signal and the received signal is calculated based on cross-correlation. The sampling frequency in this case is 1 GHz. Based on this estimation theory, the range resolution is

$$r_d = \frac{c_o}{f_s} = 0.3 \text{ meter}$$

With the offset range of the micrometer, the range resolution of the cross-correlation stage is not good enough.

In the second stage, the range resolution can be calculated by the algorithm in OFDM technique.

The range resolution is

$$r_d = \frac{c_o}{2 * f_{spa} * N_c} = \frac{c_o}{2 * BW}$$

In this equation, f_{spa} is frequency spacing between each sub carrier and N_c is the number of sub carriers. The product of these two indexes is bandwidth, which means we can improve range resolution by increasing the bandwidth.

In this case, signal bandwidth is 8GHz. then we can get the result that is

$$r_d = 0.0187 \text{ meter}$$

This estimation is much more accurate than the first one.

In the third stage, the resolution is

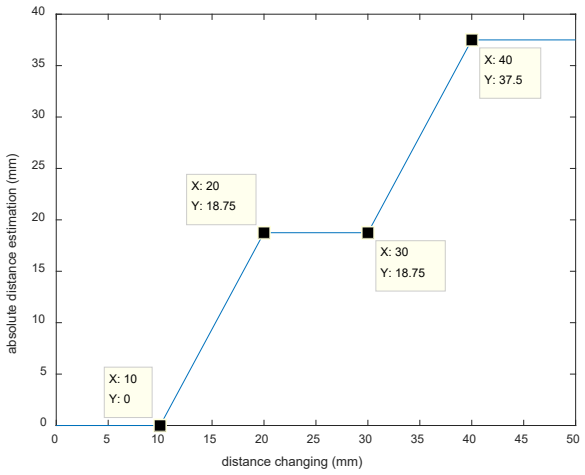
$$r_d = m * \frac{c_o}{2 * f_{spa} * N_c} = m * \frac{c_o}{2 * BW}$$

In this equation, *m* is step length of index *k*. If *m* is set to 0.2, this means $k = 0, 0.2, 0.4, \ldots, N_c - 0.2$. The resolution is

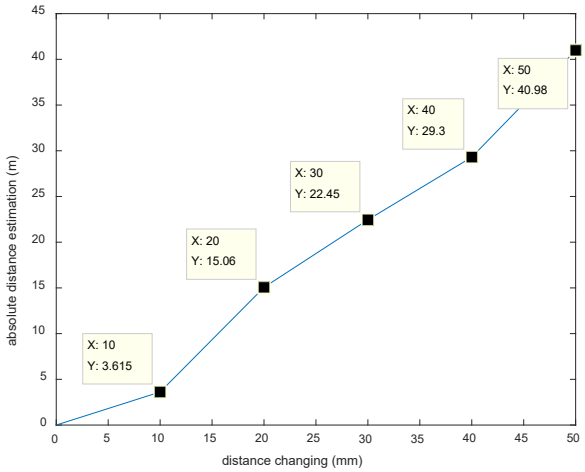
$$r_d = 0.00374 \text{ meter} = 3.74 \text{ mm}$$

With this method, the algorithm will never be the limitation of estimation resolution. If the FPGA hardware platform is powerful enough to support this operation, parameter *m* can be as small as we want. In this situation, the resolution is depended on the maximum amplitude estimation of the *sinc* main lobe and SNR in the measurement.

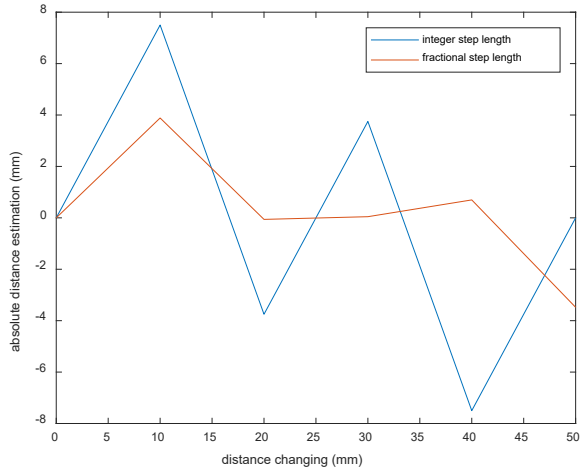
When the distance is changing from 0mm to 50mm, the estimation results of the OFDM algorithm are shown in figure 4.3. It can be seen that with the distance changing, the IDFT OFDM estimation method can only estimate a rough relative distance due to the large resolution. In figure 4.3(a), it is very clear to see that when the distance changed from 20 mm to 30 mm, OFDM technique with IDFT demodulation cannot detect this movement. As shown in figure 4.3(b), fractional OFDM method can detect every step changing and make the more accurate estimation. In figure 4.3(c), the deviation comparison is made between two OFDM methods. With the fractional step length method, the deviation, which is floated within 4 millimeters, is smaller than IDFT method.



(a)



(b)



(c)

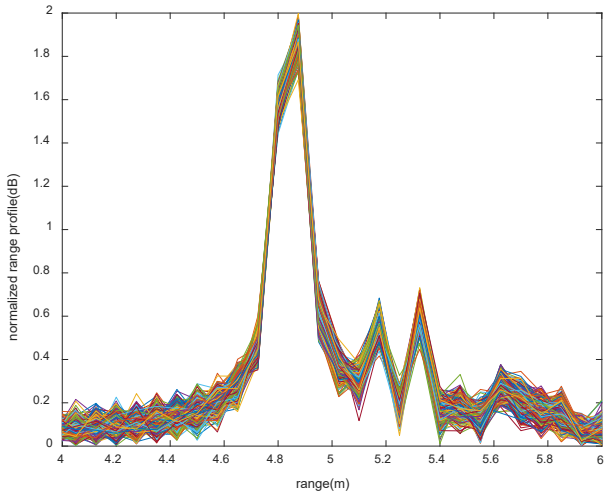
Figure 4.3. (a) Estimation based on OFDM with integer index (b) Estimation based on OFDM with fractional index (c) Comparison of deviations between two estimation methods

4.3 Multiple target measure with fractional step length method

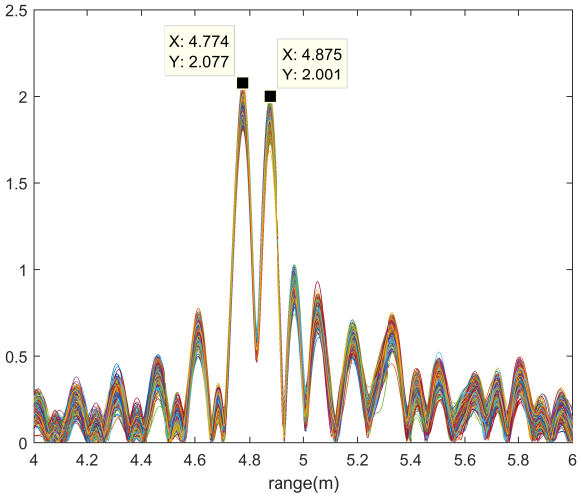
The setup of this measurement is similar as the previous one. Shown in figure 4.4, one metal pillar and one metal plate are used as two target with the distance 5 centimeters.

Figure 4.4. Two targets setup.

The measurement results are shown in figure 4.5. In the integer step length measurement, one peak shows up, which means it cannot be used to detect two target in this case. With the fractional method, two peaks show up, which stand for two targets. Due to the double track transmission, the estimation distance between two targets is 10.01 centimeters, which is as expected.



(a)



(b)

Figure 4.5. Two targets measurement (a) Integer step length estimation (b) Fractional step length estimation

5

Conclusion

In this master thesis work, two parts of work are completed. Firstly, OFDM algorithm is developed in Matlab and tested in 80 GHz equipment. In the simulation, the effect of channel response with frequency offset, phase offset, time delay and phase noise are verified. Two ideal targets are created in the simulation to test the multiple target estimation of the system. In the measurement, an arbitrary waveform generator is controlled by Matlab algorithm to generate the transmitted signal. An advanced oscilloscope is used to acquire the data. The comparison is made between integer estimation method and fractional estimation method. Using the cross-correlation, the system cannot detect the millimeter movement of target. However, in the OFDM system, the resolution of range estimation is improved to less than 2 centimeters. With the novel demodulation method, applying the fractional step length, the range estimation resolution theoretically break through the limitation. In the second part, a basic radar system is designed in DSP builder with Simulink platform and verified on Altera Arria V generation FPGA platform. PLL IP component is used to generate clock for DAC and ADC based on FPGA local oscillator, while RAM IP component is used to store the data with optimal sampling point in each symbol. A top-level design is coded in VHDL for the realization. This system is tested on 60 GHz synchronized transceiver with radar functions and the amplitude modulation is used due to only one channel port. The system is qualified and can be used in Chalmers DSP course as several lab sections.

In the future, the OFDM algorithm can be revised to test multiple targets with different channel response in the measurement. Meanwhile, the accuracy of estimation can be improved by advanced hardware. The basic FPGA radar system with lower symbol rate like 100 kbaud could be developed to test the speaker vibration. In my thesis experiment, no gain is added in the transmitter or receiver antennas. So, next step, it could be one solution to improve SNR for future work.

The most challenging work is to apply the fractional index of OFDM estimation method into FPGA hardware platform. The FPGA should have a very large space for the loop calculation and high sampling rate to provide wide bandwidth. In terms of resolution, if we take 10 GHz sampling rate, 5 GHz bandwidth and 0.1 fractional step length as an example, the range resolution is

$$r_d = 0.1 * \frac{c_0}{2 * BW} = 3 \text{ mm}$$

In this case, the channel response with noise may be one problem to consider as well. High SNR may be needed in this transceiver setup.

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Appendix

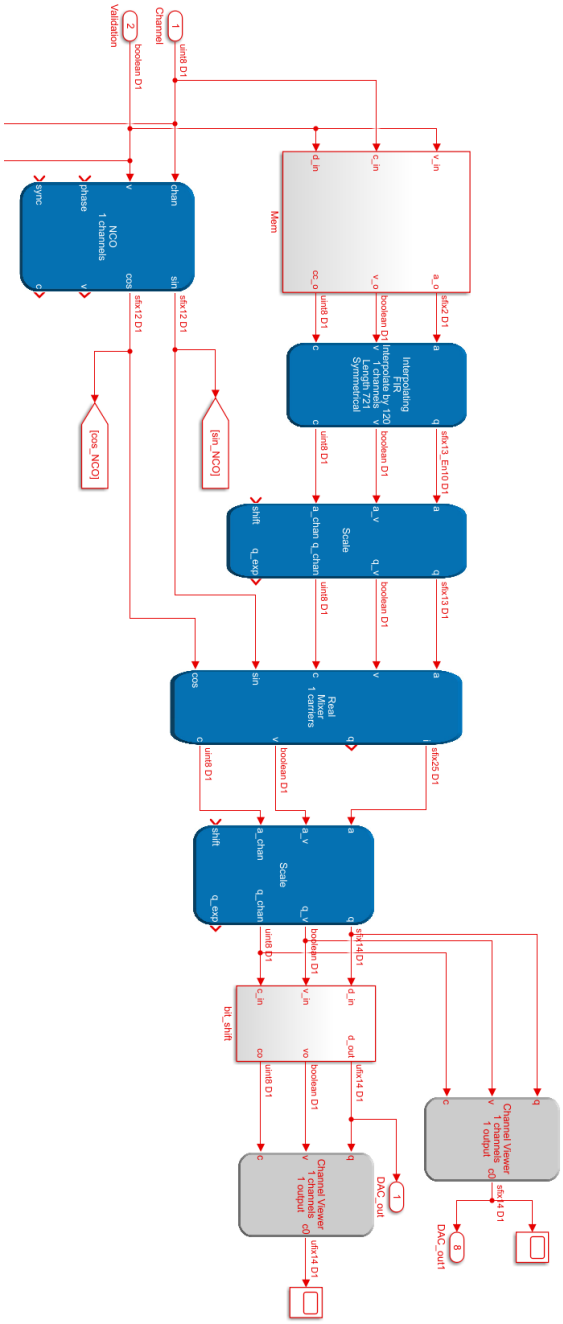

Figure 3.3. Transmitter model in Simulink

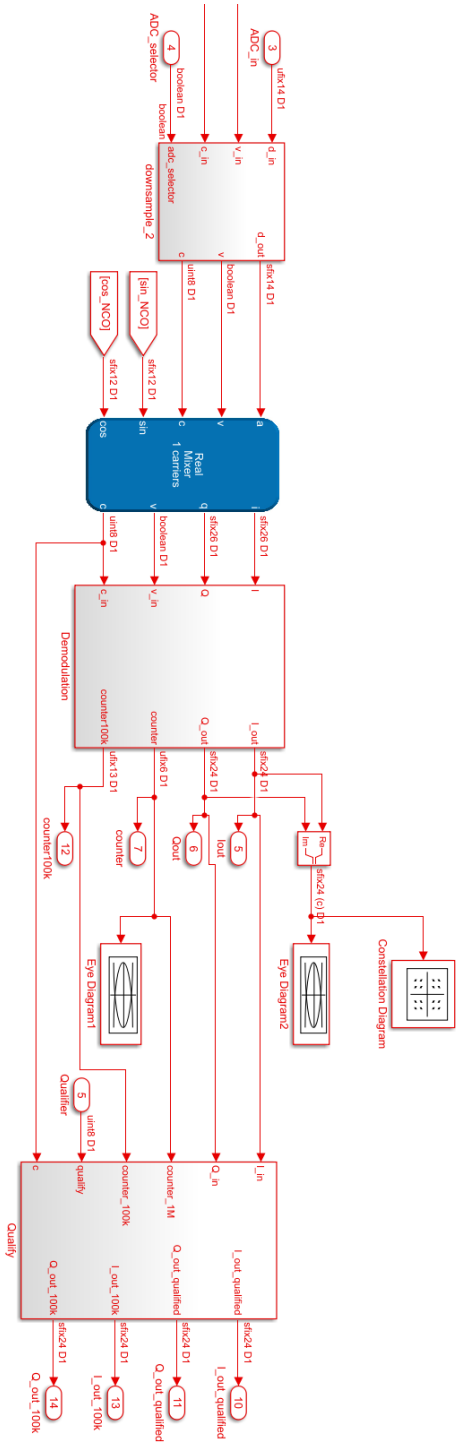

Figure 3.4. Receiver model in Simulink

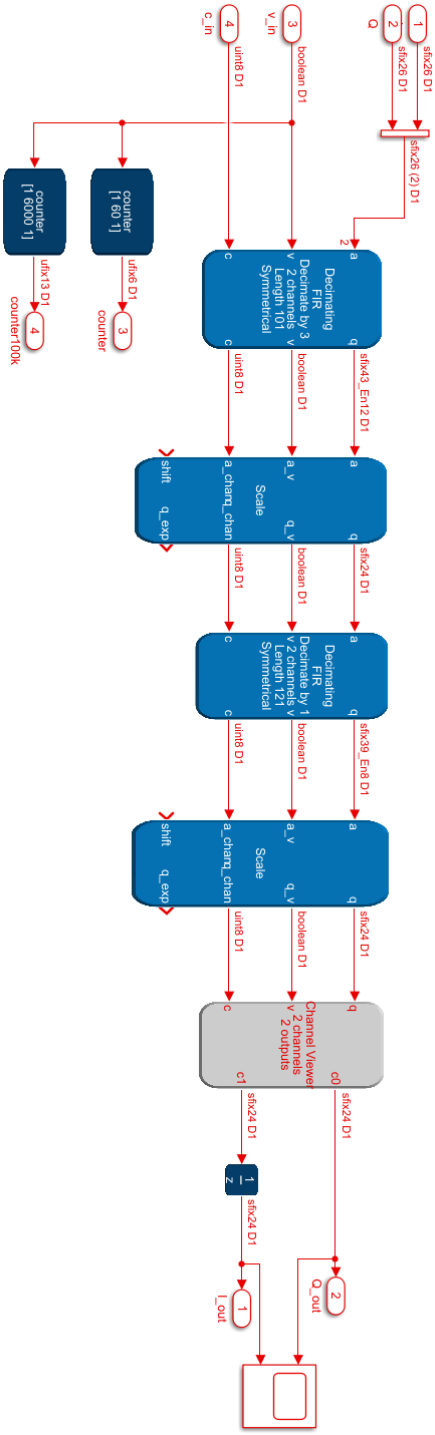

Figure 3.5. Demodulation method