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Energy Efficient High Data Rate RF-DAC based PAM Modulator

A MMIC solution using an InP-based DHBT-process at Millimeterwave Band

Master's thesis in Wireless, Photonics and Space Engineering

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Department of Microtechnology and Nanoscience, MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

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Abstract

To achieve a high-data rate wireless communication system with PAM-4 modulation is tested in this project. A MMIC solution is developed and fabricated with Teledyne Scientific Instruments, US, in their 250nm InP DHBT-process with $f_{\max}$ =650GHz. The simulated system consists of a RF-DAC, a PA, transmitter and receiver antenna with 40dBi gain, an LNA, a VGA and a PD. ADS simulation shows that the system looks promising. The critical part in the system is the RF-DAC based modulator, which is why two different solutions are tested and evaluated.The modulators are designed for an LO frequency of 70GHz, though the plan is to double the frequency when the function of the chosen RF-DAC is confirmed. The reason to not design for an LO frequency of 140GHz straight away is to simplify the testing process. Symbol rate for one of the fabricated modulators is tested and confirmed to support a 40Gbps transmission with a BER of 3.7×10^{-6}, and the energy efficiency is better than 1.2pJ/bit.

Keywords: Energy efficiency, High data rate, Pulse Amplitude Modulation, InP, RF-DAC, DHBT, MMIC, Internet of Things

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Frida Strömbeck, Gothenburg, March 2018

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1
Introduction

In today's fast paced world we are striving for solutions to transfer information faster and faster. For a sustainable future, power efficiency is key. However, there are few willing to sacrifice performance to achieve higher power efficiency. It is therefore a high priority to develop systems that can compete in speed and performance, yet have a low power consumption.

1.1 Background

The exchange of information with someone that is distant, is known as telecommunications. The most primitive form of telecommunications is using smoke signals. Before telecommunications messages had to be sent by a courier.
The history went from mechanical telegraphs in 1794, to transmissions using copper wires in 1837. Heinrich Hertz used electromagnetic waves in 1886. Optical fiber communication over a distance came in 1973.[1] Nowadays means for telecommunication is a given, and most people have access to Internet 24/7.
Both wireless communication using antennas and optical fiber communication are used today, because both systems have different advantages and drawbacks. A fiber optic system can reach far, but a wireless system is much more flexible.
The flexibility of wireless systems combined with smaller devices and antennas makes wireless communication interesting for the future's new short range applications.

1.2 Application

The primary use of wireless communication is telecommunication, such as mobile phone networks, Wireless Local Area Network (WLAN), commonly referred as WiFi, as well as mobile satellite communication for areas where WiFi is unavailable.
Wireless can also be used to replace a cable or fiber for short distances. That application is called cordless. Headphones, printers, keyboards and so on can be connected to your phone or computer etc.
All RADAR(Radio Detection and Ranging) systems rely on wireless signals. Automatic breaking function, parking assistance and automatic car following are only a few of the applications for cars for example.
There are also medical technologies using wireless communication, such as mobile body area networks (MBAN), for monitoring the patients' health.
Wireless transmission of video is also a common application. The higher the quality of the video, the more bits need to be transmitted per second.

Wireless power transfer (WPT) is the application where energy is transmitted from a power source to a device without the use of a wire. Examples include electrical trains, chargers for electrical tooth brushes or smart watches, and smart cards such as SIM cards and credit cards.
It is clear that high data rate connectivity even at a small distance is urgently needed. Since most mobile devices are battery driven, power consumption becomes a major consideration. Further more, a high data rate wireless link with decrease the transmission time, thus reduce the on-time of the transceiver which enables a longer lifetime of the device.

1.3 Problem statement and description

What limits the symbol rate of the transmission is the response time of the components making up the transmitter/receiver as well as the noise in the channel. There is a theoretical limit of the maximum bit rate that can be transferred. In practise, the performance is always lower. The limit is given by Shannon's theorem;[2]

$$C = B\log_2(1 + \frac{S}{N}) \tag{1.1}$$

where C is the channel capacity, B is the bandwidth, S is the signal power and N is the noise power.
If the response time of the components is limited the data rate can be increased by transferring more data per symbol. A common way to do this is to change the phase of the signal in combination with the amplitude. The disadvantage of this solution is that it requires synchronisation (carrier recovery) between the transmitter and the receiver, so a large portion of the power consumption is spent on that. It also requires a more complicated circuit.
In the circuits designed today there is a trade-off between a high data-rate and a high energy efficiency. The designs are usually optimised for only one of those.
Transceivers that uses on-off keying(OOK) has many advantages, such as a low DC power consumption and a small chip area due to its simplicity.[20] For cases when the bandwidth is not extremely limited as a result of frequency allocation, OOK transceivers are cost efficient. There is one big downside; the low spectral efficiency.

1.4 Purpose and Aim

In this work, MMIC(Microwave Monolithic Integrated Circuit)-solutions for energy efficient, high data-rate wireless communication will be analysed and designed.
A MMIC-process using InP(Indium Phosphide)-based DHBTs(Double Heterojunction Bipolar Transistor) with $f_{\max} = 650$GHz, and a back-end with 4 metal layers will be used for the active and passive components.
The process using InP-based DHBTs is chosen due to the wide bandwidth and high power handling capability, as well as a low noise figure. The technology ideally suited for next generation millimeterwave, mixed-signal and digital integrated circuits.

The transmitter is aimed to be designed in the frequency band 110-170 GHz, also known as the D-band. It will be optimised for highest modulation bandwidth and RF-bandwidth, in other words aiming for the highest bit-rate. However, to verify the function of the transmitter and simplify testing it will first be designed and fabricated for a frequency band around 70GHz (E-band).
Important design parameters are RF-bandwidth, IF-bandwidth, noise figure, chip-area, bit-rate, energy-per-bit, and DC-power consumption.
The suggested solution to limit the power consumption is to use Pulse Amplitude Modulation (PAM). In some cases (unipolar), no synchronisation between the transmitter and receiver is needed using this modulation technique. Further more, the design can be kept simple.
The design is fabricated at Teledyne Scientific Instruments, US, in their 250nm DHBT-process with $f_{\max}$ =650GHz.

1.5 Thesis outline

First the theory of the development of the circuit will be presented. This includes a deeper explanation of pulse amplitude modulation, followed by an overview of the circuit where the design parameters are established. A link budget of the system is then estimated, as well as a comparison with previous similar work made by others of the system and the critical components.
The tools to create and simulate the performance of the circuits is reviewed as well as the technology.
The desired functions of the modulator is explained, and different solutions to achieve those qualities are presented.
The results of this work includes the layouts of the circuits, the performance of the circuits, and the final circuit specifications.
A discussion of the similarities and differences between expected results, actual results and results of others will follow. The methods and uncertainties will be reviewed and some future research ideas and possibilities for improvement will be presented.
The report will be wrapped up with a conclusion.

2
Theoretical Background

2.1 Typical Setup

The basic transmitter/receiver system consists of a modulator followed by a Power Amplifier(PA) and an antenna. The receiver antenna is followed by a Low Noise Amplifier(LNA), and a demodulator. A simple figure can be seen in figure 2.1.

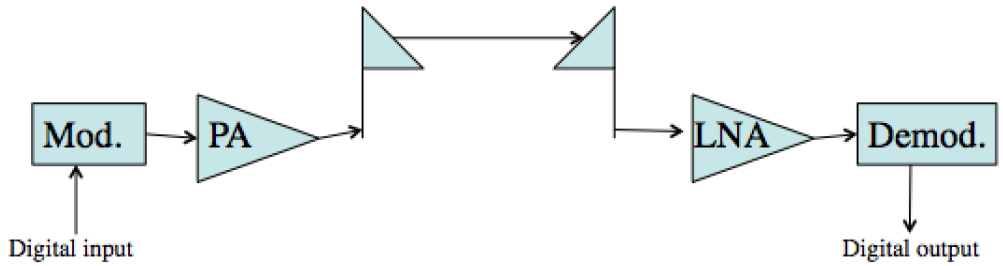


Figure 2.1: A basic transmitter and receiver.

Friis' transmission equation helps calculating the amount of power that gets transmitted from one antenna to the other.

$$P_r = \frac{G_t G_r P_t}{\text{FSPL}} \tag{2.1}$$

P_r is the received power, P_t is the transmitted power, G_t is the antenna gain of the transmitting antenna, G_r is the antenna gain of the receiving antenna, and $FSPL$ is the free space path loss. The free space path loss can be calculated using;

$$\text{FSPL} = (\frac{4\pi df}{c})^2 \tag{2.2}$$

where d is the distance, f is the frequency and c is the speed of light.[19] What limits the transmission is usually noise, both thermal noise from the receiver antenna and noise that gets added inside the components.
The thermal noise power at the input is given by;

$$N_0 = kTB \tag{2.3}$$

where k is Boltzmann's constant, T is the temperature of the antenna (usually room or outdoor temperature), and B is the bandwidth of the signal.[19]

Signal to noise ratio (SNR) is common measurement within wireless communications. It is defined as;

$$\text{SNR} = \frac{P_{in}}{N_0} = \frac{E_b}{n_0}\frac{R_b}{B} \tag{2.4}$$

where $N_0 = n_0 B$ is the noise power and $E_b R_b$ is the digital signal power. Further more, $\frac{R_b}{B}$ is the spectral efficiency.
The noise that is contributed by the component makes the SNR lower at the output of said component. The change in SNR is defined as the noise figure (NF) of the component.[19]

$$NF = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \tag{2.5}$$

For a cascaded circuit the total noise figure is given by Friis' formula for noise;

$$NF = F_1 + \frac{F_2 - 1}{G_1} \tag{2.6}$$

where F_1 is the noise figure of the first component, G_1 is the gain from the first component, and F_2 is the noise figure from the second component.[19]
The symbol error rate depends on the SNR. A higher SNR gives a smaller symbol error rate.
A symbol can contain one or many bits, depending on the spectral efficiency of the modulation format.

2.2 Choice of Modulation

The most commonly used modulation techniques are Frequency Shift Keying (FSK), Phase-Shift Keying (PSK), Amplitude Shift Keying (ASK) and Quadrature Amplitude Modulation (QAM). FSK is mostly used for amateur radio, caller ID and emergency broadcasts. The most common modulation using phase is Quadrature Phase Shift Keying (QPSK) that uses 4 different phases. When only 2 different phases are used it is called Binary Phase-Shift Keying (BPSK). QPSK and BPSK has the same bandwidth and bit error rate though, which makes QPSK the more popular choice since it has a higher spectral efficiency.
On-Off keying (OOK) is the most simple modulation based on amplitude shift keying. No carrier recovery is required, so the receiver (Rx) structure can be kept simple. The drawback with OOK is the low spectral efficiency.
QAM is a mix between amplitude and phase modulation. Spectral efficiency increases with the order of QAM, but higher SNR is needed to reach the same BER. QAM requires carrier recovery which means that it has to have a more complex Rx structure.
Pulse Amplitude Modulation (PAM) has the same benefits as OOK. It requires no carrier recovery. The advantage that PAM has to OOK is that the spectral efficiency can be higher. If 4 levels are used, 2 bits are transmitted, which is double that of OOK.

2.2.1 Pulse Amplitude Modulation

Pulse Amplitude Modulation(PAM) can be either unipolar or bipolar. For a unipolar signal all levels are non-negative, while a bipolar signal has evenly distributed levels where half of them are negative and half of them are positive. A bipolar signal uses a single side band, but requires carrier recovery. A unipolar signal can use both side bands, and a simple power detector is sufficient to demodulate the signal. In this project unipolar PAM is used.
The transmitted unipolar PAM signal over one symbol period ($0 \leq t \leq T$) is given by;

$$s_i(t) = A_i g(t) \sin(2\pi f_c t) \tag{2.7}$$

where $A_i = (i-1)d, i = 1, 2, 3...M$ for unipolar M-PAM, d is the amplitude separation distance between different levels, $g(t)$ is a real-valued pulse shaping function, and f_c is the carrier frequency.
The drawback with PAM is that it is sensitive to amplitude noise and requires a higher SNR than frequency or phase modulation. [21] Low noise material is definitely a game changer when it comes to designing circuits for PAM.
The symbol error probability for coherent bipolar M-PAM is given by;

$$P_s = \frac{2(M-1)}{M} Q\left(\sqrt{\frac{6\gamma_s}{M^2-1}}\right) \tag{2.8}$$

where $\gamma_s = \frac{\bar{E}_s}{N_0} \approx \frac{E_b}{N_0} \text{Log}_2(M)$, E_s is the average energy per symbol, and $Q(\sqrt{2}x) = \frac{\text{erfc}(x)}{2}$. Note that erfc is referring to the complementary error function.[22]
The symbol error probability for coherent unipolar M-PAM is given by;

$$P_s = \frac{2(M-1)}{M} Q\left(\sqrt{\frac{3\gamma_s}{2M^2-3M+1}}\right) \tag{2.9}$$

In figure 2.2 the symbol error probability for both unipolar and bipolar M-PAM is plotted. Unipolar PAM requires a higher signal to noise ratio, but requires a much lower DC power consumption.[22]
To achieve a symbol error probability below 10^{-5} the E_b/N_0 ratio has to be larger than 18dB for unipolar PAM-4. For unipolar PAM-8 it has to be larger than 23.5dB, so the difference is 5.5dB.

2.3 Overview of System

When designing parts of a system, it is important to have an understanding of the system as a whole. It is from the analysis of the system, the requirements for each part can be estimated and established.
System parameters to estimate:

- Antenna gain (G_t and G_r)
- Output power from transmitter
- Noise temperature
- Distance of transmission

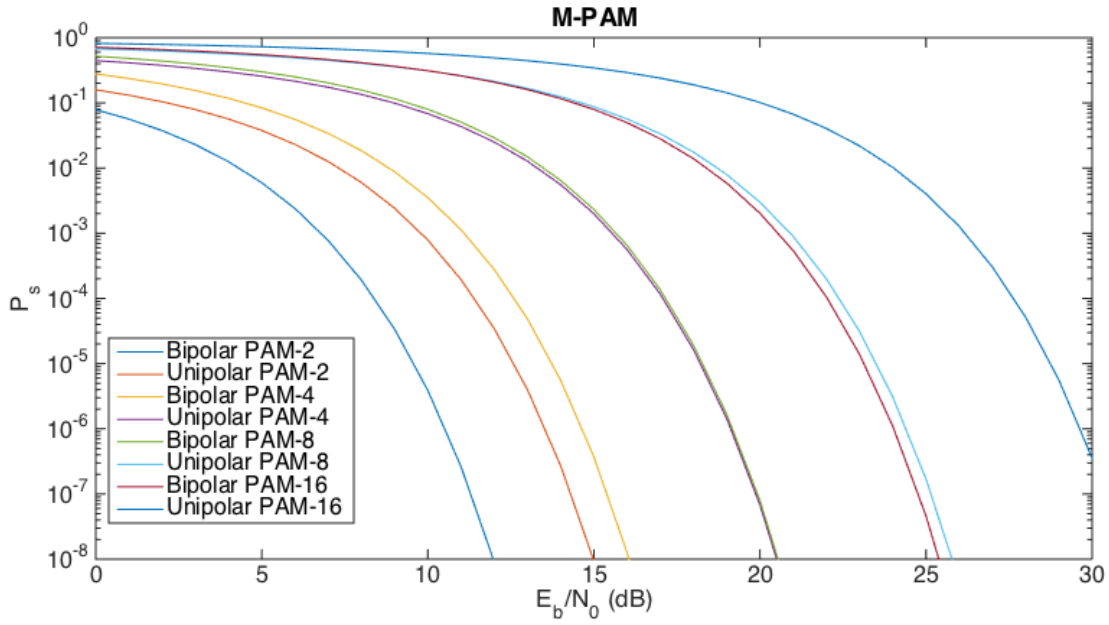


Figure 2.2: Symbol error probability for coherent M-PAM.

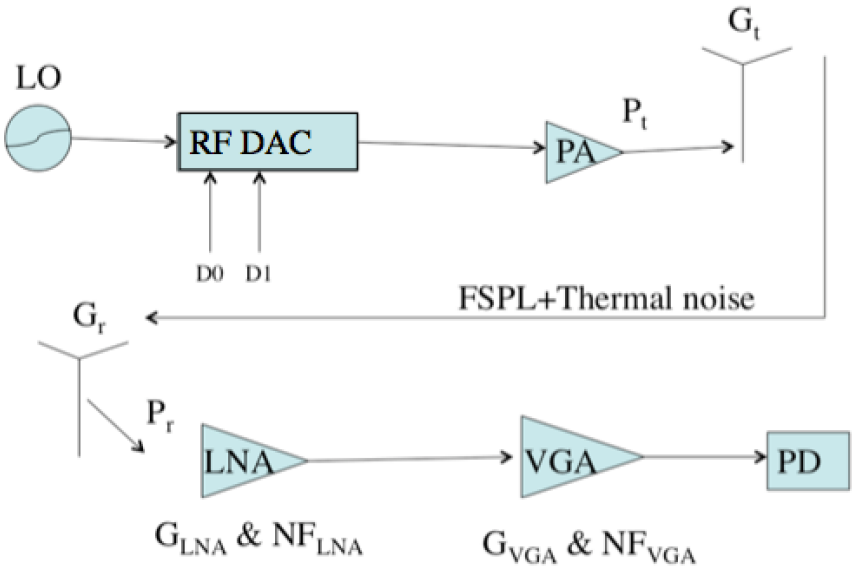


Figure 2.3: The parameters for the transmitter and receiver link.

- LNA gain
- Noise figure LNA
- VGA gain

The antennas that were to be used were already specified and have an antenna gain of $G_{\text{antenna}} = 40\text{dBi}$. The noise temperature is based on room temperature ($\approx 300\text{K}$). The reason to include a variable gain amplifier (VGA) is to control how much power get to the power detector. Further more, the input power will vary with distance changes between transmitter and receiver. The free space path loss

(FSPL) is 135dB for 1000 meters and 115dB for 100 meters at 140GHz.
The estimation of the LNA gain and noise figure were based on previous work [4]. Their LNA had a 20dB gain and a noise figure of 9dB, which means that it should be no problem designing one with a 30dB gain and maximum a 10dB noise figure, but possible to make smaller.
The saturated output power of the power amplifier is based on previous work from Teledyne Scientific Company [23], using the same technology. They achieve an output power of more than 19dBm, at 96-120GHz, with a power added efficiency (PAE) of approximately 20%. PAE is defined as;[24]

$$\mathrm{PAE} = \frac{P_{\mathrm{RF,out}} - P_{\mathrm{RF,in}}}{P_{\mathrm{DC}}} \tag{2.10}$$

Based on these estimations a link budget was done. See figure 2.4.

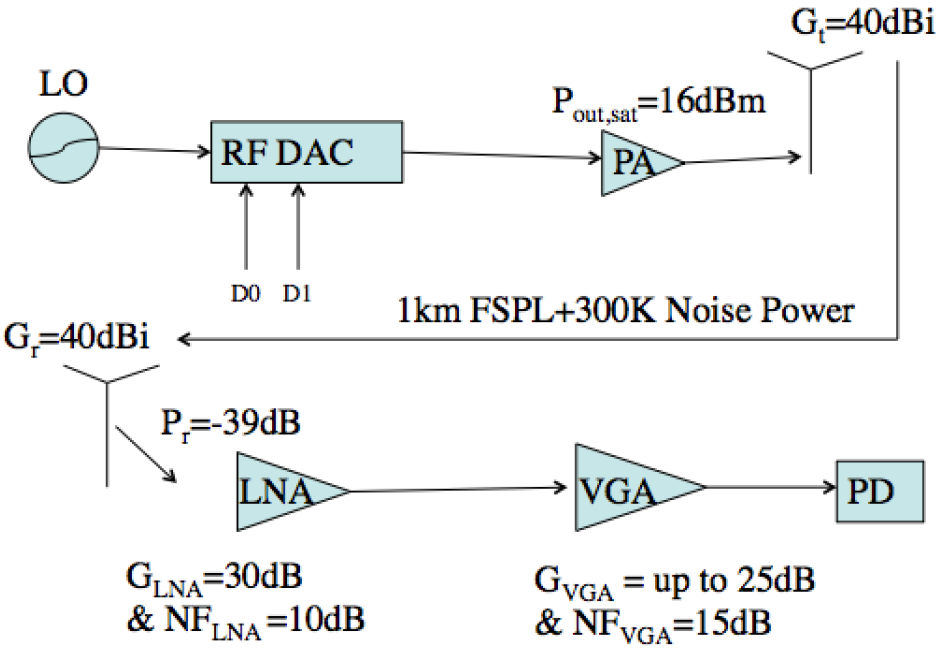


Figure 2.4: The suggested transmitter and receiver link with a center frequency of 140GHz.

2.4 Link Budget

The link budget was done for both a center frequency of 140GHz and 70GHz. The reason for 70GHz is to simplify the measurements of the circuit. A proof-of-concept system will be created first in E-band ($f_c = 70$GHz). When the functionality of the system is confirmed it will move up in frequency to D-band ($f_c = 140$GHz).
A signal to noise ratio of 19dB is theoretically enough for a low bit error rate using unipolar PAM-4.

Table 2.1: Link Budget-(from transmitter to receiver)

Parameter	$f_c = 140$GHz	$f_c = 70$GHz
P_t	16dBm	16dBm
G_t	40dBi	40dBi
$\text{FSPL}_{1\text{km}}$	-135dB	-129dB
G_r	40dBi	40dBi
P_r	-39dBm	-33dBm
$(N_0)_{40\text{GHz},300\text{K}}$	-98dB = -68dBm	-71dBm
SNR_{in}	29dB	38dB

Table 2.2: Link Budget-(in receiver)

Parameter	$f_c = 140$GHz	$f_c = 70$GHz
P_r	-39dBm	33dBm
$(N_0)_{40\text{GHz},300\text{K}}$	-98dB = -68dBm	-71dBm
G_{LNA}	30dB	30dB
NF_{LNA}	10dB	10dB
G_{VGA}	up to 25dB	up to 25dB
NF_{VGA}	15dB	15dB
$P_{\text{in,PD}}$	up to 16dBm	up to 16dBm
NF_{tot}	10+(31.6-1)/1000 $\approx$ 10 = 10dB	10dB
$\text{SNR}_{in,PD}$	29-10=19dB	38-10=28dB

2.5 Critical Component and Previous work

The critical component in the system is the RF-DAC. There are examples of previous work that include amplifiers that achieve the performance (specified in the link budget) that is required for this work.
In table 2.3 similar work of entire systems, D-band transmitter & receiver, is presented. Work done in E-band can be seen in table 2.4.

Table 2.3: Comparison with similar work in D-band (transmitter & receiver)

Technology	**DC Power Consumption**	**Size (mW)**	**Gbps (mm^2)**	**Energy Eff. pJ/bit**	**Ref.**
40nm CMOS	98.4 (17.9+80.5)	0.32(Tx) 1.68(Rx)	10	9.8	[3]
250nm InP DHBT	357 (165+192)	1.17(Tx) 1.17(Rx)	40	8.9	[4]
250nm SiGe HBT	1100 (610+490)	0.45(Tx) 0.4(Rx)	20	55	[5]
250nm InP DHBT	357 (165+192)	1.17(Tx) 1.17(Rx)	48	7.4	[6]
40nm CMOS	209 (77+132)	0.44(Tx) 1.35(Rx)	11	19	[7]

Table 2.4: Comparison with similar work in E-band (transmitter & receiver)

Technology	**DC Power Consumption**	**Size (mW)**	**Gbps (mm^2)**	**Energy Eff. pJ/bit**	**Ref.**
130 SiGe BiCMOS	2000 (1350+650)	9.7(Tx) 6.1(Rx)	> 1	NA	[8]

2.5.1 RF-DAC

Table 2.5: Comparison with similar work (Modulators)

Technology	**Frequency (GHz)**	**Data Rate (Gbps)**	**Energy Eff. pJ/bit**	**Ref.**
50nm InGaAs HEMT	113	25	0.38	[9]
65nm CMOS	77	12	0.75	[10]
0.25μm InP DHBT	100-150	14	3.35	[11]
50nm mHEMT	87.8-98.2	18	5.6	[12]
65nm CMOS	80	12	4.5	[13]
65nm CMOS	57-66	11.5	1.1	[14]

3
Circuit Design

The main concept of the system was to create a Radio Frequency-Digital to Analog Converter (RF-DAC) that is using pulse amplitude modulation (PAM).
All simulations were done by utilising Advanced Design System (ADS) that is provided by Keysight EEsof Electronic Design Automation (EDA). More information can be found at their website [25].

3.1 Technology

Teledyne Scientific Companies Indium Phosphide (InP) heterojunction bipolar transistor (HBT) process TSC250 is an advanced bipolar process that relies on submicron transistor scaling to achieve state-of-the art device performance.[26] Devices in the technology offer typical RF figures-of-merit (f_t and $f_{\max}$) of 350/600 GHz while maintaining a common-emitter breakdown voltage (BV_{CEO}) of greater than 4V. The wide bandwidth and high power handling capability of the devices make the technology ideally suited for next generation millimeter-wave, mixed-signal and digital integrated circuits.
The technology has 4 metal layers, M1,M2,M3 and M4. The dielectric constant of the interlayer dielectric (BCB) is estimated to be $\epsilon_r = 2.7$. A cross-section drawing can be seen in figure 3.1.
Thin-film resistors are formed on a thin layer of Silicon Oxide (SiO) that sits on the InP substrate. Metal-insulator-metal (MIM) capacitors are formed between M1 and the capacitor metal (CAPM) with a 200nm Silicon Nitride (SiN) dielectric layer in between.
Each layer has a maximum current density that cannot be exceeded. Metal 1 has 4mA/μm, metal 2 and 3 has 5mA/μm, metal 4 has 15mA/μm and the thin-film resistor has 1mA/μm. The VIAs connecting different layers also has limits for the current.
The design kit includes two types of transistors; standard devices, and single-sided collector contact devices. The single-sided collector device has a collector contact on only one side of the base mesa. This results in approximately a 2x increase in the collector resistant, but reduces the footprint of the transistor by approximately 30%. The estimated safe operating area for the devices can be seen in 3.2.
Usually metal 1 or metal 2 is used as the ground layer. For this project metal 2 was used as ground layer, while metal 1 was used for DC bias. That meant that RF and DC connections did not cross each others path or disturb each other.

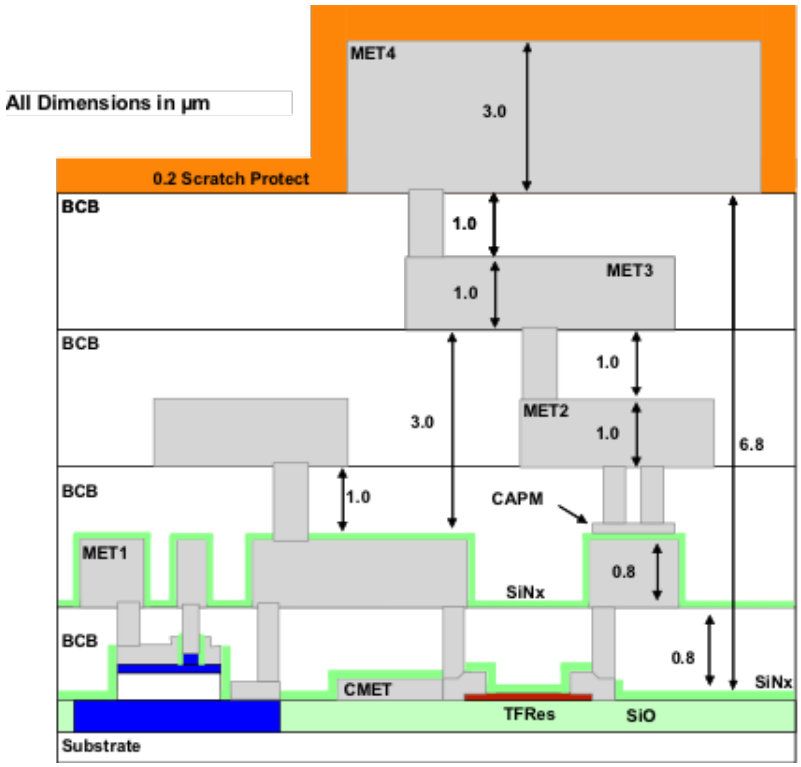


Figure 3.1: Representative cross-section of TSC250 IC technology. Drawing is not to scale. *Credit: Teledyne Scientific Company*

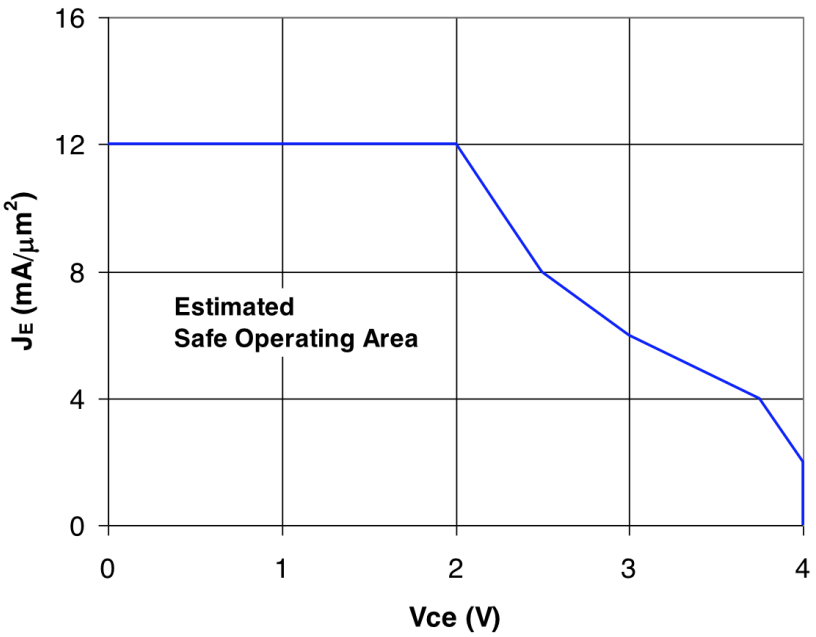


Figure 3.2: Estimated safe operating area for 250nm HBT devices in common-emitter configuration. The current density is given by $J_E = \frac{I_C}{(0.25 \times \text{Emitter length})}$. *Credit: Teledyne Scientific Company*

A design kit for TSC250 was available for ADS to simulate the predicted performance.

3.2 Design Flow

The system has a few different parts with different functions.

1. RF-DAC
2. PA
3. Transmitting antenna
4. Receiving antenna
5. LNA
6. VGA
7. PD

The required performance for each part can be estimated through a link budget. ADS ptolomy simulation is also useful to get an idea about how different parameters affect the system.

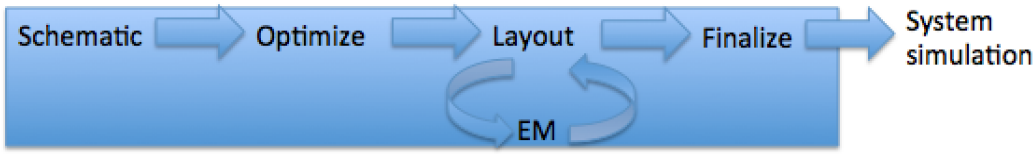


Figure 3.3: The design steps in ADS.

When the performance for each part was decided, the parts were designed one by one. The design steps of each part can be seen in figure 3.3.
A schematic for each part was first decided. The parameters for the components of each part were changed to optimise the performance. The layouts were then created using the optimised schematics as a foundation. Input and output pads as well as DC pads needs to be placed out in a way that minimises the area, but still is practical for the testing and schematic. To see how the lines and components affect each other EM-simulations were done. The layout then had to get adjusted and new EM-simulations were done until a good performance was reached. To finalise the layout, it also had to comply to all the design rules that Teledyne required to be fulfilled to be able to produce the MMIC. Each part was then placed in a system simulation to see that the whole system worked together. To improve the performance adjustments were done in the schematic or the optimisation, which meant that the other steps had to be made too.

3.3 RF-DAC

3.3.1 Design Concept

The purpose of a RF-DAC(digital-to-analog converter) is to modulate the carrier signal to represent the information that is to be transmitted. The modulation that was chosen for this project was Pulse Amplitude Modulation(PAM). The advantages of unipolar PAM is that no synchronisation (signal recovery) between transmitter and receiver is required. The most simple form of Pulse Amplitude Modulation(PAM) is On-Off-Keying(OOK). OOK can be seen in figure 3.4.

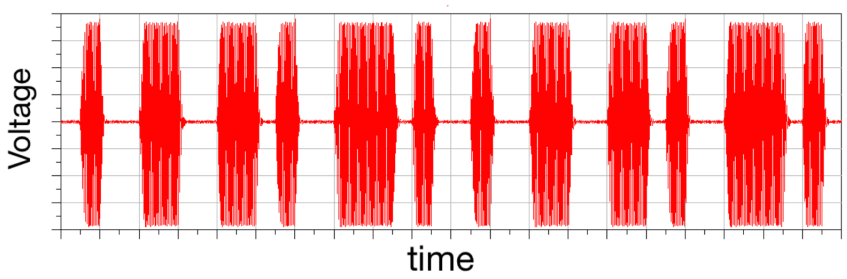
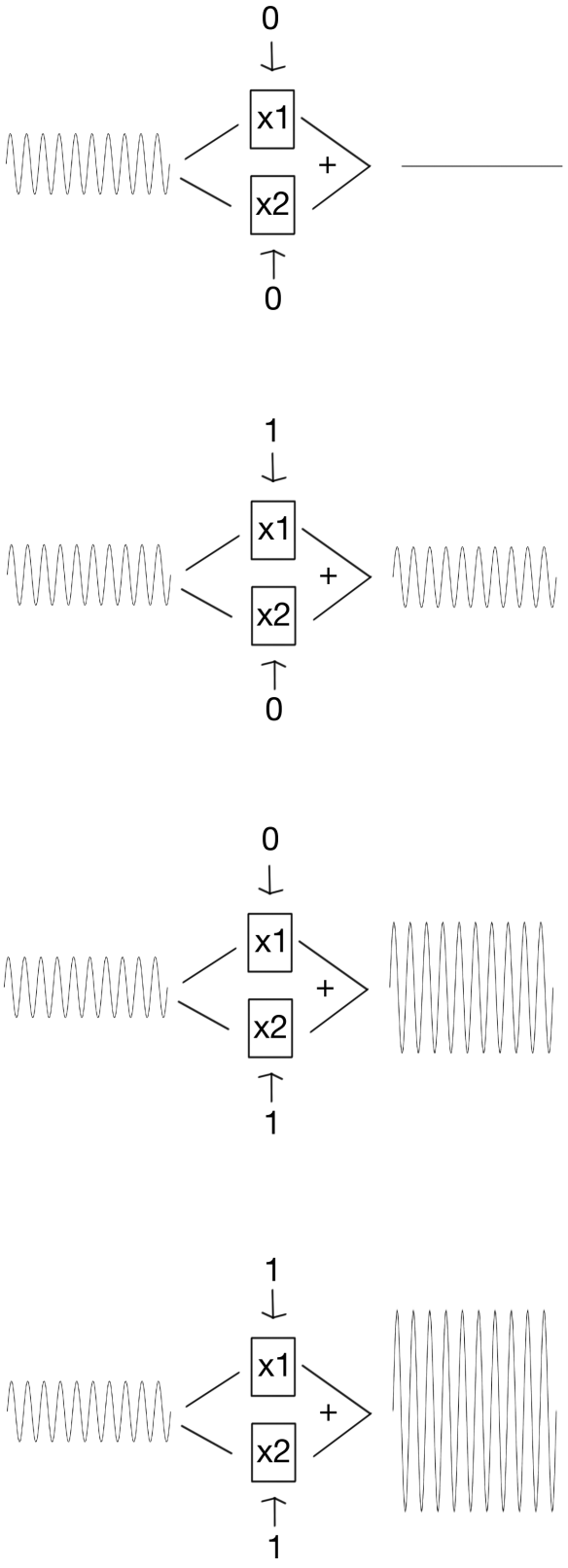


Figure 3.4: The most simple form of PAM is OOK. A transmitted signal represents "1", while no transmitted signal is "0".

PAM-4 has 4 different power levels while PAM-8 has 8 different levels, and so on.

The four different levels of PAM-4:



The idea was to create two switches. One of them requires an output that is double that of the other. The data input port that gives the strongest output power is called the Most Significant Bit (MSB), while the weaker one is called the Least Significant Bit (LSB). The output signals need to be combined in phase, to avoid cancelling each other. The input signal needs to be the same for both of them. The easiest way to achieve that is to divide one signal equally to supply both switches from the same LO(Local Oscillator).
For high-speed solutions current steering is the most commonly used technique to create an "On-Off"-switch. This can be done by using a differential pair.[17]
One way to achieve the different power levels is to use a resistive ladder to combine the output from the identical switches.[16] Another is to combine the output from two different switches, one with an amplification that is double the other. To avoid losing too much power (due to dissipation in the resistors) the second solution is used in this work.
Two different schematics for switches were selected, one differential pair solution and one cascode solution. The schematics can be seen in figure 3.5 and 3.6. At the LO input and the Data input an extra transistor stage was added to work as a buffer, a so called emitter follower.

Differential Pair (V1)

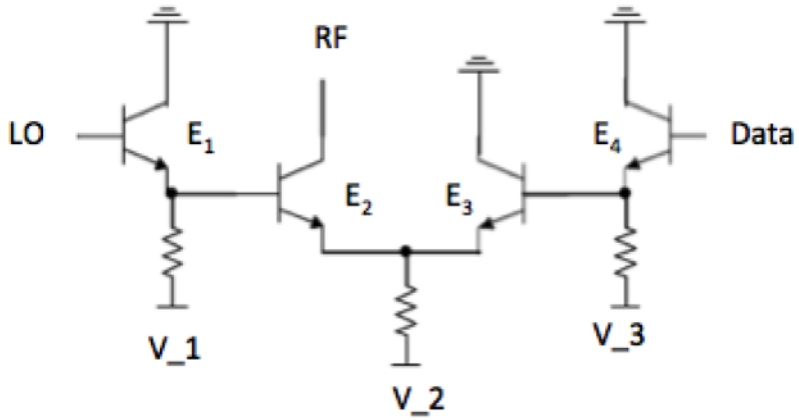


Figure 3.5: The schematic of one switch with the differential pair solution.

The design topology is based on using an emitter-coupled pair (ECP) as an adjustable attenuator. The output amplitude is controlled by the data input. When a high data input voltage is applied, the local oscillator (LO) input is heavily attenuated, which results in a low power RF output. The ECP structure allows fast switching, which is essential for high data rate transmission. High linearity is also one of the advantages of this structure. The ECP structure enables a low power operation.
The LO input signal is given at the base of E1 which is configured as emitter follower. When data bit '1' (0 V as logic '0' and 0.3 V as logic '1') is presented at the base

of E4 (data input port), it will steer the current away from E2 therefore reduce the output amplitude.

Cascode (V2)

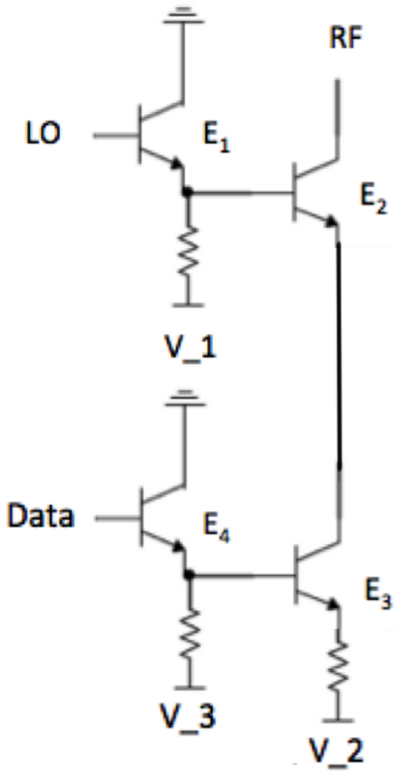


Figure 3.6: The schematic of one switch with the cascode solution.

The topology used in this design is based on two cascoded transistors. A simplified version of the schematic can be seen in figure 3.6. Transistor E1 as well as E4 are configured as emitter followers. The LO input signal is fed at the base of E1, and the data input signal at the base of transistor E4. Transistor E2 and E3 are the cascoded transistors. The collector of E3 is connected to the emitter of E2. When logic '1' (-0.4V) is presented at the data port, the voltage at the collector of E3, thus the voltage at the emitter of E2 changes. The new bias turns off the transistor, and the RF output becomes limited.

3.3.2 Schematic

Differential Pair (V1)

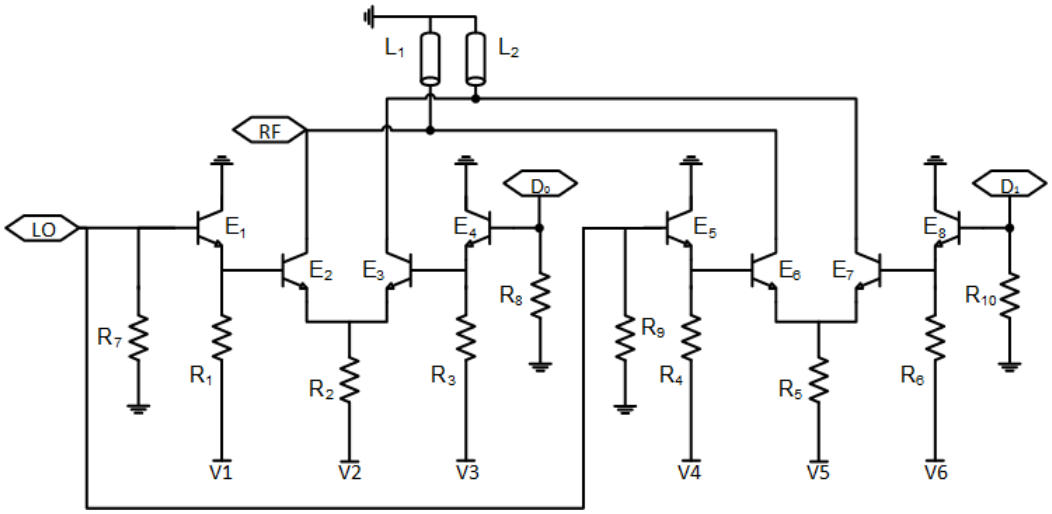


Figure 3.7: The full schematic of the differential pair RF-DAC. The value of each component can be seen in table 3.1.

Table 3.1: The values for each component in figure 3.7.

Resistors	Ω	Emitter length	μm	DC	V	TL length	μm
R1	50	E1	3	V1	-1	L1	240
R2	50	E2	8	V2	-2.1	L2	5
R3	50	E3	8	V3	-0.75		
R4	50	E4	3	V4	-1		
R5	50	E5	3	V5	-1.8		
R6	50	E6	3	V6	-0.75		
R7	100	E7	3				
R8	50	E8	3				
R9	100						
R10	50						

Cascode (V2)

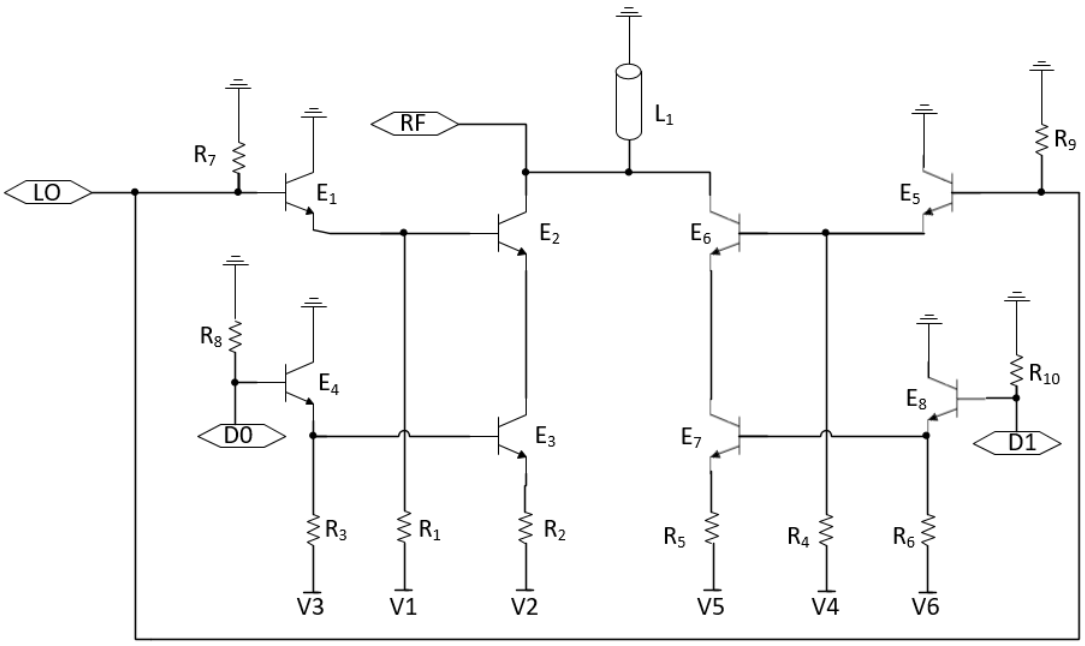


Figure 3.8: The full schematic of the cascode RF-DAC. The value of each component can be seen in table 3.2.

Table 3.2: The values for each component in figure 3.8.

Resistors	Ω	Emitter length	μm	DC	V	TL length	μm
R1	50	E1	5	V1	-0.8	L1	210
R2	50	E2	3	V2	-1.8		
R3	50	E3	3	V3	-1.4		
R4	50	E4	3	V4	-0.8		
R5	50	E5	5	V5	-2		
R6	50	E6	8	V6	-1.7		
R7	100	E7	8				
R8	50	E8	5				
R9	100						
R10	50						

3.3.3 Circuit Layout

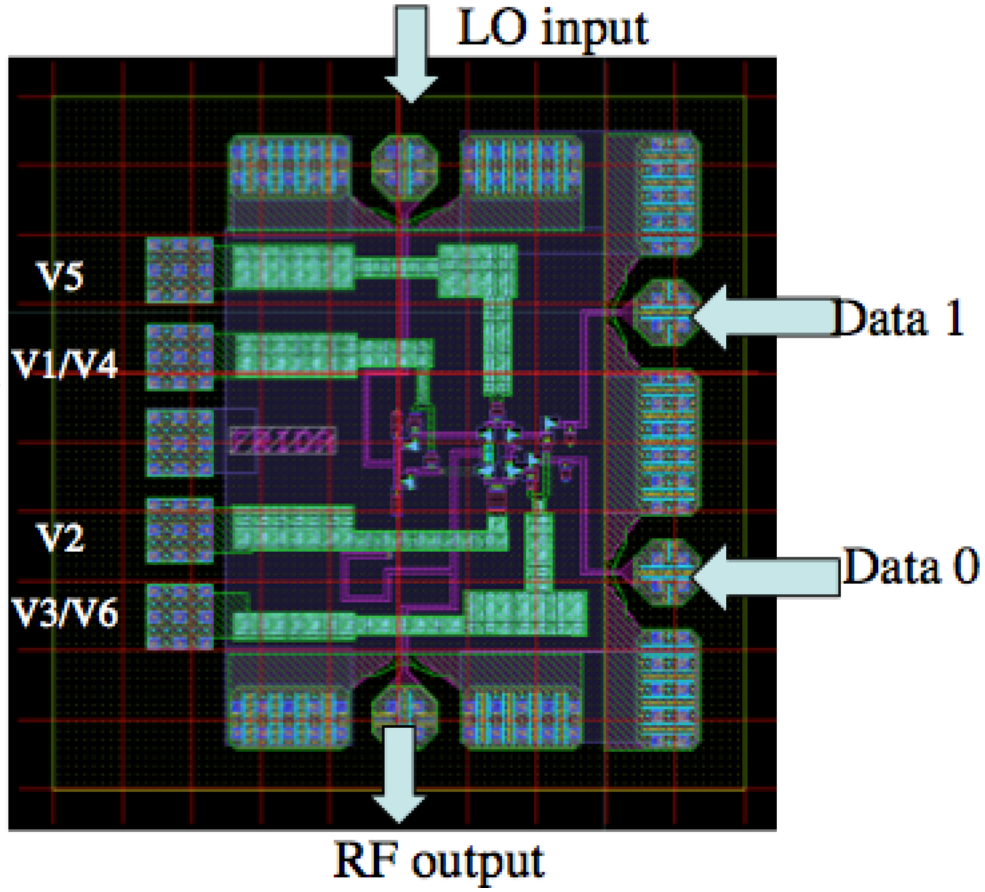


Figure 3.9: The final layout of the differential PAM-4 RF-DAC. The size is 800x800μm.

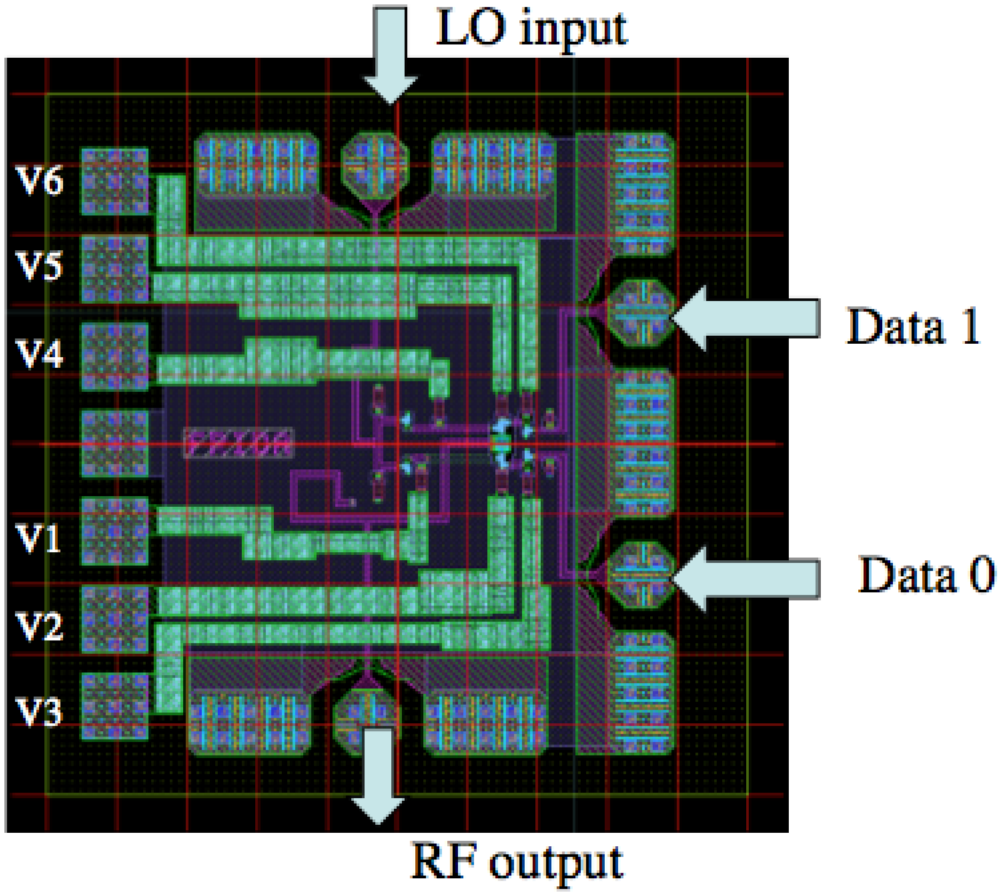


Figure 3.10: The final layout of the cascode PAM-4 RF-DAC. The size is 800x800μm.

The designs were fabricated at Teledyne Scientific Instruments, US, in their 250nm InP DHBT-process.
The total area for each modulator is 0.64mm^2.

4
Results

The system has many different parameters. To investigate how one part in the system works, the function of the other parts need to be known. That is why it is unwise to test two new and unknown circuits at the same time. To be able to test the function and behaviour of the converters with the exciting instruments at Chalmers a decision was made to design the RF-DAC at a lower frequency first. The center frequency for the "proof-of -concept"-circuits are 70/75GHz. Further more, the expected symbol rate is therefore lowered from 40GBd to 20GBd.
For the "cascode" RF-DAC simulated results will be presented. However, for the "differential pair" RF-DAC real measurements have been done.

4.1 V1:PAM-4 RF-DAC (differential pair)

The "differential pair"-RF-DAC was tested both in frequency domain and time domain.

4.1.1 Frequency Domain Measurement

In frequency domain, measurements were done using Anritsu VectorStar Vector Network Analyser (VNA) ME7838A. The LO-input frequency was swept from 30 to 130 GHz at a constant -5 dBm power level. The input power at the data ports were put to different digital settings.The measured output power versus frequency is shown in Fig. 4.1. The 3-dB bandwidth is between 60GHz and 90GHz. At 75 GHz, the modulator gives maximum -6.2 dBm output power under 0 dBm LO drive. With different input bits the output power is attenuated, comparing the output power difference between data '11' and data '00' are modulated, it can be seen that this modulator yields 10-dB dynamic range (DR) between 30-70 GHz.
The matching at the LO port (denote as S11) and the output matching at the RF port (denote as S22) are measured using the same setup. The measurement result is plotted in Fig. 4.2.
Simulation result at LO=75 GHz is also given in Fig. 4.3, where MSB (D0) voltage is swept with different LO driven power. The output power level is monitored and plotted.

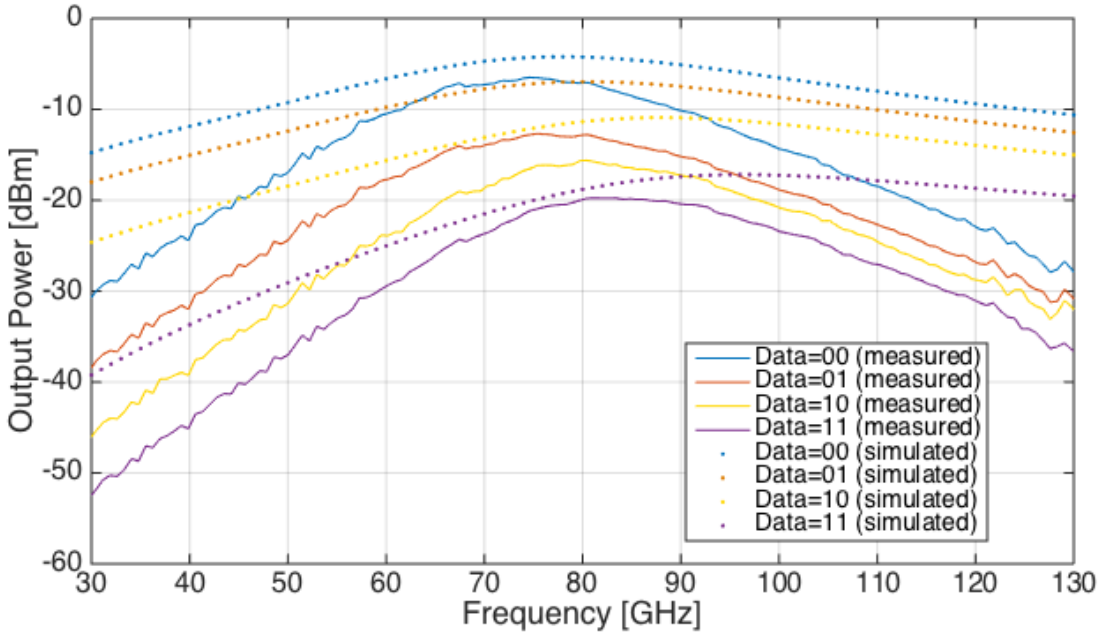


Figure 4.1: Measured output power at different frequencies with different digital input. The dotted lines are simulated values. It can be seen that the simulated values have a wider 3-dB bandwidth compared to the real measurements. This could be explained by the limited bandwidth of the probes used during the measurements.

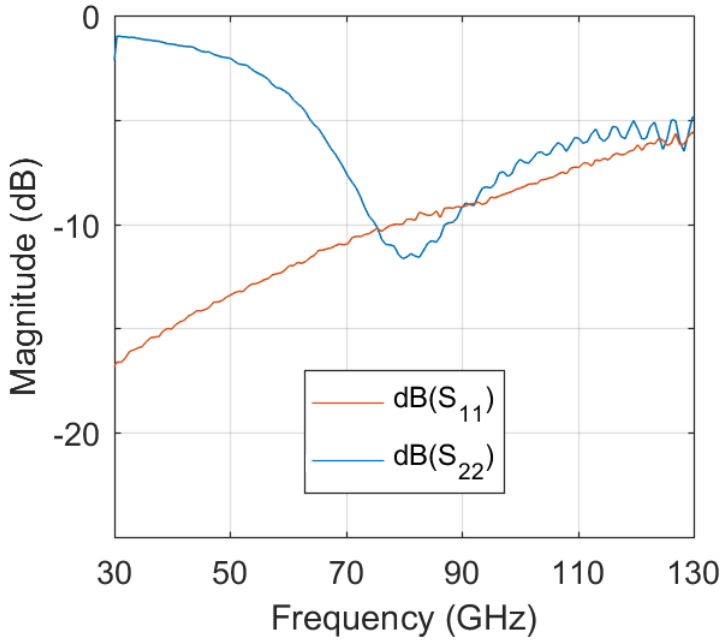


Figure 4.2: Measured input and output matching at LO and RF port.

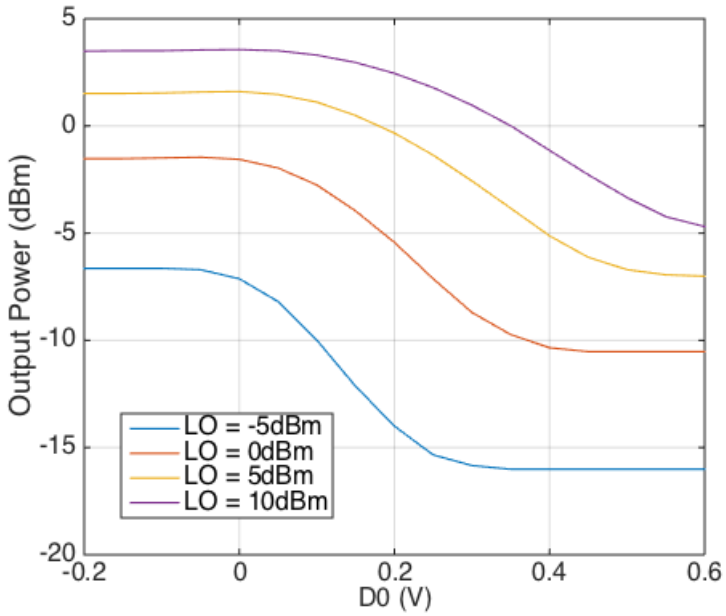


Figure 4.3: Simulated output power for different data input voltages of the MSB, with different input power (LO). The LSB is set to 0 V and the LO frequency is 75 GHz.

4.1.2 Time Domain Measurement

Time domain measurements were tested on a probe station. A Keysight M8195A arbitrary waveform generator (AWG) is used to provide binary data input to the modulator. To capture the output RF signal a Lecroy LabMaster 10-100Zi real-time oscilloscope was used. First it was tested using amplitude shift keying (ASK) as modulation format. A single PRBS-9 binary stream from AWG was fed into the data port D0. The output is captured by the oscilloscope when LO frequency was set to 50 GHz. The data rate of the PRBS-9 steam is change from 10 Gbps up to 20 Gbps and bit-error-rate (BER) is measured using the oscilloscope. The BER of 20 Gbps transmission is measured to be 1.2×10^{-8}. The time domain waveform of the 20 Gbps ASK RF signal is plotted in Fig. 4.4 and the received constellation diagram is shown in Fig. 4.5

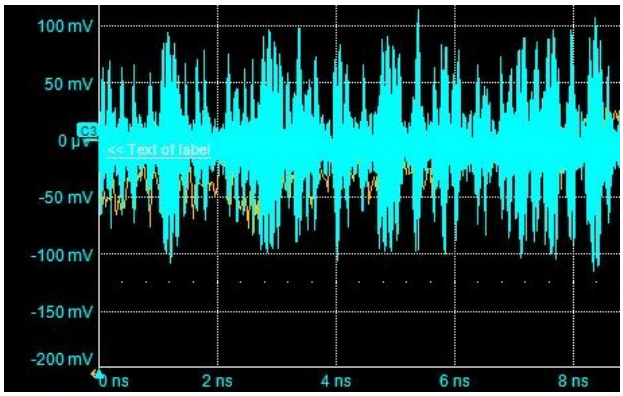


Figure 4.4: Measured 20 Gbps ASK modulated waveform in time-domain at 50 GHz center frequency

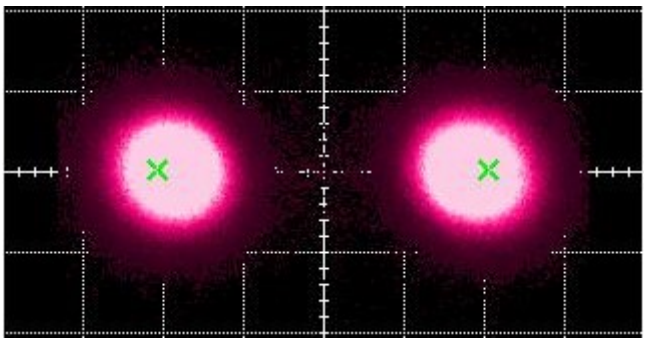


Figure 4.5: Received constellation diagram after demodulation using ASK.

The RF-DAC was also tested for PAM-4 signal modulation. Two independent binary streams (a PRBS-9 and a PRBS-10) are input to the 2 different data input ports on the modulator. The symbol rate of the PAM-4 signal was changed from 10 Gbaud up to 20 Gbaud. For 20 Gbaud, PAM-4 signal support a data rate of 40 Gbps with a symbol error rate (SER) of 3.7×10^{-6} and the received constellation diagram is shown in Fig. 4.6.

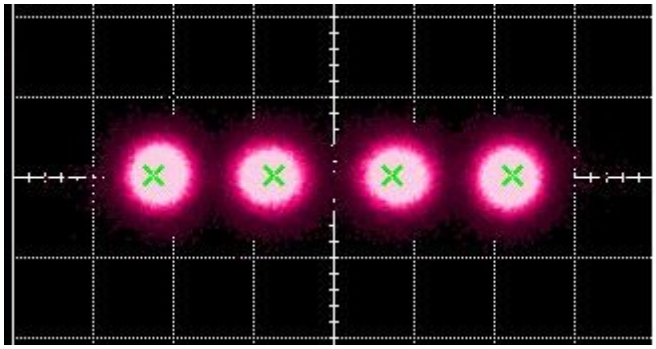


Figure 4.6: Received constellation diagram after demodulation using PAM4.

4.2 V2:PAM-4 RF-DAC (cascode)

The cascode modulator's function was simulated in both frequency and time domain.

4.2.1 Frequency Domain Simulation

The RF output power for different LO drive power can be seen in figure 4.7.

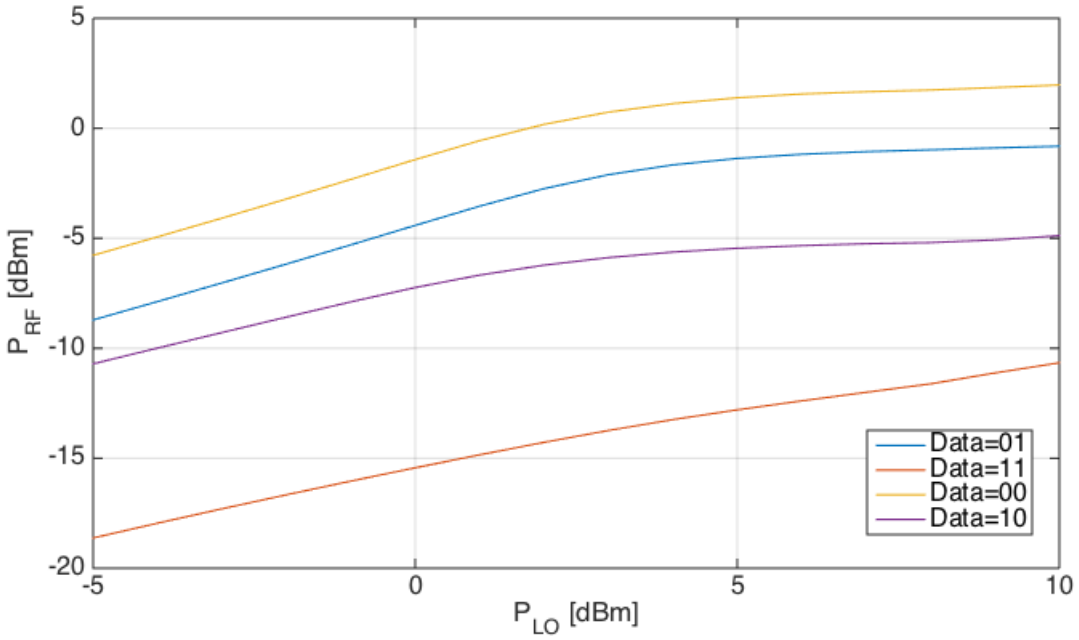


Figure 4.7: The RF output power for different values of LO input power for the "cascode" RF-DAC.

In figure 4.8 the RF output power for different frequencies and different data input is shown. At 70GHz the difference in output power between '00' and '11' is approximately 14dB. The LO input power for this simulation is 5dBm.
Simulation result of the input and output matching can be seen in figure 4.9. LO input matching denoted as 'S11' and the RF output matching denoted as 'S22'.

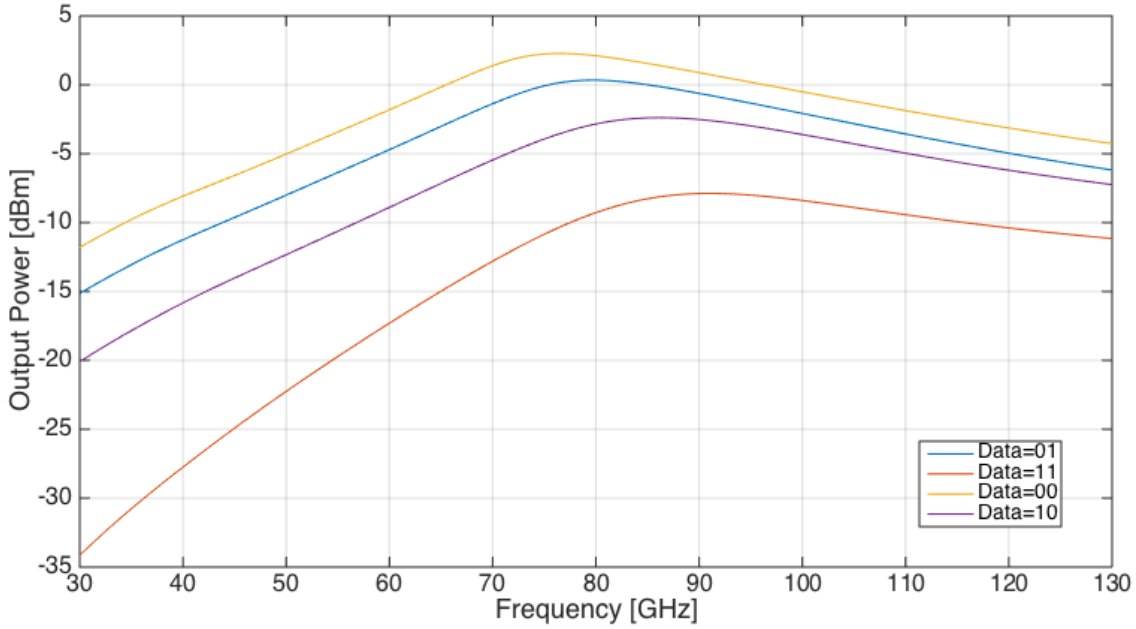


Figure 4.8: Simulated output power at different frequencies with different digital input for the "cascode" RF-DAC. The LO input power is 5dBm in this simulation.

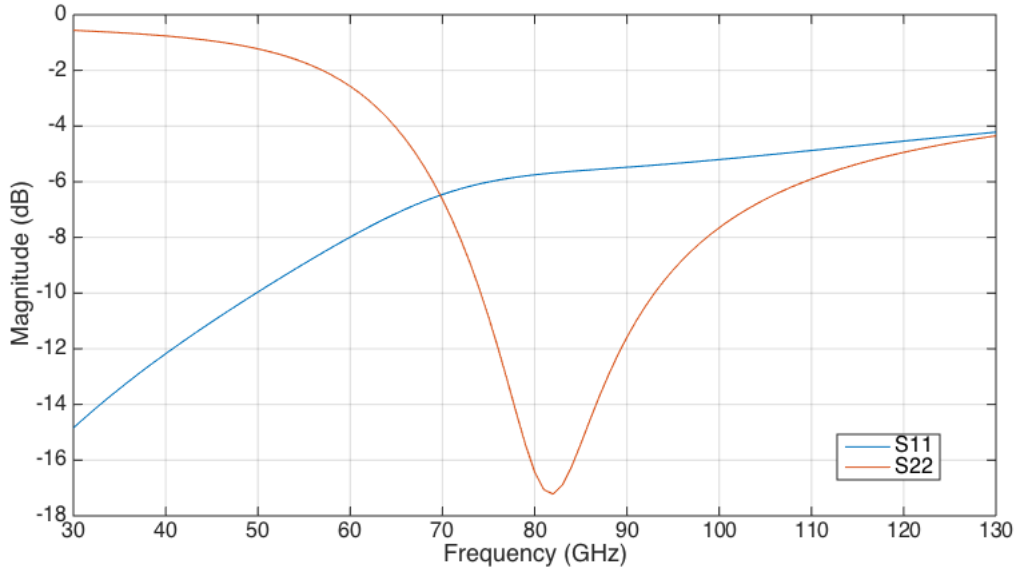


Figure 4.9: Simulated input and output matching at LO and RF port for the "cascode" RF-DAC.

4.2.2 Time Domain Simulation

Two different time domain simulations can be seen in figure 4.10 and figure 4.11. The first one shows a transmission using ASK. Same bit stream was fed into both data input ports. The LO frequency for this simulation is 70GHz and the LO input power is 5dBm. The data rate during this simulation was 30Gbps.

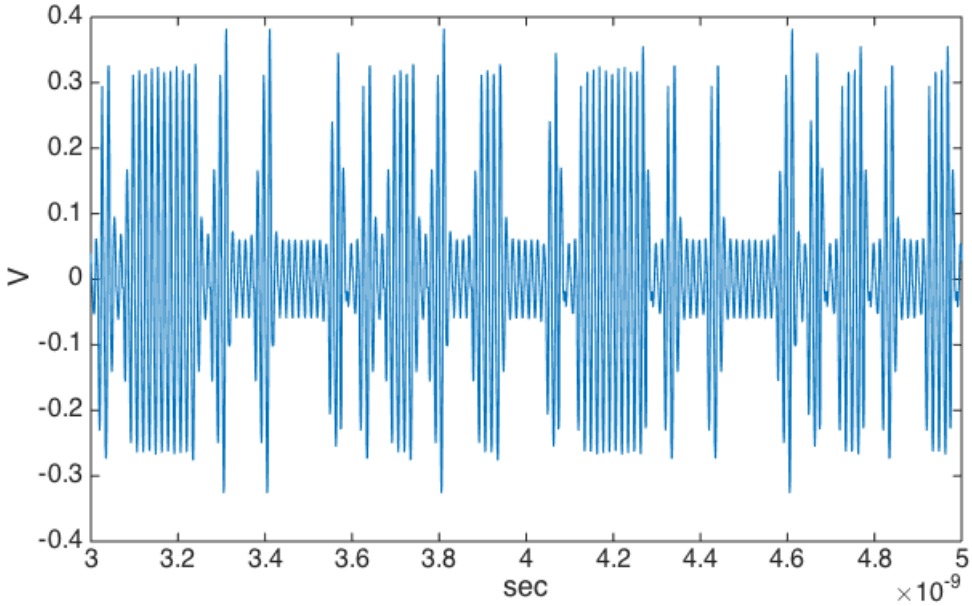


Figure 4.10: Simulated waveform with 30Gbps data rate transmission using OOK modulation for the "cascode" RF-DAC. The LO frequency is 70GHz and the LO input power is 5dBm.

In figure 4.11 two different bit streams were fed into the data ports creating a PAM-4 modulated signal. The baud rate in this simulation was 20GBd resulting in a 40Gbps transmission. The LO frequency for this simulation is 70GHz and the LO input power is 5dBm.

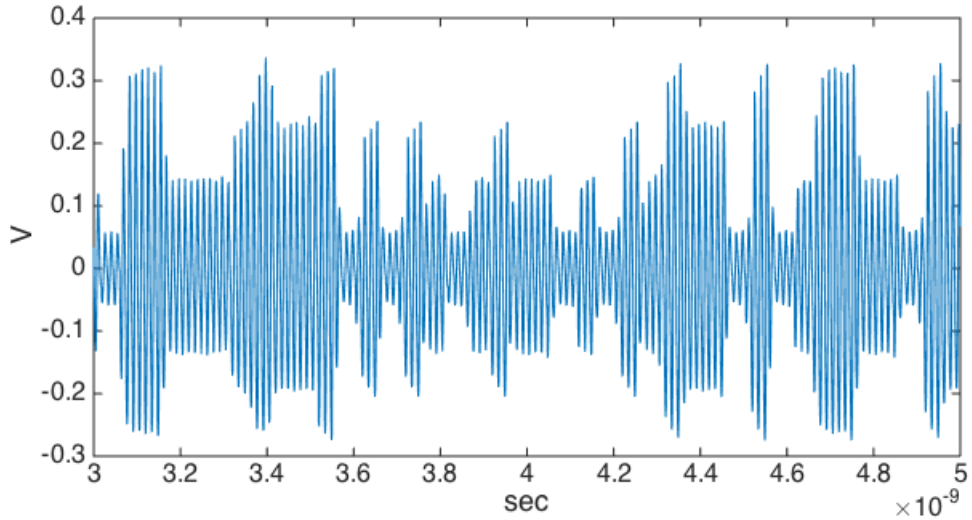


Figure 4.11: Simulated waveform with 20Gbd data rate transmission using PAM-4 modulation for the "cascode" RF-DAC. The LO frequency is 70GHz and the LO input power is 5dBm.

4.3 Specifications for the Circuits

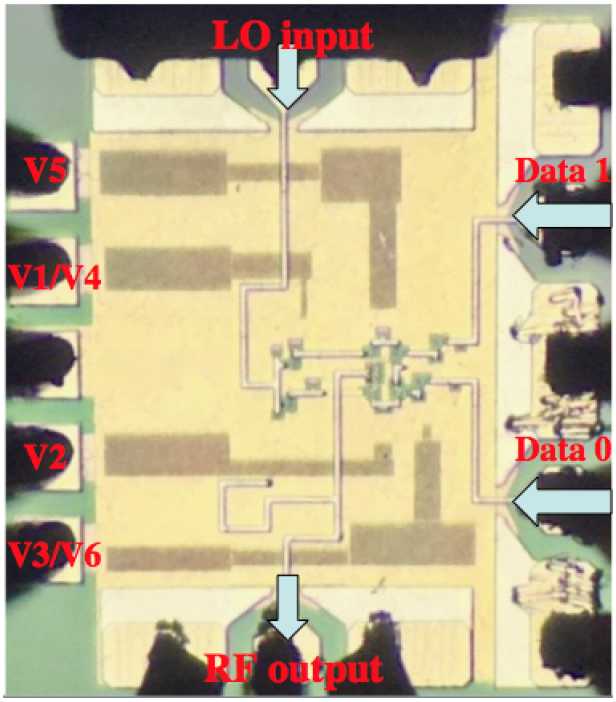


Figure 4.12: Photo of the fabricated RF-DAC (V1). The chip size is 800μm x 800μm.

Table 4.1: V1: Differential pair

Function	RF-DAC
Modulation	PAM-4
LO Input frequency	60-90GHz
LO Input power	-4 to 0 dBm
RF Output power	up to -5 dBm
DC power consumption	47.2mW (1.2pJ/bit)
Symbol rate	20GBd
Bit/symbol	2
Bit rate	40Gbit/s
Input data (0 or 1)	0V/0.3V

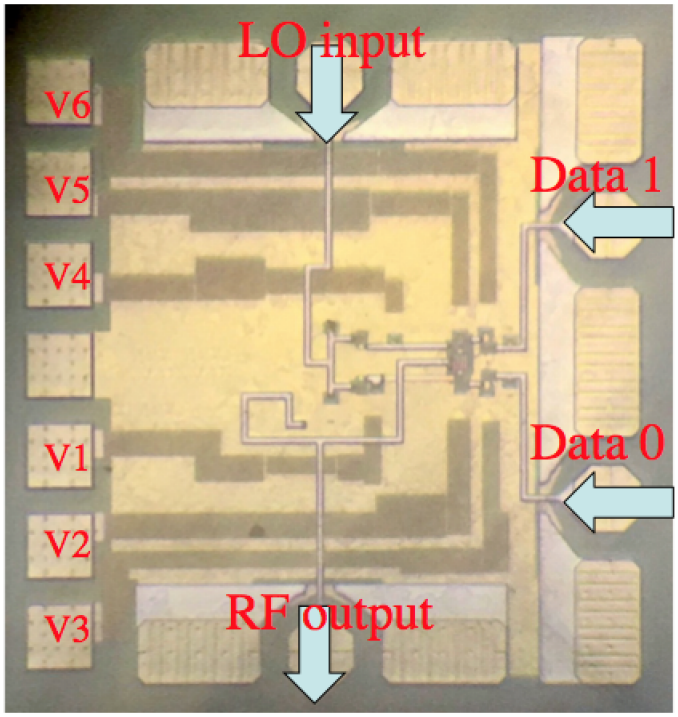


Figure 4.13: Photo of the fabricated RF-DAC (V2). The chip size is 800μm x 800μm.

Table 4.2: V2: Cascode (Estimated)

Function	RF-DAC
Modulation	PAM-4
LO Input frequency	70GHz
LO Input power	0 to 10 dBm
RF Output power	up to 2dBm
DC power consumption	41mW (1pJ/bit)
Symbol rate	20GBd
Bit/symbol	2
Bit rate	40Gbit/s
Input data (0 or 1)	0V/-0.4V

5
Discussion and Conclusion

This work has shown that it is possible to use unipolar PAM-M for wireless transmission. It is a new way of thinking and designing with power efficiency and high speed transmission both in focus. The InP-based 250nm DHBT-process that Teledyne Scientific Instruments, US, offers is providing low noise and high speed which makes new things possible.
At first the plan was to design only one modulator, but due to the novelty of the use of PAM-4 in wireless transmissions it is important to get to know how different design solutions work. The difference, that are already known after the simulation state, between the cascode solution and the differential pair solution was that the cascode solution consumed less DC power but required a higher LO input power. The differential pair modulator was more predictable and could switch between different PAM power stages quicker.
When it comes to the size of the circuits they were all relatively small. What took the most space was the output matching for the RF-DACs. Further more, the RF pads had to be large in size so the testing of the circuits is possible to do.
These results differ from those of others due to the simplicity and high bit rate of the transmitter/receiver system. It is a straight forward solution with low power consumption, and few stages. On off keying also fulfils those requirements, but cannot compete with the bit rate. When more amplitude levels are added a high bit rate is possible.
The biggest draw back with the use of unipolar M-PAM is the requirement for a larger signal to noise ratio. For cases were signal strength and low noise is not an issue, it has many advantages.
It is important to remember that this is only one solution, and many other solutions are possible. Since the use of unipolar PAM-4 and higher in ultra high speed wireless transmissions is a relatively new and untested method, all information that can be attained is important for the research in this field.
The use of ADS as a simulation and design tool is fairly standard in cases like this. There are always uncertainties when dealing with simulated results. Simulated results can be used only as an approximation and a way to approximately know the results. There are even uncertainties when measurements are done on real circuits due to errors in equipment. Small errors can of course also be made in the final design that gets sent to production. That does not mean that the concept of the design is faulty. It is important to find these possible errors or the cause of failure, especially if the model has flaws, to be able to make progress in the future.
There are many future possibilities using unipolar M-PAM. Since the fabrication of the circuits were done, further testing has been made both in time and frequency

domain. More understanding of the behaviour of the RF-DACs has been gained. Some advantages and disadvantages of the designs has been discovered, yet there is more testing that can be done. Things that can be improved include matching network, as well as using more symmetry to balance the circuit.
A higher carrier frequency can be used and more amplitude levels can be added. The efficiency of the circuits can be improved if time is given. All in all, there are plenty of opportunities to develop and explore the possibilities in this area.

To conclude this project, the finished MMIC worked relatively well. Better understanding of the process and the system has been gained, which is always needed. The DC bias conditions of the RF-DACs can be slightly adjusted to optimise the performance. In the end, proving the concept is the most important part at this point. Hopefully others will see that it is possible to create highly energy efficient systems that can compete in speed and performance too.

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