Integrated solid-state capacitors based on carbon nanostructures

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The constant demand for miniaturization, added functionality and increased performance of electronic devices systematically drives higher integration by adding more devices and functionality on a single chip. Over the last 40 years, this has been achieved by scaling CMOS technology according to Moore's law, resulting in better power performance and cost per function for each technology node. As the feature size of CMOS devices now approaches quantum or physical limits, the downscaling of devices is slowing down and therefore cannot sustain the lowering of cost and performance per function alone. As a result, a new component packaging strategy called heterogeneous integration, focusing on the performance enhancement and cost reduction at the system level, provides a new dimension and enabler to follow Moore's law in terms of system performance, by the stacking of chips (3D) or using an intermediate substrate, the interposer (2.5 D).

The full deployment of the 3D or 2.5D packaging technologies requires on-chip or in-package capacitors, not only in traditional integrated circuits, but also for integrated components, possibly on interposers, for applications such as decoupling capacitors, voltage stabilization or RF filters. In parallel, the emergence of the Internet of Things (IoT) is right around the corner, requiring not only high capacitance per unit area for the operation of the devices, but also integration of efficient and smart solutions with moderate energy storage and harvesting to operate the individual autonomous devices [1].

Traditionally, electrochemical double-layer capacitors (EDLC) [2] are devices providing the highest capacitance/footprint area [3], using the physical adsorption and electrostatic accumulation of ionic charges at the surface of the electrodes, originating from a liquid or sol-gel electrolyte [4]. However, liquid electrolytes are often toxic and corrosive, and their encapsulation presents a considerable challenge that hinders their integration directly onto CMOS chips. Consequently, integrated high density capacitors need to be fully solid-state in order to meet the requirements of stability and lifetime. Fully solid-state capacitors have faster charge and discharge rates compared to a liquid electrolyte capacitor (supercapacitors), making them more useful for high-frequency applications.

Besides bulky ceramic discrete capacitors, the simplest realization of a capacitor is the parallel plate capacitor using a thin (a few nanometers in thickness) solid dielectric layer. In this configuration, the capacitance is proportional to surface area, hence the parallel plate capacitors are limited by their footprint area. In ICs, an effective increase of the capacitance area has been achieved using deep trenches in the silicon substrate using dielectrics deposited using low-pressure chemical vapor deposition (LPCVD) [5] or multilayers of atomic layer deposition (ALD) [6]. Further increasing the capacitance requires consuming precious space on the chip, or other cost-increasing and partially reliable methods, in particular irreversible very deep reactive ion etching (DRIE) of the substrate combined with atomic layer deposition. This limits the potential for implementation of integrated capacitors. Recently, IPDiA (now Murata) has shown 500nF/mm^2 capacitors integrated in the silicon interposer at the cost of a minimum etch depth of 100µm [7] that potentially weakens the interposer's mechanical stability or imposes a large thickness of the interposer.

With the similar idea of increasing the surface area of the capacitor electrodes in mind, carbon nanostructures have been investigated as electrode materials in combination with thick dielectric layers deposited by ALD. However, such an approach has been, so far, limited by the necessity of transferring the nanostructures from the substrate on which they are grown to the active area, where they have to be used, because of the growth temperature required by such structures. Capacitors based on transferred carbon nanotubes (CNT) grown at 700ºC, subsequently coated by a 10-15nm dielectric deposited by ALD provided capacitance values of about 40nF/mm^2 [8].

The recent progress and availability of our proprietary technology has allowed the growth of vertically aligned carbon nanofibers (CNF) at a temperature compatible with CMOS technology directly rooted on the active chip, underlying substrate or component. This technology also allows the process on any substrate that can sustain a thermal budget of less than 400°C, and permits the realization and re-visiting of integrated solid-state capacitors with high-capacitance per footprint area. More specifically, integrated novel capacitors can be made of vertically aligned carbon nanofibers as one electrode material, providing a large 3D surface area for a small footprint, and their conformal coating of dielectric and a metallic counter electrode. The more than tenfold enhancement of the active surface, compared to the occupied footprint on the chip, where they are rooted, makes very efficient use of the chip. Such capacitors can therefore take advantage of the unique combination of the intrinsic electrical and surface properties of carbon nanostructures [9], without the economic and technical hindrances of the transfer process after growth, associated with the limited and laborious nature of such a transfer process.

Our enabling technology for the growth of the CNFs is catalytic plasma-enhanced chemical vapor deposition (PECVD) [10] (**Figure 1**), which made possible a completely deterministic and possibly reworkable method to produce CNFs on substrates. The positioning of the fibers on a substrate would depend on the

presence of a catalyst, whereas the CNF alignment is controlled by the electric field generated by the growth plasma, and the length of the CNF is simply determined by the time and growth conditions. Many PECVD systems using different radio frequency (RF) and microwave sources have also been developed [11-13]. However, the direct current plasma-enhanced chemical vapor deposition (DC-PECVD) has produced, so far, the best results for the fabrication of CNFs at low CMOS-compatible temperature using different pre- and post-processing techniques to cope with the inherent discharge problems that may arise when using insulating substrates [14]. The activity of the catalyst particle is crucial for the growth process [15]. It can consist of one or a few elements [16], however the vast majority of the reports regarding the growth of CNFs deal with catalysts made of transition metals: Fe, Co, Ni [16]. In addition, it is currently believed that the catalyst should form nanoparticles of a favorable size in order to initiate the growth of a CNF. Therefore, the catalyst can be deposited as a film using physical vapor deposition techniques, or directly as nanoparticles using spray coating [17] or spin coating [18], providing that the growth temperature will lead to a dissociation of the film into droplets/nanoparticles of appropriate size.

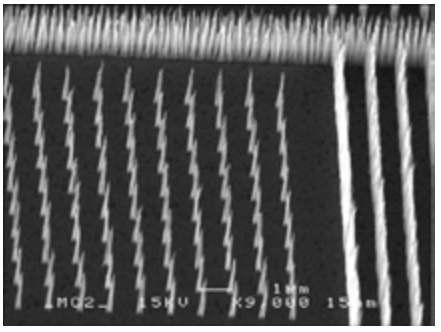

Figure 1: SEM of individual fibers.

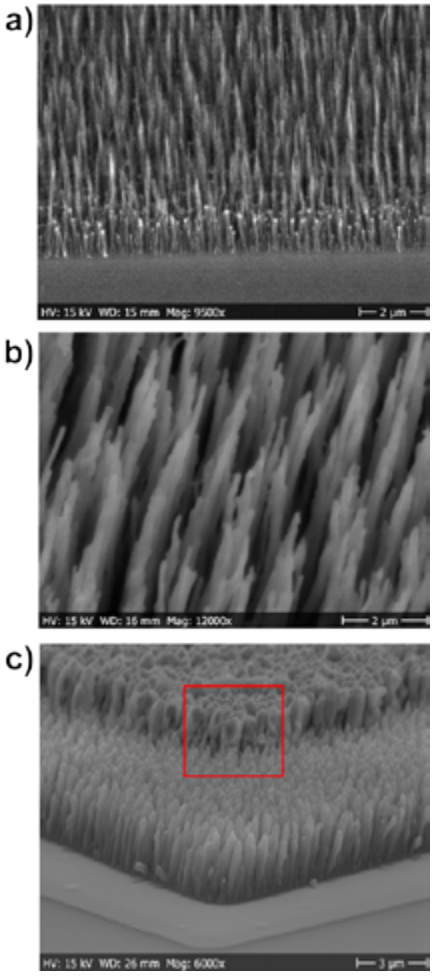

Figure 2: a) CNFs as grown; b) CNF coated with dielectrics; and c) Integrated 3D capacitor.

In a first demonstration of the CNF-based capacitor technology, very low profile 3D capacitors with a profile of 7µm have been produced. The CNFs were grown as a "forest" or "bed of nails," selectively, using DC-PECVD at 390°C in an ammonia and acetylene environment [18] (**Figure 2a**), on a Ti/Au current collector previously deposited using sputtering

on a Si substrate. Low-temperature thermal ALD was used for conformal coating of dielectric Al_2O_3 on vertically-aligned carbon nanofibers (VACNFs) (**Figure 2b**). To define the top electrode, a stack of Ti/Au was sputtered followed by photolithography to define the top electrodes (**Figure 2c**).

The capacitors with a total height of less than 7µm showed linear dependence of the capacitance per footprint area ranging from ~10-15nF/mm^2 (**Figure 3**). Therefore, they represent a credible solution in the heterogeneous integration landscape, proving truly

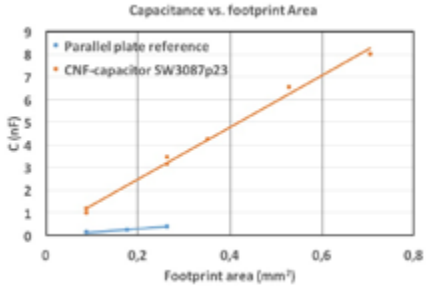

Figure 3: Comparison of Smoltek's solid-state initial integrated capacitor prototype (SmolCACH™) and parallel capacitors.

solid-state and 3D capacitors for on-chip integration for capacitance densities up to 1µF/mm^2. Further development and optimization will be needed to ready the solution for high-volume manufacturing.

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