Non-contact scanning probe technique for electric field measurements based on nanowire field-effect transistor

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A.S. Trifonov[a,b,1], D.E. Presnov[a,b], I.V. Bozhev[b], D.A. Evplov[c], V. Desmaris[d], V.A. Krupenin[b].

[a]Skobeltsyn Institute of Nuclear Physics, Lomonosov Moscow State University, 1(2), Leninskie Gory, GSP-1, Moscow 119991, Russia

[b]Physics Faculty, Lomonosov Moscow State University, Moscow 119991, Russia

[c] AIST-NT Inc, 359 Bel Marin Keys Blvd, Suite 20, Novato, California, 94949, USA

[d]Group for Advanced Receiver Development, Department of Earth and Space Science, Chalmers University of Technology, 41296 Göteborg, Sweden

Highlights:

- Field-effect transistor with nanowire channel was fabricated on the apex of silicon-on-insulator chip.
- Field scanning probe sensor was proposed and demonstrated.
- Proposed sensor may be useful tool for extremely sensitive electric field probing of solid and biological interfaces.

Abstract.

We report on the new active tip for scanning probe microscopy allowing the simultaneous measurements of surface topography and its potential profile. We designed and fabricated a field-effect transistor with nanowire channel located on the apex of silicon-on-insulator small chip. The field-effect transistor with nanowire channel was selected due to its extremely high electric field sensitivity even at room temperature. We developed the scanning probe operated in the tuning

1 Author to whom correspondence should be addressed. E-mail: trifonov.artem@phys.msu.ru

fork regime and demonstrated its reasonable spatial and field resolution. The proposed device can be a unique tool for high-sensitive, high-resolution, non-destructive potential profile mapping of nanoscale objects in physics, biology and material science. We discuss the ways to optimize the sensor charge sensitivity to the theoretical limit which is 10^{-3} e/Hz$^{-1/2}$ at room temperature.

1. Introduction.

There are a number of high-resolution scanning probe microscope (SPM) techniques for mapping the electrical properties of condensed or soft surfaces [1-15]. Electrostatic force microscopy (EFM) and Kelvin probe force microscopy (KFM) are based on the effect of the electrostatic interaction between a biased probe and the sample for calculating a quantitative value of the electric potential. These techniques demonstrate resolution in several mV at low temperatures [2]. Scanning capacitance microscopy uses electrical measurements only [3-4] and has the same level of resolution. Also there are works [5-12] where active electrical sensors were fabricated on the SPM probe apex for studying the electrical properties of the sample independently from its topography measurements. These sensors include resistive probe [5], field-effect transistors (FETs) made using CMOS-compatible [8-9] or ion milling techniques [6-7], single-electron transistors [10-11], NEMS device [12]. One more candidate for the local or SPM sensor is a modified FET with nanowire (NW) channel. Basically, NW FETs have been widely used for the development of high sensitive biosensors to detect extremely low concentrations of specific molecules (proteins, DNA, RNA) in biological systems [16-21]. The most sensitive charge/field device is a single-electron transistor, operated at low temperatures only [22]. FETs operate in wide temperature range from mK to room temperature. The charge sensitivity of FET-based scanning device at room temperature starts from ~ 100 electrons in earlier works [23] and reaches tens of electrons in later works [7-8, 24]. The charge sensitivity of NW FET is significantly better, theoretically it is several orders of magnitude smaller than the charge of single electron. Experimentally it was demonstrated charge sensitivity 4×10^{-5} e/Hz$^{-1/2}$ at 25 K (2kHz) for a 28-nm-diameter InAs NW FET [25].

NW FETs were fabricated from silicon-on-insulator (SOI) wafers using well-known technological processes: e-beam lithography, reactive ion etching (RIE), thin film vacuum deposition. Equivalent charge sensitivity of the experimental structures was estimated to be about 0.2 e/Hz$^{-1/2}$ at 10Hz and room temperature. Theoretically, their maximum sensitivity in the subthreshold mode and at low frequencies was estimated to be in the order of 10^{-3} e/Hz$^{-1/2}$ at 300 K [26-27].

In this paper, we present a NW FET fabricated on the apex of a small SOI chip, at the distance of few nanometers from its sharp corner. We developed an original technique for forming NW FET chips with very high yield and reproducibility. The tuning fork scanning technique [28] with advanced scanning algorithm was used to get topography images and, at the same time, to record electric potential profile of the samples. The fabricated devices were evaluated with metallic stripped test structures. Our results show promising aspects for NW FET investigation the electrical properties of nanostructures with high spatial and field resolution.

2. Experimental setup.

2.1. NW FET fabrication process

The sensing element of NW FET active probe is a kinked silicon nanowire ~ 500 nm long and ~80 nm wide. The similar sensing technique is described in [5-7], in our case we placed NW FET exactly on the scanning tip apex to obtain minimal distance between sensor and object.

The transistor structure was formed in the upper silicon layer of SOI wafer and connected to the macroscopic electrodes. The supporting substrate played the role of gate electrode for tuning an optimal working point of the transistor. The fabrication technique for the NW FET was described elsewhere [26]. The original technique was developed for placing the NW FET on the sharp apex of the SOI chip. The apex itself was the surface sensing element of SPM tuning fork probe .

The formation of the sharp apex in silicon chip is a trivial procedure. The cracking of silicon wafer occurs exactly along its crystallographic axes and two perpendicular intersecting cracks will form an atomically sharp apex. The angle between edges forming apex depends on the crystallographic orientation of the initial wafer. The sensitive element of the transistor should to be placed on the very chip apex. We propose an original, easy-to-use and producible approach: the formation of several transistors in the center of SOI wafer and a subsequent controllable trench-assisted cracking process in the desired place. Such approach may be useful for the formation of any nanostructure on the silicon chip apex or on any other crystal sample apex.

The guide trenches along selected crystallographic wafer axes were formed in wet etching process before the transistors fabrication. The transistors positions were defined in the calculated point of conditional intersection of the trenches lines. Final procedure was the cracking of the

wafer along guide trenches. As a result the NW FET structure was located exactly on the chip apex.

The rate of silicon etching in alkali strongly depends on the crystallographic orientation of the wafer. Triangular-shape trenches are formed after etching {100}-orientated silicon wafer through a rectangular mask. The sidewalls of trench have a {111} orientation. The sidewalls are perpendicular to the etching direction corresponding to the lowest etching rate [29]. The etching process stops on a line along the crystallographic axis, which is defined by the intersection of the {111} planes at an angle of 70,52 °.

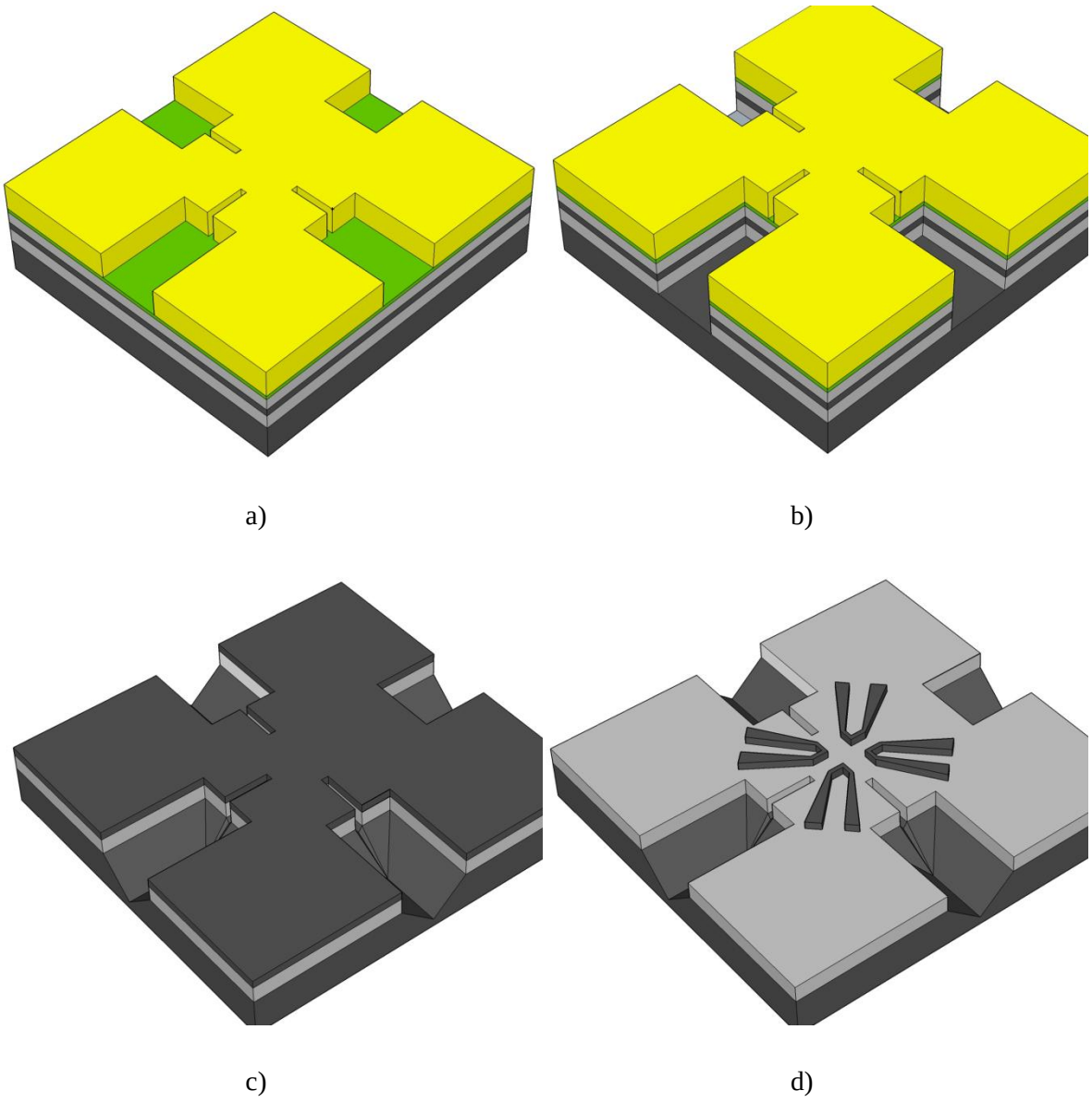
We used 5x5 mm SOI chips for the fabrication of 16 SPM probes with NW FETs. The initial 750 μm thick SOI wafer was thinned by reactive ion etching to the thickness of 300 μm to reduce the chip weight and to assist the chip cracking.

For forming the guide trenches, the SOI wafer was covered by Si_3N_4 / SiO_2 layers using plasma-enhanced chemical vapor deposition (PECVD). Rectangular mask was formed (Fig. 1a) in a thick e-beam resist (~1.5 μm, several layers of copolymer -EL11/PMMA-A4) using electron beam lithography. Reactive ion etching (in fluorine) process transferred the mask in the $Si_3N_4/SiO_2/Si/SiO_2$ layers (Fig. 1b). Then, the wafer was etched in a KOH solution. After forming triangle-shape trenches in the supporting Si layer of the SOI wafer etching process was extremely slowed down due to different etching rates for different crystallographic planes. Finally, the Si_3N_4/SiO_2 layers and the rest of e-beam resist were removed in buffered hydrofluoric (BHF) acid solution (Fig. 1c).

Next, the NW FET structures were fabricated in the top Si layer of 5x5 mm SOI chip using e-beam lithography and reactive ion etching as described in [26]. The trenches walls ({111} planes) intersection lines were used as a reference lines for calculating the coordinates of prospective chip apexes (Fig. 1d).

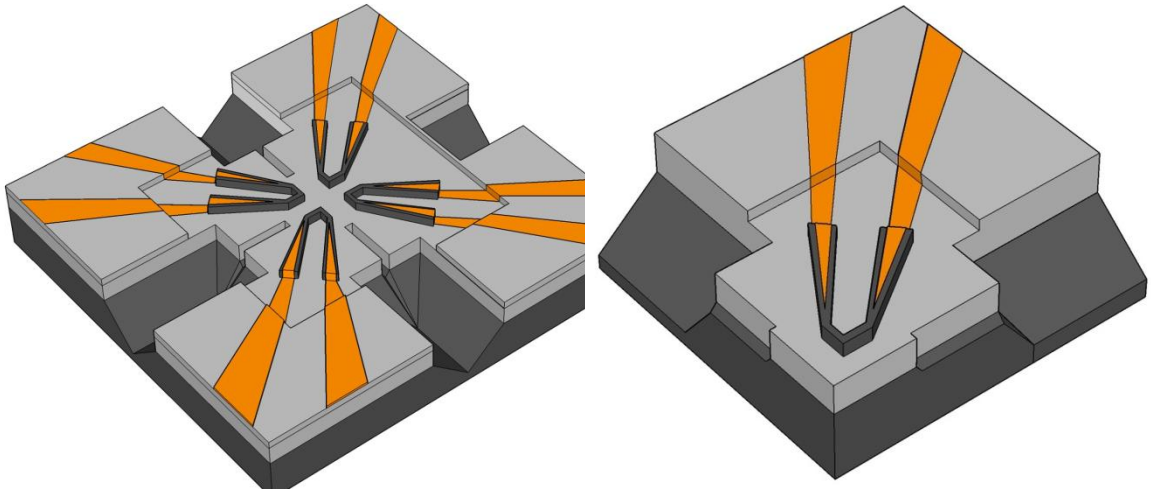
The whole top chip surface, except central ~ 120x120 μm area with NW FETs was covered by a 500 nm SiO_2 dielectric layer for additional electric isolation of macroscopic Ti electrodes from the substrate (Fig. 1e). The supporting Si layer of the SOI chip was used as gate electrode for the NW FET. This gate electrode served for tuning the optimal transistor working point during SPM measurements. The small windows in the top SiO_2 layer were opened and additional metallic (Ti) contact pads were formed to provide a reliable electrical contact for the gate electrode from the top side of the chip. In the next technological step, we cracked down the chip into 16 pieces using

trenches as a guides for applying mechanical tension. The schematic sketch of the final chip is presented in Fig. 1f. The Scanning electron microscope (SEM) images of NW FET are shown in Fig. 2. The yield of working chips was about 80%, the distance from the NW to the chip apex varies from 5 to 20 nm.



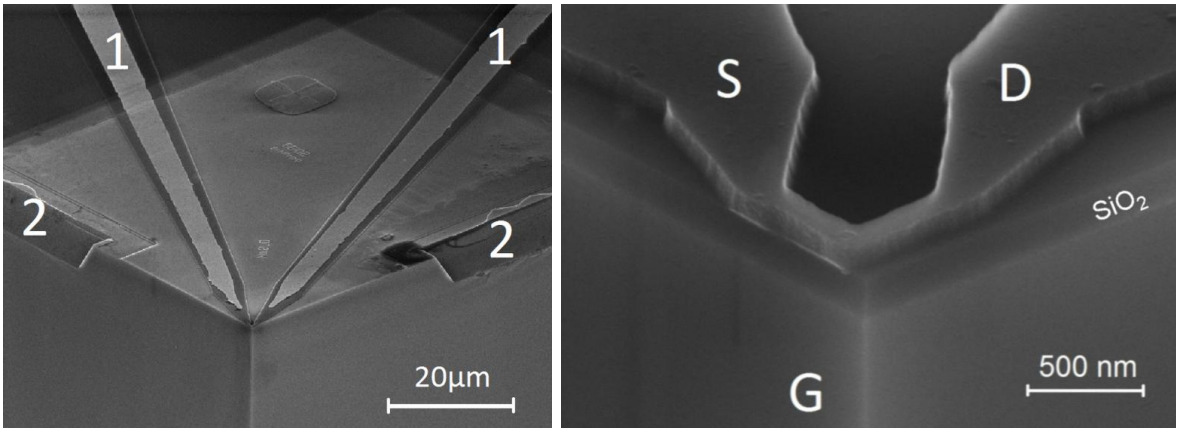
a) b)

c) d)



e) f)

Figure 1. Schematic illustration of the fabrication processes of NW FET on the chip apex. Only 4 from 16 NW FETs are shown in figs. a) - e) for clarity. Dark gray - Si, light gray - SiO_2, green - Si_3N_4, yellow - PMMA A4, orange - Ti). a) SOI wafer covered by Si_3N_4 / SiO_2 and PMMA mask layers. b) wafer after RIE, c) wafer after BHF d) formation of NW FET, e) formation of isolation layer and Ti electrodes, f) final chip.



a) b)

Fig 2. SEM images of NW FET on the chip apex. a) General view of NW FET containing macroscopic electrodes (1) and the rest of guide trenches (2). b) NW FET (S – source, D - drain) located in the vicinity of the chip apex. Supporting Si layer of the SOI chip acts as gate electrode (G).

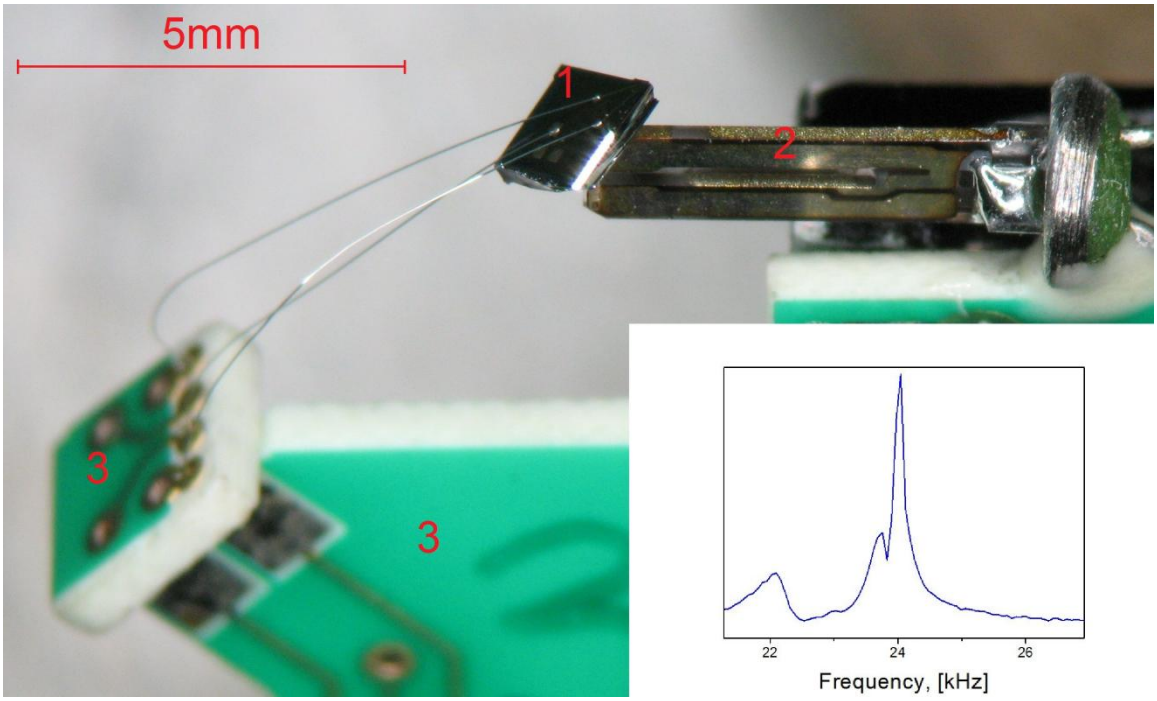


Fig. 3. An optical image of NW FET cantilever chip (1) on the tuning fork (2) assembled on the holder board (3). Inset shows frequency response function of loaded tuning fork (resonance frequency is 24.1 kHz, quality factor is 230).

2.2. Tuning fork

We used the scanning probe microscope AIST-NT SPM (model SmartSPM-1000) operating at ambient conditions in the tuning fork [28] regime (a very rigid macroscopic quartz crystal resonator of very high quality factor interacts with studying surface). The fabricated chip was epoxy-glued on one of the quartz crystal fork leg and contact pads were wire-bonded to the holder board. (Fig. 3). The chip apex works as a cantilever for the topography measurement and the NW FET operates as a field sensor. The tuning fork quartz crystal was excited mechanically on its resonance frequency, the oscillation phase shift provides a feedback signal for the surface sensing. The weight of the NW FET chip was ~ 0.8 mg, the weight of one leg of a quartz crystal resonator is ~1.3 mg. After gluing the chip, the quality factor of quartz crystal decreased by order of magnitude, down to 200-300. The resonant frequency of the whole system also shifted from 32.768 kHz to 22 - 25 kHz. However, this was enough for reliable scanning of samples topography and potential profiles at a frequency of 0.5-1.0 Hz/line.

We developed a special scanning algorithm to minimize the probe - sample interaction time. This algorithm approaches the chip to the sample for a short time for taking signals and retract back when moving the chip to the next sample point. The mechanical interaction between the NW FET chip and the sample was very weak and did not destruct the nanowire channel. The measurement time in each sample point was 0.4 - 0.8 μsec. This value is determined by the time required for measuring the transport current through the NW FET. There is a significant mutual capacitance "sample – NW channel". Settling time for the transistor current is in the order of: $\tau = 1/RC$ (R - NW resistance, C - capacitance "sample – NW channel"). Experimentally, τ may be estimated from the dependency of the NW current on "sample – NW channel" distance.

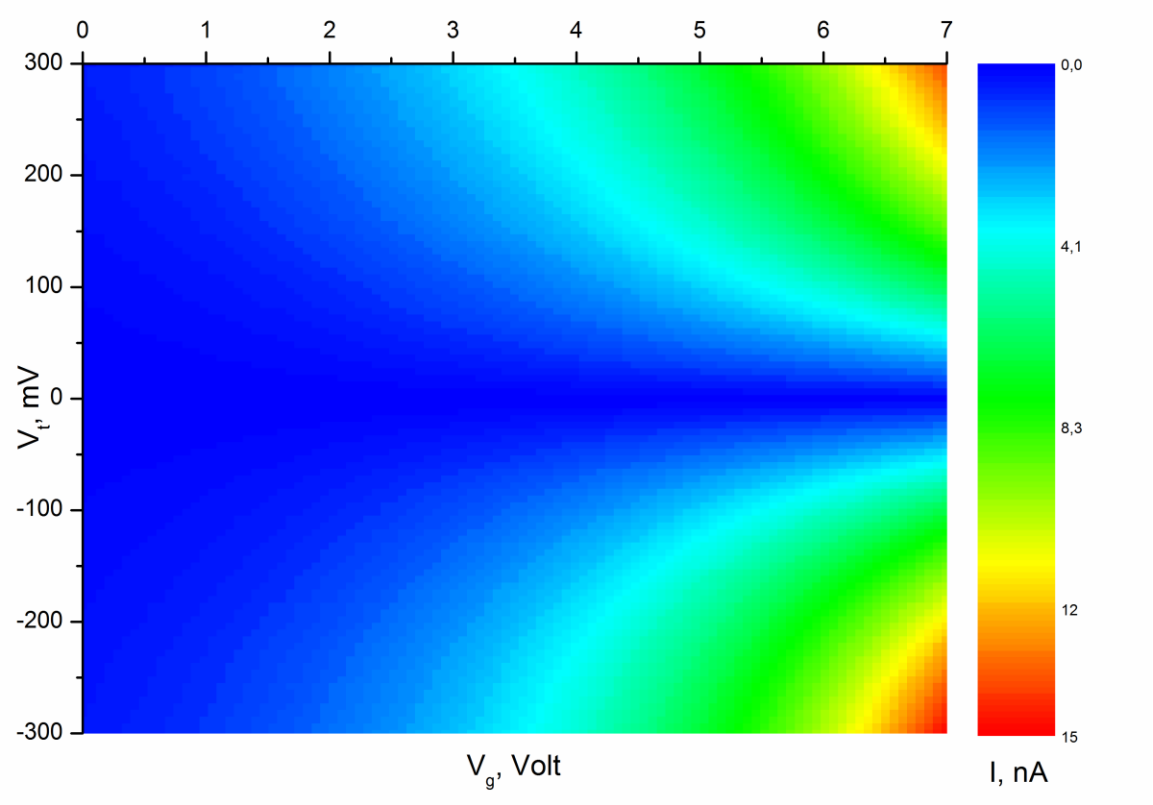
The test sample was a system of conductive Au/Cr strips (15 nm height, 50-500 nm width) fabricated on a dielectric substrate. There was possibility to apply DC voltage (up to +/- 7 Volt) to all strips.

3. Results and discussion.

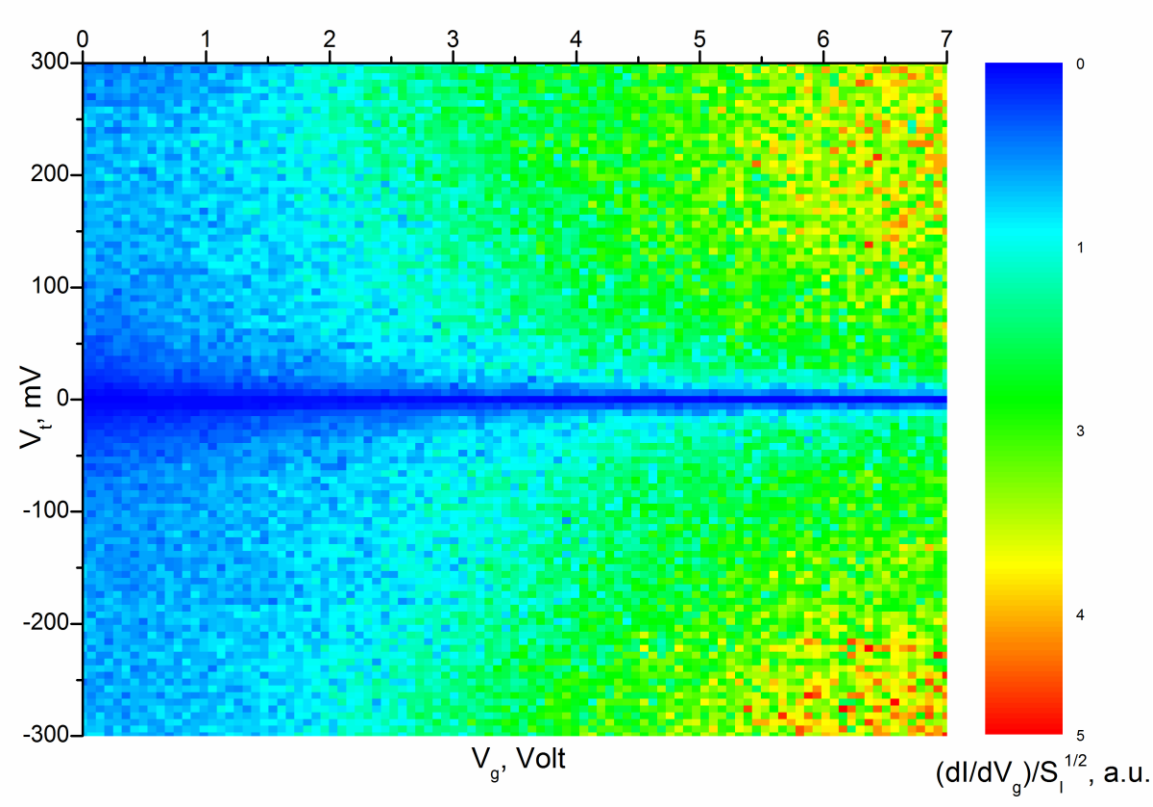
3.1. NW FET sensitivity

There are two the most important issues in the development of NW FET fabrication technology for sensing extremely weak electric response from nanoobjects. The first is the minimization of the transistor intrinsic noise. The second is detection of the optimal ranges of gate (V_g) and (V_t) transport transistor voltages. In the case of sensing application, this range must provide the maximal signal-to-noise ratio (SNR). In other words, the ratio of signal characteristic slope (dI/dV_g, I - current through NW) to the square root of the power spectral density of NW current fluctuations must be maximal. At the same time, sensor should operate at small transport current and voltage to minimize back influence on the object under study.

We recorded the NW FET contour plots $I(V_t, V_g)$ and the spectral density of current fluctuations $S_I(V_t, V_g)$ in the frequency range Δf = 50-500 Hz. The contour plots $I(V_t, V_g)$ and calculated SNR – $(dI/dV_g)/S_I^{1/2}$ - diagram at 10 Hz are presented in Fig. 4.


0
1
2
3
4
5
6
7
300
200
100
0
-100
-200
-300
V_t, mV
V_g, Volt
0,0
4,1
8,3
12
15
I, nA

a)



b)

Fig. 4. a) The contour plot $I(V_t, V_g)$ of NW FET. Current range from 0 to 15 nA; b) SNR contour plot of NW FET at 10 Hz, arbitrary units.

The NW FET sense electric field. Its sensitivity relative to its own gate potential was estimated to be about 0.15 mV/Hz-1/2 at 10Hz. We estimate the NW FET equivalent charge sensitivity by classical approach (1):

$$\delta Q = \frac{\partial Q}{\partial I}\delta I = \frac{1}{\partial I/\partial Q}\sqrt{S_I \Delta f} = \frac{C}{\partial I/\partial V_g}\sqrt{S_I \Delta f} = \left\{\frac{\sqrt{S_I \Delta f}}{\partial I/\partial V_g}\right\} C \qquad (1)$$

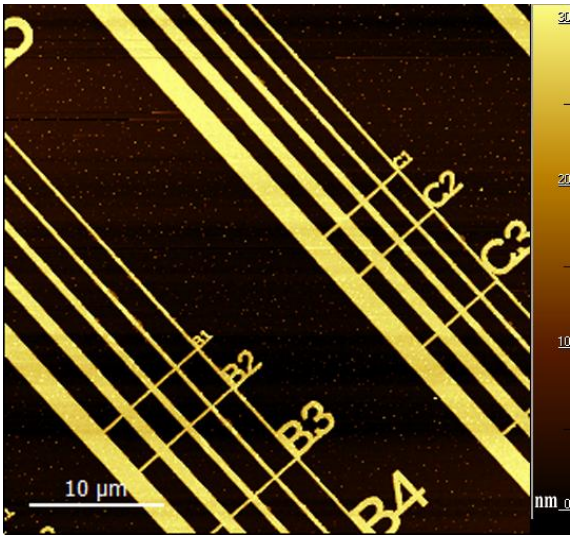
where ∂I is the change in the electric current through NW as a result of appearing additional ∂Q electric charge on the NW surface, C is the mutual capacitance of the NW and gate electrode (test sample). The capacitance coefficient in right side of (1) is inverse SNR value. We estimated the capacitance value from the geometrical and electrical parameters of our system in the same way as in [26]. This capacitance is estimated to be 0.2 fF for a NW with 1 μm length and 100 nm

width. Taking SNR value from the experimental data and a capacitance value from the estimation one can get from (1) the value of NW FET charge sensitivity at room temperature and ambient conditions:

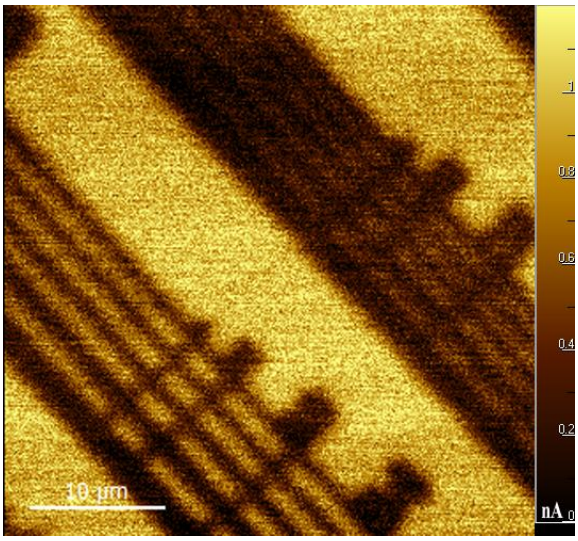
$$\delta Q \sim 0.2\ e/\sqrt{Hz} \qquad (2)$$

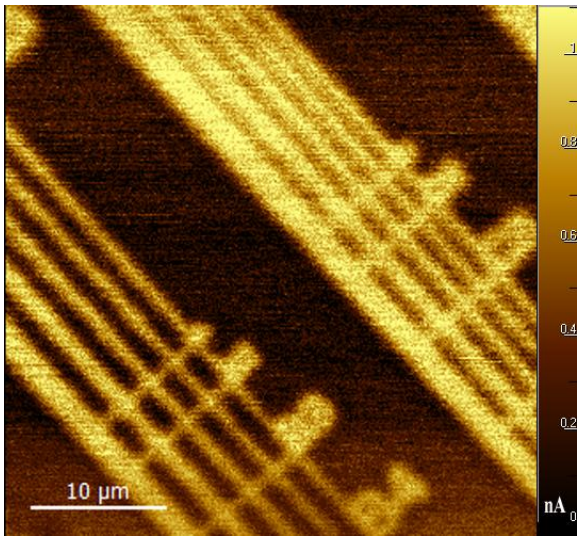
3.2. Spatial and field resolution of NW FET sensor.

The spatial resolution of NW FET field sensor is determined by the NW geometry and is limited by accuracy of technological processes. NW FET output depends on the local electric field in the vicinity of its channel generated together by test sample and NW FET gate. The field resolution of the NW FET based sensor depends on its total noise level consisting of the intrinsic transistor noise and the noise of the measuring electronics. The sensor sensitivity threshold ∂V_g relative to its own gate (back side of NW FET chip) differed from 2 to 10 mV in a single frequency band, the noise of measuring electronics was 4 orders of magnitude smaller. The equivalent field resolution of the sensor depends on the distance from NW to object. In our case the distance between a chip apex and the test sample was 2-4 nm during the measuring time period. The distance between the NW and the chip apex was also small (5 - 20 nm). Thus, the equivalent field resolution for real samples will be defined by the location of the sample and the characteristics of sample material (dielectric constant, conductivity). Topography of test sample and corresponding NW current maps are presented in Fig. 5.



a)



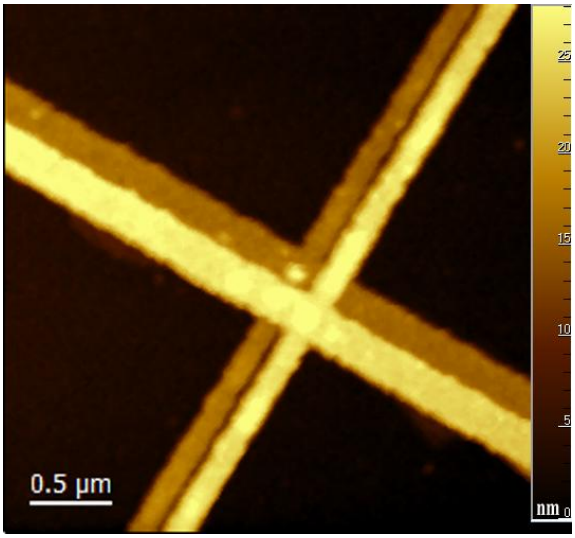


b) c)

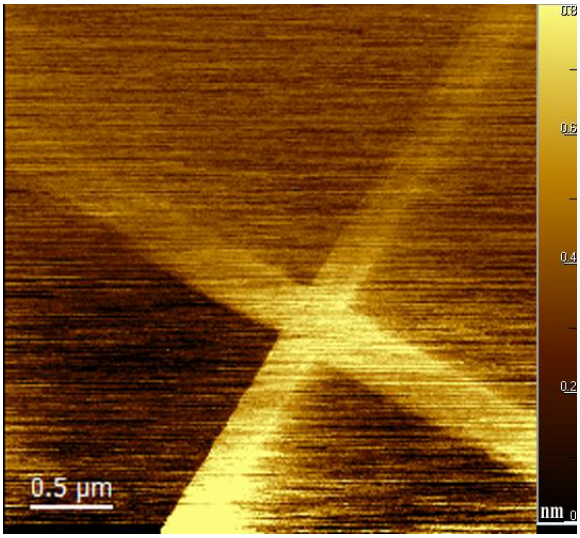
Fig. 5. Test sample topography (a) and NW current maps (b, c) for different NW FET working points: transport voltage V_t - 100 mV, gate voltage V_g - 3500 mV. b) - test structure voltage +4000 mV; NW FET current changes from 0 to 1.2 nA, c) - test structure voltage -4000 mV, NW FET current changes from 0 to 1.1 nA. The distance between the sample and the NW probe was 20 nm.

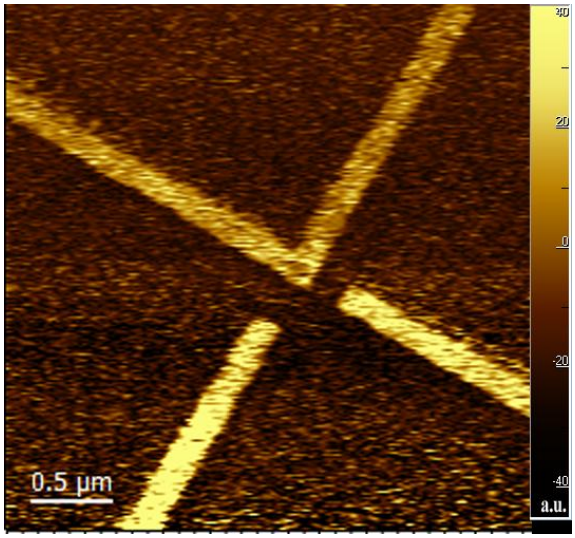
To increase the sensitivity, we decreased the distance between the NW and the chip apex to 5 nm and used lock-in technique. The distance between the sensor and the test sample was modulated with 0.5 - 1.5 nm amplitude and the response in NW current was detected. The scan rate

decreased 2-4 times due to an additional lock-in accumulation time but the spatial field resolution of NW FET became 2-3 times better comparing with direct current mapping. The results are presented in Fig. 6.



a)





b) c)

Fig. 6. a) topography, b) NW current map (NW FET current changes from 0 to 0.8 nA) and c) lock-in response map (arbitrary units). NW FET working points: Transport voltage V_t - 100 mV, gate voltage V_g - 7000 mV, test structure voltage -100 mV. Distance modulation amplitude 1 nm, modulation frequency 4166 Hz, accumulation time 4 msec. The distance between the sample and the NW probe was 5 nm.

Intrinsic transistor noise consists of two components: the fluctuations caused by the conductivity of the NW and contact electrodes. The NW contact electrodes can be ohmic or include Schottky barriers. In the case of Schottky barriers, the effect of noise reduction is achieved by increasing the contact area [30]. To reduce the noise in ohmic contacts one can select special groups of materials [31] or use heavy doped silicon for the fabrication the FET source and drain areas [32]. In our case, due to the low resistance of the Schottky barriers (1 kOhm, [26]) compared with the resistance of transistor channel barriers (tens of MOhm), contact electrodes contribution to the total transistor noise was negligible.

It was shown for single-electron transistors that the charge noise sources located in the substrate and in the dielectric layers, covering the transistor island, significantly decrease their sensitivity [33]. The sensitivity enhancement of single-electron transistors was achieved in the structures partially or completely isolated from the substrate [34-35]. Additional noise in the NW FET is also associated with movements of charges in the substrate (SiO_2 SOI layer). Such movements have a random nature, their influence on the transistor noise can be reduced by reliable isolating NW channel from the substrate. One of possible ways is fabrication of the transistors with suspended NW.

4. Conclusion.

We have developed a reproducible (yield of working chips ~ 80%) and scalable NW FETs fabrication technology. The distance from the transistor NW channel to the SOI chip apex varies from 5 to 20 nm. The CMOS-compatible fabrication technology includes e-beam lithography, wet and reactive ion etching, thin film vacuum deposition processes only. We have demonstrated the ability to use the apex of the NW FET chip as a non-contact scanning probe, working in the tuning fork mode at room temperature and ambient conditions. The scanning probe showed spatial resolution of about 10 nm in-plane and ~ 0.5 nm in height. We have demonstrated direct measurements of the potential profiles on test samples using a NW FET simultaneously with the topography measurements. The first measurements showed an electric field resolution of 10 mV in the 100 Hz band. The electric field resolution of the NW FET transistors could be improved by more than an order of magnitude by the fabrication NW FET closer to chip apex and by refining the NW FET fabrication technology for significantly decreasing the NW FET intrinsic noise.

Acknowledgments

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