Thesis for the Degree of Licentiate of Engineering

Frequency Reconfigurable and Linear Power Amplifiers Based on Doherty and Varactor Load Modulation Techniques

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Gothenburg, Sweden 2016

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ISSN 1652-0769
Technical report MC2-349

Printed by Chalmers Reproservice
Gothenburg, Sweden 2016

Abstract

In future mobile communication networks, there will be a shift towards higher carrier frequencies and highly integrated multiple antenna systems. The system performance will largely depend on the available RF hardware. As such, RF power amplifiers (PAs) with improved efficiency, linearity, and bandwidth are needed. Dynamic load modulation (DLM) is one of the most common PA efficiency enhancement techniques. By investigation of new DLM design techniques, the overall objective of this thesis is to improve the efficiency-linearity and efficiency-bandwidth trade-offs in PAs for future wireless systems.

In the first part of the thesis, a method for improving the frequency agility of varactor-based DLM PAs is proposed. It is demonstrated that class-J operation provides the possibility of enhancing the efficiency for a large dynamic range of powers by means of purely reactive load modulation across a large bandwidth. This allows for very simple realization of a varactor-based tunable output matching network. This ideal analysis of the class-J operation establishes a profound theory behind wideband capabilities of varactor-based DLM PAs. The theory is experimentally verified with a prototype PA using a GaN HEMT and SiC varactors.

In the second part, a method for improving the efficiency-linearity trade-off in Doherty PAs is proposed. The fundamental way the main and auxiliary transistors in the Doherty PA interact with each other is analyzed and generalized. The output combiner is treated as a black-box and its parameters are solved for arbitrary current profiles for the main and auxiliary branches. Solving for maximum efficiency and scaling the conventional current ratios results in new solutions with significantly higher gain. Solving for linear gain and high efficiency, and combining current scaling with reactive mismatch results in the possibility of controlling the phase response in the high power region. This control can be used to compensate the severe inherent phase distortion in Doherty PAs. The theory is experimentally verified with a highly efficient and highly linear prototype PA using GaN HEMTs.

The thesis has presented two promising techniques for improving the efficiency-bandwidth and efficiency-linearity trade-offs in PAs. The results will therefore contribute to the development of more energy efficient and high capacity wireless services in the future.

Keywords: AM/AM, AM/PM, broadband, bandwidth, Class-J, Doherty, dynamic load modulation (DLM), energy efficiency, fifth generation mobile networks (5G), gallium nitride (GaN), linear, microwave, power amplifier (PA), radio frequency (RF), silicon carbide (SiC), varactor, wideband.

List of Publications

Appended Publications

This thesis is based on work contained in the following papers:

[A] W. Hallberg, D. Gustafsson, M. Özen, C. M. Andersson, D. Kuylenstierna, and C. Fager, "A class-J power amplifier with varactor-based dynamic load modulation across a large bandwidth," IEEE MTT-S Int. Microw. Symp. Dig., pp. 1–4, May 2015.

[B] W. Hallberg, M. Özen, D. Gustafsson, K. Buisman, and C. Fager, "A Doherty power amplifier design method for improved efficiency and linearity," accepted for publication in *IEEE Trans. Microw. Theory Techn.*, 2016.

Other Publications

The content of the following publications partially overlaps with the appended papers or is out of the scope of this thesis.

[a] C. Fager, W. Hallberg, M. Özen, K. Andersson, K. Buisman and D. Gustafsson, "Design of linear and efficient power amplifiers by generalization of the Doherty theory," to be presented at *IEEE Radio and Wireless Symp.,* 2017.

[b] W. Hallberg, M. Özen, and C. Fager, "Current scaled Doherty amplifier for high efficiency and high linearity," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–4, May 2016.

[c] W. Hallberg, M. Özen, and C. Fager, "Generalized Doherty power amplifier design equations," *GigaHertz Symposium*, Mar. 2016.

[d] W. Hallberg, M. Özen, and C. Fager, "Class-B/C Doherty power amplifier," Patent application, PCT/EP2015/064919, Jul. 2015.

Notations and Abbreviations

Notations

α	Conduction angle
α_x	Angle where the gate-source voltage v_{GS} reaches V_{TH}
β	Normalized gate-source voltage drive level
β_{bo}	Drive level where the gate-source voltage v_{GS} reaches V_{TH}
η	Drain efficiency
ϕ	The phase $\phi = \omega_0 t$
ω_0	Fundamental angular frequency
g_{ds}	Drain-source conductance
g_m	Transconductance
i_{DS}	Drain-source current, time domain
I_{DS}	Drain-source current, DC component
I_{ds,ω_0}	Drain-source current, fundamental frequency component
$I_{ds,N\omega_0}$	Drain-source current, N:th frequency component
$I_{ds,max}$	Maximum fundamental drain-source current
I_{MAX}	Maximum DC drain-source current
P_{DC}	DC power
P_L	Power delivered to the fundamental load termination
R_L	Fundamental load termination resistance
$\Re$	Function that gives the real part of a complex number
V_{BR}	Breakdown voltage
v_{DS}	Drain-source voltage, time domain
V_{DS}	Drain-source voltage, DC component
V_{ds,ω_0}	Drain-source voltage, fundamental frequency component
$V_{ds,max}$	Maximum fundamental drain-source voltage
v_{GS}	Gate-source voltage, time domain
V_{GS}	Gate-source voltage, DC component
V_K	Knee voltage
V_{SAT}	Saturation voltage
V_{TH}	Threshold voltage
$\mathbb{Z}$	The set of integers

Abbreviations

5G	Fifth Generation Mobile Networks
ACPR	Adjacent Channel Power Ratio
ALM	Active Load Modulation
CW	Continuous Wave
DC	Direct Current
DLM	Dynamic Load Modulation
DSM	Dynamic Supply Modulation
DPD	Digital Pre-distortion
EA	Envelope Amplifier
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
FET	Field-effect Transistor
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
ICT	Information and Communication Technology
IM	Intermodulation
MIMO	Multiple Input Multiple Output
NMSE	Normalized Mean Square Error
OMN	Output Matching Network
OPBO	Output Power Back-off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PWM	Pulse Width Modulation
RBS	Radio Base Station
RF	Radio Frequency
SiC	Silicon Carbide

Contents

Chapter 1

Introduction

The future of humanity is dependent on sustainable development. Sustainable development includes three pillars: economical and social development while preserving the environment. Many efforts are required in all human activities for achieving sustainable development. Information and communication technology (ICT) is evermore present in society and has the potential of both enabling and restraining sustainable development. Therefore, when ICT is developed for meeting future demands, it must be done so responsibly with sustainable development in mind. While the biggest concern of the development of ICT is high energy consumption, the benefits are many. ICT can contribute in many ways to all of three pillars of sustainable development. The contributions are often analyzed in first hand and indirect effects. The first hand economic effects are quite significant. In 2011, the ICT sector, including manufacturing, trade, and services, represented 4% of the total GDP in the EU. That year, 2.7% of all employees in the EU worked in the EU ICT sector, where 91% of those worked for the emerging market of ICT services [1]. ICT also enables faster and better means of communications and access of information, which itself is a great social development. The many indirect effects ICT has on sustainable development have been analyzed by the International Institute for Sustainable Development (IISD) [2]. One example of an indirect effect is ICT enabling distant communication, which is more energy efficient from a transport point of view.

ICT is a broad term including, inter alia, telecommunications, computer technologies and software. Among these, mobile communications is an exponentially growing technology under constant development [3]. This development is pushed by the need of enhancing existing experiences and by the expansion to new use cases. Future demands put new requirements on wireless infrastructures, which in turn put new technical implications on the digital and radio frequency (RF) front end hardware. These technical implications affect all blocks in the wireless infrastructure, both digital signal processing blocks and hardware blocks. In the transceiver block, the RF power amplifier (PA) constitutes among the biggest challenges for future wireless infrastructures [4], making RF PA research crucial for future mobile communications.

RF PAs are not only central in mobile communications, they are also relevant in: other wireless communication systems, such as Bluetooth or WiFi;

other wireless technologies, such as radar [5]; or other microwave technologies, e.g. portable microwave ovens [6]. The PAs in these technologies also share some of the challenges with PAs for future mobile communications.

In order to understand the demands of RF PAs in future mobile networks, the demands of the networks themselves must first be understood. The visions of the next generation mobile networks differ substantially from previous generations, and will be discussed in more detail in the next section.

1.1 The Fifth Generation Mobile Networks

The development of current and past generations of mobile networks, i.e. 0G–4G, were mainly driven by the demand of higher data rates and higher data volumes. The development of the next generation of mobile networks, i.e. 5G, is however, driven by both similar and new demands, arising from new use cases. The demands, required advances of the networks, and technical implications of 5G will be reviewed in this section.

The Next Generation Mobile Networks Alliance (NGMN) [7], the EU Commission initiated The 5G Infrastructure Public Private Partnership (5G PPP) [8], and the GSM Association [9] are some key organizations that have similar visions for the next generation mobile network – 5G. Their visions will be summarized in the paragraphs below.

It is expected that 5G will be rolled out around 2020, and is driven by the following demands:

- The cloud. Existing and new services will utilize the cloud to a great extent. For example: video streaming will increase and employ higher quality; new platforms, such as big data analysis; new and expanded infrastructure, such as virtual machines, servers and storage.
- Ubiquitous connectivity. Reliable connectivity will be expected everywhere, e.g. demanding ventures, public spaces, and trains. In addition, ubiquitous connectivity is needed for internet of things (IoT), smart homes, and wearable technology.
- Smart infrastructure. New emerging technologies such as autonomous vehicles, smart cities (smart grid), and critical control of remote devices.

The future demands require the following advances by 5G systems:

- More connected devices
- Higher mobile data volume
- Higher data rate
- Lower energy consumption
- Lower latency
- Improved mobility
- Guaranteed performance

These requirements will have many technical implications on the wireless systems. Some examples are:

- Diverse services and devices. The vast amount of different devices and different scenarios will have very different requirements, e.g. output power and data rate requirements will differ significantly between IoT devices

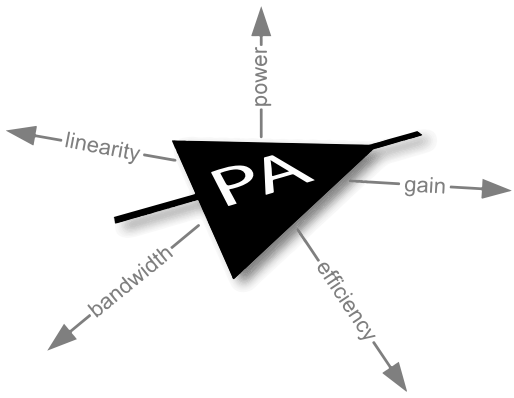


Figure 1.1: The PA designer's dilemma of property trade-offs.

and cell phones. Improved spectral efficiency will be achieved by higher order of modulation, by multiple input multiple output (MIMO) systems, and massive MIMO systems.

- Diverse spectrum. In order to support higher data rates, much higher signal bandwidths will be employed. This will lead to increased usage of higher operational frequencies. Lower frequency bands will also be maintained due to previously defined standards, different requirements (e.g. IoT), improved spectral efficiency, and spectrum sharing. The fragmented spectrum may also necessitate inter-band carrier aggregation.

- Diverse deployments. The deployment will be diversified beyond macro-, micro- and pico-base stations.

It is also important to know that there will be no successful employment of the future wireless systems if the cost is too high.

The diverse nature of 5G and related wireless systems naturally necessitate a diverse set of requirements of future PAs, which are discussed in the next section.

1.2 RF Power Amplifier Challenges

In a transmitter, the function of the PA is to amplify the signal power to a sufficient level for achieving a certain system performance at a given link distance. From a system perspective, the five most important properties of the PA are: output power, energy efficiency, gain, linearity and bandwidth. As in all circuit design, PA design is dictated by trade-offs: improving one property will often compromise another. This design dilemma is illustrated in Figure 1.1. How these trade-offs between PA properties are made will naturally depend on the particular application in a future wireless system. In this section, the different PA properties will be discussed in terms of importance and the challenges they impose. After that, implications of increasing the frequency of operation, and of increasing number of antennas (i.e. in MIMO systems) in the transmitter will be discussed.

1.2.1 PA Properties

The output power of the PA determines system performance for a given link distance, or the link distance for a given system performance.

The linearity of the PA is an essential property. Non-linear amplitude and phase responses result in unwanted in-band distortion and spectral regrowth. A PA operating in its most energy efficient mode typically presents a very non-linear behavior. Since systems often have strict linearity requirements, either the raw linearity of the PA must be improved, or it can be linearized - digitally or by analog circuitry. For conventional PAs, backing off the output power level typically increases linearity but at a great energy efficiency cost. Linearization techniques allow the PA to operate in a high energy efficient mode with improved linearity. Linearization does, however, increase complexity and reduce system energy efficiency somewhat compared to the maximum efficiency of a non-linear PA.

The energy efficiency of the PA is of utmost importance since it is one of the most power hungry components in the transmitter [10, 11]. Low energy efficiency results in high operational cost, high heat dissipation and large environmental footprint. Heat dissipation in the PA could result in many problems, e.g. failure or short life cycle. The total environmental footprint of ICT is a growing concern worldwide [12].

The gain of the PA is important for amplifying the signal power level from the previous block in the transmitter to the required output power level. In the transmitter, the signal is often amplified by a chain of individual PAs to obtain the required gain. The energy efficiency of the PA chain will be dominated by the efficiency of the end stage PA (the last PA in the chain) and its gain.

The bandwidth is another important attribute. The diversity of carrier frequencies requires either different PAs per band or fewer broadband PAs. Many different PAs require a larger size, resulting in higher material consumption, higher cost and less practical deployment. On the other hand, with known techniques, it is not an easy task to maintain an acceptable PA performance across large RF bandwidths. High signal bandwidths also necessitate high bandwidth PAs. High signal bandwidth increases cost and complexity of digital signal processing (DSP), e.g. linearization, which could make other PA properties more important, e.g. linearity.

1.2.2 Future PA Challenges

Increasing the operational frequency is necessitated by the need of larger spectrum allocation and the need of larger signal bandwidths. To increase the operational frequency, transistor technologies with higher cutoff frequencies f_T are required. For a simplified field effect transistor (FET) model, f_T is inversely proportional to the gate-source capacitance [13]. To increase the operational frequency of a transistor technology, this capacitance must be reduced. However, reducing this capacitance introduces unwanted effects, e.g. short channel effects, lower breakdown voltage and increased gate-drain leakage in FETs. In addition, it may not be possible to scale all transistor parasitics or complementary passive elements at the same rate as the gate-source capacitance. As a result, PA design becomes more challenging as the operational frequency is increased. Low break-down voltage of the transistor makes it challenging

to reach high-enough output powers. Since the output power is prioritized, other PA properties are often severely compromised. In addition, the unwanted effects of increasing f_T typically reduces energy efficiency, gain and linearity.

In MIMO transmitters, each antenna typically is driven by its own PA – for efficiency and practical reasons. When going towards massive MIMO, i.e. letting the number of antennas go to several hundreds, the PA requirements are affected in interesting ways in theory. However, increasing the number of antennas increases the complexity of the transmitter and especially the receiver. Detailed information about current and future MIMO technology can be found in [14, 15]. Splitting the output power to several PA-antenna branches reduces the output power requirements of each individual PA, which could facilitate the PA design. In addition, energy focus possibilities (coherent superposition) in MIMO could reduce output power requirements [15]. The reduced output power level requirements of each individual PA enables the use of silicon technology for the PAs, which enables a higher level of integration, imposing both new possibilities as well as new design challenges. It can also be mentioned that it is possible to reduce the signal peak to average power ratios (PAPR) in massive MIMO [16, 17], which significantly relaxes efficiency requirements of the individual PAs, possibly making the transmitter more energy efficient. Cross-talk between antennas might reduce PA linearity, but when the number of antennas increases, averaging effects might occur out of band [18].

Other PA challenges arising from increasing frequency or from increasing the number of antennas in a MIMO system are difficulties in measurements and modelling. As the operational frequency increases, cost typically goes up and accuracy typically goes down, due to, for example, sensitivity to coupling and high loss passives. As a result, it can be difficult to extract accurate transistor and system models.

All PA challenges discussed above relate cost in some ways. An important aspect in keeping the cost down is the integration capability of the PA. To integrate different function blocks in the transmitter is crucial for small size and cost in general. In addition, as the frequency increases, the process cost typically increases, making compact designs crucial.

All PA properties are deeply connected to each other and trade-offs always have to be made. It is often very difficult to determine which trade-offs should be made for the most cost- and complexity-efficient solution for a certain application. Therefore, PA research consists of concurrently improving PA properties and reducing trade-offs.

1.3 Thesis Contributions

There are many different PA design strategies for meeting future mobile communications demands. In Chapter 2, the most common PA topologies are discussed and relevant theoretical background is provided. Focus is put on the dynamic load modulation (DLM) category of PA efficiency enhancement techniques, which is the main target of this thesis. The research goal of this thesis is to improve the efficiency-bandwidth trade-off, and the efficiency-linearity trade-off in PA designs.

Varactor-based DLM is an interesting but somewhat unexplored area in load modulation, particularly bandwidth capabilities. Chapter 3 introduces, based on [Paper A], a method for maintaining high efficiency performance enabled by varactor-based DLM across a large RF bandwidth, improving the efficiency-bandwidth trade-off in PA design.

In Doherty PAs, efficiency enhancement is also achieved via DLM. It is a widely used PA architecture due to its simplicity and high efficiency performance. It has been extensively studied and many technical advancements have been achieved. However, a remaining inherent unwanted property of the Doherty PA architecture is poor linearity, which presents problems when digital linearization is constrained, e.g. in MIMO systems. Chapter 4 presents a generalized Doherty PA theory which vastly increases the design space. New solutions with higher gain, and new solutions with an improved efficiency-linearity trade-off [Paper B] are identified.

The implications of the advancements presented in this thesis are, together with possible future work, discussed in Chapter 5.

Chapter 2

Power Amplifier Fundamentals

In order to meet future wireless ICT demands, many different strategies for PA design have been implemented. Energy efficiency enhancement is on the top of the list of required attributes, and it can be accomplished by different techniques that comes with different pros and cons. This chapter will give a brief overview of the most common energy efficiency enhancement techniques.

First, the ideal transistor is defined. This is needed to properly describe the different modes of operation a PA can have. The transconductance modes of operation are described in detail, which is much required for the PA advancements described in Chapter 3 and 4. Then, switch-mode type of operation is mentioned briefly. Finally, the most common energy efficiency enhancement techniques are discussed.

2.1 The Ideal Transistor

Throughout this thesis, all notations for transistors will use FET terminology, although all derivations are valid for any technology. One of the simplest ways of modelling a FET is with a piece-wise linear current source, see Figure 2.1. The drain source current i_{DS}[1] is then a separable function f of the gate voltage v_{GS} and the drain voltage v_{DS}, i.e.

$$i_{DS} = f(v_{GS}, v_{DS}) = f_{GS}(v_{GS}) f_{DS}(v_{DS}). \tag{2.1}$$

The separated functions are given by

$$f_{GS}(v_{GS}) = \begin{cases} 0 & \text{if } v_{GS} < V_{TH} \\ g_m(v_{GS} - V_{TH}) & \text{if } V_{TH} \leq v_{GS} \leq V_{SAT} \\ I_{MAX} & \text{if } V_{SAT} < v_{GS} \end{cases}, \tag{2.2}$$

[1]Throughout this thesis, signals will be denoted the following way. Time domain: lower case letter with upper case subscripts (v_{DS}). DC component: upper case letter with upper case subscripts (V_{DS}). Frequency components: upper case letter with lower case subscripts (V_{ds}).

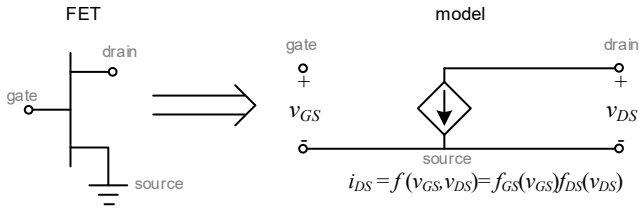


Figure 2.1: A FET can be modelled with a piece-wise linear current source.

$$f_{DS}(v_{DS}) = \begin{cases} 1/V_K \cdot v_{DS} & \text{if } 0 < v_{DS} < V_K \\ 1 + g_{ds}\,(v_{DS} - V_K)\,/I_{MAX} & \text{if } V_K \leq v_{DS} \leq V_{BR} \end{cases}, \tag{2.3}$$

and are demonstrated in Figure 2.2. The function f_{GS} is bounded by the threshold voltage V_{TH}, i.e. the gate voltage where the transistor starts to conduct, and the saturation voltage V_{SAT}, i.e. the gate voltage that yields the maximum (saturated) current I_{MAX}, which can be expressed as

$$I_{MAX} = g_m(V_{SAT} - V_{TH}), \tag{2.4}$$

where g_m is the transconductance. Moreover, g_m is the derivative, or slope, of f_{GS} in the region between V_{TH} and V_{SAT}. The function f_{DS} is bounded by the knee voltage V_K and the break down voltage V_{BR}. In the region $0 < v_{DS} < V_K$, the slope of f_{DS} is $1/V_K$, and in the region $V_K \leq v_{DS} \leq V_{BR}$, the slope is given by the conductance g_{ds} over I_{MAX}. For simplicity, V_K and g_{ds} are often set to zero. It is justified since it does not change any of the general conclusions regarding the conventional PA classes. From here on, it is assumed that $V_K = g_{ds} = 0$. The DC-characteristics, or IV-curves, which are the drain DC currents I_{DS} versus the drain DC voltage V_{DS} for different gate DC voltages V_{GS}, are plotted in Figure 2.3, both for non-zero V_K and g_{ds}, and $V_K = g_{ds} = 0$.

Modelling a transistor according to the method described above does not reflect the full, complex behavior of a real transistor, but is extremely useful for describing circuit design concepts. It is often a very good starting point to explore concepts on the ideal transistor level, and then expand them to more realistic scenarios. More complete transistor models describe a more complex non-linear current source and include many non-linear parasitics. For more details on transistor modelling, see [19].

2.2 Power Amplifier Modes

In this section, the most common different transconductance-mode and switch-mode operations of PAs are described. The most important attributes of a particular mode are its drain current and drain voltage waveforms. Ideal waveforms are calculated from the ideal transistor model and with control of an infinite amount of harmonics. The ideal waveforms are very useful for studying concepts and are a good starting point for many circuit designs. In reality, it is impossible to mimic the ideal waveforms perfectly because harmonic control is limited, especially as the frequency of operation is increased, and because of non-linearities. However, the non-ideal waveforms of real circuits typically do not degrade performance significantly compared to the ideal cases.

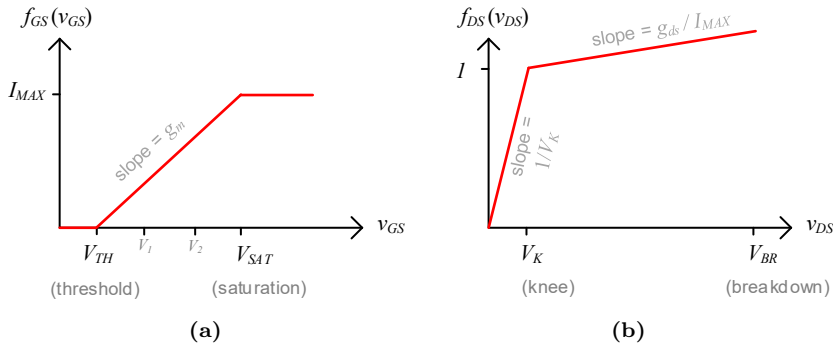


Figure 2.2: The separated functions in a piece-wise linear current source.

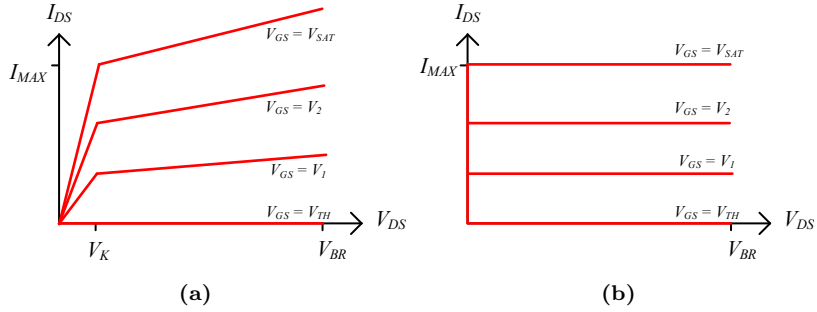


Figure 2.3: The DC-characteristics of (a) a piece-wise linear current source and (b) a piece-wise linear current source with $g_{ds} = 0$ and $V_K = 0$.

2.2.1 Transconductance Power Amplifiers

In the conventional PA classes, the input is driven by the voltage

$$v_{GS} = V_{GS} + \beta V_{gs,max} \sin(\omega_0 t), \tag{2.5}$$

where V_{GS} is the selected gate DC bias voltage, ω_0 is the fundamental angular frequency, β $(0 \leq \beta \leq 1)$ is the normalized gate-source voltage drive level, and $V_{gs,max} = V_{SAT} - V_{GS}$ is the maximum fundamental gate RF voltage swing.

The amplifier classes A, AB, B and C are defined by the voltage and current waveforms at the transistor current source. More specifically, all classes have a purely sinusoidal voltage waveform but differ by the conduction angle, α, of the current waveform at maximum drive level ($\beta = 1$), see Figure 2.4. These waveforms can also be demonstrated by load lines, i.e. i_{DS} versus v_{DS} plotted on top of the IV-curves, see Figure 2.5. The wanted waveforms are achieved by choosing proper gate bias and proper load terminations. The gate bias is selected as

$$V_{GS} = \frac{V_{TH} - V_{SAT} \sin(\frac{\pi-\alpha}{2})}{1 - \sin(\frac{\pi-\alpha}{2})}. \tag{2.6}$$

The drain bias level V_{DS} is selected as

$$V_{DS} = \frac{V_{BR} + V_K}{2}. \tag{2.7}$$

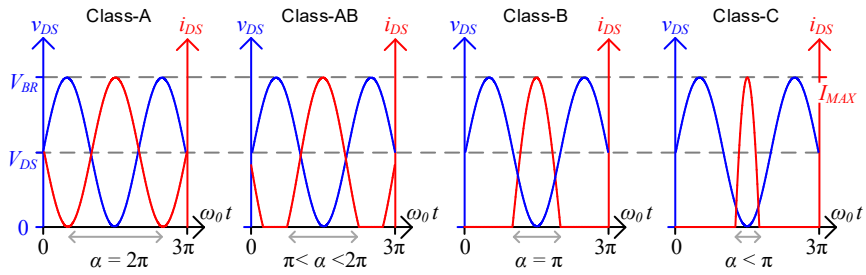


Figure 2.4: The voltage and current waveforms for the amplifier classes A, AB, B and C, at the drive level $\beta = 1$. All have a purely sinusoidal voltage waveform but differ by the conduction angle, α, of the current waveform.

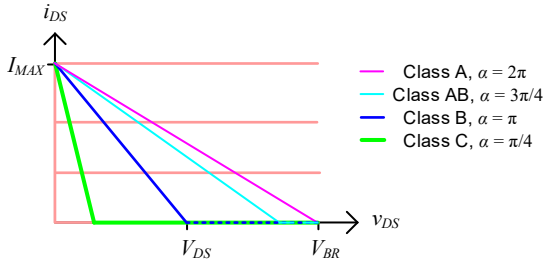


Figure 2.5: Load lines on top of IV-curves for class-A, AB, B, and C at maximum drive level ($\beta = 1$). Class-AB and -C are continuums of conduction angles but are represented with fixed values in the figure.

The purely sinusoidal drain voltage waveform is achieved by short circuiting eventual harmonic frequency content. The fundamental load termination R_L is selected for maximum possible fundamental drain voltage, $V_{ds,max} = V_{DS} - V_K$, at maximum drive level, i.e.

$$R_L = \frac{V_{ds,max}}{I_{ds,max}}, \tag{2.8}$$

where $I_{ds,max}$ is the maximum fundamental drain current, which can be found from Fourier series expansion of i_{DS}.

For class-A and -AB ($V_{GS} > V_{TH} \Leftrightarrow \alpha > \pi$), the time domain drain current can be expressed as

$$i_{DS}(\beta, \beta_{bo}) = \begin{cases} \frac{I_{MAX}}{1+\beta_{bo}} \left(\beta \sin(\omega_0 t) + \beta_{bo}\right) & \text{if } 2n\pi + \alpha_x \leq \omega_0 t \leq (2n+1)\pi - \alpha_x \\ 0 & \text{if } (2n-1)\pi - \alpha_x < \omega_0 t < 2n\pi + \alpha_x \end{cases}, \tag{2.9}$$

where $n \in \mathbb{Z}$ and

$$\sin(\alpha_x) = -\frac{\beta_{bo}}{\beta}. \tag{2.10}$$

For class-B and -C ($V_{GS} \leq V_{TH} \Leftrightarrow \alpha \leq \pi$), the time domain drain current can be expressed as

$$i_{DS}(\beta, \beta_{bo}) = \begin{cases} \frac{I_{MAX}}{1-\beta_{bo}} \left(\beta \sin(\omega_0 t) - \beta_{bo}\right) & \text{if } 2n\pi + \alpha_x \leq \omega_0 t \leq (2n+1)\pi - \alpha_x \\ 0 & \text{if } (2n-1)\pi - \alpha_x < \omega_0 t < 2n\pi + \alpha_x \end{cases}, \tag{2.11}$$

where $n \in \mathbb{Z}$ and

$$\sin(\alpha_x) = \frac{\beta_{bo}}{\beta}. \tag{2.12}$$

The parameter α_x is the angle where the gate-source voltage v_{GS} reaches V_{TH}. β_{bo} is the drive level where v_{GS} first reaches V_{TH}, and is given by

$$\beta_{bo} = \frac{|V_{TH} - V_{GS}|}{V_{gs,max}}. \tag{2.13}$$

The conduction angle α can also be expressed as

$$\alpha = \pi - 2\alpha_x. \tag{2.14}$$

A Fourier series expansion gives the frequency components. For class-A and -AB, the DC and fundamental components are

$$I_{DS}(\beta, \beta_{bo}) = F_A \Re\left\{ \beta\sqrt{1 - \frac{\beta_{bo}^2}{\beta^2}} + \beta_{bo}\pi - \beta_{bo}\cos^{-1}\frac{\beta_{bo}}{\beta} \right\}, \tag{2.15}$$

$$I_{ds,\omega_0}(\beta, \beta_{bo}) = -jF_A \Re\left\{ \beta_{bo}\sqrt{1 - \frac{\beta_{bo}^2}{\beta^2}} + \beta\pi - \beta\cos^{-1}\frac{\beta_{bo}}{\beta} \right\}, \tag{2.16}$$

where

$$F_A = \frac{I_{MAX}}{(\beta_{bo} + 1)\pi}. \tag{2.17}$$

Higher harmonics are given by

$$I_{ds,N\omega_0}(\beta, \beta_{bo}) = -F_A 2e^{-j\frac{N\pi}{2}} \Re\Bigg\{ \beta\sqrt{1 - \frac{\beta_{bo}^2}{\beta^2}} N\cos\Big(N\big(\pi - \cos^{-1}\frac{\beta_{bo}}{\beta}\big)\Big) + \beta_{bo}\sin\Big(N\big(\pi - \cos^{-1}\frac{\beta_{bo}}{\beta}\big)\Big) \Bigg\} \Big/ \big(N(N^2-1)\big), \tag{2.18}$$

where the integer $N \geq 2$. For class-B and -C, the DC and fundamental components are

$$I_{DS}(\beta, \beta_{bo}) = F_B \Re\left\{ -\beta\sqrt{1 - \frac{\beta_{bo}^2}{\beta^2}} + \beta_{bo}\cos^{-1}\frac{\beta_{bo}}{\beta} \right\}, \tag{2.19}$$

$$I_{ds,\omega_0}(\beta, \beta_{bo}) = -jF_B \Re\left\{ \beta_{bo}\sqrt{1 - \frac{\beta_{bo}^2}{\beta^2}} - \beta\cos^{-1}\frac{\beta_{bo}}{\beta} \right\}, \tag{2.20}$$

where

$$F_B = \frac{I_{MAX}}{(\beta_{bo} - 1)\pi}. \tag{2.21}$$

Higher harmonics are given by

$$I_{ds,N\omega_0}(\beta, \beta_{bo}) = F_B 2e^{-j\frac{N\pi}{2}} \Re\Bigg\{ \beta\sqrt{1 - \frac{\beta_{bo}^2}{\beta^2}} N\cos\Big(N\cos^{-1}\frac{\beta_{bo}}{\beta}\Big) - \beta_{bo}\sin\Big(N\cos^{-1}\frac{\beta_{bo}}{\beta}\Big) \Bigg\} \Big/ \big(N(N^2-1)\big), \tag{2.22}$$

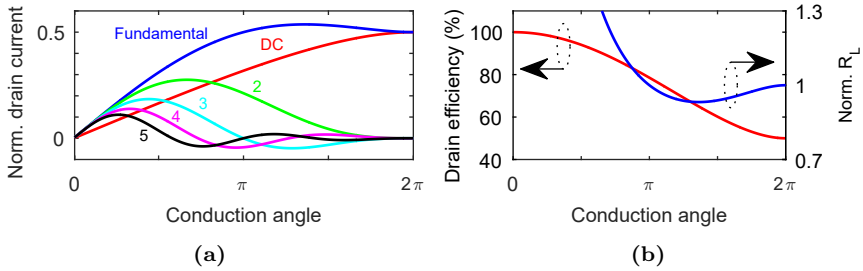


Figure 2.6: PA characteristics versus conduction angle when $\beta = 1$. (a) Presents normalized DC- and five first harmonic frequency components of the drain current, and (b) presents drain efficiency and normalized fundamental load termination R_L. The frequency components are normalized with I_{MAX}. R_L is normalized with the class-A fundamental load termination.

where the integer $N \geq 2$.

With the transistor current completely defined, PA characteristics can now be studied. PA characteristics versus conduction angle when $\beta = 1$ are presented in Figure 2.6. The figure presents normalized DC- and five first harmonic frequency components of the drain current, drain efficiency η and normalized fundamental load termination R_L. The current frequency components are normalized with I_{MAX}. R_L is normalized with the class-A fundamental load termination. The drain efficiency is defined as

$$\eta = \frac{P_L}{P_{DC}}, \tag{2.23}$$

where P_L is the fundamental power delivered to the fundamental load termination R_L. When the conduction angle goes to zero, the drain efficiency goes to 100%, the current goes to zero (thus also P_L), and R_L goes to infinity. PA characteristics versus drive level for class-A, -AB, -B and -C is presented in Figure 2.7. The figure presents DC- and fundamental currents normalized with I_{MAX}. Note that only class-A and -B present a linear fundamental current. In Figure 2.8, gain and drain efficiency are presented for the four classes versus delivered power. The gain is normalized with the class-A gain; the delivered powers are normalized with their maximum value. Note that the gain decreases as the conduction angle decreases. Also note that the drain efficiency decreases more rapidly as the delivered power is backed-off for high conduction angles. In summary: class-A presents linear and high gain, but low drain efficiency with a rapid decrease when the delivered power is backed off; class-AB presents slightly higher delivered power and slightly higher drain efficiency than class-A, but has a non-linear gain; class-B presents linear gain 6 dB lower than class-A, the same delivered power as class-A, and high drain efficiency with a slower decrease when the delivered power is backed off compared to class-A; class-C presents the highest drain efficiency, but low, non-linear gain and low delivered power.

Another mode of transconductance PAs is class-J [20]. It is a mode similar to class-B, but it utilizes the transistor's parasitic output capacitance and presents complex impedances to the current source. Class-J has the same drain efficiency and linearity as class-B, but with very peculiar waveforms at the current source. Class-J will be discussed in more detail in the next chapter.

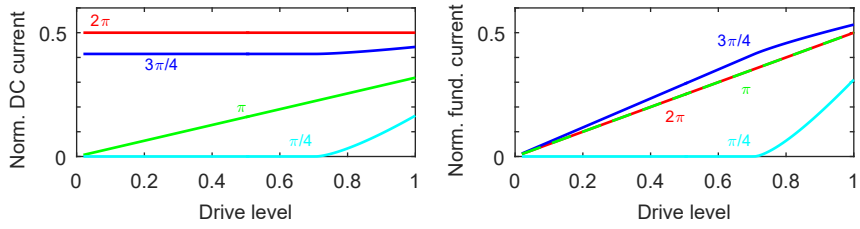


Figure 2.7: PA characteristics versus drive level for class-A ($\alpha = 2\pi$), -AB ($\alpha = 3\pi/4$), -B ($\alpha = \pi$) and -C ($\alpha = \pi/4$). (a) Presents DC currents and (b) presents fundamental currents, all normalized with I_{MAX}.

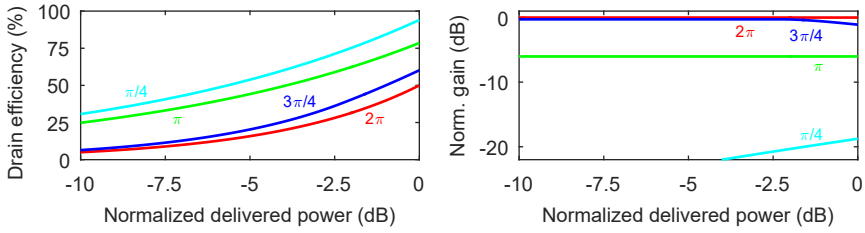


Figure 2.8: PA characteristics versus delivered power for class-A ($\alpha = 2\pi$), -AB ($\alpha = 3\pi/4$), -B ($\alpha = \pi$) and -C ($\alpha = \pi/4$). (a) Presents drain efficiency and (b) presents gain normalized with the class-A gain. The delivered powers are normalized with their maximum value.

2.2.2 Switch-mode Power Amplifiers

In switch-mode type of operation, the drain current and voltage waveforms never overlap. This results in a drain efficiency of 100% for the ideal transistor. Common classes of switch-mode PAs are class-D, D^{-1}, E, F, and F^{-1}. The load line of a switch-mode PA is presented in Figure 2.9(a). The waveforms of class-F and -F^{-1} are presented in Figure 2.9(b). For class-F, the current waveform is achieved with class-B bias, and the voltage waveform is achieved by presenting short circuit to even harmonics and open circuit to odd harmonics. For class-F^{-1}, the current waveform is achieved by driving the input with a square voltage wave, and the voltage waveform is achieved by presenting open circuit to even harmonics and short circuit to odd harmonics. Class-D and -D^{-1} generate the same waveforms as Class-F and -F^{-1}, but with a push-pull configuration. Class-E is a single ended switch-mode PA that generates non-overlapping waveforms. Class-E is one of the most common switch-mode PAs due to its simple realization. General information about switch-mode PAs can be found in [20,21]. Detailed information about class-E can be found in [22–25].

2.3 Energy Efficiency Enhancement Techniques

In the evolution of wireless communication systems, the need for higher spectral efficiency has resulted in higher order modulation schemes [26]. The large amplitude modulation of these schemes results in a large difference between

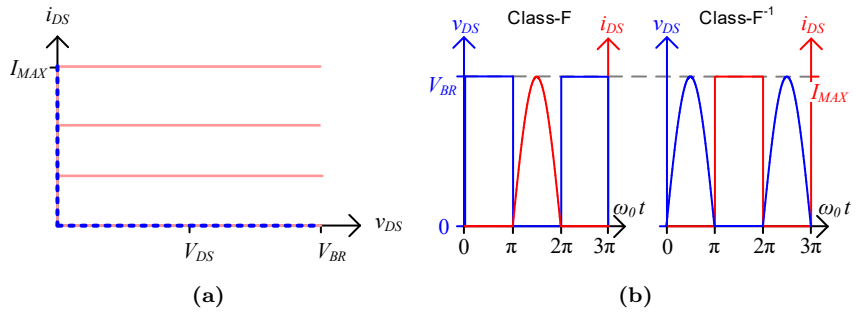


Figure 2.9: (a) Load line of a switch-mode PA and (b) the waveforms of class-F/-F^{-1}.

the signal peak power and the average power. For example, in LTE-Advanced, a single downlink carrier has roughly 9 dB PAPR, and up to 12 dB PAPR for a two-carrier aggregation [27].

The large variations in the instantaneous transmitted power result in severe degradation of the average energy efficiency of conventional PAs, since the PA has to operate at the average power to avoid clipping of the signal. This is because the drain efficiency is reduced as the delivered power is backed off, see Figure 2.8 (a). The drain efficiency is given by

$$\eta = \frac{P_L}{P_{DC}} = \frac{0.5 R_L |I_{ds,\omega_0}|^2}{V_{DS} I_{DS}}. \tag{2.24}$$

For class-B, both the fundamental drain current I_{ds,ω_0} and the DC current I_{DS} are proportional to the drive level β. As a result, the drain efficiency is proportional to β, i.e.

$$I_{ds,\omega_0} \sim \beta \text{ , and } I_{DS} \sim \beta \;\Rightarrow\; \eta \sim \beta. \tag{2.25}$$

Thus, the drain efficiency is maximum at maximum drive level and decreases as the drive level decreases.

To address the problem of low average energy efficiency of the PA for signals with high PAPR, different methods of making the drain efficiency less dependent on the delivered power have been implemented. The two most common categories of energy efficiency enhancement techniques are dynamic supply modulation (DSM) and dynamic load modulation (DLM). The various energy efficiency enhancement techniques come with different benefits and disadvantages, and are suitable for different applications. DSM and DLM will be discussed in more detail in this section. Although both categories can be implemented with PAs operating in any class, they will, for simplicity, be demonstrated with class-B mode transistors. It should also be mentioned that other types of high energy efficiency PA configurations exist, which fully exploit switch-mode PAs. Examples of such are class-S [28, 29] or pulse width modulation (RF-PWM) [30–32]. These are, however, out of scope of this thesis.

2.3.1 Dynamic Supply Modulation

The first presented DSM technique is envelope elimination and restoration (EER) [33]. EER is a polar transmitter, where the PA is fed with a phase only modulated signal, and the drain bias modulation introduces the amplitude modulation of the signal [34]. Nowadays, the most common DSM technique

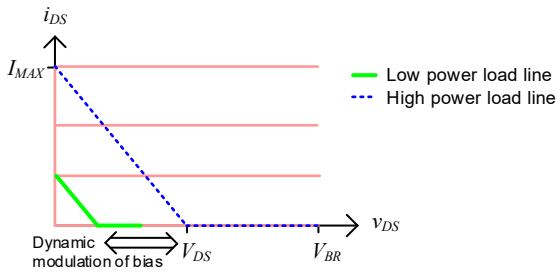


Figure 2.10: Load lines for supply modulation. The drain bias is modulated dynamically as a function of the drive level.

is envelope tracking (ET), where a both phase and amplitude modulated RF signal is fed to the PA, and the drain bias is dynamically modulated along with the envelope variations of the input signal [35, 36]. In other words, V_{DS} is made proportional to the drive level β, i.e.

$$V_{DS} \sim \beta. \tag{2.26}$$

As a result, the drain efficiency becomes independent of β. The DSM principle is illustrated in Fig. 2.10. It is however important to recognize the limits of the ideal transistor model here. For real transistors, the drain efficiency of DSM PAs can be approximated by the following equation [37, 38]:

$$\eta = \frac{\eta_{max}}{1 + \zeta_1 \frac{R_{ON}}{R_L}}, \tag{2.27}$$

where η_{max} denotes the maximum possible drain efficiency for the operation of
the drain efficiency degradation for low values of V_{DS}, and increases as the drive level is backed-off in ET. R_{ON} was not included in the transistor model when the conventional PA classes were derived, but must be included when the drain bias is modulated. ζ_1 is a constant depending on the current and voltage waveforms, i.e. a constant depending on the operation of choice, e.g. 2 for class-B. It is also important to mention that the envelope amplifier (EA) providing the supply modulation constrains the performance of the whole circuit. For example, the EA consumes power and will therefore degrade the energy efficiency of the whole circuit. Bandwidth limitations of the EA will limit signal bandwidth capabilities of the whole circuit [39].

ET is the preferred architecture for handsets due to, inter alia, its large RF bandwidth and its superb energy efficiency [40]. ET does however have limited signal bandwidth and output power capabilities. Although, much effort is put into improving these properties, e.g. [41].

2.3.2 Dynamic Load Modulation

In DLM, the fundamental load termination is dynamically modulated inversely to the envelope variations of the signal. In other words, R_L is made inversely proportional to the drive level β, i.e.

$$R_L \sim 1/\beta. \tag{2.28}$$

As a result, the drain efficiency becomes independent of β. The DLM principle is illustrated in Fig. 2.11. Again, it is important to recognize the limits of the

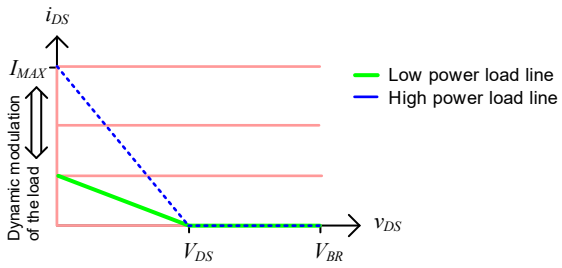


Figure 2.11: Load lines for load modulation. The fundamental load termination resistance is modulated dynamically as an inverse function of the drive level.

ideal transistor model. For real transistors, the drain efficiency of DLM PAs can be approximated by the following equation [37, 42]:

$$\eta = \frac{\eta_{max}}{1 + \zeta_2 \omega_0^2 C_{ds}^2 R_P R_L}, \tag{2.29}$$

where C_{ds} and R_P are in series elements representing parallel losses at the transistor output. ζ_2 is a constant depending on the current and voltage waveforms. It is easy to see how the drain efficiency enhancement at backed-off power levels is limited as R_L increases.

DLM can be divided into varactor-based DLM and active current injection-based DLM - also called active load modulation (ALM). Varactor-based DLM utilizes varactors to tune the load [43], whereas ALM utilizes active current injection to tune the load, as in for example outphasing [44–46] and the Doherty PA [47–49]. In ALM, a second (or peaking, or auxiliary) transistor modulates the load of a first (or carrier, or main) transistor by current injection. In fact, both transistors will load modulate each other when their output currents are combined. In outphasing, the currents from both transistors typically have the same amplitude, and the load modulation is achieved by a phase variation of the two currents. For the Doherty PA, it is the other way around: the phase difference is constant and the load modulation is achieved by an variation of the amplitude ratio of the two currents. It can also be mentioned that a continuum between outphasing and the Doherty PA exists [50, 51].

Varactor-based DLM has high power capabilities and the tunable elements may also be utilized for other purposes in addition to modulating the load, e.g. compensate for antenna mismatch [52]. Conventional class-B based varactor-based DLM PAs typically present low RF bandwidth. However, in Chapter 3 a method for a frequency reconfigurable varactor-based DLM design is presented.

For radio base stations (RBSs), the Doherty PA is the dominating architecture, thanks to its simplicity, high output power and high signal bandwidth capabilities. One draw-back for the conventional Doherty PA operation is the limited RF bandwidth. This is, however, less of a problem if the operation is modified [53–55]. Another drawback is linearity. The Doherty PA heavily relies on linearization by digital pre-distortion (DPD) to achieve necessary linearity requirements. DPD increases complexity and cost, which limits its usage in some applications. In its simplest configuration, the Doherty PA also suffers from severe gain degradation. In Chapter 4, a continuum of new Doherty PA solutions are derived, enabling a large design space. Doherty PA solutions with improved linearity and solutions with higher gain are identified.

Chapter 3

Varactor-based Dynamic Load Modulation Across a Large RF Bandwidth

In the DLM category of energy efficiency enhancement techniques, the outphasing architecture was first introduced in 1935 by H. Chireix [44], and the Doherty architecture was first introduced in 1936 by W. H. Doherty [47]. These two architectures have been extensively studied. Varactor-based DLM is a more recent architecture, proposed in 2003 by F. H. Raab [43]. Therefore, varactor-based DLM is comparatively unexplored and is a highly interesting architecture to examine for future PA demands.

This chapter reviews important varactor-based DLM advances made since [43], with an emphasis on reconfigurable wideband designs. Different reconfigurable wideband trends, including [Paper A], are discussed and compared. The strategy in [Paper A] is then explained and discussed in more detail.

3.1 Conceptual Overview

In varactor-based DLM, the varactors are used for tuning the output matching network (OMN) to present energy efficiency optimal impedances to the transistor for a dynamic range of delivered powers - following the envelope of the signal. This significantly increases the average energy efficiency of the PA for envelope varying signals. The varactor-based DLM operation is illustrated in Figure 3.1. The capacitive value of the varactor is tuned by the voltage across the varactor. This voltage is controlled by a high speed and highly efficient voltage amplifier. In contrast to DSM, this signal envelope tuning does not affect transmitter energy efficiency significantly, since the voltage amplifier only provides an insignificant amount of power. Tunable OMNs can also have other uses. They can also be used to compensate for antenna mismatch, for increasing power transfer [56] or for improving digital linearization [57]. Compensating for antenna mismatch can also be used concurrently with DLM [52]. It has also been shown that the load modulation enabled by varactor-based DLM can be selected for linearity improvements [58, 59].

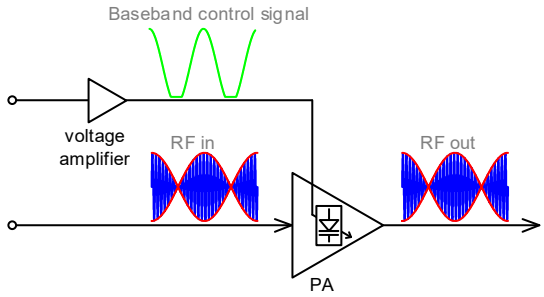


Figure 3.1: Vararctor-based dymaic load modulation architecture.

The PA in [43] utilizes a T-network for achieving load tuning close to the ideal trajectory for a class-E operated transistor, allowing a simple realization of the tunable OMN with only a single voltage control. In [59], it was shown that the optimum load trajectory of class-B requires two separate varactor controls, which increases the circuit complexity. In many designs, e.g. [60–62], however, optimum load trajectories have been found empirically by load pull measurements, resulting in limited understanding of the best way of realize the tunable OMN.

In [63], it was showed that in class-J operation, the optimum load trajectory can be selected as purely reactive, making it possible to realize the DLM with a single varactor control. It was also shown that a simple transistor model, only including a linear current source and shunt output capacitor, can predict optimum load trajectories of a GaN HEMT at 2.14 GHz very well. Thus, a profound theoretical background of the DLM operation was established, allowing for an analysis of performance trade-offs, realization and varactor requirements.

Low breakdown voltage of varactors limited the delivered power in early varactor-based DLM PA designs, but as new varactors with higher breakdown voltage while maintaining tuning capabilities emerged, delivered power levels have been scaled up to 86 W [64].

3.2 Literature Review

If a single varactor control signal is used for DLM across a large bandwidth, the varactor must present high tuning capabilities. A tunable matching network consisting of two varactor control signals allows the tuning capabilities of the varactors to reduced significantly, but at the cost of circuit complexity. The first multi-band varactor-based DLM PA, employing two varactor control signals, was demonstrated in [65]. It utilizes a 2 W SiGe HBT and operates at 0.9, 1.8, 1.9 and 2.1 GHz. Due to losses in the tunable OMN, the maximum delivered power of the PA is reduced to 28 dBm across the bands. For the three higher bands, the PA presents a drain efficiency of 40–45% at 6 dB OPBO, whereas at the lowest frequency band, the PA presents ∼19%. The PA in [65] is an important milestone for reconfigurable wideband varactor-based DLM PAs that showed the architectures possibilities. The fundamental design idea of the paper does not compromise delivered power or efficiency across a large

frequency span, but the realization became constrained by the losses in the tunable OMN.

In [66], single varactor control tunable OMN is employed. The effective tuning range is increased by reconfiguring the drain bias versus frequency. The PA utilizes a 25 W GaN HEMT operating from 1.0–1.9 GHz and presents a drain efficiency of 50–62% at 6 dB OPBO across the band. The reconfiguring of the drain bias does however reduce the maximum delivered power to ∼40 dBm across the band.

In [67], the PA employs a single varactor control tunable OMN that serves two functions: apply DLM across a sub-band (0.9–1.0 GHz), and reconfigure the OMN for conventional operation across another band (0.60–0.85 GHz). The PA is based on a 10 W GaN HEMT. It was shown that the static drain supply voltage could be optimized for each frequency in the band for improved efficiency without compromising delivered power. After this optimization, the PA presents an average power added efficiency (PAE) of 45–48% for 0.9–1.0 GHz and 30–38% for 0.60–0.85 GHz, for a 7 dB PAPR LTE signal at an average delivered power of ∼35 dBm.

In [68], a dual band DLM PA employing single varactor control tunable OMN was presented. The PA utilizes a 15 W GaN HEMT and operates at 0.685 and 1.84 GHz. The high frequency range was enabled by varactors with high breakdown voltage and high tuning range. It presents a drain efficiency of ∼61% at 6 dB OPBO for both bands, and presents a maximum output of ∼42 dBm for both bands. The design employs a comprehensive optimization of OMN parameters for optimum efficiency for both bands.

In [Paper A], the theoretical class-J DLM capabilities from [63] were extended to a wide range of frequencies. It turns out that a purely reactive load modulation provides high drain efficiency for a large dynamic range of powers for a reconfigurable frequency range of 36%. The reactive load modulation allows a simple realization of the tunable OMN with a single varactor control. A PA prototype based on a 15 W GaN HEMT and varactors with high breakdown voltage and high tuning range was fabricated. The PA presents a drain efficiency of 43–54% from 1.80–2.25 GHz at 6 dB OPBO, and presents a maximum delivered power of ∼41 dBm. The theory behind this design is explained in more detail in the next section.

3.3 Frequency Reconfigurable Class-J DLM

[Paper A] utilizes the same analysis of the DLM capabilities of the ideal class-J operation as [63], and expands the analysis to cover a large range of frequencies. In this section, the theoretical background is first presented, and then a PA prototype realization is analyzed and discussed.

3.3.1 Theoretical Background

The Class-J mode of operation is biased in the same way as class-B, but utilizes the transistor's parasitic output capacitance to present complex impedances to the current source. A schematic of a class-J circuit is presented in Figure 3.2. The transistor model includes a shunt capacitor C_{tot}, which represents the effective capacitance at the transistor output. The output of the transistor is

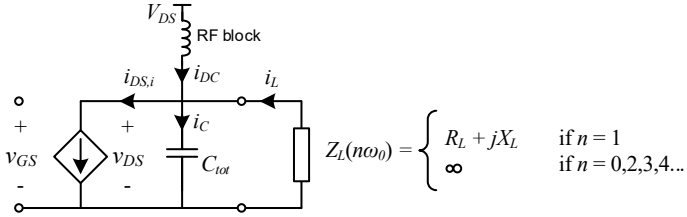


Figure 3.2: Schematic of class-J operation.

terminated with the complex impedance $Z_L = R_L + jX_L$ at the fundamental frequency, and with open circuit for all other frequencies.

The intrinsic current flowing through the current source $i_{DS,i}$ is given by (2.20). The current i_{DC} only contains a DC-component and is given by (2.19). The current flowing through the load only contains a fundamental frequency component, and can therefore be calculated from the fundamental intrinsic current:

$$I_{l,\omega_0} = I_{ds,i,\omega_0} \frac{Z_{L,i}}{Z_L}, \tag{3.1}$$

where $Z_{L,i}$ is the fundamental intrinsic load presented to the current source, i.e.

$$Z_{L,i} = \frac{Z_L}{jX_{C_{tot}} Z_L + 1}, \tag{3.2}$$

where $X_{C_{tot}} = \omega_0 C_{tot}$. The current through the capacitor C_{tot} is given by

$$i_C = i_{DC} - i_{DS,i} + i_L. \tag{3.3}$$

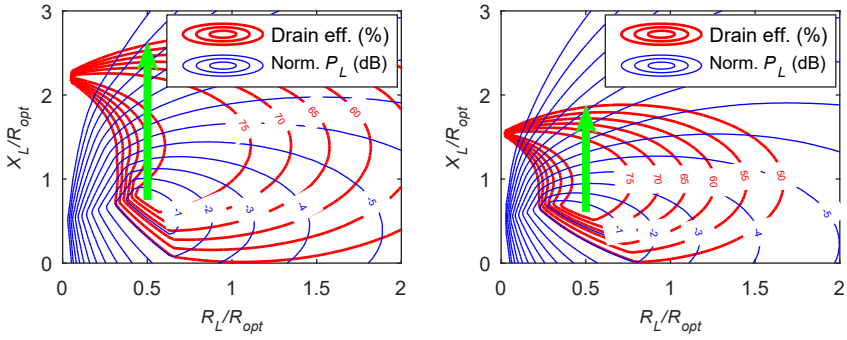
The time-domain drain-source voltage can be calculated by

$$v_{DS}(\phi) = \frac{1}{X_{C_{tot}}} \int_0^{\phi} i_C \mathrm{d}\phi + V_{OFF} =$$

$$\begin{cases} \frac{1}{X_{C_{tot}}} (\beta I_{MAX} \left[\frac{\phi}{\pi} + \cos\phi - 1\right] + \\ \qquad |I_{l,\omega_0}| \left[\cos\angle I_{l,\omega_0} - \cos\left(\phi + \angle I_{l,\omega_0}\right)\right]) + V_{OFF} & \text{if } 0 \le \phi \le \pi \\ \frac{1}{X_{C_{tot}}} (\beta I_{MAX} \left[\frac{\phi}{\pi} - 2\right] + \\ \qquad |I_{l,\omega_0}| \left[\cos\angle I_{l,\omega_0} - \cos\left(\phi + \angle I_{l,\omega_0}\right)\right]) + V_{OFF} & \text{if } \pi < \phi < 2\pi \end{cases} \tag{3.4}$$

where $\phi = \omega_0 t$, and V_{OFF} is a DC-offset selected such that the correct DC voltage is obtained, i.e. V_{DS}. With the waveforms expressed, the class-J mode can now be characterized in terms of R_s, X_s, $X_{C_{tot}}$ and β.

The class-J mode will operate for infinitely many combinations of R_L, X_L, $X_{C_{tot}}$ as long as $v_{DS}(\phi) \ge 0$. In order to grasp this, it is useful to sweep these parameters. Therefore, R_s, X_s, $X_{C_{tot}}$ and β are swept, and all solutions with $v_{DS}(\phi) \ge 0$ are saved. Since drain efficiency is the most important attribute, only the β:s that yield the highest possible drain efficiency for given R_L, X_L and $X_{C_{tot}}$, are saved. The results are presented in figures below. To generalize, R_L, X_L and $X_{C_{tot}}$ are normalized with the optimum class-B load resistance,



(a) $1/(X_{C_{tot}}/R_{opt}) = 0.45$ **(b)** $1/(X_{C_{tot}}/R_{opt}) = 0.65$

Figure 3.3: Drain efficiency and delivered power versus the resistive and reactive parts of the load termination, for two different $1/(X_{C_{tot}}/R_{opt})$. The green arrow shows a possible purely reactive load modulation.

R_{opt}, see (2.8), and the delivered power is normalized with the maximum possible class-B delivered power.

In Figure 3.3, drain efficiency and delivered power are presented as contours versus the resistive and reactive parts of the load termination, for two different $1/(X_{C_{tot}}/R_{opt})$. It can be seen that a large number of load termination impedances yield a drain efficiency over 75%. It can also be seen that if the reactive part of the load is modulated, while the resistive part is kept fixed at the normalized value of 0.5, high drain efficiency is maintained over a large range of delivered powers. The ratio $1/(X_{C_{tot}}/R_{opt})$ is proportional to frequency, which means that it is possible to have a purely reactive load modulation across a large bandwidth.

The bandwidth capabilities are demonstrated in more detail in Figure 3.4. In this figure, drain efficiency and delivered power are presented as contours versus the reactive part of the load termination and $1/(X_{C_{tot}}/R_{opt})$, which is proportional to frequency, for a fixed $R_L/R_{opt} = 0.5$. It can be seen that a purely reactive load modulation enables high drain efficiency for a large span of frequencies and for a large range of powers. Cross sections of different values of $1/(X_{C_{tot}}/R_{opt})$ are presented in Figure 3.5. It is possible to uphold a drain efficiency higher than 70% over 7.7 dB OPBO dynamic range for $0.45 \leq 1/(X_{C_{tot}}/R_{opt}) \leq 0.65$. This span corresponds to a fractional bandwidth of 36%. If the dynamic range is relaxed to 6 dB OPBO, it is possible to uphold a drain efficiency higher than 70% over an octave of bandwidth. A consequence of load modulation is non-linear gain response. The non-linear gain for low powers can however be avoided by only modulating X_L at high powers. That way, the gain response is flat up until the load modulation. The gain drop at high powers very much resembles the gain response of a load modulated class-B PA, where the gain is proportional to the resistive load termination. In Figure 3.6, the corresponding load lines and waveforms at the current source, for $1/(X_{C_{tot}}/R_{opt}) = 0.55$ and $R_L/R_{opt} = 0.5$, and for different normalized delivered powers, are presented.

One way of achieving the purely reactive load modulation is with a series varactor and series inductor, see Figure 3.7. In this configuration, the total

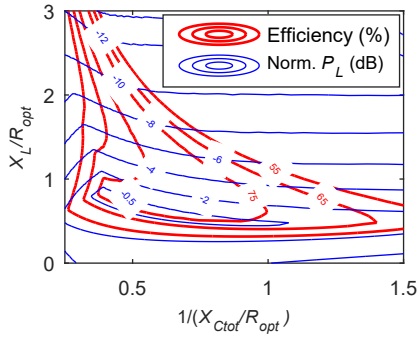


Figure 3.4: Drain efficiency and delivered power versus the reactive part of the load termination and $1/(X_{C_{tot}}/R_{opt})$ (proportional to frequency), for a fixed $R_L/R_{opt} = 0.5$.

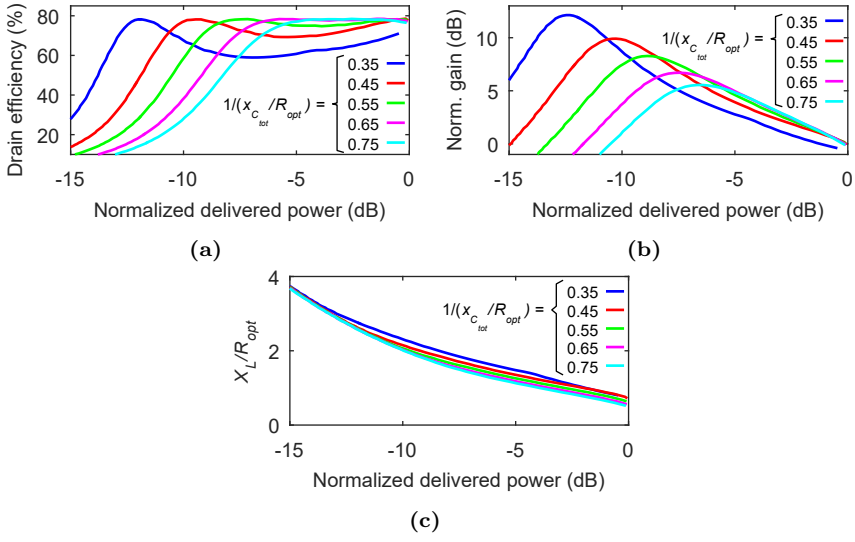


Figure 3.5: Cross sections for different $1/(X_{C_{tot}}/R_{opt})$, for a fixed $R_L/R_{opt} = 0.5$.

reactance is given by

$$X_L = \omega L_s - \frac{1}{\omega C_s}. \tag{3.5}$$

For example, if the inductor presents $\omega L_s/R_{opt} = 4$ (at $1/(X_{C_{tot}}/R_{opt}) = 0.65$), the capacitive tuning of the varactor must be between 1 and 1.5 for $1/(X_{C_{tot}}/R_{opt}) = 0.65$, and between 2.4 and 5.1 for $1/(X_{C_{tot}}/R_{opt}) = 0.45$, where the two cases have been normalized with the same capacitance. Thus, the total capacitive tuning range of the varactor, in this example, must be between 1 and 5.1. Higher frequency range requires higher tuning range. The tuning range can be reduced by increasing the inductance, but at the cost of requiring very fine tuning at the higher frequencies, and at the cost of increasing the RF voltage swing over the varactor, which lowers the effective tuning range. This limits the possible frequency range in reality for this topology. It can also be mentioned that it is possible to achieve a purely reactive load modulation by a shunt varactor and an impedance transformer [63], although in that

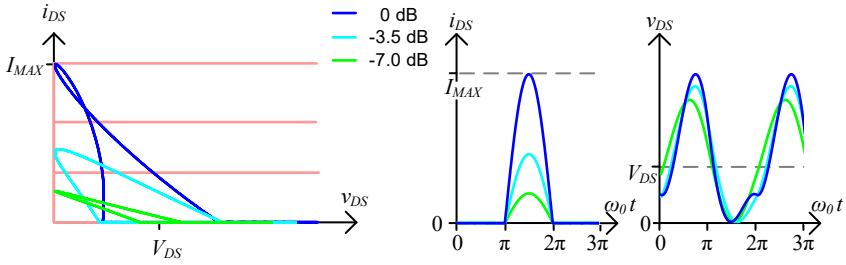


Figure 3.6: Load lines and waveforms for a purely reactive load modulated class-J PA with $1/(X_{C_{tot}}/R_{opt}) = 0.55$ and $R_L/R_{opt} = 0.5$, for different normalized delivered powers.

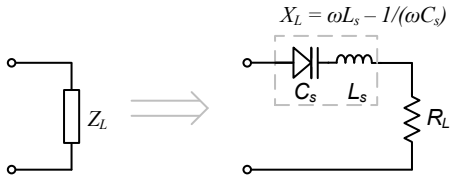


Figure 3.7: A a series varactor and series inductor configuration for achieving a purely reactive load modulation.

configuration, the impedance transformer will limit the bandwidth. In either configuration, limited possibilities to present open circuit to higher harmonics across the band for all powers will cause a deviation from the class-J operation, which may make reactive load modulation less optimal.

3.3.2 Circuit Prototype

The wideband capabilities of the series varactor terminated class-J DLM PA were demonstrated by a prototype in [Paper A]. The prototype PA employs a 15 W GaN HEMT CGH60015D from Cree. The PA targets a center frequency of 2.14 GHz.

A first step of evaluating the new wideband possibilities is to perform simulations with the transistor model where the input and output networks consist of ideal passives and ideal capacitive tuning. In these simulations, the transistor is stabilized, perfect open harmonic terminations are presented to the output of the transistor, input matching is presented by ideal passives, and the load is purely reactively modulated and has a constant resistive value. The simulations present a drain efficiency >60% over 6 dB OPBO dynamic range over almost an octave of bandwidth centered around 2.14 GHz. However, it is important to mention that in these simulations, the ideal capacitive tuning range for an octave of bandwidth is not realistic for practical implementation. Nevertheless, it is still interesting to evaluate the purely reactive load modulation on real transistors. In addition, due to the gain dropping off at frequencies far away from the center, the PAE is >60% over 6 dB OPBO dynamic range only from 1.8 GHz to 2.3 GHz. The results from these simulations will be presented together with measurements in figures later in this section. From the theory, the ideal reactive modulation (X_L/R_{opt}) is 0.72–1.80 for 1.8 GHz and 0.56–1.60 for 2.5 GHz. From the simulations, it turns

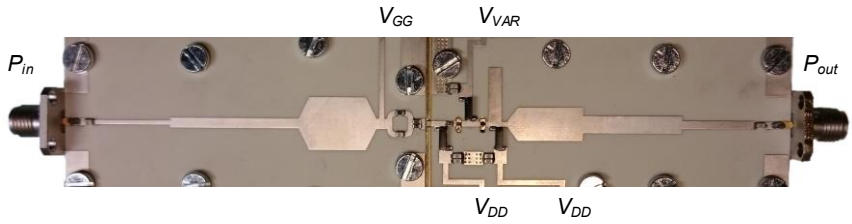


Figure 3.8: Photograph of the core area of the fabricated varactor-based DLM PA. The transistor is soldered to a ridge in the middle.

out that the optimum reactive load modulation for this transistor is 0.58–1.45 for 1.8 GHz and 0.47–1.18 for 2.5 GHz. These modulation regions vary a bit depending on how much the transistor is compressed. Overall, a purely reactive load modulation is very beneficial for high drain efficiency operation across a large bandwidth for this transistor. Tuning the reactive load from 1.8 to 2.5 GHz should be feasible in practical implementations.

A photograph of the core area of the fabricated varactor-based DLM PA prototype is shown in Figure 3.8. A photo of the whole circuit and the corresponding schematic can be found in [Paper A]. The design follows the series inductor series varactor topology from Figure 3.7. SiC varactors [69] were used in an anti-series configuration to reach the wanted capacitive range. A shunt stub had to be added in order to center the second harmonics around open circuit across the frequency band.

The drain efficiency versus frequency at maximum delivered power and at 6 dB OPBO is presented in Figure 3.9(a). The maximum delivered power versus frequency is presented in Figure 3.9(b). The three cases in the figures are:

- Simulations with the real transistor model where the input and output networks consist of ideal passives and ideal capacitive tuning (sim. 1). The capacitive tuning range in these simulations is practically unrealistic.
- Cut-ready simulations using the transistor model from the vendor, an in-house varactor model, passives modelled by Modelithics, and EM simulations using Keysight Momentum (sim. 2).
- Measurements of the fabricated PA prototype (meas.)

For all cases, the varactor voltage has been optimized for maximum efficiency versus delivered power. The drain efficiency drops somewhat when realistic, lossy input/output networks are used instead of ideal ones. The bandwidth of the cut-ready simulations is also lower compared to when ideal input/output networks are used. This is due to limited tuning range and non-perfect modulation across the band. The PA prototype presents a similar trend as the cut-ready simulations, but with slightly lower values. The measurements are performed up to 2.25 GHz due to severe gain reduction beyond this frequency.

For the three cases, drain efficiency, gain and varactor voltage versus delivered power for 1.8, 2.0 and 2.2 GHz are presented in Figure 3.10. All three cases present similar trends. However, the gain drops off at higher frequencies for the cut-ready simulations and the measurements. The gain drop of the cut-ready simulations may be attributed to a slightly different operation than

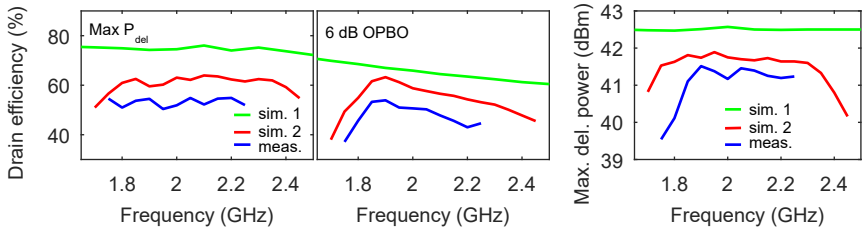


Figure 3.9: (a) Drain efficiency versus frequency at maximum delivered power and at 6 dB OPBO. (b) Maximum delivered power versus frequency. *Sim.* 1 denotes simulations with a real transistor model and ideal input/output networks, *sim.* 2 denotes cut-ready simulations, and *meas.* denotes measurements of the fabricated prototype.

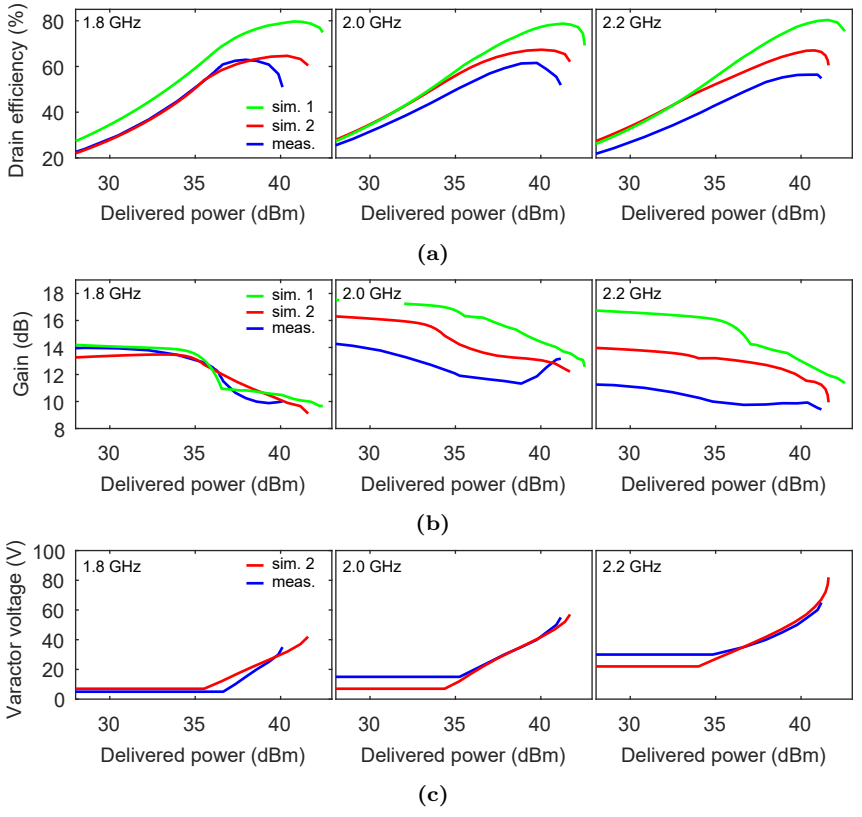
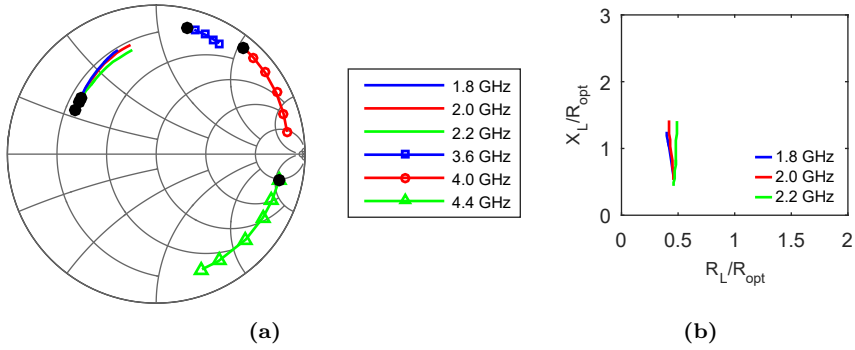


Figure 3.10: (a) Drain efficiency, (b) gain, and (c) varactor voltage versus delivered power for 1.8, 2.0 and 2.2 GHz. *Sim.* 1 denotes simulations with a real transistor model and ideal input/output networks, *sim.* 2 denotes cut-ready simulations, and *meas.* denotes measurements of the fabricated prototype.

the ideal case. The gain drop of the measurements may be attributed to an inaccurate transistor model.

The fundamental and second harmonic load modulations at the reference plane (see Figure 3.2) for cut-ready simulations are presented in Figure 3.11. It can be seen that the fundamental load modulation is almost purely reactive,



(a) **(b)**

Figure 3.11: (a) Fundamental and second harmonic load modulation for cut-ready simulations, represented by reflection coefficients in a Smith chart normalized with 50 Ω. The maximum power levels are marked with a solid black circle. (b) Fundamental load modulation for cut-ready simulations in Cartesian coordinates normalized with $Ropt = 27\ \Omega$.

which is what is sought after. The second harmonic load modulation is, unfortunately, a bit spread out.

Linearized measurements are presented for a 3.84 MHz W-CDMA signal with 6.7 dB PAPR across 1.8–2.2 GHz in [Paper A]. A similar measurement setup as in [70] was used. The PA presents an average PAE higher than 39% across the band with an adjacent channel power ratio (ACPR) lower than 45 dBc after DPD linearization.

The performance of the cut-ready simulations is degraded somewhat due to lower tuning capabilities of the real varactors and the non-perfect reactive tuning. The non-perfect open circuit of the second harmonics causes a deviation from the class-J operation, which may make reactive load modulation less optimal. The performance degradation of the fabricated PA may be attributed to an inaccurate transistor model. Nevertheless, the fabricated PA presents good energy efficiency performance from 1.8-2.2 GHz.

3.4 Discussion

While [65–68] all present impressive performance figures, none of them describes the mechanics behind the operation. [Paper A] has established a profound theory of the mechanics behind class-J DLM across a large bandwidth that does not compromise other PA properties, such as delivered power. [Paper A] has demonstrated that the optimal load trajectories of the ideal class-J operation map well to a real GaN transistor for a large range of frequencies. Although the PA prototype presents good results in terms of efficiency, delivered power and frequency range, there is much room for improvements in the implementation. For example: higher model accuracy could move measurements closer to simulations; other topologies for the OMN could be investigated for effective tuning range; improved varactor technology would improve tuning range.

Chapter 4

Generalized Doherty Power Amplifiers

Since the Doherty PA was first introduced in 1936 [47], the architecture has been extensively studied [71–73]. While many efforts have been put into generalizing the operation for extended efficiency enhancement [48, 49, 74–79] or extended bandwidth [53–55, 80–88], fewer studies have been made on analyzing the fundamental way the main and auxiliary transistors interact with each other. It turns out that such analysis can lead to record efficiency performance [89, 90], or improved efficiency-linearity trade-off [Paper B].

This chapter first reviews the conventional Doherty PA operation. Then the operation is generalized to arbitrary current profiles while maintaining the efficiency performance. After that, the operation is generalized for improved linearity. While [Paper B] focuses on the practical implementation of the generalized theory, this chapter focuses on the underlying theory. Moreover, deriving equations are included for the sake of completeness.

4.1 The Conventional Doherty PA

The Doherty PA operates according to a simple concept: an auxiliary transistor (also called peaking) injects a current into the output of a main transistor (also called carrier) to modulate the load of the main transistor, to maintain high drain efficiency for a large range of output powers. It is presumed that the auxiliary transistor is off up until the input voltage drive level β_{bo}, where it starts to conduct and therefore starts modulate the load of the main transistor. This leads to an efficiency peak at both maximum power and at an OPBO level, which is referred to as γ, for the whole PA circuit. W. H. Doherty derived the circuit topology and design parameters for $\gamma = 6$ dB [47]. Raab expanded the theory by analytically showing that γ can be arbitrary if a certain relationship between the main and auxiliary transistor currents is met [48]; Iwamoto et al. later demonstrated this concept with a prototype [49]. A conventional Doherty PA has a given output combiner network, consisting of a quarter-wave transformer and a resistive load termination, and a given input phase delay of 90 degrees, see Figure 4.1. The characteristic impedance of the quarter-

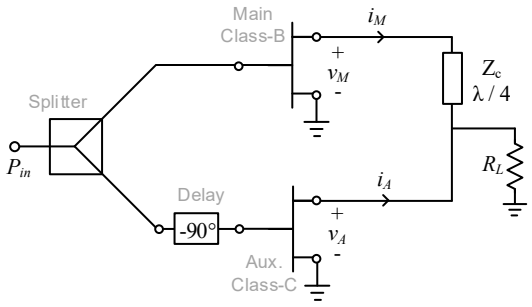


Figure 4.1: The conventional Doherty PA architecture.

wave transformer and the resistance of the load termination are functions of transistor parameters and γ. Although the conventional Doherty PA topology consists of an input power splitter between the main and auxiliary transistor, the Doherty PA operation can also be achieved with individually controlled dual inputs [91, 92]. In the conventional Doherty PA, the main transistor is operated in class-B, and the auxiliary transistor is operated in class-C in order to turn on at the intended drive level β_{bo}. In Figure 4.1, currents going into the output combining network are denoted i_M, i_A and contain the fundamental components I_m, I_a, and the DC components I_M, I_A. The voltages are denoted equivalently.

The Doherty PA operation can be described as: certain current profiles for the main and the auxiliary transistors are selected, then the output combiner network is solved for a maximum efficiency performance - which is equivalent to solve for maximum voltage swing. The current profiles of the conventional Doherty PA are given by

$$\left|I_a\big|_{\beta=1}\right| = \left(\frac{1}{\beta_{bo}} - 1\right)\left|I_m\big|_{\beta=1}\right|, \tag{4.1}$$

$$\left|I_a\big|_{\beta=\beta_{bo}}\right| = 0, \tag{4.2}$$

$$\underline{/I_a/I_m} = -90^\circ, \tag{4.3}$$

where R_{opt} is the optimum class-B load resistance. The solution to the conventional quarter-wave output combiner is

$$Z_c = R_{opt}, \tag{4.4}$$

$$R_L = \beta_{bo} R_{opt}. \tag{4.5}$$

The fundamental powers delivered to the load are related by

$$P_L\big|_{\beta=1} = \gamma P_L\big|_{\beta=\beta_{bo}}, \tag{4.6}$$

which can be expanded to

$$P_m\big|_{\beta=1} + P_a\big|_{\beta=1} = \gamma P_m\big|_{\beta=\beta_{bo}}, \tag{4.7}$$

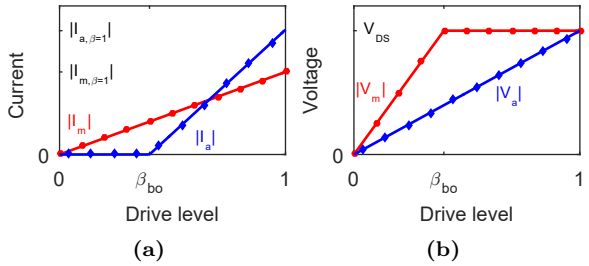


Figure 4.2: (a) Current and (b) voltage profiles of the conventional Doherty PA.

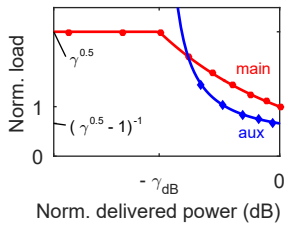


Figure 4.3: The main and auxiliary transistor load modulation versus normalized delivered power of the Doherty PA, for the conventional Doherty PA. The load is normalized with the optimum class-B load.

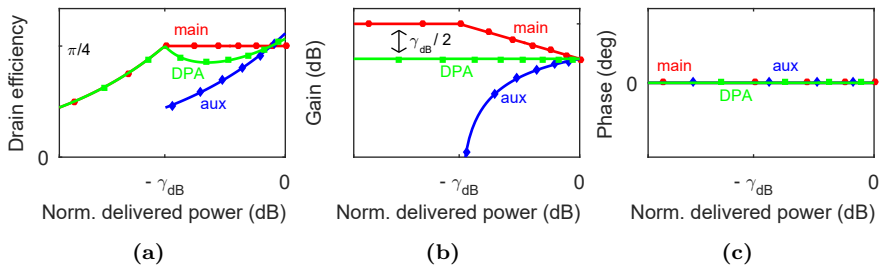


Figure 4.4: (a) Drain efficiency, (b) gain, and (c) phase of the main transistor, the auxiliary transistor, and the Doherty PA, versus normalized delivered power of the Doherty PA.

where P_m and P_a are fundamental powers at the output of the main and auxiliary transistors. β_{bo} is related to γ according to

$$\gamma = \frac{1}{\beta_{bo}^2}. \tag{4.8}$$

The behavior and performance of the conventional Doherty PA is presented in Figures 4.2–4.4. For the main transistor, the class-B DC and fundamental currents are calculated from (2.19),(2.20). The class-C currents of the auxiliary transistor are also calculated from (2.19),(2.20), but are approximated to piece-wise linear according to

$$I_{A,lin} = \begin{cases} 0, & \beta_{bo} > \beta \\ I_A\big|_{\beta=1} \frac{\beta-\beta_{bo}}{1-\beta_{bo}}, & \beta_{bo} \leq \beta \end{cases}, \tag{4.9}$$

$$|I_{a,lin}| = \begin{cases} 0, & \beta_{bo} > \beta \\ \left|I_a\right|_{\beta=1}\left| \frac{\beta-\beta_{bo}}{1-\beta_{bo}}, & \beta_{bo} \leq \beta \end{cases}. \tag{4.10}$$

This piece-wise approximation will be used for class-C throughout this chapter. The approximation simplifies the visualization of the ideal Doherty PA operation and does not affect any conclusions. The real ideal class-C current results in smoother behavior in the transition from the power region where the auxiliary transistor is off, i.e. the *low power region*, to the power region where the auxiliary transistor is on, i.e. the *high power region*, which is irrelevant when studying the ideal Doherty PA.

The current and voltage profiles are presented in Figure 4.2. Note the flat voltage of the main transistor in the high power region. The load modulation of the main and auxiliary transistors are presented versus normalized delivered power of the whole Doherty PA in Figure 4.3. The load is normalized with the optimum class-B load. Note that the load presented to the auxiliary transistor goes to infinity when the β goes to β_{bo}. In Figure 4.4, drain efficiency, gain and phase are plotted for the main transistor, the auxiliary transistor, and the Doherty PA, versus normalized delivered power of the Doherty PA. The main transistor presents maximum class-B drain efficiency in the high power region, but the drain efficiency of the Doherty PA is degraded somewhat for intermediate power levels in the high power region due to the auxiliary transistor. The main and auxiliary transistors both present non-linear gain responses, but when combined into the Doherty PA, the PA presents linear gain. The ideal Doherty PA also presents a completely linear phase response.

4.2 The Generalized Doherty PA

Some advances in the generalization of the Doherty PA have been presented in recent years. In order to solve practical limitations in the realization of the output network for a N-way Doherty PA, the Doherty PA theory was expanded by treating the output network as a *black-box* combiner in [93]. The network parameters of this combiner network and the device periphery ratio are solved for maximum efficiency at maximum power and at back-off for any predetermined γ. In [93], the input phase delay θ is fixed to $\pm 90°$ when the circuit parameters are derived. In [89,90], on the other hand, Özen *et al.* showed that the input phase delay can adopt other values. The input phase delay θ and the output combiner parameters are solved for any predetermined γ for two fully utilized symmetrical transistors, i.e. for a device periphery ratio of one. For two fully utilized symmetrical transistors and when $\gamma > 6$ dB for a class-B–class-B Doherty PA, or $\gamma > 4.8$ dB for a class-B–class-C Doherty PA, the main and auxiliary transistor current relationship will deviate from the conventional Doherty PA current relationship. Due to the freedom of θ, it was shown that the presented solution still provides maximum efficiency at maximum power and at the predetermined back-off level γ, at the cost of some non-linearity. It was further shown that by using the proposed combiner synthesis approach, impedance matching networks and offset lines [94], which are required in practice for parasitic compensation and impedance transformation, can be integrated into the same network. However, some of the Doherty PA circuit design parameters in [89, 90] are solved analytically and some are found numerically.

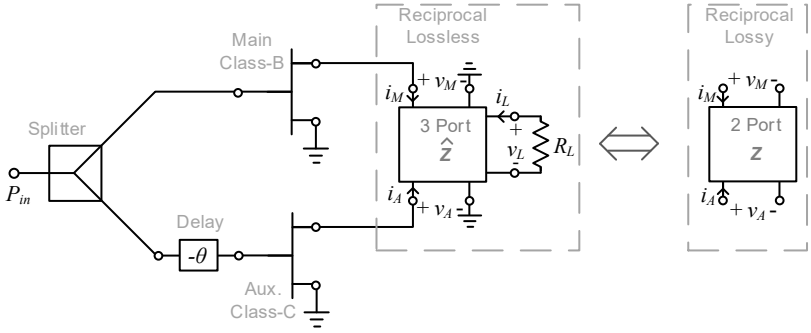


Figure 4.5: The generalized Doherty PA architecture.

In [95], the parameters for a black-box three-port output combiner were solved for an arbitrary power ratio between the outputs of the two transistors. However, the consequences of non-conventional current profiles resulting from the arbitrary power ratio, nor the limitation of the range of power ratios were studied.

In this section, the Doherty PA operation is generalized beyond the symmetrical limitation [d]. Just like [89, 90], the generalized Doherty PA operation is derived in terms of two-port network parameters. In contrast to the three-port derivation in [95], the two-port derivation is significantly more simple. Furthermore, the full consequences of non-conventional currents are studied and all parameters in the generalization are derived analytically. In the next section, it will be shown how these findings can be used for improving the linearity of the Doherty PA.

4.2.1 Derivation of a Generalized Operation

It is possible to generalize the Doherty PA operation by making the main and auxiliary transistor current relationship independent of β_{bo}. The conventional quarter-wave output combiner only enables optimum efficiency if (4.1) is fulfilled. Therefore, the output combiner is instead an arbitrary reciprocal and lossless three-port network with the load terminated at the third port. It turns out that this three-port network can be represented by an equivalent lossy and reciprocal two-port network, i.e. the resistive load termination has been absorbed into the combiner [90]. This two-port representation simplifies the analysis of the generalized Doherty PA significantly. The phase difference of the main and auxiliary transistor currents is generalized to θ. The generalization of the Doherty PA architecture is presented in Figure 4.5.

The current profiles of the generalized Doherty PA are given by

$$\left|I_a\big|_{\beta=1}\right| = r_c \left|I_m\big|_{\beta=1}\right|, \tag{4.11}$$

$$\left|I_a\big|_{\beta=\beta_{bo}}\right| = 0, \tag{4.12}$$

$$\angle I_a/I_m = -\theta. \tag{4.13}$$

Here, r_c is a current ratio parameter independent of β_{bo} (or γ). It is useful to compare how the generalized current ratio compare to the conventional current ratio. Therefore, a normalized current ratio is introduced as

$$\hat{r}_c = \frac{r_c}{\frac{1}{\beta_{bo}} - 1}. \tag{4.14}$$

Thus, if $\hat{r}_c = 1$, a conventional ratio is obtained, and if $\hat{r}_c \neq 1$, the conventional current ratio is scaled.

The two-port output combiner parameters are solved for maximum voltage swing at $\beta = 1$ and $\beta = \beta_{bo}$. This can be expressed as

$$Z_{11} + Z_{12}\frac{I_a\big|_{\beta=1}}{I_m\big|_{\beta=1}} = \frac{V_m\big|_{\beta=1}}{I_m\big|_{\beta=1}}, \tag{4.15}$$

$$Z_{22} + Z_{12}\frac{I_m\big|_{\beta=1}}{I_a\big|_{\beta=1}} = \frac{V_a\big|_{\beta=1}}{I_a\big|_{\beta=1}}, \tag{4.16}$$

$$Z_{11} + Z_{12}\frac{I_a\big|_{\beta=\beta_{bo}}}{I_m\big|_{\beta=\beta_{bo}}} = \frac{V_m\big|_{\beta=\beta_{bo}}}{I_m\big|_{\beta=\beta_{bo}}}, \tag{4.17}$$

$$Z_{22} + Z_{12}\frac{I_m\big|_{\beta=\beta_{bo}}}{I_a\big|_{\beta=\beta_{bo}}} = \frac{V_a\big|_{\beta=\beta_{bo}}}{I_a\big|_{\beta=\beta_{bo}}}, \tag{4.18}$$

where

$$\left|V_m\big|_{\beta=1}\right| = \left|V_a\big|_{\beta=1}\right| = \left|V_m\big|_{\beta=\beta_{bo}}\right| = V_{DS}. \tag{4.19}$$

Since $V_{DS}/|I_m\big|_{\beta=1}| = R_{opt}$ and $\left|I_a\big|_{\beta=\beta_{bo}}\right| = 0$, the solution becomes

$$Z_{11} = \frac{R_{opt}}{\beta_{bo}}, \tag{4.20}$$

$$Z_{12} = Z_{21} = -\frac{R_{opt}e^{j\theta}}{\hat{r}_c}, \tag{4.21}$$

$$Z_{22} = \frac{R_{opt}\beta_{bo}(\hat{r}_c + e^{j2\theta})}{\hat{r}_c^2(1-\beta_{bo})}. \tag{4.22}$$

The relation between β_{bo} and γ is found by the Doherty PA power relation (4.7) and is given by:

$$\gamma = \frac{\beta_{bo}(1-\hat{r}_c) + \hat{r}_c}{\beta_{bo}^2}. \tag{4.23}$$

The condition that the lossy and reciprocal two-port network must be equivalent to a lossless and reciprocal three-port network with the third port terminated with a load, leads to the following restriction [90]

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\}. \tag{4.24}$$

From this restriction, the phase offset θ has four solutions according to

$$\theta = \begin{cases} \pm\theta_x \\ \pm(\pi - \theta_x) \end{cases}, \tag{4.25}$$

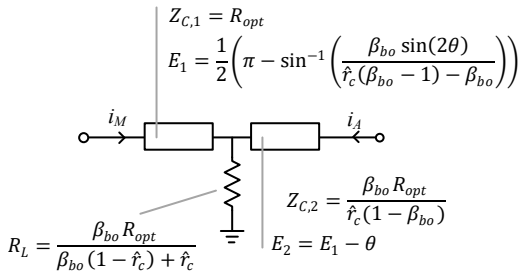


Figure 4.6: One combiner solution to the generalized Doherty PA architecture when $\theta = +\theta_x$.

where

$$\theta_x = \tan^{-1}\left(\sqrt{\frac{\beta_{bo}+\hat{r}_c}{1-\hat{r}_c}}\right). \tag{4.26}$$

It can be seen that $\hat{r}_c \leq 1$ for physical solutions. A lower limit of $\hat{r}_c$ will be set by the condition that the drain voltage must always be larger than zero, which yields

$$\frac{2}{\gamma+1} \leq \hat{r}_c \leq 1. \tag{4.27}$$

There are many ways of realizing the output combiner of the generalized Doherty PA. One explicit example for $\theta = +\theta_x$ is presented in Figure 4.6. For more general approaches, see [90, 95].

4.2.2 Generalized Phase Response

The voltage across the load termination at the third port in Figure 4.5 can be expressed in terms of the two-port network parameters [Paper B]:

$$V_l = \pm j\sqrt{R_L \Re\{Z_{11}\}}I_m \pm j\sqrt{R_L \Re\{Z_{22}\}}I_a. \tag{4.28}$$

The four solutions arise from the four possible choices of θ, see (4.25). From this, the phase response of the generalized Doherty PA can be calculated. For a conventional Doherty PA, i.e. $\hat{r}_c = 1$, the two-port parameter Z_{22} is zero, which simplifies the expression significantly. The phase of the conventional Doherty PA is only a function of the phase of the main transistor current. Since Z_{22} becomes non-zero when the current ratio is scaled, the phase response becomes a function of complex currents and combiner parameters. It is interesting to compare the phase at the maximum power level and the backed-off power level. Therefore, the following ratio is interesting

$$\frac{V_l\big|_{\beta=1}}{V_l\big|_{\beta=\beta_{bo}}} = \frac{\left|I_m\big|_{\beta=1}\right| e^{j\angle I_m|_{\beta=1}}}{\left|I_m\big|_{\beta=\beta_{bo}}\right| e^{j\angle I_m|_{\beta=\beta_{bo}}}} \frac{\pm j\sqrt{\Re\{Z_{11}\}} \pm j\sqrt{\Re\{Z_{22}\}}r_c e^{-j\theta}}{\pm j\sqrt{\Re\{Z_{11}\}}}. \tag{4.29}$$

From this ratio, it can be seen that the Doherty PA phase difference between maximum power and the backed-off power level is dependent on the inherent phase response of the main transistor, but not on the one of the auxiliary

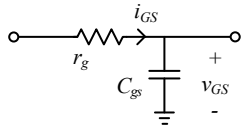


Figure 4.7: A model of the input of a transistor.

transistor. It is however important to mention that this equation does not describe the phase response in between these power levels.

4.2.3 Generalized Gain Response

Scaling the main and auxiliary current ratio from conventional values will cause the gain to compress from drive levels between $\beta = \beta_{bo}$ to $\beta = 1$. The gain compression between these two points can be expressed as

$$G_{comp} = \frac{G\big|_{\beta=1}}{G\big|_{\beta=\beta_{bo}}} = \hat{r}_c(1-\beta_{bo}) + \beta_{bo}. \tag{4.30}$$

Note that this equation is equal to one when $\hat{r}_c = 1$, which means that the gain will be linear. When $\hat{r}_c$ decreases, the gain compression will increase.

In order to study the absolute gain of the generalized Doherty PA, the inputs of the transistors need a more realistic model. One such model is shown in Fig. 4.7. For this model, assuming parasitics scaling linearly with transistor size, a main split ratio can be derived:

$$d_{P,m} = \frac{1}{1 + \frac{S_{aux}}{(1-\beta_{bo})^2}}, \tag{4.31}$$

where the split ratio is defined from

$$P_{in} = P_{in,m} + P_{in,a} = d_{P,m}P_{in} + (1-d_{P,m})P_{in}, \tag{4.32}$$

and S_{aux} is the relative size, i.e. maximum DC current, of the auxiliary transistor compared to the main transistor and can be calculated from

$$S_{aux} = \hat{r}_c \frac{\pi}{2} \frac{(\beta_{bo}-1)^2}{\beta_{bo}\left(\cos^{-1}(\beta_{bo}) - \beta_{bo}\sqrt{1-\beta_{bo}^2}\right)}. \tag{4.33}$$

The Doherty PA small signal gain is maximized by maximizing $d_{P,m}$. For a given β_{bo}, $d_{P,m}$ can be maximized by reducing $\hat{r}_c$.

For comparisons, the generalized Doherty PA gain can be normalized with the gain of single, conventional class-B PA. For the generalized Doherty PA, the gain will always be constant up until β_{bo}, therefore the normalization can be expressed as

$$\frac{G\big|_{\beta=\beta_{bo}}}{G_{class-B}} = \frac{d_{P,m}}{\beta_{bo}}. \tag{4.34}$$

Now, all necessary equations have been derived and the performance of the generalized Doherty PA operation can be studied.

4.2.4 Performance Evaluation

Below follows a comparison between three different solutions to the generalized Doherty PA for $\gamma = 6$ dB. The three cases include the maximum, the minimum, and a value in between of $\hat{r}_c$.

Case I:	$\hat{r}_c = 1$	$S_{aux} = 1.27$
Case II:	$\hat{r}_c = 0.68$	$S_{aux} = 1$
Case III:	$\hat{r}_c = 0.40$	$S_{aux} = 0.71$

Case I is a conventional Doherty PA, i.e. no current scaling. Case II is the same solution as was described in [89, 90], i.e. some current scaling to reach symmetrical transistor sizes. Case III is the solution with maximum current scaling according to (4.27). The main transistors in all cases have the same size, i.e. they have the same maximum DC current.

In Figure 4.8, the magnitudes of the fundamental drain current and drain voltage for both transistors are plotted versus drive level for the three cases defined above. It can be seen that Case I has the well-known conventional Doherty PA current and voltage profiles. Note that the maximum main and auxiliary currents are equal. Case II and III, where current scaling is applied, have non-conventional current and voltage profiles: the maximum auxiliary current is lower than the maximum main current, and the auxiliary drain voltage is non-linear. Also, the auxiliary drain voltage increases at β_{bo} as $\hat{r}_c$ becomes smaller.

The load modulation for the main and auxiliary transistors are plotted in Figure 4.9. The main transistor load modulation is always purely resistive and goes from R_{opt} at maximum power to R_{opt}/β_{bo} at back-off. The auxiliary transistor load modulation is purely resistive for the conventional Doherty PA solution (Case I) but becomes complex for the current scaled solutions. The impedance changes from $V_a\big|_{\beta=1}/I_a\big|_{\beta=1}$ at maximum power to infinity at back-off. The auxiliary transistor load modulation in Figure 4.9 (b) is valid for $\theta = +\theta_x$ and $\theta = -(\pi - \theta_x)$. For $\theta = -\theta_x$ and $\theta = +(\pi - \theta_x)$, the auxiliary transistor load modulation is mirrored in the real axis.

The drain efficiency versus normalized delivered power is plotted in Figure 4.10(a). All cases present very similar efficiencies. The small variations come from different class-C bias and different load modulation of the auxiliary transistor.

In Figure 4.10(b), normalized gain is plotted versus normalized delivered power. The gain has been normalized to the single class-B gain, see (4.34). It can be seen that the gain is significantly higher for the current scaled versions compared to the conventional Doherty PA solution, but at the cost of some non-linearity.

The phase of the load termination voltage is plotted versus normalized delivered power in Figure 4.10(c). It can be seen that conventional Doherty PA has zero phase distortion, but that the current scaled Doherty PAs present phase distortion for ideal transistors. This phase distortion goes in different directions depending on the choice of θ.

So how do all these result translate to Doherty PAs with real transistors? For one thing, the gain of an ideal class-B transistor is proportional to the resistive load termination. Real transistors show a weaker relation, e.g. see

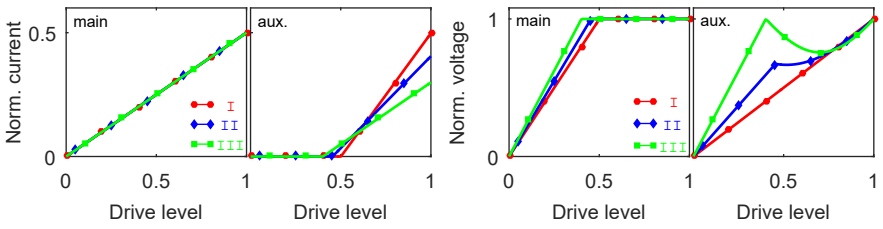


Figure 4.8: (a) Current and (b) voltage profiles of the generalized Doherty PA for Case I, II and III. The current is normalized with I_{MAX}. The voltage is normalized with V_{DS}.

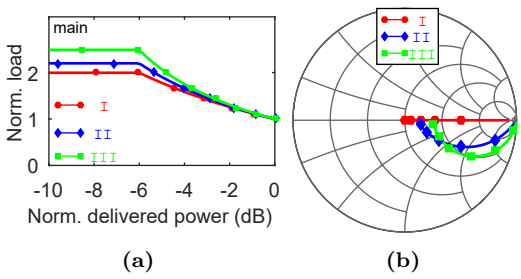


Figure 4.9: (a) Main and (b) auxiliary transistor load modulation versus delivered power for the generalized Doherty PA for Case I, II and III. The load is normalized with the optimum class-B load in both plots. The load modulation of the main transistor is purely resistive and is therefore shown in a Cartesian plot. The load modulation in (b) is valid for $\theta = +\theta_x$ and $\theta = -(\pi - \theta_x)$.

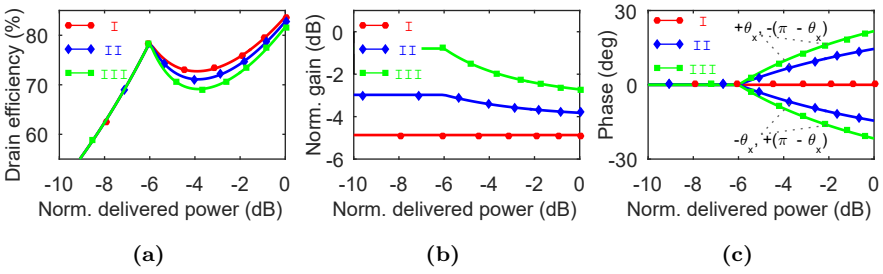


Figure 4.10: (a) Drain efficiency, (b) gain, and (c) phase versus normalized delivered power of the Doherty PA, for the generalized Doherty PA for Case I, II and III. The gain is normalized with the single class-B gain.

the previous chapter. Therefore, the absolute values of the gains presented in this chapter do not translate directly to Doherty PAs with real transistors. However, current scaled Doherty PAs require less power to be split into the auxiliary transistor, which translates well to Doherty PAs with real transistors. Thus, current scaled Doherty PAs with real transistors present higher gain, and therefore potentially higher PAE. However, from (4.7), it can be seen that current scaled Doherty PAs require the backed-off power level of the main transistor to be further away from the maximum power level of the main transistor for a given γ. This results in lower efficiency at back-off for the Doherty PA according to (2.29). If the gain of the transistor is low enough to

limit PAE, the gain increase of the current scaled Doherty PA could result in higher PAE than the conventional Doherty PA. One other method of improving gain is the dual input Doherty PA [91, 92]. That configuration achieves better bandwidth performance and eliminates the gain loss from the analog input power splitter, but at the cost of two complete up-converting stages, significantly increasing the circuit complexity. The non-linearities of the current scaled Doherty PA are often not a limitation since many practical Doherty PAs are very non-linear and rely on DPD.

4.3 Improving Linearity

Even though the ideal Doherty PA presents perfectly linear gain and phase responses, the gain and phase responses for Doherty PAs with real transistors are non-linear. The gain is often compressed to reach higher efficiency levels and the load modulation causes severe phase distortion in the high power region. Due to the Miller effect, the phase response of a transistor becomes dependent on the resistive load termination [96–98]. Therefore, in the high power region, where the load of the main transistor is modulated, the phase response of the main transistor is very non-linear. Which in turn means that the phase response of the Doherty PA is very non-linear, see (4.29).

An approach to improve overall linearity was presented in [94, 99, 100], where the linearity of Doherty PA was improved by optimizing biases for intermodulation (IM) product cancellation at the load. The current profiles of a Doherty PA are, inter alia, a function the bias levels. Therefore, optimizing bias levels for IM cancellation will most likely change the current profiles and degrade drain efficiency. In N-way Doherty PAs, the extra auxiliary transistors provide extra degrees of freedom, making it easier to find both efficiency and linearity optimized solutions [74, 101], but at the cost of complexity.

A method of improving the phase distortion is to introduce a reactive mismatch to the wanted load terminations the Doherty PA is presenting to the transistors [Paper B]. These reactive mismatches introduce phase shifts which can be used to even out the phase differences in the high power region of the Doherty PA. A mismatch will however reduce delivered power and drain efficiency.

In [Paper B] it was showed that the general Doherty PA can be solved for linear gain for all current ratios. Furthermore, it was shown that current scaling can be combined together with reactive mismatch to compensate the inherent non-linear response of the Doherty PA. This combination hardly affects the drain efficiency performance, allowing for highly linear and highly efficient solutions for Doherty PAs with real transistors.

In this section, the mechanics behind the method in [Paper B] is first evaluated on ideal transistors, and then verificative experimental data is shown.

4.3.1 The Ideal Case

For the generalized Doherty PA equations, linear gain can be obtained if the drain efficiency of the main transistor at back-off is relaxed. If (4.7) is solved

together with (4.11) while enforcing (4.8), i.e.

$$\gamma = \frac{1}{\beta_{bo}^2},$$

the drain voltage swing of the main transistor at back-off becomes

$$\left|V_m\big|_{\beta=\beta_{bo}}\right| = V_{DS}\left(\beta_{bo}(1-\hat{r}_c)+\hat{r}_c\right). \tag{4.35}$$

This can also be expressed as

$$R_m\big|_{\beta=\beta_{bo}} = (1+r_c)\, R_m\big|_{\beta=1}. \tag{4.36}$$

Note that the non-normalized r_c is used here. The resistances are calculated from the impedance $Z(\beta) = V(\beta)/I(\beta)$, which in this case are purely resistive. When adding reactive mismatch to these impedances, it is very important to know that (4.24) imposes the following constraint

$$\Re\Big\{Z_m\big|_{\beta=\beta_{bo}}\Big\} \geq (1+r_c)\,\Re\Big\{Z_m\big|_{\beta=1}\Big\}. \tag{4.37}$$

Now, reactive mismatch can safely be added to the impedances. The following impedances are defined

$$Z_m\big|_{\beta=1} = R_m\big|_{\beta=1} \pm jX_m\big|_{\beta=1}, \tag{4.38}$$

$$Z_m\big|_{\beta=\beta_{bo}} = R_m\big|_{\beta=\beta_{bo}} \pm jX_m\big|_{\beta=\beta_{bo}}. \tag{4.39}$$

Adding a reactive component to Z_a only affects the imaginary part of Z_{22}, and does therefore not affect the phase response of the Doherty PA. The resistive and reactive parts of these impedances are defined such that the maximum possible voltage swing is always reached.

$$R_m\big|_{\beta=1} = U_m R_{opt}, \tag{4.40}$$

$$X_m\big|_{\beta=1} = \sqrt{1-U_m^2}\,R_{opt}, \tag{4.41}$$

$$R_m\big|_{\beta=\beta_{bo}} = U_m\,(1+r_c)\,R_{opt}, \tag{4.42}$$

$$X_m\big|_{\beta=\beta_{bo}} = \sqrt{1/\beta_{bo}^2-(1+r_c)^2U_m^2}\,R_{opt}. \tag{4.43}$$

Here U_m can be seen as a utilization parameter that can take any value from 0 to 1. For the conventional Doherty PA, i.e. $\hat{r}_c = 1$, U_m must be smaller than one if reactive mismatch is added. This will clearly lower the drain efficiency. From (4.35), it can be seen that U_m can be equal to 1 when reactive mismatch is added at back-off if $\hat{r}_c < 1$. This means that the efficiency performance of the current scaled Doherty PA does not degrade significantly when reactive mismatch is added. It is also important to mention that the power utilization is proportional to U_m.

Below follows a comparison between three different solutions to the generalized Doherty PA for $\gamma = 6$ dB. The first case is the conventional Doherty PA. The other two cases have been solved for linear gain and for a phase distortion of 30°. The cases are summarized in Table 4.1. The performance is presented

Table 4.1: Comparison of three different $\gamma = 6$ dB Doherty PAs. Case A is the conventional Doherty PA. Case B and C have been solved for linear gain and for a phase distortion of 30°. All impedances are normalized with R_{opt}. In this table, data for negative X_m and $\theta = +\theta_x$ / $\theta = -(\pi - \theta_x)$ is presented. Z_{11} is equal to $Z_m\big|_{\beta=\beta_{bo}}$.

Case	$\hat{r}_c$	U_m	$Z_m\big\|_{\beta=1}$	$Z_m\big\|_{\beta=\beta_{bo}}$	Z_{12}	Z_{22}
A	1	1	1.0+j0	2.0+j0	0–j1.0	0+j0
B	1	0.78	0.78-j0.63	1.55–j1.25	–0.81–j0.59	0.42+j0.94
C	0.85	1	1.0+j0	1.84–j0.76	–1.13-j0.73	0.69+j1.52

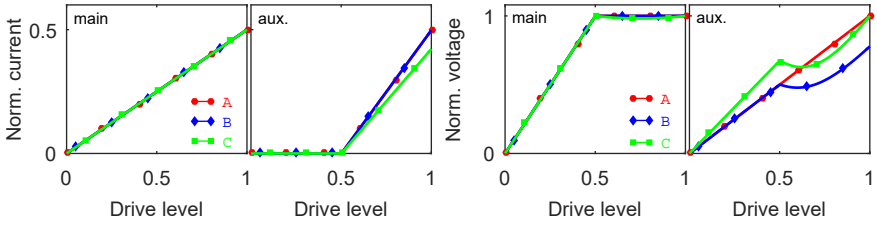


Figure 4.11: (a) Current and (b) voltage profiles of the generalized Doherty PA for Case A, B and C. The current is normalized with I_{MAX}. The voltage is normalized with V_{DS}.

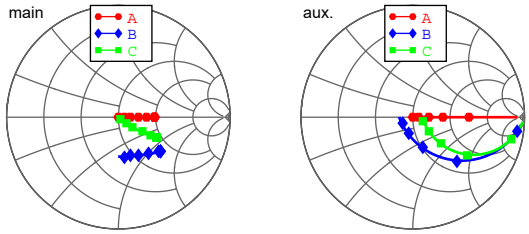


Figure 4.12: (a) Main and (b) auxiliary transistor load modulation versus delivered power for the generalized Doherty PA for Case A, B and C. The load is normalized with the optimum class-B load in both plots. The load modulation in is valid for $\theta = +\theta_x$ and $\theta = -(\pi - \theta_x)$ and negative X_m.

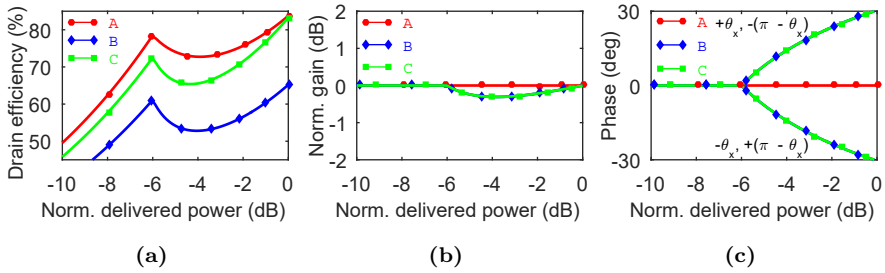


Figure 4.13: (a) Drain efficiency, (b) gain, and (c) phase versus normalized delivered power of the Doherty PA, for the generalized Doherty PA for Case A, B and C. The gain is normalized with itself.

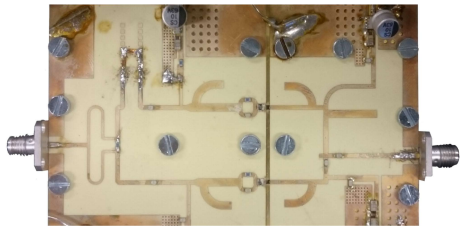


Figure 4.14: Photograph of the core area of the fabricated Doherty PA. The transistors are soldered to a ridge in the middle.

in Figures 4.11–4.13. All cases have the same current and voltage profiles for the main transistor. The auxiliary transistor voltage is increased at back-off, as seen before, when the current ratio is scaled. The auxiliary transistor voltage for Case B is decreased at maximum power due to lacking reactive mismatch of the auxiliary transistor. A reactive mismatch here would increase the voltage to the nominal value, but without affecting the performance in any way. The load modulation follows the expected behavior of current scaling and reactive mismatch. Note the complex load modulation of the auxiliary transistor for Case B. Reactive mismatch introduces an insignificant gain non-linearity. Reactive mismatch significantly degrades efficiency, but when combined with current scaling, the efficiency is hardly affected. Thus, the operation of a Doherty PA with high efficiency and linear gain, with full control of the phase response in the high power region has been derived.

4.3.2 Circuit Prototype

The linearity capabilities of the current scaled Doherty PA were experimentally verified with a prototype PA in [Paper B]. The prototype PA employs the 15 W GaN HEMT CGH60015D from Cree. The PA targets the frequency 2.14 GHz and $\gamma = 8$ dB. A photograph of the core area of the fabricated Doherty PA prototype is shown in Figure 4.14. A photo of the whole circuit and the corresponding schematic can be found in [Paper B].

The design procedure was to first select a $Z_m\big|_{\beta=\beta_{bo}}$ that yields a good trade-off between gain compression and efficiency. Then all possible values of reactive mismatch of $Z_m\big|_{\beta=1}$ for many different current ratios between the main and auxiliary transistors were evaluated, and the best solution was selected.

The phase compensating effect of current scaling and reactive mismatch is demonstrated in Figure 4.15, where the phase is plotted in different planes for cut-ready simulations. The figure presents the phase response of the main transistor current, the auxiliary transistor current, and the voltage across the load. The figure also includes the phase response the circuit would have had if the main and auxiliary transistors had inherently flat phase responses ($\angle$ comb). It can be seen that the main transistor presents severe phase distortion and that it is cancelled by current scaling and reactive mismatch.

Simulated and measured performance is presented in Figure 4.16. The gain offset between simulations and measurements is believed to be a consequence of inaccurate modelling of the transistors, for more details, see [Paper B]. Despite this difference, the prototype PA presents nearly flat gain and phase responses

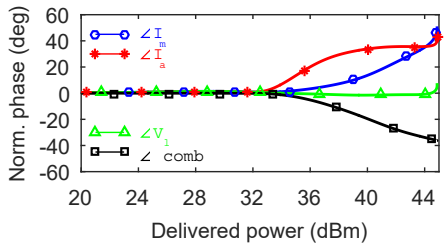


Figure 4.15: The phase response in different planes for cut-ready simulations.

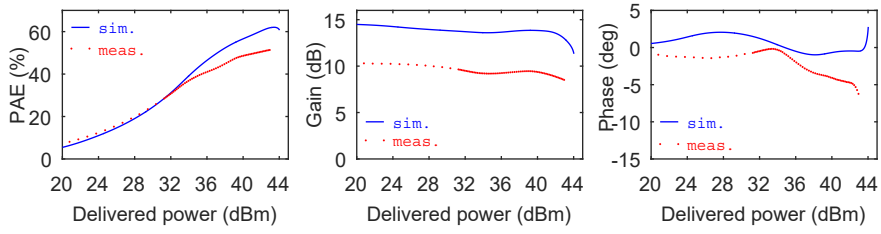


Figure 4.16: (a) Drain efficiency, (b) gain, and (c) phase versus delivered power for cut-ready simulations and measurements.

with a PAE of 39% at 8 dB OPBO.

Modulated measurements for the prototype are presented for a 5, 10 and 20 MHz LTE signal with 8.6 dB PAPR in [Paper B]. The PA presents an average PAE of 40% for all signals with an average delivered power of 35.4 dBm. Without DPD, the PA presents an adjacent channel power ratio lower than –40.5 dBc for all signals - a state-of-the-art raw linearity and efficiency performance, for comparisons with other PAs see [Paper B].

4.4 Discussion

The generalized Doherty PA operation has been proven very useful in practical designs. The combiner parameters can be solved for any impedances of choice. This results in the possibility to absorb the output matching into the combiner. One of the biggest advantages of treating the output combiner as a black-box is therefore that it works extremely well for Doherty PAs with real transistors. Thus, the Doherty PA behavior can be estimated directly from load-pull data, and the full Doherty PA behavior can then be simulated for many different solutions extremely fast.

In [89, 90], a generalized Doherty PA theory for symmetrical transistors was used for optimizing the operation for efficiency, resulting in PA prototypes with record efficiency performance. In this chapter, the generalized Doherty PA theory was expanded beyond symmetrical transistors and all derivations were made analytically. In [Paper B], the expanded generalized Doherty PA theory was solved for linear gain together with reactive mismatch and current scaling, optimizing the operation for a trade-off between efficiency and linearity, resulting in a PA prototype presenting excellent raw linearity while maintaining high efficiency.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

This thesis has aimed to improve the bandwidth-efficiency trade-off, and the efficiency-linearity trade-off in PA design.

It was demonstrated that class-J operation provides the possibility of enhancing the efficiency for a large dynamic range of powers by means of purely reactive load modulation across a large bandwidth. This allows for very simple realization of a varactor-based tunable output matching network. The ideal analysis of the class-J operation established a profound theory behind wideband capabilities of varactor-based DLM. With this theory, it is easier to find optimal solutions and see what trade-offs that have to be made.

The Doherty PA operation was generalized by treating the output combiner as black-box and solving its parameters for arbitrary current profiles. Solving for maximum efficiency and scaling the conventional current ratios results in new solutions with significantly higher gain. Solving for linear gain and high efficiency, and combining current scaling and reactive mismatch results in the possibility of controlling the phase response in the high power region. This control can be used to compensate the severe inherent phase distortion in the high power region – coming from the load modulation in real transistors – in Doherty PAs. Treating the output combiner as a black-box is a robust and flexible method that has created a whole new direction of Doherty PA research.

The reconfigurable wideband class-J DLM PA has potential in applications where many different frequency bands must be supported, allowing for a more compact size of the transmitter. The linear Doherty PA has potential in applications with limited linearization possibilities. Improved raw linearity can relax required DPD complexity or eliminate the need for it altogether.

The thesis has presented two promising techniques for improving the efficiency-bandwidth and efficiency-linearity trade-offs in PAs. The results will therefore contribute to the development of more energy efficient and high capacity wireless services in the future. The focus on lower energy consumption results in the indirect effect of a smaller environmental footprint left behind

by ICT, and local environmental sustainability benefits, for example in badly infrastructured areas where the backhaul infrastructure is run by diesel generators. Altogether, PA advancements are crucial for successful development of ICT, which in turn is a corner-stone for sustainable human development.

5.2 Future Work

Based on the requirements of 5G systems, the author believes the five following PA research topics to be highly interesting:

- Explore the full potential of current scaled Doherty PAs for millimeter-waves. The improved gain of the current scaled Doherty PA is promising since the gain at millimeter-wave frequencies typically is limited.
- Further improve raw PA linearity while maintaining high efficiency. Even though current scaling enables an improved linearity-efficiency trade-off, the back-off gain compression versus efficiency trade-off is still a big problem.
- Explore and expand the bandwidth capabilities of the linear Doherty PA. In this thesis, all Doherty PA derivations were made assuming single frequency operation.
- Cut cost by reducing area, i.e. compact designs, and by using low cost technologies, e.g. Si/SiGe. It would also be interesting to integrate baseband circuit control to enable more complex operation, e.g. gate bias modulation in the Doherty PA. Similar approaches as in Chapter 4 could be used to derive a generalized Doherty PA operation for such controls.
- Improve testbeds and characterization. Since transistor models do not always predict reality good enough, a problem that typically increases versus frequency, a step towards measurement-based designs may be necessary.

Acknowledgments

These past two years as a Ph.D. student have really just flown by. It has been a challenging yet very enjoyable period for me. I feel that I am well on my way to become an independent researcher and I am looking forward to the coming years of pursuing the Ph.D degree. I would like to take this opportunity to express my gratitude to the people who have supported me throughout my studies, making this work possible.

Thank you Prof. Herbert Zirath, head of the Microwave Electronics Laboratory, for letting me be part of your outstanding research group. It has truly been an honor to take part in advanced research on the international arena.

I would like to express the deepest appreciation to my main supervisor Prof. Christian Fager. I cannot imagine a better supervisor than you. Thank you for always being available, despite your incredibly busy schedule, for fruitful discussions. Your supervision has enabled a creative and efficient research environment and your encouragement has allowed me to grow as a researcher and as a person.

My sincere thanks also goes to my assistant supervisor Prof. Dan Kuylenstierna. Thank you for all valuable feedback you have provided me. I would also like to acknowledge your help in developing my pedagogical skills. It has sincerely been enjoyable assisting you teaching.

I am highly indebted to Dr. Mustafa Özen. Your technical expertise has been priceless in my work. I would also like to thank you for always taking the time to brainstorm with me.

I am particularly grateful to Dr. David Gustafsson for providing me with very valuable advice and feedback. Your perfectionism has helped me push myself and reach higher levels.

I wish to acknowledge the help provided by Prof. Koen Buisman. Thank you for your outstanding expertise and for providing me with new perspective on things.

Thank you Dr. Christer Andersson for providing me with assistance with my work on varactor-based dynamic load modulation power amplifiers.

Special thanks to project members Dr. Jonas Hansryd, Dr. Kristoffer Andersson and Thomas Emanuelsson at Ericsson AB for providing your industrial expertise.

Finally, I would like to thank my colleges for providing a good working environment.

This research has been carried out in two projects:

The Energy Efficient Millimeter Wave Transmitters (EMIL) project, financed by the Swedish Governmental Agency of Innovation Systems (VINNOVA), Ericsson AB and Chalmers University of Technology.

The Energy Efficient MIMO Transmitter (EMIT) project, within the GigaHertz Centre, financed by the Swedish Governmental Agency for Innovation Systems (VINNOVA), Chalmers University of Technology, Ericsson, Infineon Technologies, National Instruments, and NXP Semiconductors.

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