Thesis for The Degree of Doctor of Philosophy

Characterisation and Modelling of Graphene FETs for Terahertz Mixers and Detectors

Michael Andersson

Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
Göteborg, Sweden, 2016

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Michael Andersson

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Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
SE-412 96 Göteborg, Sweden
Phone: +46 (0) 31 772 1000

Cover: From left side to right side, agreement of the Volterra FET power detector model to measured GFET NEP, a micrograph of a 600 GHz antenna-integrated direct detector with an SEM image of the GFET and a micrograph of a 200 GHz integrated CPW mixer with an SEM image of the GFET.

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Abstract

Graphene is a two-dimensional sheet of carbon atoms with numerous envisaged applications owing to its exciting properties. In particular, ultrahigh-speed graphene field effect transistors (GFETs) are possible due to the unprecedented carrier velocities in ideal graphene. Thus, GFETs may potentially advance the current upper operation frequency limit of RF electronics.

In this thesis, the practical viability of high-frequency GFETs based on large-area graphene from chemical vapour deposition (CVD) is investigated. Device-level GFET model parameters are extracted to identify performance bottlenecks. Passive mixer and power detector terahertz circuits operating above the present active GFET transit time limit are demonstrated.

The first device-level microwave noise characterisation of a CVD GFET is presented. This allows for the de-embedding of the noise parameters and construction of noise models for the intrinsic device. The correlation of the gate and drain noise in the PRC model is comparable to that of Si MOSFETs. This indicates higher long-term GFET noise relative to HEMTs.

An analytical power detector model derived using Volterra analysis on the FET large-signal model is verified at frequencies up to 67 GHz. The drain current derivatives, intrinsic capacitors and parasitic resistors of the closed-form expressions for the noise equivalent power (NEP) are extracted from DC and S-parameter measurements. The model shows that a short gate length and a bandgap in the channel are required for optimal FET sensitivity.

A power detector integrated with a split bow-tie antenna on a Si substrate demonstrates an optical NEP of 500 pW/Hz$^{1/2}$ at 600 GHz. This represents a state-of-the-art result for quasi-optically coupled, rectifying direct detectors based on GFETs operating at room temperature.

The subharmonic GFET mixer utilising the electron-hole symmetry in graphene is scaled to operate with a centre frequency of 200 GHz, the highest frequency reported so far for graphene integrated circuits. The down-converter circuit is implemented in a coplanar waveguide (CPW) on Si and exhibits a conversion loss (CL) of 29 $\pm$ 2 dB in the 185-210 GHz band.

In conclusion, the CVD GFETs in this thesis are unlikely to reach the performance required for high-end RF applications. Instead, they currently appear more likely to compete in niche applications such as flexible electronics.

Keywords: Field-effect transistors (FETs), graphene, integrated circuits, microwave amplifiers, millimetre and submillimetre waves, nanofabrication, noise modelling, nonlinear device modelling, power detectors, subharmonic resistive mixers, terahertz detectors, Volterra.

List of publications

Appended papers

This thesis is based on the following papers:

[A] **M. Andersson** and J. Stake, "An Accurate Empirical Model Based on Volterra Series for FET Power Detectors," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 5, pp. 1431-1441, May 2016. DOI: 10.1109/TMTT.2016.2532326

[B] A. Zak, **M. Andersson**, M. Bauer, J. Matukas, A. Lisauskas, H. G. Roskos, and J. Stake, "Antenna-Integrated 0.6 THz FET Direct Detectors Based on CVD graphene," in *Nano Letters*, vol. 14, no. 10, pp. 5834-5838, September 2014. DOI: 10.1021/nl5027309

[C] **M. Andersson**, Y. Zhang, and J. Stake, "A 185-215 GHz Subharmonic Resistive Graphene FET Integrated Mixer on Silicon," submitted to *IEEE Transactions on Microwave Theory and Techniques*, July 2016.

[D] **M. Andersson**, O. Habibpour, J. Vukusic, and J. Stake, "Resistive Graphene FET Subharmonic Mixers: Noise and Linearity Assessment," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 4035-4042, December 2012. DOI: 10.1109/TMTT.2012.2221141

[E] **M. Andersson**, O. Habibpour, J. Vukusic, and J. Stake, "10 dB small-signal graphene FET amplifier," in *Electronics Letters*, vol. 48, no. 14, pp. 861-863, July 2012. DOI: 10.1049/el.2012.1347

[F] M. Tanzid, **M. Andersson**, J. Sun, and J. Stake, "Microwave noise characterization of graphene field effect transistors," in *Applied Physics Letters*, vol. 104, no. 1, pp. 013502-1−013502-4, January 2014. DOI: 10.1063/1.4861115

[G] **M. Andersson**, A. Vorobiev, J. Sun, A. Yurgens, S. Gevorgian, and J. Stake, "Microwave characterization of Ti/Au-graphene contacts," in *Applied Physics Letters*, vol. 103, no. 17, pp. 173111-1−173111-4, October 2013. DOI: 10.1063/1.4826645

[H] S. Bidmeshkipour, A. Vorobiev, **M. Andersson**, A. Kompany, and J. Stake "Effect of ferroelectric substrate on carrier mobility in graphene field-effect transistors," in *Applied Physics Letters*, vol. 107, no. 17, pp. 173106-1−173106-5, October 2015. DOI: 10.1063/1.4934696

[I] **M. Andersson**, A. Özçelikkale, M. Johansson, U. Engström, A. Vorobiev, and J. Stake, "Feasibility of Ambient RF Energy Harvesting for Self-Sustainable M2M Communications Using Transparent and Flexible Graphene Antennas," accepted for publication in *IEEE Access*, August 2016.

Other papers and publications

The following papers and publications are not appended to the thesis, either due to contents overlapping with appended papers, or due to contents not related to the thesis.

[a] Y. Zhang, **M. Andersson**, and J. Stake, "A 200 GHz Graphene FET Resistive Subharmonic Mixer," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, San Fransisco, USA, 2016. DOI: 10.1109/MWSYM.2016.7540287

[b] A. Generalov, **M. Andersson**, X. Yang, and J. Stake, "Optimization of THz graphene FET detector integrated with a bowtie antenna," *10th European Conference on Antennas and Propagation (EuCAP)*, Davos, Switzerland, 2016. DOI: 10.1109/EuCAP.2016.7481475

[c] M. Bauer, A. Lisauskas, A. Zak, **M. Andersson**, J. Stake, J. Matukas, and H. Roskos, "Terahertz detection with graphene field-effect transistors," *Graphene Week 2015*, Manchester, United Kingdom, 2015.

[d] M. Bauer, **M. Andersson**, A. Zak, P. Sakalas, D. Čibiraité A. Lisauskas, M. Schröter, J. Stake, and H. Roskos, "The potential of sensitivity enhancement by the thermoelectric effect in carbon-nanotube and graphene Tera-FETs," *19th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures (EDISON'19)*, Salamanca, Spain, 2015. DOI: 10.1088/1742-6596/647/1/012004

[e] **M. Andersson**, A. Vorobiev, S. Gevorgian, and J. Stake, "Extraction of carrier transport properties in graphene from microwave measurements," *European Microwave Conference (EuMC) 2014*, Rome, Italy, 2014. DOI: 10.1109/EuMC.2014.6986444

[f] **M. Andersson**, A. Vorobiev, S. Gevorgian, and J. Stake, "Comparison of carrier scattering mechanisms in chemical vapor deposited graphene on fused silica and strontium titanite substrates," *Graphene Week 2014*, Göteborg, Sweden, 2014.

[g] A. Zak, **M. Andersson**, M. Bauer, A. Lisauskas, H. Roskos, and J. Stake, "20 μm gate width CVD graphene FETs for 0.6 THz detection," *39th IEEE International Conference on Infrared, Millimeter and Terahertz Waves*, Tucson, Arizona, 2014. DOI: 10.1109/IRMMW-THz.2014.6956250

[h] **M. Andersson**, A. Vorobiev, J. Sun, A. Yurgens, and J. Stake, "Towards Graphene Electrodes for High Performance Acoustic Resonators," in *37th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE)*, Warnemünde, Germany, 2013.

[i] **M. Andersson**, O. Habibpour, J. Vukusic, and J. Stake, "Noise Figure Characterization of a Subharmonic Graphene FET mixer," in *IEEE MTT-S International Microwave Symposium (IMS) Digest*, Montreal, Canada, 2012. DOI: 10.1109/MWSYM.2012.6259519

[j] **M. Andersson**, O. Habibpour, J. Vukusic, and J. Stake, "Towards Practical Graphene Field Effect Transistors for Microwaves," in *Giga-Hertz Symposium*, Stockholm, Sweden, 2012.

Acronyms

2DEG Two-Dimensional Electron Gas. 1, 8

Al_2O_3 Aluminium Oxide. 8, 18, 21, 27

ALD Atomic Layer Deposition. 18, 21

CAD Computer-Aided Design. 38

CL Conversion Loss. 34, 42

CMOS Complementary Metal-Oxide-Semiconductor. 2, 15, 30, 31, 43, 47, 49, 53

CNT Carbon NanoTube. 2

CPW CoPlanar Waveguide. 38, 43–45

CVD Chemical Vapour Deposition. 3, 12–16, 19–22, 25, 30, 31, 37, 39, 41, 51, 53, 54

DOS Density of States. 8, 19

EM ElectroMagnetic. 40

FET Field-Effect Transistor. 1–3, 5, 6, 9, 11, 18, 19, 22–28, 30–34, 40–43, 47–49, 53, 54

GaAs Gallium Arsenide. 1, 7, 8, 22, 30, 31, 37, 42, 43

GaN Gallium Nitride. 7, 42

GFET Graphene Field-Effect Transistor. 2, 3, 5, 9, 11, 12, 17–31, 33, 34, 39–46, 49, 50, 53, 54

h-BN Hexagonal Boron Nitride. 2, 8, 10, 13, 14, 16, 54

HEMT High Electron Mobility Transistor. 1, 2, 19, 22, 25, 26, 29–31, 37, 43, 49, 54

IF Intermediate Frequency. 3, 34, 37, 42

IIP3 Input Third-Order Intercept Point. 42

IM3 Third-Order Intermodulation. 34, 35

InAs Indium Arsenide. 2, 7

InP Indium Phosphide. 1, 2, 22, 29, 31, 37

$LiNbO_3$ Lithium Niobium Oxide. 11

LNA Low-Noise Amplifier. 1, 30, 37, 54

LO Local Oscillator. 3, 32, 34, 35, 42, 43, 45, 53

M2M Machine-to-Machine. 50, 51

MAG Maximum Available Gain. 25

MESFET Metal-Semiconductor Field-Effect Transistor. 1

MMIC Monolithic Microwave Integrated Circuit. 1, 37

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor. 3, 30, 31, 54

NEP Noise Equivalent Power. 32, 34, 47, 49, 50, 53

NF Noise Figure. 26, 28, 41

NW NanoWire. 2

PMMA Poly(Methyl MethAcrylate). 14, 17, 22

RF Radio Frequency. 15, 17, 18, 22, 32, 34, 37, 42, 43, 45, 47, 48, 50, 51, 53, 54

SEM Scanning Electron Microscope. 14, 20

SiC Silicon Carbide. 11, 14–16, 22, 26, 30, 31, 40, 41, 54

SiO_2 Silicon Dioxide. 8–12, 14, 16, 18, 20, 30

THz Terahertz. 1–3, 37, 46, 49, 53

TLM Transmission Line Method. 20, 21, 23, 26

Notations

β_v Detector voltage responsivity. 32, 33, 48

Γ_S Source reflection coefficient. 28, 39, 40

Δf Noise bandwidth. 27

ε Dielectric permittivity. 10

μ Carrier mobility. 7, 9, 10, 21

ρ Electrical resistivity. 7, 10, 25

σ Electrical conductivity. 7–9

C Gate-drain noise correlation coefficient. 27–30

C_{gd} Intrinsic gate-drain capacitance. 24–28, 32, 33, 48

C_{gs} Intrinsic gate-source capacitance. 24–26, 32, 33, 48

$\mathcal{E}$ Electric field. 9, 10

E Energy. 5, 6, 8, 10

E_F Fermi energy. 6, 8

E_g Energy bandgap. 7, 11

G_T Transducer power gain. 39

I_{ds} Drain-source DC current. 22, 25, 28–31, 33, 34, 54

L_g Gate length. 9, 23–26, 28–31, 39, 48, 49

NF_{min} Minimum noise figure of a two-port. 26, 28, 41

P PRC drain noise coefficient. 27–29

R PRC gate noise coefficient. 27–29

R_D Parasitic drain resistance. 9, 19, 23–26, 33, 48

R_G Parasitic gate resistance. 23–26, 30, 31

R_S Parasitic source resistance. 9, 19, 23–26, 30, 31, 33, 48

R_n Noise resistance. 26, 28

R_{sh} Sheet resistance. 19–22, 50

S_{BA} Ambient RF intensity to harvest. 50

T_d Equivalent drain noise temperature. 26–29, 41

T_g Equivalent gate noise temperature. 26–29, 41

T_{min} Minimum noise temperature of a two-port. 26, 29

T_n Equivalent input noise temperature. 26, 28, 41

U Mason's unilateral gain. 23–25

V_{Dirac} Gate voltage of the Dirac point. 9, 34, 35

W_g Gate width. 9, 19, 24–26, 31, 39, 48

Y Electrical admittance. 26

Z Electrical impedance. 44

Z_0 Transmission line characteristic impedance. 22, 26, 33, 47, 48

$\overline{e^2}$ Noise voltage. 27

f Frequency. 26, 27, 29, 32, 43, 47, 48

f_{max} Maximum frequency of oscillation. 1, 2, 23–26, 29, 31, 37, 39, 41

f_T Cutoff frequency. 1, 2, 23–26, 30, 31, 39

g_{me} Extrinsic (DC) transconductance. 22, 25, 30, 31

g_{mi} Intrinsic (small-signal) transconductance. 24, 25, 28, 31

h_{21} Short circuit current gain. 23

$\hbar$ Planck's constant. 6, 8, 11

$\overline{i_d^2}$ Drain noise current. 27, 28

$\overline{i_g^2}$ Gate noise current. 27, 28

k_B Boltzmann's constant. 8, 10, 11, 27, 28

n Total carrier concentration. 7–11, 21

n_0 Residual carrier concentration. 8, 21

n_{th} Thermally generated carrier concentration. 8, 10

q Electron charge. 7, 9, 21, 27

v_F Fermi velocity. 6, 8, 11

v_{sat} Carrier saturation velocity. 10, 11

Contents

Chapter 1

Introduction

High-frequency electromagnetic waves in the microwave (300 MHz to 100 GHz) and terahertz (loosely defined as 100 GHz to 10 THz) frequency regions of the spectrum are used in numerous applications. Wireless technology that operates in the lower-GHz range is a defining factor of life today as an enabler of the rapidly increasing flow of data exchanged in modern society. In the THz regime, historically niche applications in spectroscopy, earth remote sensing and radio astronomy are dominating [1]. Nevertheless, more recently, interest and practical implementation of THz in fields closer to everyday life, including security and surveillance [2], medicine and disease diagnostics [3], and future high-speed communication networks [4] have emerged.

Today, the lack of compact, room-temperature and affordable sources and transmitters, detectors and receivers hinders the full utilisation of the great potential of THz waves. Attempts to bridge this so-called THz gap have been initiated both by increasing in frequency from the electronics side [5] and by decreasing in frequency from the photonics side [6]. In solid-state technology, the Schottky diode is the longtime workhorse for THz electronics [7]. Importantly, the noise of high spectral resolution and diode-based heterodyne receivers has a fundamental limit given by the conversion loss of the down-converting mixer.

An active receiver designed with field-effect transistors (FETs) permits both potentially lower noise and a higher circuit integration level. Presently, FETs are used in THz receivers to feed power to diode multiplier chains and for intermediate frequency low-noise amplifiers (LNAs). Vast progress has been achieved since the demonstration of the first microwave GaAs MESFET in 1967 [8] and the advent of the GaAs monolithic microwave integrated circuit (MMIC) technology during the 1970s [9]. Subsequently, the strategy to achieve higher frequencies has been to scale to the shortest transistor channels possible and use channel materials with the highest possible carrier velocities. A milestone was the introduction of the GaAs high electron mobility transistor (HEMT) [10]. The HEMT utilises a 2DEG channel to separate the carriers from the impurity dopants. Currently, the leading FET technology is the InP HEMT with maximum frequency of oscillation $f_{max} = 1.5$ THz [11] and cutoff frequency $f_T = 688$ GHz [12]. This allows for the of design small-signal InP HEMT amplifiers above 1 THz [11]. In addition, passive FET detectors are used in low-spectral-resolution, incoherent receivers at several THz [13].

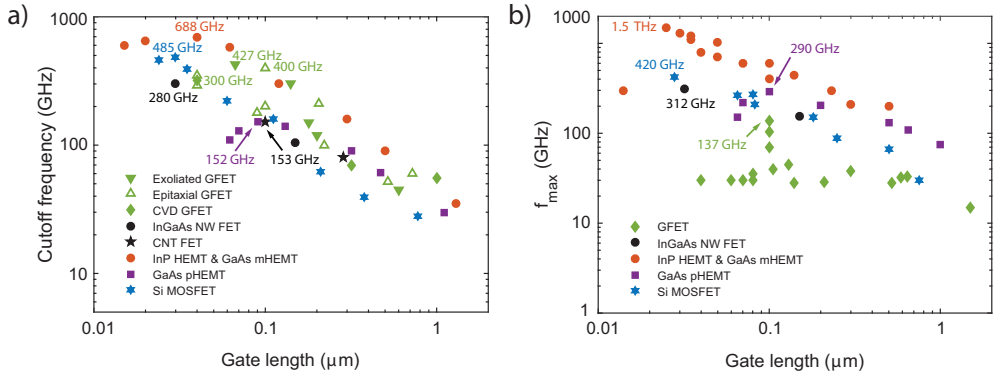

Fig. 1.1: State-of-the-art de-embedded a) f_T and b) f_{max} for HEMTs, Si CMOS, CNT [11, 17] and NW FETs [15, 16] against reported intrinsic GFETs [11, 17–21].

However, as shown in Fig. 1.1 the InP HEMT has seemingly reached its performance limits in terms of gate length scaling. Moreover, the modern III-V epitaxy enables the growth of pure InAs channels on InP substrates to maximise the carrier velocity. Furthermore, InP HEMT is an expensive and low-yield technology. Consequently, researchers constantly scrutinise new device layouts and new candidate materials with potentially higher carrier velocities for FETs to reach further into the THz range. In this context, semiconducting carbon nanotubes (CNTs) [14] and wrap-around gated InAs nanowires (NWs) [15,16] are explored. To date, they are not competitive with the state-of-the-art technologies in Fig. 1.1 for high-frequency transistors.

In this thesis, the intrinsically high-mobility carbon material graphene [22] is studied for use in high-frequency FETs. Graphene belongs to a group of two-dimensional materials attracting significant attention for electronics due to their distinctive and diverse properties [23]. The toolbox contains zero-bandgap materials (graphene, silicene and germanene), semiconductors (MoS_2 and black phosphorous) and insulators (boron nitride). Potential applications for these materials are found based both on their individual attributes and by the utility enabled when stacked in heterostructures [24]. Notably, graphene alone exhibits a set of qualities that open new possibilities. The electrical conductivity together with bendability and transparency is advantageous for touchscreens and transparent electrodes [25]. The low ratio of volume to area combined with the field effect is favourable for sensors [26]. The outstanding mobility and mechanical flexibility make graphene a potential platform for the next generation of high-speed transistors [17] and ubiquitous electronics [27].

The state-of-the-art high-frequency GFETs are summarised in Fig. 1.1. Judging from the record intrinsic cutoff frequency $f_T = 427$ GHz [18], graphene has an edge over CNTs and NWs and is even comparable to III-V HEMTs. In the absence of a bandgap, the poor current saturation in GFETs results in low f_{max} values. Moreover, there is an alarming discrepancy in the extrinsic values, which include the parasitics and are limited to <50 GHz [19, 21]. The carrier mobility in GFETs is currently greatly impeded by the oxides sandwiching graphene. This may be solved by sandwiching graphene in hexagonal boron nitride (h-BN) [28]. However, there is presently no *in situ* growth method for wafer-scale h-BN/graphene/h-BN heterostructures.

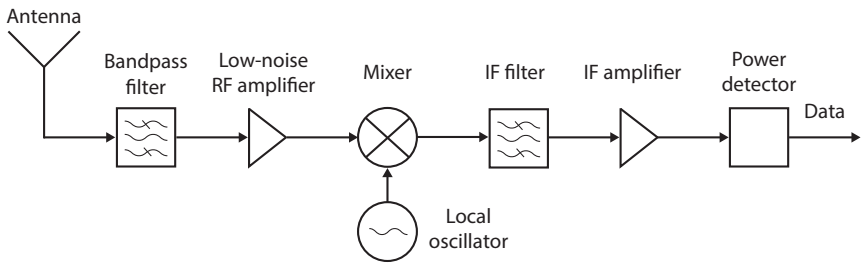

Fig. 1.2: The block diagram of a typical heterodyne receiver. The mixer is not present in an incoherent receiver, resulting in lower spectral resolution.

An essential objective of this thesis work was to advance the wafer-scale GFET technology. Consequently, a fabrication process for GFETs on graphene grown by chemical vapour deposition (CVD) on copper foils and transferred to silicon substrates [29] was developed. The process presented in this thesis can be transferred to full wafer-scale [30] and potentially to flexible substrates [27]. The main contributions to the field of graphene high-frequency electronics are divided into two categories. First, the extraction of models to perceive current and fundamental problems for GFETs is described. Second, the fabrication of circuit demonstrators towards a GFET THz detector focal-plane array [31] and a GFET-based millimetre wave heterodyne receiver is described (Fig. 1.2).

The model highlight is the verification of analytical expressions for the FET power detector figures of merit based on a Volterra analysis of the nonlinear FET equivalent circuit [Paper A]. The missing bandgap, rather than the low mobility, is implied to be the major obstacle for higher GFET sensitivity.

Moreover, noise models of active microwave GFETs for small-signal IF amplifiers are extracted to establish a first indication of the long-term prospects of the GFET noise performance [Paper F]. The noise correlation factor and the gate length normalised noise figure are comparable with Si MOSFETs. Future studies will establish whether higher-quality gate stacks improve the correlation or if it is fundamental to the device structure.

The demonstrator highlights are the subharmonic GFET mixer scaled to a record frequency of 200 GHz for integrated graphene circuits [Paper C] and the quasi-optical GFET detector with record sensitivity at 600 GHz [Paper B]. The subharmonic mixer operation is inherent in graphene due to the symmetry of electron and hole carriers [32] and is advantageous at millimetre waves to allow a lower frequency for the high-power local oscillator (LO) source.

1.1 Thesis outline

The thesis chapters introduce graphene and microwave technology in a wider context to set the scene for the appended papers. *Chapter 2* compares the relevant theoretical electronic properties of graphene to the current practical status of graphene synthesis. *Chapter 3* describes the figures of merit and methods of characterisation and modelling for active and passive microwave and THz GFETs. *Chapter 4* presents the technological background for the integrated GFET circuit demonstrators. *Chapter 5* finally draws summarising conclusions out of which future work directions are identified.

Chapter 2

Graphene properties for high-speed electronics

Fast microwave FETs are core building blocks, i.e., in high-speed communication networks. To realise such a device, the carrier transit time under the gate must be short. This necessitates a short gate length transistor and a channel material with the highest possible carrier velocity. This chapter presents the theoretical potential and practical limitations of graphene in this context to understand the current performance and future improvements of GFETs.

2.1 Graphene band structure

Graphene consists of a monolayer of carbon atoms in a hexagonal lattice, connected via sp^2-hybridisation, as shown in Fig. 2.1a). In graphene, each atom has three neighbours connected by strong covalent, in-plane σ-bonds. Whereas these electrons are localised, defining the carbon-carbon binding distance of $a_{C-C} = 1.42$ Å, the remaining valence electrons are delocalised in out-of-plane covalent π-bonds as illustrated in Fig. 2.1b). The span of the π-orbitals defines the thickness of graphene as 0.34 nm. The σ-bonds constitute the mechanical strength of graphene, whereas the electrons in π-bonds account for its electrical conductivity. In principle, the π-electrons move in a plane outside the graphene sheet, resulting in a negligible lattice collision rate and an extraordinary carrier velocity given an applied electric field. Often, *single-layer* or *monolayer* graphene is clearly emphasised to distinguish it from bilayer or few-layer graphene (> 2 layers), with distinctively different properties. Unless explicitly stated, in this thesis, graphene refers to a monolayer material.

Understanding the unique electrical properties of graphene starts with the knowledge of its energy dispersion (electronic band structure), i.e., the energy-momentum relation for electrons and holes, first derived in 1947 [33]. Using a nearest neighbour tight-binding (NNTB) approximation of the honeycomb lattice, the dispersion of the π-electrons [23] can be expressed as

$$E(\mathbf{k}) = \pm\gamma\sqrt{1 + 4\cos\frac{\sqrt{3}a}{2}k_x\cos\frac{a}{2}k_y + 4\cos^2\frac{a}{2}k_y}, \tag{2.1}$$

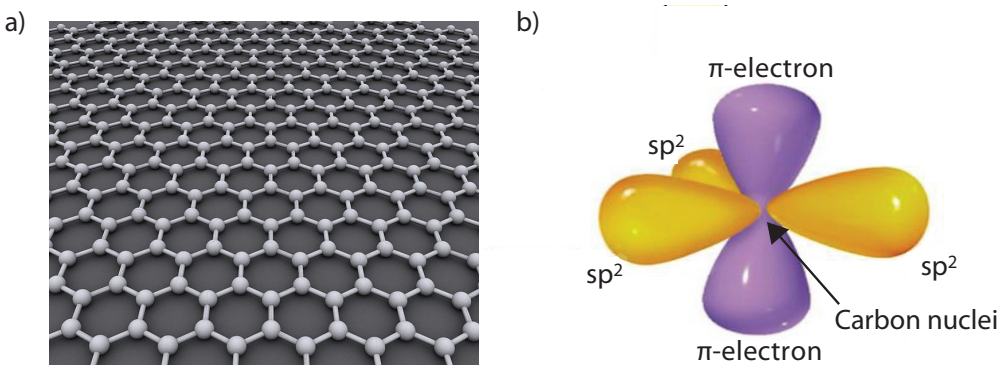

Fig. 2.1: a) Graphene honeycomb lattice. b) Visualisation of electron clouds in sp^2-hybridisation, localised in plane σ-bonds and out of plane delocalised π-electrons [34].

where $\gamma = 2.8$ eV is the nearest neighbour overlap energy, and the constant $a = \sqrt{3}a_{C-C} = 2.46$ Å. In Eq. 2.1, which is derived under the assumption of electron and hole symmetry, the plus and minus signs correspond to the conduction (π^*) and valence (π) bands, respectively. The NNTB model agrees well with *ab initio* calculations within $\pm$ 1 eV of the intrinsic Fermi energy level, $E_F = 0$ eV, where the conduction and valence bands touch without a bandgap. The bandstructure of graphene is illustrated in Fig. 2.2.

The performance of graphene-based electronic devices is governed mainly by the dispersion when $|E| < 0.4$ eV, the E_F range reachable by field- or impurity-induced carriers. This corresponds to the regions closest to the six K and K′ points of the first Brillouin zone. Here, the energy-momentum relation is further simplified to a cone - see the inset of Fig. 2.2 - given by

$$E(\mathbf{k}) = \pm\hbar v_F \sqrt{k_x^2 + k_y^2}. \tag{2.2}$$

In Eq. 2.2, $\hbar$ is Planck's constant, and $v_F = 3\gamma a/2\hbar \simeq 10^8$ cm/s is the Fermi velocity (upper limit of the carrier velocity) in graphene within the tight binding approximation. The linear dispersion indicates massless particles described by the *Dirac equation*, giving the names *Dirac points* where the conduction and valence bands meet. These massless particles, the so-called *Dirac fermions*, represent the origin of the superior carrier mobilities expected in graphene.

2.2 Carrier transport in graphene

The high-frequency performance of FETs depends on the carrier dynamics in the channel, quantified by the mobility and peak velocity, i.e., the response of the carriers to an applied electric field. Graphene is compared with Si, III-V semiconductors and single-layer MoS_2 in Table 2.1. The intrinsic cut-off frequency, i.e., the high-frequency limit of a material, can be related to these properties. In principle, $f_{T,int} = \frac{v}{2\pi L_g}$, where the carrier velocity in the channel is ultimately bound by the peak velocity $v = v_{peak}$. In practice, the importance of the peak velocity increases compared to the mobility due to higher electric fields when scaling the gate length. Clearly, graphene appears to be an outstanding candidate to reach extremely high frequencies.

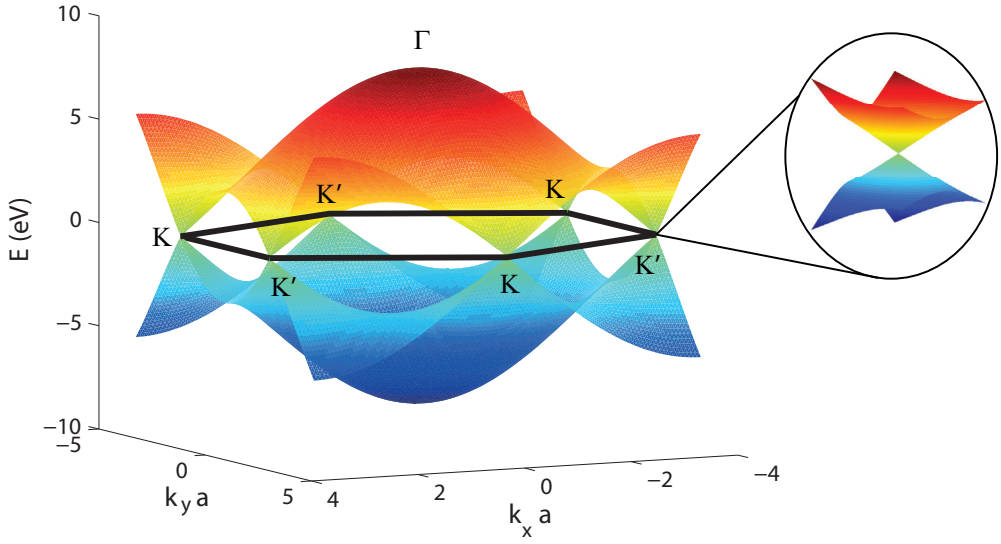

Fig. 2.2: Band structure of graphene in the tight binding approximation within the 1st Brillouin zone (Eq. 2.1). Inset shows the famous Dirac cone (Eq. 2.2).

Table 2.1: Effective mass, low-field mobility, peak velocity and bandgap of low-doped semiconductors at room temperature. *Intrinsic, $n \sim 10^{12}$ cm^{-2}.

	MoS_2	Si	GaN	GaAs	InAs	InSb	Graphene*
m_e^*/m_0	0.6	0.98	0.19	0.063	0.023	0.015	0
μ_e (cm^2/Vs)	100 [35]	1,400	1,600	8,000	33,000	88,000	200,000 [36]
μ_h (cm^2/Vs)	-	500	200	400	500	850	200,000
v_{peak} (10^7 cm/s)	0.3 [35]	1	2.4	1.8	3.5	5	~ 10
E_g (eV)	1.8	1.12	3.4	1.43	0.36	0.18	0

However, in device fabrication, a substrate and gate dielectric sandwich are usually required. Unless care is taken, this leads to increased scattering of the out-of-plane electrons and degradation of the ideal values in graphene. Accordingly, most results are in the diffusive transport regime with a carrier mean free path shorter than the sample length. In the diffusive limit, the conductivity is given by $\sigma^{-1} = (nq\mu_C + \sigma_{min})^{-1} + \rho_s$ [28,37]. Here, μ_C models the mobility due to long-range Coulomb scattering, and ρ_s models the short-range scattering from neutral defects in the graphene lattice. Furthermore, σ_{min} is the residual conductivity due to remaining carriers when biasing for the Fermi level to lie at the Dirac point of the electronic spectrum. In samples with high impurity concentration, $\sigma \propto n$ at high carrier densities, with Coulomb scattering being the dominant mechanism [22, 38]. However, in cleaner samples, a sublinear $\sigma(n)$ is found, attributed to short-range scattering [28, 39]. In addition to the diffusive regime, ballistic transport has been reported from cryogenic temperatures all the way up to room temperature [40–42]. Note also that the sublinear $\sigma \propto \sqrt{n}$ has been interpreted as ballistic transport in suspended graphene with a micrometre mean free path comparable to the sample dimensions [40]. The mechanisms governing the concentration, minimum conductivity, mobility and mean free path in graphene are discussed next.

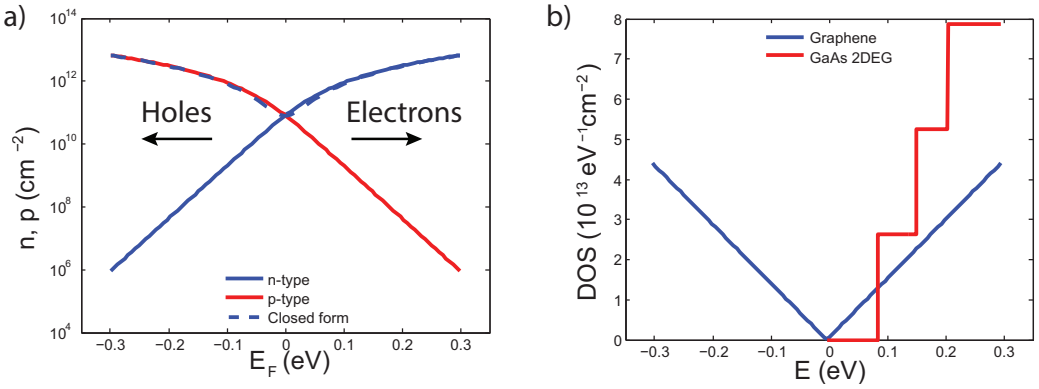

Fig. 2.3: a) Carrier concentrations versus E_F at room temperature [23] and b) DOS in graphene compared with an AlGaAs/GaAs 2DEG with $n_s = 0.67 \cdot 10^{12}$ cm^{-2} [44].

2.2.1 Gate-induced versus residual carrier concentration

Due to the gapless spectrum of graphene, either electron or hole carriers may be induced by shifting the Fermi level. This can be accomplished via the field effect [22], charge transfer from metal contacts to graphene [43] or molecules adsorbed on the graphene surface [26]. The carrier concentration versus the Fermi level and the density of states (DOS) versus energy level in graphene at room temperature are plotted in Fig. 2.3. The carrier density can easily exceed that of a two-dimensional electron gas (2DEG) where $n_s \sim 10^{12}$ cm^{-2} [44]. In fact, with the Al_2O_3 dielectric in the devices fabricated as part of this thesis, $n > 1 \cdot 10^{13}$ cm^{-2} is easily attained at a top-gate voltage $V_g \lesssim 5$ V.

Importantly, without external bias and at room temperature, the thermal carrier concentration in the absence of a bandgap is given by

$$n_{th} = \frac{\pi}{6}\left(\frac{k_B T}{\hbar v_F}\right)^2, \tag{2.3}$$

which results in $n_{th} = 8 \cdot 10^{10}$ cm^{-2}. The concentration of carriers is identically zero only at $T = 0$ K, for ideal and perfectly clean graphene. All experimental graphene, however, requires an additional parameter to explain the behaviour at the minimum conductivity point, i.e., the gate voltage that most closely corresponds to the Dirac point of the electronic spectrum. This parameter is the so-called residual carrier density, n_0. In particular, σ_{min} exhibits a wider plateau at room temperature [38] and a weaker temperature dependence upon cooling than expected solely from thermal generation [40]. It is the result of a spatially inhomogeneous potential created by impurities in the substrate or at the graphene-substrate interface, with concentration n_{imp} [39]. As a consequence, the degree of disorder and thus the residual carrier concentration are highly substrate-dependent properties. It ranges from $10^{11} - 10^{12}$ cm^{-2} on SiO_2/Si samples [38] via $\sim 10^{10}$ cm^{-2} on h-BN [28] to $\sim 10^8$ cm^{-2} in a current-annealed, suspended sample [37]. As a rule of thumb, the temperature dependence of σ_{min} is suppressed unless $k_B T > E_{puddle} = \hbar v_F \sqrt{\pi n_0}$.

2.2.2 Extraction of the low-field mobility

At low transverse electric fields, the carrier drift velocity is linear in field strength with the low-field mobility, $v_{drift} = \mu\mathcal{E}$. The carrier mobility is thus a decisive property for the FET speed at long gate lengths. Several distinct ways to extract the carrier mobility exist, and some care should be taken in comparing the values obtained by the different methods [45].

First, the *Hall effect mobility* in graphene can be measured on a dedicated Hall bar [22,40] or van der Pauw [46,47] structure with the aid of a transverse magnetic field. Because the mobility and the carrier concentration appear as a product in the expression for resistivity, a Hall measurement is the only method that unambiguously separates them.

Second, the *conductivity mobility* defined explicitly by $\mu \equiv \frac{\sigma}{nq}$ is sometimes reported for graphene [22, 41, 48]. The conductivity, σ, is derived from the four-contact resistance of a graphene patch with well-defined dimensions. The carrier density, n, is estimated via the gate capacitance and voltage.

Third, the *field-effect mobility* defined by the slope of the conductivity curve $\mu \equiv \frac{1}{C_g}\frac{d\sigma}{dV_g}$ is occasionally presented [28, 49]. Likely the most common method for graphene is a variant of the field-effect mobility based on fitting of the GFET transfer characteristics [50]. This is valid for samples with mobility limited by charged impurity scattering, where $\sigma \propto n$, which yields one carrier-density-independent value for conductivity mobility. The contact resistance is excluded by fitting to the complete expression

$$R_{tot} = 2R_c + R_{channel} = R_S + R_D + \frac{L_g}{W_g q \mu \sqrt{n_0^2 + \left(\frac{C_g(V_g - V_{Dirac})}{q}\right)^2}}, \quad (2.4)$$

where $2R_c$ is the sum of the drain and source contact resistances. This is the method of choice to extract mobility for the GFETs reported in this thesis because no special test structure is required to be fabricated.

2.2.3 Limitations on the low-field mobility in graphene

The dielectric environment in most cases limits transport in graphene to the diffusive regime. Several carrier scattering mechanisms recognised to limit the mobility of graphene are listed below. The list starts from the fundamental mechanisms and moves on to the detrimental limitations of the common SiO_2 substrates, and the discussion finally moves on to its possible replacement.

- **Longitudinal acoustic phonons (LAP) [36]**: The theoretical upper bound for mobility is set by the LAP interaction. It contributes with the resistivity of 30 Ω/sq at room temperature independent of concentration [36]. Although this results in a mobility $\mu \sim 200,000$ cm^2/Vs at a carrier concentration $n = 10^{12}$ cm^{-2}, it drops rapidly as $\mu \propto 1/n$.

- **Charged impurities (Coulomb scattering) [38, 39]**: For graphene on SiO_2, the phonon scattering is masked by typical impurity densities which limit the experimental mobility to $\sim 10,000$ cm^2/Vs [22, 50].

Table 2.2: Temperature dependence of resistivity, ρ, as a result of scattering mechanisms in graphene. E_0 is the energy of the surface optical phonon mode.

Scattering mechanism	T interval	T dependence
Longitudinal acoustic phonons [36]	$T > 20$ K	$\rho \propto T$
Charged impurities (Coulomb) [36]	$\forall\ T$	None
Remote interfacial phonons [36]	$\forall\ T$	$\rho \propto \frac{1}{e^{E_0/k_B T}-1}$
Flexural phonons [52]	$\forall\ T$	$\rho \propto T^2$

- **Remote interfacial phonons (RIP) [36,51]**: Even in the ideal case of no charged impurities, the lowest RIP mode of SiO_2 (59 meV) would set an upper limit of 40,000 cm^2/Vs at room temperature [36]. Exchanging the SiO_2 substrate for a high-ε substrate screens the impurities but at the expense of low-energy surface optical phonons. This increases RIP scattering and results in a small improvement at 300 K [51].

- **Flexural phonons (FP) [52]**: This represents a dominant mechanism of scattering in free-standing graphene samples. It consists of static ripples introduced on rough substrate surfaces that are frozen in when suspending the graphene.

Along these lines, h-BN provides an alternative substrate with a number of valuable properties [28]. It has the same hexagonal structure as graphene with a lattice mismatch of only $\sim 2\%$. The surface of h-BN is inert, drastically reducing the attachment of impurities compared with SiO_2. As a result, one benefits from the higher RIP modes of h-BN (>100 meV) while maintaining the gating ability of SiO_2 ($\varepsilon_{h-BN} \sim \varepsilon_{SiO_2}$) and without losing performance due to the weak impurity screening. At room temperature, graphene on h-BN [42] may show significantly higher mobility than suspended graphene [52]. Graphene conforms to the extremely smooth surface of h-BN, therefore limiting the scattering on graphene ripples. In fact, mobilities at the LAP limit at room temperature have been shown for graphene encapsulated in h-BN [41]. In addition, h-BN would allow for benefits in cooled graphene devices, as concluded from Table 2.2. At carrier concentrations $n \gg n_{th}$, the mobility has an inverse temperature dependence compared with the resistivity. The large-scale feasibility of graphene and h-BN synthesis is discussed in Section 2.3.

2.2.4 High-field carrier velocities in graphene

In general, in high electric fields, the carrier velocity reaches a peak value before approaching the saturated velocity. However, in graphene, a soft saturation without peak is observed, which is described by [48]

$$v_{drift} = \frac{\mu\mathcal{E}}{\left(1 + (\mu\mathcal{E}/v_{sat})^{\gamma}\right)^{1/\gamma}}, \tag{2.5}$$

where μ is the low-field mobility, and v_{sat} is the saturated carrier velocity. At short gate lengths, the saturation velocity is thus a more crucial parameter for

graphene than the mobility to make a fast FET. The saturation velocity in graphene is bound by the optical phonon energy, the carrier concentration and the temperature as a result of phonon occupation, $N_{OP} = 1/(e^{\hbar\omega_{OP}/k_BT} - 1)$. This can be well predicted by the simple model

$$v_{sat} = \frac{2\omega_{OP}}{\pi\sqrt{\pi n}}\sqrt{1 - \frac{\omega_{OP}^2}{4\pi n v_F^2}}\frac{1}{N_{OP}+1}. \tag{2.6}$$

For ideal graphene, the saturation velocity is theoretically bound by the Fermi velocity, $v_F = 10^8$ cm/s, by the intrinsic phonon mode, $\hbar\omega_{OP} = 160$ meV, in the limit of low carrier concentration. On SiO_2, however, it is severely deteriorated as a result of the substrate surface optical phonon mode with lower energy, $\hbar\omega_{OP} = 55$ meV [48]. Consequently, the extracted v_{sat} on SiO_2 and SiC is in the range of $1 - 2 \cdot 10^7$ cm/s. Higher drift velocities by a factor of two should be possible if the substrate limitation can be overcome. In addition, for nanometre sized GFETs, the high-frequency limit can be enhanced by transient velocity overshoot [53], observed also in III-V semiconductors [44].

2.2.5 Opening a bandgap in graphene

In GFETs, a bandgap in graphene is desirable for improved performance of the devices. Two main routes are to induce it either by lateral confinement in a graphene nanoribbon or by a perpendicular field in bilayer graphene.

First, in *graphene nanoribbons*, the bandgap depends inversely on the width, w, as $E_g = \alpha/w$. The proportionality constant crucially depends on the edge structure and roughness [54]. Ribbons prepared by electron beam lithography and oxygen plasma etching have well-defined orientation in arrays. However, the edge roughness sets limits on $\alpha = 0.2$ eV·nm and the width is restricted to $w > 10$ nm [55]. Moreover, ribbons thermally exfoliated from graphite and sonicated enabled $w \sim 2$ nm [56]. In addition, these ribbons had significantly smoother edges. Consequently, for $\alpha = 0.8$ eV·nm, a large $E_g \sim 0.4$ eV and an I_{ON}/I_{OFF} ratio $\sim 10^6$ at room temperature were demonstrated. The disadvantages include random positions, directions and no control of ribbon sizes. Similarly, isolated sub-nanometre ribbons with perfect edges have been fabricated by self-assembly [57]. However, without the possibility for array fabrication, they are useless for microwave transistors.

Second, *breaking bilayer graphene symmetry* opens a bandgap [58]. Different amounts of carriers are introduced in the two layers from the top and bottom sides of the bilayer. Preferably for applications, double-gated FETs have been used to introduce a tuneable bandgap [59]. A gap up to 0.25 eV [58] and an on-off ratio ~ 100 at room temperature [59] was achieved using combined top and backgates. Another option is the use of substrates with built-in fields, such as SiC [60] or ferroelectric $LiNbO_3$ [Paper H].

However, the mobility in graphene severely degrades as a sizeable bandgap is opened, following the same trend as for conventional semiconductors [17]. The highest mobilities reported at room temperature for 20 nm and 50 nm wide graphene nanoribbons are 2,000 cm^2/Vs and 3,000 cm^2/Vs, suspended [61] and on substrate [62], respectively. In the same way for bilayer graphene, the intrinsic mobility is severely degraded by the re-shaped bandstructure to $\sim 10,000$ cm^2/Vs at a sizeable bandgap necessary for applications [63].

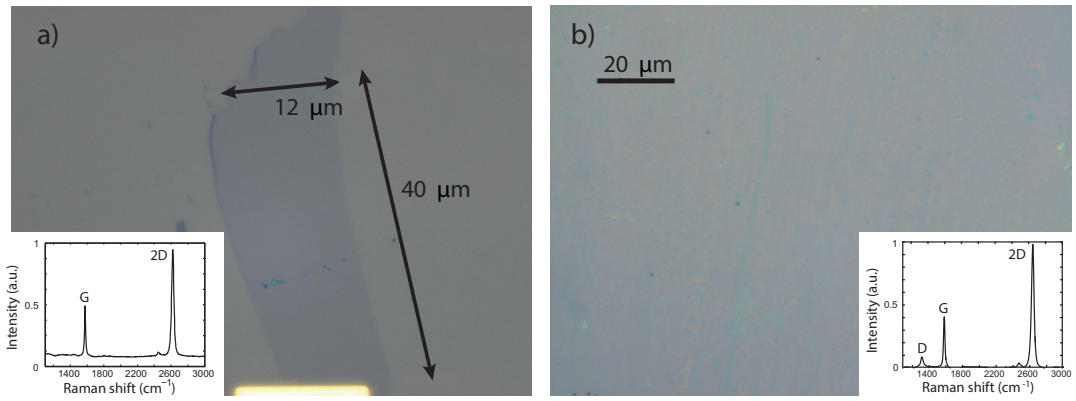

Fig. 2.4: Optical identification of single-layer graphene on SiO_2/Si substrate by a) exfoliation and b) CVD growth on Cu catalyst in a virtually hole-free area. The insets show the respective Raman signature characteristic of monolayer graphene.

2.3 Practical status of graphene synthesis

The term graphene has different meanings depending on the intended application, e.g., in terms of number of layers, electronic quality or visual transparency. This subsection describes the graphene synthesis methods relevant within the scope of this thesis. It concludes with the motivation and implications of the graphene used for the device and circuit demonstrators herein.

2.3.1 Exfoliation from highly ordered graphite

Mechanical exfoliation provides graphene of highest quality for fundamental research, whereas liquid phase exfoliation provides inexpensive graphene in large quantities for low-cost and low-performance applications.

The Scotch tape method, i.e., peeling off single layers from bulk graphite, was first demonstrated systematically in 2004 [22]. It still produces the highest mobility and lowest defect density graphene. The best mobilities both in suspended samples at $T = 240$ K of ∼100,000 cm^2/Vs [40] and at 5 K of 1,000,000 cm^2/Vs [52] as well as on substrate (hexagonal boron nitride) at $T = 230$ K of ∼100,000 cm^2/Vs [49] and at 4 K of ∼140,000 cm^2/Vs [49] use mechanically exfoliated material at a carrier density of 10^{11} cm^{-2}. Translated to a mean free path, this means micrometre-scale ballistic transport. The GFETs in [Paper D] and [Paper E] are fabricated on exfoliated graphene. A flake made by mechanical exfoliation of is shown in Fig. 2.4a).

On the other end of the scale, mass exfoliation from graphite flakes in liquids by sonication or shear-mixing produces few-layer graphene flakes suitable for inkjet printing [64]. The resulting graphene is multi-flake but could reach acceptable sheet resistance for certain applications and mobility comparable to metal oxide semiconductors such as IGZO for flexible active devices.

2.3.2 Graphene and h-BN synthesis by CVD

The possibility of growing thin graphitic films by CVD on different metal surfaces has been long explored. The development led to the currently most

promising technique for the CVD growth of single-layer graphene, which is on Cu foils [29]. Graphene is formed on Cu mainly by the surface-catalysed decomposition of a methane precursor, given the extremely low carbon solubility in Cu [65]. Once a layer of graphene covers the surface, the catalytic effect ceases, which results in a growth closely self-limited to a single layer. Indeed, up to 95% of the grown material can be controlled to be monolayer.

In this thesis, graphene was grown on 50 μm thick and 99.995+ % purity Cu foil in a cold-wall CVD system (Black Magic, AIXTRON), based on the recipe by Sun et al. [66]. The foils are pre-cleaned in acetone, isopropanol and acetic acid to remove organic contaminants and native oxides. The copper is annealed *in situ* for 5 min in 20 sccm H_2 and 1,000 sccm Ar $\sim 1,000\,^{\circ}$C. In addition to having a reductive effect on remaining oxygen, this increases the grain size of the Cu, thus improving the domain size of the grown graphene. Finally, the carbon precursor gas, 30 sccm methane (CH_4) diluted to 5% in Ar, is introduced. After 5-10 min, while maintaining a temperature $\sim 1,000\,^{\circ}$C, the methane gas is turned off and the catalyst is cooled to room temperature.

The major drawbacks of the in-house CVD growth reactor are the poor temperature control and uniformity over the copper surface [67]. Uncontrolled growth temperature and excess particle contamination in the system lead to variations of the graphene nucleation density. The resulting films consist of many small, coalesced graphene domains ($\lesssim 5$ μm) with different orientations (Fig. 2.5). Between the domains, the grain boundaries act as line defects that increase the carrier scattering and deteriorate the graphene mobility. Nevertheless, the Raman spectra of the in-house CVD graphene in a low-doped area [Paper H] is comparable to the exfoliated samples. Consequently, the CVD graphene exhibits $I_{2D}/I_G \sim 2$, an FWHM of the 2D peak ~ 35 cm^{-1} and only a small D peak $I_D/I_G \sim 0.2$, as shown in Fig. 2.4b).

Recently, tremendous efforts have been undertaken by many research groups to reduce the nucleation density and grow large single-domain graphene crystals. These include optimisation of the methane partial pressure [68], pre-growth polishing of the Cu foil to remove defects and grain boundaries which act as nucleation centres [69], non-reducing pre-annealing conditions to reduce the graphene nucleation by remaining copper oxide [70] and even intentional passivation with oxygen [71]. Altogether, centimetre-scale isolated and randomly positioned grains have been achieved with an order of magnitude better mobility. The growth time, however, is inherently longer due to the low carbon source supply and can be up to several days. Notably, for continuous films suitable for device applications, the largest grain size reported is ~ 1 mm [46].

Graphene and atomically flat hexagonal boron nitride should be considered as a system and preferably be synthesised *in situ* by CVD at the wafer scale. Recently, it has been shown that single-domain CVD graphene on exfoliated h-BN can reach mobilities on the same order as exfoliated samples [42]. However, the CVD growth of h-BN on metal catalysts or catalyst-free graphene growth directly on h-BN is much less mature, with limited domain size and poor layer control [72]. Different experimental conditions have been explored, including wet layer-by-layer transfer of CVD graphene from Cu foil onto CVD h-BN from Fe foil [73], CVD growth of nanometre graphene flakes onto exfoliated h-BN [74] and sequential growth of CVD graphene onto CVD h-BN on Cu [75]. None of the above are repeatable processes at the wafer scale.

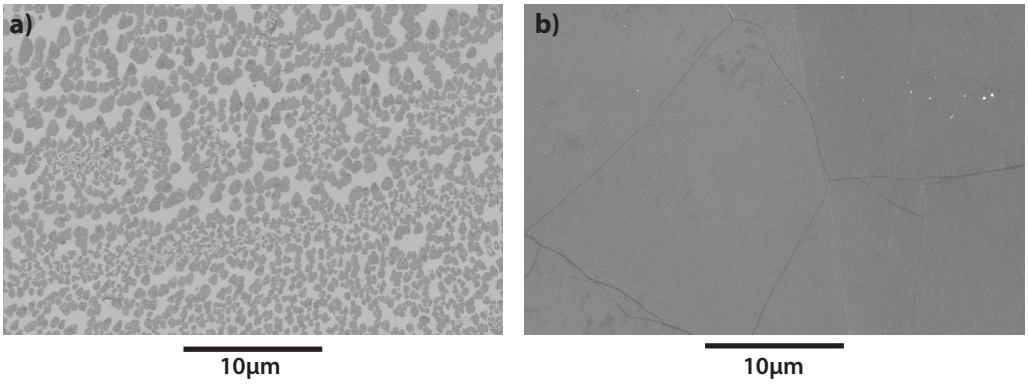

Fig. 2.5: SEM images of as-synthesised in-house CVD graphene on Cu foil that demonstrates a) the high nucleation density on a partially covered sample and in b) mutually rotated graphene domains on a continuously grown sample.

2.3.3 Transfer of CVD materials to insulating substrates

For material characterisation and device fabrication, the CVD graphene must be moved to an electrically insulating substrate. Commonly, a temporary PMMA resist film is spun onto the graphene surface, whereas the copper is etched away [66] or separated by the H_2 bubbling process [76], the method of choice in this thesis. Utilising a semi-rigid plastic frame reduces the occurrences of wrinkles and holes while facilitating convenient handling. The resulting transferred graphene to SiO_2/Si is presented in Fig. 2.4b). Simultaneously, the transfer is a major drawback of the CVD graphene. A severe transfer-related issue is the extrinsic reduction of mobility from PMMA residuals and water trapped at the graphene substrate interface. The water molecules act as acceptors, sometimes resulting in strong and unrepeatable p-type films. For high-temperature, post-transfer annealing to be effective in removing such contaminations and improving the electric quality of graphene, large-scale h-BN supports are required [28]. In addition, dry transfer of CVD graphene has been demonstrated using van der Waals forces on the scale of h-BN flake sizes [42] and at the large wafer scale using thermal release tape [25].

2.3.4 Sublimation and CVD growth on SiC

Graphene can be grown on SiC substrates either by thermal sublimation of Si from the surface at high temperature or by CVD from a gaseous precursor. A main advantage is that direct growth of graphene on a semi-insulating substrate is possible, without the need for transfer processes.

Sublimation from the *Si-face* of SiC can be relatively well controlled; both monolayer and Bernal stacked bilayer are feasible [77]. The first attempts at vacuum at $T \sim 1,200\,^{\circ}\mathrm{C}$ resulted in small flakes and a rough sample surface. Later, it was found that the presence of an inert gas, typically 1 atm Ar [77], limits the Si desorption rate and allows growth temperatures up to $2,000\,^{\circ}\mathrm{C}$. The different growth kinetics result in a smoother surface covered by larger area domains. Room temperature mobility values of Si-face sublimated graphene are limited by low-energy phonons to below $1,000$ cm^2/Vs at an electron concentration of $\sim 10^{13}$ cm^{-2}. This mobility is enhanced by

hydrogen intercalation, effectively decoupling the graphene from the substrate to make it quasi-free-standing, to 3,000 cm^2/Vs [78].

Recently, the CVD growth on the *Si-face* of SiC including *in situ* hydrogen intercalation was reported for synthesis of both monolayer [47] and bilayer [60] graphene. The obtained hole concentration was shown to closely match that induced by the spontaneous polarisation of the SiC substrate, indicating the high quality of the films. Accordingly, the mobilities reach 6,000 cm^2/Vs as measured over 10×10 mm^2 areas. Due to the pre-growth surface annealing step used in both the sublimation and CVD methods, step bunching on the SiC surface occurs. Terraces of 5-10 μm width form where the grown graphene is mono- or bilayer, depending on the recipe, whereas on the 5-10 nm steps separating the terraces, an additional layer forms. Smaller terrace widths and step heights and higher mobilities occur closer to the SiC wafer centre, indicating the importance of a high-quality starting material [47].

Controlling the sublimation rate of silicon from the *C-face* of SiC is more challenging, and stacks of mutually rotated, decoupled monolayers are formed. Nevertheless, the C-face epitaxial graphene displays up to several times higher mobility than the Si-face [79], as a result of a different interface structure, proving its potential for high-frequency electronics.

2.3.5 Which type of graphene and why?

Considering applications of graphene, the described large-volume production methods can be divided as suitable either for high-performance electronics in which a higher cost is acceptable or for mass deployment in medium-performance applications where a lower cost is necessary. In both cases, bilayer graphene is desirable for electronics because it allows a bandgap to be opened.

The graphene on SiC belongs to the first category. Directly synthesised on a semi-insulating substrate, it is mainly well suited for RF electronics and resistance standards [80]. Moreover, the growth of bilayer graphene is well controlled, and a bandgap may be induced in this material for free due to the spontaneous polarisation of the SiC substrate.

The CVD graphene has prospects mostly for the second category. The transfer of CVD graphene is both a major advantage in terms of versatility, in that it can be transferred from the catalyst to any host substrate in principle, and a quality and reproducibility issue at the same time. The transfer allows for applications in transparent conductors [25] and as a ubiquitous platform for flexible active devices on plastics [27]. In addition, CVD graphene can potentially be integrated into standard CMOS processes, in the back-end-of-line after careful consideration of the temperature budget and metal cross-contamination from etched Cu foil residuals [30]. However, the growth of continuous AB-stacked bilayer graphene by CVD is not yet achieved. Some efforts utilise the catalytic effect of Cu in a region spatially separated from the growth region [70]. Bilayer crystals with mobility of $\sim$20,000 cm^2/Vs and a bandgap opened by a vertical field have been grown on the outside of a Cu foil enclosure, using carbon diffused from the catalytically active inner surface [81].

Printed graphene from flakes exfoliated in liquid may complement CVD graphene in interconnects and transparent conductors where a higher sheet resistance is acceptable to make a universal electronics platform.

In summary, the applicability of CVD graphene to different substrates best enables the exploitation of the unique properties of graphene as a material for the opening of new niche applications. Furthermore, to conform with utility in applications, continuous CVD graphene is used throughout this thesis, despite its lower mobility $< 2,000\ \mathrm{cm}^2/\mathrm{Vs}$ [66]. A condensed summary of the synthesis methods discussed is given in Table 2.3. For graphene to ever compete with III-V high-speed devices, a major breakthrough in the synthesis of h-BN and large-domain bilayer graphene heterostructures at the wafer scale is necessary.

Table 2.3: Comparative summary of graphene growth methods and associated properties relevant to applications. The mobility values are for supported graphene on the following substrates and at room temperature: [1)] SiO_2/Si and [2)] h-BN. For the CVD growth on Cu foil, [†] isolated single crystals and [‡] coalesced continuous film.

	Scalability limit	Layer control	Domain size	Mobility $(\mathrm{cm}^2/\mathrm{Vs})$	Cost	Versatility
Mechanical exfoliation [49]	Graphite grains	Poor	< 1 mm	20,000[1)]-100,000[2)]	High	Research
CVD[†] on Cu-foil [71]	Domain size	Good ($\leq$ 1L)	< 50 mm	10,000[1)]-30,000[2)]	High	Medium
CVD[‡] on Cu-foil [46]	Reactor dimensions	Good ($\leq$ 1L)	< 1 mm	$< 6,000$[1)]	Medium	High
Sublimation Si-face [78]	SiC wafers < 6 inch	Good ($\leq$ 2L)	$< 10\ \mu$m	$< 3,000$	High	Low
CVD on SI SiC [47]	SiC wafers < 6 inch	Good ($\leq$ 2L)	$< 10\ \mu$m	$< 6,000$	High	Low
Sublimation C-face [79]	SiC wafers < 6 inch	Poor	-	$< 30,000$	High	Low
Liquid exfoliation [64]	Ink-jet printer	Poor	$< 1\ \mu$m	< 100	Low	Medium

Chapter 3

Fabrication, device-level characterisation and modelling of GFETs

This chapter discusses the operation principles, performance indicators and modelling of GFETs in active amplifiers and passive detectors and mixers. To design GFET-based circuits, characterisation and model development at the device level are necessary. This thesis contributes a small-signal analysis of passive GFET power detectors in [Paper A]. The large-signal model proposed in [82] is used to design and analyse resistive GFET mixers in [Paper C] and [Paper D]. In addition, active GFETs used for amplification are distinguished by their small-signal gain and noise figure, which are the topics of [Paper F].

3.1 Device fabrication

The measurement frequency and characterisation environment dictate whether the device is laid out with coplanar pads for on-wafer access or an antenna for free-space characterisation. However, the fabrication flow is analogous in both cases. Subsequent to graphene growth and transfer, an electron beam lithography-based process is used to fabricate test structures and GFETs. The general steps are illustrated in Fig. 3.1 and motivated by references below. All detailed process parameters are listed in Appendix A.

- **Mesa- and nanoconstriction etching in O_2 plasma** at 50 W RF power and 50 mTorr pressure for 6 s using a negative resist mask. This step provides device isolation and improves the current on-off ratio [83].
- **Ohmic contacts (1 nm Ti/15 nm Pd/100 nm Au)** are formed by evaporation and lift-off. The thin Ti is used as an adhesion layer, whereas low contact resistance is assured by the Pd layer [84, 85].
- **Annealing in Ar ambient at 230 °C for 15 min** which helps to remove residual PMMA in the channel region [86] and reduces the contact resistance for chemisorbed metals on graphene such as Pd [87].

- **Atomic layer deposition (ALD) at 300 °C for 15 nm Al_2O_3** of top-gate oxide. Prior to the ALD deposition, a seed layer of 4×1.5 nm in thickness is formed by natural oxidation of evaporated Al [50].
- **Gate fingers with 100 nm access gaps** are patterned and metallised with 10 nm Ti/300 nm Au or 250 nm Al/10 nm Ti/50 nm Au.
- **Coplanar pads or antennas (10 nm Ti/300 nm Au)** overlapping the ohmic metal are formed on the SiO_2 surface by evaporation. First, the Al_2O_3 is etched in buffered oxide etch, with the Au as the etch stop. Coplanar access and antenna-coupled GFETs are shown in Fig. 3.2.

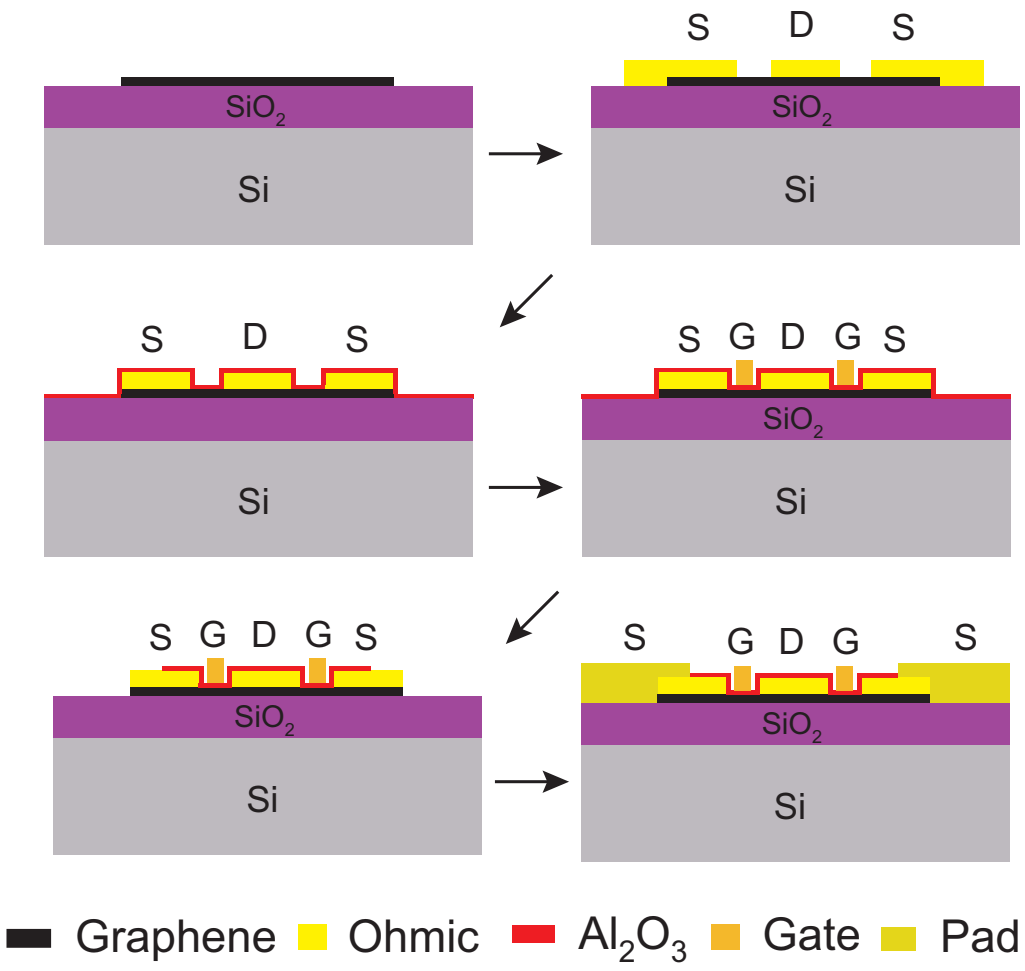

Fig. 3.1: Schematics of the fabrication steps for a two-finger GFET.

3.2 DC characterisation of GFETs

To realise high-performance FETs, it is important to fabricate high-quality ohmic contacts and graphene with low sheet resistance. Extraction of mobility and contact resistance from DC measurements is thus important for both yield analysis and models to predict the RF performance of the devices. Most importantly, these parameters reflect directly on the transconductance.

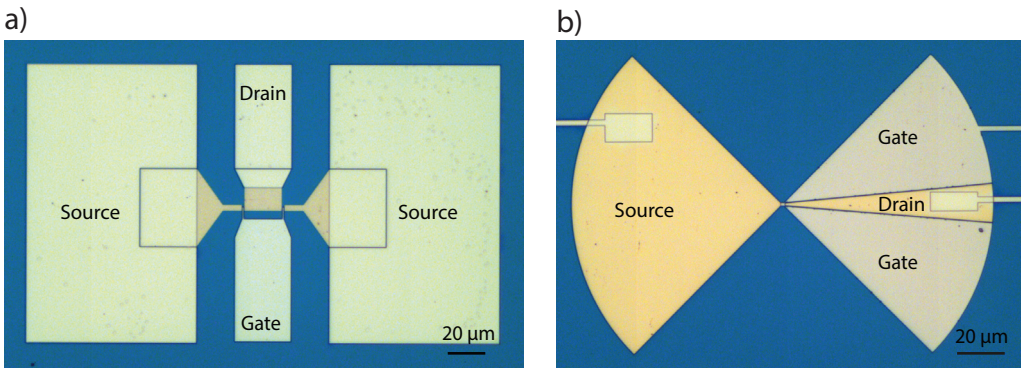

Fig. 3.2: Two finalised GFETs outlined with a) coplanar access pads for on-wafer characterisation and b) a broadband bow-tie antenna for free-space characterisation.

3.2.1 Ohmic contacts to graphene

The parasitic source and drain resistances in a symmetric FET layout are equal and may be expressed as a sum of the interface resistance and the access resistance, $R_S = R_D = (R_cW + R_{sh}L_a)/W_g$, where R_cW is the metal-graphene contact resistance, R_{sh} is the sheet resistance, L_a is the access gap length, and W_g is the gate width. Achieving a good ohmic contact to graphene has been the subject of extensive study, and the mechanisms have been gradually clarified.

- Early work focused on the "side-contact" geometry, i.e., a picture in which the deposited metal is thought to lie on the graphene surface. The low contact resistivity with high work function metals such as Pd [84] and Ni [88] was attributed to charge transfer and resulting DOS enhancement [43]. For this type of contact, a clean interface is required [89]. This was achieved in this work using an e-beam resist process.

- On this line, a high starting carrier concentration in the graphene is most effective, which was proved by gating to be independent of the carrier sign [84]. This is an inherent property in epitaxially grown graphene, where low contact resistances have been repeatedly reported [90]. However, selective doping of graphene is desired to produce a device structure similar to the use of cap layers in HEMTs [44].

- Recent studies elucidated the advantage of using a chemisorbed metal contact on graphene in an "edge-contact" geometry [41]. Metals such as Ni, Pd and Ti chemisorb on graphene [43] and bind particularly strongly to reactive sites such as graphene edges. The edges can be formed in graphene defected by O_2-plasma ashing [91] or metal-catalysed etching [88] or in a controlled manner by lithographic patterning [92, 93]. In fact, spontaneous end-contact formation after deposition of chemisorbed metals on CVD graphene was reported [85], which could be further enhanced after annealing [87].

In this work, a large variability of contact resistances within batches has been observed. A large dataset of two-probe contact resistances to CVD graphene is summarised in Fig. 3.3, yielding a mean $R_cW \sim 600\ \Omega\mu m$.

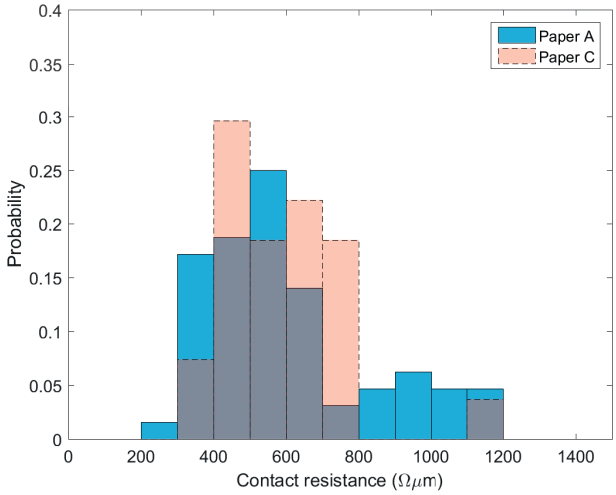

Fig. 3.3: Two-probe contact resistance extracted with Eq. 2.4. The distribution is for ∼100 GFETs from batches fabricated in the process of [Paper A] and [Paper C].

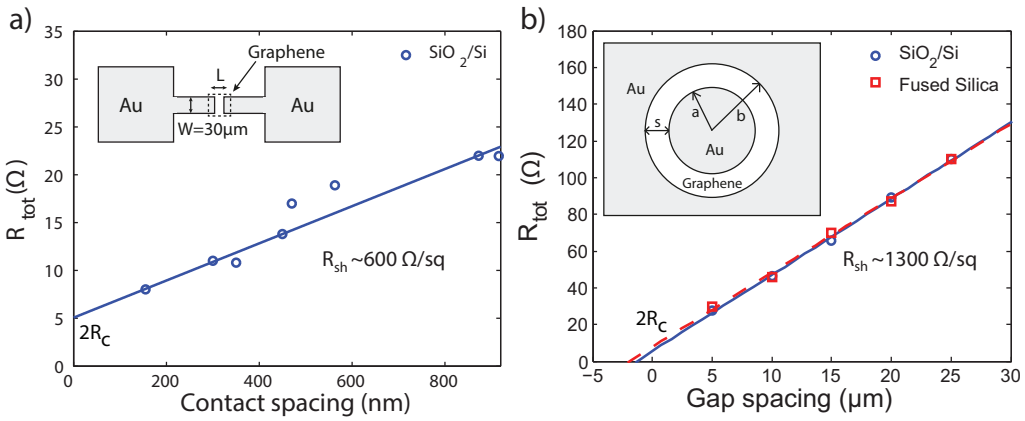

Fig. 3.4: TLM results for CVD graphene on SiO_2/Si substrates with a) Pd based contact which gives $R_cW = 80\ \Omega\mu$m [Paper F] and b) Ti metallised contact with $R_cW = 900\ \Omega\mu$m [Paper G]. The insets illustrate the TLM structure layouts.

Better accuracy is obtained within the four-probe transmission line method (TLM) measurements. Using this extrapolation approach, which is illustrated in Fig. 3.4, resistivities for the contacts reach the state of the art; $<100\ \Omega\mu m$ with Pd metallisation [Paper F] and $900\ \Omega\mu m$ with Ti metallisation [Paper G] were reported, respectively. As discussed above, a combination of high carrier concentration and edge-contact formation is the likely explanation for the low value in [Paper F]. An accurate determination of a small R_cW with a large R_{sh} and an inhomogeneous material becomes a delicate task [89]. Consequently, the TLM layout was designed as shown in the inset of Fig. 3.4a) to have small resistance, $R_{tot} = 2R_c + R_{sh}L/W$. In addition, the narrow contact spacings were measured with SEM.

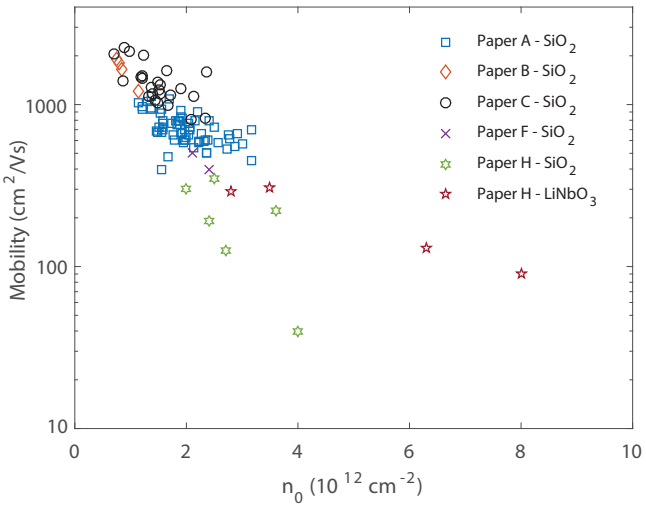

Fig. 3.5: Compilation of hole mobilities versus the residual concentrations extracted from fitting of Eq. 2.4 using top gates. All devices were fabricated on CVD graphene in different batches during the work on the papers appended to this thesis.

3.2.2 Channel mobility and sheet resistance

The mobility values reproduced in Table 2.3 are measured for graphene on a substrate. However, in current GFET structures with top gates, the graphene is usually sandwiched between *two* oxide interfaces, as shown in Fig. 3.1. The seeded ALD deposition of Al_2O_3 used herein has been shown to preserve the mobility well in exfoliated graphene [50]. Extending the results in [Paper H], a larger collection of mobilities and residual carrier concentrations extracted from least squares fitting to Eq. 2.4 are shown in Fig. 3.5. According to [38], all of these CVD samples are considered to be "dirty" (with high impurity concentration n_{imp}), compared with the exfoliated samples in [Paper D] and [Paper E] with $n_0 \sim 5 \cdot 10^{11}$ cm^{-2}, which are relatively "clean". Building on the analysis in [Paper H], one reason for the variation is an irregular Al_2O_3 dielectric quality, most likely exacerbated by the requirement for a seed layer.

In addition to active devices calling for high mobilities, passive components as transparent electrodes [25] and antennas [Paper I] are also considered. These require only to minimise the graphene sheet resistance, $R_{sh} = (qn\mu)^{-1}$. The combination of low sheet resistance and high transparency together with the variety of envisioned substrates necessitates CVD graphene. Typical values for sheet resistance in this work are 0.5 - 1 kΩ/sq, from the TLM graphs in Fig. 3.4. Attempts to further reduce the sheet resistance used surface-functionalised multilayer CVD graphene. However, the reproducibility and stability of chemical treatments are questionable. The most promising route is the $FeCl_3$ intercalation process. The competitiveness of graphene to ITO is summarised in Table 3.1. Typical application requirements are 10-100 Ω/sq for transparent electrodes [25]. This means that graphene is practically viable for transparent conductors in touchscreens, where it can replace the expensive, rare and brittle indium tin oxide (ITO) currently used. Graphene for antennas is further discussed in Section 4.6.

Table 3.1: R_{sh} and T for graphene versus # layers and chemical treatment. [a] Layer-by-layer transfer, Cu catalyst. [b] Intercalated, Cu-Ni catalyst.

# layers	Treatment	R_{sh} (Ω/sq)	T (%)	Removal	Ref.
1 - 4[a]	PMMA	130 - 40	97 - 90	-	[25]
1 - 4[a]	HNO_3	110 - 30	97 - 90	Desorbs in air	[25]
1 - 4[a]	$FeCl_3$	95 - 55	-	H_2O adsorption	[94]
2 - 4[b]	$FeCl_3$	400 - 20	95 - 90	Stable in air	[95]
ITO	-	100/10/2	90/85/80	-	-

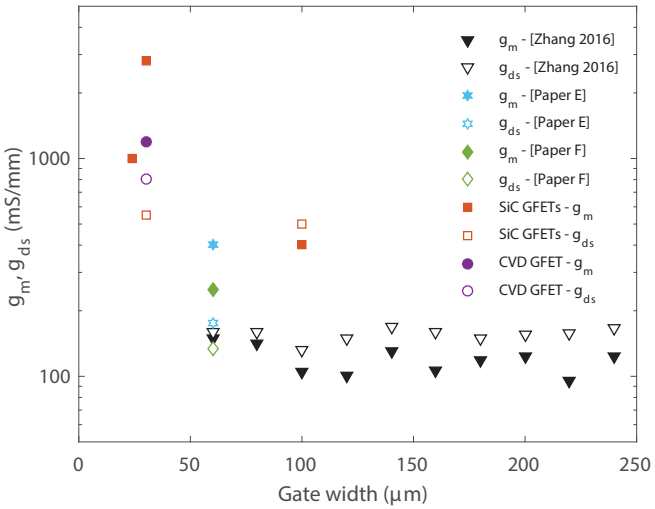

Fig. 3.6: Extrinsic transconductance and output conductance of the CVD GFETs in [96], [Paper F] and the exfoliated GFET [Paper E]. For comparison, the reported values for ultrathin gate oxide SiC [21, 97, 98] and CVD [99] GFETs are given.

3.2.3 Transconductance and output conductance

The extrinsic transconductance, $g_{me} = dI_{ds}/dV_{gs}$, and output conductance, $g_{de} = dI_{ds}/dV_{ds}$, provide a connection between the DC and RF performance of an FET through the low frequency small-signal gain

$$|S_{21}| = \frac{2Z_0 g_{me}}{1 + Z_0 g_{de}}. \tag{3.1}$$

An overview of the devices used in the fabricated amplifiers in this thesis is given in Fig. 3.6. Scaling the gate width, higher gain can be achieved by the increased g_{me}, but the effect is diminished by the simultaneous increase of g_{de}. Extreme scaling of the gate oxide thickness at gate lengths $\leq$ 250 nm, good mobility in SiC graphene and low contact resistances are responsible for the impressive transconductances in the SiC GFETs. These normalised transconductances are even higher than for GaAs and InP HEMTs [44]. However, the related low on-resistance together with the lack of current saturation yields higher g_{de} in the SiC graphene devices relative to III-V devices.

3.3 Small-signal equivalent FET circuit

The starting point to understand all models discussed hereafter is the linear small-signal equivalent FET circuit shown in Fig. 3.7. The circuit consists of two parts, the parasitics associated with the measurement pads and the intrinsic elements describing the behaviour of the device itself. Naturally, the parasitics are bias independent, whereas the intrinsic elements must be extracted at the DC bias point of interest depending on the application. The model predicts the response of the FET to a sinusoidal input signal at a certain frequency and with an amplitude small enough not to disturb the DC bias value. Consequently, the small-signal equivalent circuit can be applied directly to the modelling of active FETs in low-noise amplifiers ($V_{ds} \neq 0$ V). Furthermore, it provides the foundation for the extended large-signal circuit needed to model passive FETs in detectors and mixers ($V_{ds} \equiv 0$ V) as discussed in Section 3.6. The circuit elements are found according to the following procedures.

- The pad capacitances, resistances and inductances are extracted from the S-parameters of open and short structures excluding the graphene channel in a manner similar to standard cold-FET measurements [100].
- The series resistances R_S and R_D are determined from DC measurements on separate TLM test structures, which are described in Section 3.2.1.
- The gate resistance R_G is found by DC end-to-end measurements [44]. For the GFETs with $L_g = 1$ μm and Au or Al gate, it is $\sim$50 Ω/mm.
- The parasitics are de-embedded [101] from the measured GFET S-parameter matrix at the chosen DC bias point [102], and a closed-form and direct extraction of the intrinsic component values is performed [103].

Finally, a post-optimisation of the S-parameter fit is performed. The final S-parameter fits of one passive and one active GFET are shown in Fig. 3.8.

3.4 Graphene for active microwave FETs

This section introduces the high frequency figures of merit of microwave FETs and relates them to the equivalent small-signal circuit. The frequency limits of the current GFET technology are benchmarked within this framework.

3.4.1 Figures of merit for active FET two-ports

The upper frequency limits of active microwave FETs are benchmarked via the cutoff frequency (f_T) and the maximum frequency of oscillation (f_{max}) which can be derived from measured S-parameters at a chosen DC bias [44]. The cutoff frequency is where the short-circuit current gain, $|h_{21}|$, equals unity

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}. \tag{3.2}$$

In a similar manner, the maximum frequency of oscillation is found when the Mason gain [104] or unilateral power gain, U, is unity where

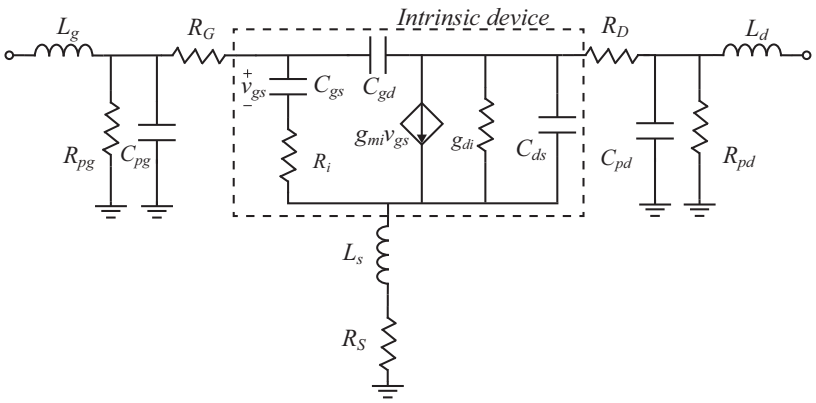

Fig. 3.7: The linear small-signal equivalent circuit of an FET, which is divided into DC-bias-independent parasitics and DC-bias-dependent intrinsic elements.

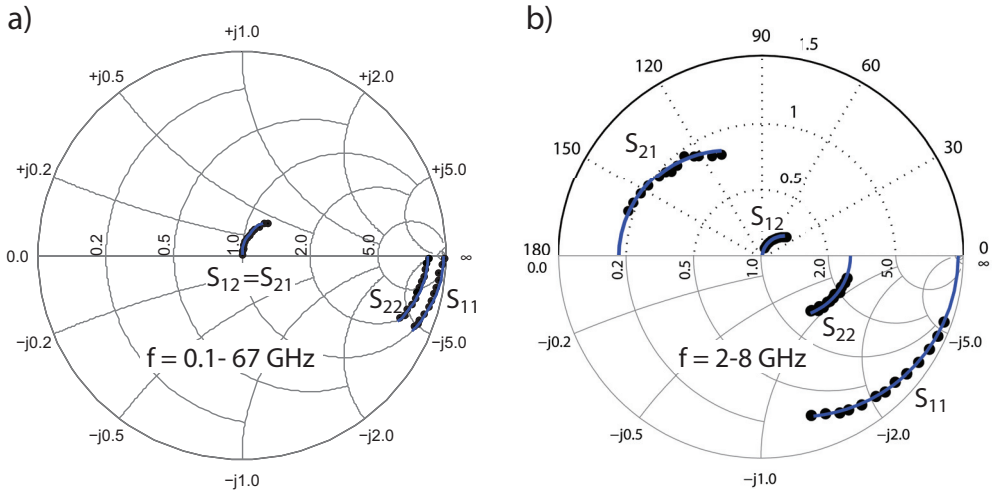

Fig. 3.8: The S-parameters of a) passive GFET, which is reciprocal ($S_{12} = S_{21}$) with $L_g = 1$ μm and $W_g = 2 \times 1.25$ μm [Paper A], and b) active GFET, which has forward gain ($S_{21} > 1$) with $L_g = 1$ μm and $W_g = 2 \times 60$ μm [Paper F].

$$U = \frac{|S_{12} - S_{21}|^2}{det(\mathbf{I} - \mathbf{SS}^*)}. \tag{3.3}$$

Useful expressions for the optimisation of f_T and f_{max} are derived from the small-signal equivalent circuit of an FET as shown in Fig. 3.7:

$$f_T = \frac{g_{mi}}{2\pi} \frac{1}{(C_{gs} + C_{gd})(1 + g_{di}(R_D + R_S)) + C_{gd} g_{mi}(R_D + R_S) + C_{pg}} \tag{3.4}$$

and (excluding pad capacitances and inductances from the analysis)

$$f_{max} = \frac{g_{mi}}{2\pi(C_{gs} + C_{gd})} \frac{1}{2\sqrt{g_{di}(R_i + R_S + R_G) + g_{mi} R_G \frac{C_{gd}}{C_{gs}+C_{gd}}}}. \tag{3.5}$$

Table 3.2: Extrinsic versus pad de-embedded and intrinsic f_T and f_{max} (GHz) of state-of-the-art GFETs in wafer-scale technologies. f_{max} from † U and ‡ MAG.

	$f_{T,ext}$	$f_{T,de}$	$f_{T,int}$	$f_{max,ext}$	$f_{max,de}$	$f_{max,int}$
Epitaxial† [19]	41	-	110	38	-	70
CVD† [27]	24	39	198	6.5	7.6	28
Epitaxial‡ [21]	44	107	407	41	60	120

The parameters extracted at DC now have direct bearing in this context. A high carrier mobility reflects on a large g_{mi}, which is the change in drain current with gate voltage, $g_{mi} = dI_{ds}/dV_{gs}$. Further inspection reveals the importance of minimising the parasitic resistances R_S, R_D and R_G of the source, drain and gate, respectively. The source and drain resistances constitute the transition resistance from metal to graphene and access resistance. They are technology specific and discussed in more detail in Section 3.2.1. The gate resistance, on the other hand, is simply the geometrical resistance of a metal stack after accounting for small-signal conditions, $R_G = R_{G,DC}/3 = \rho_G \frac{W_g}{3L_g h_g}$ [44]. Here, L_g (W_g) is the gate length (width), and ρ_G is the resistivity of the gate metal. Similar to mature FET technologies, it can be kept low even for short gate lengths by the use of mushroom gates [44], not required at $L_g = 1$ μm.

As a final remark, the contact resistances act to degrade the extrinsic transconductance, g_{me}, and the extrinsic output conductance, g_{de}, measured at the GFET terminals compared with the intrinsic ones in Eq. 3.4 and Eq. 3.5. The gain capabilities of a device from a high mobility material with large intrinsic transconductance can thus be severely impaired by high contact resistances. Mathematically, this is expressed in the form [105]

$$g_{mi} = \frac{g_m^0}{\left(1 - (R_S + R_D) g_{de} (1 + R_S g_m^0)\right)} \tag{3.6}$$

and

$$g_{di} = \frac{g_d^0}{\left(1 - R_S g_{me} (1 + (R_S + R_D) g_d^0)\right)}, \tag{3.7}$$

where $g_m^0 = \frac{g_{me}}{1 - R_S g_{me}}$ and $g_d^0 = \frac{g_{de}}{1 - (R_S + R_D) g_{de}}$.

3.4.2 Benchmark of state-of-the-art active GFETs

From Fig. 1.1, the cutoff frequencies of GFETs seem to compare well with III-V HEMTs. The f_{max} values do not look as impressive, although an optimisation of R_G can improve the f_T/f_{max} ratio [19, 98]. Still, there is a fundamental limit due to the lack of a bandgap, which gives large g_{di} due to poor current saturation. However, the given cutoff frequencies in Fig. 1.1 for GFETs are the intrinsic values, $f_{T,int} = \frac{g_{mi}}{2\pi(C_{gs} + C_{gd})}$. The comparison of as-measured (extrinsic) and de-embedded (in the case of GFETs often the same as intrinsic) values in Table 3.2 displays a large deviation. This is explained by narrow devices resulting in a high ratio of parasitic gate pad capacitance to

intrinsic gate capacitance $C_{pg}/(C_{gs}+C_{gd})$ for short gate length devices. This is especially true for flakes on highly resistive Si substrates, which results in higher pad capacitance compared with semi-insulating III-V substrates [106]. Extracting a large value from a small one causes the de-embedding to be error prone. The highest extrinsic f_T of 40 - 50 GHz are thus realised on insulating glass [107] and SiC [19, 21, 98] substrates. In addition, for GFETs, R_S and R_D are often de-embedded in a questionable way using separate open and short structures without graphene (see Section 3.2.1; TLM measurements necessary). This is because cold-FET measurements [102] are not possible on a GFET as it has no distinct off state. In fact, the effect of the contact resistances is not removed for the de-embedded f_T of III-V HEMTs but is considered as a parasitic delay [12]. For GFETs in general and in particular, GFETs with small gate widths, this contribution can be prominent in boosting the intrinsic f_T, shown in Fig. 1.1 [27, 108]. This brings another factor of uncertainty into the comparison between GFETs and other technologies.

The short gate length GFETs with high intrinsic f_T exhibit no actual power gain even at low-GHz frequencies and a system impedance $Z_0 = 50\ \Omega$. The transistors fabricated in this thesis are designed to operate with small-signal power gains ($S_{21} > 1$) in the frequency region < 5 GHz. Consequently, a gate length $L_g = 1\ \mu$m was chosen to achieve efficient gate modulation of the drain current and thus a higher transconductance [97]. However, this means that the gate capacitance will be comparatively large. As such, the devices have f_T and f_{max} values ∼10 - 15 GHz from the as-measured S-parameters in [Paper E] and [Paper F]. Since these GFETs have gate widths $W_g \geq 60\ \mu$m, the intrinsic values are on the same order of magnitude as the extrinsic ones.

3.5 Quantifying the GFET noise performance

The noise figure (NF) is used to quantify the noise performance of microwave FETs. It is defined as the degradation in the signal-to-noise ratio from the input to the output of the device and must be low to design a sensitive receiver [109]. The noise figure relates to the equivalent noise temperature (T_n) referred to the device input as $NF = 1 + T_n/T_0$, where $T_0 = 290$ K. The FET noise figure depends on the source admittance presented at the gate port of the device [110] according to

$$NF(Y_s) = NF_{min} + \frac{R_n}{G_s} \cdot |Y_s - Y_{opt}|^2, \tag{3.8}$$

where NF_{min} is the minimum achievable noise figure used as a benchmark [44]. Furthermore, Y_{opt} is the optimum admittance for which NF_{min} is realised, and the noise resistance, R_n, describes the sensitivity of NF to mismatches when $Y_s \neq Y_{opt}$. Empirically, it has been noted that the design of low-noise FETs, to a high degree, mirrors that of high-f_T/f_{max} devices [111]. In particular, $T_{min} \approx \frac{f}{f_T}\sqrt{(R_S + R_G + R_i)T_g g_{di} T_d}$ where T_d and T_g are fitting factors [112]. Thus, high mobility and saturation velocity are prerequisites for low noise.

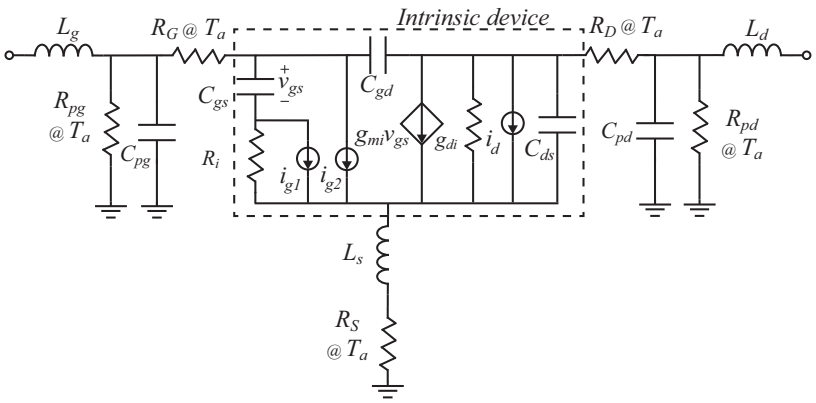

Fig. 3.9: Small-signal circuit for the GFET noise model at a given bias, with the Pospieszalski (i_{g1}, i_d) [113] and PRC (i_{g2}, i_d) [114] noise currents [Paper F].

3.5.1 Noise modelling of FETs

The most important sources of noise in microwave FETs are thermal noise from the resistive part of the channel and parasitic resistances and high-field diffusion noise from the velocity saturated part of the channel [44]. As such, the minimum noise figure typically displays an optimum value at a low drain current and decreases at cryogenic temperatures if scattering decreases. In the presence of a significant DC gate leakage current, the shot noise has to be considered as well, $\overline{i_{gs}^2} = 2qI_g\Delta f$. In this thesis, the Al_2O_3 gate oxide provides devices with $I_g < 1$ nA, which is a negligible level based on the current GFET noise performance. In certain applications, such as oscillators, $1/f$ noise with a corner frequency of ~ 100 kHz in graphene [115] is also important.

From a noise modelling point of view, one can consider the intrinsic FET as a two-port described by gate (input) and drain (output) noise sources. These are inserted in the intrinsic part of the standard FET small-signal circuit from Fig. 3.7. This is shown within the dashed rectangle in Fig. 3.9 for the two models considered, namely, the Pospieszalski [113] and PRC models [114].

- The PRC model has two model coefficients, namely, P for the drain noise current ($\overline{i_d^2}$) and R for the gate noise current ($\overline{i_g^2}$). The currents are correlated with the purely imaginary correlation coefficient C. The feedback capacitance C_{gd} is neglected in the analysis. This is a reasonable assumption since $\overline{i_{d,C_{gd}}^2} = \overline{i_d^2}\left(1 + \left(\frac{f}{f_0}\right)^2\right) \approx \overline{i_d^2}$, where $f_0 = g_{di}/2\pi C_{gd}$ [116].

- In the Pospieszalski model, equivalent temperatures are assigned to all dissipative elements in the intrinsic FET, i.e., T_g of R_i for the gate noise and T_d of R_{ds} for the drain noise. It is essentially equal to the PRC model provided $C = \sqrt{R/P}$, which was noted at an early stage [113].

Relationships between the model parameters and noise currents are given in Table 3.3. The parasitic resistances contribute thermal noise given the ambient temperature, $\overline{e^2} = 4k_BT_aR\Delta f$, in both models. The two models provide slightly different information on the noise performance of a particular device. The Pospieszalski model is "practical", while the PRC model is geared towards physics and the early work by van der Ziel on FET noise [117, 118].

Table 3.3: Definition of the FET noise currents shown in Fig. 3.9.

	$\overline{i_g^2}$	$\overline{i_d^2}$	C
Pospieszalski	$4k_B\Delta f T_g/R_i$	$4k_B\Delta f T_d g_{di}$	-
PRC	$4k_B T_a \omega^2 C_{gs}^2 R\Delta f/g_{mi}$	$4k_B T_a g_{mi} P\Delta f$	$j\frac{Im\left(\overline{i_g \cdot i_d^*}\right)}{\sqrt{\overline{i_g^2}\cdot\overline{i_d^2}}}$

3.5.2 Construction of a GFET noise model

The determination of all four GFET noise parameters is performed by measuring the noise figures for different source impedances (diverse Γ_S) and making a least-square fit to Eq. 3.8. On-wafer measurements were performed with an NP5 test set, an electronic tuner and the cold source method. The DUT noise temperature (T_n) is determined from the output noise power (P_{out}) by

$$T_n(\Gamma_S) = \frac{P_{out}(\Gamma_S)}{k_B G_{DUT}(\Gamma_S)\Delta f} - T_{in}, \tag{3.9}$$

where T_{in} is assumed to be equal to room temperature for all values of Γ_S. A network analyser independently determines the tuner states, receiver reflection coefficient and DUT S-parameters, which yields G_{DUT}. The receiver noise parameters are measured separately [119], making it possible to find P_{out}.

The NF_{min} in the 2 - 8 GHz range for a 2×30 μm device with $L_g = 1$ μm at $I_{ds} = 370$ mA/mm is shown in Fig. 3.10a). The noise resistance decreases from $\sim 300\Omega$ at 2 GHz to $\sim 200\Omega$ at 8 GHz [Paper F]. As a result of the high R_n, the $NF_{50\Omega}$ of $\sim 8 - 9$ dB is large. The fundamental conditions for the measured noise parameters derived from the correlation of noise sources in an FET, $|Cor| < 1$ and $\mathrm{Re}(Cor) > 0$ [113], are satisfied, as shown in Fig. 3.10b).

A knowledge of all four noise parameters allows for a systematic extraction of the model parameters in Section 3.5.1 once the small-signal circuit elements are known, as discussed in Section 3.3. The subsequent main steps in the noise model extraction and adequate references are listed below.

- Determine the chain noise correlation matrix at each frequency of the device from the measured noise parameters according to (11) in [120].
- De-embed the noise contribution of the parasitics using the admittance matrices derived from the circuit in Fig. 3.9 to find the intrinsic noise correlation matrix of the subcircuit within the dashed rectangle [121].
- Extract the noise model parameters from the intrinsic noise correlation matrix at each frequency point [122]. The result is shown in Fig. 3.11.

For comparison, the values of T_g and T_d in the Pospieszalski model were found by least-square optimisation to closed-form expressions for the intrinsic noise parameters following [113], after the inclusion of C_{gd}. The resulting values, $T_g = 700$ K and $T_d = 1950$ K, are close to the mean values from the direct extraction (which neglects C_{gd}), which are shown as lines in Fig. 3.11. The resulting model curves are shown on top of the measurement points in Fig. 3.10. The pad resistances are a main limiting factor of the GFETs, and

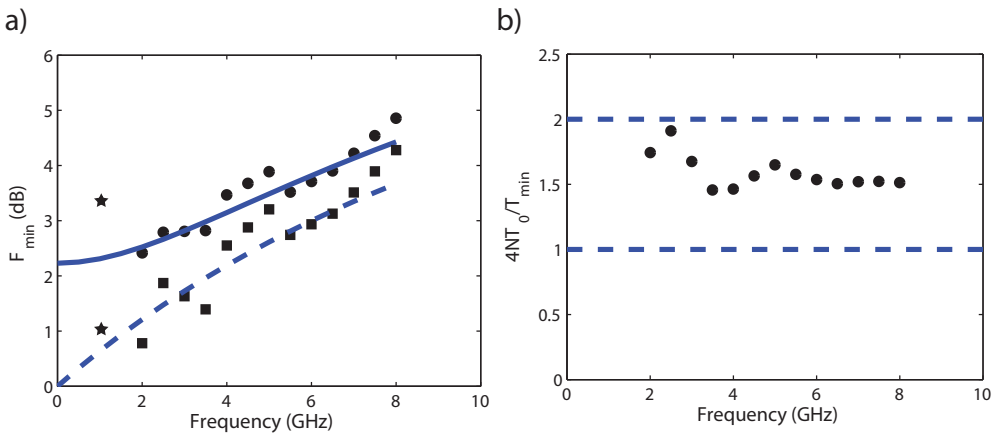

Fig. 3.10: a) Measured (•) and intrintsic (■) F_{min} of a 2×30 μm device at $I_{ds} = 370$ mA/mm [Paper F]. Values from [Paper E] given by ($\star$). b) The measured noise parameters fulfils the requirement that $1 < 4NT_0/T_{min} < 2$ [113].

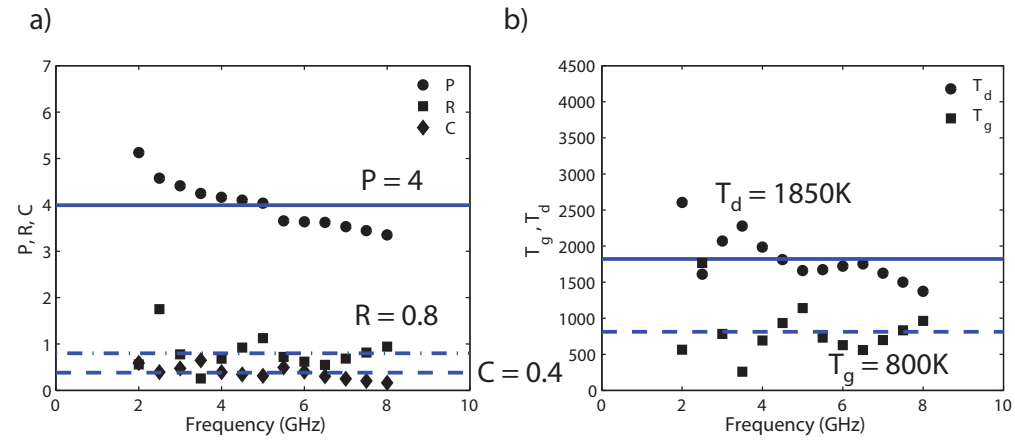

Fig. 3.11: a) Extracted P (•), R (■) and C (♦) coefficients of PRC model versus frequency. b) Extracted T_g (•) and T_d (■) of Pospieszalski model versus frequency. Lines and labels show mean values over all frequency points.

they result from the lossy substrate. Noise figures from < 1 dB to 2 GHz and from < 3 dB to 8 GHz appear feasible given the intrinsic device performance. In comparison, as observed from the extensive comparison shown in Fig. 3.12, InP HEMTs provide a room temperature $F_{min} < 1$ dB to ~ 90 GHz.

3.5.3 Prospects for GFET low-noise amplifiers

The impressive transconductance values in Fig. 3.6 bode well for GFET-based amplifiers. These numbers are partly a result of graphene's capability for high current densities. On the one hand, maximising the amplifier small-signal gain and f_{max} by using a high drain current only comes at the expense of high DC power consumption. On the other hand, the requirement of a high drain current to achieve power gain raises concerns regarding the fundamental limits on the noise levels in GFET amplifiers. For instance in [Paper F], the gate bias used is for the highest gain required to measure the noise with the highest accuracy, whereas an optimum noise level likely occurs at lower drain currents. This is indicated by the $T_{min}/f/L_g$ (K/GHz/μm) data in [Paper F].

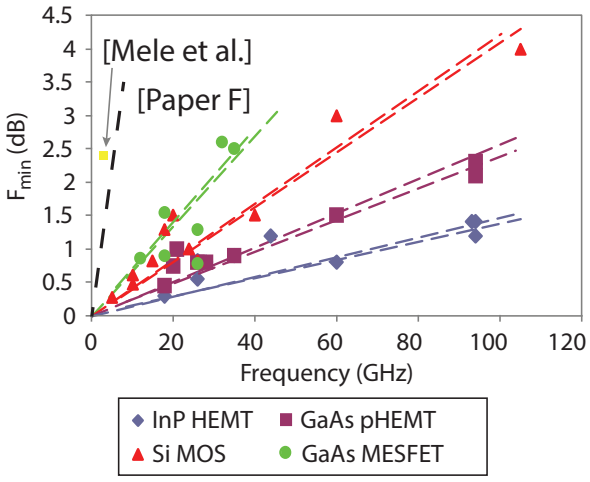

Fig. 3.12: Intrinsic F_{min} of the GFET with $L_g = 1$ μm [Paper F] compared with Si and III-V technologies [123], and the SiC GFET result for a $L_g = 150$ nm device [124].

Pospieszalski highlighted the importance of the "quality of pinch off" [112] for low-noise performance. To elaborate on this, in Table 3.4, the expression for the FET minimum noise temperature from Section 3.5 is divided into two parts, both of which must be minimised. These are the bias-dependent intrinsic part, represented by $\sqrt{I_{ds}/g_{me}}$, and the parasitic resistors, R_S and R_G. Seemingly, bridging the factor-of-two mobility gap to GaAs pHEMT could make SiC GFETs competitive. Nevertheless, the latest GFET LNA noise figure of 6 dB at 14 GHz [125] is out-of-scale in Fig. 3.12. In addition, there is a striking difference in the CMOS performance when the figures of merit in Table 3.4 are compared to the slope of the minimum noise figure plot in Fig. 3.12. Clearly, the numbers in Table 3.4 are only part of the story.

Moreover, when normalised to the gate length, the GFET noise is comparable to that in recent Si CMOS nodes [126]. However, the lower f_T of GFETs currently prohibits them from reaching the same noise figures as CMOS devices. A similarity between the noise performance of the oxide-gated MOSFETs [123] and GFETs [Paper F] is the poor correlation factor for the gate and drain noise. The substraction of the gate noise from the drain noise contributes to the outstanding low noise performance of HEMTs, despite the resemblance to CMOS in Table 3.4. This is expressed as a correlation factor that is close to unity in the PRC model, $C > 0.9$ [116]. Therefore, the poor noise correlation can be a fundamental drawback of the GFET structure.

Another study on an SiC GFET with $L_g = 150$ nm reported a similar $F_{min} = 2.4$ dB at 3 GHz that was extracted from $NF_{50\Omega}$ measurements [124]. This value is very close to that observed in the measured curve shown in Fig. 3.10. The GFET in [Paper F] thus shows larger potential based on its longer gate length. There is a limited benefit of cryogenic cooling on the mobility and noise in these GFETs because of the high impurity density at the graphene/SiO_2 interface, as shown in Fig. 3.5. In combination with small grains, this limits the mobility in the current CVD GFETs to $\lesssim 2,000$ cm^2/Vs at room temperature. Hence, the carriers are most likely in the linear transport region, regardless of the high average field ~ 1.4 V/μm. On the contrary, the optimum low-noise bias for III-V FETs occurs with velocity saturation [44].

Table 3.4: Comparison of the maximum gain bias for GFETs with the optimum low-noise bias for HEMTs and CMOS devices at room temperature. For the lowest noise, the parasitics must be as small as possible and the device should be biased to minimise $\sqrt{I_{ds}}/g_{me}$. † Small-signal gate resistance divided by total gate width.

	$L_g \times W_g$ (μm^2)	g_{me} (mS/mm)	I_{ds} (mA/mm)	$\frac{\sqrt{I_{ds}}/g_m}{\left(\sqrt{\frac{mmV}{S}}\right)}$	R_S (Ωmm) R_G† (Ω/mm)
GFET [Paper F]	1×60	250	370	2.43	0.13 / 18
CVD GFET [99]	0.5×30	1,200	700	0.70	- / -
SiC GFET [21]	0.1×30	2,800	2,000	0.51	0.06 / 143
SiC GFET [98]	0.25×24	1,000	2,200	1.48	0.09 / 63
SiC GFET [125]	0.2×40	730	1,600	1.73	0.08 / 73
GaAs pHEMT [127]	0.13×140	480	140	0.78	0.05 / 2
InP pHEMT [128]	0.13×200	1,065	75	0.26	0.24 / 25
MOSFET [129]	0.065×100	1,050	186	0.41	0.1 / 106

3.6 Large-signal equivalent FET circuit

The small-signal equivalent circuit is useful for modelling the S-parameters and noise parameters of FETs under the assumption of linear operation. However, given a single sinusoidal input or multiple sinusoidal inputs at different frequencies, the large-signal FET model in Fig. 3.13 is required to predict the generation of new frequencies. The model is based on finding a suitable mathematical expression to empirically match the measured drain-source current versus the DC bias. Consequently, this results in a nonlinear FET description since it also models higher-order derivatives. A comparison between the measured and modelled drain current derivatives for a GFET [82] from [Paper A] is illustrated in Fig. 3.14. The embedding linear circuit is the same as the small-signal model, and thus it is extracted in the same way. To obtain the full nonlinear FET model, the bias dependence of the intrinsic capacitors is included. This is important when the reactive currents become appreciable at high frequencies. Finally, it is verified that the large-signal model in Fig. 3.13 is reduced to the small-signal circuit in Fig. 3.7 by linearising the nonlinear current source at a specific bias point, i.e., $i_{ds} \approx g_{mi}v_{gs} + g_{di}v_{ds}$. The DC source reduces to a small-signal current source (g_{mi}) and a conductance (g_{di}).

3.7 Nonlinear circuit applications of GFETs

This section describes the modelling principles of FET power detectors and resistive FET mixers in relation to the large-signal circuit. These are passive modes of operation and can be designed far above the transit time limited frequencies f_T and f_{max} of active FETs. The power detectors in [Paper A] are weakly nonlinear, with a single-frequency small-signal excitation, and they are thus analytically analysed with Volterra series. The mixers in [Paper C] and [Paper D] are strongly nonlinear, they have a large-signal LO pump and one (or two) small-signal excitations, and they are best analysed using the harmonic balance technique within a commercial circuit simulator.

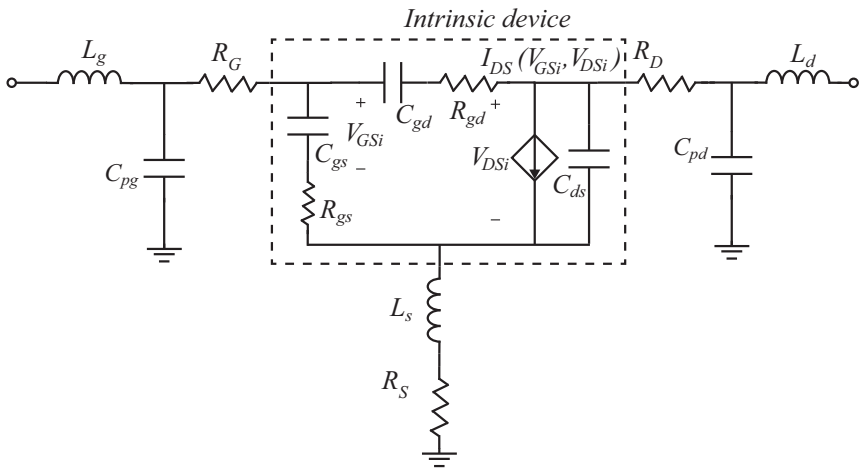

Fig. 3.13: Nonlinear representation of an FET using an equation-based description for the current source. The embedding circuit is assumed to be linear [Paper A].

3.7.1 Volterra analysis of FET power detectors

An FET power detector, like a low-noise amplifier, is typically also operated with a small-signal input. This is the so-called square-law regime in which the output DC voltage is proportional to the input RF power. The proportionality constant is defined as the detector voltage responsivity

$$\beta_v = V_{DC}/P_{RF}. \tag{3.10}$$

However, the operation principle is fundamentally different from that of the amplifier. Any nonlinearity in an amplifier gives rise to undesirable harmonic distortion. In contrast, the detector relies on this device nonlinearity for intentional harmonic frequency generation, which includes the rectified DC signal. Zero-bias detector operation is preferred to avoid excess $1/f$ noise and thus minimise the thermal noise-limited noise equivalent power

$$NEP = \frac{v_n}{|\beta_v|} = \frac{\sqrt{4k_B T R_{ds}}}{|\beta_v|}. \tag{3.11}$$

As a consequence of the cold-FET bias, the intrinsic gate capacitors $C_{gs} \approx C_{gd}$. Furthermore, the cold-FET bias results in a vanishing transconductance [102].

The foundation used to analyse this small-signal nonlinear problem is a Taylor expansion of the large-signal current source around the DC bias point

$$i_{ds}\left(V_{GSi}, V_{DSi}\right) \approx g_{d1} v_{dsi} \; + \; \frac{1}{2} g_{d2} v_{dsi}^2 \; + \; g_{d1s1} v_{dsi} v_{gsi}. \tag{3.12}$$

The weak nonlinearity of the FET current at $V_{ds} = 0$ V allows for accurate analytical calculations using only the second-order derivatives in the Taylor approximation. By neglecting the linear embedding circuit for the moment and exciting the nonlinearity with a sinusoidal input signal, $v_{dsi}(t) = \cos(\omega t)$, the size of the DC voltage is proportional to the so-called curvature

$$\gamma = \frac{d^2 I_{ds}}{dV_{ds}^2} \Bigg/ \frac{dI_{ds}}{dV_{ds}} = \frac{1}{2} \frac{g_{d2}}{g_{d1}}. \tag{3.13}$$

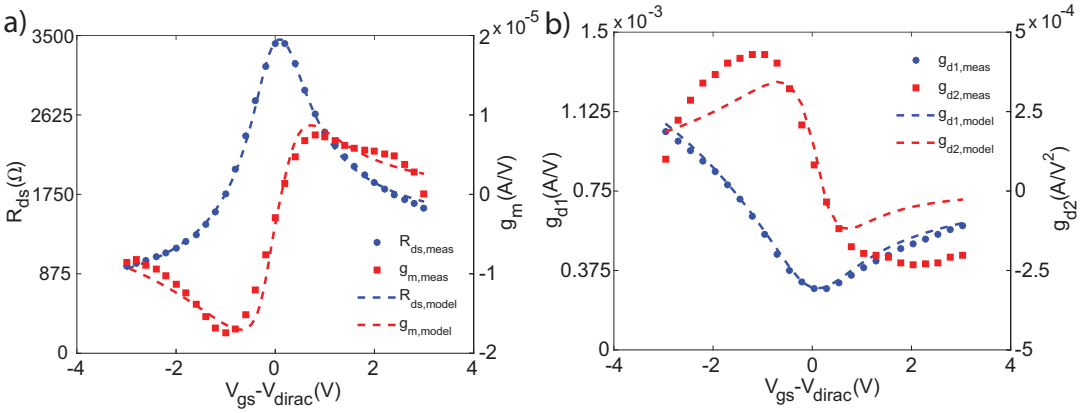

Fig. 3.14: Comparison of measured and modelled a) transfer characteristics, transconductance and b) drain current derivatives w.r.t. the drain voltage [Paper A].

However, it is challenging to accurately reproduce the higher-order derivatives for a GFET with nonlinear models, as illustrated in Fig. 3.14 [82]. Therefore, the second-order derivatives for the current source in Fig. 3.13 were extracted directly from DC measurements in [Paper A].

Understanding how to address the nonlinearity, the linear embedding circuit is introduced in the discussion. Because of the significant feedback capacitance in the equivalent circuit, there is no linear transfer function to relate the control voltages in the model to the input signal. The power detector must thus be analysed using Volterra series [130]. This is performed using the method of nonlinear currents with a single-tone excitation, $v_s(t) = V_s \cos(\omega t)$. The main steps in this method are listed below.

- Replace the current source in Fig. 3.13 by the first-order coefficient g_{d1}. Solve the linear circuit for the first-order voltages v_{gs1} and v_{ds1}.
- Insert the voltages into Eq. 3.12 to obtain the second-order current i_{ds2}.
- Identify the DC term and calculate the rectified voltage $V_{DC} = I_{DC}/g_{d1}$.
- The voltage responsivity is $\beta_v = P_{av}/V_{DC}$, in which $P_{av} = V_s^2/8Z_0$.

In the same way that the active FET gain decreases with frequency, the diminishing responsivity of power detectors at higher frequency is ascribed to the intrinsic and parasitic capacitances that shunt the FET nonlinearity. Similar to the limit frequencies of an active FET derived from the small-signal circuit, cf. Eq. 3.4 and Eq. 3.5, the Volterra series allows the derivation of a 3-dB frequency of the FET power detector from the large-signal circuit

$$f_{3dB} = \frac{1}{2\pi C_{gd}(C_{gs})\sqrt{R_j R_D(R_S)}}. \tag{3.14}$$

The expression in Eq. 3.14 is valid for drain (gate) coupling of the input signal. The responsivity is halved at the 3-dB frequency, or equivalently the NEP doubled, compared to their respective low-frequency values.

3.7.2 Operation principle of resistive mixers

A mixer is a frequency-translating component for RF carrier signals. The mixer is either used to up-convert the frequency in a transmitter or down-convert it in a receiver. Similar to the power detector, the resistive FET mixer takes a small RF input signal at the drain terminal [131]. The major difference is that a large LO signal is simultaneously applied to the gate terminal. This large-signal/small-signal problem calls for different simulation methods than the power detector. The large-signal LO results in a time-varying drain-source conductance waveform, $g(t)$, calculated by harmonic balance analysis [130]. The small-signal is then applied, and the output is calculated using the conversion matrix approach. Expressing the periodic conductance waveform via a Fourier series, the resistive mixer operation can be summarised by

$$i_{ds}(t) = g(t) \times v_{RF}(t) = \left(g_0 + 2\sum_{n=1}^{\infty} g_n cos(n\omega_{LO}t) \right) \times cos(\omega_{RF}t). \quad (3.15)$$

The product of two sinusoids contains the sum and difference frequencies, $\cos(\omega_{RF}t) \times \cos(n\omega_{LO}t) = \frac{1}{2}\left[\cos(\omega_{RF} + n\omega_{LO})t + \cos(\omega_{RF} - n\omega_{LO})t\right]$. The sum and difference frequencies correspond to frequency up- and down-conversions, respectively. By definition, g_0, g_1 and g_n in Eq. 3.15 give the output related to the RF frequency, fundamental mixing and $\times n$ subharmonic mixing, respectively. A unique feature of the channel conductance of GFETs is the symmetry around V_{Dirac}, which inherently result in a large g_2. Due to the electron-hole duality, GFETs thus offers subharmonic mixing in a single device [32].

The resistive mixer performance is quantified as the conversion loss from the RF frequency to the intermediate (IF) frequency, $CL = P_{RF}/P_{IF} > 1$. As is evident from Fig. 3.14a), the drain-source resistance is well described by the nonlinear GFET model. Thus, the model was used to accurately simulate the GFET mixer CL in [Paper C] and [Paper D] using harmonic balance.

The introduction of the resistive FET mixer was motivated by the better linearity compared to diode mixers [131]. This is described qualitatively by a third-order Taylor expansion of the cold-FET drain-source current

$$i_{ds} \approx \frac{dI_{ds}}{dV_{ds}} \cdot v_{RF} + \frac{d^2 I_{ds}}{dV_{ds}^2} \cdot v_{RF}^2 + \frac{d^3 I_{ds}}{dV_{ds}^3} \cdot v_{RF}^3 = g_d \cdot v_{RF} + g_{d2} \cdot v_{RF}^2 + g_{d3} \cdot v_{RF}^3. \quad (3.16)$$

Considering a two-tone input at f_1 and f_2, the coefficient g_{d3} is responsible for the detrimental IM3 products at $2f_1 - f_2$ and $2f_2 - f_1$. These spurious frequencies are close to f_1 and f_2 and thus impossible to filter out. Similar to the power detector, the drain is biased at $V_{ds} = 0$ V, so the FET resistive mixer operates in the linear regime of its output characteristics. The mixer is thus expected to be highly linear because g_{d3} is small for all time instances of (or equivalently, all gate voltages in) the LO sweep. As can be inferred from Fig. 3.14b), the g_{d3} for GFETs peaks at $V_{gs} = V_{Dirac}$. This indicate that fundamental GFET mixers, which are biased such that $R_{ds} \approx (R_{max} + R_{min})/2$, are more linear than subharmonic GFET mixers. Two-tone harmonic balance simulations predicted the subharmonic IM3 products within a few dB of the experimental values in [Paper D].

Chapter 4

High-frequency circuits based on GFETs

In this chapter, several integrated circuit functions are demonstrated using GFETs towards the realisation of a full millimetre-wave receiver. Currently, an RF frequency amplifier is not feasible above a few GHz as a result of the limited f_{max} of GFETs. Mixers, IF amplifiers and power detectors are thus a part of the design focus of [Paper A-E]. The background on integrated circuit technology and planar transmission lines is first presented. This is followed by demonstrations of the mixer and amplifier integrated circuits. Furthermore, the techniques for characterisation of THz power detectors are discussed including the quasi-optical coupling of electromagnetic energy. Finally, the utilisation of graphene for RF energy harvesting antennas is discussed [Paper I].

4.1 Integrated microwave circuits

Traditional microwave circuit technology uses discrete active devices mounted onto a different substrate that contains the transmission line circuitry; this is called hybrid integration. Hybrid integration is non-preferable at frequencies in the higher end of the millimetre wave range and above due to concerns with mounting tolerances, reliability, reproducibility and parasitic effects. Instead, at these frequencies the circuits use a higher integration level where the active and passive devices are both supported on the same substrate. The two main methods of performing this integration are the monolithic microwave circuit integration (MMIC) [9] and the heterogenous circuit integration. Today, the MMIC technology using HEMTs has matured to fabricate complete receivers on GaAs [132] and ultra-low noise LNAs on InP [128]. Heterogenous integration is generally explored to combine the advantageous properties of both III-V active devices with a silicon substrate, such as in high-power devices [133]. Formally, circuits made from CVD graphene are heterogeneously integrated, as the active device layer is transferred to a non-native silicon substrate. However, circuits made from epitaxial graphene are considered to be monolithic [125]. In this thesis, the amplifier circuit in [Paper E] is an example of hybrid integration, whereas the mixer of [Paper C] is a heterogenous circuit.

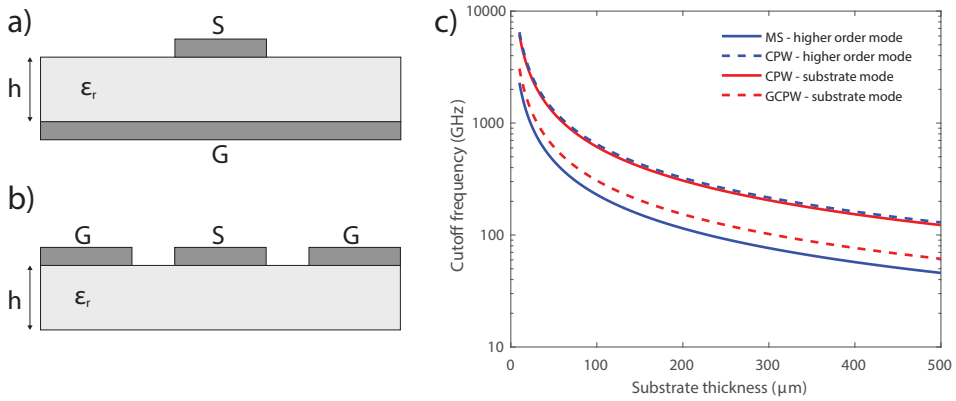

Fig. 4.1: Cross-sections of the a) microstrip (MS) and b) coplanar waveguide (CPW). c) Comparison of cutoff frequencies on Si for the first higher-order modes on MS and CPW. The lowest-order substrate mode for CPW is also shown [136, 137].

4.1.1 Planar transmission lines

The two most frequently used planar transmission lines for guiding electromagnetic energy in microwave integrated circuits are the microstrip (MS) and the coplanar waveguide (CPW), as shown Fig. 4.1a) and b). The microstrip is dominant at microwave frequencies as it has well-developed computer-aided design (CAD) design kits. However, with increasing frequency starting in the higher millimetre wave regime, the CPW has attracted significant interest [134]. This is because microstrip circuits require extremely thin substrates at very high frequencies, as shown in Fig. 4.1c), which are lossy and impractical to handle [132, 135]. The list below highlights some design guidelines, merits and limitations of CPW lines [9, 135–137].

- Proper electrical grounding of the active devices even at millimetre wave frequencies is obtained in CPWs due to the low source inductance.
- Airbridges connecting the groundplanes are needed to suppress the odd CPW (slotline) mode, especially at circuit discontinuities.
- Parallel plate transmission line (substrate) modes can be excited in CPWs when a bottom ground plane is present, e.g., in a package or on the metallic chuck of a probe station. This can be avoided by keeping the substrate thin in terms of wavelength as illustrated in Fig. 4.1c).
- If there is a lower limit on the substrate thickness, via holes and backside metallisation in the CPW circuit can be used to short the substrate mode. This is also preferable in applications where a heat sink is necessary.
- The electric field confinement in the substrate is low, and the current flows close to the edges of the centre conductor. This makes both radiation loss and metal loss concerns in CPW circuit design.
- A well-designed CPW line is broadband with low frequency dispersion.

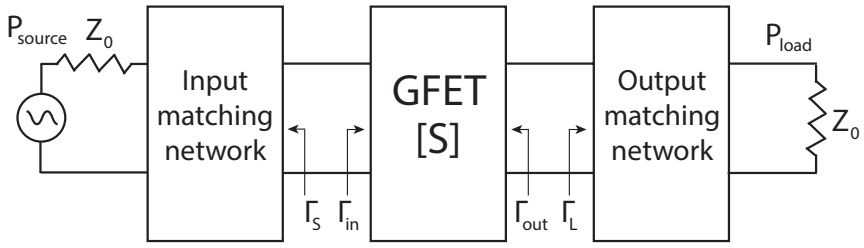

Fig. 4.2: Schematic drawing of a single-stage small-signal GFET amplifier layout.

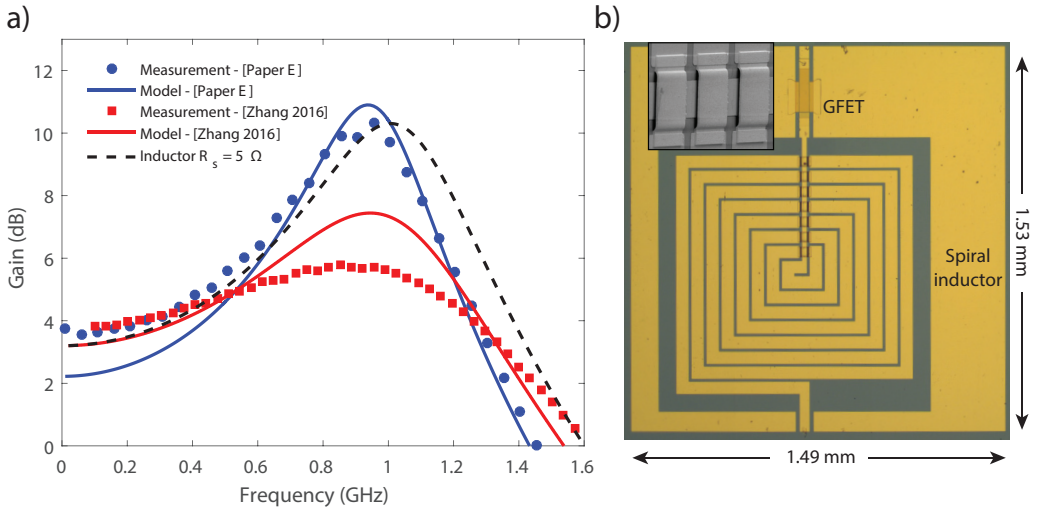

Fig. 4.3: a) Performance of small-signal GFET amplifiers using an exfoliated GFET ($L_g = 1\ \mu m$, $W_g = 2 \times 30\ \mu m$) and a wire inductor [Paper E], as well as a CVD GFET ($L_g = 1\ \mu m$, $W_g = 2 \times 120\ \mu m$) and a planar inductor [96]. The dashed black line shows the CVD GFET matched with a similar but low-loss planar inductor.
b) Micrograph of the planar amplifier with SEM image of the airbridges in the inset.

4.2 Small-signal GFET amplifiers

The value of f_{max} is the highest frequency at which a transistor can provide power gain under idealised conditions. Typically, however, values of f_T and f_{max} should be several times higher than the intended application frequency for the device to exhibit gain at practical impedance levels. The actual gain of an amplifier is the so-called transducer power gain, which, at a certain bias point and from the S-parameter matrix at a certain frequency, is given by

$$G_T = \frac{P_{load}}{P_{source}} = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}. \tag{4.1}$$

In Eq. 4.1, Γ_{in} is the reflection coefficient looking into the device input, while Γ_S and Γ_L are the reflection coefficients looking from the device towards the source and load, as shown in Fig. 4.2. The stipulation that $|S_{21}| > 1$ is an important prerequisite to fabricate an amplifier. With the starting point of $|S_{21}|^2$, the amplifier gain is further enhanced by designing input and output impedance matching networks, which are quantified by the source and load reflection coefficients, Γ_s and Γ_L, respectively [138]. The matching networks

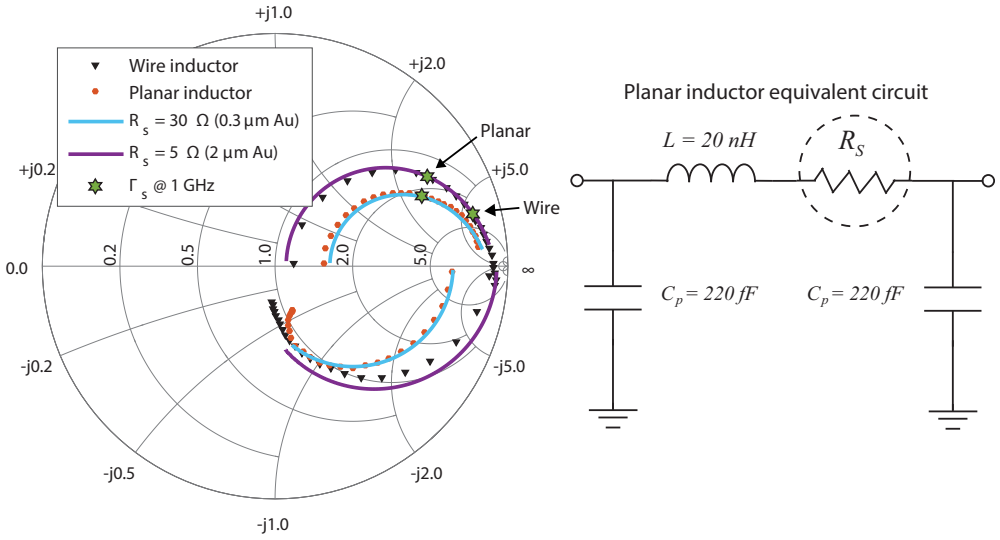

Fig. 4.4: Measured S-parameters up to 2 GHz for the surface mount wire inductor ($L = 36$ nH from the datasheet) [Paper E] and the planar inductor ($L = 20$ nH from the extracted equivalent circuit) [96]. A simulated planar inductor with thicker gold is included for comparison. The models were verified by EM simulation.

are implemented either by distributed transmission lines [125] or by lumped inductors and capacitors, as is the case in [Paper E] using a surface mount inductor and in [30,96] using integrated planar inductors. Ideally, the matching networks should be lossless.

4.2.1 Matching circuit design and performance

The first matched small-signal amplifier which exhibits substantial power gain at microwave frequencies was demonstrated in [Paper E]. Previously, only voltage gain at gigahertz frequencies was reported [99]. After the publication of [Paper E], several reports have appeared demonstrating power gain in integrated GFET amplifiers including a 4 dB gain achieved at 4.8 GHz using a CVD GFET [30] and a 3.4 dB gain achieved at 14.3 GHz with an SiC GFET [125]. Moreover, in conjunction with [Paper C], CVD GFETs integrated with planar inductors were fabricated. The results were presented in [96] and are introduced for comparison to [Paper E] below.

In the low-GHz frequency range, the input impedance of the on-wafer GFETs is inherently capacitive. Thus, the source reflection coefficient for maximum gain lies in the inductive half plane of the Smith Chart close to that of an open circuit, $\Gamma_S \approx S_{11}^*$ [Paper E]. On the other hand, the output impedance for relatively wide devices is reasonably close to 50 Ω, and the enhancement from drain matching is small when weighed against the increased circuit complexity. Discrete matching networks were chosen here since distributed matching circuits on a silicon substrate would consume an impractically large area at such a low frequency. A series inductor on the gate port is selected for simultaneous matching and convenient DC biasing.

The first proof-of-concept amplifier in [Paper E] is based on an exfoliated graphene FET and a surface mount inductor. The second-generation

design from [96] realised with a CVD graphene FET uses an integrated on-chip matching inductor. This demonstrates a higher possible integration level of the technology as we move towards the full wafer-scale. The performance of the two amplifiers is compared in Fig. 4.3. Both designs use GFETs with 1-μm-long gates, while the CVD device is considerably wider to accommodate the lower normalised transconductance due to its thicker gate oxide. The reduced gain for the CVD GFET is related to the high resistive loss of the fabricated planar inductor. This is identified using the inductor equivalent circuit in Fig. 4.4. This shows the need for electroplating of $\sim$2 μm Au for the bottom metallisation of the inductor. The capacitive loss on the high-resistive silicon is reasonably low. In this thesis, the active devices both operate with a 6 - 10 dB gain at 1 GHz $\approx 0.1 \cdot f_{max}$. Similarly, the recently demonstrated IC with a 200-nm-gate SiC GFET can provide a lower 3.4 dB amplification closer to the limit frequency at 14.3 GHz $\approx 0.35 \cdot f_{max}$ [125].

4.2.2 Analysis of the amplifier noise figure

The noise figure of the amplifier in [Paper E] at the design frequency of 1 GHz was determined as NF $= 6.4 \pm 0.4$ dB. The measurement was performed with the Y-factor method, which by definition amounts to finding

$$Y = \frac{P_H}{P_C} = \frac{T_H + T_n}{T_C + T_n}. \tag{4.2}$$

The hot and cold noise powers, P_H and P_C, are measured at the output of the device while presenting the known hot and cold noise temperatures, T_H and T_C, at its input. The total noise temperature T_n is solved from Eq. 4.2. To distinguish the device and measurement receiver noise figures, the device gain is de-embedded using the cascade formula [109]. The gain is measured via the output noise powers with the device and a through connection inserted in the measurement path, $G_{DUT} = (P'_H - P'_C)/(P_H - P_C)$.

To obtain the minimum noise figure of the GFET itself, the Pospieszalski noise model was extracted for the complete amplifier. It was assumed in the extraction that $T_g = T_a$ [139]. Thus, the measured amplifier noise figure at a single source impedance at each frequency is enough for the extraction of the second frequency independent model parameter $T_d \approx 23,000$ K. This value of T_d is significantly higher than values reported for other GFETs [140], [Paper F] as well as other FET technologies [112, 113]. Since a satisfactory fit was obtained, this indicates the lumping of several noise mechanisms into the drain current source. However, gate leakage current, which can cause an increased noise figure in this frequency range [123], was not observed. Instead, the likely cause of the high T_d in [Paper E] is the omission of the substrate resistors R_{pg} and R_{pd}. These have been shown to have a similar effect on the minimum noise figure as a conducting gate in [Paper F]. Indeed, for the GFETs on semi-insulating SiC, lower expected values of $T_d < 2,000$ K were found even without the inclusion of the substrate resistors in the model [124,140]. In addition, the large uncertainty in the extraction of the source resistance for an exfoliated GFET propagates into the calculated value for T_d. To summarise, the slope of NF_{min} versus frequency in [Paper E] is likely overestimated.

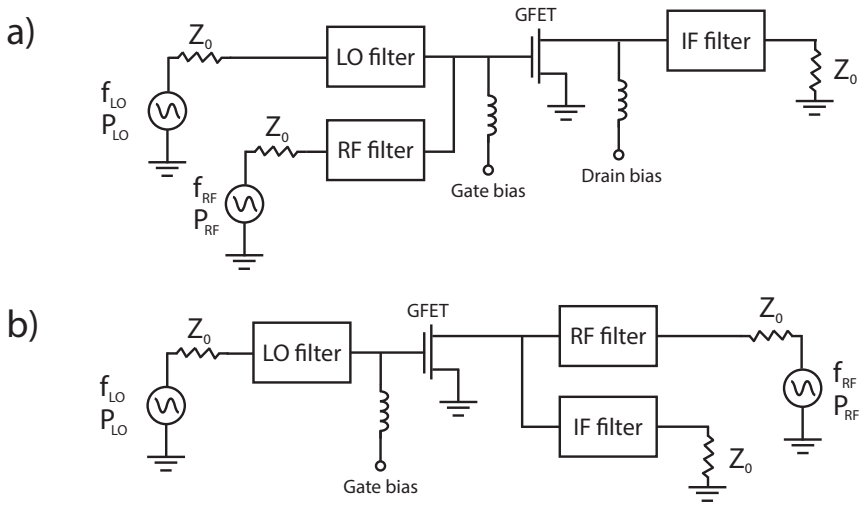

Fig. 4.5: Schematic circuits for single-ended a) active and b) resistive GFET mixers.

4.3 Frequency mixers based on GFETs

There are two main operation modes of the frequency mixers shown in Fig. 4.5, the transconductance (active) mixer and the resistive (passive) mixer. In the active mixer, the RF signal applied on the gate is mixed with an LO pumped transconductance waveform. In the resistive mixer, the drain-source resistance is pumped and mixed with an RF signal applied at the drain. Moreover, the mixers are divided into fundamental ($f_{IF} = f_{RF} - f_{LO}$) and subharmonic ($f_{IF} = f_{RF} - 2f_{LO}$). The active mixer designs are often fundamental, whereas both fundamental and subharmonic resistive mixers are commonly found. In any case, all variants require filter circuitry to separate the LO, RF and IF signal paths and to apply a DC gate bias. In addition, balanced designs can be used for improved isolation and linearity [130]. The conversion loss of all the down-converting resistive GFET mixers discussed below are compared in Fig. 4.6 to those of other technologies. These results should be compared to the theoretical minimum conversion loss of 3.9 dB in a resistive mixer [141].

4.3.1 Fundamental mixers

The reported active GFET mixers are limited by the small transconductance and give CL $>$ 14 dB up to 5 GHz [30,142]. Similarly, the best resistive GFET mixer also gives CL = 14 dB at 2 GHz and a comparable LO power level [143]. However, these results should also be compared to GaAs FETs, which provide a CG of $\sim$ 10 dB in the active mixer operation mode [130].

The IIP3 quality factor, $Q(IIP3) = IIP3/P_{LO}$, is a useful parameter to compare the linearity of different mixers. This is because an increased LO power minimises the duration of the LO sweep where the mixer is close to the nonlinear turn-on region [144]. GaN power devices give high linearity but low $Q(IIP3)$ since they can withstand a very high LO power [145]. As predicted in Section 3.7.2, the fundamental GFET resistive mixers [143] outperform the subharmonic counterparts [83] and [Paper D], and they are comparable to GaAs technology in terms of linearity, $Q(IIP3) \sim 20$ dB [131].

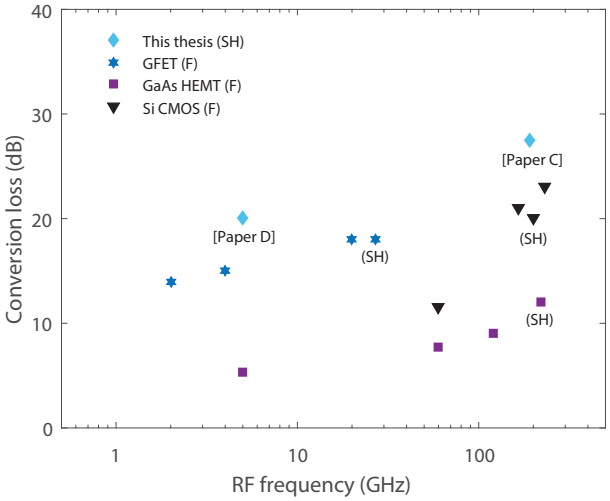

Fig. 4.6: Conversion loss for the GFET resistive mixers in [Paper C] and [Paper D] compared to the literature [83, 142, 143] and to other FET resistive mixers realised in the mature GaAs [132, 141] and Si CMOS [146, 147] technology nodes. The labels correspond to the following: F = Fundamental, SH = SubHarmonic.

4.3.2 Subharmonic mixers

Subharmonic mixers are common especially for millimetre waves to relax the frequency requirement of the high-power LO pump. Furthermore, the larger frequency separation, $f_{LO} \approx f_{RF}/2$, simplifies the filter design. In particular, the separation helps to prevent LO leakage through the gate-drain capacitance to the RF port, which is increasingly severe at higher frequencies. Conventionally, the subharmonic resistive GaAs mixers use two HEMTs where the LO is fed 180 ° out of phase to the devices [148]. Similarly, subharmonic diode mixers use an anti-parallel diode pair. As explained in Section 3.7.2, the GFET uniquely allows subharmonic mixing in a single device. This concept has been demonstrated using external filters at 2−5 GHz [32], [Paper D], and in a 30 GHz integrated microstrip mixer based on an exfoliated graphene flake [83].

The frequency of the integrated subharmonic GFET mixer in [Paper C] is scaled further to $f_{RF} = 200$ GHz. Based on Section 4.1.1, CPWs were chosen for the transmission line interconnects and filters the due to the relaxed requirement on substrate thickness compared to microstrips. Extensive full-wave simulations were performed in CST microwave studio (FDTD method) to verify the single-mode characteristics of the CPW lines and prevent excessive radiation loss. A photo of the fabricated mixer circuit is shown in Fig. 4.7 and labelled to indicate the physical realisation of the filters. To suppress the excitation of substrate modes, the high resistive silicon substrate was lapped down to a thickness of 100 μm. Airbridges were fabricated using a sacrificial PMGI layer to ensure the same electrical potential of both groundplanes. The detailed fabrication parameters for the airbridges are given in Appendix A.

To confirm the millimetre wave CPW design, the full four-port circuit S-parameters were measured in a break-out configuration where the GFET was replaced by a through line. Broadband measurements were made up to 145 GHz and in the 140-220 GHz (WR-5) band using 1 mm coaxial and

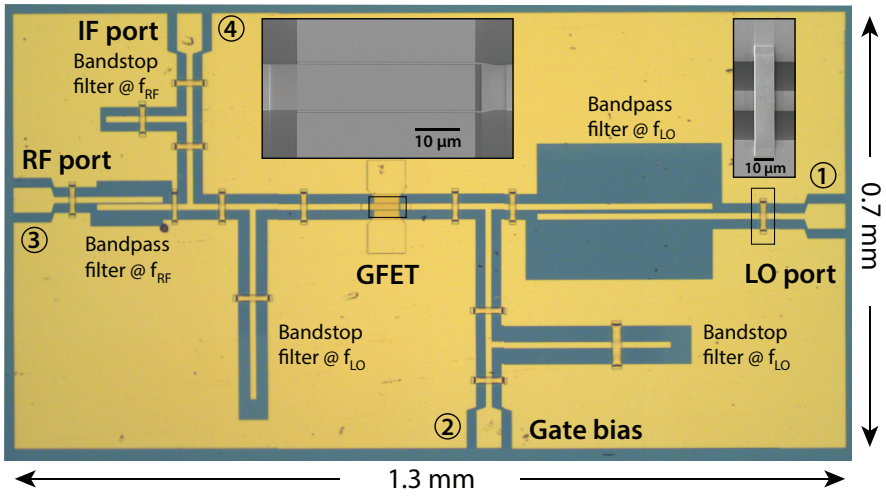

Fig. 4.7: The G-band subharmonic resistive GFET mixer IC reported in [Paper C].

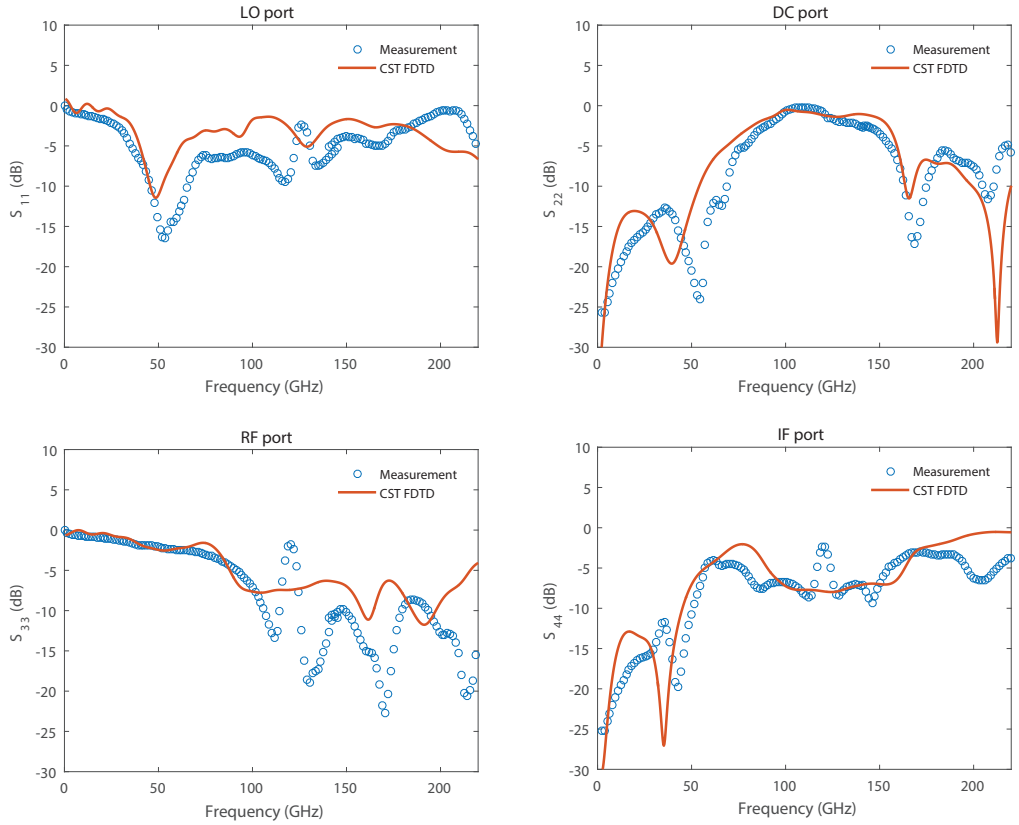

Fig. 4.8: Reflection S-parameters of the airbridged four-port CPW mixer circuit.

waveguide interface probes, respectively. Six independent on-wafer two-port measurements were conducted, each with the remaining two ports left open. Mathematically, an open port amounts to striking the corresponding row and column in the Z-matrix. In this manner, the four-port Z-matrix was assembled backwards from the individually measured two-port Z-matrices and converted to retrieve the 16-element S-matrix. The results are shown in Fig. 4.8 for port reflections and Fig. 4.9 for transmission between the ports.

Finally, the on-wafer mixer conversion loss was measured to be 29 ± 2 dB within the RF frequency interval 185-210 GHz using the setup in Fig. 4.10. To improve the conversion loss, the pumped GFET resistance should resemble a square wave with a higher on-off ratio and even on- and off-state times, i.e., a bandgap is required for graphene. However, even in the absence of a bandgap, improved mobility and contact resistance would be advantageous in the GFET resistive mixer to reduce the LO power required to switch between the on- and off-states. In addition, a receiver design was fabricated where the mixer in Fig. 4.7 was cascaded with the IF amplifier in Fig. 4.3 via a DC block capacitor. However, no functioning circuit could be measured due to the low GFET yield.

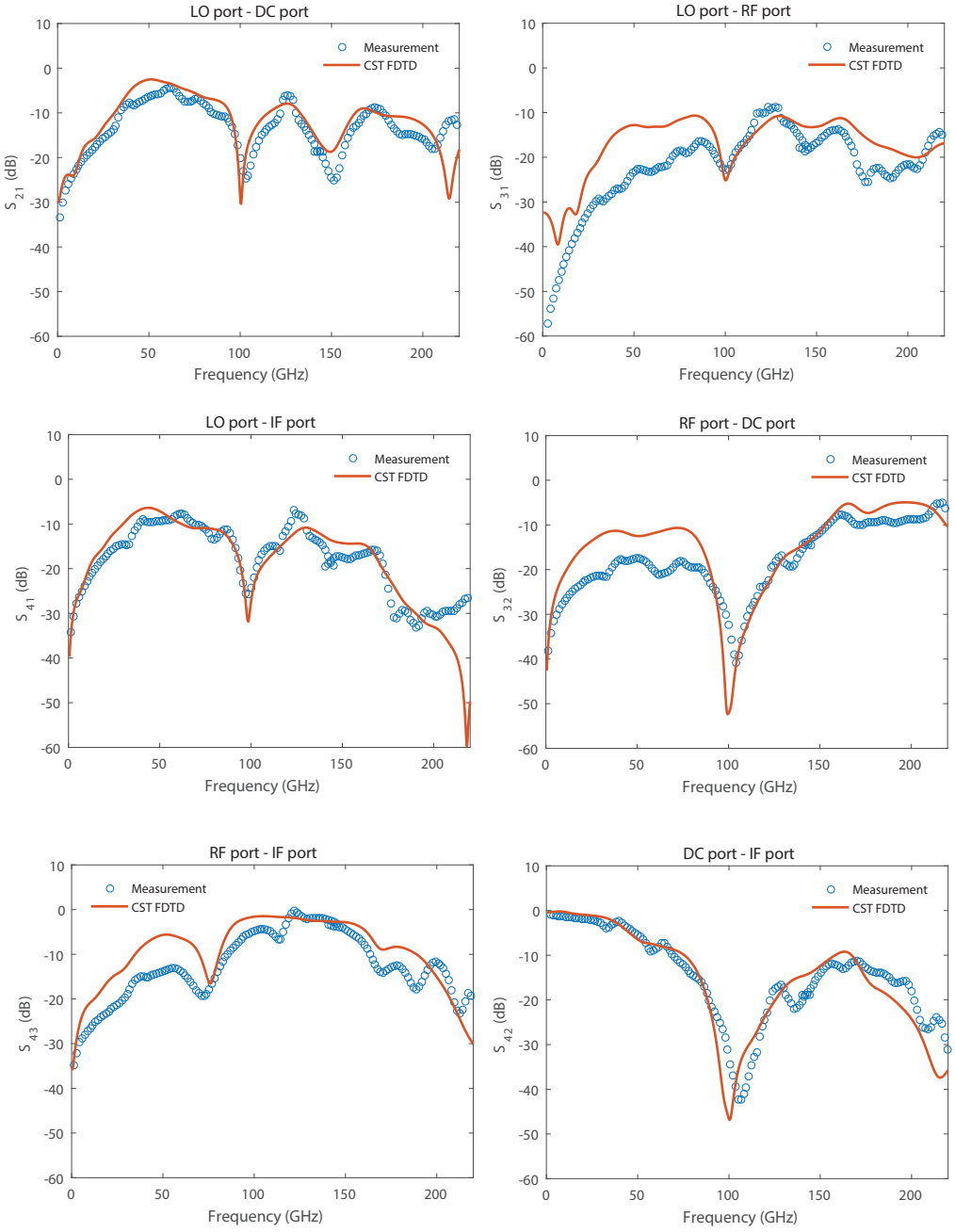

Fig. 4.9: Transmission S-parameters of the airbridged four-port CPW mixer circuit.

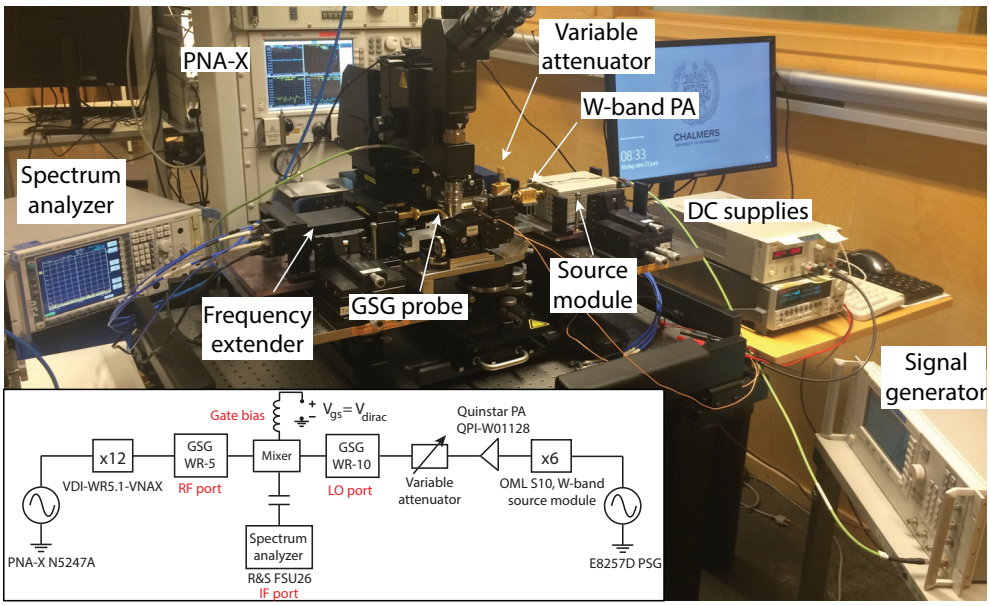

Fig. 4.10: The on-wafer RF measurement setup used to characterise the G-band subharmonic resistive GFET mixer IC reported in [Paper C]. The reference receiver of the PNA is used to level the mixer input power at the extender output.

4.4 Quasi-optical THz circuits

The straightforward method for testing devices and circuits in a lab is to connect probes directly to measurement pads on the wafer surface. High-frequency probes are commercially available up to a frequency of 1 THz. However, they come with an exponentially increasing price for higher frequency bands.

The most accurate power calibration method for detectors is to mount a single chip in a waveguide. Similarly, the method of choice for receivers below 1 THz is to couple the power into a waveguide via a horn antenna. An on-chip probe serves as an efficient transition to couple the linearly polarised electric field to the detector. The drawback is the expensive micromachining required to fabricate the small dimensions of waveguides above 1 THz. Furthermore, the thin samples required result in inconvenient mounting of the chips.

One solution is to use a lithographically defined planar antenna integrated on the same substrate as the detector. The main beam is directed towards the substrate since it has a higher dielectric constant than air. However, rays are trapped inside the substrate outside the critical angle, $2 \cdot \Theta_c$, as shown in Fig. 4.11a). To avoid these internal reflections, the substrate is placed onto an extended hemispherical lens [149] of the same dielectric material, as shown in Fig. 4.11b). A quasi-optical circuit is designed to match the Gaussian beam phasefronts from the source to the lens layout to efficiently couple the power, as illustrated in Fig. 4.11c). This approach was used in [Paper B] to characterise the GFET power detector integrated with a bow-tie antenna on the substrate and mounted on a hyperhemispherical lens. The antenna impedance and pattern bandwidths can be wide for self-complimentary planar antennas, such as in the bow-tie, log-periodic and log-spiral designs [150]. The lens size has to be adapted to the wavelength for optimum coupling.

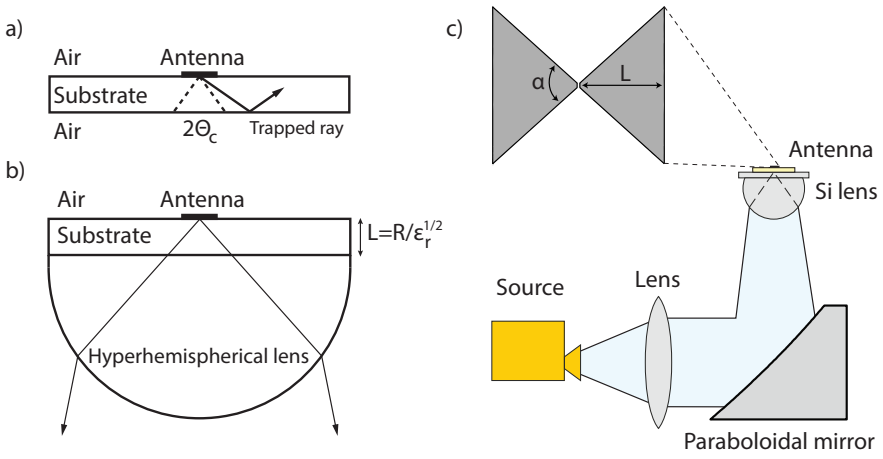

Fig. 4.11: a) Planar antenna radiating on a substrate illustrating the trapped rays. b) The same planar antenna on a hyperhemispherical lens to prevent reflected rays. c) Quasi-optical circuit used to match the Gaussian beam wavefront from the source to the lens [Paper B]. The inset shows the bow-tie angle α and the bow-tie length L.

The bow-tie antenna from [Paper B] is illustrated in the inset of Fig. 4.11c). The outer and inner dimensions yield the upper and lower frequency limits, respectively, while the angle defines the real part of the antenna impedance. The simulated impedance in the lower frequency range of Fig. 4.12a) shows that this particular design is electrically small at 600 GHz. An electrically longer bow-tie has an off-broadside radiation pattern on an infinitely thick dielectric substrate [151]. However, the radiation pattern of an electrically short bow-tie on an infinite substrate resembles that of the simple dipole. This is then steered further towards the perpendicular direction by using the lens. The high simulated directivity from CST is illustrated in Fig. 4.12b) using a hyperhemispherical lens with a diameter $d = 5$ mm.

4.5 Electrical model for FET THz detectors

The plasma-wave theory has been predominantly used to explain the power detection in FETs [152]. The experimental FET detectors are said to operate in the so-called broadband detection regime, where a weak gate length and a strong mobility dependence on the NEP is suggested. Moreover, the theory indicates that the NEP decreases at high frequency where the plasmonic effect is stronger. The plasmon effects might play a role in dedicated device structures. However, the NEP compilation in Fig. 4.13 displays no clear-cut sensitivity enhancement in high mobility III-V heterostructures compared to CMOS. Furthermore, there is roughly a NEP $\propto f^2$ trend at high frequencies.

To address these discrepancies between theory and experiment, the Volterra-based electrical model in [Paper A] was developed. It clarifies the influence of mobility and RF frequency on the NEP and was used to derive device design rules, both under conjugately matched conditions and when $R_j \gg Z_0$. Here, $R_j = 1/g_{d1}$ is the real part of the small-signal FET impedance. This situation is typical for detectors fed by standard probe and antenna impedances, and it is therefore used as the example in the discussion below.

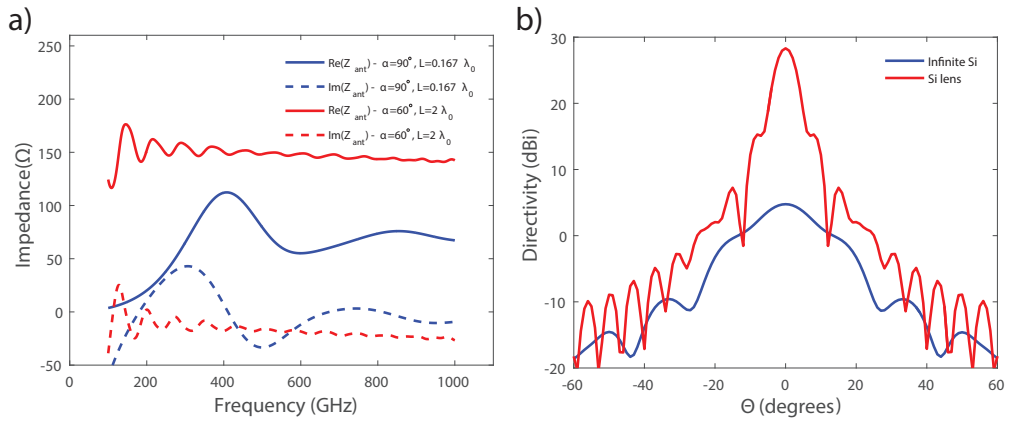

Fig. 4.12: a) Simulated antenna impedance from CST for the bow-tie antennas in [Paper B] ($\sim$ 65 Ω) and [151] ($\sim$ 150 Ω). The lengths are given in free-space wavelengths at 600 GHz. b) Simulated antenna patterns from CST for the bow-tie antenna in [Paper B] on an infinite Si substrate and an hyperhemispherical Si lens with diameter $d = 2R = 5$ mm $= 10\lambda_0$ at 600 GHz and extension $L = R/\sqrt{\varepsilon_r}$.

4.5.1 Frequency dependence of the NEP

The full frequency dependence of the FET power detector NEP is derived in [Paper A]. Particularly in the high-frequency limit, $f \gtrsim 3 \cdot f_{3dB}$, and for drain coupling of the input RF signal, the model yields the responsivity

$$\beta_v \approx \frac{2Z_0\gamma}{4\pi^2 f^2 C_{gd}^2 \left(R_D + Z_0\right)^2} \propto 1/f^2. \tag{4.3}$$

This relation also applies for the gate coupling of the input RF signal by replacing C_{gd} by C_{gs} and R_D by R_S. Likewise, a similar expression holds for power detector diodes [162], as indicated by the dashed trendline in Fig. 4.13. The comparison is not strictly quantitative, since the proportionality constant in Eq. 4.3 depends on the antenna impedance, FET technology and device dimensions. Similarly, the f_{3dB} point depends on the FET technology and device dimensions. Thus, it should be noted that the lower limit of validity for the f^2 asymptote is not the same for the different technologies in Fig. 4.13. Performing wideband 50 Ω probed measurements on a single FET eliminates the listed uncertainties and enables a truly quantitative extraction of the frequency dependence. This verification was performed on GFETs up to 67 GHz, which was $\sim 2.5 \cdot f_{3dB}$ in [Paper A]. More characterisation is necessary to determine the full frequency dependence between [Paper A] and [Paper B] for the GFET technology developed in this thesis.

4.5.2 Design and characterisation of GFET detectors

Based on the closed-form expressions for NEP in [Paper A], the significance of the gate length, gate width and mobility was elucidated. The analysis is based on geometrical scaling for the detector impedance $R_j \propto L_g/W_g$, the intrinsic FET capacitors $C_{gs} \approx C_{gd} \propto L_g \times W_g$ and the series resistances $R_S \approx R_D \propto 1/W_g$. In addition, the key roles of the gate bias and the on-off ratio for the FET power detector performance are explained.

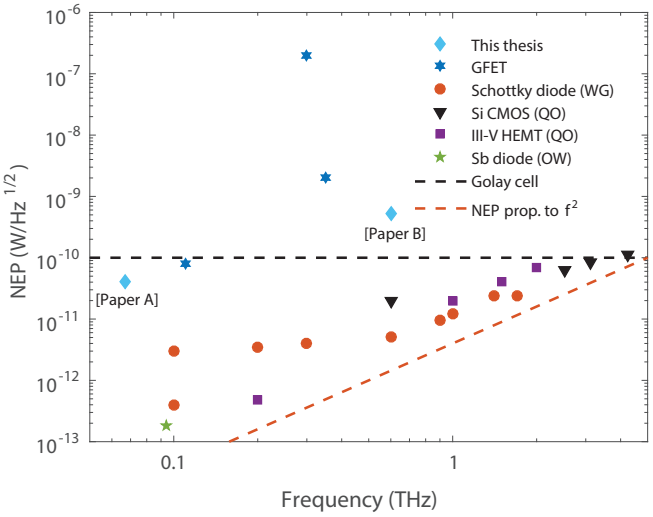

Fig. 4.13: Comparison of NEP for GFET detectors in [Paper A] and [Paper B] to literature [153–155] and to other solid-state rectifiers: Schottky diodes [156–158], Si CMOS [13], III-V HEMTs [159, 160], and Sb backward diodes [161]. The labels correspond to: OW = On-Wafer, WG = WaveGuide, and QO = Quasi-Optical.

- The NEP for a mismatched FET detector improves when the capacitance is minimised as $L_g \to 0$ until the fringing fields sets the lower NEP limit.
- The model predicts a smaller influence of the gate width on the NEP. For quasi-optical detectors, narrower FETs have resulted in lower NEP, which is likely a result of the easier antenna-integration of the FET.
- The mobility dependence is only implicit in the detector impedance R_j. There is no explicit NEP decrease observed for high-mobility FETs.
- The FET on-off ratio has a significant impact on the NEP. The gate bias can therefore effectively increase the intrinsic FET impedance while maintaining a low series resistance. Thus the curvature, $\gamma = g_{d2}/g_{d1}$, can be large close to the threshold even though cold-FETs are linear [131].

A state-of-the art NEP of 40 pW/Hz$^{1/2}$ at 67 GHz was achieved for GFETs using the design rules, as shown in Fig. 4.14 [Paper A]. Furthermore, the NEP of 500 pW/Hz$^{1/2}$ at 600 GHz in [Paper B] could be improved by down-scaling the gate length. However, there is an order of magnitude discrepancy between the GFET and CMOS performance in Fig 4.13. One reason is that the true optical NEPs are given in this thesis, in contrast to the NEPs reported for CMOS, which are corrected for quasi-optical losses and the beam profile shape. Nevertheless, enabling a bandgap in the graphene channel to improve the GFET curvature is required to compete with CMOS in power detectors.

Finally, it is interesting to compare the GFET NEP to that of commercial room temperature detectors for laboratory use and THz cameras. These are based on thermal effects: Erickson metres, Golay cells, pyroelectric detectors and semiconductor bolometers [163]. They exhibit extremely broadband NEP of ∼100 pW/Hz$^{1/2}$, as highlighted by the horizontal line in Fig. 4.13. However, the thermal processes are orders of magnitude slower than electrical detectors.

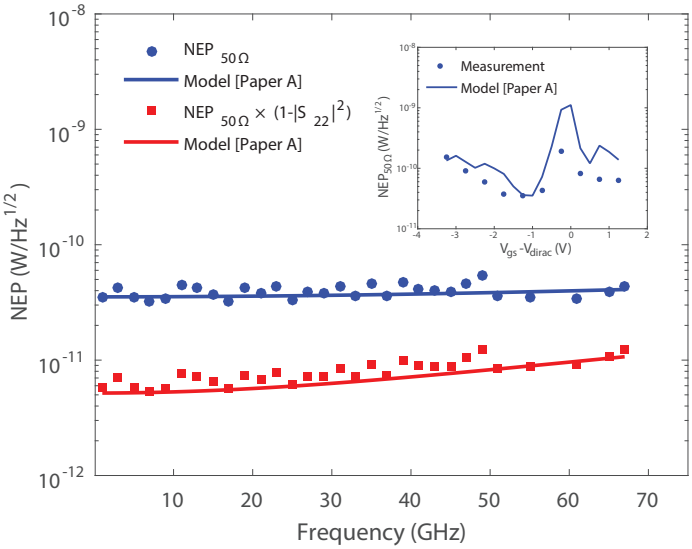

Fig. 4.14: The Volterra model agreement of NEP for a GFET ($L_g = 0.5$ μm and $W_g = 2 \times 1.25$ μm) versus frequency and gate voltage (in the inset) [Paper A].

4.6 Graphene antennas for energy harvesting

In addition to high data rate communications links, the Internet of things is an essential part of the next generation mobile networks. Specifically, the machine-to-machine (M2M) communication of sensor readings is predicted to take place on a massive scale to monitor and control the status of objects and people. The deployment and maintenance of the sensors are required to be cheap and eco-friendly, which means that they must be operated self-sustainable instead of relying on battery power. One option for ubiquitous sensor deployment in urban environments is to harvest RF energy. However, new materials are required to realise the omnipresent Internet of things. In particular, transparent and flexible antennas would enable a diversity of M2M applications, e.g., on windows, or for wearable devices.

This was the motivation to evaluate the prospects of using graphene dipole antennas to harvest RF energy for self-sustainable M2M sensors in [Paper I]. The graphene antenna efficiency was simulated in Ansys HFSS, and translated to the harvested power based on experimental ambient RF power levels [164]. Finally, the harvested power was subtracted from the transmitter DC power consumptions of a current state-of-the-art commercial transceiver [165], and an ultra-low-power transceiver demonstrated at a research institution [166]. The dependence of the transceiver net power consumption on the graphene antenna sheet resistance is shown in Fig. 4.15, under the M2M assumption of one sensor status transmission per day. Conclusions for the two most interesting combinations of available power and power consumption are listed below.

- On a location with average RF intensity, S_{BA}, the low-power transceiver and graphene $R_{sh} < 100$ Ω/sq are required for self-sustainable operation.
- On a location with maximum RF intensity, S_{BA}, the commercial transceiver and graphene $R_{sh} < 5$ Ω/sq are required for self-sustainable operation.

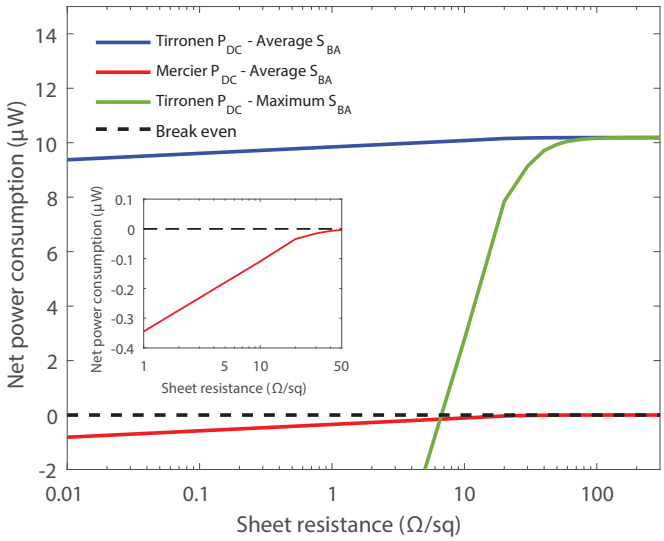

Fig. 4.15: The net power consumption of the transceiver assuming a single data transmission event per day [Paper I]. Energy is harvested in the communication frequency bands around 2 GHz using a graphene dipole antenna.

As summarised in Section 3.2.2, special treatments can only reduce the multilayer CVD graphene sheet resistance to ∼20 Ω/sq. Thus, transparent antennas with sufficient efficiency for self-sustainable sensors is currently a very challenging task, given the available ambient RF power and DC power consumption of transmitters for M2M systems. Nevertheless, the cost and flexibility advantages from ink-jet printed, opaque graphene might be used.

Chapter 5

Conclusions and future outlook

The objective of this thesis was to advance wafer-scale graphene technology for microwave and THz applications. To this end, fabrication, characterisation and modelling of CVD GFETs on silicon substrates for RF applications were conducted to identify the performance limits of the technology. Furthermore, both the integrated 200 GHz subharmonic mixer circuit and the 600 GHz quasi-optical power detector are state-of-the-art GFET demonstrators.

Today, the GFET THz detector operation is ascribed to overdamped plasma-waves. The take-home message of the plasma-wave theory is that a high carrier mobility is the most important factor for sensitive detection. However, the GFET power detector in [Paper B] performs an order of magnitude worse than its CMOS counterparts despite the higher mobility. The electrical model for FET power detectors in [Paper A] aims to explain this discrepancy. Contrary to previous models, the missing bandgap rather than the mobility is the key to understanding the inferior GFET detector. Since it is based on the lumped large-signal FET equivalent circuit, the model lends itself to the derivation of closed-form expressions for the NEP in the intrinsic capacitances and parasitic resistances. In contrast to the plasma-wave picture, these equations reveal an inverse gate length and frequency dependence of the NEP.

Similar to the power detectors, the high conversion loss of the passive GFET resistive subharmonic mixers in [Paper C] and [Paper D] is not due to the low mobility. This only increases the demand on the LO sweep power to pump the mixer between the on- and off-states. Instead, the ultimate problems for fundamental and subharmonic resistive GFET mixers reside in the high series resistance and the missing graphene bandgap, which limit the on- and off-states, respectively. The methods of establishing a bandgap in graphene simultaneously degrade the mobility. This is unfortunate for active GFETs, which require both a sizeable bandgap and a high mobility. However, even a bandgap at reduced mobility is a major progress step for the performance of both GFET power detectors and mixers. Furthermore, the subharmonic GFET mixers require the gate to be biased at the Dirac voltage. Under this bias condition, higher levels of third-order intermodulation are generated than in fundamental resistive mixers operated for minimum conversion loss.

Contrary to passive applications, high mobility is the key to higher transconductance in active GFETs. Together with a bandgap to reduce the output conductance this is required to maximise the cutoff frequency and maximum frequency of oscillation, for which a vast amount of experimental data exists. However, knowledge of the microwave noise performance of active GFETs is equally important for the design of LNAs in receiver circuits. For the first time, the full GFET noise parameters are reported in [Paper F]. This enables the construction of the Pospieszalski and PRC noise models. Similar to the case of oxide-gated silicon MOSFETs, a low correlation factor is extracted in the PRC model for the gate and drain noise sources. Future studies have to fully clarify whether the correlation factor can be improved by higher quality gate stacks on graphene or if the low correlation factor is a limitation of the GFET device structure. Additionally, better gate stacks would improve the CVD GFET mobility. In other words, it is necessary to elucidate if both the $\sqrt{I_{ds}}/g_m$ ratio and the correlation factor in GFETs can compete with the values observed for III-V HEMTs.

Currently, replacements to both the bottom- and top-gate graphene-oxide interfaces are developed to improve the carrier mobility for active CVD GFETs. The h-BN dielectric environment is optimal for high-mobility graphene on the scale of exfoliated flakes. However, there are no procedures for high-quality layer-by-layer transfer or *in situ* growth of large-area h-BN and CVD graphene on a technologically relevant scale. The development of the h-BN technology is especially important for realising low-noise GFETs. Moreover, by screening the charged impurities using high-κ ferroelectrics is effective to improve the mobility only in dirty graphene samples from inherently low levels [Paper H].

In addition to the bandgap and mobility issues, the high contact resistance is often highlighted as a major obstacle for GFET technology in RF electronics. The bottlenecks of metal contacts have been identified to a large extent. However, in CVD graphene processing there is poor reproducibility [Paper G]. A high contact resistance deteriorates the resistive mixer conversion loss, the detector noise equivalent power and the amplifier noise figure [Paper E].

Presently, epitaxial GFETs show more reproducible mobility and contact resistance, and they are more promising than CVD GFETs for high-end RF circuits. In addition, hydrogen-intercalated bilayer graphene on SiC exhibits a small bandgap induced by the built-in field in the substrate. Still, there is a large gap in its performance compared to even silicon microwave FETs.

Therefore, the most likely opportunities for CVD graphene are in applications where current technology performs poorly, in particular, for flexible electronics. For instance, the potential of graphene antennas for deployment in a ubiquitous Internet of things scenario is investigated in [Paper I]. In this context, the inherent versatility in the transfer of CVD graphene to arbitrary substrates is a decisive factor. Consequently, the CVD GFET circuits on silicon presented in this thesis can be viewed as the preamble for flexible graphene-based terahertz electronics. In addition, the CVD graphene has a higher potential than SiC graphene for high-end RF GFETs given a significant breakthrough in the growth of graphene and boron nitride heterostructures.

Chapter 6

Summary of appended papers

This chapter presents a brief summary of the content of the appended papers and a short description of my contribution to each paper.

Paper A

An Accurate Empirical Model Based on Volterra Series for FET Power Detectors

In this paper an empirical and equivalent circuit based model for FET power detectors was presented and experimentally verified by measurements on GFETs. Main results are the closed-form expressions for the detector responsivity and noise equivalent power and the dimensional scaling rules.

My contributions: Initiated the work and derived the model equations. Then designed, fabricated and characterised the devices to assess the model validity. Interpreted the results and wrote the paper.

Paper B

Antenna-Integrated 0.6 THz FET Direct Detectors Based on CVD Graphene

In this paper a state-of-the-art quasi-optical GFET power detector with noise equivalent power of 500 pW/Hz$^{1/2}$ at 600 GHz is demonstrated.

My contributions: Main responsible for the device fabrication. Participated with co-authors in the design, characterisation and writing of the paper.

Paper C

A 185-215 GHz Subharmonic Resistive Graphene FET Integrated Mixer on Silicon

In this paper the a record high frequency for integrated graphene electronics is shown. The results show state-of-the-art performance in terms of both conversion loss and operating frequency.

My contributions: Main responsible for the circuit fabrication scheme and the millimetre wave characterisation. Provided regular input during the circuit design phase and took a leading role in the writing of the paper.

Paper D

Resistive Graphene FET Subharmonic Mixers: Noise and Linearity Assessment

In this paper the conversion loss, noise figure and linearity of GFET resistive mixers in the 2-5 GHz frequency range are reported.

My contributions: Performed the fabrication, characterisation and analysis together with co-authors. Main responsible for writing the paper.

Paper E

10-dB small-signal graphene FET amplifier

In this paper the first GFET amplifier with 10 dB gain and 6.4 dB noise figure is reported, fabricated on exfoliated graphene. Tentative noise modelling based on the Pospieszalski model is performed.

My contributions: Suggested the concept, performed the fabrication and noise modelling. Took part in the characterisation and wrote the letter.

Paper F

Microwave noise characterization of graphene field effect transistors

In this paper the source-pull noise figure results on a GFET were presented. After de-embedding the parasitics from the noise parameters, the possibility of 1-dB noise figure up to 2 GHz was predicted.

My contributions: Main responsible for arranging the noise measurements. Provided daily input during the phases of fabrication, data analysis and noise model development. Took a significant role in the writing of the paper.

Paper G

Microwave characterization of Ti/Au-graphene contacts

In this paper microwave measurements on circular TLM structures are used to model the capacitance associated with the metal-graphene contact.

My contributions: Fabricated and measured the test structures. Performed the data interpretation together with co-authors and wrote the paper.

Paper H

Effect of ferroelectric substrate on carrier mobility in graphene field-effect transistors

In this paper a mobility enhancement on $LiNbO_3$ by screening of charged impurity is found at levels below 1,000 cm^2/Vs. Moreover, gate oxide quality is correlated to the graphene mobility via the microwave loss tangent.

My contributions: Participated in the fabrication and provided feedback during the data analysis and paper writing.

Paper I

Feasibility of Ambient RF Energy Harvesting for Self-Sustainable M2M Communications Using Transparent and Flexible Graphene Antennas

In this paper power budget calculations were performed to assess the viability of using transparent and flexible graphene antennas to harvest RF energy to power sensors in ubiquitous use cases in the future Internet of things.

My contributions: Responsible for a major part of the literature study, coordinated the calculations with input from the co-authors and wrote the paper.

Appendix A

Recipe CVD GFET circuits

The fabrication steps assumes the grown CVD graphene is transferred to a 10×10 mm^2 or 20×20 mm^2 high resistivity Si chip with alignment marks.

1 Mesa and nanoconstriction etch

- Spin coat the negative tone **ma-N 2401** resist undiluted at **3000 rpm** during **30 s** for **100 nm** thickness.
- Soft bake on hotplate at **110 °C** for **60 s**.
- E-beam expose pattern **proximity corrected** using **BEAMER** at **100 kV/2 nA** with a dose of **400 μC/cm^2**.
- Develop for **30 s** in **MF-CD-26**, rinse DI, N_2 blow dry.
- Resist ash at **50 W** RF power/**250 mTorr** pressure for **5 s**.
- Etch graphene at **50 W** RF power/**50 mTorr** pressure for **6 s**.
- Ash top resist at **50 W** RF power/**250 mTorr** pressure for **3 s**.
- Strip resist in **acetone** for **5 min** at **19 °C**, rinse IPA, N_2 blow dry.

2 Ohmic contact metallisation

- Spin coat **copolymer** resist diluted in ethyl lactate (10% w/w) at **3000 rpm** during **60 s** for **400 nm** thickness.
- Soft bake on hotplate at **170 °C** for **5 min**.
- Spin coat **AR-P 6200.13** resist diluted 1:2 in anisole (4.3% w/w) at **4000 rpm** during **60 s** for **70 nm** thickness.
- Soft bake on hotplate at **170 °C** for **5 min**.
- E-beam expose pattern **proximity corrected** using **BEAMER** at **100 kV/10 nA** with a dose of **350 μC/cm^2**.
- Develop AR-P for **45 s** in **n-Amylacetate**, N_2 blow dry.
- Develop copolymer for **2 min** in **MIBK:IPA 1:1**, N_2 blow dry.
- Evaporate **1 nm Ti/15 nm Pd/100 nm Au**.
- Lift-off in **acetone** for **10 min** at **70 °C**, rinse IPA, N_2 blow dry.

3 Gate oxide formation

- Anneal in **1000 sccm Ar** gas flow for **15 min** at **230 °C**.
- Evaporate **1 nm Al**, oxidise on hotplate at **170 °C**, repeat **4 times**.
- Thermal ALD of **176 cycles** at **300 °C** for **15 nm Al_2O_3**.

4 Gate finger metallisation

- Spin coat, bake, expose and develop according to ***step 2***.
- Evaporate **250 nm Al/10 nm Ti/50 nm Au**.
- Lift-off in remover **mr-Rem 400** for **15 min** at **50 °C**, rinse acetone and IPA, N_2 blow dry.

5 Oxide etch to access ohmic metal layer

- Spin coat **S1813** resist at **4000 rpm/30 s** for **1.3 μm** thickness.
- Soft bake on hotplate at **110 °C** for **2 min**.
- Expose direct laser writer, **intensity 100%** and **focus offset 0%**.
- Develop for **60 s** in **MF319**, rinse DI, N_2 blow dry.
- Resist ash at **50 W** RF power/**250 mTorr** pressure for **30 s**.
- **Buffered oxide etch (7:1)** dip for **30 s**, rinse DI, N_2 blow dry.
- Ash at **50 W** RF power/**250 mTorr** pressure for **30 s**.
- Strip resist in **acetone** at **70 °C** for **5 min**.

6 Pad and/or antenna metallisation (feature sizes $\gtrsim$ 5 μm, Au thickness $\lesssim$ 300 nm)

- Dehydration bake on hotplate at **200 °C** for **2 min**.
- Spin coat **HMDS** adhesion promoter at **3000 rpm/30 s**.
- Spin coat **LOR 3B** at **4000 rpm/60 s** for **400 nm** thickness.
- Soft bake on hotplate **200 °C** for **5 min**.
- Spin coat **S1805** resist at **4000 rpm/60 s** for **500 nm** thickness.
- Soft bake on hotplate at **110 °C** for **60 s**.
- Expose direct laser writer, **intensity 70%** and **focus offset 0%**.
- Develop S1805 and etch $<$ **1 μm undercut in LOR** by **MF319** starting with **30 s**, rinse DI, N_2 blow dry.
- Resist ash at **50 W** RF power/**250 mTorr** pressure for **10 s**.
- Evaporate **10 nm Ti/300 nm Au**.
- Lift-off in remover **1165** (or mr-Rem 400) for **15 min** at **50 °C**, rinse acetone and IPA, N_2 blow dry.

7 Coplanar waveguide circuit metallisation (feature sizes $\lesssim$ 5 μm, Au thickness $\lesssim$ 500 nm)

- Spin coat **copolymer** resist diluted in ethyl lactate (10% w/w) at **5000 rpm** during **60 s** for **300 nm** thickness.
- Soft bake on hotplate at **170 °C** for **5 min**.
- Spin coat **copolymer** resist diluted in ethyl lactate (10% w/w) at **3000 rpm** during **60 s** for **400 nm** thickness.
- Soft bake on hotplate at **170 °C** for **5 min**.
- Spin coat **AR-P 6200.13** resist diluted 1:2 in anisole (4.3% w/w) at **4000 rpm** during **60 s** for **70 nm** thickness.
- Soft bake on hotplate at **170 °C** for **5 min**.
- E-beam expose pattern **proximity corrected** using **BEAMER** at **100 kV/35 nA** with a dose of **350 μC/cm^2**.
- Develop AR-P for **45 s** in **n-Amylacetate**, N_2 blow dry.
- Develop copolymer for **2 min** in **MIBK:IPA 1:1**, N_2 blow dry.
- Resist ash at **50 W** RF power/**250 mTorr** pressure for **5 s**.
- Evaporate **10 nm Ti/500 nm Au**.
- Lift-off in **acetone** for **10 min** at **70 °C**, rinse IPA, N_2 blow dry.

8 PMGI patterning by e-beam (after lapping)

- Dehydration bake on hotplate at **160 °C** for **5 min**.
- Spin coat **PMGI SF11** at **2000 rpm/45 s** for **1.2 μm** thickness.
- Soft bake on hotplate at **160 °C** for **10 min**.
- E-beam expose pattern **proximity corrected** using **BEAMER** at **100 kV/35 nA** with a dose of **850 μC/cm^2**.
- Develop in **101A** starting with **2 min**, rinse DI, N_2 blow dry.
- Resist ash at **50 W** RF power/**250 mTorr** pressure for **10 s**.
- Reflow PMGI in oven at **250 °C** for **30 s**.

9 PMGI patterning by laser writer (before lapping)

- Spin coat and bake PMGI according to ***step 8***.
- Spin coat **S1813** resist at **4000 rpm/30 s** for **1.3 μm** thickness.
- Soft bake on hotplate at **110 °C** for **2 min**.
- Expose direct laser writer, **intensity 100%** and **focus offset 0%**.
- Develop the S1813 imaging layer and **strip unprotected PMGI** by **MF319** for **2 min 15 s**, rinse DI, N_2 blow dry.
- Ash down the S1813 layer at **50 W** RF power/**250 mTorr** pressure **step-by-step** (rate $\sim$100 nm/min).
- Dip in **acetone** for **5 s**, rinse IPA, N_2 blow dry.
- Reflow PMGI in oven at **250 °C** for **30 s**.

10 Airbridge metallisation (before or after lapping)

- Spin coat **PMMA A11** resist diluted in anisole (11% w/w) at **3000 rpm** during **45 s** for $>$ **2** μ**m** thickness.
- Soft bake on hotplate at **160 °C** for **10 min**.
- E-beam expose pattern **proximity corrected** using **BEAMER** at **100 kV/35 nA** with a dose of **1000** μ**C/cm^2**.
- Develop in **IPA:DI 10:1** for **2 min**, rinse IPA, N_2 blow dry.
- Resist ash at **50 W** RF power/**250 mTorr** pressure for **20 s**.
- Evaporate **10 nm Ti/1000 nm Au**.
- Lift-off in **acetone** for **10 min** at **80 °C**.
- Strip PMGI in remover **1165** for **10 min** at **80 °C**.
- Rinse in acetone and IPA and N_2 blow dry.

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