Frequency Multiplier Based on Distributed Superconducting Tunnel Junctions: Theory, Design and Characterization

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Frequency Multiplier Based on Distributed Superconducting Tunnel Junctions: Theory, Design and Characterization

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***Abstract*— In this paper, we present the analysis, design and characterization of the first frequency multiplier using distributed SIS junctions. We derived analytical expressions describing the properties of the distributed SIS junction as a frequency multiplier. The modeling of the distributed SIS junctions shows that high conversion efficiency can be achieved when used as the multiplier. The measured output power generated by such multiplier employing the distributed SIS junction at the second harmonic of the input frequency is in good agreement with the model. Furthermore, the frequency multiplier based on distributed SIS junction was for the first time able to pump an SIS mixer. The multiplication efficiency of the distributed SIS junction is 15-30 % for a fractional bandwidth of 10% with excellent spectral line purity. The -3 dB line width of the multiplied signal is 1 Hz, which was limited by the resolution bandwidth of the spectrum analyzer. The results attained in this work show that the distributed SIS junction frequency multiplier has considerable future potential, and could possibly be used in LO source in single-end and multi-pixel SIS mixer receivers.**

***Index Terms*—SIS frequency multipliers, Superconducting tunnel junctions, Submillimeter wave devices.**

I. Introduction

MODERN cryogenic heterodyne millimeter and sub millimeter receivers for radio-astronomy most often employ Superconductor-Insulator-Superconductor (SIS) tunnel junctions as mixers. The noise contribution from the mixer is greatly reduced due to quantum nature of the SIS tunnel junction operation and limited by zero-fluctuation quantum noise. When operated in the quantum mode, the SIS mixer enables conversion gain while the tunneling current voltage (I-V) characteristic of the junction exhibits extremely sharp quasiparticle tunnel current (QTC) nonlinearity [1]. This technology provides ultimate sensitivity and offers possibilities for spectral line (spectroscopic) observations [2], [3], [4].

Generally, in these ultrasensitive SIS receivers, the LO source and frequency multipliers are placed at room temperature, and the LO signal is coupled to the mixer either using long stainless- steel waveguide or quasi-optics. In the case of waveguide LO coupling, quite substantial fraction of the LO power is lost because of the waveguide losses. For multi-pixel receivers, the LO distribution system introduce even a bigger challenge as it becomes bulky and extremely complex. Because, apart from quantum cascade lasers, the solid-state fundamental sources are not available above 120-130 GHz the LO source end stage is typically some sort of frequency multiplier, where the nonlinear element is usually a Schottky diode. These LO frequency multipliers can generate signals up to 1-2 THz [5],[6]. There has also been a lot of work carried out on frequency generation based on Josephson effect, both using low-Tc superconductors [7] and high-Tc superconductors [8]. Often, the superconductor electronics based LO source and the mixer are integrated on a single chip [7, 9]. However in the majority of the practical receivers, a semiconductor multiplication of the frequency was used to generate the LO power with disadvantages described above.

On the other hand, the extremely nonlinear behavior and quantum nature of operation of an SIS tunnel junction give reasons to believe that an SIS device designed for frequency multiplication can operate with very high conversion efficiencies, since the higher order QTC harmonics in an ideal SIS junction would be similar to the Fourier series of a Dirac delta function. However, until now, little work has been done on understanding and modeling of the harmonic generation (frequency multiplication) in SIS devices using quasiparticle tunneling effect [10, 11] in comparison to sub harmonic mixers [12],[13],[14]. The power output is defined primarily on the tunnel current, since the voltage scale of the SIS junction is fixed with respect to the gap voltage, V_g of the superconductors. Likewise, the tunnel current in the SIS junction is dependent on the junction area and transparency. It is the physical parameters, such as the junction area, A, and normal resistance, R_N, which defines the output power of the SIS junction and is therefore proportional to the junction size (which is relatively small for SIS junction frequency multiplier), since the voltage scale, which leaves the current as the only parameter defining the power. According to our simulations, the generated output power at the second harmonic ranges over a few nano-watts to few hundreds of nano-watts depending on the SIS junction structure and size. The output power produced by an SIS junction based multiplier could be further increased by using an array of SIS junctions [1] or by power combining techniques [6]. Furthermore, the most sensitive heterodyne receivers in the millimeter/submillimeter region use the SIS and HEB mixers

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[15], which require a very low LO power. From this perspective, the SIS frequency multiplier is completely compatible with the SIS/HEB mixer systems with respect to its operating environment and power requirements [16]. Moreover, the SIS junction frequency multiplier could also be integrated with the SIS mixer on the same chip, similar to the approach described for flux-flow oscillators in [9] to minimize the path between the multiplier and the SIS mixer, and thus minimize the power loss. From the other hand, in multi-pixel heterodyne systems, where the complexity of the LO distribution and LO power requirement are among the biggest challenges, an SIS frequency multiplier could offer a very attractive alternative. In such a scenario, the phase locking (if needed) and distribution of the LO (e.g., Schottky or HBV multipliers) signal can be carried out at much lower frequencies, where attaining high output power is much easier [17], [18], [19], and the transmission loss is less detrimental. In this case, the final multiplication stage could consist of a SIS frequency multiplier integrated with the mixer and with a possibility to adjust the power through the choice of the DC bias at the SIS multiplier junction. In this paper, we analyze and design the first frequency multiplier based on a distributed (long) SIS junction. Even though the approach of integrating the multiplier and SIS mixer on a single chip is very appealing, for the first demonstration, we opt for a nonintegrated approach.

Recently, an experimental paper published by Billade et al. [20] experimentally proved the presence of the second harmonic generated by a SIS junction series array consisting of 68 elements. However, the overall conversion efficiency was insufficient and only a few nano-watts of power could be delivered at the output frequency and not enough to pump an SIS mixer. In this paper we suggest and study both theoretically and experimentally a frequency multiplier based on presumably more practical alternative, the distributed (long) SIS junction. We employ the both large signal modeling and the Tucker's approximation, i.e., assuming that the pumping signal applied across the SIS junction is purely sinusoidal [1] and study the conversion efficiency for both cases. Furthermore, in the study, it is shown that different junction parameters had pronounced impact on the performance of the SIS junction frequency multiplier.

The structure of this paper is as following: in the Section II-A below, the induced QTC due to an external pumping signal (PS) is discussed. In the Section II-B, the harmonic behavior of the QTC is discussed, where the importance of some key features is highlighted. In the Section II-C, both the lumped and series array SIS junction are discussed. In the Section II-D, we develop the closed form expressions describing the properties of the distributed SIS junction frequency multiplier, which are later used in the circuit design. The output power and efficiency at the generated harmonics of interest are discussed in the Section II-E. In the Section II-F, we introduce the large signal model. The estimated conversion efficiency from the large signal model is also presented. The multiplier circuit design is discussed in the Section III. Finally, the Section IV treats the measurement setup and the obtained results. The measurement results are also compared with modeled data as shown in the Section IV.

II. THEORY

A. Quasi-particle Tunnel Current

The quasi-particle tunnel current in SIS tunnel junctions has been studied in great detail in [1]. The induced QTC due to an applied fundamental RF signal, i.e., pumping signal is given by:

$$I_{PS}(V_{bias},\omega) = 2\pi\sum_{m=0}^{\infty}[a_m - ib_m] \tag{1}$$

with the magnitudes of a_m and b_m given by:

$$2a_m = \sum_{n=-\infty}^{\infty} J_n(\alpha)(J(\alpha)_{n+m} + J(\alpha)_{n-m})\, I_{dc}\left(V_{bias} + \frac{n\hbar\omega}{e}\right)$$

$$2b_m = \sum_{n=-\infty}^{\infty} J_n(\alpha)(J(\alpha)_{n+m} - J(\alpha)_{n-m})\, I_{KK}\left(V_{bias} + \frac{n\hbar\omega}{e}\right) \tag{2}$$

where, m is the harmonic number and $m=0$ is for the pumped dc QTC, $J_n(\alpha)$ is the Bessel function of the first kind, α is the pumping factor i.e., the amplitude of the PS waveform normalized with the photon voltage $\alpha = eV_{PS}/\hbar\omega_{PS}$. I_{dc} and I_{KK} are the imaginary and real parts of the complex current response function:

$$r(V) = jI_{dc}(V) + I_{KK}(V) \tag{3}$$

Furthermore, I_{KK} is the reactive part of the QTC, which relates to the dissipative part of the tunnel current through the Kramers-Kronig transform:

$$I_{KK}(V) = P\int_{-\infty}^{\infty}\frac{d\bar{V}}{\pi}\frac{I_{dc}(\bar{V}) - \bar{V}/R_N}{\bar{V}-V} \tag{4}$$

where P is the Cauchy principal value integral and R_N is the normal state resistance of the niobium superconducting electrodes of the SIS junctions.

Clearly, even though it may sound controversial, the real and imaginary part of the induced tunnel current given by eq. (1)-(2), are proportional to the imaginary (I_{dc}) and real (I_{KK}) part of the current response function respectively.

The real and imaginary part of the response function in eq. (3) must be obtained in order to compute the closed form expression of the QTC given by eq. (1)-(2). The dissipative part of the current response function could be either directly measured (dc I-V characteristics) or calculated from complicated theoretical expressions, which has to be computed numerically [1, 21]. The reactive part of the un-pumped tunnel current i.e., I_{KK}, could be obtained through eq. (4). In this paper we use an empirical model, eq. (5) for the dissipative part of the tunnel current i.e., I_{dc}, in order to study the I_{KK} current effect on the overall QTC.

$$I_{dc}(V) = \left[\frac{V}{R_L}\left(\frac{1}{1+e^{-a(V+V_g)}}\right) + \frac{V}{R_N}\left(\frac{1}{1+e^{a(V+V_g)}}\right)\right] + \left[\frac{V}{R_L}\left(\frac{1}{1+e^{a(V-V_g)}}\right) + \frac{V}{R_N}\left(\frac{1}{1+e^{-a(V-V_g)}}\right)\right] \tag{5}$$

The empirical model we suggest has four fitting parameters: R_L is the subgap resistance, R_N is the normal resistance, V_g is the gap voltage, and the coefficient, a, accounts for the transition width at gap voltage, henceforward referred to as the current onset sharpness. Three out of the four fitting parameters (R_L, R_N, and V_g) used in the empirical model are physical parameters, which are extracted from the measured I-V characteristics [22]. The current onset sharpness width coefficient, a, is estimated through fitting and has a typical value of approximately $3\text{-}4\cdot10^4$ (V^{-1}) for the Nb-AlO_x-Nb junctions produced in-house [23]. This parameter can be used as a measure of the junction quality, as explained in section II-E.

The first term in the square bracket in the eq. (5) is the dc quasiparticle tunnel current with respect to negative bias voltage, whereas the second term in the square bracket accounts for positive bias voltage. The two terms inside the square brackets refer to the subgap and normal electron current, i.e., the current before and after the gap onset, whereas the Fermi-Dirac-like functions define where the onset occurs and its sharpness. Fig. 1 shows the comparison between the modeled and the measured I-V characteristics. Clearly, the modeled I-V characteristic of the SIS junction is in a very good agreement with the measured one.

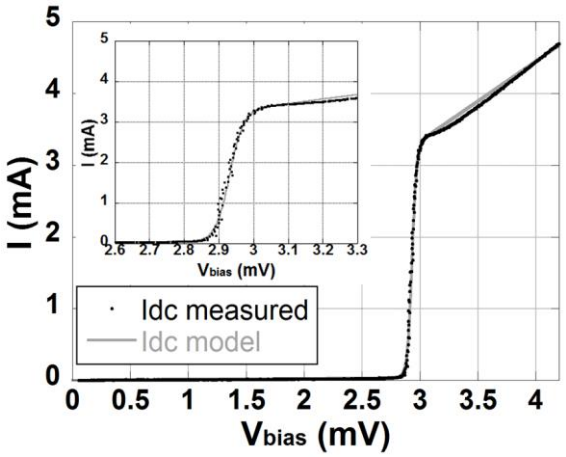

Fig. 1: Modeled I-V according to equation (5) compared with measured I-V characteristics. The insert shows the I-V curve close to the gap voltage.

B. Harmonic behavior of the QTC

When PS is applied, the behavior of the output current at different harmonics could be studied through eq. (1). However, the SIS quantum impedance is required in order to study the output power. The small signal quantum admittance of the SIS junction [1] is expressed as:

$$Y_{mm'} = G_{mm'} + jB_{mm'} \tag{6}$$

$$G_{mm'} = \frac{e}{2\hbar\omega_{m'}} \sum_{n,n'=-\infty}^{\infty} J_n(\alpha)J_{n'}(\alpha)\delta_{m-m',n'-n}\{ \left[I_{dc}\left(V_0 + n'\frac{\hbar\omega}{e} + \frac{\hbar\omega_{m'}}{e}\right) - I_{dc}\left(V_0 + n'\frac{\hbar\omega}{e}\right)\right] + \left[I_{dc}\left(V_0 + n\frac{\hbar\omega}{e}\right) - I_{dc}\left(V_0 + n\frac{\hbar\omega}{e} - \frac{\hbar\omega_{m'}}{e}\right)\right]\} \tag{7}$$

$$B_{mm'} = \frac{e}{2\hbar\omega_{m'}} \sum_{n,n'=-\infty}^{\infty} J_n(\alpha)J_{n'}(\alpha)\delta_{m-m',n'-n}\{ \left[I_{KK}\left(V_0 + n'\frac{\hbar\omega}{e} + \frac{\hbar\omega_{m'}}{e}\right) - I_{KK}\left(V_0 + n'\frac{\hbar\omega}{e}\right)\right] - \left[I_{KK}\left(V_0 + n\frac{\hbar\omega}{e}\right) - I_{KK}\left(V_0 + n\frac{\hbar\omega}{e} - \frac{\hbar\omega_{m'}}{e}\right)\right]\} \tag{8}$$

The quantum admittance at the different harmonics is given by *m=m', i.e.*, Y_{mm}. The generated power at the second harmonic ($m=2$) could be estimated through equations (1)-(8). The power due to the real, imaginary and resultant part of the quasiparticle tunnel current with respect to the bias voltage at pumping factor, $\alpha=1.2$ are shown in Fig. 2 for the second harmonic. Table I summarizes the SIS junction parameters used for the calculations. The pumping frequency in this example is 100 GHz, whereas the 2nd harmonic corresponds to 200 GHz.

The fine structures in Fig. 2 are separated exactly by the voltage corresponding to the multiple of the applied PS photon size. Thereby, Fig. 2 clearly shows the presence of the multi-photon processes. Furthermore, Fig.2 also shows that the maximum total power corresponds to the maximum reactive power, and that the real part of the power at that point is zero. The importance and the impact of the reactive component of the total power will be further discussed in the Section II-E.

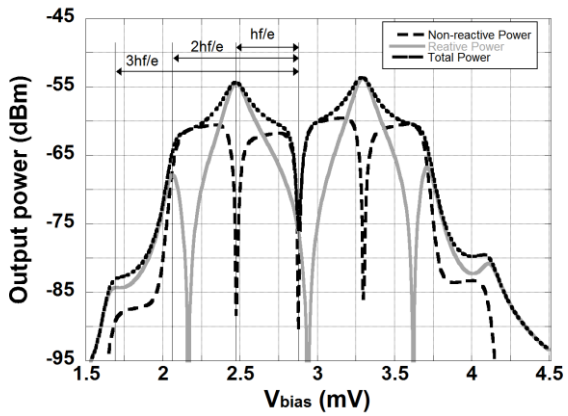

Fig. 2: The calculated power generation due to the second harmonic of the QTC at the pumping factor $\boldsymbol{\alpha = 1.2}$. The dashed line shows the power due to the non-reactive QTC, whereas the solid gray plot illustrates the power due to the reactive QTC. The dotted line shows the total power at the second harmonic.

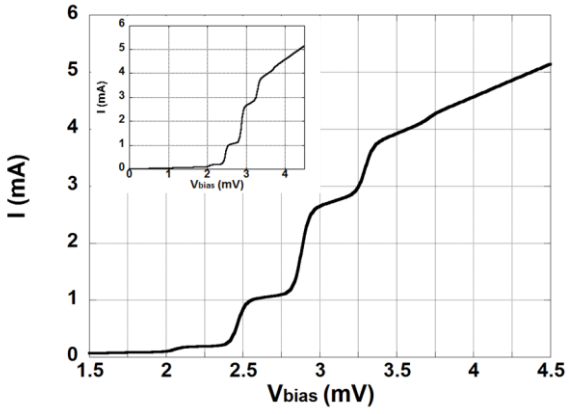

Fig. 3: The calculated pumped dc I-V at the pumping factor $\alpha = 1.2$, whereas the insert show the induced static I-V for the voltage rang of 0-5 mV.

TABLE I. COEFFICIENT VALUES FOR THE EMPIRICAL IVC MODEL OF Nb-AlOx-Nb SIS JUNCTION.

Leakage resistance, R_L (Ω)	Normal resistance, R_N (Ω)	Gap voltage, Vg (mV) at 4 K	Onset coefficient, a (1/V)
55	0.91	2.91	$4 \cdot 10^4$

C. Lumped single or series array SIS junctions

When designing a frequency multiplier, several properties of the multiplier need to be considered. One of the key properties is the output power at the generated harmonic of interest. Another key parameter is the impedance at the input and at the harmonics frequencies of interest.

With the fixed voltage scale to Vg, the output power of SIS junctions can be assumed to be proportional to the area of the junction [10] for the given tunnel barrier transparency, and N^2 for a series array configuration [1], where N is the number of SIS junctions. However, the SIS junction geometric capacitance is also proportional to the junction area, which limits the SIS junction size, since the higher harmonics would be short-circuited due to the geometric capacitance. This seriously limits the performance of the SIS junction as a frequency multiplier. The solution to this problem is in principle to have several or many junctions in series, which would reduce the junction capacitance and at the same time increase the total output power of SIS junction array by a factor of N^2. Billade et al. [20] employed this approach. However, it seems that this approach raises many new challenges and questions.

The series SIS junction array, even just a few elements must be considered as a distributed array of junction at these frequencies. The reason is that the simplifying assumption regarding the inductance in the equivalent circuit of series SIS junctions array used in [1] is only valid for relatively low frequencies. Consequently, this means that the waveform across all of the SIS frequency multiplier junctions must be considered and simultaneously solved for, in order to account for the impedance due to the junctions themselves and the transmission line inductance in between the junctions. Furthermore, it is also likely that in such arrangement, the first few junctions could be pumped much harder than remaining junctions [20]. This could lead to local (over)heating of the junctions and thus affecting the total performance of SIS multiplier as discussed in [20].

Another drawback with the series array arrangement may be that the power from the PS would be distributed among other harmonics than the expected one in the multiplication chain. This is most likely because the first junction would generate numerous harmonics with different magnitudes as shown in (1) and (2) as a response to the input PS signal; these harmonics are then input to the next junction. At the second junction, there would be both multiplications, up and down conversion of the input signals. The output of the second junction would contain low and high output frequencies with sufficient output power, and these are the input for the following junctions. This would lead to local heating of the junctions and severe degradation of the SIS frequency multiplier efficiency with overall complexity of achieving the optimum performance of all the junctions in the series array.

Obviously, a different option for using SIS junction as frequency multiplier is warranted.

D. The distributed SIS junction

In 1996, Belitsky et al. published an extensive paper regarding the distributed (long) SIS junction and its characteristics [24]. However, in that paper, the reactive portion of the quantum impedance, which is due to the Kramers-Kronig part of the tunnel current was neglected, as commonly done when considering the SIS junction for mixer operation. On the other hand, when the SIS junction is considered for frequency multiplication, it is essential that the reactive portion of the SIS quantum impedance is included [25].

For the modeling, a similar approach as in [24], [26] was employed; the distributed SIS junction is therefore modeled as a microstrip-line (MSL) as shown in Fig.4, where s is the tunnel barrier thickness, W is the strip width, d_s is the thickness of the superconducting counter electrode, d_g is the superconducting ground electrode.

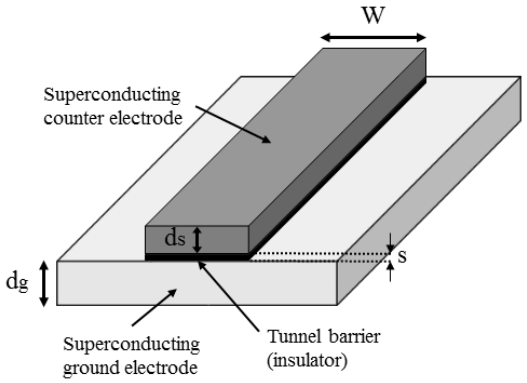

Fig. 4: Topology of the distributed SIS tunnel junction, s is the tunnel barrier thickness, ds and dg are the superconducting counter and ground electrodes respectively, W is the distributed junction width.

The circuit diagram of the presented SIS microstrip line tunnel junction is shown in Fig.5.

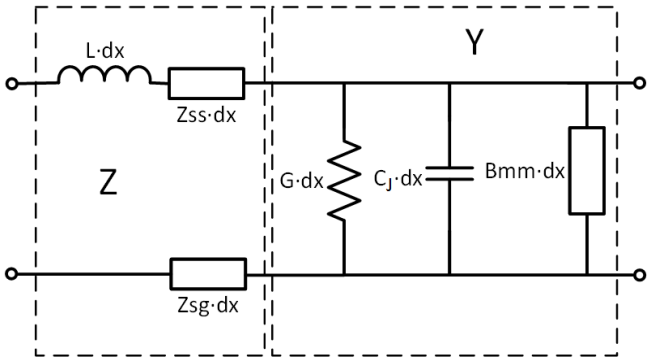

Fig. 5: Circuit diagram for small portion dx of a superconductor-insulator-superconductor tunnel microstrip line. L and C are specific geometrical inductance and capacitance per unit length, whereas Zss and Zsg are the surface resistance of the strip and ground electrode respectively. B_{mm} is reactive part of SIS quantum admittance.

From the circuit diagram, the propagation factor, γ, for a microstrip line with series impedance Z and admittance Y of unit length can be expressed as follows:

$$\gamma = \sqrt{ZY} \tag{9}$$

$$Z = j\frac{\omega \mu_0 s}{W} + \frac{1}{W}\left(Z_{ss} + Z_{sg}\right) \tag{10}$$

$$Y = W \cdot G_{RF} + j\omega W \cdot C_s + jB_{RF} \tag{11}$$

$$C_s = \frac{0.3}{\ln(R_N A)} \quad (12)$$

$$G_{RF} = \frac{G_{mm}}{A} \quad (13)$$

$$B_{RF} = \frac{B_{mm}}{A} \quad (14)$$

where Z_{ss} and Z_{sg} are the surface impedance of the superconducting counter and ground electrodes respectively, C_s is the specific capacitance in pF/μm^2 [27], G_{RF} (Ω μm^2)$^{-1}$ is the conductance of the RF quantum admittance real part that originates from the photon-assisted tunneling current through the barrier per area unit, whereas B_{RF} is the reactive part of the RF quantum admittance per area unit.

The specific surface impedance Z_S per square of a superconducting film with thickness d is expressed as following [26]:

$$Z_s(\omega) = \sqrt{\frac{j\omega\mu_0}{\sigma}}\coth\left(d\sqrt{j\omega\mu_0\sigma}\right) \quad (15)$$

where ω, is the angular frequency, μ_0 is the magnetic permeability of vacuum and σ is the complex conductivity of a superconductor [28]. The specific surface impedance in eq. (15) is calculated in the same fashion as in [24, 26]; the superconducting material parameters for niobium that was used in our modelling could be found in Table II.

In order to study the behavior of SIS microstrip line tunnel junction propagation factor, both the series impedance Z and admittance Y has to be calculated through eq. (5)-(7) and (8)-(10) respectively, which then results in the following expression:

$$\gamma = \sqrt{\left(j\omega\mu_0 s + \left(Z_{ss} + Z_{sg}\right)\right)\cdot\left(G_{RF} + j\omega C_s + jB_{RF}\right)} \quad (16)$$

TABLE II: Nb SUPERCONDUCTING MATERIAL PARAMETERS

London penetration depth (nm)[a]	Gap voltage Vg (mV) at (T=0 K)	Critical temperature Tc (K)	Normal state conductivity $\sigma_n(\Omega^{-1}m^{-1})$
85	*2.86*	*9*	*$1.57\cdot10^7$*

[a]SEE REFERENCE [24].

From eq. (16) it could be seen that the junction capacitance is tuned with the aid of the reactive part of the quantum impedance B_{RF}, hence, changing the propagation factor significantly. In a separate study [29], it was shown that the losses (real part of the propagation factor) in the distributed SIS junction was significantly increased, up to 35% at specific junction parameters and bias voltages as a consequence of the introduction of the reactive portion of the quantum impedance. The impact of the losses on the generated power at the higher harmonics could be introduced through the characteristic impedance of the distributed SIS junction given by eq. (18). A practical configuration of the microstrip line is the open stub, as it results in useful input and output impedance values. The input impedance of an open stub lossy microstrip line is given as following:

$$Z_{in} = Z_0\coth(\gamma l) \quad (17)$$

where l is the length of the distributed SIS junction and Z_0 is the characteristic impedance of the microstrip line SIS junction, given by:

$$Z_0 = \sqrt{\frac{Z}{Y}} \quad (18)$$

where Z and Y is given by (10) and (11) respectively.

From the input impedance plotted in Fig. 6, it can be seen that the impedance values occur periodically, and with values larger than 2 Ohms. This is a very interesting result, showing that the microstrip line SIS junction is not restricted to the generation of only the first or second harmonic of the input signal. It could actually as well be used for the 3rd and 4th harmonics. Furthermore, it can be seen that the input impedance at the lower frequencies ($f < 150$ GHz) is reduced compared to the higher frequencies.

The advantages of the distributed SIS junction are that because of internal resonances the impedance could be pure real and reach reasonably high values but also practical for both large area of the distributed SIS junction and high frequency. Compared to the series SIS array, the distributed (long) SIS junction at resonant frequency would neither suffer from the local heating effect, which would occur due to over pumping in a few junctions, nor would the multiplier have major efficiency degradation due to the propagation of both multiple harmonics and mixing products simultaneously as the series of resonances provide favorable matching for harmonics' signal only.

In conclusion, according to our modelling, the distributed SIS junction, when operated as a frequency multiplier shows considerable advantages over the lumped SIS junction (insufficient attainable power) or a series SIS junction array (heating and complex junction interaction). For this reason, the distributed SIS junction is used as the frequency multiplier in this paper.

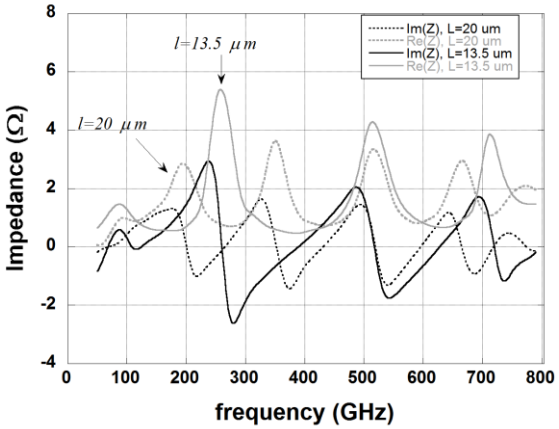

Fig. 6: The complex impedance of the resonant distributed SIS junction for the two different lengths of the junction, *l=20* μm and *l= 13.5* μm at the pumping factor α= 2.

E. Output Power and Efficiency

As it was shown by our earlier publication [30], the reactive part of the QTC has a fundamental impact on the total tunnel current of the SIS junction since it determines the maximum power of the generated harmonic, which is clearly seen in Fig. 2. This also could be understood from eq. (1)-(2), since the reactive QTC is proportional to the real part of the current response function I_{KK}. Therefore, the larger the peak value of I_{KK}, hence the larger the peak value of the reactive current

would be, as shown in Fig. 7. Recall that the peak value of I_{KK}, which occurs at the gap voltage, is shifted by the photon voltage $\pm n\hbar\omega/e$ as shown in eq. (2) when RF signal is applied across an SIS junction. Consequently, the peak powers of the generated signals at higher harmonics are found at the bias voltages of $V_g \pm n\hbar\omega/e$, as seen in Fig. 2. Furthermore, by taking the second derivative of eq. (4) together with the modeled dc QTC expression in eq. (5), it was also shown in [30] that the maximum value of the reactive tunnel current depends strongly on the quality of the SIS junction. Consequently, the normal resistance, R_N should be low, approximately 1-3 Ω so that an practical attainable impedance value is achieved, whereas the leakage resistance, R_L and the onset sharpness coefficient, a, should be as high as possible for practical SIS junctions in order to maximize the reactive tunnel current, thereby maximizing the output power of the SIS junction at the desired harmonic. In fact, the conversion efficiency of the SIS multiplier is strongly dependent on the onset sharpness parameter. This fact emphasizes upon the importance of the SIS junction quality quantified by parameter a, *e.g.*, a 37.5% change of the onset sharpness a, results up to 15 % degradation in the conversion efficiency.

In [1], a simplifying assumption of the PS signal applied to the SIS junction was made in order to attain the expression shown in eq. (7) and (8). It was assumed that the waveform of the PS source at the SIS junction is purely sinusoidal. We believe that this assumption can still be valid if a bandpass (BP) filter is used in front of the SIS junction in order to short out the unwanted harmonics of the PS source. For this reason, the resulting quantum impedance of SIS junction due to this approximation was used to calculate the conversion efficiencies of the SIS frequency multiplier. The conversion efficiency of the 2nd and 3rd harmonics with different pumping factors, α is shown at the Fig.8. The onset sharpness, a used for the plots in Fig. 8, is $2.5\cdot10^4$ (V^{-1}), which is 37.5% lower than the typical value. The exaggerated lower value of the onset sharpness accounts for the possible heating due to the large pumping factor and the power dissipation in the coil used for the suppression of the Josephson effect. Respectively, the peak values of conversion efficiencies shown in Fig.8 would improve by up to 15 % when the typical onset sharpness $a = 4\cdot10^4$ (V^{-1}) is used in the model.

The output power of the distributed SIS junction at the second harmonic is of the order of a few hundreds of nano Watts. In order to increase the output power of the distributed SIS junction, a power combining technique could be used rather than a series array layout for the same reasons as discussed in the Section II-C.

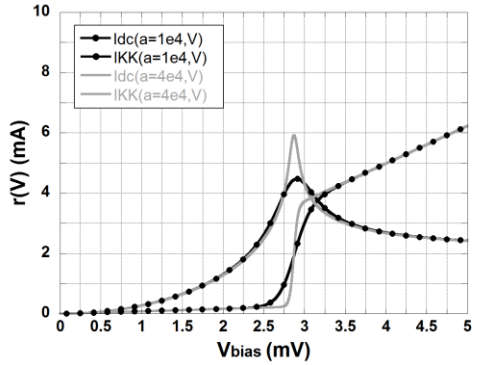

Fig. 7: The I_{KK} current with respect to the bias voltage for junctions with different quality factors (onset sharpness), a.

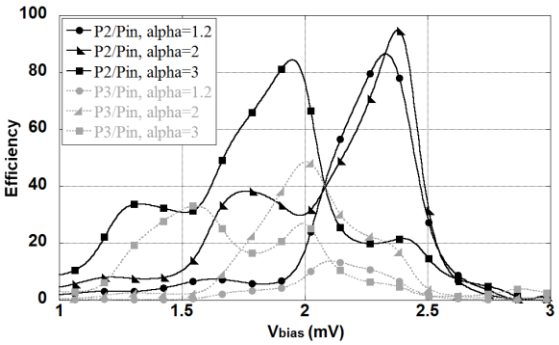

Fig. 8: The conversion efficiency at the 2nd (black curves) and 3rd (gray curves) harmonics three different pumping factors, α=1.2, 2 and 3.

F. Large Signal Model

Accurate analysis of a circuit containing a SIS junction requires a self-consistent large-signal solution for the voltage across the nonlinear device. In the method used here, two realistic simplifications are made; 1: The Josephson effect is not included as it is assumed to be suppressed with external magnetic field; 2: Self-oscillation and other nonharmonic frequency generation effects are ruled out.

The harmonic balance method employed here follows the procedure described by Hicks et al. [31] for SIS mixers. The equivalent circuit diagram used in this analysis is shown in Fig. 9. The circuit diagram is bisected at the linear-nonlinear interface and each half is treated separately. The nonlinear portion of the circuit is modelled in the time domain whereas the embedding network, which includes the surface impedance and the geometrical capacitance of the distributed SIS junction, is treated in frequency domain.

Early results of the harmonic balance simulations confirms the high conversion efficiency from the simplified single tone PS waveform given by equations (1)-(2) and (6)-(8), as discussed and shown in previous section, see Fig.8. The conversion efficiencies for the 2nd harmonic at the pumping factor $\alpha = 1.5$ and $\alpha = 3$ attained with the large signal modeling are 90% and 50% respectively. The conversion efficiencies of the 3rd harmonic for the same pumping factors were approximately 30% and 15% respectively. Furthermore, according to the tunnel current spectrum attained by the large signal model and presented in Fig.10, even higher harmonics such as the 4th or 5th may have sufficiently good multiplication efficiency, for the model based on the given above assumptions.

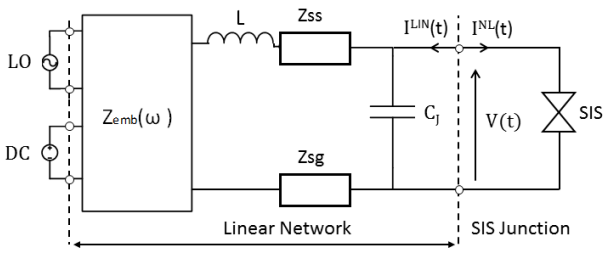

Fig. 9: Distributed SIS multiplier circuit. L and C_J are geometrical inductance and capacitance, whereas Zss and Zsg are the surface resistance of the microstrip and ground electrode respectively.

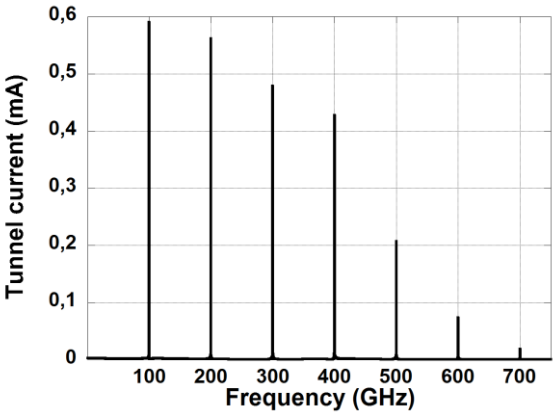

Fig.10: The large signal harmonic spectrum of the induced quasiparticle tunnel current. The pumping frequency signal at 100 GHz is presented along with harmonic tones up to 7th harmonic. It is clearly seen enhanced intensity of the harmonics 2, 3, 4.

However, the limitation of this large signal modeling technique resides in the use of time domain simulations, which could be quite demanding for computation power. However, to our experience, modern computers provide enough computation power to make those time domain simulations affordable. Another limitation seems to be that the dependence of the reactive part of the tunnel current, which is given by the Kramers-Kronig transform of the dc tunnel current in the frequency domain is not that pronounced with respect to the conversion efficiency in the time domain simulations, i.e., the sharper the onset current is, the higher would become the peak power. However, the spectral domain large signal model technique [32], where all the calculations are directly made in the frequency domain, show that the imaginary part of the induced QTC is proportional to the real part of the current response function (i.e., I_{KK}) as suggested in the previous section.

In summary, the distributed SIS junction shows promising potential for high conversion efficiency for frequency multiplication, both in attainable power and multiplication efficiency even at the higher order harmonics.

III. Frequency Multiplier Circuit Design and Fabrication

A prototype frequency Multiplier employing a Distributed Superconducting-insulator-superconductor junction (DSM) was designed and fabricated as shown in Fig. 12. Aiming for enhancing the generated power of the 2nd harmonic, a topology with two DSM in parallel with power combining by a Wilkinson power combiner. The DSM chip was designed for a frequency multiplication factor of two with a WR-10 input (3-mm band), resulting in the frequency output in WR-5 (1.5-mm band). The reason for choosing this particular frequency band was the availability of the metrology, and, in particular, a 163–211 GHz SIS mixer [33] intended to be used to study the generated signals.

The DSM chip consists of two waveguide to microstrip transitions (also referred to as probes), two impedance transformers, two Wilkinson power dividers, two bandpass (BP) filters and two distributed SIS multipliers as schematically shown in Fig. 11. Furthermore, the DSM chip employs a choke structure on the top of a 60 μm high resistivity silicon substrate used as the ground for the entire circuitry. As the insulation for various microstrip structures we used a 0.2 μm SiO_2 dielectric layer.

Fig. 13 shows a photograph of the multiplier waveguide block with an E-plane split. The DSM chip is placed inside a chip channel and the coupling between the PS and the generated second harmonic signal in waveguides and the chip is achieved using E-probes extending inside the waveguides. For the pumping frequency side, a radial probe as described in [34] was used, whereas, for the high-frequency side, a probe with integrated bias-T [35] was used to allow the dc biasing of the DSM. An SMA connector was employed for dc biasing the DSM, where the SMA center pin was soldered to an intermediate dc substrate. The dc substrate was then connected to the DSM chip using bond wires. The choke structure was dc grounded by connecting one bond wire on each side of the low impedance section directly to the waveguide block, as shown in Fig. 12. The BP filters are used to isolate the input and output from each other and at the same time filter out unwanted possible harmonics of the pumping signal, whereas the Wilkinson divider and combiner are used for the parallel DSM operation in order to increase the total output power. From Fig.12, it can be seen that the silicon substrate is tapered to a smaller substrate width from approximately the center i.e., right after the distributed SIS junctions. The reason is that after the multiplication of the input signal, all dimensions of the choke structure scales with the frequency, i.e., the choke structure needs to be scaled accordingly for normal operation at the output frequency.

The input and output impedance of the distributed Nb-AlO_x-Nb SIS junction, which is 1 μm wide, 20 μm long and $R_NA = 30$ Ohm·μm² was calculated as shown in section II-D. The input impedance at 93 GHz was $Z_1 \approx 1+j0.3\ \Omega$ whereas the impedance at the second harmonic i.e., 186 GHz is $Z_2 \approx 2.3\ \Omega$. The input and output circuit chains in the DSM chip were optimized with respect to the input and output impedance, i.e., Z_1 and Z_2. The optimization procedure was carried out in Keysight EMPro, ADS and Momentum [36]. Furthermore, all microstrip lines were made of superconducting niobium in order to minimize the loss in the microstrip lines due to finite conductivity and non-zero operating temperature [26]. Notice that in this case, the loss of the superconductor arises when high-frequency magnetic field penetrates a thin surface layer and induces oscillations of the electrons which are not bound in Cooper pairs. Therefore, the power dissipation caused by the motion of the unpaired electrons [37]. Furthermore, the characteristic impedance and lengths of all circuit elements has to be corrected due to the added kinetic inductance of the superconducting transmission line. Detailed description and closed form expression for both characteristic impedance and propagation factor could be found in [38].

Fabrication of the DSM chips generally followed the process flow described in [23]. The Nb/Al–AlO_x/Nb trilayer was grown in a single vacuum run by means of dc magnetron sputtering. The patterns of the layers forming the DSM circuitry were defined by contact photolithography. The bottom Nb electrode, 200 nm thick, was deposited at 0.9 nm/s rate followed by about 7 nm Al deposited at 0.3 nm/s rate. The fresh Al surface was exposed to pure oxygen at room temperature and at a pressure of $6.9 \cdot 10^{-2}$ mbar for 15 min to

form the AlO_x tunnel barrier. Finally, 100 nm thick Nb counter electrode was deposited under the same conditions as the bottom electrode. The base electrode pattern has been etched through the Nb/Al–AlO_x/Nb trilayer by a sequence of CF_4 +O_2 for Nb and Cl_2 for Al–AlO_x reactive ion etching (RIE), correspondingly. The junction pattern was defined by RIE process with a stop at Al–AlO_x layer. Anodization with voltage up to 13 V was followed by a deposition of 200 nm thick SiO_2 by means of reactive RF magnetron sputtering; the SiO_2 layer was lifted-off forming interlayer insulation. Another SiO_2 layer of 150 nm thickness was consequently deposited and defined by lift-off forming locally areas where thicker SiO_2 layer was required by the DSM design. Layer of Ti-N alloy with a sheet resistance of 11.5 Ohm/square had been formed by reactive magnetron sputtering of Ti target in Ar and N_2 atmosphere and its shape was defined by lift-off. A 350 nm thick Nb lines layer was deposited by dc sputtering and followed by RIE. Finally, the contact pads were formed by lift-off of the Nb 100 nm / Pd 150 nm bilayer.

The DSM device was designed to be made on as thin as 60 μm Si substrate. For easier handling during the DSM SIS thin film processing, it was carried out on the silicon-on-insulator (SOI) wafer with 60 μm thick device and 550 μm thick carrier parts of the wafer. Upon the DSM SIS processing was completed and dc testing of the fabricated circuits proved their suitability for the measurements, the individual chips shape was formed by etching down in the device layer of the SOI wafer and, consequently, the carrier part of the SOI wafer was etched away, both following the process described in [39].

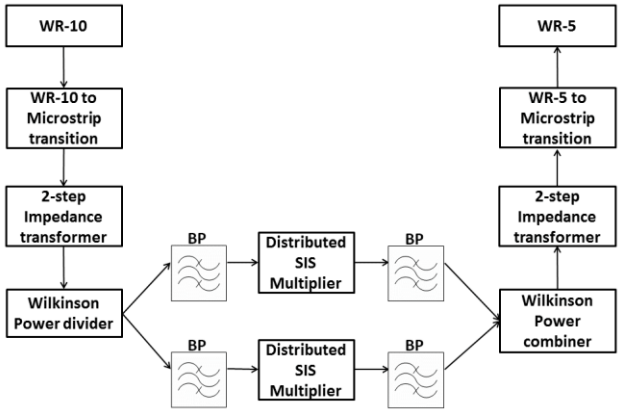

Fig. 11. Block diagram overview of the DSM test chip.

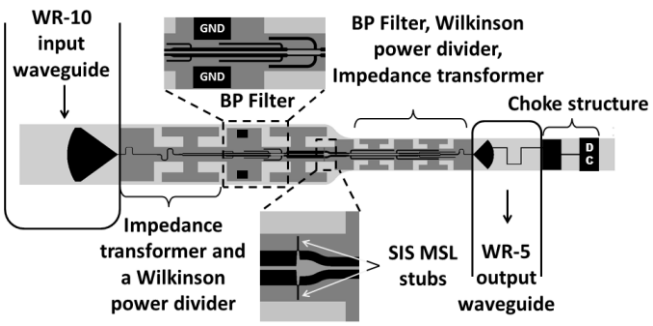

Fig. 12: The CAD drawing of the test chip showing the two distributed SIS stub junctions in parallel, two filter sections, the input and the output probes together with respective waveguides. The dc bias and choke structure ground (GND) ports are shown as well. Each distributed SIS junction is 1 μm wide and 20 μm long.

IV. Measurements and Results

A. Measurement Setup

The characterization of the device performance was carried out at 4 K in a cryostat with a closed-cycle refrigerator similar to [20]. Fig. 14 shows a block-diagram of the test setup used for the DSM measurements. To study the response from DSM, an SIS mixer [33] that covers the RF frequencies from 163–211 GHz with 4–8 GHz intermediate frequency (IF) bandwidth, was connected at the output of DSM . The DSM was pumped with a phase locked 83-105 GHz Gunn oscillator through a WR-10 waveguide, and the output of the DSM was coupled to the input of the mixer using a 3 cm long WR-5 waveguide.

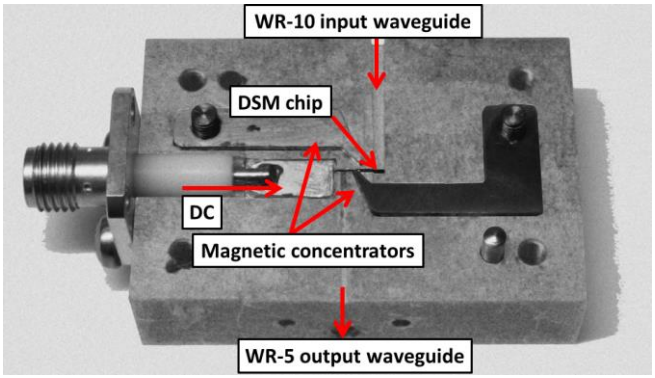

Fig. 13: Photograph of the multiplier assembly showing input and output waveguide, SMA connector for dc biasing and location of the DSM chip.

In this experiment, the Josephson effect for both the SIS mixer and DSM were suppressed using two independent magnetic coils. An isolator and a cryogenic low-noise amplifier were used at the output of the SIS mixer. The SIS mixer was pumped using a 171-203 GHz LO consisting of an Agilent frequency synthesizer and followed by a amplifier / multiplier chain (×6) [40]. The IF output was analyzed with a spectrum analyzer.

In order to investigate the spectral response of the DSM, the LO frequency of the SIS mixer used for this purpose was set between 174–203 GHz, and the DSM was pumped with frequencies such that the expected DSM output power at the second harmonic would always fall inside the 4–8 GHz band of the down converted mixer IF. All measurements were performed using specially developed data acquisition software.

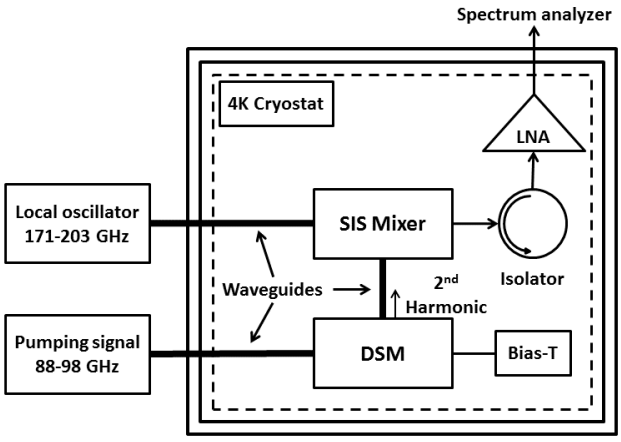

Fig. 14: Schematic of the experimental setup used to study the test device. The cryostat contains the DSM test chip connected through a WR-5 waveguide to a 163–211 GHz SIS mixer. Both the SIS mixer and the DSM test chip are pumped using two separate local oscillators

B. DSM Output Power

The physical parameters of the SIS (Nb-AlOx-Nb) junction such as gap voltage (V_g), normal resistance (R_N) and subgap resistance (R_L) were calculated from the measured dc I-V characteristics, see Fig. 1. The fitting parameter, *a*, which is associated with quasiparticle tunnel current onset sharpness in equation (3) was also estimated from the measured dc I-V characteristic. These parameters were implemented in equation (3) and (2) for *m=0* in order to extract the pumping factor. Here, we used a simple extraction procedure of the pumping factor, were we compared the modeled and measured pumped dc I-V characteristics of the DSM. The pumping factor in the model is adjusted until satisfactory agreement between the model and the measurement was achieved, see Fig. 15.

The output power dependence of the frequency multiplier on the dc bias voltage was investigated by measuring the IF power of the SIS mixer while sweeping the DSM bias voltage. In this case, both the frequency and the output power of the two sources used for the SIS mixer (LO) and the DSM (PS) test chips respectively were fixed. The process was repeated for different pumping factors. A comparison between the measured and the predicted power at the second harmonic is shown in Fig. 16, where the amplification of the LNA and cable losses are accounted for. The comparison is made for a typical power response of the DSM test chip at 93 GHz and a pumping power of α≈3. The predicted output power at the second harmonic was estimated by $P = 0.5Re(Z_2)|I_{RF}|^2$, the impedance Z_2 being calculated as shown in section II-D, whereas the induced QTC, I_{PS} is calculated using eq. (1) and (2). The modeled and measured power are in good correspondence for the extracted pumping factor especially taking into consideration that the modeling did not accounted changes in the pumping power delivered to the junction vs. dc bias. The peak values of the modeled and measured power at $V - n\hbar\omega_{RF}/e$ were almost identical between the measured and the simulated curves, see Fig. 16. Furthermore, it can be seen that all the fine structure of the theoretically predicted curve (equation (1)-(2)) could be found in the measured data. The fine structures in Fig. 16 are separated exactly by the voltage corresponding to the multiple of the applied LO photon size. Thereby, Fig. 16 clearly shows the presence of the multi-photon processes. The peak power vs. the frequency at the second harmonic, which corresponds to a fractional band width of 10%, is shown in Fig. 17. There is a minor deviation close to the gap voltage between the model and the measurement data in Fig. 16. Furthermore, the measured power response seems to be slightly wider than predicted by the model. In our model, a constant pumping factor was assumed for all dc bias points, whereas in reality, the pumping factor varies depending on the bias voltage because of the DSM changing impedance. This explanation was tested in our model by splitting the pumped dc I-V in to three sections, were the pumping factor for each section was extracted separately. In this case, the modelled output power at the second harmonic with the new pumping factors proved to give even better agreement between model and measurement than shown in Fig. 16. However, at this stage, the constant pumping for the entire I-V employed in order to avoid a figure containing stitched plots. Additionally, some discrepancy could also be attributed to the possible limitations of measurement setup itself. Nonetheless, the measured power of the second harmonic shown in Fig. 16 is in a good agreement with the theoretically predicted power and corresponds to the features predicted by the model attributed to the contribution from the I_{KK} as discussed in section II-F.

C. Efficiency

During the same experiment, we were also able to demonstrate pumping of the SIS mixer only with the output signal of the DSM test chip. In this case, the LO power of the SIS mixer (LO of the down converter at the Fig.14) was switched off and the DSM was biased at the maximum power at the pumping factor α≈3. Once, the DSM parameters were set, a bias voltage sweep of 0-3.4 mV of the SIS mixer and the measurement was conducted. The pumped dc I-V characteristic of the SIS mixer is shown in Fig. 18. The un-pumped SIS mixer current at 2.5 mV bias voltage was approximately 1 μA, whereas the pumped SIS mixer current was approximately 25 μA. The pumping factor, α_{mix}, of the SIS mixer driven by the output signal of the DSM test chip was estimated with the same iteration method as described earlier in the Section IV-B, which resulted in the value $\alpha_{mix} \approx 0.35$. Even though a higher output power is desired for normal operation of an SIS mixer ($\alpha_{mix} \approx 0.8$-1) this shows potential possibility to use DSM as a part of practical receiver. It should be noted though that the conditions of the test setup are not fully optimum for achieving maximum pumping factor at the mixer. Since the DSB was placed onto a separate chip and employed dedicated waveguide mount. For the purpose of assessing the power of the second harmonic generated by DSM, we should include losses as the output signal travels through a BP filter, Wilkinson power combiner, impedance transformer, waveguide probe and roughly 6 cm long WR-5 waveguide in total with two flanges until it arrives to the input of the SIS mixer block. Inside the SIS mixer block the signal continues to travel 3 cm before it arrives to the waveguide to microstrip probe, which is then impedance transformed and connected to a SIS mixer through a LO coupler [4]. The input and output power of the DSM was estimated by using the extracted pumping factor related to the DSM chip at the input frequency and the pumping factor related to the SIS mixer at the output frequency. Furthermore, by taking into account the losses of the high frequency superconducting microstrip line as shown in [26], and accounting for various mismatch as shown in Table III, we were able to make an estimation of the DSM efficiency to be at 15-30%. This indicates that the output power at the DSM is 4.3-7.4 dB or 2.7 to 5.5 times higher than the measured power at the SIS mixer junction.

The estimated from the measurements efficiency of the SIS junction frequency multiplier of 15-30% is reasonably close to the modelled perfectly matched DSM at 200 GHz, which is close to 50% according to the large signal model. Furthermore, it is seen from the modelling in section II-D that the DSM input impedance at 100 GHz is approximately 1 Ω, whereas the output impedance is 2.3 Ω. The efficiency calculated with $\eta = P_2/P_1 = Re(Z_1)|V_2|^2/Re(Z_2)|V_1|^2$ show that the input and output impedance ratio is approximately 43% for the DSM input pumping frequency of 100 GHz, whereas the impedance ratio is 125% for the input frequency at 300 GHz (see the impedance curve for 13.5 μm long distributed junction in Fig. 8). This indicates that the efficiency at higher frequencies should be expected to be greater than 15-30 %. Furthermore, the output of the DSM chip could be further increased by combining the power of more DSM junctions.

Furthermore, the results demonstrated here open up possibility of the DSM integration with the SIS mixer in order to maximize the power transmission from the DSM to the SIS mixer. This technology show future potential as LO source especially for multi-pixel SIS mixer layout.

D.Spectral Width

One of the most important requirements on any frequency multiplier is that it preserves the spectral purity of the input signal.

The spectral line-width of the multiplied signal was measured with the resolution and video bandwidth of the spectrum analyzer set to 1 Hz (lowest value the spectrum analyzer could set) and 10 Hz respectively. Furthermore, during the measurement, the Gunn oscillator (signal to DSM) was phase locked. The -3dB line-width of the output signal was found to be 1 Hz. Fig. 19 shows the power spectrum of the multiplied signal. The spectrum is centered at 6 GHz with a 2 kHz span and resolution bandwidth of 20 kHz. Furthermore, for careful investigations, we could determine that the spurious in Fig. 19 originates from the LO signal to the SIS mixer.

TABLE III: LOSS AND MISMATCH BETWEEN DSM AND SIS MIXER

Circuits	Loss
Two WR-5 Probes	0.5-0.9 dB
Two Filters	0.7-1.1 dB
Wilkinson Power combiner	0.5-1.0 dB
Two 2-Section impedance transformers	0.6-1.2 dB
Thickness discontinuity in the choke structure SiO2 dielectric	0.2-0.4
Total Waveguide distance	1.5-1.8 dB
LO coupler in the SIS mixer block	0.3-1 dB
Total Loss	**4.35-7.4 dB**

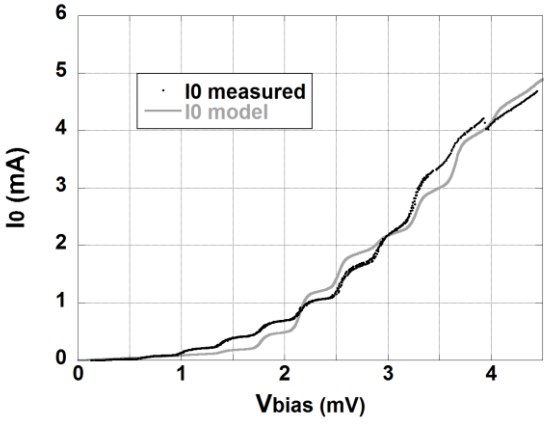

Fig. 15: The pumped dc DSM is compared with the model. The pumping factor in the model is adjusted until satisfactory agreement between model and measurement is achieved. The pumping factor in this plot is $\boldsymbol{\alpha \approx 3}$. Discrepancy was caused by varying the pumping factor while changing the dc bias and consequently the matching impedance of the DSM.

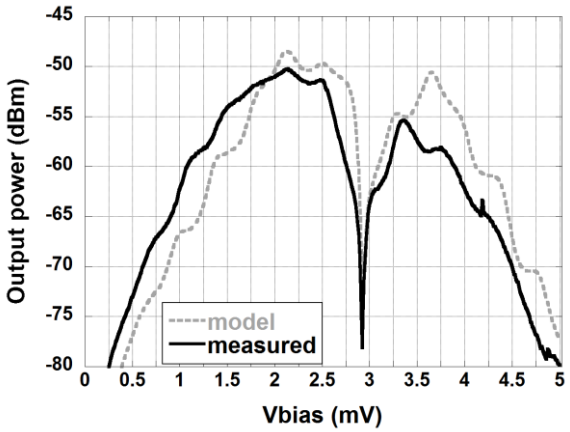

Fig. 16: A comparison of the measured and predicted power at the 2nd harmonic i.e., 186 GHz (93 GHz input frequency) vs. bias voltage and pumping factor $\boldsymbol{\alpha \approx 3}$. The peak powers are due to the real part of current response function, i.e., I_{KK}. The figure shows excellent correspondence between model and measurement. Furthermore, contribution of the IF amplification chain is removed here. The measured power is also corrected with 5.85 dB, which corresponds to the average value of the estimated losses in table III.

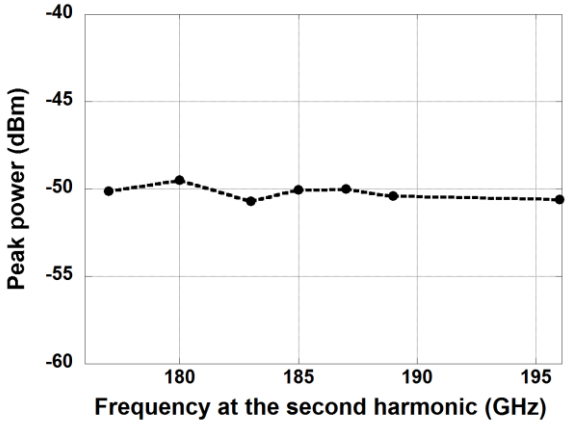

Fig. 17: The peak power vs the frequency at the second harmonic over a fractional bandwidth of 10%.

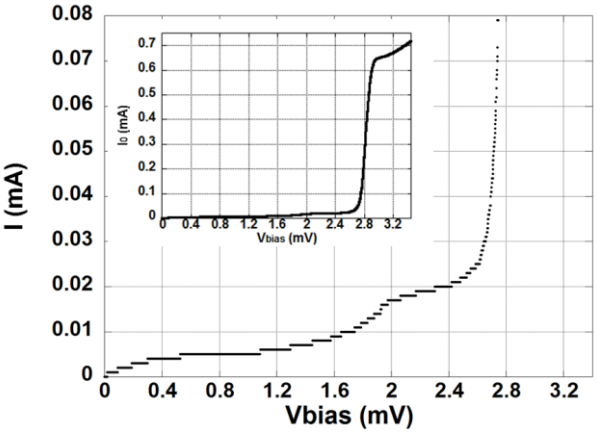

Fig. 18: Pumped dc I-V characteristics of the SIS mixer. The zoomed plot clearly shows the quantum response of the SIS mixer for the output power of the DSM at twice the input frequency i.e., at 186 GHz. The step-structure of the zoomed IVC is due to limitation of data acquisition system (steps show the last digit of the current ADC).

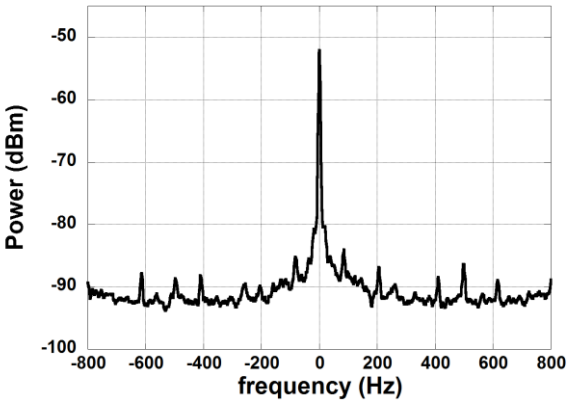

Fig. 19: The spectrum is centered at 6 GHz with a 2 kHz span and resolution bandwidth of 100 Hz.

V. Conclusions

In this paper, we have introduced, modelled, designed and experimentally demonstrated for the first time a frequency multiplier using a distributed (long) SIS junction. We have presented analytical expressions describing the properties of such distributed SIS junction. The modeling of the device shows that the distributed SIS junction can achieve high conversion efficiency, which was consistent with large signal harmonic balance simulations of the SIS junction multiplier. The measured output power of the distributed SIS junction in the regime of the generated second harmonic is in good agreement with the modeled output power. Furthermore, the distributed SIS junction as a frequency multiplier was for the first time able to pump an SIS mixer. The efficiency of the distributed SIS junction is estimated to be 15-30 % for a fractional bandwidth of 10% with excellent spectral line purity. The -3 dB line width of the multiplied signal is 1 Hz, which was limited by the lowest resolution bandwidth of the spectrum analyzer. The results presented in this work show that the distributed SIS junction frequency multiplier has potential to become useful component in LO source of superconducting low-noise single-end receivers, SIS and HEB, and possibly be used in multi-pixel receivers.

Acknowledgment

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