Thesis for the degree of Licentiate of Engineering

Vertical-Cavity Surface-Emitting Lasers: Large Signal Dynamics and Silicon Photonics Integration

Emanuel P. Haglund

Photonics Laboratory
Department of Microtechnology and Nanoscience – MC2
Chalmers University of Technology
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Emanuel P. Haglund

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Photonics Laboratory
Department of Microtechnology and Nanoscience – MC2
Chalmers University of Technology
SE-412 96 Göteborg
Sweden
Telephone: +46 (0)31-772 1000

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Emanuel P. Haglund
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Chalmers University of Technology, SE-412 96 Göteborg, Sweden

Abstract

The GaAs-based vertical-cavity surface-emitting laser (VCSEL) is the standard light source in today's optical interconnects, due to its energy efficiency, low cost, and high speed already at low drive currents. The latest commercial VCSELs operate at data rates of up to 28 Gb/s, but it is expected that higher speeds will be required in the near future.

One important parameter for the speed is the damping of the relaxation oscillations. A higher damping is affordable at low data rates to reduce signal degradation due to overshoot and jitter, while lower damping is required to reach higher data rates. A VCSEL with the damping optimized for high data rates enabled error-free transmission at record-high data rates of 57 Gb/s over 1 m optical fiber, 55 Gb/s over 50 m optical fiber, and 43 Gb/s over 100 m optical fiber.

For future interconnect links it is of interest with tighter integration between the optics and the silicon-based electronics. Employing heterogeneous integration techniques to integrate GaAs-based VCSELs on silicon could potentially enable integrated multi-wavelength VCSEL arrays, thus increasing the data rate through parallelization. Heterogeneous integration of GaAs-based VCSELs would also benefit applications that need short-wavelength light sources, such as photonic integrated circuits for life sciences and biophotonics. By employing ultra-thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) bonding we have demonstrated silicon-integrated short-wavelength hybrid-cavity VCSELs with up to 1.6 mW optical output power, with modulation bandwidth of 11 GHz and capable of data transmission at data rates up to 20 Gb/s.

Keywords: Heterogeneous integration, high-speed modulation, large signal modulation, laser dynamics, optical interconnects, semiconductor lasers, silicon photonics, vertical-cavity surface-emitting laser (VCSEL).

List of Papers

This thesis is based on the following appended papers:

[A] P. Westbergh, **E. P. Haglund**, E. Haglund, R. Safaisini, J. S. Gustavsson, and A. Larsson, "High-speed 850 nm VCSELs operating error free up to 57 Gbit/s," *Electronics Letters*, vol. 49, no. 16, pp. 1021–1023, Aug. 2013.

[B] **E. P. Haglund**, P. Westbergh, J. S. Gustavsson, and A. Larsson, "Impact of damping on high-speed large signal VCSEL dynamics," *Journal of Lightwave Technology*, vol. 33, no. 4, pp. 795–801, Feb. 2015.

[C] **E. P. Haglund**, S. Kumari, P. Westbergh, J. S. Gustavsson, G. Roelkens, R. Baets, and A. Larsson, "Silicon-integrated short-wavelength hybrid-cavity VCSEL," *Optics Express*, vol. 23, no. 26, pp. 33 634–33 640, Dec. 2015.

[D] **E. P. Haglund**, S. Kumari, P. Westbergh, J. S. Gustavsson, R. G. Baets, G. Roelkens, and A. Larsson, "20-Gb/s modulation of silicon-integrated short-wavelength hybrid-cavity VCSELs," *IEEE Photonics Technology Letters*, vol. 28, no. 8, pp. 856–859, Apr. 2016.

Related publications and conference contributions by the author not included in the thesis:

Journal papers

[E] E. Haglund, P. Westbergh, J. S. Gustavsson, **E. P. Haglund**, A. Larsson, M. Geen, and A. Joel, "30 GHz bandwidth 850 nm VCSEL with sub-100 fJ/bit energy dissipation at 25–50 Gbit/s," *Electronics Letters*, vol. 51, no. 14, pp. 1096–1097, Jul. 2015.

[F] E. Haglund, P. Westbergh, J. S. Gustavsson, **E. P. Haglund**, and A. Larsson, "High-speed VCSELs with strong confinement of optical fields and carriers," *Journal of Lightwave Technology*, vol. 34, no. 2, pp. 269–277, Jan. 2016.

Conference presentations and papers

[G] E. Haglund, P. Westbergh, **E. P. Haglund**, R. Safaisini, J. Gustavsson, K. Szczerba, Å. Haglund, and A. Larsson, "850 nm datacom VCSELs for higher-speed and longer-reach transmission", *European VCSEL Day*, Lausanne, Switzerland, Jun. 2013.

[H] **E. P. Haglund**, P. Westbergh, E. Haglund, J. S. Gustavsson, and A. Larsson, "High-speed 850-nm VCSELs operating error-free beyond 50 Gbit/s," *Optics and Photonics in Sweden*, Uppsala, Sweden, Oct. 2013.

[I] E. Haglund, R. Safaisini, Å. Haglund, P. Westbergh, **E. P. Haglund**, J. S. Gustavsson, and A. Larsson, "Quasi-single mode VCSELs for longer-reach multimode fiber optical interconnects", *Summer School on Optical Interconnects*, Thessaloniki, Greece, Jun. 2014.

[J] **E. P. Haglund**, P. Westbergh, J. S. Gustavsson, and A. Larsson, "Optimum damping level for high-speed large signal VCSEL modulation," *Optics and Photonics in Sweden*, Göteborg, Sweden, Nov. 2014.

[K] **E. P. Haglund**, P. Westbergh, J. S. Gustavsson, and A. Larsson, "Impact of damping on large signal VCSEL dynamics," in *IEEE International Semiconductor Laser Conference*, Palma de Mallorca, Spain, Sept. 2014, pp. 78–79.

[L] S. Kumari, J. S. Gustavsson, R. Wang, **E. P. Haglund**, P. Westbergh, D. Sanchez, E. Haglund, Å. Haglund, J. Bengtsson, N. Le Thomas, G. Roelkens, A. Larsson, and R. Baets, "Integration of GaAs-based VCSEL array on SiN platform with HCG reflectors for WDM applications," in *Proceedings of SPIE*, vol. 9372, San Francisco, CA, USA, Feb. 2015, Paper 93720U.

[M] A. Larsson, P. Westbergh, J. S. Gustavsson, E. Haglund, and **E. P. Haglund**, "High speed VCSELs and VCSEL arrays for single and multicore fiber interconnects," in *Proceedings of SPIE*, vol. 9381, San Francisco, CA, USA, Feb. 2015, Paper 93810D.

[N] E. Haglund, P. Westbergh, J. S. Gustavsson, **E. P. Haglund**, A. Larsson, M. Geen, and A. Joel, "High speed 850 nm VCSEL with 30 GHz modulation bandwidth," in *European Conference on Lasers and Electro-Optics*, Munich, Germany, Jun. 2015, Paper CB-2.4.

[O] **E. P. Haglund**, S. Kumari, P. Westbergh, J. S. Gustavsson, G. Roelkens, R. Baets, and A. Larsson, "Silicon-integrated 850-nm hybrid-cavity VCSEL," *Optics and Photonics in Sweden*, Stockholm, Sweden, Oct. 2015.

[P] **E. P. Haglund**, S. Kumari, P. Westbergh, J. S. Gustavsson, G. Roelkens, R. Baets, and A. Larsson, "Dynamic properties of silicon-integrated short-wavelength hybrid-cavity VCSEL," in *Proceedings of SPIE*, vol. 9766, San Francisco, CA, USA, Feb. 2016, Paper 976607.

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Emanuel P. Haglund

Göteborg
May 2016

List of Abbreviations

4-PAM	4-level pulse amplitude modulation
BCB	benzocyclobutene
BER	bit error rate
BTJ	buried tunnel junction
CMOS	complementary metal-oxide-semiconductor
DBR	distributed Bragg reflector
DVS-BCB	divinylsiloxane-bis-benzocyclobutene
FEC	forward error correction
FIB	focused ion beam
GSG	ground-signal-ground
HCG	high-contrast grating
HPC	high performance computer
HVCL	hybrid vertical-cavity laser
ICP	inductively coupled plasma
MOCVD	metal-organic chemical vapor deposition
OOK	on-off keying
PCE	power conversion efficiency
PECVD	plasma-enhanced chemical vapor deposition

PIC	photonic integrated circuit
PRBS	pseudo random bit sequence
QW	quantum well
RIE	reactive ion etching
RT	room temperature
S_{21}	small signal modulation response
SCH	separate confinement heterostructure
SEM	scanning electron microscope
SiN	silicon nitride
SiP	silicon photonics
SOI	silicon-on-insulator
VCSEL	vertical-cavity surface-emitting laser
VNA	vector network analyzer
VOA	variable optical attenuator
WDM	wavelength division multiplexing

Contents

Chapter 1

Introduction

Today's lifestyle takes the connection to the Internet for granted. Connecting with friends and family through social networks, storing photographs, as well as streaming music and movies are just a few of the things we do online. Commonly this is referred to as cloud computing, as we use our smartphones, tablets, and computers etc. as terminals, while the actual processing and storage of the data is handled by huge data centers [1]. Since the computational capacity of a single computer is far from enough, these data centers consists of large amounts of interconnected servers, to provide simultaneous computing in the servers [2]. The parallelization technique has also been employed to build powerful high performance computers (HPCs). An example is the world's fastest (as of May 2016) supercomputer Tianhe-2, that has over three million cores [3].

Previously the interconnects have employed electrical copper cables, but the increasing amount of data transfer has forced the move to optical interconnects, due to the higher data rates, longer reach, and lower power consumption enabled by optical links [4]. The typical light source in such optical interconnects is the directly modulated GaAs-based vertical-cavity surface-emitting laser (VCSEL), due to its low-cost fabrication, energy-efficient operation, and high bandwidth at low drive currents [5]. Commercial VCSELs capable of data rates up to 28 Gb/s are currently available from several manufacturers [6]. However, data rates of 40, 50, and even 100 Gb/s are expected in future standards, which will require even faster VCSELs.

To date, most of the optical interconnects ranges from a few meters up to a few hundred meters, but the majority of the links are below 30 m. In the future it is expected that even shorter links, e.g. board-to-board and chip-to-chip

interconnects, would benefit from the higher speed and efficiency of the optical interconnects. However, this requires tighter integration between the electrical and the photonic integrated circuits (PICs) for feasible operation. Since the material of choice for electrical circuits, silicon, cannot be used to produce efficient light sources, one possible route is heterogeneous integration of GaAs-based VCSELs on a silicon-based platform for PICs, compatible with standard complementary metal-oxide-semiconductor (CMOS) fabrication. Integration of GaAs-based VCSELs to such PICs would also benefit applications that require a short-wavelength light source, such as life sciences and biophotonics, where for example the presence of biological substances could be detected using microresonators.

1.1 State-of-the-Art

Significant progress has been made the last few years on increasing the bandwidth and data rates possible for directly modulated GaAs-based VCSELs. In 2007 researchers at NEC demonstrated 1100-nm VCSELs with 24 GHz bandwidth capable of transmitting data rates up to 40 Gb/s [7]. A few years later in 2011 researchers at TU Berlin demonstrated 980-nm VCSELs operating up to 44 Gb/s. In 2013, 850-nm VCSELs developed at Chalmers with 28 GHz bandwidth [8] could support data rates up to 57 Gb/s at room temperature (RT, Paper A) and 40 Gb/s at 85°C [9]. By employing driver and receiver circuits with equalization these VCSELs could transmit data rates up to 71 Gb/s at 28°C and 50 Gb/s at 90°C [10, 11]. In 2014, researchers at TU Berlin demonstrated 980-nm VCSELs operating up to 50 Gb/s at 25°C and 46 Gb/s at 85°C [12]. Even more recently, the latest generation of VCSELs from Chalmers demonstrated bandwidths of up to 30 GHz and energy dissipation of less than 100 fJ/bit up to 50 Gb/s [13].

Heterogeneous integration of InP-based VCSELs on silicon was first demonstrated using optical pumping below RT [14], while electrically pumped VCSELs with almost 1 mW output power and enabling data rates up to 5 Gb/s were demonstrated recently [15]. In Paper C we demonstrate heterogeneously integrated GaAs-based VCSELs on silicon with output powers up to 1.6 mW at 25°C. These VCSELs were shown to support data rates up to 20 Gb/s (Paper D).

1.2 Outline of Thesis

The thesis is organized as follows. Semiconductor lasers, and in particular VCSELs, are introduced in Chapter 2, while silicon photonics integration of VCSELs is discussed in Chapter 3. The dynamics of VCSELs are presented in Chapter 4, while the high-speed measurement techniques used for characterization are presented in Chapter 5. Chapter 6 describes the VCSEL fabrication processes, and finally a future outlook is given in Chapter 7.

Chapter 2

Semiconductor Lasers

Laser is an acronym for light amplification by stimulated emission of radiation. Amplification (or gain) is achieved by a quantum mechanical process that allows a photon to stimulate the deexcitation of an excited electron from a higher to a lower energy state if the photon energy corresponds to the energy difference between the two states. When the electron is deexcited a copy (same frequency, phase, and direction) of the stimulating photon is emitted. A laser also needs optical feedback (even though it is not indicated in the acronym), which is typically achieved by inserting the gain medium in an optical resonator (or optical cavity) consisting of semitransparent mirrors. Lasing will occur if sufficient energy is supplied to the gain medium within the cavity.

To achieve lasing two criteria have to be met. The gain should be sufficient to compensate for all optical losses in the cavity (internal and mirror losses) and the phase of the field must repeat itself after one round-trip. The threshold material gain needed for lasing to start is given by

$$g_{\mathrm{th}} = \frac{1}{\Gamma}\left[\alpha_{\mathrm{i}} + \alpha_{\mathrm{m}}\right] = \frac{1}{\Gamma}\left[\alpha_{\mathrm{i}} + \frac{1}{2L}\ln\left(\frac{1}{R_1 R_2}\right)\right], \tag{2.1}$$

where $\Gamma = V_{\mathrm{a}}/V_{\mathrm{p}}$ is the optical confinement factor (i.e. the overlap between the active region and the optical field, where V_{a} is the volume of the active region and V_{p} is the lasing mode volume), α_{i} and α_{m} are the internal and mirror losses, respectively, L is the cavity length, and R_1 and R_2 are the mirror power reflectivities. In a semiconductor laser the gain is provided by transitions across the bandgap, from conduction band states to valance band states. The bandgap energy will therefore determine the wavelength (or color) of the output light. The active region of a semiconductor laser is typically an

intrinsic region sandwiched between p- and n-doped material that are designed to have higher bandgap than the intrinsic active material, which provides confinement of the carriers to the active region. By injecting carriers (electrons and holes) they accumulate in the active region. The injected current needed to reach the threshold gain in (2.1) is called the threshold current I_{th}.

The phase condition on the other hand is given by

$$\exp\left(-\mathrm{j}\frac{2\pi}{\lambda_0/n_{\text{eff}}}\cdot 2L\right)=1 \quad \Rightarrow \quad \lambda_0=\frac{2Ln_{\text{eff}}}{m}, \tag{2.2}$$

where λ_0 is the lasing wavelength (in vacuum), n_{eff} is the effective refractive index of the cavity, and m is an integer number.

The simplest possible semiconductor laser is the Fabry-Perot laser, which is an edge-emitting laser. The reflections at the cleaved facets, due to the high refractive index contrast between semiconductor material and air, give enough feedback to achieve lasing together with the high gain over a relatively long distance along the cavity.

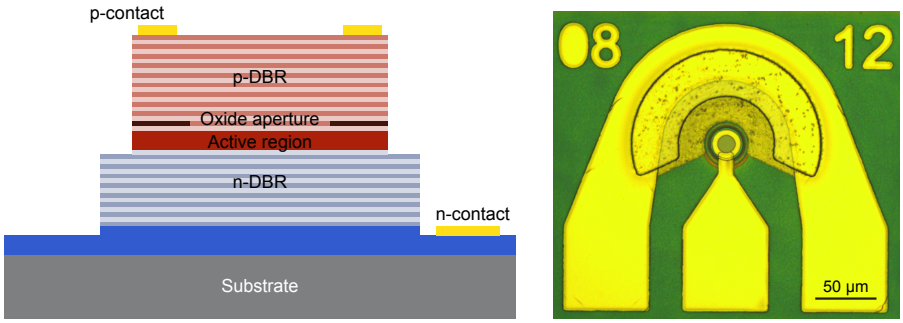
2.1 VCSELs

The first experimental demonstration of a laser by Maiman in 1960 [16] was quickly followed by the first semiconductor laser in 1962 [17] by Hall et. al. However, it was not until 1979 (almost 20 years later) the group of Iga demonstrated the first vertical-cavity surface-emitting laser (VCSEL) [18].

2.1.1 Mirror Reflectivity and Gain

The VCSEL is a semiconductor laser where the optical cavity is oriented perpendicular to the semiconductor substrate surface, in contrast to edge-emitters. This means that light is emitted from the top surface, enabling simple wafer level testing of devices. However, since the cavity is vertical, the length over which the photons can interact with the gain medium is very short (tens of nanometers) resulting in small round-trip gain. This requires very high reflectivities (>99%) from the two mirrors defining the cavity to ensure that the optical losses in the cavity are sufficiently low. A schematic cross-section and a microscope top view of a VCSEL can be seen in Fig. 2.1.

The reflectivity needed is typically achieved by using distributed Bragg reflectors (DBRs). A DBR consists of a number of pairs of alternating $\lambda/4$-thick layers, with different refractive index. Typically DBRs for VCSELs are either epitaxially grown semiconductors or consist of dielectric materials. The



(a) (b)

Fig. 2.1. (a) Schematic cross-section of a VCSEL, and (b) microscope top view of a VCSEL on chip.

number of pairs needed for >99% reflectivity depends on the refractive index contrast between the layers. The materials available for epitaxial DBRs have relatively low refractive index contrast which requires ∼20–30 DBR pairs for sufficient reflectivity, while dielectric materials have the possibility for much larger refractive index contrast and typically require less than 10 DBR pairs for sufficient reflectivity.

For sufficient gain the intrinsic part of the active region consists of multiple quantum wells (QWs) in a separate confinement heterostructure (SCH), where carriers are trapped leading to a high carrier density. Traditionally 850-nm VCSELs have employed GaAs QWs, but employing strained InGaAs QWs increases the differential gain, which is advantageous to reach higher speed.

2.1.2 Transverse Confinement

The photons are confined to the active region vertically by the two DBRs, nevertheless both carriers and photons need to be transversely confined to the center of the active region. Some examples of transverse confinement schemes are etched air post [19], ion implantation [20], buried tunnel junction (BTJ) [21], and oxide aperture [22], as illustrated in Fig. 2.2. The etched air post (Fig. 2.2a) is obviously the simplest solution where the optical field is confined by the large refractive index contrast between semiconductor and air, but scattering and carrier recombination at the semiconductor-air interface cause problems. Defining the aperture by implanting ions (Fig. 2.2b), usually protons, was successfully used for the first commercial VCSELs. The implanted regions

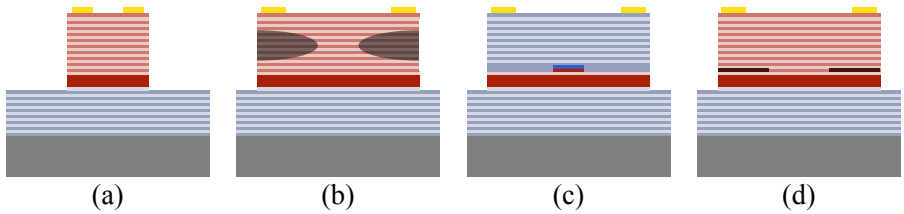


Fig. 2.2. Transverse confinement schemes: (a) etched air post, (b) ion implantation, (c) buried tunnel junction, and (d) oxide aperture.

become highly resistive, which confines the carriers to the center. However, the implantation does not change the refractive index significantly causing the optical field to be confined by gain guiding and thermal lensing (caused by the temperature rise in the active region under operation, which changes the refractive index slightly), which will cause the modal behavior to depend on the injection current [23]. The BTJ (Fig. 2.2c) provides both optical and electrical confinement and has been successfully implemented for long-wavelength InP-based VCSELs, but it has proven more difficult to implement at shorter wavelengths [24], although InGaAs-based BTJ VCSELs at 1100 nm have been demonstrated [7]. Oxide-confined GaAs-based VCSELs (Fig. 2.2d) utilize selective oxidation of high Al-content AlGaAs-layers to form the oxide apertures (in contrast to InP-based VCSELs that lack a high quality oxide), which provides both electrical and optical confinement since the resulting oxide is isolating and has lower refractive index than the non-oxidized material. Apart from the excellent high-speed properties presented in Section 1.1, oxide-aperture VCSELs have yielded power conversion efficiencies (PCEs) of more than 60% [25], which makes it the confinement scheme of choice for this work.

2.1.3 Temperature Effects

Since the VCSEL cavity is short (on the order of the wavelength), the emission wavelength is set by the cavity resonance rather than the gain peak. The emission wavelength is therefore red-shifting with temperature, which increases with current due to resistive Joule heating, due the temperature dependence of the refractive index of the semiconductor material. This causes the cavity resonance wavelength of GaAs-based VCSELs to increase with ∼0.06–0.09 nm/°C, while the gain peak is red-shifted with ∼0.32–0.33 nm/°C due to bandgap shrinkage [26]. Obviously, the best situation arises when the cavity resonance is aligned with the gain peak, where the lowest threshold current is obtained,

but the different red-shift rates will eventually position the gain peak too far away from the cavity resonance, increasing the threshold current too much for lasing to occur. To enable operation at elevated temperatures the cavity resonance is often detuned with respect to the gain peak, i.e. the cavity resonance is red-shifted with respect to the gain peak at room temperature, causing the resonance and gain to align at elevated temperature. This technique has been used to be able to operate well above 100°C [27].

Chapter 3

Silicon Photonics Integration

Silicon photonics (SiP) has attracted significant attention since the mid-1980s [28, 29]. The vision from the start has been to realize photonic integrated circuits (PICs, or "superchips", as they were called) including both optical and electrical circuits on silicon [30–32]. The main reason to pursue SiP PICs is the potential to integrate many functions in a PIC that can be produced in high volumes at low cost in CMOS fabs. Today SiP PIC platforms for both optical communication and sensing are becoming mature, but they still lack efficient light generation. A possible route is heterogeneous integration of direct bandgap III-V material that can provide the optical gain needed.

3.1 Heterogeneous Integration

Integration of lasers onto a SiP PIC can be made in different ways [33]. The laser can be processed on its native substrate and transferred to the PIC using flip-chip techniques [34, 35] or the III-V material can be grown directly on the Si substrate [33, 36]. However, flip-chip techniques require stringent alignment of the individual lasers, while direct growth of high quality III-V material has proven difficult. An alternative technique is bonding of epitaxial III-V films onto the PIC, which can be processed after bonding exploiting lithographic alignment techniques. This is referred to as heterogeneous integration.

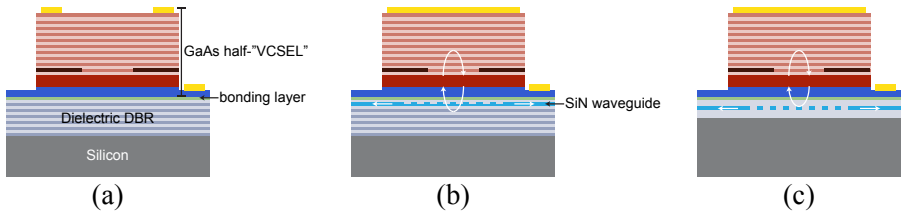


Fig. 3.1. Hybrid vertical-cavity lasers with surface emission (a), in-plane waveguide emission using a weak diffraction grating (b), and using a HCG (c).

The bonding can be either direct (using Van der Waals forces) or adhesive [37]. Adhesive bonding has the advantage of being more resistant against surface roughness and contamination. This work (Paper C and D) has been focused on heterogeneous integration of short-wavelength VCSELs, where the epitaxial layers have been transferred to a reflector on a Si substrate using ultra-thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding [38]. Silicon-on-insulator (SOI) optical waveguides absorb short-wavelength light, which makes the silicon nitride (SiN) waveguide [39] platform an attractive choice for GaAs-based VCSELs.

3.1.1 Hybrid Vertical-Cavity Lasers

In Paper C and D a GaAs-based "half-VCSEL" epitaxial structure, containing a DBR and an active region, is transferred to a reflector on silicon, resulting in a hybrid vertical-cavity laser (HVCL) with surface-emission (i.e. a hybrid-cavity VCSEL), see Fig. 3.1(a). The hybrid cavity means that the optical field extends over both the GaAs-based and Si-integrated parts, which provides an opportunity to tap off some optical power into in-plane waveguides on the SiN SiP PIC. By suppressing the surface emission (by increased top mirror reflectivity), while coupling some light into in-plane PIC waveguides it is possible to form a HVCL with in-plane emission. The in-plane coupling of the HVCL can be achieved by a weak diffraction grating inside the cavity [40] if a dielectric DBR is used as reflector on top of the Si substrate, see Fig. 3.1(b). An alternative is to use a SiN high-contrast grating (HCG) as both reflector and coupler (Fig. 3.1c) [41], which also could be used to set the resonance wavelength of individual HVCLs by the grating parameters [42, 43] to enable fabrication of fully integrated multi-wavelength laser arrays for short-wavelength wavelength division multiplexed (WDM) optical interconnects [44].

3.1.2 Thermal Effects

Silicon has inherently good thermal conductivity, but the dielectrics used to form a reflector on top of the silicon have worse thermal conductivity and will act as an insulation that prevents the heat generated in the HVCL active region to escape down to the substrate. The hybrid-cavity VCSELs in Paper C and D therefore have ∼3 times worse thermal impedance than ordinary oxide-confined VCSELs [45], which will affect both static and dynamic performance negatively. To improve the performance the heat must be allowed to spread, for example using integrated metallic heat-spreaders [46].

Chapter 4

VCSEL Dynamics

The VCSEL is typically directly modulated with large signals. To improve the performance it is important to be able to predict the speed limiting factors. This chapter introduces the VCSEL small signal dynamics and briefly discuses some considerations for large signal operation.

4.1 Small Signal Dynamics

It follows from the standard coupled rate equations that the intrinsic small-signal modulation response of a single mode laser is that of a damped second order system. However, VCSELs are typically multimode, but due to the high overlap of the transverse modes they can still be treated as a single mode [47]. By also accounting for the parasitics by an additional pole, the transfer function is given by [48]

$$H(f) = \text{const.} \cdot \frac{f_\text{r}^2}{f_\text{r}^2 - f^2 + \text{j}\frac{f}{2\pi}\gamma} \cdot \frac{1}{1 + \text{j}\frac{f}{f_\text{p}}}, \tag{4.1}$$

where f_r is the resonance frequency, γ the damping factor, and f_p the parasitic cut-off frequency. The resonance frequency is given by

$$f_\text{r} = \frac{1}{2\pi}\sqrt{\frac{v_\text{g} \cdot (\partial g/\partial n) \cdot S}{\tau_\text{p} \cdot (1 + \varepsilon S)}}, \tag{4.2}$$

where v_g is the group velocity, $\partial g/\partial n$ the differential gain, S the photon density, τ_p the photon lifetime, and ε the gain compression factor. The increase of

the resonance frequency with the photon density is typically quantified by the D-factor defined as

$$D \equiv \frac{f_\mathrm{r}}{\sqrt{I - I_\mathrm{th}}}, \tag{4.3}$$

where $I - I_\mathrm{th}$ is the injected current above the threshold. The damping factor in (4.1) is given by

$$\gamma = K \cdot f_\mathrm{r}^2 + \gamma_0, \tag{4.4}$$

where γ_0 is the damping offset and the K-factor is given by

$$K = 4\pi^2 \left(\tau_\mathrm{p} + \frac{\varepsilon}{v_\mathrm{g} \cdot (\partial g / \partial n)} \right). \tag{4.5}$$

4.2 Bandwidth Limitations

The intrinsic bandwidth (without parasitics and thermal effects) is limited by the K-factor through

$$f_\mathrm{3dB,max} = \frac{2\pi\sqrt{2}}{K} \tag{4.6}$$

and is typically exceeding 30 GHz [49]. In Fig. 4.1 the extracted intrinsic response of the VCSEL used in Paper A is shown to have a bandwidth exceeding 50 GHz (blue line). Due to thermal effects and parasitics, bandwidths at these levels are not reached in practice. Thermal effects will eventually limit the build up of photon density, setting a limit on the maximum resonance frequency, consequently limiting the bandwidth to 33 GHz in Fig. 4.1 (green line). The parasitics (resistance and capacitance) will reduce the actual modulation current through the active region at frequencies above the cut-off frequency, resulting in an effective bandwidth of ∼24 GHz (red line).

This means that it is important to design VCSELs with low heat generation, good heat conductivity, low resistance, and low capacitance to overcome the thermal effects and the parasitics. Better heat conductivity can be obtained by employing binary alloys in the DBR [50]. The DBR resistance can be reduced by graded interfaces and modulation doping or by bypassing the DBR using intra-cavity contacts [25]. The parasitic capacitance across the oxide layer can be reduced by including additional oxide layers, which will effectively increase the oxide thickness and reduce the capacitance [51–53].

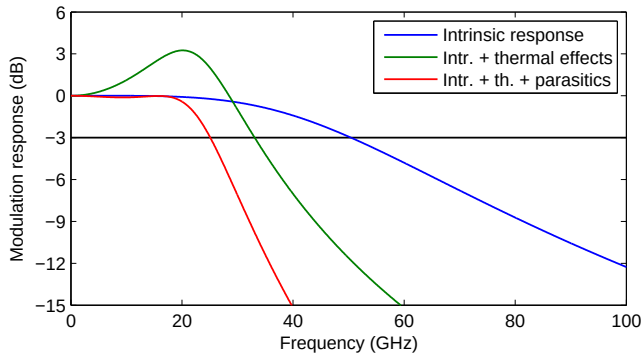


Fig. 4.1. Intrinsic and extrinsic modulation response extracted from the VCSEL used in Paper A with K- and D-factors of 0.17 ns and 9.0 GHz/mA$^{1/2}$, respectively, along with a parasitic pole, $f_p \approx 17$ GHz.

4.3 Large Signal Dynamics

Since the K-factor depends on the photon lifetime, τ_p, it is possible to tune the K-factor by adjusting the photon lifetime. It is possible to reduce the photon lifetime by a shallow surface etch of the top DBR layer, since the photon lifetime is set by the reflectivities of the DBRs. This will give a slightly out of phase reflection at the semiconductor-air interface, effectively lowering the DBR reflectivity and consequently also the photon lifetime and K-factor [54].

In Paper B, we utilized this effect to investigate the impact of damping (through the K-factor) on high-speed large signal VCSEL dynamics. We found that the optimum damping depends on the data rate. Lower data rates can afford higher damping, whereas to achieve higher data rates it is crucial with lower damping to reach the bandwidth and output power needed in the link. However, too low damping will cause excessive overshoot and ringing, which is detrimental for the signal quality.

Chapter 5

High-Speed Measurements

In order to characterize the VCSELs high-speed properties both small and large signal measurements have to be performed. The small signal modulation response provides data that allows for fitting of the theoretical transfer function in Chapter 4.1, while the large signal experiments are closer to the real application of data transmission.

5.1 Small Signal Modulation Response

The small signal modulation response (S_{21}) is measured using a vector network analyzer (VNA) connected to the VCSEL through a bias-T to allow DC biasing. By employing VCSEL bondpads that are matching the ground-signal-ground (GSG) probe pitch, the VCSEL can be probed directly on wafer. The output light from the VCSEL is coupled into a short multimode fiber using either an anti-reflection coated lens package or a butt-coupled bare fiber tip. The fiber is connected through a variable optical attenuator (VOA) to a high-speed photodetector connected to the VNA. The VOA is included to avoid saturating the detector. The measured data is then corrected for the response of the probe and detector before the transfer function (4.1) is fitted to the response. From the fit the K- and D-factors can be extracted. A schematic of the measurement setup can be seen in Fig. 5.1.

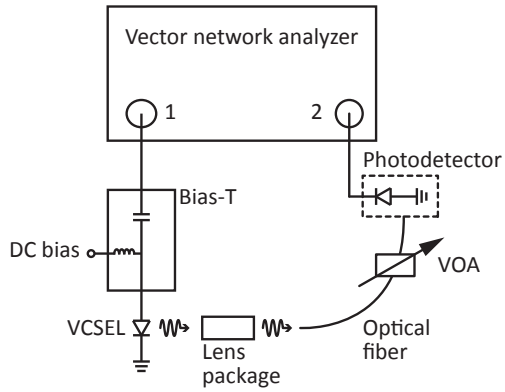


Fig. 5.1. Measurement setup for the small signal modulation response.

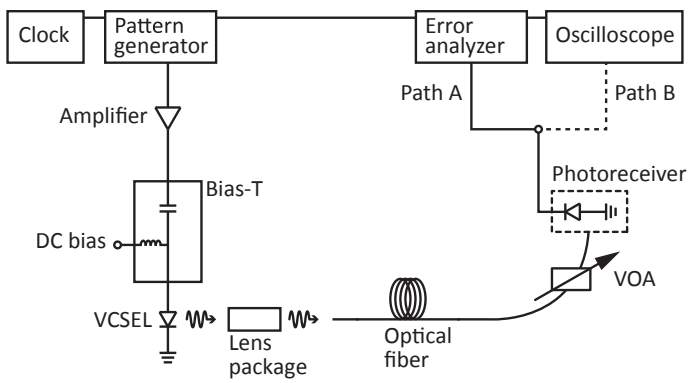


Fig. 5.2. Large signal data transmission setup. Path A is used to measure BERs, while path B is used to record eye diagrams.

5.2 Large Signal Data Transmission

In the simplest modulation format the ones and zeros are represented by setting the VCSEL in either its on- or off-state. This binary modulation format is called on-off keying (OOK). To perform large signal data transmission experiments an OOK signal consisting of pseudo random bit sequences (PRBSs) from a pattern generator is amplified and fed to the VCSEL through a bias-T and a GSG probe. The light is coupled into a multimode fiber connected to a photoreceiver through a VOA. The electrical signal from the photoreceiver is connected to an oscilloscope to record eye diagrams (an overlay of the signal waveform) or an error analyzer synchronized with the pattern generator to count the number of errors in the received signal. A schematic of the setup is shown in Fig. 5.2. By relating the number of errors to the total number of bits the bit error rate (BER) can be calculated. For very low BERs the time needed to accumulate errors is very long. For reasonable measurements times it is therefore necessary to use statistical methods. It is required that N_{bits} is detected without any error to ensure a BER below p with a statistical confidence c, where N_{bits} is given by [55]

$$N_{\text{bits}} = -\frac{\ln(1-c)}{p}. \tag{5.1}$$

Typically a statistical confidence of 95% is required, which for a BER below 10^{-12} (often defined as error-free) require $3 \cdot 10^{12}$ error-free bits, which corresponds to measurement times of 5 and 1 min at 10 and 50 Gb/s, respectively. However, in this work $6 \cdot 10^{12}$ error-free bits were required, corresponding to a BER below $5 \cdot 10^{-13}$ with 95% confidence or alternatively a BER below 10^{-12} with 99.75% confidence.

Chapter 6

VCSEL Fabrication

The complex VCSEL epitaxial structures used in this work were grown by metal-organic chemical vapor deposition (MOCVD) on undoped 3" GaAs substrates at IQE Europe Ltd. In MOCVD, organic molecules are used to transport III-metals (Al, Ga, In) to the heated substrate, where they react with arsine (AsH_3) to form a III-As epitaxial film [56]. After the epitaxial growth VCSELs were fabricated using a range of standard processing steps, including photolithography, thin film deposition, etching, and wet oxidation. This chapter introduces these processing steps and describes the full fabrication process for both high-speed and silicon-integrated hybrid-cavity VCSELs.

6.1 Photolithography

Photolithography is the standard method to transfer a pattern on a mask onto a semiconductor wafer in the semiconductor industry. Even though several more advanced techniques with sub-micron resolution exist, such as nanoimprint and electron beam lithography, standard UV photolithography has been used in this work since the resolution of approximately 1 µm [56] is sufficient. However, control of transverse modes and the polarization state using surface structures would require the higher resolution of nanoimprint and electron beam lithography.

Photolithography relies on the optical sensitivity of a photoresist, which is spin coated on the wafer at a few thousand rounds per minute to form a thin film of a few micrometers. The photoresist is then selectively exposed with ultra-violet light through a chromium photomask. During the following

development the exposed or nonexposed photoresist will be removed depending on whether the photoresist has positive or negative tone. The pattern is now transferred to the wafer and can be used to protect parts of the wafer surface during subsequent etching or deposition steps.

6.2 Thin Film Deposition

There are several different techniques to deposit thin films. In this work the dielectric material silicon nitride (SiN) has been deposited using sputtering and plasma-enhanced chemical vapor deposition (PECVD), while metals have been deposited using sputtering and electron beam evaporation.

Sputtering is a technique where inert ions in a plasma are accelerated towards a target of the material to deposit. The accelerated ions will knock out target atoms that will diffuse toward the wafer where they form a thin film [57]. In the SiN case, reactive N_2-gas is injected to form a dielectric thin film with the sputtered silicon atoms, whereas metals are deposited without the presence of any reactive gas.

Since the PECVD is plasma enhanced, the gases injected to the chamber can be made chemically reactive by the plasma even at relatively low temperatures, which is important to avoid damage to the GaAs epitaxial structure or any contacts [56]. In this work SiN was deposited by injecting SiH_4 and N_2 into an Ar plasma, where they react to form a SiN thin film on the wafer surface. During both sputtering and PECVD the resulting stoichiometry will depend on the deposition conditions and is therefore typically denoted Si_xN_y.

Another way of depositing metal is by electron beam evaporation, where metal is heated by an incident electron beam. When the metal is heated beyond its melting point it will evaporate. The atoms in the vapor will travel through the vacuum chamber and form a metal film on the substrate surface [57].

6.3 Etching

Removal of AlGaAs material can be achieved with both wet and dry etching techniques. Wet etching is as the name suggests based on liquid solutions that are able to chemically dissolve material, often with good selectivity. However, wet etching is hard to accurately control and will not result in vertical sidewalls as perfect anisotropic etching is difficult to achieve. Dry etching, which makes use of chemicals in gaseous form in a plasma, on the other hand has the possibility to combine a chemical etch with a physical,

since the chemical reactions can be combined with ion bombardment [56]. The combination of chemical and physical etching makes it possible to adjust the process parameters to achieve an anisotropic etch.

The main dry etching technique used in this work has been inductively coupled plasma (ICP) reactive ion etching (RIE). The ICP is used to create a high-density plasma of the reactive gases used. Ions from the plasma are accelerated toward the substrate were they will chemically react with the surface removing material from the horizontal surface resulting in a directional etch. The gas used to etch the AlGaAs epitaxial structure is a mixture of $SiCl_4$ and Ar. ICP RIE was also used to etch Si_xN_y with NF_3, and benzocyclobutene (BCB) using a mixture of CF_4 and O_2. The etch depth can be accurately monitored by an *in situ* laser interferometer endpoint detection system in the ICP RIE system.

To obtain precise shallow etch depths of the top DBR layer to tune the photon lifetime Ar ion milling was used. Ar ion milling is a purely physical process where inert Ar ions are generated and accelerated towards the wafer surface where the ions sputter material from the surface [56]. Since the etch is not chemical the etch rate is predictable and the etch depth can be controlled by the etch time.

6.4 Wet Oxidation

Selective wet oxidation of high aluminum-content AlGaAs is used to form the VCSEL oxide aperture. The wet oxidation is performed after the mesa etch by exposing the high aluminum-content AlGaAs layers to water vapor at elevated temperature [58]. The wet oxidation rate depends on the aluminum content, making it possible to include secondary oxide layers that oxidizes slower than the primary oxide layers. In this work an N_2-bubbler is used to transport water vapor from a water beaker held at 95°C to the oxidation furnace held at 420°C, achieving a typical oxidation rate of $\sim$0.3 µm/min for $Al_{0.98}Ga_{0.02}As$. The oxidation front is observed *in situ* using IR illumination and a microscope with a CCD camera. Since the oxidation rate is very sensitive to the temperature even the small temperature gradient across the sample is enough for the oxide aperture diameter to become nonuniform [58]. To improve the uniformity the sample can be rotated 180° after half the oxidation time. A scanning electron microscope (SEM) micrograph of an oxide aperture in a focused ion beam (FIB) VCSEL cross-section is shown in Fig. 6.1.

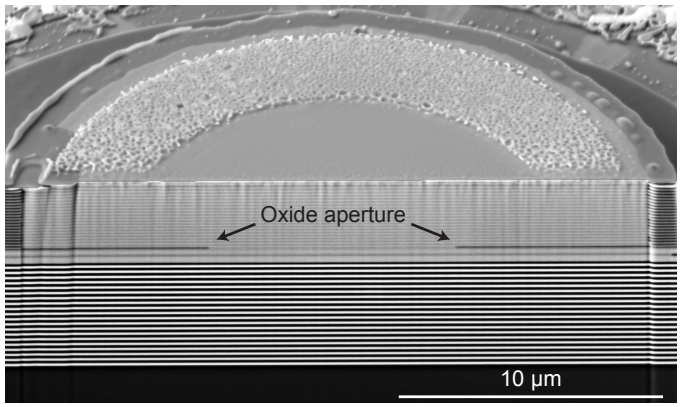


Fig. 6.1. SEM micrograph of an oxide aperture (indicated) in a FIB VCSEL cross-section.

6.5 High-Speed VCSEL Fabrication Process

Before processing, the 3" wafer is cleaved into 8×10 mm chips. After cleaning the chips, Ti/Pt/Au p-contacts are deposited along with alignment marks using electron beam evaporation. A hard mask, defined in sputtered Si_xN_y, for circular mesas with diameters of 22, 24, 26, 28 µm is etched using ICP-RIE with NF_3 chemistry, followed by etching the mesas using ICP-RIE with $SiCl_4$ chemistry. The *in situ* laser interferometer endpoint detection system of the ICP-RIE system is used to stop accurately at the desired etch depth and expose the oxide layers without exposing the AlAs layers in the bottom DBR. The chip and mesa surface is protected by a PECVD deposited Si_xN_y layer, which is removed at the mesa sidewalls before oxidation. Oxide apertures are formed by wet oxidation at 420°C. A second mesa is etched down to the contact layer below the bottom DBR, again using ICP-RIE with $SiCl_4$ chemistry. The protective Si_xN_y layer is removed using ICP-RIE with NF_3 chemistry, followed by electron beam evaporation of Ni/Ge/Au n-contacts, annealed in an inert N_2 atmosphere at 430°C for 30 s. The contact layer is removed outside the mesas and the n-contacts to reduce the bondpad capacitance. A thick BCB layer is spin-coated to planarize the surface and allows for deposition of Ti/Au bondpads in a GSG configuration by sputtering. Finally, the top DBR layer was thinned by Ar ion milling to set the photon lifetime. The fabrication process for high-speed VCSELs is illustrated in Fig. 6.2.

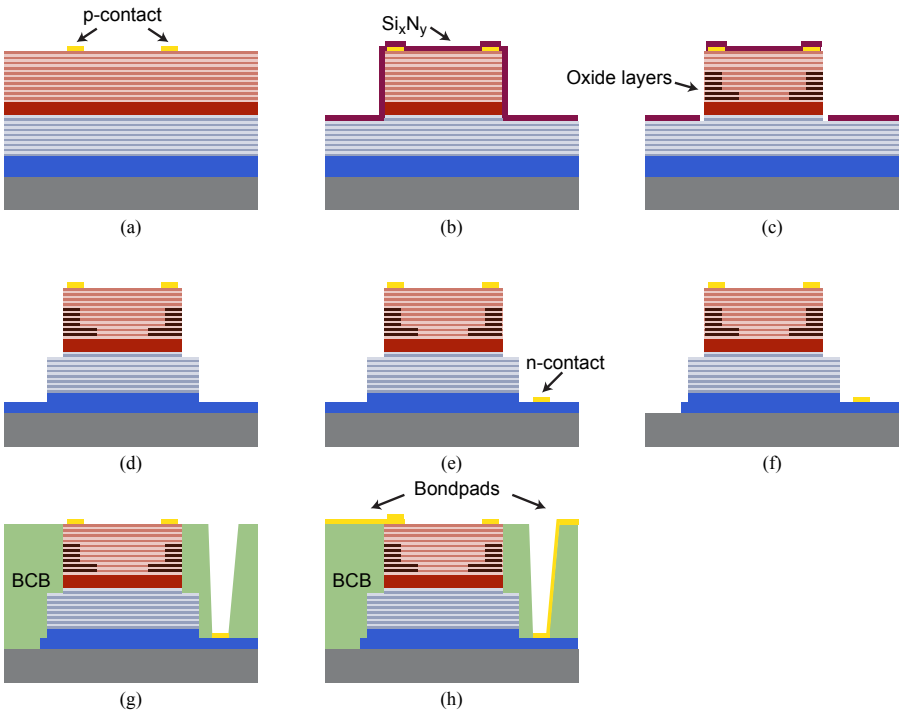


Fig. 6.2. The process steps for high-speed VCSEL fabrication includes: (a) *p*-contact deposition, (b) mesa etching followed by deposition of Si_xN_y, (c) oxide aperture formation after opening of the Si_xN_y on the mesa side walls, (d) second mesa etching, (e) *n*-contact deposition, (f) *n*-contact layer removal beneath the *p*-bondpad, (g) planarization with BCB, and (h) deposition of bondpads.

6.6 Silicon-Integrated Hybrid-Cavity VCSEL Fabrication Process

The silicon-integrated hybrid-cavity VCSELs have a similar fabrication process as the high-speed VCSELs (Section 6.5) after the bonding of the GaAs-based "half-VCSEL" structure to the dielectric DBR on Si using DVS-BCB and removal of the GaAs substrate. However, to allow residual gas trapped in the bonding layer to escape during subsequent high temperature process steps the mesas were isolated by trenches etched through the epitaxial III-V structure before the mesas. Further, to reach the thin intra-cavity contact layer just below the active region, the mesa etch is stopped within the contact layer, where the n-contact is deposited and annealed after oxidation and removal of the protective Si_xN_y layer. The fabrication process for silicon-integrated hybrid-cavity VCSELs is illustrated in Fig. 6.3.

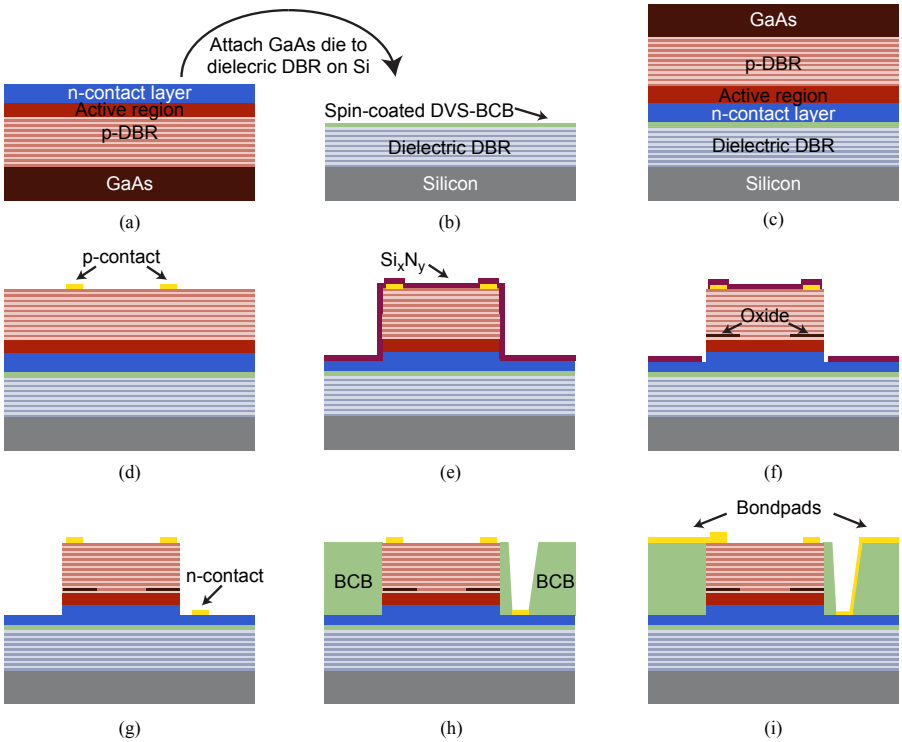


Fig. 6.3. The process steps for silicon-integrated hybrid-cavity VCSEL fabrication includes: (a-c) bonding of the GaAs-based "half-VCSEL" structure to the dielectric DBR on Si spin-coated with DVS-BCB followed by removal of the GaAs substrate, (d) *p*-contact deposition, (e) mesa etching followed by deposition of Si_xN_y, (f) oxide aperture formation after opening of Si_xN_y on mesa side walls, (g) *n*-contact deposition, (h) planarization with BCB, and (i) deposition of bondpads.

Chapter 7

Future Outlook

As indicated in Chapter 4, the high-speed VCSEL performance is limited by the device resistance and capacitance along with heat generation and thermal impedance. Employing intra-cavity contacts is a viable route that bypasses the DBR resistance, which already has led to record-high PCE [25]. By also moving to longer wavelengths (for example 980 nm or 1060 nm) by adding more indium in the QWs the differential gain is increased, which is beneficial for high-speed operation. Further, at wavelengths above 940 nm it is possible to use binary GaAs in the DBRs, which could benefit the thermal impedance and the electrical resistance.

Even though some improvements of high-speed VCSEL performance could be expected through reduced resistance, capacitance, and thermal impedance, it is probable that it will not be enough to meet the future bandwidth demands. The future standards already consider higher order modulation formats like 4-level pulse amplitude modulation (4-PAM) and forward error correction (FEC) codes. It also becomes increasingly more important to co-optimize the driver electronics (possibly also including equalization) with the VCSEL to achieve best performance without increasing the power consumption.

The silicon-integrated hybrid-cavity VCSELs needs to be further developed with better thermal properties and lower capacitance to be able to catch up with state-of-the-art high-speed VCSELs. This can possibly be achieved by integrated metallic heat-spreaders and additional oxide layers, as discussed in Sections 3.1.2 and 4.2.

Since the goal is to realize efficient integrated light sources on SiP PICs, in-plane emission is crucial. Some possibilities for in-plane coupling were

presented in Section 3.1.1, but so far in-plane coupling from a HVCL has only been demonstrated using optical pumping yielding very low output power [41].

Integrated multi-wavelength arrays of HVCLs would also enable the realization of PIC-based WDM transmitters for optical interconnects and multi-wavelength sources for biophotonics and life sciences.

Chapter 8

Summary of Papers

Paper A

"High-speed 850 nm VCSELs operating error free up to 57 Gbit/s,"
Electronics Letters, vol. 49, no. 16, pp. 1021–1023, Aug. 2013.

This paper presents error-free data transmission at RT without equalization up to 57 Gb/s over 1 m OM4 multimode fiber. At longer fiber lengths, 55 Gb/s and 43 Gb/s over 50 and 100 m, respectively, were demonstrated. These data rates are record-high for binary links without equalization. The results were obtained using a VCSEL with the damping optimized for high data rates. The VCSEL has a bandwidth of ∼24 GHz, and K- and D-factors of ∼0.17 ns and ∼9 GHz/mA$^{1/2}$, respectively.

My contribution: I performed all measurements, analyzed the results, and co-authored the paper.

Paper B

"Impact of damping on high-speed large signal VCSEL dynamics,"
Journal of Lightwave Technology, vol. 33, no. 4, pp. 795–801, Feb. 2015.

In this paper the results from a study of how damping affects the large signal VCSEL dynamics are presented. Through measurements of turn-on delays, eye diagrams, and BERs, we conclude that the optimum damping depends on the

data rate. At low data rates it is affordable with more damping, whereas at higher data rates the higher bandwidth and slope efficiency of a less damped VCSEL are needed.

My contribution: I fabricated the VCSELs together with P. Westbergh. I performed all measurements, analyzed the results, and wrote the paper. I also presented the results at the IEEE International Semiconductor Laser Conference 2014 (Palma de Mallorca, Spain).

Paper C

"Silicon-integrated short-wavelength hybrid-cavity VCSEL," *Optics Express*, vol. 23, no. 26, pp. 33634–33640, Dec. 2015.

This paper presents the design, fabrication, and static performance of a short-wavelength hybrid-cavity VCSEL heterogeneously integrated on silicon. DVS-BCB adhesive bonding is used to attach a GaAs-based "half-VCSEL" to a dielectric DBR on silicon to form a hybrid vertical cavity, where the standing-wave optical field extends over both the GaAs- and silicon-based parts. A 9-µm oxide-aperture diameter hybrid-cavity VCSEL produces 1.6 mW of output power at 845 nm.

My contribution: I established the GaAs-processing part of the silicon-integrated hybrid-cavity VCSELs at Chalmers and fabricated the VCSELs. I performed the measurements and analyzed the results. I co-authored the paper and was the corresponding author. I also presented the results at SPIE Photonics West 2016 (San Francisco, CA, USA).

Paper D

"20-Gb/s modulation of silicon-integrated short-wavelength hybrid-cavity VCSELs," *IEEE Photonics Technology Letters*, vol. 28, no. 8, pp. 856–859, Apr. 2016.

This letter presents the dynamics of the silicon-integrated hybrid-cavity VCSELs in Paper C, with optimized damping (Paper B) for large signal data transmission. A 5-µm oxide-aperture diameter hybrid-cavity VCSEL with a small signal bandwidth of 11 GHz is capable of error-free data transmission up to 20 Gb/s. The hybrid-cavity VCSEL has K- and D-factors of 0.2 ns and 7 GHz/mA$^{1/2}$,

respectively. An analysis of the small signal modulation response reveals that the bandwidth (and consequentially the possible data rate) is limited by both thermal effects and parasitics.

My contribution: I fabricated the silicon-integrated hybrid-cavity VCSELs, performed the measurements, and analyzed the results. I wrote the paper and presented the results at SPIE Photonics West 2016 (San Francisco, CA, USA).

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