An Accurate Empirical Model Based on Volterra Series for FET Power Detectors

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***Abstract*—An empirical model for field-effect transistor (FET) based power detectors is presented. The electrical model constitutes a Volterra analysis based on a Taylor series expansion of the drain current together with a linear embedding small-signal circuit. It is fully extracted from S-parameters and *IV* curves. The final result are closed-form expressions for the frequency dependence of the noise equivalent power (NEP) in terms of the FET intrinsic capacitances and parasitic resistances. Excellent model agreement to measured NEP of coplanar access graphene FETs with varying channel dimensions up to 67 GHz is obtained. The influence of gate length on responsivity and NEP is theoretically and experimentally studied.**

***Index Terms*—Analytical model, field-effect transistors (FETs), graphene, microwave detectors, power detectors, terahertz detectors, Volterra.**

I. Introduction

DIRECT square-law power detectors are important in numerous applications utilizing radio waves down to submillimeter waves, requiring low-to-moderate spectral resolution [1]. The diverse applications have very different demands on parameters such as receiver cost, sensitivity, and integration level. The scale spans from highly integrated solutions in standard semiconductor processes for commercial imaging systems in security and surveillance [2] to cost-insensitive state-of-the-art cryogenic bolometer detectors for radioastronomy [3]. As a result of the different target applications, a variety of technologies for detector implementation are used.

In applications at room-temperature demanding only moderate sensitivity, nonlinear solid-state devices are frequently used as rectifying total power detectors. Among two terminal devices, the well-established zero-bias GaAs Schottky diode detector technology is continuously used in both waveguide [4] and quasi-optical configurations [5]. In parallel, novel diode material combinations are explored [6]. Further, Schottky diodes fabricated in HEMT processes offers a high integration level with low-noise pre-amplification up to W-band [7]. Recently, the classic concept of backward detector diodes [8] has been refined in the zero-bias Sb tunneling diode [9], [10]. Together with separate pre-amplifier chips, they provide sensitive W-band power detectors [11]. Besides diodes, three-terminal solid-state devices are explored for detector circuits with the main focus on field-effect transistors (FETs). Millimeter-wave and terahertz detection was first demonstrated in III–V HEMTs [12]–[14], later Si CMOS [15], and most recently, graphene [16]–[18]. Antenna-coupled MOSFETs have especially emerged as a candidate for active terahertz imaging arrays, integrating also the read-out electronics [19]. This is enabled by single detectors in low-cost bulk CMOS processes operating with noise equivalent power (NEP) < 100 pW/Hz$^{1/2}$ well above 1 THz [20]. In design of detector circuits there is a demand on models easily implemented in circuit simulators. The models should provide design rules for responsivity, NEP, and device input impedance versus frequency. Preferably, the model should be derived from dc and S-parameter characterization. Today, the small-signal analysis of detector diodes is based on such methods using Taylor polynomials [21].

However, the stated requirements are not fully met for the current FET detector models. Attempts to use Taylor expansion for the nonlinearity in FETs are nonphysical. Either only the mixed second derivative is used [22] or second derivatives are completely omitted [23]. Instead, physical models are constructed from the plasma-wave theory by Dyakonov–Shur [24]. The profound importance of high mobility in this theory, ultimately predicting resonant detection, has weak support in experiments [25], [26]. In addition, the plasma-wave theory predicts enhanced intrinsic responsivity with frequency, anticipated to be constant with gate length without frequency limit [24]. Still, a distinct responsivity drop at higher frequencies is repeatedly found experimentally, e.g., $\sim 1/f^2$ in [27] together with enhanced performance when shrinking the gate length [20]. The reported models, on the other hand, give frequency dependencies ranging from $1/f$ [27], [28], via $1/f^2$ [22], all the way to $1/f^4$ [28], [29]. The experimentally obtained frequency roll-off is entirely explained by fitting a parasitic capacitance [27]. Evidently, a clear consensus and understanding to model the mechanisms behind the frequency dependence is lacking. Likewise, the models based on plasma-wave theory require fitting parameters to predict the variation of responsivity with gate bias [27], [30]–[32]. Furthermore, the gate voltage derivative of the drain current is used, which is not well defined for FETs at zero drain bias.

Currently, implementations in circuit simulators use physical transistor models. The idea from plasma-wave theory to use an *RC* gate network in simulation has weak experimental support [28], [33]. Instead, the experimental results in [19] encourages a QS simulation approach. Indeed, lumped transistor models

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are established for design of circuits at terahertz frequencies as long as the gate width is carefully scaled to avoid unwanted distributed effects [34]. Considering the narrow devices used in the so-called broadband detection regime [19], the distributed analogy of the gate to a transmission line is hence redundant. Nevertheless, no explicit device design rules derived from the physical models are discussed.

In this paper, an empirical model approach for FET small-signal power detectors is presented. It works with any lumped large-signal model topology extractable from *IV* curves and S-parameters. The FET rectifying capability is predicted by the nonlinearity of the drain current in a Taylor expansion. The circuit inevitably has feedback and the Taylor expansion is included in a Volterra series for calculation of responsivity [35]. Volterra series is already established, e.g., for analysis of intermodulation in amplifiers [36] and mixers [37].

The standard FET equivalent circuit in [38] and [39] is used as the basis for the calculations in this paper, omitting the nonlinear bias dependence of the capacitors. The model contains few and easily interpretable parameters. Closed-form expressions for the thermal noise limited NEP are derived. The equations explicitly show the importance of minimizing intrinsic FET capacitance and parasitic resistance. The embedding linear circuit gives a $1/f^2$ dependence at high frequencies. Instead of plasma waves, this paper shows that the FET detector operation can be described electrically just as the diode detector [21]. Excellent agreement to probed measurements on graphene FETs (GEFTs) up to 67 GHz is found. The presented equations extend into the terahertz frequency range until the onset of new mechanisms modifies the equivalent circuit.

II. Diode Power Detector

To emphasize the similarity of FET and diode detectors, it is instructive to start by recapitulating the results for two-terminal diode rectifiers [21]. The diode model used in the literature is shown in Fig. 1(a). Small-signal analysis of diodes is based on the power series expansion of the current–voltage characteristics around the dc bias point (V_d, I_d),

$$i_d(V_d) = I_d(V_d) + \frac{dI_d}{dV_d}(v_d - V_d) + \frac{1}{2}\frac{d^2 I_d}{dV_d^2}(v_d - V_d)^2 + \cdots. \quad (1)$$

From (1), the most important dc figure-of-merit for the rectifying capability is the *curvature*, γ, defined by

$$\gamma = \frac{\frac{d^2 I_d}{dV_d^2}}{\frac{dI_d}{dV_d}}. \quad (2)$$

A. Conjugately Matched Responsivity

If the diode is conjugately matched to the source, the voltage responsivity is directly proportional to the curvature. The responsivity is, however, restricted by the series resistance, R_s, and the diode junction capacitance, C_j. These result in a roll-off of the responsivity at high frequencies according to

$$\beta_{v,\max} \simeq \frac{1}{2}\gamma R_j \frac{1}{1 + \frac{R_s}{R_j}} \frac{1}{1 + \frac{R_s}{R_j} + \omega^2 C_j^2 R_j R_s} \quad (3)$$

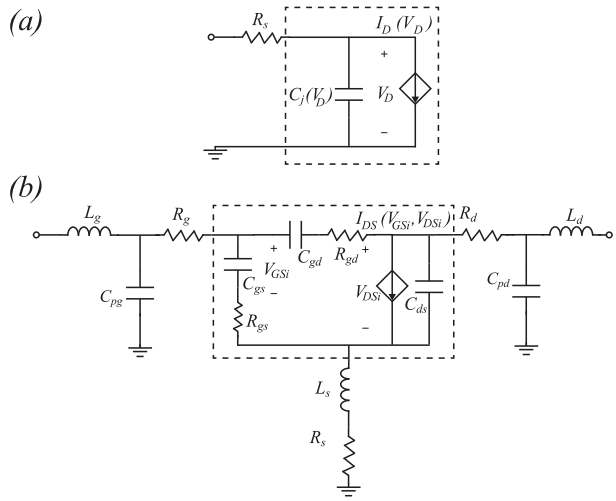

Fig. 1. (a) Large-signal diode model and (b) large-signal FET model. The intrinsic elements are bias dependent in both cases. The nonlinear *IV* sources can be described either directly from measurements or by model equations.

where $R_j = (dI_d/dV_d)^{-1}$ is the diode differential resistance at the chosen bias point. For zero-bias detector diodes with $R_j \gg R_s$, there is equality in (3). From the high-frequency limit of (3), it possible to derive the 3-dB frequency as

$$f_{3\ \mathrm{dB,max}} \approx \frac{1}{2\pi C_j \sqrt{R_j R_s}}. \quad (4)$$

The definition in (4) is directly in voltage responsivity and the intrinsic junction resistance R_j appears in the denominator. Note the difference to the more frequently used figure-of-merit for diodes, $f_c = 1/(2\pi R_s C_j)$. Above the frequency $f_{3\ \mathrm{dB,max}}$, the *intrinsic* responsivity drops rapidly as $1/f^2$.

B. Responsivity With Arbitrary Source Impedance

In the general case, the diode impedance is not conjugately matched to the source, $Z_s \neq Z_d^*$. Now the *power* reflection coefficient $\Gamma_p = (Z_d - Z_s^*)/(Z_d + Z_s)$ or mismatch factor $M_s = 4\Re(Z_s)R_j/|Z_s + Z_d|^2$ [40] must be taken into account. These quantify the decrease from the maximum matched responsivity as given by

$$\beta_v = \beta_{v,\max} \cdot (1 - |\Gamma_p|^2) = \beta_{v,\max} \cdot M_s. \quad (5)$$

For a detector measured in a probed setup, the standardized system impedance is $Z_s = 50\ \Omega$. Similarly, for typical broadband antennas used to couple the incident radiation, $\Re(Z_{\mathrm{ant}}) < 100\ \Omega$. In the low-frequency limit, $Z_d \approx R_j$ and the source impedance is real. Under such conditions it is often valid that $R_j \gg Z_s$ or $R_j \gg R_{\mathrm{ant}}$ and, as approximation,

$$\beta_v \approx 2Z_s\gamma \text{ or } \beta_v \approx 2\Re(Z_{\mathrm{ant}})\gamma. \quad (6)$$

This demonstrates that a severely mismatched diode exhibits a responsivity directly proportional to the source impedance.

III. FET Power Detector

In this section, the Volterra series analysis is applied to gate- and drain-coupled FETs. The standardized FET model used as

the foundation for the analysis is shown in Fig. 1(b). The analysis is quasi-static (QS) as $R_{\rm gs}$ and $R_{\rm gd}$ are neglected to allow the analytical derivations. In what follows, close resemblance to the diode equations will be exposed. The core is the nonlinear current source, which for GFETs is described either directly from measured *IV* or by nonlinear *IV* models in circuit simulators [41]–[43].

A. Method of Nonlinear Currents for FET Detectors

A FET has two control voltages. Correspondingly, the power series is a two-variable Taylor expansion. We choose the *intrinsic* gate- and drain-bias voltages, $V_{{\rm GS}i}$ and $V_{{\rm DS}i}$, as control voltages. The Taylor coefficients at the bias point $(V_{{\rm GS}i}, V_{{\rm DS}i}, I_{\rm DS})$ are defined by the partial derivatives

$$g_{dxsy}(V_{{\rm GS}i}, V_{{\rm DS}i}) = \frac{\partial^{x+y} I_{\rm DS}(V_{{\rm GS}i}, V_{{\rm DS}i})}{\partial V_{{\rm DS}i}^{x} \partial V_{{\rm GS}i}^{y}}. \quad (7)$$

Typical FET detectors operate cold, $V_{\rm DS} \equiv 0$ V. This minimizes $1/f$ noise and maximizes sensitivity [44]. This condition has two implications when setting up the model. First, in a zero-bias FET, the feedback capacitance $C_{\rm gd} \approx C_{\rm gs}$ [17]. The strong feedback (memory) implies that the linear and nonlinear elements are interwoven in the equivalent circuit. This necessitates the use of Volterra series. Secondly, the partial derivatives solely in $V_{{\rm GS}i}$ vanish since the transconductance $g_m \to 0$. Consequently, only the $V_{{\rm DS}i}$ derivatives are nonzero and, when limiting ourselves to second order,

$$i_{\rm ds}(V_{{\rm GS}i}, V_{{\rm DS}i}) \approx g_{d1} v_{{\rm ds}i} + \frac{1}{2} g_{d2} v_{{\rm ds}i}^2 + g_{d1s1} v_{{\rm ds}i} v_{{\rm gs}i}. \quad (8)$$

From (8), it follows that, for a cold-FET, the RF signal must be present *at least* at the drain terminal. Otherwise, no rectified dc signal can be read from the drain. Note that the coefficients g_{d2} and g_{d1s1} may have opposite sign, e.g., for the exemplifying GFETs in this paper $g_{d2} \approx -g_{d1s1} \forall\ V_{\rm gs}$. The most significant difference to the diode is the appearance of the mixed derivative. Also, compared to a zero-bias diode, the gate bias in a FET provides an additional parameter to tune the performance since $g_{dxsy} = g_{dxsy}(V_{{\rm GS}i}, V_{{\rm DS}i})$.

We now calculate the voltage responsivity β_v from the circuit in Fig. 1(b) within the method of nonlinear currents, which amounts to four steps [35]. The current source, embedded by an arbitrary network of linear components, is represented by the power series coefficients g_{d1}, g_{d2}, and g_{d1s1}. First, solve the *linearized circuit*, including g_{d1}, for the first-order voltages under the single-tone excitation $v_s(t) = V_s \cos(\omega_{\rm RF} t)$. The general result is $v_{\rm gs1}(t) = |\alpha_{\rm gs}| V_s \cos(\omega_{\rm RF} t + \angle\alpha_{\rm gs})$ and $v_{\rm ds1}(t) = |\alpha_{\rm ds}| V_s \cos(\omega_{\rm RF} t + \angle\alpha_{\rm ds})$. Second, calculate the second-order current remembering to also retain the phases

$$\begin{aligned} i_{\rm ds2}(t) &= \frac{1}{2} g_{d2} v_{\rm ds1}(t)^2 + g_{d1s1} v_{\rm ds1}(t) v_{\rm gs1}(t) \\ &= \frac{1}{2} g_{d2} |\alpha_{\rm ds}|^2 V_s^2 \cos^2(\omega_{\rm RF} t + \angle\alpha_{\rm ds}) \\ &\quad + g_{d1s1} |\alpha_{\rm gs}| V_s \cos(\omega_{\rm RF} t + \angle\alpha_{\rm gs}) |\alpha_{\rm ds}| V_s \cos(\omega_{\rm RF} t + \angle\alpha_{\rm ds}). \end{aligned} \quad (9)$$

Third, identify the dc term of (9) as

$$\begin{aligned} I_{\rm DC} = &\frac{1}{4} g_{d2} |\alpha_{\rm ds}|^2 V_s^2 \\ &+ \frac{1}{2} g_{d1s1} |\alpha_{\rm gs}| |\alpha_{\rm ds}| V_s^2 \cos(\angle\alpha_{\rm gs} - \angle\alpha_{\rm ds}). \end{aligned} \quad (10)$$

Finally, calculate $V_{\rm DC} = I_{\rm DC}/g_{d1}$ and $\beta_v = V_{\rm DC}/P_{\rm av}$ where the available input power is $P_{\rm av} = V_s^2/8\Re(Z_s)$. Depending on if the signal is fed to the gate or drain terminal, there exist two expressions for the maximum matched responsivity, which are counterparts of (3) for the diode. Further details are given in Sections III-B and III-C, respectively.

The most relevant figure-of-merit for the direct detector, the NEP, is now straightforwardly derived from the calculated β_v. It defines the lowest detectable RF input power within 1 Hz of bandwidth (i.e., equivalently an integration time of 1 s for $V_{\rm DC}$) and is given by

$${\rm NEP} = \frac{v_n}{|\beta_v|} = \frac{\sqrt{4 k_B T R_j}}{|\beta_v|}. \quad (11)$$

The assumption is that of Johnson noise [45] only. This is reasonable for zero-bias diodes [10] and valid also in FETs with a negligible gate leakage current [17], [18]. Deviations occur due to $1/f$ noise at high input RF power [4].

B. RF Gate Coupling

In the absence of pad capacitances, the gate-coupled FET closely resembles the diode model since the drain resistance R_d is open circuited. This effectively reduces the FET to a one-port. In this comparison, the equivalent of the diode junction capacitance is the gate–source capacitance $(C_{\rm gs} \leftrightarrow C_j)$. Similarly the source resistance phenomenologically takes the role of the series resistance of the diode $(R_{s,{\rm FET}} \leftrightarrow R_{s,{\rm diode}})$.

It is also interesting to compare to broadband plasma-wave theory for FET detectors. This attributed the detection in the high-frequency limit to the inactive part of channel, $L_g > L_0$, acting as a shunting capacitor [19]. In Fig. 1(b), this role is clearly undertaken by the *intrinsic* feedback capacitance $C_{\rm gd}$. This capacitance effectively shorts the RF signal to the nonlinearity at high frequency. At low frequency, an external capacitor is still required for the gate-coupled FET detector.

1) Conjugately Matched Responsivity: Maximum responsivity in gate coupling is achieved when $1/j\omega C_{\rm gd} \to 0$. The resulting low-frequency counterpart to the ideal diode voltage responsivity is given by

$$\beta_{v,\max} = -\frac{1}{2} \frac{g_{d2} + 2 g_{d1s1}}{g_{d1}} \frac{1}{g_{d1}} = -\frac{1}{2} \gamma_{\rm gate} R_j. \quad (12)$$

The same nomenclature as for the diode is used. Thus, the differential resistance of the FET channel at the chosen gate bias point is $R_j = (dI_{\rm ds}/dV_{\rm ds})^{-1} = 1/g_{d1}$. The slightly different position of R_s in the FET gives the similar result to the diode for the conjugately matched responsivity

$$\beta_{v,\max} \simeq \frac{1}{2} \gamma_{\rm gate} R_j \frac{R_j}{R_j + R_s} \frac{1}{1 + \omega^2 C_{\rm gs}^2 R_j R_s}. \quad (13)$$

Again, equality in (13) is under the condition that $R_j \gg Rs$. This is true in practice even for shorter gate lengths with bias

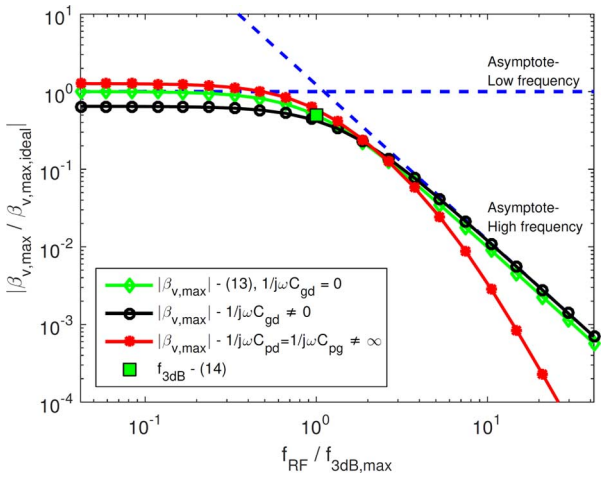

Fig. 2. Qualitative $\beta_{v,\max}$ with RF on gate port, normalized to the case when $1/j\omega C_{\rm gd} \to 0$. For the nonideal case $1/j\omega C_{\rm gd} \neq 0$, the capacitances are equal $C_{\rm gd} = C_{\rm gs}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

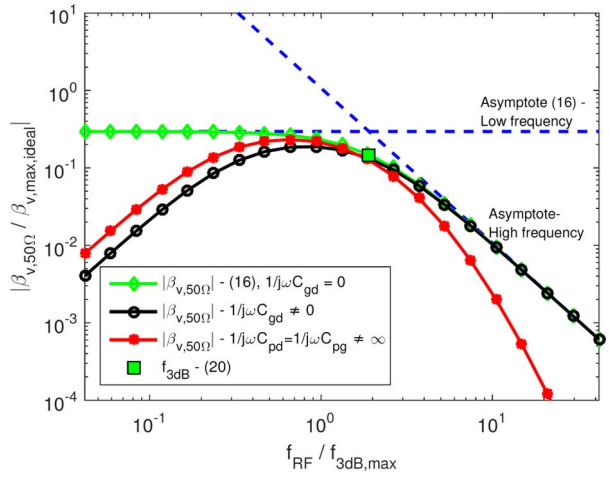

Fig. 3. Qualitative $\beta_{v,50\ \Omega}$ with RF on gate port, normalized to the ideal *matched* response. For the nonideal case $1/j\omega C_{\rm gd} \neq 0$, the capacitances are equal $C_{\rm gd} = C_{\rm gs}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

for optimum sensitivity in the majority of FETs [14], [19]. However, care must be taken in short gate-length GFETs due to the lack of band gap and the consequently missing off-state. A closer inspection of (13) reveals the same $1/f^2$ dependence at high frequencies as for the diode. In the low-frequency limit with negligible R_s, (13) simplifies into (12). Utilizing the low- and high-frequency limit expressions together, the 3-dB frequency of halved responsivity is derived to be

$$f_{3\ \rm dB,max} \approx \frac{1}{2\pi C_{\rm gs}\sqrt{R_j R_s}}. \tag{14}$$

Typical curves are shown in Fig. 2. The inclusion of a finite $1/j\omega C_{\rm gd}$ decreases the low-frequency responsivity, while the high-frequency values still match. The 3-dB frequency is reduced further by including the parasitic gate pad capacitances $C_{\rm pg} = C_{\rm pd}$. A $1/f^4$ region also appears.

2) Responsivity With Arbitrary Source Impedance: Under general impedance conditions the responsivity will be reduced as quantified by the mismatch factor, M_s. This is determined by the input impedance, $Z_{\rm in}$, at the gate port with *drain open terminated*. The input impedance is calculated from the standard 50-Ω two-port S-parameters [40] used for the extraction of the model parameters in Fig. 1(b). As for the diode, the relation between measured responsivity, β_v, and conjugately matched responsivity, $\beta_{v,\max}$, is then

$$\beta_v = \beta_{v,\max} \cdot M_s = \beta_{v,\max} \cdot \left(1 - \left|\frac{Z_{\rm in} - Z_s}{Z_{\rm in} + Z_s}\right|^2\right). \tag{15}$$

Curves based on (15) are shown in Fig. 3. A finite $1/j\omega C_{\rm gd}$ results in a maximum of the responsivity at a certain frequency.

The corresponding FET input impedance looking into the gate port is presented in Fig. 4. Note that both the real and imaginary parts for the intrinsic FET impedance decreases with frequency. As a result, the *intrinsic* mismatch factor to 50 Ω shown in Fig. 5 improves with frequency. Consequently, the responsivity at 50 Ω approaches the matched value at high frequencies, as was seen in Fig. 2. The input impedance is easily interpreted

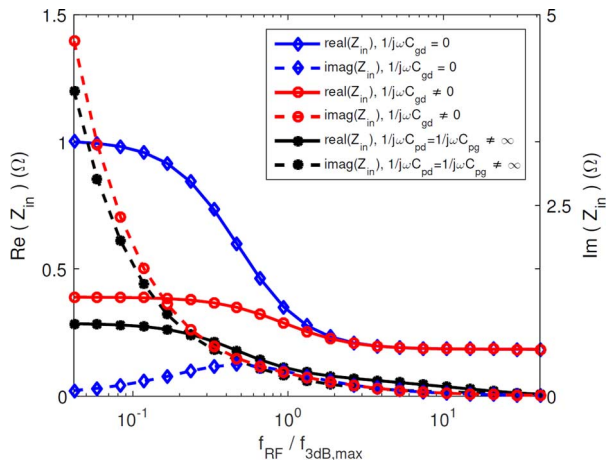

Fig. 4. Qualitative $Z_{\rm in}$ with RF on gate port normalized to the real part when $1/j\omega C_{\rm gd} \to 0$. For the nonideal case $1/j\omega C_{\rm gd} \neq 0$, the capacitances are equal $C_{\rm gd} = C_{\rm gs}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

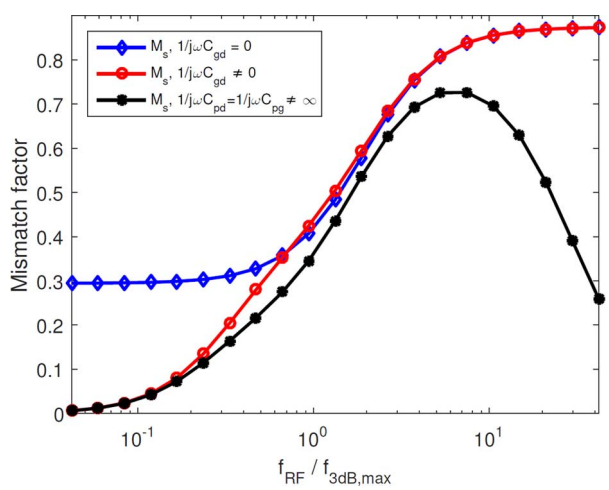

Fig. 5. Qualitative M_s to 50 Ω with RF on gate port with and without the ideal $1/j\omega C_{\rm gd} \to 0$. For the nonideal case $1/j\omega C_{\rm gd} \neq 0$, the capacitances are equal $C_{\rm gd} = C_{\rm gs}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

and physically reasonable, as opposed to impedance estimations in the plasma-wave theory [27] and when treating the gate as a transmission line [22].

A representative case is $R_j \gg Z_s$, such as a probed 50-Ω system. The voltage responsivity in closed form is then

$$\beta_v = \frac{\beta_v(0)}{1+\left(\frac{\omega}{\omega_1}\right)^2}. \tag{16}$$

The corresponding low-frequency responsivity is

$$\beta_v(0) = \frac{2Z_s\gamma_{\rm gate}}{g_{d1}^2\left(\frac{1}{g_{d1}}+R_s+Z_s\right)^2} \tag{17}$$

and the model corner frequency is

$$\omega_1 = \frac{g_{d1}\left(\frac{1}{g_{d1}}+R_s+Z_s\right)}{C_{\rm gs}(R_s+Z_s)}. \tag{18}$$

For the high-frequency limit, (16) yields

$$\beta_v(\omega) \approx \frac{2Z_s\gamma_{\rm gate}}{\omega^2 C_{\rm gs}^2(R_s+Z_s)^2}. \tag{19}$$

This makes it possible to define the 3-dB frequency as

$$f_{3\ {\rm dB},50\ \Omega} \approx \frac{(R_j+R_s+Z_s)}{R_j}\cdot\frac{1}{2\pi C_{\rm gs}(R_s+Z_s)}. \tag{20}$$

The frequency-dependent counterpart to (6) for the diode is

$$\beta_v(\omega) = \frac{2Z_s\gamma_{\rm gate}}{1+\omega^2 C_{\rm gs}^2(R_s+Z_s)^2}. \tag{21}$$

Including the parasitic pad capacitances $C_{\rm pg} = C_{\rm pd}$, the low-frequency responsivity is improved. However, the roll-off contains a $1/f^4$ region. This is shown by the black dashed lines in Figs. 2 and 3. This is due to the shunting of $C_{\rm pg}$. The mismatch factor in Fig. 5 has a maximum for the same reason.

C. RF Drain Coupling

In the drain-coupling scheme the RF signal is fed directly to the rectifying nonlinearity. However, ac grounding of the gate is necessary, as previously discussed in [27]. This is seen by looking at the intrinsic FET when $C_{\rm gd} = C_{\rm gs}$. It follows that $v_{\rm gsi} \to v_{\rm dsi}/2$. Now from (12) with $g_{d2} = -g_{d1s1}$, as a consequence, $\beta_{v,\max} \to 0$. If instead, $1/j\omega C_{\rm gs} \to 0$ or $1/j\omega C_{\rm pg} \to 0$, $v_{\rm gsi} \neq v_{\rm dsi}/2$ and $\beta_{v,\max} \neq 0$. The asymmetry in control voltages in our method is an analogy to the asymmetry condition between gate and drain in [24].

Under these asymmetry conditions, we have again reduced the FET to a diode-like circuit. In this case, the feedback capacitance, $C_{\rm gd}$, has to be minimized. This is since $C_{\rm gd}$ now plays the role of $C_{\rm gs}$ in the gate-coupling case or the diode junction capacitance C_j. The equivalent of the diode series resistance or FET source resistance for the gate-coupled FET depends on how the gate is ac grounded. It is either the sum of drain and source resistances $(R_d + R_s)$ if $1/j\omega C{\rm gs} \to 0$ or simply R_d if $1/j\omega C_{\rm pg} \to 0$, as R_s is short circuited.

1) Conjugately Matched Responsivity: Looking on the ideal drain-coupled FET without parasitics, under both conditions $1/j\omega C_{\rm gs} \to 0$ and $1/j\omega C_{\rm pg} \to 0$, the result is the same. The ideal matched drain-coupled responsivity contains only the g_{d2} derivative as given by

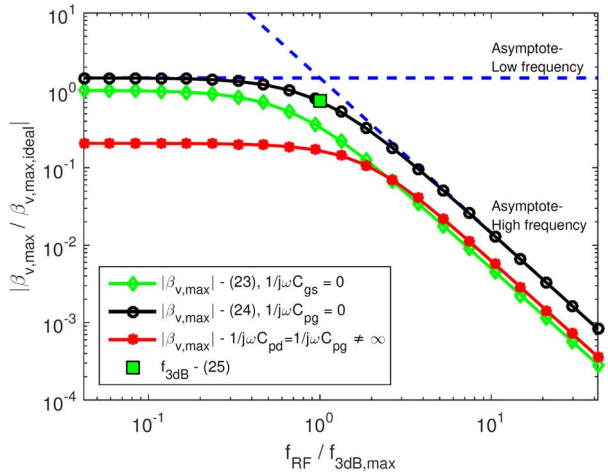

Fig. 6. Qualitative $\beta_{v,\max}$ with RF on drain port, normalized to the case when $1/j\omega C_{\rm gs} \to 0$. For the nonideal case $1/j\omega C_{\rm gs} \neq 0$, the capacitances are equal $C_{\rm gs} = C_{\rm gd}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

$$\beta_{v,\max} = -\frac{1}{2}\frac{g_{d2}}{g_{d1}}\frac{1}{g_{d1}} = -\frac{1}{2}\gamma_{\rm drain}R_j. \tag{22}$$

Thus, it is exactly the same expression as for the diode since $v_{\rm gs1} \to 0$. Further, if $g_{d2} \approx -g_{d1s1}$, the matched responsivity with RF incident on drain is of the same magnitude, but with the opposite sign compared to coupling RF on the gate. However, when inserting the intrinsic FET capacitors $C_{\rm gs} = C_{\rm gd}$ and the parasitic series resistances $R_s = R_d$ into the circuit, the two cases are different.

First, if the FET is made such that $1/j\omega C_{\rm gs} \to 0$, then

$$\beta_{v,\max} \simeq \frac{1}{2}\gamma_{\rm drain}R_j\frac{R_j}{R_j+R_s+R_d}\frac{1}{1+\omega^2 C_{\rm gd}^2 R_j(R_s+R_d)}. \tag{23}$$

It corresponds to the gate-coupled FET with twice the series resistance. Equality is conditioned by $R_j \gg (R_s + R_d)$. The curve from (23) is shown by the green line in Fig. 6.

Second, if instead the condition $1/j\omega C_{\rm pg} \to 0$ prevails, then

$$\beta_{v,\max} = \frac{R_j^3\left(g_{d2}-\frac{2g_{d1s1}R_s}{R_j}\right)}{2(R_j+R_d+R_s)}\frac{1}{1+\omega^2 C_{\rm gd}^2 R_j R_d}. \tag{24}$$

This is shown as the black line in Fig. 6. In the limit of low-frequency and negligible series resistances, (24) reduces to (22). Clearly the mixed derivative needs to be included only if $R_s \neq 0$. Again, the $1/f^2$ dependence at high frequencies is evident. Likewise, the 3-dB frequency is in complete analogy with the gate-coupled FET and is given as

$$f_{3\ {\rm dB},\max} \approx \frac{1}{2\pi C_{\rm gd}\sqrt{R_j R_d}}. \tag{25}$$

The drain-coupled FET with $1/j\omega C_{\rm pg} \to 0$ gives the best responsivity of the different schemes analyzed in this paper.

2) Responsivity With Arbitrary Source Impedance: Just as for the diode and the gate-coupled FET, mismatch decreases the responsivity if connecting the drain to a 50-Ω source. This is illustrated in Fig. 7. Given that $R_j \gg Z_s$, the responsivity plotted by the green line and the 3-dB frequency are from (16)–(21).

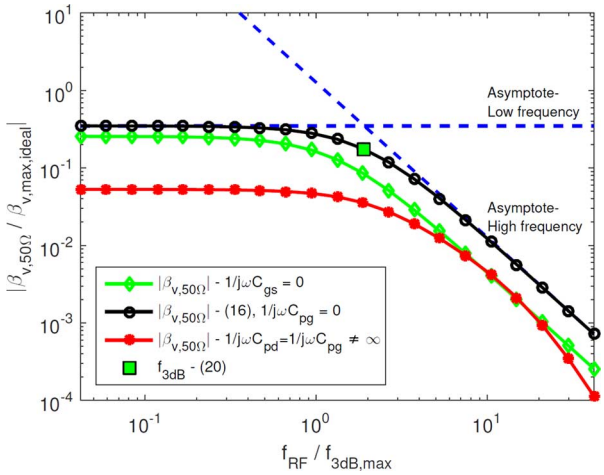

Fig. 7. Qualitative $\beta_{v,50\ \Omega}$ with RF on drain port, normalized to the ideal *matched* response. For the nonideal case $1/j\omega C_{\rm gs} \neq 0$, the capacitances are equal $C_{\rm gs} = C_{\rm gd}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

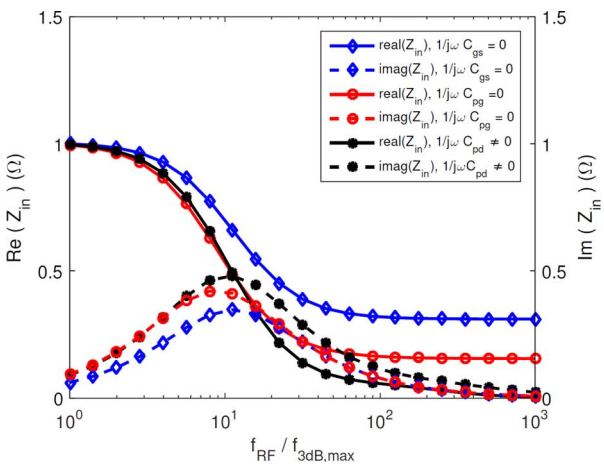

Fig. 8. Qualitative $Z_{\rm in}$ with RF on drain port normalized to the real part when $1/j\omega C_{\rm gs} \to 0$. For the nonideal case $1/j\omega C_{\rm gs} \neq 0$, the capacitances are equal $C_{\rm gs} = C_{\rm gd}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

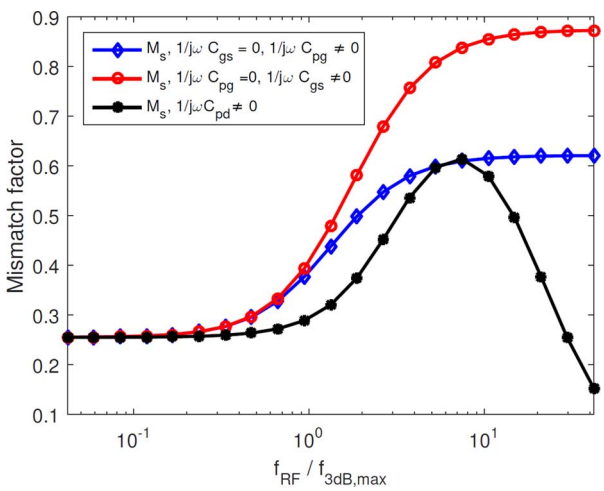

Fig. 9. Qualitative M_s to 50 Ω with RF on drain port with and without the ideal $1/j\omega C_{\rm gs} \to 0$. For the nonideal case $1/j\omega C_{\rm gs} \neq 0$, the capacitances are equal $C_{\rm gs} = C_{\rm gd}$. The pads are assumed to have $C_{\rm pg} = C_{\rm pd} = 10$ fF.

The components $C_{\rm gs}$, R_s, and $\gamma_{\rm gate}$ are replaced by $C_{\rm gd}$, R_d, and $\gamma_{\rm drain}$, respectively.

Details of the input impedance as seen from the drain and the resulting mismatch factor are shown in Figs. 8 and 9. The mismatch factor is better in the low-frequency region. This is related to the fact that the imaginary part exhibits a maximum versus frequency. Just as for the gate-coupling scheme, the mismatch factor improves with frequency. The exception is when the parasitic capacitance $C_{\rm pd}$ is included.

In addition, $C_{\rm pd}$ gives a $1/f^4$ region for the responsivity in 50 Ω. This is shown by the red line in Fig. 7. Inductances increases the responsivity at intermediate frequencies, while above this range an even steeper decrease is anticipated.

D. FET Detector Layout Design Optimization

In the previous sections, the issue of modeling FET power detectors was approached using Volterra series. Based on the derived closed-form expressions, we will now consider the optimization problem in device design. The derived scaling behavior applies to both the gate-coupled device, which obeys (13) and (14), as well as the drain-coupled device, following (23) and (25). The analysis includes the intrinsic FET and series resistances for a symmetrical and zero-biased device. This suggests equal contact resistances, $R_s \approx R_d = \rho_c/W_g$, and equally divided gate capacitance, $C_{\rm gs} \approx C_{\rm gd} = C_{\rm ox}W_gL_g/2$. Here, ρ_c is the contact resistance normalized to gate width while $C_{\rm ox}$ is gate–oxide capacitance per area. In a similar manner, the drain current scales as $I_{\rm ds} \propto W_g/L_g$. This means that all the drain voltage derivatives, $g_{d1}, g_{d2}, g_{d1s1} \propto W_g/L_g$. As a consequence, the ratios in the FET curvatures $\gamma_{\rm gate}$ and $\gamma_{\rm drain}$ are independent of the dimensions.

Adopting these scaling rules indicates for the *low-frequency* matched responsivity, $\beta_{v,\max} \propto \gamma/g_{d1} \propto L_g/W_g$. On the contrary, the *high-frequency limit* as quantified by the 3-dB frequency is insensitive to width, but scales inversely with gate length, $f_{3\ {\rm dB},\max} \propto 1/L_g^{3/2}$. Importantly, note the opposite dependencies in between low-frequency $\beta_{v,\max}$ and $f_{3\ {\rm dB},\max}$. This contradiction implies an optimum gate length to reach the lowest NEP given a certain frequency of operation. Assuming the frequency is ω and that $R_j \gg R_s$, by inserting (13) into (11) and differentiating we arrive at

$$L_{g,{\rm NEP}_{\rm opt,min}} = \left(\frac{R_{\rm sh}\rho_c C_{\rm ox}^2\omega^2}{2}\right)^{-1/3}. \qquad (26)$$

In (26), $R_{\rm sh}$ is the sheet resistance of the FET channel for a chosen gate bias. Notably, typical FET terahertz detectors achieve lowest NEP close to the threshold voltage. At such bias where $R_{\rm sh}$ is large, the trend is a monotonically decreasing matched NEP to the smallest realizable gate lengths. In practice, the trend should saturate due to fringing fields expected to set a lower limit for the gate capacitance [46].

Likewise for a mismatched device from (21) into (11), independent of frequency ${\rm NEP}_{50\ \Omega,\min}$ occurs at $L_g \to 0$. This trend of reducing the *intrinsic* FET capacitance to improve NEP agrees with experimental scaling results [20]. However, it considerably differs from published plasma-wave models. In these models the performance in the broadband detection regime is at most a weak function of gate length [15], [24].

Conversely to the weak gate-length dependence, plasma-wave theory predicts a pronounced positive effect of high mobility for broadband detection [24], [27]. In spite of the substantially higher channel mobility at room temperature in III–V

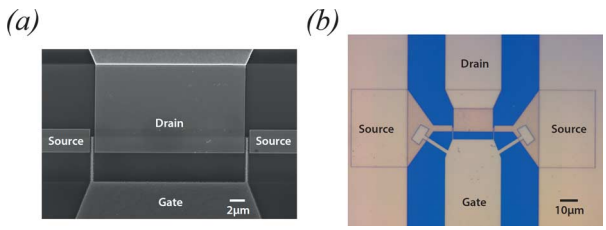

Fig. 10. (a) SEM image of standard GFET used to extract intrinsic capacitances from S-parameters and (b) optical image of detector GFET with extra $C_{\rm pg}$. Channel dimensions are $W_g = 2 \times 1.25$ μm and $L_g = 0.5$ μm for both.

HEMTs [14], they present modest sensitivity compared to the best Si MOSFETs [20]. This is captured in the current model, where no explicit mobility dependence is present. Instead, mobility is only included in $R_{\rm sh}$ inside $R_j = R_{\rm sh}L_g/W_g$. To emphasize the importance of R_j, by inserting (13) into (11) and differentiating we arrive at its value for $\mathrm{NEP}_{\rm opt,min}$,

$$R_{j,\mathrm{NEP}_{\min}} = \frac{1+\omega^2 C_{\rm gs}^2 R_s^2 + \sqrt{1+14\omega^2 C_{\rm gs}^2 R_s^2 + \omega^4 C_{\rm gs}^4 R_s^4}}{2\omega^2 C_{\rm gs}^2 R_s}. \tag{27}$$

Given $R_{\rm sh}$, there are no unique device dimensions to satisfy (27) and the attained $\mathrm{NEP}_{\min}$ are different. Designs with lowest $\mathrm{NEP}_{\min}$ are accompanied by the highest $R_{j,\mathrm{NEP}_{\min}}$. Therefore, the device dimensions must be selected as a compromise between the actual value $\mathrm{NEP}_{\min}$ and an $R_{j,\mathrm{NEP}_{\min}}$, which gives an adequate match to the RF source impedance. The problem of impractically high $R_{j,\mathrm{NEP}_{\min}}$ is relaxed at higher frequencies since the FET input impedance is reduced.

The considerations in this section are limited to drift conditions, i.e., under strong inversion bias in the FET channel. This is not a strong limitation since optimum NEP is reported to occur under such bias conditions [19]. The general trend when increasing the frequency to millimeter waves is a scaling towards smaller area detector FETs. Still, for the microwave range, a device with $L_g > 1$ μm might be the best choice.

IV. Model Validation

Devices with coplanar access pads were fabricated from CVD graphene by the procedures in [18] and [47] [see Fig. 10(a)]. A narrow gate width $W_g = 2 \times 1.25$ μm allows to study NEP under the condition $R_j \gg Z_s$. The gate-length dependence of NEP, as discussed in Section III-D, is studied via devices with $L_g = 0.5$ μm, $L_g = 1$ μm, and $L_g = 2$ μm. In the following, focus is on RF drain coupling. For this purpose, devices with external $C_{\rm pg}$ as overlapping metal–insulator–metal (MIM) capacitors were separately manufactured [see Fig. 10(b)].

First, responsivity was measured on-wafer with an Agilent 8275D signal generator and a Keithley 2000 multimeter in the 1–67-GHz band. The RF and dc paths on the drain port were separated by an external bias-tee. The RF power was calibrated using an Agilent E4419B power meter together with power sensors HP8487A (1–50 GHz) and V8486A (50–67 GHz). Correction for the measured probe loss was performed. The final input power ranged from 23 to 2 μW in $Z_s = 50$ Ω, which is well inside the linear regime of GFET detector operation. The measurement setup is shown in Fig. 11.

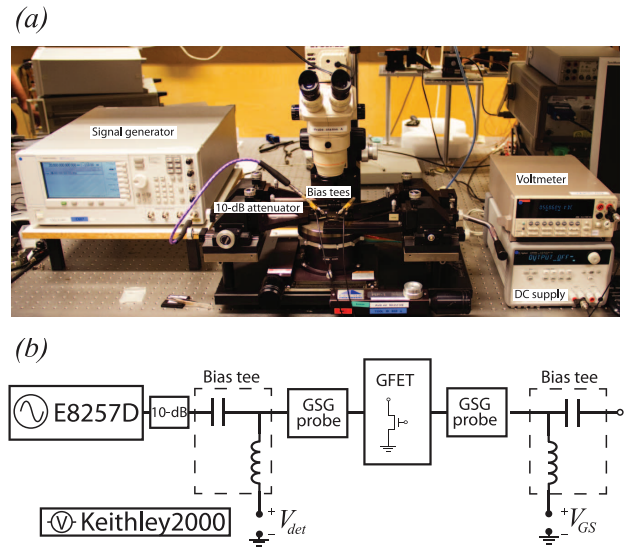

Fig. 11. (a) Photograph and (b) schematic drawing of the GFET power detector measurement setup outlined for RF drain coupling.

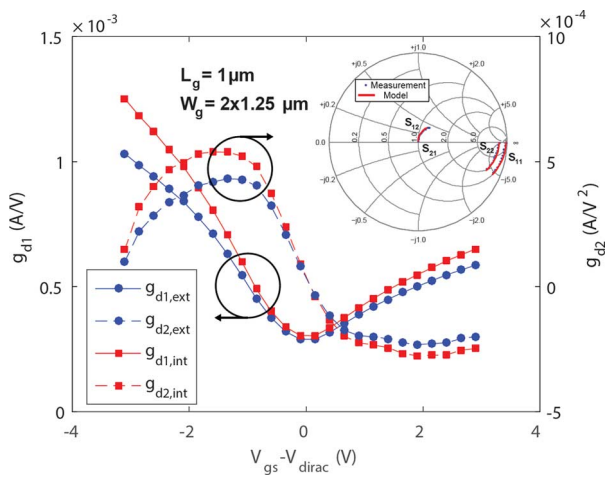

Fig. 12. Measured first-order, g_{d1}, and second-order, g_{d2}, drain voltage derivatives at $V_{\rm ds} = 0$ V versus $V_{\rm gs}$. The inset shows S-parameters for GFET with same dimensions without extra $C_{\rm pg}$ used to extract the intrinsic capacitors.

Second, dc measurements were performed in order to extract the Taylor coefficients used in the modeling procedure. To extract reproducibly the second-order derivatives, fifth-order polynomials were fitted to the measured output characteristics $I_{\rm ds}(V_{\rm ds})$ as $V_{\rm gs}$ is stepped. Finally, the derivatives are shifted to the reference plane of the intrinsic control voltages used in the model in Fig. 1(b). Under our current cold-FET bias conditions the intrinsic derivatives are given by

$$g_{d1i} = \frac{g_{d1e}}{1-(R_s+R_d)g_{d1e}} \tag{28}$$

and

$$g_{d2i} = \frac{g_{d2e}}{(1-(R_s+R_d)g_{d1e})^2}. \tag{29}$$

The contact resistances were found by fitting the measured transfer characteristics $I_{\rm ds}(V_{\rm gs})$ [41] and cross-checked by de-embedding S-parameters. The gate bias dependence for g_{d1} and g_{d2} for the $L_g = 1$ μm device are shown in Fig. 12. It was verified that $g_{d1s1} \approx -g_{d2}$ is a reasonable assumption.

TABLE I
LINEAR MODEL PARAMETERS, $W_g = 2 \times 1.25$ μm. THE PARASITICS ARE $R_g \approx 0$ Ω, $C_{\rm pg} = C_{\rm pd} = 2$ fF, $L_g = 20$ pH, $L_d = 10$ pH, AND $L_s = 5$ pH

L_g (μm)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	$R_s = R_d$ (Ω)	$NEP_{50\Omega,\ 67GHz}$ $\left(\text{pW/Hz}^{1/2}\right)$	$NEP_{opt,\ 67GHz}$ $\left(\text{pW/Hz}^{1/2}\right)$	$f_{3dB,50\Omega}$ (GHz)	$f_{3dB,max}$ (GHz)
0.5	3	5	4	60	40	10	170	65
1.0	5	6	3	85	85	25	125	40
2.0	6	8	3	130	130	45	90	30

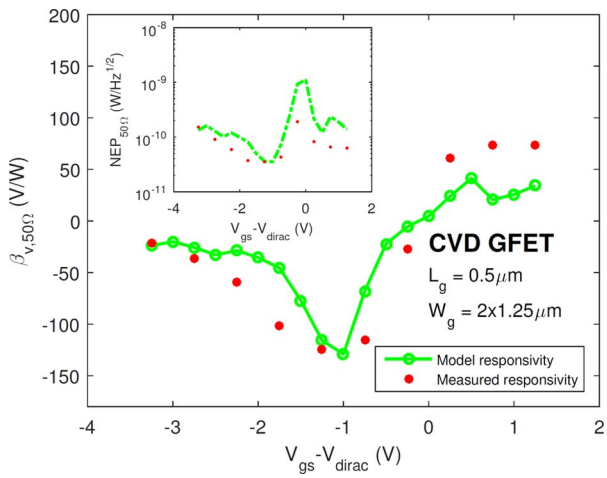

Fig. 13. Responsivity versus $V_{\rm gs}$ at $V_{\rm ds} = 0$ V and $f_{\rm RF} = 1$ GHz.

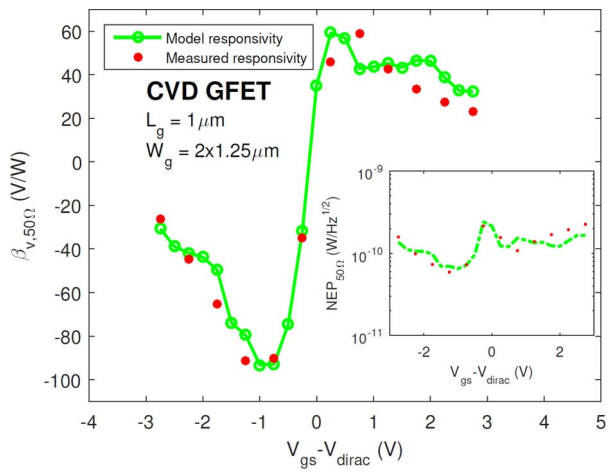

Fig. 14. Responsivity versus $V_{\rm gs}$ at $V_{\rm ds} = 0$ V and $f_{\rm RF} = 1$ GHz.

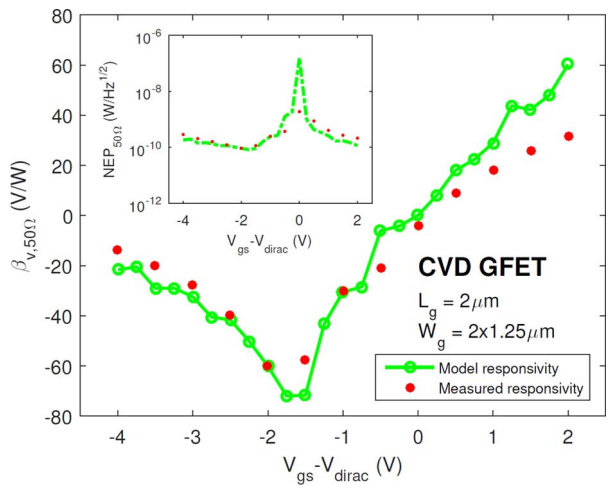

Fig. 15. Responsivity versus $V_{\rm gs}$ at $V_{\rm ds} = 0$ V and $f_{\rm RF} = 1$ GHz.

Third, the GFET S-parameters were measured on-chip up to 67 GHz using an Agilent E8391A VNA together with a thru-reflect-line (TRL) calibration substrate. Separate open and short de-embedding structures were measured to extract the parasitic capacitors and inductors, respectively. The intrinsic GFET capacitors are then extracted from the zero-bias FET two-port S-parameters [47]. The measured and modeled S-parameters for a $L_g = 1$ μm device at $V_{\rm GS} = V_{\rm DS} = 0$ V are shown in Fig. 12 inset. The capacitor variation with gate bias was negligible. All values of linear model parameters for the different gate lengths are summarized in Table I.

Finally, all parameters extracted from dc and S-parameter measurements are inserted into the closed-form Volterra model expressions of Section III-C for RF coupling on the drain. The $V_{\rm gs}$ variation of responsivity and NEP (insets) are verified for the different gate lengths in Figs. 13–15. The sign shift and asymmetry in the *IV* characteristics shown in Fig. 12 is directly reflected on the responsivity versus bias in Fig. 14. The same asymmetry was previously reported for GFETs at higher frequencies [18]. Furthermore, Figs. 16–18 gives the frequency dependence of NEP at optimum gate bias. Note that the simple closed-form expressions are used for the model curves. In addition to the $Z_s = 50$ Ω performance, the measured $\Gamma_{out} \approx S_{22}$ is used to calculate the mismatch factor and estimate the conjugately matched NEP values. For completeness, the corresponding responsivities are given in the insets. Despite the variation in device contact resistance, the pronounced positive effect of decreasing L_g on the most important figures-of-merit is highlighted in Table I. Record NEP values for GFETs in this frequency range [17] are obtained by realizing the designs of Section III-D.

Throughout Section III, the in-plane capacitance $C_{\rm ds}$ was disregarded compared to the vertical gate capacitors $C_{\rm gs}$ and $C_{\rm gd}$. However, considering the narrow gate width of the fabricated GFET detectors, $C_{\rm ds}$ becomes comparable to $C_{\rm gd}$. As it is in parallel to the nonlinearity in Fig. 1(b), it is important to account for in modeling the frequency roll-off. In Figs. 13–18, $C_{\rm ds}$ was empirically added directly in parallel to $C_{\rm gd}$ with excellent model agreement.

Complementary to the devices in Table I, the gate-width dependence was investigated when $L_g = 0.5$ μm. The result is presented in Table II. It conforms with the prediction of (16)

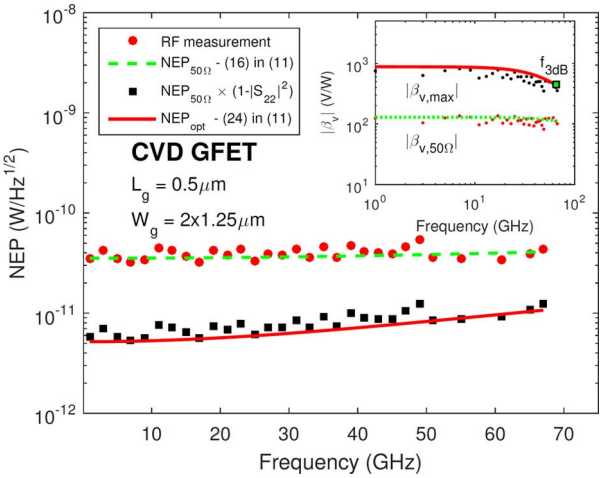

Fig. 16. Measured and modeled minimum NEP versus f_{RF} at $V_{\mathrm{ds}} = 0$ V.

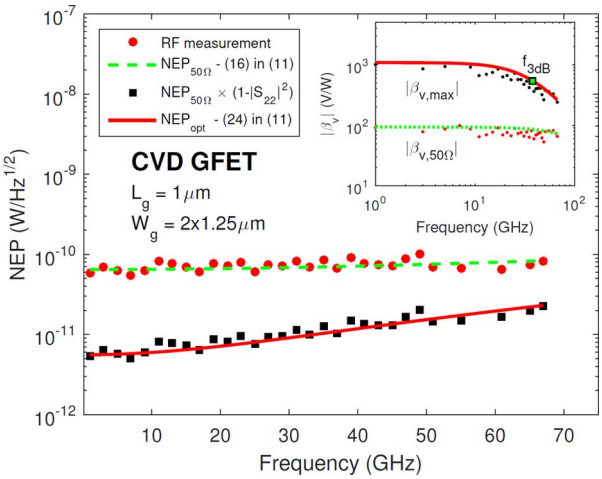

Fig. 17. Measured and modeled minimum NEP versus f_{RF} at $V_{\mathrm{ds}} = 0$ V.

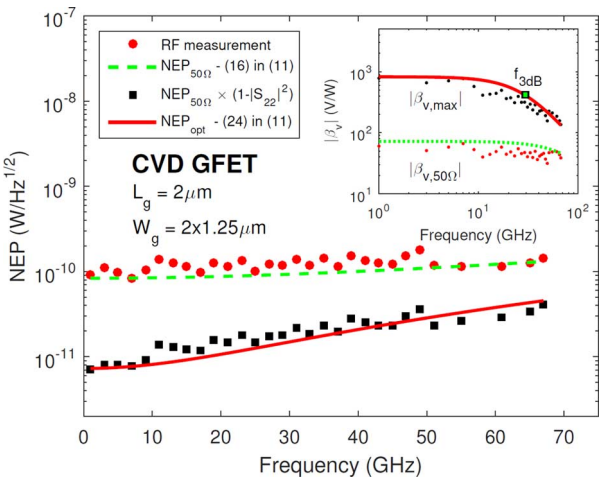

Fig. 18. Measured and modeled minimum NEP versus f_{RF} at $V_{\mathrm{ds}} = 0$ V.

and (24) inserted in (11), NEP_{opt} improves with decreasing W_g, while $\mathrm{NEP}_{50\ \Omega}$ is independent of W_g, respectively.

For comparison to the above results, the gate-coupling case was briefly investigated on a GFET without extra C_{pg}, [see Fig. 10(a)]. The results are given in Fig. 19 and essentially reproduces the predictions in Section III-B, especially the reversed sign for the responsivity compared to drain coupling and the effect of the limited C_{gd} at low frequencies. The values for

TABLE II
GATE-WIDTH SCALING OF NEP WHEN $L_g = 0.5\ \mu$m

W_g (μm)	2×1.25	2×2.5	2×5	2×10
$NEP_{50\Omega,\ 67GHz}$ $\left(\mathrm{pW/Hz^{1/2}}\right)$	40	45	45	60
$NEP_{opt,\ 67GHz}$ $\left(\mathrm{pW/Hz^{1/2}}\right)$	10	15	20	50

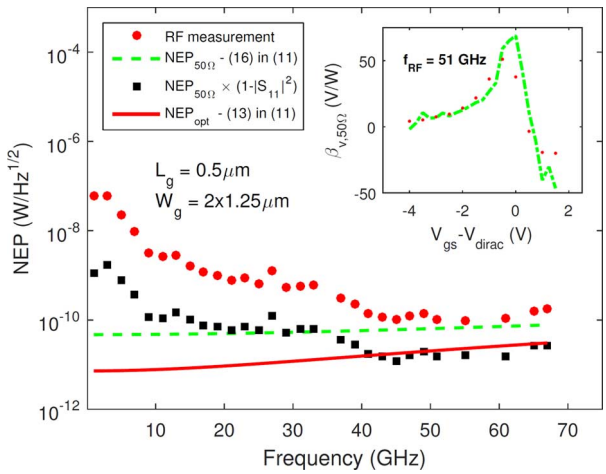

Fig. 19. Minimum NEP versus f_{RF} of a gate-coupled standard GFET at $V_{\mathrm{ds}} = 0$ V. The inset shows responsivity versus V_{gs} at $f_{\mathrm{RF}} = 51$ GHz.

$\mathrm{NEP}_{50\ \Omega}$ and NEP_{opt} at 67 GHz are approximately twice compared to the drain-coupled device in Table I given the same channel dimensions due to the higher $R_s = 200\ \Omega$.

V. Model Limitations and Implications

In this paper, GFETs are used as an example technology. Still, the model is applicable for other FET technologies based on suitable equivalent-circuit topologies. Furthermore, the extracted capacitances are expected to change weakly with frequency [34]. Thus, the model upper frequency limit is expected to exceed the measurement range here. By extrapolating the model from low frequency to 600 GHz, the levels for $\beta_{v,50\ \Omega} \sim 10$ V/W and $\mathrm{NEP}_{50,\Omega} \sim 500$ pW/Hz$^{1/2}$ are estimated, on the same order as the antenna-coupled GFET in [18]. However, additional characterization is necessary to unambiguously determine the frequency limits of the derived expressions. Numerically, the Volterra approach based on the circuit in Fig. 1(b) may be generalized to better approximate a distributed gate network [38] if required at higher frequencies. Suitable equivalent circuit topologies to account for nonquasi-static (NQS) effects at low V_{ds} are discussed in [48]. The first-order approximation is to include R_{gs} and R_{gd} in Fig. 1(b) [49]. For higher order circuits to be extracted empirically, optimization-based schemes are available [50]. By this, the reasoning is approaching the methods in [28]. Nevertheless, the Volterra understanding of the rectification mechanism would be classical nonlinearity and the parameter extraction traceable as opposed to plasma-wave models [24], [27]. Likewise, correspondence at higher frequencies might require inclusion of nonlinear capacitors generating terms at the fundamental frequency altering $v_{\mathrm{ds1}}(t)$ and $v_{\mathrm{gs1}}(t)$

in (9). Also, additional loss mechanisms can become important [51].

For the model to treat deviations from the FET linear region ($V_{\rm ds} \neq 0$), more terms have to be included in (10). This may enhance nonlinearity and, thus, responsivity, as previously reported [44]. This can be explained by larger g_{d2} and the fact that the last second-order term $g_{s2} \neq 0$. Similarly, the analysis in this paper is fundamentally limited to small-signal operation. To deal with saturation effects at high input powers, extensions are required at least in the Taylor expansion of $I_{\rm ds}$ in (8). Likewise, the design rules in Section III-D has to be reconsidered if $1/f$ noise contributions need to be considered.

In the Volterra picture, from Section III-D, the mobility is not a very decisive property. Instead, every zero-biased FET at $V_{\rm ds} = 0$ V has a fundamental limitation in smaller g_{d2} compared to zero-biased diodes. This apparent drawback for detection in the FET linear regime is what minimizes intermodulation in a FET resistive mixer at $V_{\rm ds} = 0$ V [52]. Nevertheless, the curvature in (2) can be comparable to diodes as the channel resistance may be very large in (or close to) the subthreshold gate bias regime. Thus, matching is more difficult for the FET. Considering the GFETs in this paper, the intrinsic curvature is $\gamma_i \lesssim 2\ V^{-1}$ as no distinct off-state for the current exists. This should be compared to Schottky diodes where $\gamma_i \sim 30\ V^{-1}$ [4] and for Sb backward diodes where $\gamma_i \sim 47\ V^{-1}$ [10] has been demonstrated. This is a serious limitation considering the limiting values $R_s \approx R_d$ and $C_{\rm gs} \approx C_{\rm gd}$ for a GFET are on the same order as the model analogues R_s and C_j for the diodes [5], [6], [10].

VI. Conclusions

In this paper, modeling of power detection in FETs was approached empirically. The nonlinearity of the drain current at zero drain bias is enough to predict the low-frequency rectified dc response. Closed-form expressions for high-frequency NEP were derived based on Volterra analysis. Similar to the diode detector, these contain the curvature, the intrinsic capacitances, and the parasitic resistances. The optimal detection scheme predicted was RF input on drain, while gate is capacitively grounded. Excellent model agreement to probed measurements on coplanar GFETs up to 67 GHz was found.

The closed-form expressions were utilized to analyze the FET detector concerning both the channel carrier properties and device dimensions. Carrier mobility was assigned a minor role in the resulting sensitivity. Instead, the currently worse GFET performance compared to CMOS is attributed to the inability to bias for a high-resistance off-state. This is, in turn, a consequence of the relatively higher linearity of FETs compared to detector diodes at zero bias. The importance of short gate length was predicted theoretically and verified experimentally. Above the 3-dB frequency of the FET detector, the NEP increases as f^2. Thus, it is of fundamental importance at terahertz frequencies to decrease intrinsic capacitance.

The presented model extends well into the submillimeter-wave range with minor modification. Natural extensions are the inclusion of high-frequency loss and nonlinear capacitances. Furthermore, it applies to any FET that operates as a small-signal power detector based on the same equivalent circuit.

Acknowledgment

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References

[1] F. Sizov and A. Rogalski, "THz detectors," *Progr. Quantum Electron.*, vol. 34, no. 5, pp. 278–347, Sep. 2010.
[2] L. Yujiri, M. Shoucri, and P. Moffa, "Passive millimeter-wave imaging," *IEEE Microw. Mag.*, vol. 4, no. 3, pp. 39–50, Sep. 2003.
[3] J. Zmuidzinas and P. L. Richards, "Superconducting detectors and mixers for millimeter and submillimeter astrophysics," *Proc. IEEE*, vol. 92, no. 10, pp. 1597–1616, Oct. 2004.
[4] J. L. Hesler and T. W. Crowe, "Responsivity and noise measurements of zero-bias schottky diode detectors," in *18th Int. Space Terahertz Technol. Symp.*, Mar. 2007, pp. 89–92.
[5] L. Liu, J. L. Hesler, H. Xu, A. W. Lichtenberger, and R. M. Weikle, "A broadband quasi-optical terahertz detector utilizing a zero bias Schottky diode," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 9, pp. 504–506, Sep. 2010.
[6] H. Kazemi *et al.*, "Ultra sensitive ErAs/InAlGaAs direct detectors for millimeter wave and THz imaging applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 1367–1370.
[7] D. C. W. Lo *et al.*, "A monolithic W-band high-gain LNA/detector for millimeter wave radiometric imaging applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1995, pp. 1117–1120.
[8] C. A. Burrus, "Backward diodes for low-level millimeter-wave detection," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-11, no. 5, pp. 357–362, Sep. 1963.
[9] J. N. Schulman and D. H. Chow, "Sb-heterostructure interband backward diodes," *IEEE Electron Device Lett.*, vol. 21, no. 7, pp. 353–355, Jul. 2000.
[10] Z. Zhang, R. Rajavel, P. Deelman, and P. Fay, "Sub-micron area heterojunction backward diode millimeter-wave detectors with 0.18 pW/Hz$^{1/2}$ noise equivalent power," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 5, pp. 267–269, May 2011.
[11] J. J. Lynch *et al.*, "Passive millimeter-wave imaging module with preamplified zero-bias detection," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 7, pp. 1592–1600, Jul. 2008.
[12] J. -Q. Lü, M. S. Shur, J. L. Hesler, L. Sun, and R. Weikle, "Terahertz detector utilizing two-dimensional electronic fluid," *IEEE Electron Device Lett.*, vol. 19, no. 10, pp. 373–375, Oct. 1998.
[13] J. D. Sun, Y. F. Sun, D. M. Wu, Y. Cai, H. Qin, and B. S. Zhang, "High-responsivity, low-noise, room-temperature, self-mixing terahertz detector realized using floating antennas on a GaN-based field-effect transistor," *Appl. Phys. Lett.*, vol. 100, pp. 013506-1–013506-4, 2012.
[14] Y. Kurita *et al.*, "Ultrahigh sensitive sub-terahertz detection by InP-based asymmetric dual-grating high-electron-mobility transistors and their broadband characteristics," *Appl. Phys. Lett.*, vol. 104, pp. 251114-1–251114-4, 2014.
[15] R. Tauk *et al.*, "Plasma wave detection of terahertz radiation by silicon field effect transistors: Responsivity and noise equivalent power," *Appl. Phys. Lett.*, vol. 89, pp. 253511-1–253511-3, 2006.
[16] L. Vicarelli *et al.*, "Graphene field-effect transistors as room-temperature terahertz detectors," *Nat. Mater.*, vol. 11, pp. 865–871, 2012.
[17] J. S. Moon *et al.*, "Graphene FET-based zero-bias RF to millimeter-wave detection," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1357–1359, Sep. 2012.
[18] A. Zak *et al.*, "Antenna-integrated 0.6 THz FET direct detectors based on CVD graphene," *Nano Lett.*, vol. 14, no. 10, pp. 5834–5838, 2014.
[19] E. Öjefors, U. R. Pfeiffer, A. Lisauskas, and H. G. Roskos, "A 0.65 THz focal-plane array in a quarter-micron CMOS process technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1968–1976, Jul. 2009.
[20] A. Lisauskas *et al.*, "Exploration of terahertz imaging with silicon MOSFETs," *J. Infrared. Millim. Terahertz Waves*, vol. 35, no. 1, pp. 63–80, Jan. 2014.
[21] A. M. Cowley and H. O. Sorensen, "Quantitative comparison of solid-state microwave detectors," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-14, no. 2, pp. 588–602, Dec. 1966.
[22] M. Sakhno, A. Golenkov, and F. Sizov, "Uncooled detector challenges: Millimeter-wave and terahertz long channel field effect transistor and Schottky barrier diode detectors," *J. Appl. Phys.*, vol. 114, pp. 164503-1–164503-18, 2013.
[23] S. Preu, S. Kim, R. Verma, P. G. Burke, M. S. Sherwin, and A. C. Gossard, "An improved model for non-resonant terahertz detection in field-effect transistors," *J. Appl. Phys.*, vol. 111, pp. 024502-1–024502-9, Jan. 2012.

[24] M. Dyakonov and M. Shur, "Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 380–387, Mar. 1996.
[25] W. Knap, Y. Deng, S. Rumynantsev, and M. S. Shur, "Resonant detection of subterahertz and terahertz radiation by plasma waves in submicron field-effect transistors," *Appl. Phys. Lett.*, vol. 81, pp. 4637–4639, 2002.
[26] A. E1. Fatimy *et al.*, "Resonant and voltage-tunable terahertz detection in InGaAs/InP nanometer transistors," *J. Appl. Phys.*, vol. 89, pp. 131926-1–131926-3, 2006.
[27] S. Boppel *et al.*, "CMOS integrated antenna-coupled field-effect transistors for the detection of radiation from 0.2 to 4.3 THz," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 3834–3843, Dec. 2012.
[28] A. Gutin, T. Ytterdal, V. Kachorovskii, A. Muraviev, and M. Shur, "THz SPICE for modeling detectors and nonquadratic response at large input signal," *IEEE Sensors J.*, vol. 13, no. 1, pp. 55–62, Jan. 2013.
[29] W. Stillman *et al.*, "Silicon FINFETs as detectors of terahertz and subterahertz radiation," *Int. J. High Speed Electron. Syst.*, vol. 20, no. 1, pp. 27–42, Mar. 2011.
[30] W. Knap *et al.*, "Nonresonant detection of terahertz radiation in field effect transistors," *J. Appl. Phys.*, vol. 91, pp. 9346–9353, 2002.
[31] M. Sakowicz *et al.*, "Terahertz responsivity of field effect transistors versus their static channel conductivity and loading effects," *J. Appl. Phys.*, vol. 110, pp. 054512-1–054512-6, 2011.
[32] A. Gutin, V. Kachorovski, A. Muraviev, and M. Shur, "Plasmonic terahertz detector response at high intensities," *J. Appl. Phys.*, vol. 112, pp. 014508-1–014508-5, 2012.
[33] A. Gutin, T. Ytterdal, A. Muravirv, and M. Shur, "Modelling effect of parasitics in plasmonic FETs," *Solid State Electron.*, vol. 104, pp. 75–78, Feb. 2015.
[34] W. R. Deal *et al.*, "Low noise amplification at 0.67 THz using 30 nm InP HEMTs," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 368–370, Jul. 2011.
[35] J. J. Bussgang, L. Ehrman, and J. W. Graham, "Analysis of nonlinear systems with multiple inputs," *Proc. IEEE*, vol. 62, no. 8, pp. 1088–1119, Aug. 1974.
[36] R. A. Minasian, "Intermodulation distortion analysis of MESFET amplifiers using the volterra series representation," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-28, no. 1, pp. 1–8, Jan. 1980.
[37] S. A. Maas, "Two-tone intermodulation in diode mixers," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-35, no. 3, pp. 307–314, Mar. 1987.
[38] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 7, pp. 1151–1159, Jul. 1988.
[39] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 7, pp. 891–895, Jul. 1990.
[40] G. Gonzalez*, Microwave Transistor Amplifiers: Analysis and Design*. Upper Saddle River, NJ, USA: Prentice-Hall, 1997.
[41] O. Habibpour, J. Vukusic, and J. Stake, "A large-signal graphene FET model," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 968–975, Apr. 2012.
[42] F. Fregonese, M. Magallo, C. Maneux, H. Happy, and T. Zimmer, "Scalable electrical compact modeling for graphene FET transistors," *IEEE Trans. Nanotechnol.*, vol. 12, no. 4, pp. 539–546, Jul. 2013.
[43] S. Rodriguez *et al.*, "A comprehensive graphene FET model for circuit design," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1199–1206, Apr. 2014.
[44] A. Lisauskas *et al.*, "Terahertz responsivity and low-frequency noise in biased silicon field-effect transistors," *Appl. Phys. Lett.*, vol. 102, pp. 153505-1–153505-4, 2013.
[45] J. B. Johnson, "Thermal agitation of electricity in conductors," *Phys. Rev.*, vol. 32, no. 1, pp. 97–109, Jul. 1928.
[46] H. Wang, A. Hsu, D. S. Lee, K. K. Kim, J. Kong, and T. Palacios, "Delay analysis of graphene field-effect transistors," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 324–326, Mar. 2012.
[47] M. Tanzid, M. A. Andersson, J. Sun, and J. Stake, "Microwave noise characterization of graphene field effect transistors," *Appl. Phys. Lett.*, vol. 104, pp. 013502-1–013502-4, 2014.
[48] S. C. Kang and P. Roblin, "Optimal second-order small-signal model for long- and short-channel three-terminal MOSFET/MODFET wave equation," *IEEE Trans. Electron Devices*, vol. 39, no. 8, pp. 1909–1915, Aug. 1988.
[49] M. Bagheri, "An improved MODFET microwave analysis," *IEEE Trans. Electron Devices*, vol. 35, no. 7, pp. 1147–1149, Jul. 1988.
[50] C. Van Niekerk, P. Meyer, D. M. M. -P. Schreurs, and P. B. Winson, "A robust integrated multibias parameter-extraction method for MESFET and HEMT models," *IEEE Trans. Microw. Theory Techn.*, vol. 48, no. 5, pp. 777–786, May 2000.
[51] A. Y. Tang and J. Stake, "Impact of eddy currents and crowding effects on high-frequency losses in planar schottky diodes," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3260–3269, Oct. 2011.
[52] S. A. Maas, "A GaAs MESFET mixer with very low intermodulation," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-35, no. 4, pp. 425–429, Apr. 1987.

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