Individual capacitor voltage balancing in H-bridge cascaded multilevel STATCOM at zero current operating mode

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Index Terms

Static Synchronous Compensator (STATCOM), Converter control, FACTS, High voltage power converters, Modulation strategy, Multilevel converters, Voltage Source Converter (VSC).

Abstract

Individual capacitor voltage balancing is one of the challenges in the field of multilevel converters, especially when the phase legs of the converter are connected in star configuration. This issue can be even more problematic when the converter is operating close to zero average current operating mode. This paper first shows the issue related to the capacitor voltage balancing at zero average-current mode and second proposes a novel algorithm to overcome this problem. The method proposes a modulation technique for individual balancing in H-bridge cascaded multilevel converters operated at zero average-current mode. The proposed algorithm modifies the conventional sorting algorithm based on current ripple. The individual DC-link voltage control method is applied to a 19-level star-connected cascaded converter in PSCAD and simulation results verify the ability of the proposed method in maintaining the balancing of the capacitors voltages at zero current injection mode. Several practical limitation such as forward voltage drop over semiconductor elements, noise in measured data, delay in the digital controller, switching deadtime, and grid voltage harmonics are also considered in the model.

INTRODUCTION

Modular multilevel converters are today widely implemented power converters for high-power high-voltage applications. The output voltage waveform of a multilevel converter is synthesized by selecting different voltage levels obtained from DC voltage sources of each module. In particular applications such as STATCOM, DC voltage sources can be replaced by capacitors since active power is not exchanged.

Among several challenges associated with modular multilevel converters, individual capacitor voltage balancing is one the main technical issue specially in STATCOM applications. To overcome this challenge, several different modulation techniques based on sorting algorithm have been proposed in the literature [2],[3]. Sorting algorithm can be implemented by Carrier-Disposition PWM (CD-PWM) [4], Nearest Level Control (NLC) [5],[6],[7], Nearest Vector Control (NVC) [8],[9], Distributed Commutations Modulation (DCM) [10] or predictive sorting algorithm [11]. In order to reduce or completely remove the common mode switching actions, many papers propose different modified sorting algorithms. This has been done in [12] by using Phase-Shifted PWM (PS-PWM) and choosing the cells with highest and lowest voltage only, instead of sorting all the capacitor voltages. The same algorithm where CD-PWM is proposed in [13]. A modification on NLC to remove the common modes is proposed in [14]. Reference [15] Proposes three different methods to deal with this problem, which are mainly based on predictions.

Although sorting algorithm is an effective solution for voltage balancing when the converter is exchanging current with the grid, less attentions have been paid for zero average-current operating mode (which is standby mode for

STATCOM) in literature. Sorting algorithm needs current sign information to provide a correct sorting pattern. As a consequence, when the exchanging current that flows in the cells is zero the sorting algorithm is unable to take the correct insertion decision for proper balancing of the capacitor voltages. In practical applications, this is even more problematic when noise is also added in the measured current signal.

Among the multilevel topologies, those with circulating current ability such as delta- connected cascaded converter suffer less from this problem. A circulating current can flow inside the delta (without grid exchange) at zero current mode and can be used for balancing purposes. On the other hand, star-connected cascaded configuration does not have the benefit of the circulating current since any circulating current in the phase leg equals the current exchanged with the grid.

This paper proposes a solution for capacitor voltage balancing at zero current mode. The method proposes a modified sorting algorithm for capacitor balancing at zero current mode with a star-connected cascaded converter. Observe that the same approach can be used for delta configuration. It is of importance to stress that the investigated method is for zero-current condition only, since when a current circulates in the phase leg the classical sorting can be adopted. The proposed modified sorting algorithm is verified via simulation using PSCAD simulation tool. In order to assess the sensitivity of the proposed method, white noise is added to the cell voltage and line current measurement signals. Other practical limitations such as delay in the discrete controller, deadtime for switches, voltage drop over diodes and grid voltage harmonics are also considered in the simulation model. The obtained results show the ability of the proposed method to maintain capacitor balancing at zero current mode.

H-BRIDGE CASCADED MULTILEVEL STATCOM

Topology and control overview

Figure 1 shows the line-diagram of a H-bridge cascaded multilevel converter in star configuration and its overall control block diagram. The control method is a *dq*-based cascade control strategy, where the inner loop aims at controlling the converter current components and the outer loops are to control the capacitor voltages at each phase. A Phase Lock Loop (PLL) estimates the transformation angle θ in order to obtain all the *dq* quantities.The outer control loops determine the reference direct and quadrature component of the current based on desired DC-link voltage and desired reactive power.

The inner current control loop [1], based on a PI regulator, generates the reference voltages for each phase. The aim of outer loop control is to generate the required reference direct and quadrature component of the current. Since the *dq* transformation is synchronized with the grid voltage, the quadrature component of the current is associate with the reactive power and direct component is associate with the active power. Therefore, the direct component can be used to compensate the STATCOM losses and regulate the DC-link voltage.

To generate the reference direct component of the current, cluster voltages are fed into the cluster control block. Cluster voltage is defined as the average voltage of all cell voltages in each phase leg. The cluster controllers, based on single-phase DC-link voltage controllers, aim to control the average energy stored in the DC-link capacitors. Mathematical equations for cluster controller are as follow:

$$v_{ca,ave} = \frac{\sum_{i=1}^{N} v_{cai}}{N} \ , \ v_{cb,ave} = \frac{\sum_{i=1}^{N} v_{cbi}}{N} \ , \ v_{cc,ave} = \frac{\sum_{i=1}^{N} v_{cci}}{N} \tag{1}$$

$$\begin{aligned} i_{a,ref} &= k(v_{dc,ref}^2 - v_{ca,ave}^2)\cos(\theta) \\ i_{b,ref} &= k(v_{dc,ref}^2 - v_{cb,ave}^2)\cos(\theta - \tfrac{2\pi}{3}) \\ i_{c,ref} &= k(v_{dc,ref}^2 - v_{cc,ave}^2)\cos(\theta + \tfrac{2\pi}{3}) \end{aligned} \tag{2}$$

where cos(θ) is to generate an AC current in phase with the grid voltage, $v_{cai}, v_{cbi}, v_{cci}$ are capacitor voltages of each cell for the corresponding phase and k is the cluster control proportional gain. These three phase currents are then transferred to the dq-reference frame to generate the desired reference direct component of the current.

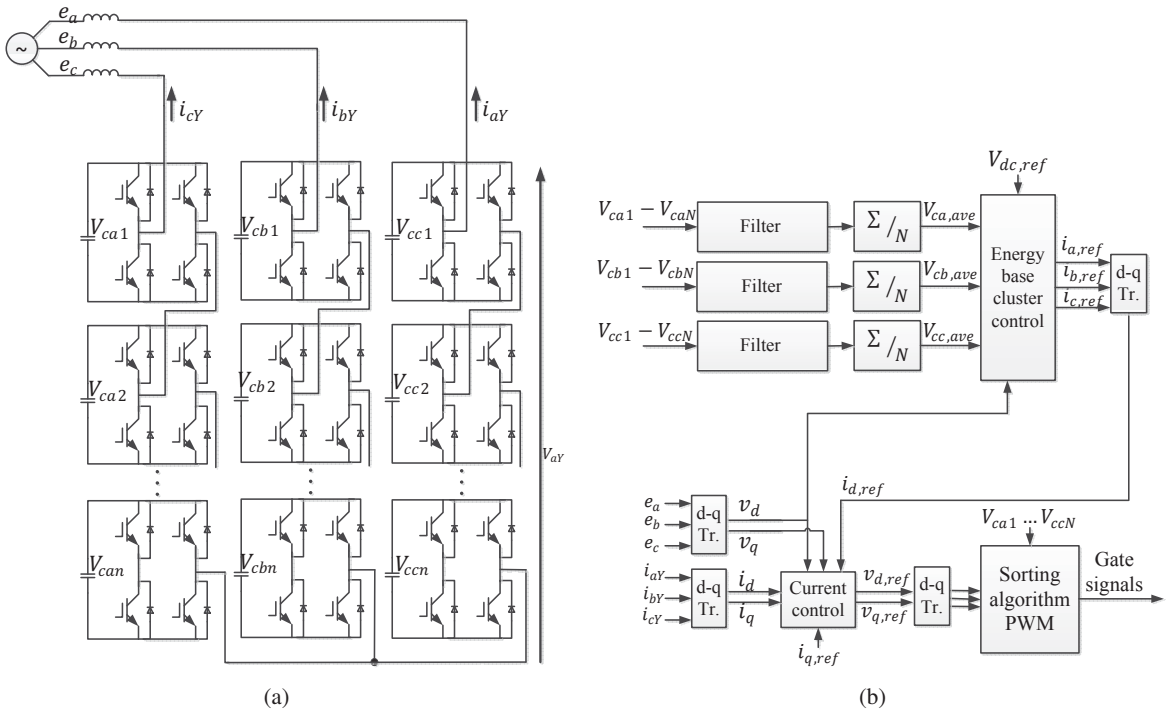

Figure 1. H-bridge star-connected cascaded multilevel converter with control block diagram. (a) topology, (b) control.

Sorting algorithm and modulation technique

The current controller sends the three-phase voltage references to the modulator. At the beginning of each control cycle, the minimum number of cells to be inserted (direct or reverse), and the fractional part of the voltage references are determined. The fractional part is then properly scaled and compared with a carrier.

If the state of the phase leg is in the charging mode (considering the direction of the current to be toward the converter, charging mode is when reference voltage and current at each phase have the same sign) then capacitors at each phase are sorted in ascending order. The required numbers of cells that are supposed to be inserted are chosen from the capacitors with the lowest voltage. For the remaining capacitors, the one with the lowest voltage is chosen to be modulated by the fractional part of the voltage reference. The rest of the cells are fully bypassed.

The same process can be used for discharging mode (voltage and current at each phase are in opposite sign). But at the discharging mode the capacitors with highest voltages are used instead.

For practical implementation, $floor$ and *rem* commands can be used for the sorting PWM. $floor(x)$ returns the nearest positive integer lower or equal to x. $rem(a/b)$ returns the fractional part of a divided b. For example if the reference voltage in one phase is -19 kV and each cell voltage is $V_{dc} = 3.33\ kV$, then $floor(-19/3.33)$=5 and $rem(-19/3.33)$=-2.35. The fractional part of the reference voltage is normalized with the cell voltage and will be used to modulate a cell. In this example eventually 5 cells must be reversed inserted and one cell must be modulated with the fractional part.

ZERO CURRENT OPERATING MODE

Figure 2 shows the principle of operation of unipolar PWM when reference voltage is positive. The reference value in Fig. 2 is the fractional part of the reference voltage.

As shown in the right figure, if the RMS value of the current becomes zero, the sign of the instantaneous current will change in the middle of two sampling points. This implies a discharging following by a charging state during one control cycle. The same sign change is observable when reference voltage is negative. When reference voltage is negative, the instantaneous current is positive in the first half cycle and is negative in the second half. This implies again a discharging following by a charging state during one control cycle.

The sorting algorithm PWM determines the switching pattern during one control cycle based on the charging or discharging mode; however the sign of the instantaneous current at zero current mode shows that a single detection in the beginning of each control cycle is not sufficient to determine the sorting pattern. Therefore, the detection of charging or discharging, and consequently the sorting pattern, must be updated in the middle of two sampling points.

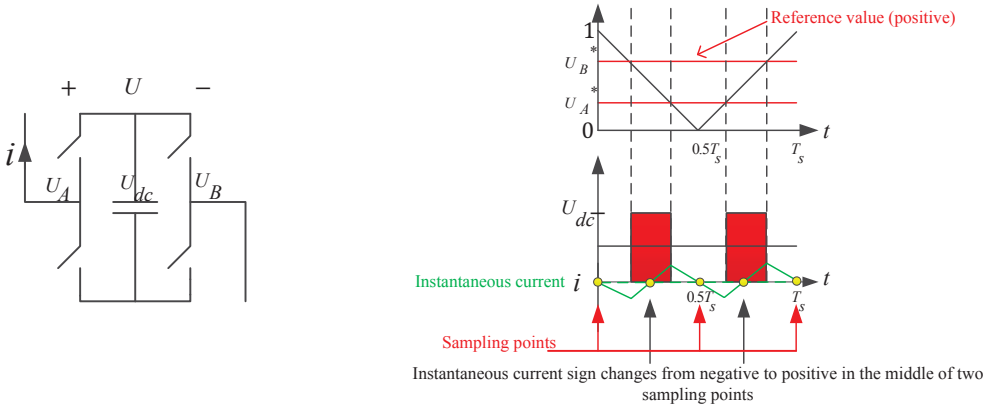

Figure 2. Zero current mode operation in unipolar PWM and positive reference voltage. (left) H-bridge converter, (right) unipolar PWM principle.

The conventional sorting algorithm is applied to a 19-level star-connected cascaded converter in PSCAD. Table I shows the system parameters selected for the simulation study.

Table I
CIRCUIT PARAMETERS IN FIG. 1

Rated appearance power	S	120 MVA
Nominal line to line rms voltage	V_s	33 kV
Filter inductance	L	4.3 mH (0.15 pu)
Filter resistor	R	0.136 Ω (0.015 pu)
DC bus voltage of each cell	V_{dc}	3.33 kV
Carrier frequency for PWM	f_c	500 Hz
Grid frequency	f_o	50 Hz
Number of cells per phase	N	9
Capacitor size	C	4mF (0.087pu)

In order to provide more realistic model, the capacitors in each cell are paralleled with a resistor. This resistor is to model the internal losses in the cell and is chosen to be different from cell to cell. In addition to the resistors, $\pm 20\%$ deviation is chosen for capacitors sizes (3.2 to 4.8 mF). This amount of deviations are exaggerated quantities in order to speed-up the voltage deviation.

Figure 3 shows the simulation results when using the conventional sorting algorithm. Figure 3 (top) shows the line current in phase *a* while the lower figure shows the capacitor voltages in phase *a*. Similar behavior can be observed

for the other phases. All figures are showing the measured quantities in per unit. At t=0.9 S, the reactive current is changed from 0.35 pu to zero. Figure. 3 shows that conventional sorting algorithm is not able to provide proper individual cell balancing at zero current mode.

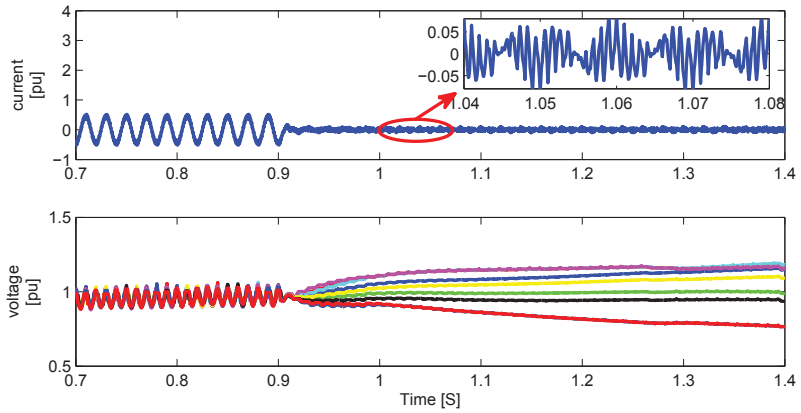

Figure 3. Capacitor voltages and line current in phase *a* without the proposed method. (top) line current, (bottom) capacitor voltages.

Figure 4 shows a zoom of a cell output voltage, line current between two sampling points and interrupt signals. It can be observed from this figure that the sign of the current is negative in the first half of the control period and changes to positive after almost half of the period as anticipated in the previous section. Theoretically, at zero current operating mode, the current sign changes exactly in the middle of the control period. This provides equal positive and negative areas which lead to equal charging and discharging. Consequently the capacitor voltage should remain constant. However in practical applications this symmetry will not be achieved, leading to slightly more charging or discharging area in this specific example. Consequently capacitor voltages will not remain constant and diverge from their reference values.

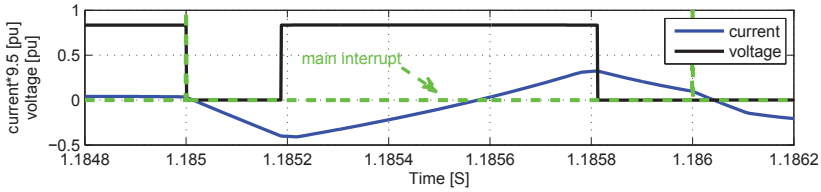

Figure 4. Cell output voltage and line current (Current is multiplied by 9.5) together with main interrupts.

PROPOSED SOLUTION

The proposed method takes advantage of the knowledge of the sign of the current ripple in zero current mode. In STATCOM applications even if the reactive current is zero, there is always a small active current flowing in order to keep the charge of all capacitors and compensate for the losses. In this case the RMS value of the current is not zero. This is beneficial for sorting algorithm since a small flowing current with small ripple amplitudes can be used for the sorting algorithm PWM. But measurement noise can affect the detection accuracy of charging or discharging mode. The noise amplitudes can become bigger than the actual current.

In this section a solution is proposed, which is independent from measuring the current. The proposed method assumes that the ripple amplitudes are bigger than the RMS value when the exchanging current is small and thus ripples sign are pretty similar to the zero current mode.

As explained in the previous section, at zero current mode the control cycles always start by discharging mode and in the middle of the control cycle changes to charging mode. Due to this fact, current and voltage measurement are not needed anymore to detect the charging or discharging modes.

In the proposed method two sets of interrupts are used. The main interrupt is synchronized with the top and bottom of the main carrier; this interrupt is used for sampling of the measured quantities. The second interrupt is located between the two sampling points. The second interrupt is introduced in order to indicate the point that the discharging mode changes to charging mode. Whenever this interrupt is enabled, the sorting algorithm must change the sorting pattern according to the new mode.

The modified sorting algorithm proposed here should be used for zero-current condition only, since when a current circulates in the phase leg the classical sorting can be adopted. In this paper, the threshold for the activation of the proposed controller is set to 0.03 pu.

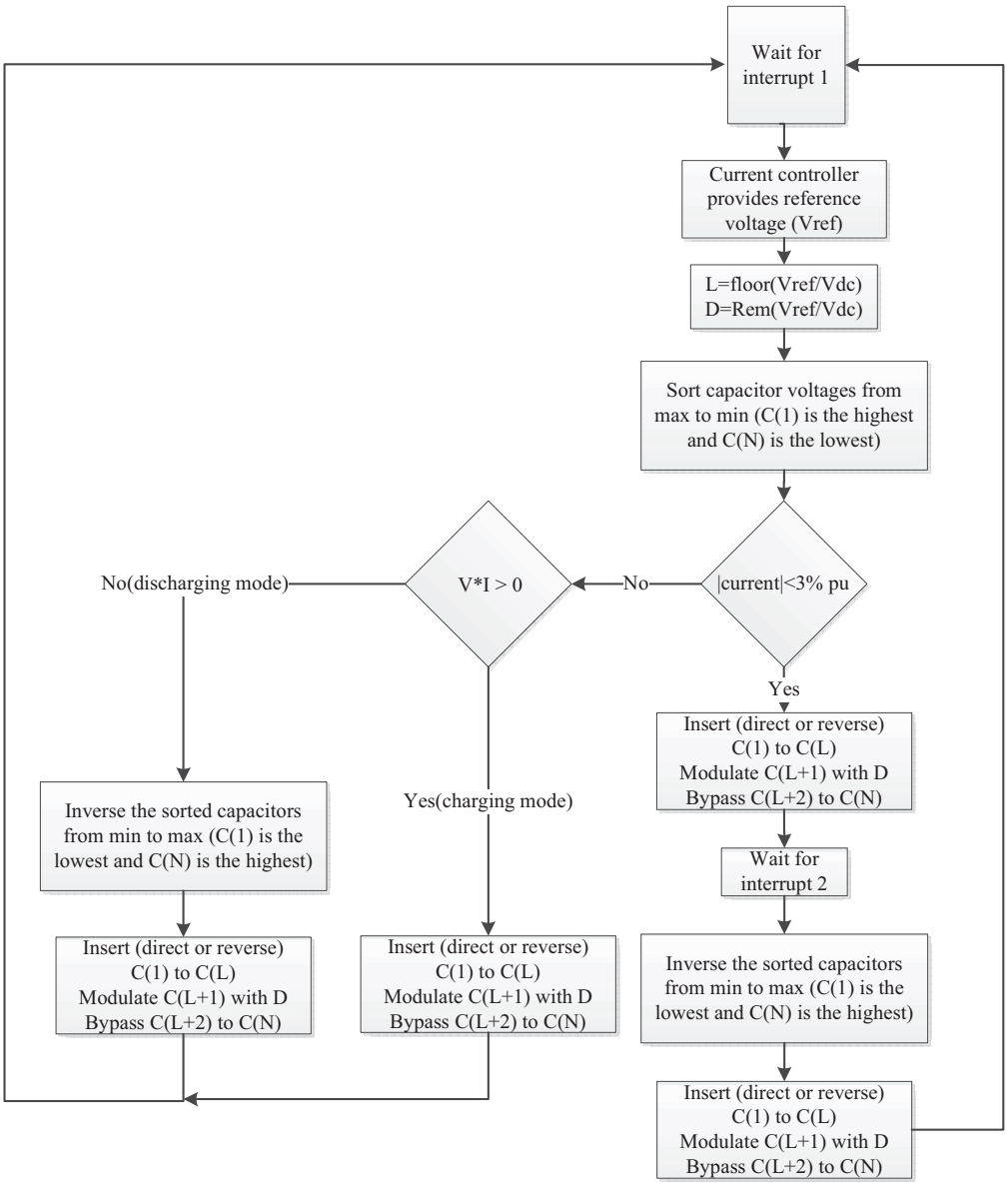

Figure 5. flowchart of the proposed controller.

The flowchart of the proposed controller is shown in Fig. 5. In the beginning of each main interrupt, first the reference voltage is determined. Then the number of cells that must be inserted (direct or reverse) and fractional part of the reference voltage are determined. Whenever the RMS value of the current is in the range of zero to the predefined threshold (0.03 pu in this case), the proposed method is activated. According to the sign of the current ripple discussed in the previous section, every control cycle starts with the discharging mode regardless of the polarity of the voltage. Thus the first sorting pattern is determined based on the discharging mode. Afterward, the controller waits to receive the second interrupt. From the middle of the control cycle to the end the phase leg is in the charging mode thus second sorting pattern is determined based on the charging mode. Finally the controller waits for the main interrupt to continue the same process.

It is worth mentioning that charging and discharging pattern explained here (discharging first charging second) is based on the assumption that there is no delay in the digital controller. Considering one-sample delay in the digital controller, the charging and discharging pattern must be reversed (charging first discharging second). The reason is that due to one-sample delay, in each interrupt the controller decides about the next control period.

SIMULATION RESULTS

The proposed DC-link voltage control method is applied to the same simulation case study presented in the previous section. Figure 6 shows the simulation results when using the proposed method. Figure 6 (top) shows the 3-phase line currents and Fig. 6 (bottom) shows the capacitor voltages in phase *a*,*b* and *c*. All figures are showing the measured data in per unit. At t=0.9 S, the reactive current is changed from 0.35 pu to zero. Figure 6 shows that the proposed algorithm is able to provide proper individual cell balancing at zero current mode.

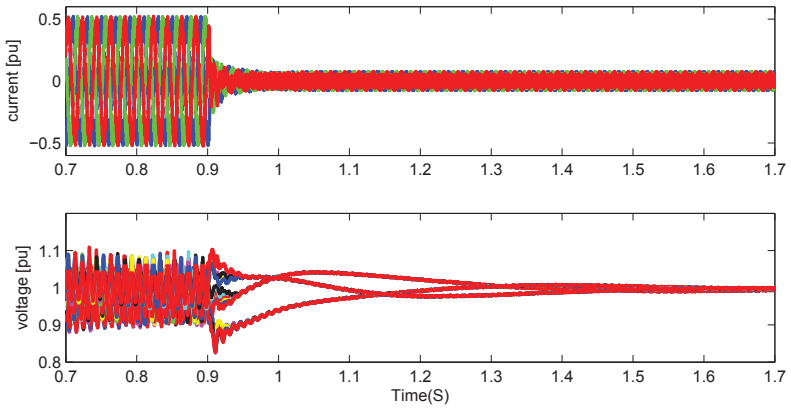

Figure 6. Capacitor voltages and line current by using the proposed method. (top) Three-phase line currents, (bottom) all capacitor voltages in each phase.

Figure 7 shows a zoom of two cells output voltage, line current between two sampling points together with main and secondary interrupts. Figure 7 shows that unlike the conventional sorting algorithm (Fig. 4), the output voltage is not generated only by one cell. According to the proposed method, the PWM pulse is first generated by a cell that is chosen based on discharging mode and after half a period (at the secondary interrupt) the PWM pulse is completed by a cell which is chosen based on the charging mode.

Figure 8 shows simulation results of line current and cells voltages when the reference current varies from 0.03 pu inductive to 0.03 pu capacitive. From t=0.7s to t=0.8s reactive power is set to zero. From t=0.8s to t=1s 0.03 pu inductive and from t=1s to t=1.2s 0.03 pu capacitive reactive power are set. The current ripple amplitude from Fig. 3 (top) is 0.07 pu (i.e., above the threshold level). As it is shown in Fig. 8 (bottom), the proposed method is able to provide proper individual cell balancing.

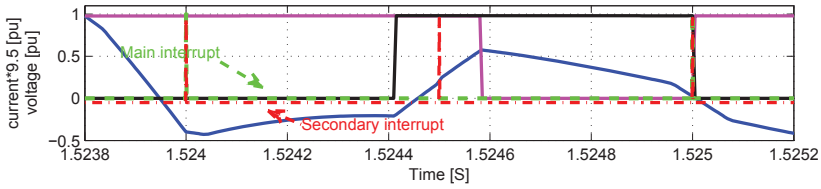

Figure 7. Two cells output voltages and line current (Current is multiplied by 9.5) together with main and secondary interrupts.

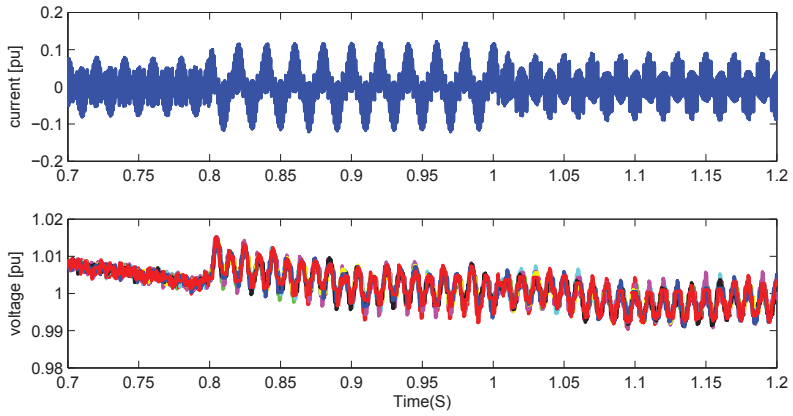

Figure 8. Capacitor voltages and line current with the proposed method in the current range of -0.03 pu to +0.03 pu. (top) phase *a* current, (bottom) capacitor voltages.

To evaluate the robustness of the proposed method, 0.05 pu white noise is added to the current and voltage measurements. Due to inevitable delay in discrete controller, one-sample delay is considered in the controller. In order to provide a more realistic model, deadtime of 5 μS for the switches and 2 V forward voltage drop over valves are considered. The amount of noise, deadtime and capacitor size variations chosen here are exaggerated quantities in order to verify the robustness of the proposed method under extreme cases. Figure. 9 shows the obtained simulation results.

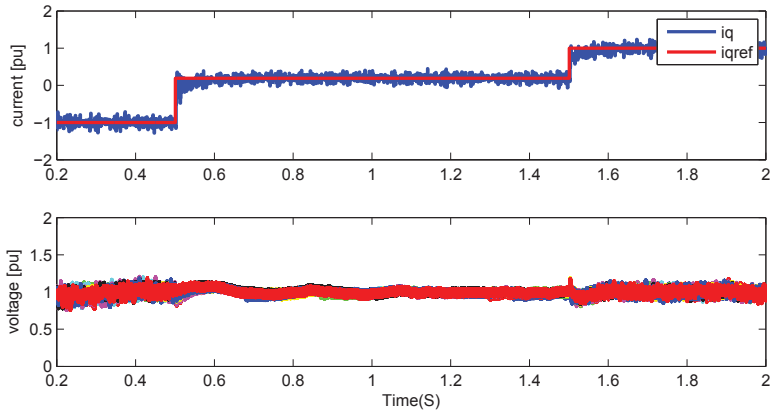

Figure 9. Simulation results by considering noise, delay, deadtime and valves voltage drop. (top) Reactive component of current and its reference, (bottom) Capacitor voltages in phase *a*.

Figure. 9 (top) shows the reactive component of the current and its reference. The reference reactive current is set to 1 pu in the beginning and changes to zero and -1 pu at $T = 0.5S$ and $T = 1.5S$. Figure. 9 (bottom) shows the successful operation of the controller in balancing the capacitor voltages.

It should be noted that the extra interrupt only changes the sorting pattern and switching states of the converter between two sampling points. The proposed method does not affect the main current controller or reference voltages. Therefore this method does not imply any transient when the converter moves into or back from standby mode.

Effect of grid voltage harmonic on proposed solutions

In order to evaluate the proposed method in presence of grid voltage harmonics, a 5th harmonic of 0.016 pu amplitude and a 7th harmonic of 0.011 pu amplitude are added to the grid voltage. Figure 10 shows the grid voltages, reactive component of the current and capacitor voltages. The same conditions (such as noise and delay) described in the previous section are kept for this set of simulations. Observe that again the proposed method allows successful capacitor voltage balancing during zero average-current exchanging mode.

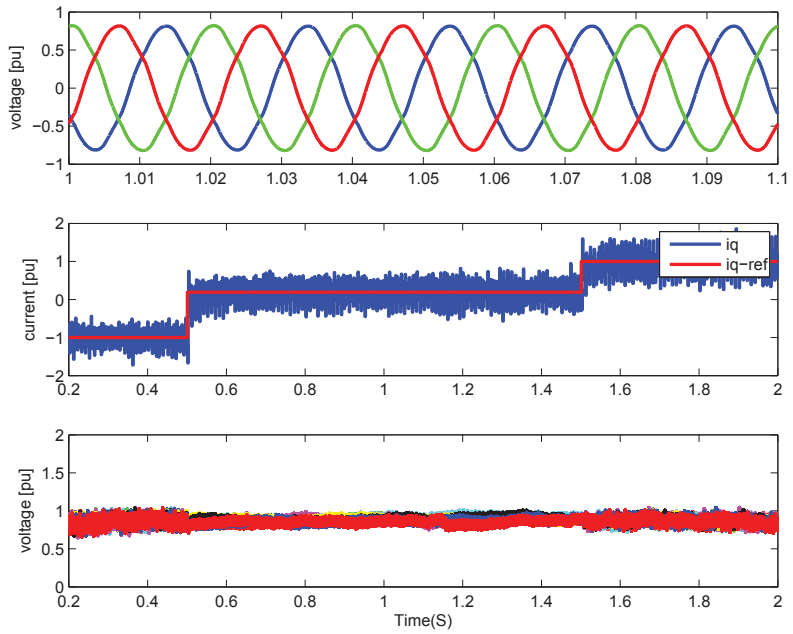

Figure 10. Effect of grid voltage harmonics on the proposed method. (top) grid voltages, (middle) reactive component of the current and its reference, (bottom) capacitor voltages in phase *a*.

CONCLUSION

This paper proposes a solution for individual cell voltage balancing at zero current operating mode. The method modifies the conventional sorting algorithm according to the sign of the current ripple at zero current mode. The sign of the current ripple shows that the instantaneous current sign information in the beginning of each control cycle is not enough for a proper balancing action. Therefore the conventional sorting algorithm is unable to provide a perfect balancing at zero current mode. The modified method proposes the use of an additional interrupt between two sampling points in order to modify the sorting pattern. Simulation results show perfect balancing at zero current mode by using the proposed method while the conventional sorting algorithm is unable to provide the balancing at this point. The proposed method shows good balancing ability even when adding measurement noise and other practical limitations.

Since this method uses the current ripple, the operating range of the proposed method is limited by current ripple amplitudes. The proposed method is valid as long as the RMS value of the current is less than the current ripple

amplitude and must be avoided beyond this region. Grid voltage harmonics can affect this method if the current that cause by harmonics exceed the amplitude of ripples.

This method does not affect the main current controller or reference voltages and therefore it does not imply any transient when the converter moves into or back from standby mode. The method only changes the charging logic in the middle of two sampling points, which leads to an extra switching. The increase in the switching frequency leads to higher, but since the converter is operating at zero current mode this amount of loss is negligible.

Although the proposed method is validated and presented for star configuration, it can also be applied for delta structure. But for the delta configuration, circulating current provides an extra degree of freedom which can be used for voltage balancing purposes. The circulating current solution is an easier approach for capacitor voltage balancing, however star configuration does not have the benefit of the circulating current.

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