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Effect of ferroelectric substrate on carrier mobility in graphene field-effect transistors

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Effect of $LiNbO_3$ ferroelectric substrate on the carrier mobility in top gated graphene field-effect transistors (G-FETs) is demonstrated. It is shown that, at the same residual concentration of the charge carriers, the mobility in the G-FETs on the $LiNbO_3$ substrate is higher than that on the SiO_2/Si substrate. The effect is associated with reduction of Coulomb scattering via screening the charged impurity field by the field induced in the ferroelectric substrate, but significant only for mobilities below 1000 cm^2/V s. Raman spectra analysis and correlations established between mobility and microwave loss tangent of the Al_2O_3 gate dielectric indicate that the charged impurities are located predominantly at the gate dielectric and/or at the gate dielectric/graphene interface and are likely associated with oxygen vacancies.
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The property of very high carrier mobility and speed in graphene enables the possibility of much faster electronics than with traditional semiconductors. The room-temperature intrinsic mobility in single layer graphene is above 100 000 cm^2/V s, which is larger than in the highest mobility III-V compounds.[1–3] According to the calculations, the graphene based high frequency electronics might reach the still uncovered terahertz range offering many exciting applications.

However, realization of graphene in prospective high frequency electronics is hindered by strong extrinsic limitation of mobility caused by vicinity of dielectrics. The highest reported room-temperature mobility values in graphene field-effect transistors (G-FETs), utilizing different dielectric materials, including Al_2O_3, Y_2O_3, HfO_2, BN, SiC, SiO_2, and polymers, are below 24 000 cm^2/V s.[4–9] A reason is the Coulomb scattering caused by charged impurities.[1,10] In a simple model, the charged impurities are located either inside the substrate or created near the graphene-substrate interface during the processing and induce a spatially inhomogeneous screened Coulomb potential.[10] Nature and origin of the charged impurities are not fully understood and may vary depending on certain processing of samples. For instance, the charged impurities can be associated with water molecules trapped at the graphene-substrate interface or with the oxygen vacancies in the gate dielectric.[11–13] Non-controllable concentration and spatial inhomogeneity of the charged impurities result in that the mobility in the G-FETs is typically well below the highest reported values (Refs. 9 and 14–18), the residual carrier concentration is high, it is non-reproducible, and spatially distributed over the wafer surface.

Theoretical considerations show that the mobility governed by Coulomb scattering can be increased by screening the charged impurity field by a corresponding field induced in an adjacent dielectric with a relatively high dielectric constant.[10] The screening effect has been demonstrated experimentally by examples of the G-FETs with high k HfO_2 and ferroelectric PZT as the top and back gate, respectively.[13,19] The G-FET on PZT reveals carrier mobility up to 70 000 cm^2/V s in a few-layer graphene at room temperature.[19] In both cases, the charged impurities are assumed to be located inside or at the interface of the high dielectric constant material, such as oxygen vacancies in HfO_2, or adsorbates on the PZT surface.[13,19] So far, no data has been published on the screening effect of a high k substrate in the top gated G-FETs. The theory is also developed for the simple model of a graphene layer on top of a substrate.[10] Therefore, it is not clear how effectively the substrate polarization can screen the charged impurities located at the top gate dielectric or at the top interface. The use of the substrate polarization is motivated by the possibility of development of the bilayer G-FETs with ferroelectrically induced bandgap.[20] In this paper, we report the effect of the $LiNbO_3$ ferroelectric substrate polarization on the mobility in the top-gated single layer G-FETs by comparative analysis with that based on the SiO_2/Si substrate.

In this work, graphene is grown on the copper foil in a cold-wall low-pressure CVD system and transferred onto Si, with 90 nm thick SiO_2, and $LiNbO_3$ substrates. Bulk resistivity of the Si substrate is 10 kΩ cm. The $LiNbO_3$ substrate is a z-cut single crystal with spontaneous polarization pointing to the surface and the in-plane and out-of-plane dielectric constants of 85 and 25, respectively. Details and sequences of the fabrication steps and layout of the G-FETs are similar to those given in Ref. 21, with an exception that the 15 nm thick Al_2O_3 gate dielectric layer is grown by the atomic layer deposition in thermal mode at 300 °C on top of the seed layer. The seed layer is formed by two steps of thermal oxidation of 1 nm thick Al films deposited by e-beam evaporation.

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The total thickness of the Al_2O_3 layer is 17.5 nm. The G-FETs with different gate lengths (L_g) of 0.3 μm, 0.6 μm, and 1.0 μm and same access length of 0.1 μm are fabricated. Fig. 1 shows a typical SEM image plan view of a fabricated G-FET. The graphene layers and the G-FETs are characterized at room temperature. Before fabrication of transistor structures, the Raman spectra are measured using a Horiba scientific spectrometer with a 638 nm laser. Drain resistance is calculated at the drain voltage equal to −0.1 V. The complex input impedance of the G-FETs is calculated as $Z = Z_0(1 + S_{11})/(1 - S_{11}) = R + jX$ with S_{11} parameters obtained from one port reflection measurements using an Agilent N5230A vector network analyzer at 0 V dc bias. The input loss tangent of the G-FETs is calculated as $\tan\delta = -R/X$.

Fig. 2 shows the Raman spectra of the *G* and 2*D* bands. The 2*D* to *G* peak intensity ratio is a strong function of the charge carrier concentration and does not depend on the strain.[22–24] As it can be seen from Fig. 2, the intensity ratios are, approximately 1.7 for both substrates. For the single layer graphene, produced by microcleavage, which can be considered unstrained, such an intensity ratio corresponds to the position of the *G* peak at, approximately, 1586 cm^{-1}.[22] The upshifts of the peaks observed in our experiments can be attributed to the compressive strain produced by our CVD growth and transfer processes.[24,25] Unlike the 2*D* peak, which always upshifts with the excitation energy due to double resonance, the *G* peak position does not depend on the wavelength.[22] Therefore, correlations between the 2*D* to *G* peak intensity ratio, position of the *G* peak, and the charge carrier concentration established for the 514 nm laser (Ref. 26) are also valid for our case of the 638 nm laser. In the unstrained graphene, the *G* peak position at 1586 cm^{-1} corresponds to the charge carrier concentration of 2×10^{12} cm^{-2}.[26] Therefore, we assume that the residual concentration of the charge carriers in our graphene layers on both substrates, before fabrication of the G-FET structures, is below 2×10^{12} cm^{-2}. The upshift of the $LiNbO_3$ *G* peak (Fig. 2) can be attributed to a slightly larger concentration of the charge carriers.[26]

Fig. 3 shows the drain resistance of the G-FETs with $L_g = 0.6$ μm versus gate voltage. It can be seen that the drain resistance of the G-FETs on the $LiNbO_3$ substrate reveals typical dependence with a maxima corresponding to the Dirac point. Therefore, we assume that the Coulomb scattering

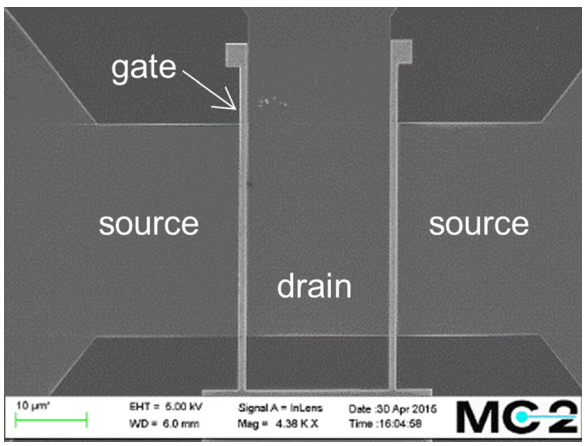

FIG. 1. SEM image plan view of a G-FET.

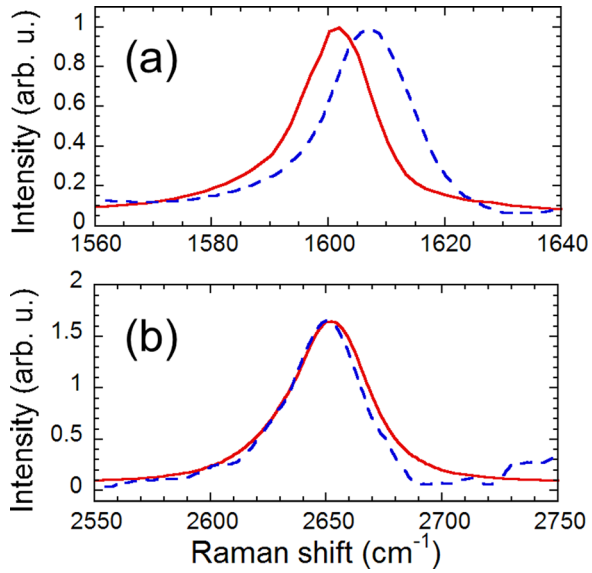

FIG. 2. Raman spectra of the *G* bands (a) and 2*D* bands (b) of graphene layers on the SiO_2/Si (solid lines) and $LiNbO_3$ (dashed lines) substrates.

dominates and the mobility does not depend on the concentration of the charge carriers.[10] This allows for extraction of the mobility from the drain resistance (R) dependence by fitting the semi-empirical model[27]

$$R = R_c + \frac{L}{W}\frac{1}{\mu e}\frac{1}{\sqrt{n_0^2 + \left((V - V_{Dir})\frac{C}{e}\right)^2}},$$

where R_c is the contact resistance, μ is the mobility of the charge carriers, e is the elementary charge, n_o is the residual carrier concentration, V is the gate voltage, V_{Dir} is the Dirac voltage, and C is the gate capacitance per unit area. The R_c consists mainly of the metal/graphene contact and access resistances. It can be shown that the graphene quantum capacitance can be ignored. The C is calculated assuming the dielectric constant of Al_2O_3 equal 7.5.[28] As it can be seen from Fig. 3, at the same gate voltage modulus the drain resistance above the Dirac point is larger for both substrates. This can be explained by lower electron mobility and higher contact resistance due to formation of the p-n barrier at the

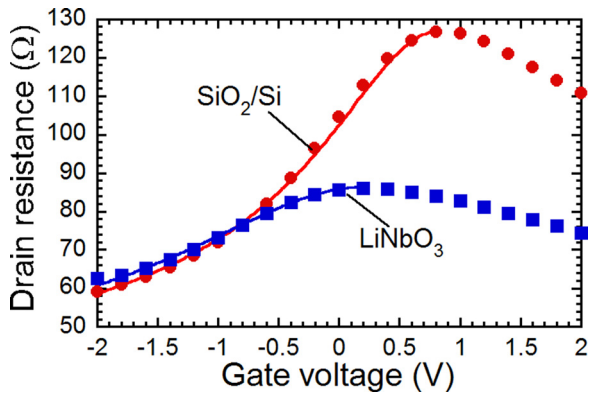

FIG. 3. Drain resistance of the G-FETs with $L_g = 0.6$ μm on the SiO_2/Si (circles) and $LiNbO_3$ (squares) substrates versus gate voltage along with modeling results (lines).

metal/graphene contact.[29,30] The solid lines in Fig. 3 represent fitting the model in the hole branches. Good agreement with the measured data confirms the assumption of the Coulomb scattering and hence constant mobility. The model parameters extracted are $R_c = 28\ \Omega$ and $27\ \Omega$, $\mu = 300\,\mathrm{cm^2/V\,s}$ and $300\,\mathrm{cm^2/V\,s}$, $n_0 = 2.1 \times 10^{12}\,\mathrm{cm^{-2}}$ and $3.5 \times 10^{12}\,\mathrm{cm^{-2}}$ for the SiO_2/Si and $LiNbO_3$ substrates, respectively.

According to the self-consistent theory, the mobility limited by the Coulomb scattering depends only on the charged impurity concentration and the dielectric constant of the substrate.[10] The charged impurity concentration directly defines the residual concentration of the charge carriers.[10] Therefore, there should be correlation between the mobility and the residual concentration of the charge carriers. Fig. 4 shows the hole mobility in the G-FETs with different gate lengths versus residual concentration of charge carriers found by fitting the drain resistance model to the measured data. It can be seen that there are clear correlations. The mobility increases with lower residual concentration of the charge carriers. Obviously, this is due to lower concentration of the charged impurities and, correspondingly, reduced scattering. At the same residual concentration of the charge carriers, the charged impurity concentration for the $LiNbO_3$ substrate should be higher, due to the lower fine-structure constant.[10] However, as can be seen from Fig. 4, the mobility is also higher. This indicates the effect of the ferroelectric substrate on the mobility caused by more effective screening of the local charged impurity field by the corresponding field induced in $LiNbO_3$ because of higher dielectric constant. However, extrapolation of the dependence to the lower residual concentration of the charge carriers reveals that the effect can be significant only at relatively high concentration of the charged impurities, which corresponds to mobilities below $1000\,\mathrm{cm^2/V\,s}$. In general, the residual concentration of the charge carriers on $LiNbO_3$ is larger (Fig. 4), which can be explained partly by larger concentration of the charged impurities in the $LiNbO_3$ substrate or at the graphene/substrate interface. This is in agreement with the upshift of the *G* peak in the Raman spectra (see Fig. 2(a)). In all cases, the residual concentration of the charge carriers is larger than that found from the Raman spectra analysis, less than $2 \times 10^{12}\,\mathrm{cm^{-2}}$. Therefore, one can conclude that the charged impurities are located predominantly at the gate dielectric or at the gate dielectric/graphene interface. To support this conclusion, we investigated the correlations between the residual concentration of the charge carriers and the microwave dielectric loss in the gate dielectric.

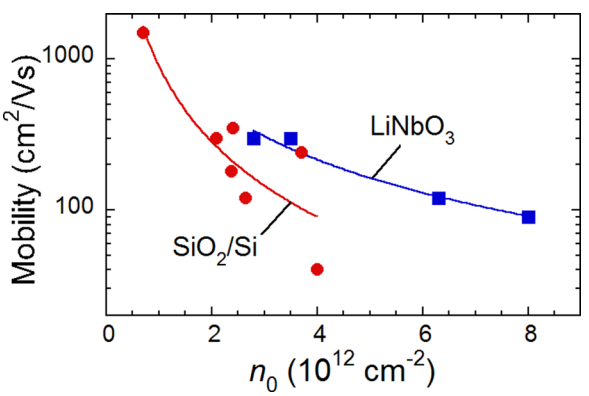

FIG. 4. Hole mobility of the G-FETs on the SiO_2/Si (circles) and $LiNbO_3$ (squares) substrates versus residual concentration of charge carriers (n_0). Lines are fitting curves. The highest mobility data are taken from Ref. 31 to indicate the trend.

Fig. 5 shows the measured input loss tangents of the G-FETs versus frequency. It can be seen that at sufficiently high frequencies the dependences are linear, indicating that loss associated with series resistance R_s dominates and $\tan\delta \approx R_s\omega C_g$. The R_s is associated mainly with the access and contact areas of the G-FETs. The R_s can be found as the real part of the input impedance at the high frequency limit and corresponding loss can be de-embedded from the total input losses.[32] The de-embedded loss tangents $\tan\delta_{de}$ are shown in Fig. 5. It can be seen that for the $LiNbO_3$ substrate the $\tan\delta_{de}$ is rather frequency independent. In accordance with the universal relaxation (Curie-von Schweidler) law, observed in a wide range of materials, the real ε and imaginary ε_{im} parts of the dielectric constant have the same frequency dependence (ω^{n-1}, where $0 < n < 1$) and, therefore, the loss tangent is frequency independent $\tan\delta = \varepsilon_{im}/\varepsilon$.[33,34] Hence, for the $LiNbO_3$ substrate the $\tan\delta_{de}$ represents pure gate dielectric loss. The low frequency tails of the loss tangents of the G-FETs on the SiO_2/Si substrate (Fig. 5) can be explained by an additional dielectric loss associated with the Si surface conductivity.[35] The dielectric dispersion in the Si is characterized by the dielectric (Maxwell) relaxation frequency (Ref. 36) $\omega_{dr} = 1/(\varepsilon_{Si}\varepsilon_0\rho_{Si})$, where $\varepsilon_{Si} = 11.65$ (Ref. 37) and ρ_{Si} are the dielectric constant and surface resistivity, respectively. According to the Drude model in the frequency range $\omega \gg \omega_{dr}$, the loss tangent is $\tan\delta_{Si} = \omega_{dr}/\omega$. Fig. 5 shows the $\tan\delta_{Si}$ fitted into the low frequency tail of the $\tan\delta_{de}$ at the $\rho_{Si} = 8.1\,\Omega\,\mathrm{cm}$. Subtracting the $\tan\delta_{Si}$ from the $\tan\delta_{de}$ allows for evaluation of the pure gate dielectric loss of the G-FETs on the SiO_2/Si substrates.

Fig. 6 shows the loss tangents of the gate dielectric of the G-FETs at 20 GHz versus residual concentration of the charge carriers. It can be seen that there are clear correlations. The gate dielectric loss tangent increases with the residual concentration of the charge carriers. This draws the following conclusions. First, the charged impurities inducing the residual charge carriers and which are responsible for the Coulomb scattering in graphene simultaneously cause an extrinsic microwave loss in the gate dielectric. Therefore, the

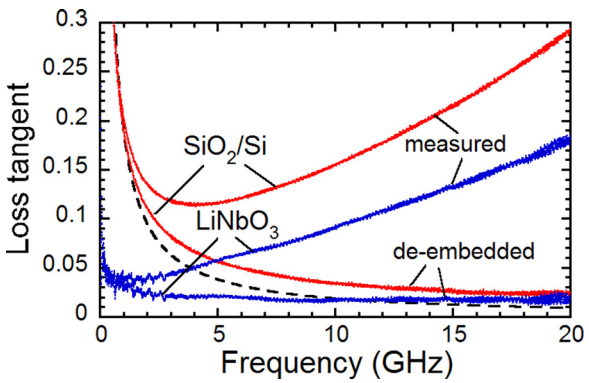

FIG. 5. Measured and de-embedded loss tangents of the G-FETs with $L_g = 0.6\,\mu\mathrm{m}$ on the SiO_2/Si and $LiNbO_3$ substrates versus frequency. The loss tangent in the Si substrate (dashed line) is also shown.

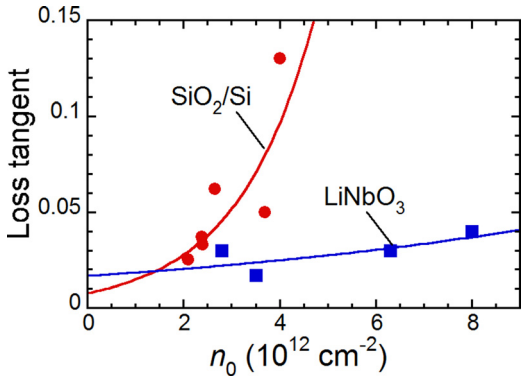

FIG. 6. Loss tangent of the gate dielectric of the G-FETs on SiO_2/Si (circles) and $LiNbO_3$ (squares) substrates at 20 GHz versus residual concentration of charge carriers (n_0). Lines are fitting curves.

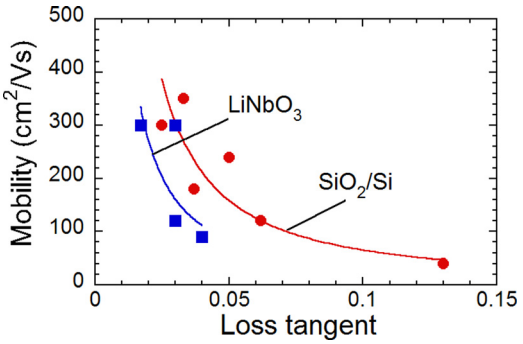

FIG. 7. Hole mobility of the G-FETs on the SiO_2/Si (circles) and $LiNbO_3$ (squares) substrates versus loss tangent of the gate dielectric. Lines are fitting curves.

charged impurities are located predominantly at the gate dielectric or at the top interface. This is in agreement with the analysis of the Raman spectra and the drain resistance above. The microwave loss mechanism can be similar to that in the displacive paraelectrics and associated with electrostriction. The electrostriction about the charged defect excites acoustic vibrations in the medium, which tends to dissipate the energy of the microwave field.[34] The charged defects in the displacive paraelectrics are associated mainly with the oxygen vacancies (Ref. 33), which are also the main intrinsic defects in Al_2O_3.[38] Therefore, we assume that the oxygen vacancies in Al_2O_3 are the source of the extrinsic microwave loss in the gate dielectric and simultaneously responsible for the Coulomb scattering of the charge carriers. It can be seen from Fig. 6 that the dependence for the $LiNbO_3$ substrate is much weaker than that for the SiO_2/Si. This can be explained assuming more effective screening of the local charged impurity field by the corresponding field induced in $LiNbO_3$ because of much higher dielectric constant. It is the same screening mechanism which reduces the Coulomb scattering and results in the higher mobility at the same residual concentration of the charge carriers, see Fig. 4. Therefore, it confirms the effect of the ferroelectric substrate on the mobility. It can be seen that at the residual concentration of the charge carriers below $2 \times 10^{12}\,cm^{-2}$, the screening effect on the loss tangent is negligible, which is in agreement with the effect on the mobility, see Fig. 4. This again can be explained by the low concentration of the charged impurities which can be screened.

In the case of dominating Coulomb scattering and the charged impurities located in the gate dielectric, the loss tangent can be used as a parameter to characterize the mobility. Fig. 7 shows the hole mobility of the G-FETs on the SiO_2/Si and $LiNbO_3$ substrates versus loss tangent. It can be seen that the mobility increases sharply when the loss tangent decreases due to reduction of the charged impurity concentration and corresponding Coulomb scattering. At the same loss tangent, the mobility for the SiO_2/Si substrate is approximately twice as large. This can be explained by the stronger effect of screening on the loss tangent than that on the Coulomb scattering. Obviously, the concentration of the charged impurities in the gate dielectric, which are most likely oxygen vacancies in Al_2O_3, can be decreased by the technology optimization and the loss tangent can be as low as that of the bulk counterparts, down to 10^{-5}.[39] It can be seen from Fig. 7 that at this level of the loss tangent the mobility can be greatly increased, well above $1000\,cm^2/V\,s$.[2]

In conclusion, we demonstrated the screening effect of the $LiNbO_3$ ferroelectric substrate polarization on the charged impurity scattering field allowing for increase in the carrier mobility of the top gated G-FETs. However, the effect is only significant for the mobilities below $1000\,cm^2/V\,s$. Raman spectra analysis and correlations established between mobility and microwave loss tangent of the Al_2O_3 gate dielectric indicate that the charged impurities are located predominantly at the gate dielectric and/or at the top interface, and can be associated with oxygen vacancies. The gate dielectric technology optimization may allow for significant increase in the carrier mobility up to the limitations by other scattering mechanisms. $LiNbO_3$ can be used as a substrate for development of the bilayer G-FETs with ferroelectrically induced bandgap.

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