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Impact of Forward Error Correction on Energy Consumption of VCSEL-based Transmitters

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Abstract We present an analysis of the effect of FEC on energy consumption of VCSEL based transmitters for short-range optical links. We show that a low-complexity FEC can reduce the overall energy consumption of the transmitter.

Introduction

Energy consumption of short-range optical links is a matter of increasing importance for both operational cost and environmental reasons. Such links are typically built using directly modulated 850-nm vertical cavity surface emitting lasers (VCSELs). The main advantages of VCSELs are large modulation bandwidths, reaching 30 GHz¹, and energy consumption, demonstrated to be as low as 108 fJ/bit at 40 Gbps² and 56 fJ/bit at 25 Gbps³.

Forward error correction (FEC) is a subject of interest for the next generation of datacom standards and has been introduced already in the Infiniband standard⁴. FEC reduces the required optical signal power at the receiver, and consequently at the transmitter, at the expense of energy consumption to perform encoding and decoding. This reduction translates to reduced energy consumption in the VCSEL and the driver and does not affect energy consumption of the analog components of the receiver.

In this paper the trade-off between power consumption of simple FEC circuits and VCSEL based transmitters is studied.

VCSEL and driver power consumption

The VCSEL energy consumption is quantified using the heat-to-data ratio³ (HDR). The thermal power (heat) is calculated as the total electrical input power minus the optical output power³. The energy consumption can also be quantified using the total input electrical energy-to-data ratio³ (EDR).

At a fixed extinction ratio (ER) the VCSEL EDR is dependent on the optical modulation amplitude (OMA) at the VCSEL output. An example of experimentally measured EDR as a function of OMA

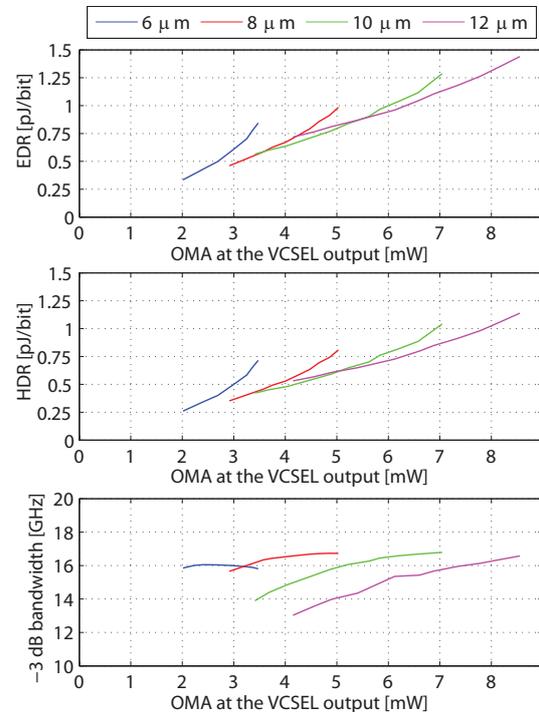


Fig. 1: Experimental EDR, HDR and modulation bandwidth at $ER = 6$ dB for VCSELs with oxide aperture diameters in the range $6 \mu\text{m}$ to $12 \mu\text{m}$.

at an $ER=6$ dB is shown in Fig. 1. The EDR was measured for four VCSELs with 6, 8, 10 and $12 \mu\text{m}$ oxide apertures. The details of the VCSELs design are described in⁵. Smaller apertures increase the modulation bandwidth at low bias currents and low OMA, but increase the differential resistance³. The modulation bandwidth plotted against the OMA is also included in Fig. 1.

We see from Fig. 1 that the VCSEL EDR can be approximated as $EDR \approx \eta_{bit} OMA$, where η_{bit} is a proportionality constant between OMA and EDR. For the VCSELs used in the measurements in Fig. 1 $\eta_{bit} = 0.15$ pJ/bit/mW. All VCSELs have

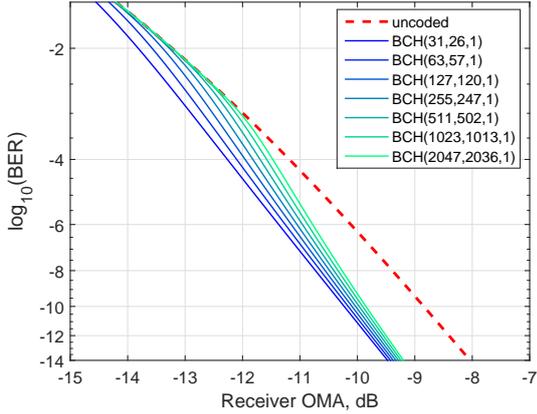


Fig. 2: Post-FEC BER as a function of the receiver OMA at 20 Gbps data rate (including the FEC overhead).

maximum bandwidth up to 17 GHz and can support data rates up to 20 Gbps. However, with decreasing OMA, a smaller aperture size VCSEL should be used to maintain the high data rate.

Another important energy consuming component in the transmitter is the VCSEL driver. In general, one may treat the driver as a current source driving the laser. In the following, we assume the same bias voltage drop and the same signal impedance for driver and load, implying equal power dissipation in each. Therefore, the transmitter (i.e. VCSEL and the driver) EDR can be approximated as $EDR \approx 2\eta_{bit}OMA$. Simple CMOS drivers are of interest because they have a good potential for low energy consumption⁶, reaching numbers as low as 1 pJ/bit for a complete link⁶. The driver energy consumption in⁶ was comparable to the VCSEL energy consumption and it was shown to be variable with the VCSEL bias current and OMA.

The energy consumption of the photodiode and the following amplifier is not considered here, but it is expected to be driven by the required amplitude at the output (e.g. at the input to a following decision circuit).

OMA requirements and FEC

With FEC the acceptable bit error rate (BER) at the receiver output is increased and therefore the receiver OMA can be reduced. The transmitted OMA is the receiver OMA increased by the link power budget and it is also reduced with FEC. The transmitter EDR is also proportionally lower, given the linear dependence of the EDR on the OMA. Simplicity of the FEC is important for low power consumption, and therefore BCH codes with error correction capability t of 1 bit per block are considered, with code length n in the range between 31 and 2047 bits. The theoretical post-

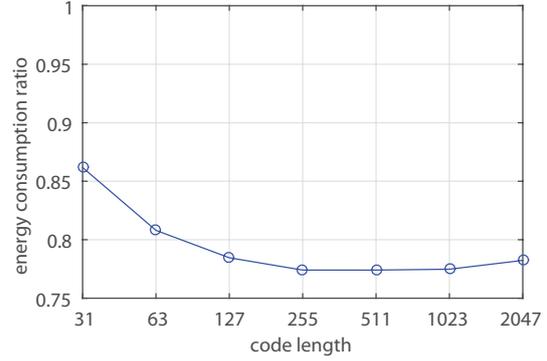


Fig. 3: EDR of a transmitter in a link with single error correcting BCH code relative to EDR of a transmitter in a link without FEC.

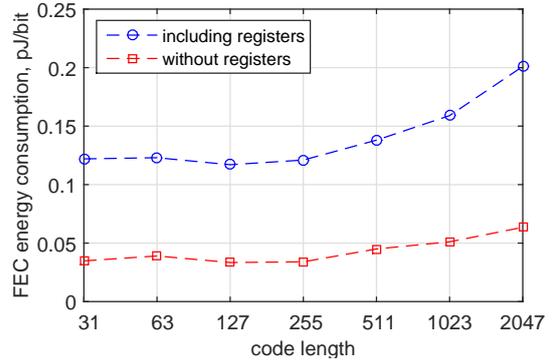


Fig. 4: Energy consumption per bit in the FEC encoder and decoder, including and excluding the registers.

FEC BER as a function of the OMA at the receiver for 20 Gbps is shown in Fig. 2. The codes are labeled in the conventional format (n, k, t) , where k is the number of information bits. The BER for a case without FEC is also included. The following assumptions were made: laser relative intensity noise was -140 dB/Hz, photodiode responsivity of 0.4 A/W, receiver noise figure of 5 dB, room temperature and a 50 Ohm resistance.

For a target post-FEC BER of 10^{-12} the BCH codes provide approximately 1 dB improved sensitivity, as shown in Fig. 2. The FEC introduces an overhead, which reduces the effective data rate. The transmitter EDR will be proportional to the required receiver OMA and inversely proportional to the code rate k/n . The ratio of the EDR of a transmitter with FEC to the EDR of a transmitter without FEC, as a function of n , is shown in Fig. 3. For n equal to 255, 511 and 1023 the FEC gives a 22% saving in transmitter EDR. There is an n minimizing the EDR, because at fixed t shorter codes have higher overhead and longer codes have lower coding gain. The increased overhead reduces the effective data rate, increasing the EDR.

The FEC encoder and decoder for the BCH codes which achieves 20 Gbps throughput, was

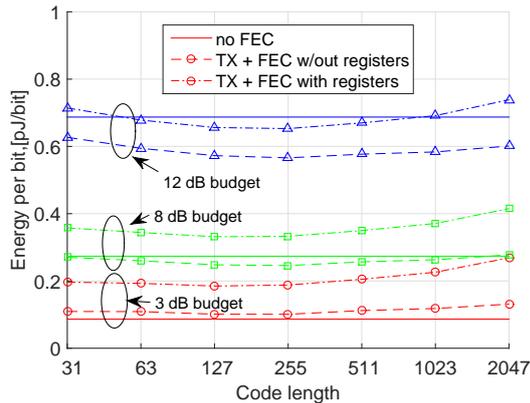


Fig. 5: Overall transmitter and FEC circuits energy consumption for link budgets of 3, 8 and 12 dB.

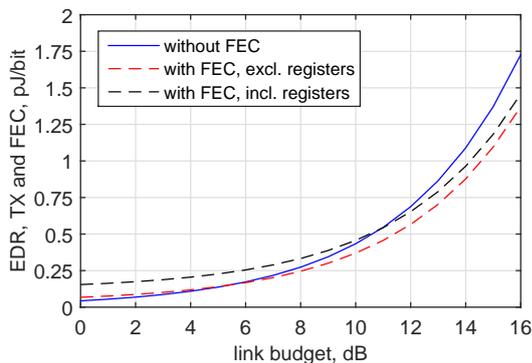


Fig. 6: Transmitter and FEC energy consumption as a function of the link budget, with (255,247,1) BCH code.

synthesized using Cadence RTL Compiler and a commercially available 65 nm general-purpose standard- V_t library. The used library was characterized at 1.1 V, nominal corner, and 25°C. The FEC encoder uses a fully-parallel blockwise systematic encoding based on parity-check XOR-trees, thus eliminating energy consuming buffers. The decoder uses a fully-parallel syndrome table based decoding. XOR-trees are used to generate the syndrome which is mapped to an error. This is highly efficient for single error correcting codes, but the complexity increases rapidly with error correction capability. The energy consumption per bit of the FEC encoder and decoder is shown in Fig. 4, both including and excluding the registers. The energy consumption per bit of the FEC circuits increases with code length. The registers account for around 2/3 of the energy consumption of the FEC, but there is a possibility that the registers could be re-used e.g., for run-length coding. In this case only the encoder and decoder would add EDR overhead.

Whether the FEC increases or decreases the total EDR depends on the code length and the link budget. The overall energy consumption of the 20 Gbps transmitter and the FEC circuits, including and excluding registers, is shown in Fig. 5.

Three link budget values are considered: 3, 8 and 12 dB. The transmitter EDR for the case without FEC is also included as a reference. At small link budgets (e.g., the 3 dB case) the FEC circuits increase the EDR, but at larger link budgets the FEC yields a total decrease in the EDR. The lowest overall energy consumption for all cases with FEC is for (255,247,1) BCH code. The EDR with this code as a function of the link budget is shown in Fig. 6. At large link budgets, the EDR saving in the transmitter outweighs the energy consumption increase due to the FEC.

Conclusions

A single error correcting BCH code can reduce the energy consumption of a VCSEL based transmitter. At large link budgets this reduction outweighs the energy consumption of the FEC circuits and net energy consumption reduction is achieved. The FEC registers could also be shared with run-length coding, meaning that the energy overhead for the FEC is minimized. There is further potential for reduction of the energy consumption of the FEC circuits using more advanced technology nodes and with lower supply voltage. For more efficient FEC circuits the break-even point at which there would be a net reduction of the energy consumption would occur for smaller link budgets.

Acknowledgements

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