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High speed bus analysis

Field bus and real time communication in high levels of EMI

Master of Science Thesis in Embedded Electronic System Design

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Abstract

In this report, high speed bus communication alternatives in high levels of EMI are investigated. The intended target is a weld system consisting of several parts where one is a power source. Weld power sources are subject to safety regulations regarding electrical safety. Therefore electronic communication between different ground potential regions are subject to high isolation requirements.

Hardware, protocol and software application aspects are evaluated using theoretical investigations and practical evaluations. Communication links with hard and soft real time requirements are investigated, with a focus on low total system cost. Cheap Plastic Optical Fiber links and Fast Ethernet links were evaluated in a lab setup with regards to the electrical, link speed and real time requirements. Software protocol handling was optimized for the embedded target system.

Laboratory evaluations indicated that the use of copper Ethernet was possible with regards to EMI. The use of cheap Plastic Optical Fiber links also provide sufficient data rate, while at the same time providing high galvanic isolation and EMI immunity.

Acknowledgements

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List of Acronyms

BGA Ball Grid Array

BPSK Binary Phase Shift Keying

CAN Controller Area Network

CAN FD CAN Flexible Data-rate

CGA Column Grid Array

CM Common Mode

CPU Central Processing Unit

CRC Cyclic Redundancy Check

DM Differential Mode

DMA Direct Memory Access

ECU Electronic Control Unit

EMI ElectroMagnetic Interference

EMS ElectroMagnetic Susceptibility

FIFO First In, First Out

FPGA Field Programmable Gate Array

FSK Frequency Shift Keying

GCC GNU Compiler Collection

GPIO General Purpose Input/Output (I/O)

GPL GNU General Public License

HAL Hardware Abstraction Layer

I/O Input/Output

IGBT Insulated-Gate Bipolar Transistor

IP Intellectual Property

JTAG Joint Test Action Group

LVDS Low-Voltage Differential Signalling

MAC Medium Access Controller

MAG Metal Active Gas

MCU Microcontroller Unit

MIG Metal Inert Gas

MII Media Independent Interface

MISO Master Input/Slave Output

MMA Manual Metal Arc

MOSI Master Output/Slave Input

OFDM Orthogonal Frequency-Division Multiplexing

PCB Printed Circuit Board

PECL Positive Emitter-Coupled Logic

PHY Physical layer transceiver

PLL Phase Locked Loop

POF Plastic Optical Fiber

PSK Phase Shift Keying

QAM Quadrature Amplitude Modulation

QFP Quad Flat Package

RAM Random Access Memory

RMII Reduced Media Independent Interface

SMPS Switched Mode Power Supply

SOIC Small-Outline Integrated Circuit

SPI Serial Peripheral Interface

STP Shielded Twisted Pair

TDMA Time Division Multiple Access

UART Universal Asynchronous Receiver/Transmitter

UTP Unshielded Twisted Pair

Contents

1 Introduction

Digital communication is used in almost all electronic equipment, enabling large amounts of information to be transmitted over few wires. Communication links can be part of real-time regulation loops or used for messaging between components, among other purposes. Requirements for a communication link are set by system performance, such as throughput, latency, and regulation loop frequency. Other aspects, including tolerable error rates and system cost, must also be considered. This project will investigate electronic communication alternatives in weld equipment, an application characterized by very high levels of ElectroMagnetic Interference (EMI).

1.1 Background

ESAB is one of the world leaders in welding and cutting technology. Their product range contains industrial cutting machines, welding filler metals, manual and robotic welding machines among many other things [1].

A weld process is used to join two pieces of metal together by melting parts of the metal and adding a filler material. The metal joined by the weld is called work piece. Figure 1.1 shows the basic principle of Manual Metal Arc (MMA) welding. Energy for the weld is commonly supplied by an electrical current, either DC or AC, and the regulation of this current influences the quality of the weld. To supply the current, ESAB has a product line of regulated high current power sources, with currents in the range of 100 A to 1600 A [1]. Switching of such high currents creates a noisy environment in terms of EMI [2].

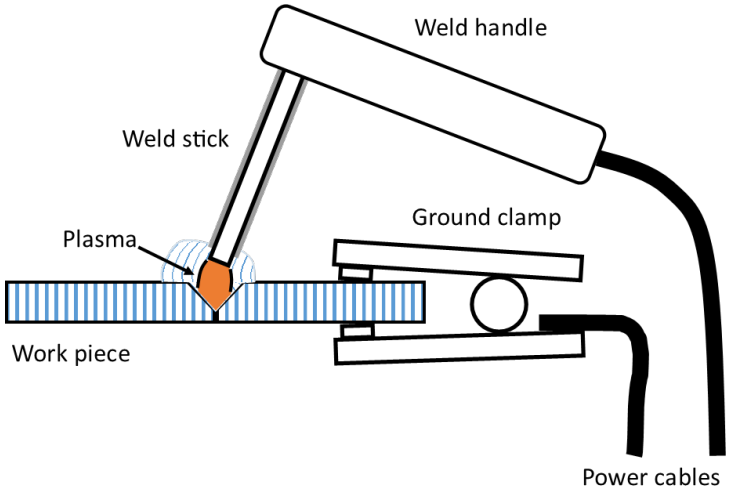


Figure 1.1: MMA welding principle showing weld region with work piece, weld stick, and ground clamp.

A complete weld system consists of several components such as power supply, wire feeder, and torch cooler, see Figure 1.2. These components all contain one or several Electronic Control Units (ECUs), among which communication links are connected. One communication link in the investigated system carries a

custom protocol for real-time weld process regulation. Handling of this protocol generates a relatively high load, approximately 35 %, in the main Microcontroller Unit (MCU). For future possibly higher regulation loop frequencies, this protocol handling is a limiting factor.

Other parts of the investigated system communicate on a generic bus. This bus is currently a Controller Area Network (CAN) bus configured at 400 kbit/s and can meet only lower real-time requirements. System communication is connected between external enclosures sometimes running in parallel with the weld cable, exposing the communication link to high levels of EMI. The communication speed of this bus is a limiting factor for larger transfers such as software upgrades.

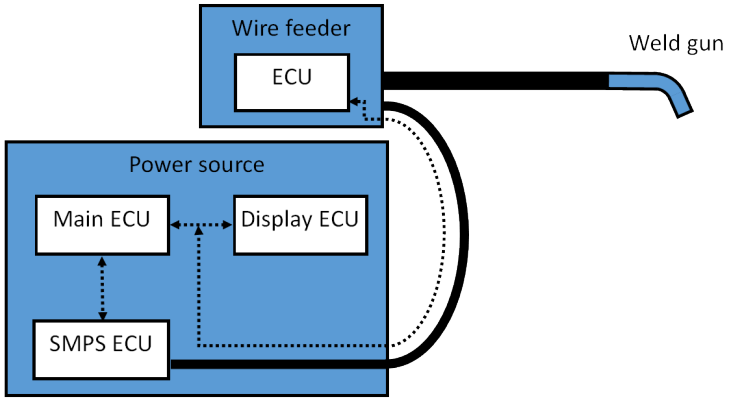


Figure 1.2: Principle overview of some of the communication and power links in a Metal Inert Gas (MIG) weld system, with communication links dashed.

1.2 Intended outcome

This project shall evaluate alternatives to the currently implemented communication solution, including the currently implemented solution itself. The goal is to provide an alternative that gives room for future upgrades, handles the real-time specifications including future refinements of the control loop, is reliable, handles the EMI aspects of the weld system environment, meets galvanic isolation requirements, and is cost efficient. For reliability reasons, the different communication channels, i.e. regulation loop interface and general bus communication, need to be separated in different fault containment regions such that a failure of a less critical bus does not propagate to a failure of a more critical process control bus or security critical communication bus.

In a large welding system, various components such as power supply, wire feeder and weld control handle are all connected by the weld current cable. To minimize external communication cabling, communication over the weld cable shall be investigated. Security aspects regarding emergency stop over bus communication shall also be considered. For remote control using i.e. handheld devices and for firmware upgrades to the system, wireless communications for interconnect with other systems shall be investigated.

1.3 Project boundaries

This project shall only focus on the communication between system components. Included in this restriction are physical communication links and the protocol used for the communication. Hardware board area and cost, as well as MCU and Field Programmable Gate Array (FPGA) utilization levels, are also included. Not included are other system design parameters like regulation loop design, power supply design, microcontroller system software architecture or other parts of the system.

Electronic communication can utilize protocol features such as self correcting codes for high reliability of transferred messages. Such measures, however, are not considered in this project.

1.4 Time plan

This project is to be carried out during a period of 20 weeks between 2015-01-19 and 2015-06-05, i.e. calendar weeks 4 through 23. The first part will be focused on characterization and instrumentation of the current implementation to find bottlenecks and gain reference measurements for the final evaluation. Following that, a theoretical study of currently available alternatives and current research to evaluate alternatives for a future system will be performed. If changes need to be implemented in the current hardware design, these must be introduced directly after the evaluation phase so that a prototype can be manufactured. The prototype is to be designed and manufactured by a third party. PCB design and assembly process will therefore not be a major part of this project. Software and HDL changes will be implemented in parallel with the hardware prototype.

Once everything is in place, the prototype will be evaluated in lab measurements for comparison with the previous implementation measurements.

2 Method

To evaluate alternatives for this project, data will be collected in three ways. First, the existing system will be evaluated in terms of hardware components and software implementation. Second, a literature study covering the research related to the project will be performed and possible hardware solutions will be evaluated. Third, one or two alternatives will be assessed in a lab setup evaluating the performance in an environment similar to the intended field usage of the system.

Software evaluation is to be performed on prototype and development boards with the targeted MCU and FPGA. Instrumentation of the software will be performed either with the integrated debug interface in the MCU, by measuring the physical signals on the board, or a combination thereof.

Lab measurements on the proposed prototype systems will be performed at ESAB's lab facilities. These tests will evaluate the EMI aspects of the communication systems, as well as verify that the proposed solution will be usable in a weld system. Tests will include measuring induced voltages on the physical medium, as well as counting the number of signaling errors in the communication channel.

Since the project is intended for cost sensitive products the total cost is an important factor to consider. The total cost for each solution will be summarized from suppliers at high quantities intended for production. This cost summary will be a factor when deciding which systems to evaluate as prototype hardware implementations.

3 Technical background

This section will serve as a very brief introduction to some of the technology concepts used throughout this report.

Common Mode and Differential Mode signaling A signal can be transmitted over a wire in Common Mode (CM) or Differential Mode (DM). CM signaling refers to a voltage on a wire referenced to a common ground potential, also known as even mode voltage on a cable pair. DM signaling refers to a voltage between two wires, also known as odd mode voltage on a twisted pair. Figure 3.1 illustrates these voltages for both a single wire referenced to ground, and a twisted pair.

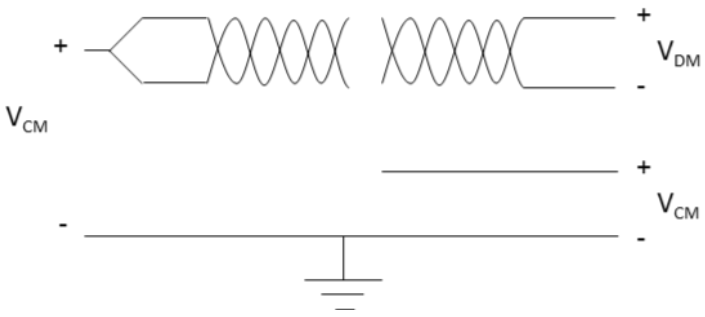


Figure 3.1: Principle for Common Mode and Differential Mode voltages

Baud rate and link speed Electronic communication data bits are often logically represented on the physical medium as a number of symbols. These symbols often consist of more bits than the number of data bits they represent. The reason for this representation can be to provide synchronization or data integrity. One example is to add one start bit before eight data bits, followed by one stop bit. In this case the logical frame to be transmitted carries eight data bit represented as ten physical bits, known as an 8B10B scheme. The transmission speed of physical data bits over a wire, say 9600 per second, is called the baud rate, i.e. 9600 bd. Actual data bits transmitted at that baud rate is $9600 \cdot 0.8 = 7680$ per second, called the link speed, i.e. 7680 bit/s.

UART A Universal Asynchronous Receiver/Transmitter (UART) is an asynchronous serial communication concept used widely in electronic communication systems. Communication is carried over a single wire in each direction, using a predefined communication link speed. The physical medium can take many forms, such as single wire referenced to a common ground potential, differential signaling over twisted pair, and optical signaling either over optical cabling or through free space. Bits are transmitted at the predefined rate from the transmitter. The receiver performs sampling of the line state to detect incoming bits at a rate generally 16 or 8 times that of the baud rate. Typically, when a first bit is detected the receiver starts counting through half the bit, then takes another sample for verification, and then continues by counting the 16 or 8 cycles

to take a sample at the center of the next bit. This counting continues for a predefined number of bits in each frame, typically 10 frame bits for 8 data bits.

Figure 3.2 illustrates the operating principle of a receiver with 8 times oversampling. At t_0 a possible start bit is detected, four cycles later, at t_1, the assumed center point of that bit is sampled again for verification. Another eight cycles later, at t_2, the assumed center point of the first data bit is sampled, after yet another eight cycles, at t_3, the second data point is sampled. This sampling continues until all frame bits have been received.

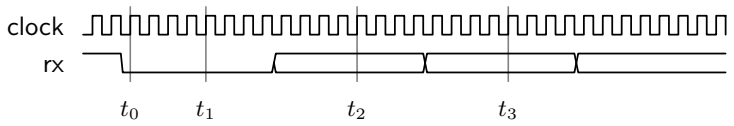


Figure 3.2: Receiver principle for a UART with 8 times oversampling rate

SPI A Serial Peripheral Interface (SPI) bus is a synchronous bus with one or multiple masters connected to one or several slave peripherals. Communication is carried over three wires: clock, Master Output/Slave Input (MOSI), and Master Input/Slave Output (MISO). An optional extra wire per slave can be used to select with which slave the master is communicating. The clock polarity, idle high or idle low, and phase, latching on rising or falling clock edge, are often configurable. Bits are clocked out from the master transmit, MOSI, line 180° out of clock phase, and clocked in to the slave on the configured clock phase. Simultaneously, bits are similarly transmitted from the slave on the MISO line to the master. Figure 3.3 illustrates a simple example with one active low slave select line. Bits are clocked out on falling clock edge, and latched at the receiver side on rising clock edge. In the figure, four bits are sent in each direction.

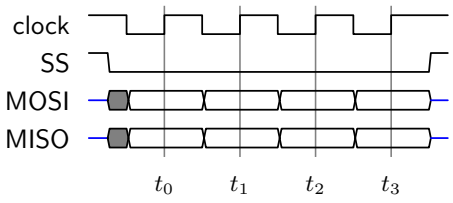


Figure 3.3: SPI bus operating principle

Serializer and deserializer A serializer is a circuit with a parallel bus input and a serial bus output. Parallel words are latched on the input bus and then serially shifted out on the output bus.

A deserializer is, similarly, a circuit with a serial bus input and a parallel bus output. Words are received on the serial bus and output on the parallel side.

4 Current system

A modern weld system consists of one or several enclosures containing power source, wire feeder, gas supply, torch cooler, and other units depending on the weld process used [1]. From the power source, the weld power cable is connected either to a wire feeder or directly to a weld handle and the work piece. Each unit contains one or several ECUs that control the different parts of the weld system. For the system to function, electronic communication messages need to be passed among the ECUs. Communication can be carried between ECUs within a single enclosure or between ECUs in different enclosures. Figure 1.2 illustrates some of the communication and power links in a MIG weld system.

Environments in which a weld system typically operate include industrial fabrication, mining, and ship yards. These environments can be physically rough, as well as include several different weld systems operating on the same work piece generating an electrically noisy environment.

4.1 Regulation loop communication

The power supply unit consists of a digitally controlled Switched Mode Power Supply (SMPS), which is responsible for keeping the set current, and a power supply main control module which is running an outer regulation loop, setting the current value for the SMPS. To enable this outer regulation loop, a communication channel between the SMPS and the main control module is used for real time exchange of status and commands, illustrated by the dashed line between "Main ECU" and "SMPS ECU" in Figure 1.2. The real-time communication is triggered at periodic intervals by a digital control node in the SMPS. At the beginning of each period, a message with a fixed number of fields is sent.

Due to electrical safety requirements there is a need of high voltage isolation between the power supply and control module. Therefore, the communication is carried over an optical fiber cable, connecting the power supply and the control module with a serial bus. This link is configured at 2/3 of the maximum available speed given the current selection of microcontroller, using a custom tightly packed communication frame.

The implemented communication protocol uses dynamic escaping of certain reserved bytes by inserting one extra escape byte before the specific byte, generating a dynamic component to the message frame. For verification of the received data a checksum is also added before sending any message over the communication channel. The handling of this protocol frame is performed strictly in software in the microcontroller, which generates a relatively high Central Processing Unit (CPU) load of approximately 35 %. After processing status data from the SMPS, the microcontroller sends a response command message with a size similar to the SMPS's status message.

Present switching frequency of the power supply gives the possibility of fine grained control over the weld current. With future faster power switching elements, such as Insulated-Gate Bipolar Transistors (IGBTs), this control can be further improved with higher frequencies. Higher frequencies, in turn, requires shorter time intervals of the outer control loop, putting a higher demand on both the speed of the communication link and the processing time in the microcontroller.

4.2 System communication bus

For non-real-time-critical communication among control units, user interfaces, and external components such as wire feeders, the system communicates using CAN buses at 400 kbit/s, illustrated by the dashed line between “Main ECU”, “Display ECU” and “Wire feeder ECU” in Figure 1.2. The communication protocol used on the CAN bus is the standardized CANOpen [3], which provides handling of communication objects and addressing. The bus speed is a limiting factor with larger data transfers, such as software download for firmware upgrades. External communication links can be exposed to both mechanical wear due to the physical environment, and to the electrical noise from the weld cable often running in parallel with the communication cable.

5 Requirements

This section will summarize the requirements on the system to be implemented.

5.1 Weld parameter regulation

For future improvements of the weld process regulation it can be beneficiary to increase the regulation loop frequency. The current system runs the outer regulation loop at a frequency of 10 kHz. The proposed new system has a target performance for the outer loop regulation of weld process parameters at 20 kHz.

The precise setup of the control system is out of scope for this report, only the feedback and control data exchange is considered.

5.2 MCU load

When calculating the next set point value for the outer regulation loop, all calculations are performed in a highly prioritized process on the microcontroller on the control board. The processing load on the microcontroller due to this calculation shall not exceed 30 % to give enough room for other functions to be processed.

A 20 kHz regulation loop cycle means a regulation period of 50 µs. To keep processing load under 30 %, the total processing can take a maximum of 15 µs.

5.3 Performance and speed

Different parts of the system have different requirements regarding the communication link speed. The most critical communication link is the link between the control board and the power source controller, where messages for the outer weld parameter regulation loop are communicated. This communication link needs to exchange sampled values and new set points within the desired 20 kHz regulation cycle. For the weld current source to be able to adjust the output current or voltage in time for the next sample, the next set point shall be returned as soon as possible after the sampled value is sent. If the current value is sampled at the start of the regulation cycle, the next set point should ideally be returned before one half cycle has passed. Given a maximum processing time of 15 µs from reception of sampled values to the sending of new set point values, a protocol with maximum message size 20 B, and for exchanging two message frames in one cycle the minimum link speed becomes

$$\frac{2 \cdot 20 \cdot 8}{\frac{50}{2} - 15} = 32\,\text{Mbit/s} \tag{5.1}$$

The system communication bus shall be faster than the current CAN system, while still enabling communication over distances up to 30 m. Processing of messages of lower real-time priority shall not have a worse response time than the currently implemented CAN system.

5.4 Galvanic isolation

Since the power source of a weld system is connected to the electrical power grid, there is a risk of electrical shock if the mains voltage can come in contact

with any secondary electrical circuits. In a weld system the welding circuit is completely exposed at the weld handle and ground clamp. Therefore it is important with a high level of galvanic isolation between the primary, mains voltage, side and secondary, i.e. welding circuit, side.

The level of isolation for protection against electrical shock in welding equipment is standardized in IEC 60974-1 [4]. These isolation requirements apply to all connections between different ground potential regions in the weld system, including the communication links.

To fulfill the isolation requirements set by the standard, different levels of isolation has been determined between different regions in the weld system. For the communication links investigated in this project, the following levels of isolation shall be met without flashover or dielectric breakdown: the link between the main controller board and the current source controller shall withstand a test voltage of >3833 V, the links between other system components shall withstand a test voltage of >606 V.

5.5 Electromagnetic susceptibility

Since the electrical environment of a weld system is very noisy, the communication links must be designed with EMI tolerance in mind. The requirements regarding ElectroMagnetic Susceptibility (EMS) are expressed as bit error rates in this report. For weld parameter regulation loop messaging, the bit error rate needs to be near zero, especially during critical moments of the weld process.

5.6 Reliability and robustness

For external bus the cables are exposed to multiple connect/disconnect cycles with field conditions. Mechanical wear at the work site also needs to be considered; for example, at a construction site, the cables can get run over by heavy machinery. An external bus failure, such as a short circuit or open bus circuit, shall not propagate into an internal bus failure.

Since weld equipment can be operated both indoors and outdoors, in cold and warm environments, the electronic components need to handle a wide temperature range. The IEC 60974-1 specifies a minimum range of −10 °C to 40 °C, however market specific requirements extend this further. Standard industrial temperature range for components is −40 °C to 85 °C.

5.7 Safety

For personal safety, emergency stop functionality over bus shall be considered. This is especially important for remotely operated power sources. For mixed severity levels on a single bus the criticality level can be assessed [5].

5.8 Cost

Intended applications for the results of this project is systems ranging from larger industrial systems down to compact personal systems. The smaller systems are associated with a lower system cost generating stricter requirements

regarding component cost. Communication solutions considered will have a requirement of keeping the total system cost down. Therefore the total system cost is an important factor when proposing a communication solution.

6 Alternatives

This section describes the different investigated communication alternatives in more detail.

6.1 Regulation loop communication

This section will present and analyze different communication link alternatives for the outer regulation loop.

Asynchronous communication relies on transmitter and receiver to have matching clocks or by other means be able to reconstruct the bit rate for the line. This synchronization can either be performed by matched clock generation circuits at both ends, or by the use of a line encoding that enables clock synchronization.

A simple UART line coding is the 8B10B in which 8 data bits are encoded within 10 line symbols, which consists of one start bit followed by the 8 data bits and finally one stop bit. This 80 % efficiency, requires the baud rate on the wire to be at least 40 Mbd, according to the requirement of 32 Mbit/s bit rate.

In the currently used STM32F4 MCU, the architecture is interconnected with a BusMatrix [6]. This BusMatrix enables communication between bus masters, such as the ARM core and Direct Memory Access (DMA) blocks, and between peripherals and memories. The DMA blocks have dedicated buses to some peripherals, therefore, the main interconnection bottleneck is at the memory ports. Arbitration of BusMatrix masters are performed in round-robin order, which may add additional latency for memory accesses. The CPU can issue transfers up to 14 memory cycles in length, and the DMA blocks can issue burst transfers up to 16 B [7].

6.1.1 Current MCU UART hardware alternative

A block schematic of the current system can be seen in Figure 6.1. The main ECU driven by an STM32F4 [6] MCU is shown to the left and the SMPS ECU driven by a LatticeXP2 [8] FPGA to the right. They are interconnected with a UART channel over optical fiber cables.

The currently used MCU can run the UART at a baud rate up to 11.25 Mbd, which is much lower than the minimum required baud rate of 40 Mbd. Therefore, the overall response time is too high, as can be seen in Figure 6.2.

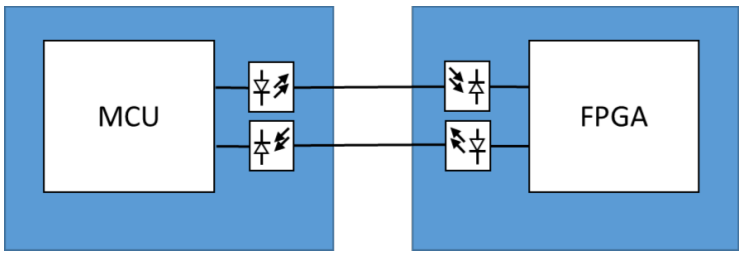


Figure 6.1: Block schematic of communication alternative based on optical UART

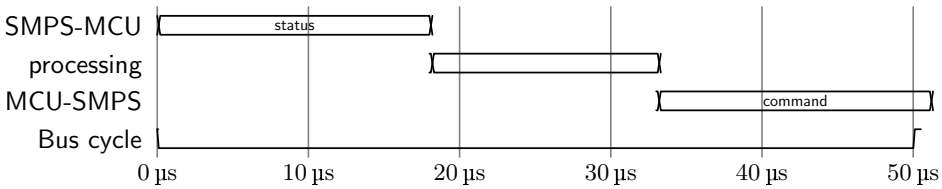


Figure 6.2: Current MCU 11.25 Mbd UART timing diagram, which fails to meet a 50 µs bus cycle

6.1.2 Custom external UART in FPGA

A custom external UART implemented in an FPGA clocked at 320 MHz could perform 8x sampling per bit at 40 Mbd. The FPGA and MCU could be connected with an SPI bus. This method would allow the FPGA to push the received frame to the MCU as it arrives on the UART interface. This setup would make the MCU an SPI slave device, and could let the MCU perform DMA memory transfers from the incoming SPI First In, First Out (FIFO) to buffer memory. A block diagram of this setup can be seen in Figure 6.3.

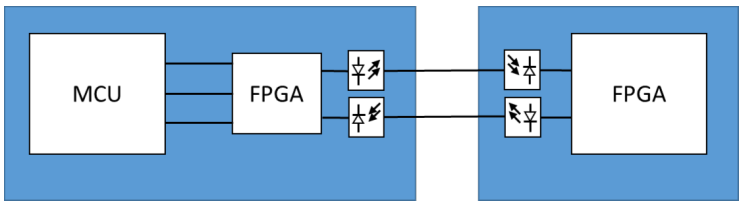


Figure 6.3: Block schematic of external FPGA UART accelerator

The FPGA could also perform protocol operations like detecting start of frame byte for synchronization and performing error detection. With these protocol actions performed in the FPGA, the MCU would only need to parse the data to calculate the next command value. With an SPI clock frequency of 40 MHz, a timing diagram as seen in Figure 6.4 is achieved.

A simple reference UART design from Lattice Semiconductor was synthesized with Lattice Diamond [9] for a Lattice Semiconductor MachXO3L-1300 [10] FPGA. The synthesized design fits with good margin (only 2 % register, 3 % SLICE, 3 % LUT4, and 31 % PIO usage) in the FPGA. This is without the SPI interface or protocol handling; however, those functions should easily fit in the unused logic of the FPGA. Unfortunately, the synthesis for the UART with baud rate 40 Mbd in 8x sampling mode fails to reach the required 320 MHz on the MachXO3, with a critical path only achieving 196 MHz. This limitation is mainly because the simple reference design does not utilize any Phase Locked Loop (PLL) block for the clock generation, with the result that the complete design needs to operate at high frequency with state machine clock dividers.

6.1.3 Serializer/deserializer IC

There exist several different serializer and deserializer integrated circuits which utilize one or several Low-Voltage Differential Signalling (LVDS) serial chan-

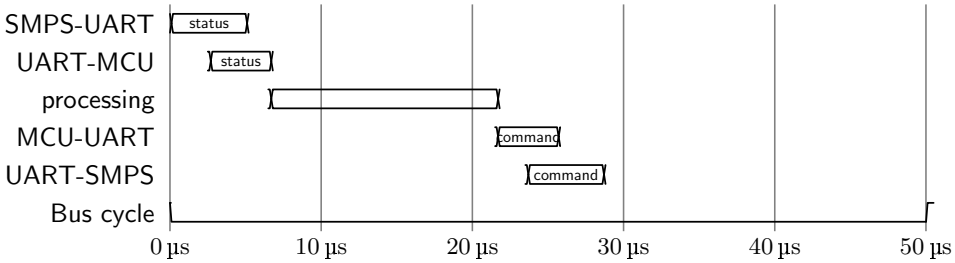


Figure 6.4: External custom UART 40 Mbd timing diagram with 40 MHz SPI to MCU, minimal buffering

nels. Circuits provided by Texas Instruments [11], targeted at backplane signaling as well as twisted pair channels, are configurable between 100 Mbit/s and 660 Mbit/s, with 10 bit words on the parallel side.

For electrical isolation, a signal transformer would be needed at each end of a channel for twisted pair cabling, as illustrated in Figure 6.5. Another alternative is optical transceiver circuits with Positive Emitter-Coupled Logic (PECL) compatible inputs and outputs connected to the LVDS inputs and outputs of the serializer and deserializer circuits [12]. A block diagram of the optical alternative can be seen in Figure 6.6.

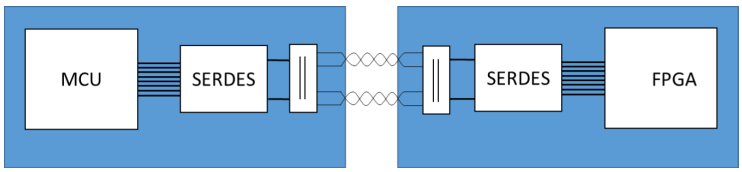


Figure 6.5: Block diagram of serializer/deserializer with copper cabling

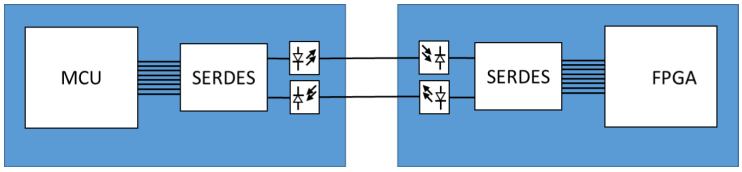


Figure 6.6: Block diagram of serializer/deserializer with optical cabling

A drawback with these circuits is that they must be synchronized before data can be transmitted across the channel. While data is sent, synchronization is enabled by the data frames, however during idle periods the circuits can drift out of sync. Continuous synchronization can be accomplished by sending synchronization pattern frames while no other data is being sent. However, properly detecting if the circuits are in sync requires extra signal lines across the communication channel [11].

Another drawback is the relatively high cost for each circuit at approximately $4, making each channel cost $8 only for the circuits. For dual direction communication, four circuits are needed, at the double of that cost. Line ter-

minations, cabling, connectors, isolation transformers, or optical transceivers would add even more to this cost.

Without dedicated medium access controller hardware, the software needs to perform more protocol operations. One example is the control of link synchronization status.

Figure 6.7 shows a timing diagram for this solution operated at 100 Mbit/s.

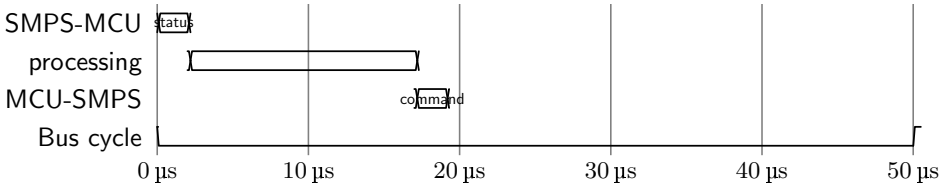


Figure 6.7: 100 Mbit/s serializer/deserializer timing diagram

6.1.4 SPI

To overcome the clock recovery of an asynchronous protocol, a synchronous protocol such as SPI over optical link can be implemented. The current MCU is able to operate SPI at up to 45 MHz as either master or slave. The FPGA in the SMPS can easily operate at any integer divisor of 120 MHz, i.e. 40, 30, 24 or 20. A clock frequency of 40 MHz using the current hardware only requires one additional optical receiver and transmitter pair for the clock signal.

Standard SPI This solution requires a third set of optical communication hardware to carry the clock signal; see Figure 6.8 for a block diagram of this alternative. Since SPI is a master-slave protocol, the FPGA in the SMPS would be the master, since it provides the time base in the system. After transferring the status values to the MCU, the FPGA would then need to wait for processing to be performed and then fetch the command frame from the MCU. This scheme requires a dedicated time slot for the response, in addition to the status frame. Timing for this solution can be seen in Figure 6.9.

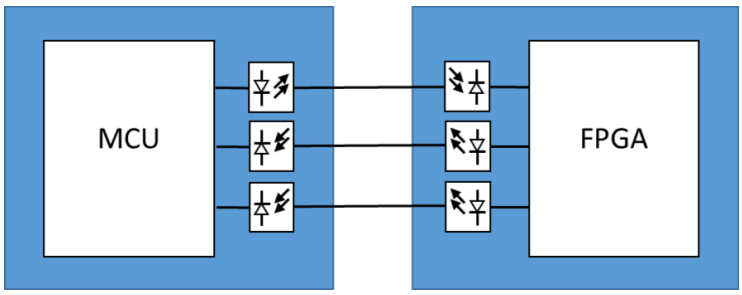


Figure 6.8: Block diagram of SPI over optical cabling

Alternating clock/data To save on the extra optical communication hardware, a setup where the clock and data lines are alternating can be introduced.

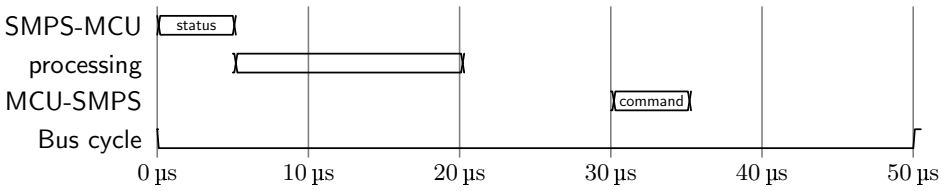


Figure 6.9: SPI 40 MHz over plastic optical fiber timing diagram with time triggered communication and SMPS as master

In this setup, the communication channel will only be able to utilize half duplex communication. This does, however, not impose further restrictions on the system since data is only transferred in one direction at time. When either side is set to receive data, that side will be the clock driver, or master in SPI terms.

In order to allow alternate signaling directions, a sort of Time Division Multiple Access (TDMA) needs to be set up. Since the FPGA provides the most accurate time base, the scheme could work in this order:

1. FPGA holds the role of clock master
2. At time t=0 the FPGA reads 1 B from MCU to initiate the cycle
3. The clock master role switches
4. The MCU reads out the status frame from the FPGA 20 B
5. Next set point is calculated
6. The MCU reads 1 B to indicate that an answer is ready
7. Clock master role switches
8. The FPGA reads the response

A timing diagram of the above scheme can be seen in Figure 6.11. This setup requires no extra hardware on the FPGA side since the alternation of the input and output data and clock line can be gated within the FPGA itself. On the MCU side one 1-2 DEMUX from the RX line to clock or data input, and one 2-1 MUX from clock or data output to the TX line are needed. These MUXes would be controlled by a General Purpose I/O (GPIO) pin on the MCU. See Figure 6.10 for a block diagram of this setup.

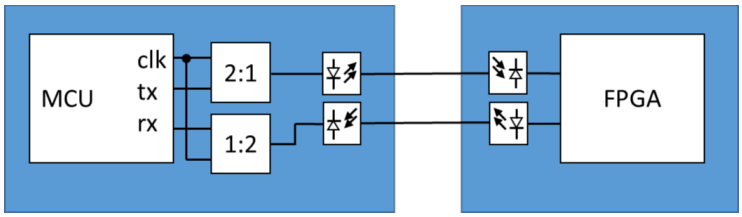


Figure 6.10: Block diagram of SPI over optical cabling with alternating master

This solution is cheap in terms of hardware, but adds a lot to the complexity of the timing of the communication protocol. A messaging protocol would need

to take care of many synchronization corner cases to avoid problems with out of sync or deadlock.

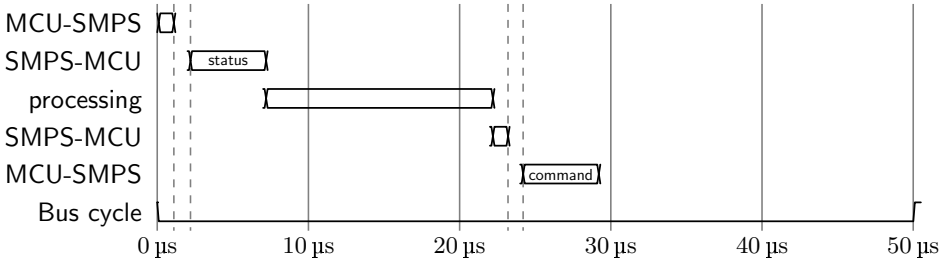


Figure 6.11: Alternating SPI 40 MHz over plastic optical fiber timing diagram with alternating clock master role

6.1.5 Ethernet based alternatives

Ethernet is very common in office IT installations and increasingly considered also in the automotive industry [13]. There are also many automation field bus systems available based on Ethernet, i.e. EtherCAT [14], ProfiNET [15], and SERCOS III [16]. All these systems use the physical and medium access protocol of Ethernet in more or less standard setups.

Cost and isolation Board area requirements for an Ethernet based solution are much larger than the simple UART or SPI optical alternative. As can be seen in Table 6.1, the total cost for a copper Ethernet communication link is less than the current optical solution. Problems with the twisted pair copper wire solution include separation of the ground plane around the Ethernet connector and transformer, and possible EMS of the cabling itself.

One alternative is Ethernet over Plastic Optical Fiber (POF). Avago provides a POF transceiver sized as a standard RJ45 connector [17]. See Figure 6.12 for a block diagram of an optical Ethernet solution.

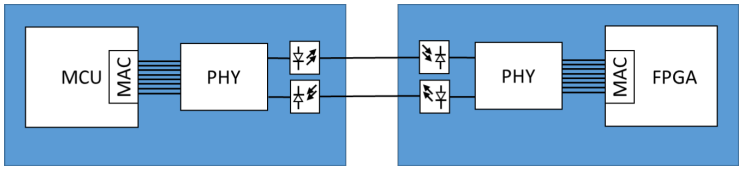


Figure 6.12: Block diagram of Ethernet over optical cabling with MAC as an IP block in the FPGA

On the FPGA side, a Physical layer transceiver (PHY) and a Medium Access Controller (MAC) controller are needed. The PHY can be the same as on the MCU side. Using the same PHY on both sides also keeps development effort down since knowledge of the device can be reused. The MAC can either be a separate chip, as seen in Figure 6.13, or integrated in the FPGA as an Intellectual Property (IP) block, as seen in Figure 6.14. There are even combined PHY and MAC chips available [18].

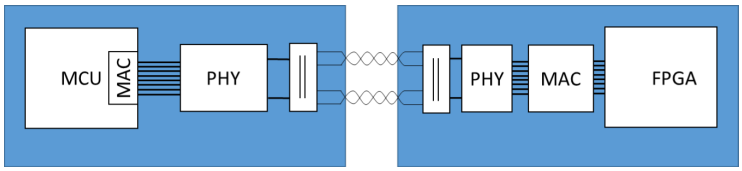


Figure 6.13: Block diagram of Ethernet over copper cabling with external MAC circuit on FPGA side

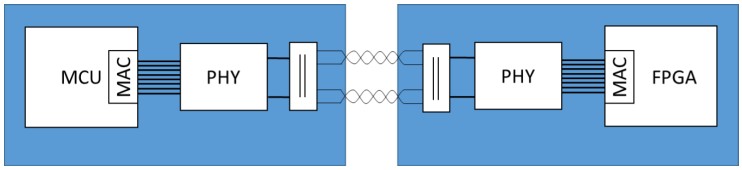


Figure 6.14: Block diagram of Ethernet over copper cabling with MAC as an IP block in the FPGA

Lattice Semiconductor [19] provides an IP core Ethernet MAC configurable at either Fast Ethernet (10/100 Mbit/s) or Gigabit Ethernet. The IP core is available free of charge for evaluation with licensing options for production use. Utilization level for this IP core in the LatticeXP2-5E FPGA corresponds to approximately 37 % of the resources. Therefore, a larger FPGA would be needed, such as the LatticeXP2-8E. With the larger FPGA, the resource utilization corresponds to approximately 23 % instead.

Another alternative for the MAC controller would be to implement a simplified controller. This would be possible since the link and nodes have a predetermined setup. Functionalities that could be optimized away would be for example the 10 Mbit/s, half duplex operation modes and address filtering. A basis for this simplified controller could be the Ethernet MAC project from OpenCores [20]. Another 10/100 Ethernet MAC IP core is available from Cobham Gaisler AB under the GNU General Public License (GPL) [21].

Performance Each Ethernet MAC frame carries an overhead of 26 B. This frame includes standardized Preamble (7 B), Start Frame Delimiter (1 B), Destination (6 B) and Source (6 B) Addresses, Length/Type (2 B), data bytes padded to a minimum of 46 B and a Frame Check Sequence (4 B). A custom protocol with a minimum amount of tightly packed data, i.e. the previously described 20 B, means that the MAC data field needs to be padded to 46 B. This gives a minimum frame size of $26 + 46 = 72\,\text{B} = 576\,\text{bit}$. Therefore the minimum time to transfer one data frame over the wire becomes $576\,\text{bit}/100\,\text{Mbit/s} = 5.76\,\mu\text{s}$. Figure 6.15 illustrates the timing for Fast Ethernet with minimum frame size.

6.1.6 Summary

Table 6.1 gives a summary of the alternatives with related cost. The cost for each solution includes electronic components, connectors, cabling, and any extra component cost if a larger or faster MCU or FPGA is needed. All costs are related to the estimated cost of the current solution. Detailed component lists

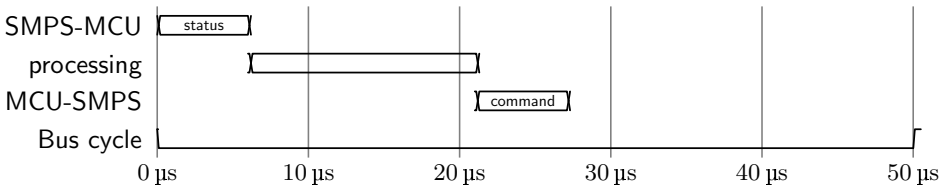


Figure 6.15: Fast Ethernet timing diagram

for the alternatives can be found in Appendix B.

Alternative	Speed	Reg. freq.	Isolation	MCU load	Board area	Cost ($)	Relative cost
Current UART Avago optics/connector	7.5 Mbit/s	10 kHz	>5 kV	35 %	375 mm^2	46.54	1
Ext. FPGA UART XO3L-1300, IF optics/bare	32 Mbit/s	20 kHz	4.5 kV	26 %	570 mm^2	26.69	0.57
SERDES	100 Mbit/s	20 kHz		>30 %			
Copper cabling			4.5 kV		700 mm^2	36.26	0.78
Optical cabling			>5 kV		600 mm^2	63.45	1.36
SPI link	40 Mbit/s	20 kHz	>5 kV	30 %			
Avago optics/bare					760 mm^2	58.16	1.25
IF optics/bare					760 mm^2	36.72	0.79
Alternating SPI	40 Mbit/s	20 kHz	>5 kV	30 %			
Avago optics/bare					450 mm^2	39.01	0.84
IF optics/bare					450 mm^2	24.71	0.53
Fast Ethernet copper	100 Mbit/s	20 kHz	4.5 kV	26 %			
		External MAC			1250 mm^2	30.14	0.65
		MAC in larger FPGA, 1000 units			1000 mm^2	33.23	0.71
Fast Ethernet optical Plastic fiber, “RJ45”	100 Mbit/s	20 kHz	>5 kV	26 %			
		External MAC			900 mm^2	50.72	1.09
		MAC in larger FPGA, 1000 units			650 mm^2	56.99	1.22

Table 6.1: Regulation loop communication comparison table. MCU load is approximated based on profiling of current system and hardware offloading

6.2 System communication

This section will present and analyze different alternatives for system bus communication. When considering a generic system bus with multiple connection points, an important factor is the connection topology. Connection topologies include straight bus with stub connections, ring connections, and star connections. With these topologies reflections, and therefore impedance matching terminations, is an important factor. These terminations are implemented based on transmission line theory [22]. Another important factor is shielding and grounding of the shield to avoid ground loops and noise at the connector [23].

The physical composition of the cable itself is important for reducing EMI, with twisted pair copper cables being preferable over non-twisted wire to reduce DM EMI [24]. For safety aspects regarding for example emergency stop over the communication bus, special care is needed [25, 26]. Such special care includes continuous transmission of safety status messages, with the ability to detect, and act upon, loss or distortion of such messages [27, 28].

Protocol and software aspects when adding or removing a device from the bus are important for ease of use.

6.2.1 CAN

CAN is a traditional communication bus used in vehicle and automation networks [3]. It is well understood and tested but limited in network speed to a maximum of 1 Mbit/s in the base standard. Signaling is carried over one twisted wire pair connected in a traditional bus topology.

An extension to the base standard, CAN Flexible Data-rate (CAN FD), increases the link speed up to 15 Mbit/s. It is backward compatible with standard CAN, since it performs arbitration at standard speed. After the initial arbitration, a bit can be set to indicate that the data portion of the message is transmitted at higher speed. This requires new controllers to operate at that speed, but enables older controllers to communicate with lower speed. Current selection of microcontrollers, in various parts of the system, have integrated CAN controllers which support speeds up to 1 Mbit/s.

MCU manufacturers like ST Microelectronics and Freescale offer products with CAN FD planned or active [29, 30]. These products are currently targeted at high reliability markets and suppliers like Farnell, Mouser, and DigiKey do not hold any of those in stock. General list pricing is not set either.

6.2.2 FlexRay

FlexRay was developed to be the replacement for CAN in safety critical applications like X-by-Wire [31, 32]. The protocol uses TDMA with configurable static and dynamic slots in each time period. Electrical signaling is carried over one single differential pair. The bus can be connected in any of the traditional bus topologies, like single bus with stubs, daisy chained bus, passive star, and active star with repeaters. The FlexRay architecture consists of a communication controller with a host interface to the MCU, and a bus driver (transceiver) with a standardized serial interface to the communication controller. Optionally, a bus guardian can be used to automatically disable the bus driver outside of its time slot for fail silent operation [33].

Electrically, FlexRay has four different signal states: `Idle_LP`, `Idle`, `Data_1`, and `Data_0`. The `Idle_LP` state is simply no differential between ground and either of the conductors, `Idle` has the same bias offset between ground and both conductors. `Data_1` and `Data_0` are represented as either a positive or negative differential of 1.2 V between the two conductors of the twisted pair at the driving side, with a minimum of 0.8 V at the receiving bus interface. Signal recovery in FlexRay is very similar to a UART with eight times oversampling per bit symbol.

FlexRay bus driver circuits are readily available from multiple vendors [34, 35]. Texas Instruments provides safety critical MCU [36] with dual FlexRay controllers running two ARM Cortex-R4F cores, but it is an expensive alternative. There exist other MCU alternatives as well, most targeted at automotive safety critical applications, therefore putting them in the same price range as the Texas Instruments MCU. External FlexRay controller circuits have been manufactured, but they do not seem to be available anymore. Suppliers like Farnell, Mouser, and DigiKey do not hold such circuits in stock.

Research is still ongoing [37], but the FlexRay Consortium website is no longer available after the release of version 3.1 of the standard.

6.2.3 Ethernet based fieldbus

Several fieldbus standards utilize the hardware layer of the standard Ethernet specification. Since Ethernet uses differential twisted copper wire pairs for signaling, it is relatively immune to common mode EMI. The Ethernet standard [38] defines the electrical characteristics of the Ethernet differential pair signaling. The differential voltage, V_{dm}, shall be 450 mV to 1170 mV, positive or negative. Signaling for Fast Ethernet, 100 Mbit/s, is carried on a 125 MHz channel using a 4B5B line coding.

EtherCAT The EtherCAT architecture consists of one master node, which is responsible for initiating all communication, and multiple slave nodes. The master node sends one frame which the slaves read, process and alter in-place as it passes through to send a reply.

The connection topology uses point-to-point physical links. A network can be logically connected as a ring, bus, star or a combination thereof using gateway devices. If the slave does not have a connection to forward the frame on, the frame is returned back on the incoming link.

Each slave has an EtherCAT Slave Information (ESI) file containing its properties such as device profile. The default basic implementation preconfigures the network and all devices using a configuration tool. This tool generates an EtherCAT Network Information (ENI) file which the master uses to communicate with the network. Optionally, the master stack can be extended with dynamic hot connect or disconnect feature. Slave devices detect hot connect or disconnect of links in less than 15 µs [14].

The hardware needed for the master is only a standard Ethernet connection. A software stack is also needed on the master; such stacks are available from several vendors including Acontis [39] and Koenig PA [40]. There are two classes of master devices: class A implements the full master stack, whereas class B can be limited for embedded systems. For the slaves, two Ethernet connectors and PHYs are needed together with an EtherCAT slave controller [14].

EtherCAT has several device profiles including FSoE Safety over EtherCAT complying to the Safety Integrity Level SIL3.

EtherCAT uses standard Ethernet frames and can be encapsulated in UDP/IP for transport over a larger network. There is also an option of using the CAN application protocol over EtherCAT called CAN over EtherCAT (CoE).

Custom protocol over Ethernet Since a weld system consists of a small number of predetermined nodes, a custom protocol can be encapsulated directly in an Ethernet frame to minimize processing overhead. Two Ethernet ports on each board with a switch circuit connecting to a third port toward the microcontroller can be used to build a high speed bus architecture. There are microcontrollers with integrated Ethernet switch and dual MAC controllers for this scenario [41]. Standalone dual-port Ethernet with integrated MAC and PHY circuits with a third host bus are also available [42].

This setup is very similar to EtherCAT and PROFINET, except that a custom protocol is used instead of the standardized one. One specific example would be to encapsulate CANOpen [3] directly in the Ethernet frames to provide an easy upgrade path for the software but drastically increase the bus speed.

Real time and prioritizing properties of the bus are drastically different between the CAN and Ethernet systems. In a CAN bus system, prioritization of messages are handled at the electrical signaling level. If multiple nodes start sending messages at the same time, only the message with highest priority based on message id will be transmitted in full on the bus [3]. In an Ethernet based system, on the other hand, only one frame is allowed on any link at a time, with collisions handled by retransmissions [38]. The proposed system above with point-to-point links interconnected with small three-port switches at each node will only let one message at a time pass between any two nodes in the system. Therefore, prioritization of messages needs to be handled either dynamically in a software stack, or statically by a TDMA scheme.

6.2.4 One-Pair EtherNet

BroadR-Reach specifies an Ethernet communication system over a single twisted pair, and is standardized by the OPEN (One-Pair EtherNet) Alliance Special Interest Group [13]. It is developed for the automotive industry, with focus on cost and EMI. The standard enables 100 Mbit/s link speeds over links up to 25 m.

BroadR-Reach specifies the physical layer of the Ethernet standard, with the standard Media Independent Interface (MII) to the MAC. PHY devices [43, 44], are in early stages of being released to the market. Capacitive coupling can be used between the PHY and the twisted pair cable, eliminating the need of a signal transformer, possibly reducing the cost of the interface. These products are not yet available at general electronic distributors, and no list price has been set.

6.2.5 Summary

Table 6.2 gives a summary of the alternatives with related cost. For CAN FD the cost of the CAN controller is not included, since no available product with such a controller was found to be available at the time of this project. BroadR-Reach

PHY cost is not included since no pricing was set. A cost for the EtherCAT master stack was also not publicly available, however the overall cost for an EtherCAT solution becomes much higher than the corresponding cost for CAN, FlexRay, and likely also a CAN FD solution. Detailed component lists for the alternatives can be found in Appendix C.

Alternative	Speed	Isolation	Cost ($)	Relative cost
CAN	1 Mbit/s	2.5 kV	4.68	1
CAN FD	8 Mbit/s	2.5 kV	4.65+	> 1
FlexRay	10 Mbit/s	2.5 kV	15.09	3.22
EtherCAT master	10/100 Mbit/s	1.5 kV	12.81+	> 2.74
EtherCAT slave	10/100 Mbit/s	1.5 kV	20.99	4.48
Custom Ethernet master	10/100 Mbit/s	1.5 kV	12.38	2.65
Custom Ethernet slave	10/100 Mbit/s	1.5 kV	20.35	4.35
BroadR-Reach master	100 Mbit/s	1.5 kV	3.39+	> 0.7
BroadR-Reach slave	100 Mbit/s	1.5 kV	14.85+	> 3.17

Table 6.2: Inter board communication comparison table

6.3 Wireless communication

This section will give a short overview of some of the available technologies for wireless communication that can be applicable to an industrial setting. Due to time constraints during the project, an in-depth evaluation was not possible to perform on the wireless link alternatives.

In a weld system operated in an industrial environment, long external cables between weld system units can be problematic. Cables can become damaged when moving equipment around, they can pick up considerable amounts of EMI when running in parallel with long high-current weld cables, and they can be a work place hazard if tripped over by workers. For these reasons, wireless communication alternatives can be of interest for communication between separate units in a weld system.

Link distance between units in a weld system can range from less than one meter up to tens of meters, between power source and wire feeder. Weld systems can be operated in environments with multiple weld systems nearby, increasing the possibility of inter-system interference. In certain construction environments, such as ship construction, weld systems can be operated in environments where radio signals can be blocked by for example thick steel walls.

CAN in Automation has standardized a CANOpen gateway profile, CiA 457 [3], which specifies messaging between wired and wireless CAN networks. The physical layer is not specified. Alternatives that could be considered include WirelessHART [45], IEEE802.15.4/IEEE802.15.4e [46, 47], Bluetooth [48], and wireless Ethernet [49]. Table 6.3 lists these alternatives with important parameters.

6.4 Communication over weld cable

Investigations into communication over weld cable was not thouroughly performed mainly due to time constraints, but also because of a related patent [50].

Alternative	Operating frequency	Maximum speed	Approximate range
WirelessHART	868 MHz, 902-928 MHz, 2.4 GHz	250 kbit/s	10 m
IEEE802.15.4	868 MHz, 902-928 MHz, 2.4 GHz	250 kbit/s	10 m
Bluetooth	2.4 GHz	1 Mbit/s	10 m
Wireless Ethernet	2.4 GHz, 5 GHz	>11 Mbit/s	25 m

Table 6.3: Wireless communication alternatives comparison table

This patent protects the use of Binary Phase Shift Keying (BPSK) modulation over weld cable for communication using carrier frequencies of approximately 128 kHz and 141 kHz. There are, however, several other modulation techniques that could be investigated instead, such as Quadrature Amplitude Modulation (QAM), Frequency Shift Keying (FSK), and higher order Phase Shift Keying (PSK).

An important aspect for communication over weld cable is the communication channel characteristics of the power cable in combination with the modulated weld current. A similar scenario has been investigated [51] for communication over three-phase power cables with pulse-width modulated electrical motors. The study concluded that for the carrier frequency investigated (70 MHz), the three-phase power cable was not suitable for data communications.

Commercially available alternatives exist, some of which are based on the standardized Broadband over Power Line Networks [52]. This standard utilizes Orthogonal Frequency-Division Multiplexing (OFDM) with speeds up to 500 Mbit/s.

7 Hardware prototype

This section will describe prototype hardware used or manufactured for purposes of measurements. When selecting components it is important to consider whether they are designed for EMI tolerance. This is especially important for PHY devices connecting to long copper cables. Transceivers can be designed in certain configurations for EMI tolerance [53]. Often, the details of a PHY design are not published, however many manufacturers mention EMI tolerance as a feature of certain PHY devices.

7.1 Ethernet

To evaluate Ethernet over copper cabling, an existing prototype board with Fast Ethernet hardware was used. This board only had a 1500 V isolation signal transformer, but measurement setups were prepared such that the high levels of isolation were not needed. A higher level of isolation can be achieved for copper based Ethernet by utilizing a 4500 V isolation signal transformer and designing the Printed Circuit Board (PCB) with large clearance of more than 18 mm around the analog Ethernet signals.

To suppress CM EMI on the Ethernet cable, the use of Common Mode Choke on the differential signals between the connector and transformer is beneficial [54–57]. On the utilized prototype boards there was one common mode choke [58] on each of the receive and transmit channels. The Ethernet transformer [59] had one common mode choke on each of the receive and transmit channels integrated as well.

The shielding of the Ethernet connector was connected to a ground plane common for the analog Ethernet signal components between the connector and transformer. This ground plane was connected to the board DC ground plane through a ferrite inductor. Figure 7.1 illustrates the reference Ethernet analog circuit with extra common mode chokes on receive and transmit pairs.

Since the inductor from Ethernet ground to board ground provides a DC path from the wire into the board, it counteracts the intended high potential isolation. For test purposes this inductor was removed in some of the performed measurements, see section 9.2.1 for further details.

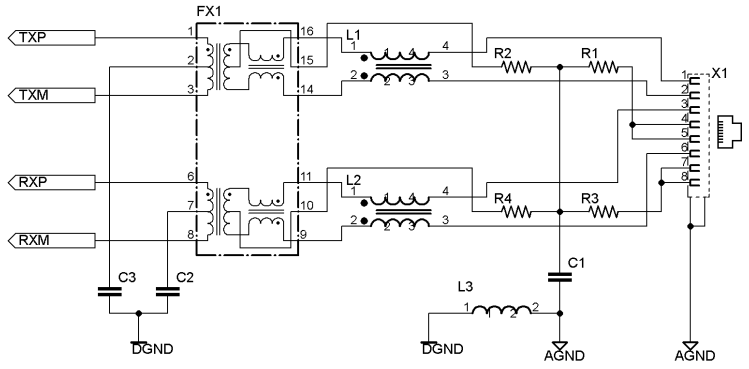


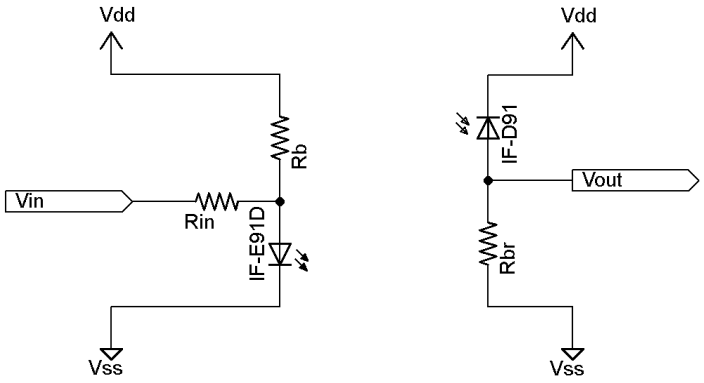
Figure 7.1: Ethernet analog side with extra common mode chokes between connector and signal transformer

7.2 Optical SPI

To evaluate the use of SPI over optical cabling, a simple test circuit was constructed. Optical modules from Industrial Fiberoptics were used, which require external biasing for the sender LED [60] and receiver photodiode [61]. For cabling between transmitter and receiver, 1 m of plastic optical fiber was used [62].

Biasing the sender diode with a current of 20 mA gives an output power at the end of 1 m cable of $-9.6\,\mathrm{dB\,mW}$ to $-7.4\,\mathrm{dB\,mW}$ according to the datasheet [60], with typical output power $-8.2\,\mathrm{dB\,mW}$. The receiver has a responsivity of $0.4\,\mu\mathrm{A}/\mu\mathrm{W}$ at 632 nm [61]. At the typical transmitter output power at 20 mA, the receiver photodiode would drive 60 µA through the load resistor.

A bias circuit, as seen in Figure 7.2a, based on the datasheet measurement circuit, was used for the transmitter.



(a) IF E91D transmitter bias circuit (b) IF D91 receiver bias circuit

Figure 7.2: Industrial Fiberoptics transmitter and receiver bias circuits

Since the target design uses $V_{dd} = 3.3\,\mathrm{V}$ and the test circuit in the datasheets were designed for 5 V, the biasing component values were recalculated. Resulting bias resistor values are:

$$R_b = 396\,\Omega \approx 470\,\Omega \tag{7.1}$$

$$R_{in,max} = 126\,\Omega \approx 120\,\Omega \tag{7.2}$$

See Appendix A for the full calculations.

For the receiver, a bias circuit as shown in Figure 7.2b was used. The MCU [6] requires input voltage to be higher than 2.31 V for logic high, and lower than 0.99 V for logic low. The FPGA [8] requires input voltage to be higher than 2.0 V for logic high, and lower than 0.8 V for logic low. To generate a voltage higher than 2.31 V over the R_{br} resistor when driving 60 µA the resistor needs to be at least $38.5\,\mathrm{k}\Omega$.

The setup of one optical channel, with the previously calculated resistor values, was tested with a 2 MHz square wave signal generator and an oscilloscope. This test resulted in very slow slew rates on the measured output signal, resulting in a signal that was only a few millivolt peak-to-peak. These slow slew rates are the result of the capacitance over the reverse-biased photodiode, in combination with the large resistor to ground.

By testing a few combinations of transmitter biasing currents and receiver load resistors, a peak output voltage at 2 MHz was found to be 40 mV AC. This was achieved with a transmitter bias current of approximately 30 mA in combination with a receiver load resistor of 1.5 kΩ, also generating a DC voltage offset of approximately 160 mV at the output.

Since the output voltage from the receiver was too low to directly drive a logic input, an amplifier circuit was designed and simulated. The amplifier circuit was based on an optical receiver design solution from Linear Technology [63], which consists of a transimpedance amplifier and a high speed comparator circuit. A current source (I1) was used to simulate the photodiode, as can be seen in Figure 7.3. This circuit also includes the parasitic capacitance (C1) over the feedback resistor (R3). The output drives a capacitance (C4) modeling the input capacitance of the MCU.

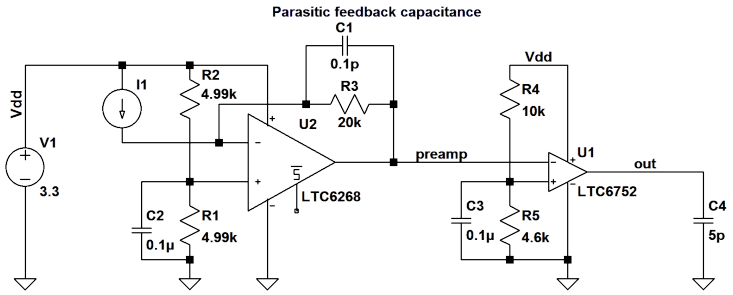


Figure 7.3: IF D91 receiver amplifier simulation circuit

Simulation results show an AC transfer function with good margin at 40 MHz, as seen in Figure 7.4. Simulated rise and fall delay is approximately 5.5 ns, as can be seen in Figure 7.5a and Figure 7.5b.

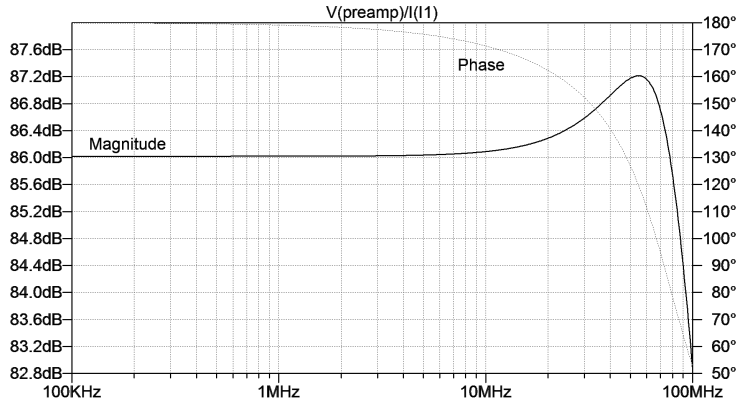
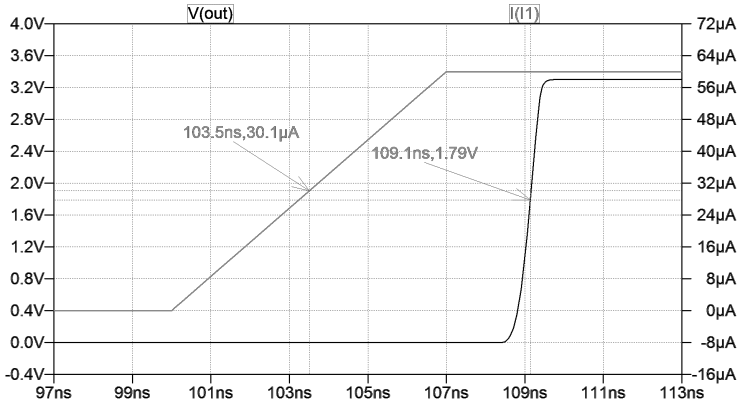
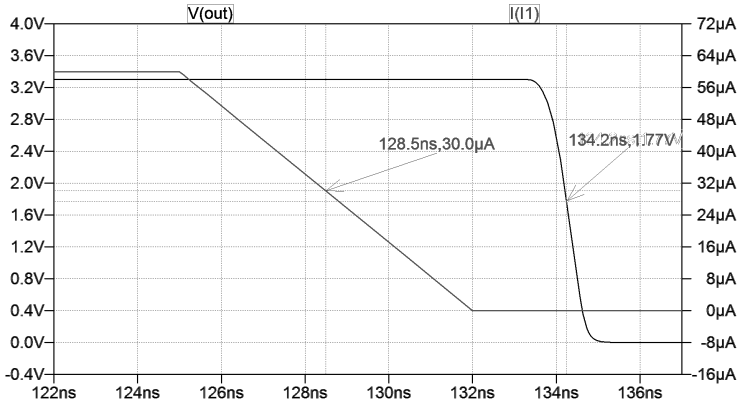


Figure 7.4: IF D91 receiver amplifier simulated AC transfer function



(a) Rise delay time



(b) Fall delay time

Figure 7.5: IF D91 receiver amplifier simulated delay times

8 Software

This section describes software implemented for profiling, demonstration or prototype applications.

8.1 MCU load considerations

When considering software implementations, the MCU performance needs to be considered in the early design. This is especially important for the hard real-time regulation loop communication channel. To minimize MCU load, a DMA controller can be used to receive data into and send data from system memory. The currently used MCU has several different memory systems, including the possibility of external Random Access Memory (RAM). With the BusMatrix of the currently used MCU, DMA and CPU masters can access different memory systems at the same time without penalty idle cycles. MCU load in such a setup would originate mainly from communication protocol overhead processing, and calculation of the next set point value.

8.2 Regulation loop Ethernet demonstration

A simple demonstration was set up for the alternative of passing the regulation loop messages over the Ethernet protocol. The hardware used was an already existing control board prototype with Ethernet PHY [64], Ethernet transformer, and RJ45 connector for copper Ethernet. Since the microprocessor on that board [6] included a MAC hardware block with dedicated DMA controller and Cyclic Redundancy Check (CRC) calculation block, the idea was to minimize MCU utilization by doing as little as possible in software.

When a data frame arrives at the MAC block in the MCU, the data bits of the frame are stored in a temporary FIFO. Once the FIFO has filled to a preset level, a dedicated DMA starts to copy the frame into a predefined receive buffer in MCU main memory. As soon as the frame has been transferred to the receive buffer, an interrupt is generated, enabling the software to begin processing the arrived frame. Each buffer segment can be owned by either the DMA or the CPU, such that if the CPU has ownership, the DMA will not overwrite any data in that buffer segment. A control bit in the buffer memory is used to signal the ownership of each segment.

To complete the Ethernet physical layer, a PHY device is connected to the MAC to translate the digital signals into symbols on the wire. The PHY on the above-mentioned hardware board is connected using the Reduced Media Independent Interface (RMII) towards the MAC. ST Microelectronics provides a library for this line of microprocessors, including a Hardware Abstraction Layer (HAL) for the Ethernet MAC. This HAL needed to be configured and extended to support the PHY device on the board for proper initialization after power up. Minor modifications, such as the bus address and internal register addresses of the PHY, was set up and a modified initialization function was written.

Once the PHY initialization was implemented and verified, software was written which listened for raw MAC frames containing octet fields very similar to the already implemented communication protocol. No filtering on MAC addresses was performed since the intended system has a predefined set of nodes.

The protocol frames consisted of one octet indicating the type of frame, followed by nine data field octets consisting of values of one or two octets in width. The two octet wide fields were transferred in microcontroller native endian order (little endian), which generates minimal processing of the data after arrival before it can be used in the application.

In the demonstration software, a C struct was set up such that the compiler aligned each field in the same order and at the same memory offsets as the data fields in the received frame. The compiler used was the GNU Compiler Collection (GCC) [65] which can be instructed to pack struct fields smaller than one word to achieve this, see Listing 1. It must, however, be noted that this type of compiler and target CPU dependancy greatly reduces portability of the software. Any such implementation is therefore to be kept to a minimum, and only if needed to fulfill strict performance requirements.

As seen in Figure 8.1, the payload of an Ethernet frame, without 802.1q tag field, starts at the half-word boundary when stored on a 32-bit system. The ARMv7-M architecture [66] enables loading and storing of byte fields on each byte boundary, half-word fields on each half-word boundary and full words on each word boundary without introducing extra load cycles. In this case the fourth field in the frame is a 16 bit (half-word) field but not aligned on the half-word boundary, see Figure 8.2. Since an unaligned half-word cannot be directly loaded into the registers by the CPU architecture, the accesses for that field are translated by the compiler into two accesses to the corresponding high and low bytes of the half-word. This slight performance hit can be rectified by inserting padding into the protocol to align each data type on the corresponding memory boundary, as illustrated in Figure 8.3 and Listing 2.

When the interrupt from the MAC DMA was triggered, the software used the first memory address, with an added offset of 14 B for the MAC headers, of the receive buffer as the base address for the struct. After that the address pointer for the struct could be passed to the code generating the response frame based on the frame type and values of the frame fields. In this case only a simple mockup with minimal processing was used to isolate protocol handling time from processing time.

The response data frame was filled directly into the DMA send buffer using a similar struct as the receive frame. With this scheme there is minimal passing of data between functions and methods, only one address word for the received and sent frames each.

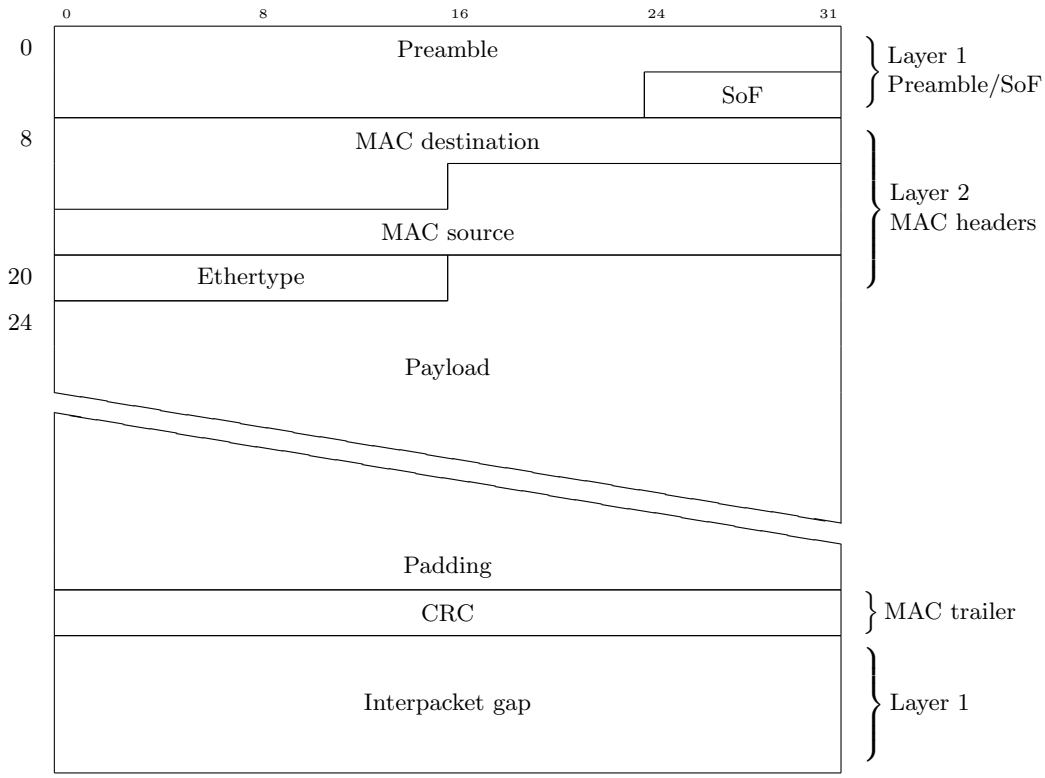


Figure 8.1: Structure of minimum length Ethernet packet as seen on wire. Octets numbered on left side, bits numbered on top

```
1   struct receivedFrame {
2     uint8_t  type;
3     uint8_t  data1;
4     uint8_t  data2;
5     uint16_t data3;
6     uint16_t data4;
7     uint8_t  data5;
8     uint16_t data6;
9     uint8_t  end;
10  } __attribute__((
        __packed__));
```

Listing 1: Receive frame struct, tightly packed in memory

```
1   struct receivedFrame {
2     uint8_t  type;
3     uint8_t  data1;
4     uint8_t  data2;
5     uint16_t data3;
6     uint16_t data4;
7     uint8_t  data5;
8     uint16_t data6;
9     uint8_t  end;
10  };
```

Listing 2: Receive frame struct, implicitly padded

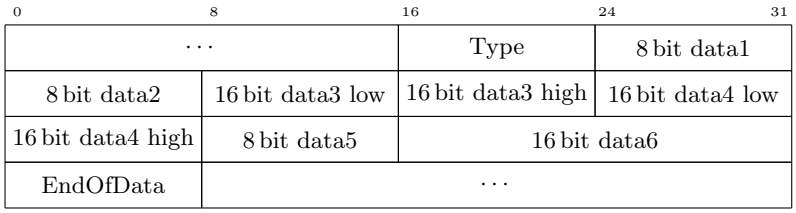


Figure 8.2: Structure of evaluated protocol data using tightly packed frame, as represented in Ethernet receive buffer memory.

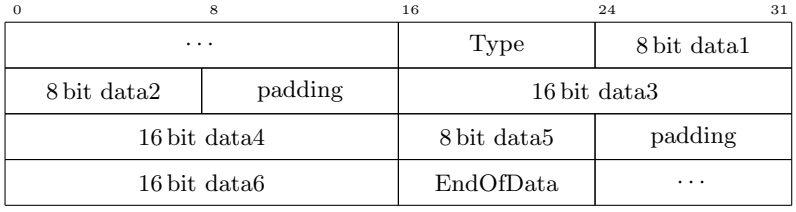


Figure 8.3: Structure of evaluated protocol data using padded frame, as represented in Ethernet receive buffer memory.

9 Measurements and verification

This section contains profiling of software and measurements on running hardware prototypes.

9.1 Microprocessor utilization

To profile the time it takes for various software functions to execute on a microcontroller, a simple measurement setup was assembled. In the software a GPIO pin was toggled at the start and end of the code path to be profiled, generating a step response which had a width corresponding to the time passed during execution of the code path. The GPIO pins in the target MCU operate at a maximum frequency of 90 MHz, therefore introducing a maximum delay of 11 ns between the ARM core operating at 180 MHz and the GPIO pin. However the delay is small compared to the microsecond time scale being measured, and introduced approximately equally on both set and reset operations. The voltage level on the physical pin was measured using an oscilloscope. Adding this overhead of toggling a GPIO pin introduced approximately 0.05 µs to the target microprocessor software execution time for each toggle.

9.1.1 Current implementation profiling

At the beginning of the project, the current implementation was profiled to gain knowledge of the regulation loop induced MCU load. The measurement setup consisted of hardware prototype boards with software executing the outer regulation loop in a demo application. To measure timing, a GPIO pin toggle as described above and the UART pins at the MCU was measured with an oscilloscope. The result can be seen in Figure 9.1, showing a measurement with the full weld regulation loop running. It was seen that turning off the weld regulation, i.e. no active weld process but with idle command messages being exchanged, decreased the MCU time by up to 10 µs depending on type of weld process. Therefore this time was considered the inherent regulation process time of the software, and the rest of the time considered as parts of protocol processing.

Other specific protocol operations were also measured to get a deeper understanding of what was loading the MCU, as can be seen in Table 9.1.

Operation	Measured time
Checksum calculation	2.2 µs
Framing and escape handling	6.8 µs

Table 9.1: Measured protocol software operation timings on existing implementation

9.1.2 Profiling of Ethernet demonstration

The simple demonstration software described in section 8.2 was loaded on the target board and started in debug mode using a Joint Test Action Group (JTAG) connection with the development environment. An Ethernet cable was connected to a computer running a simple software sending Ethernet MAC

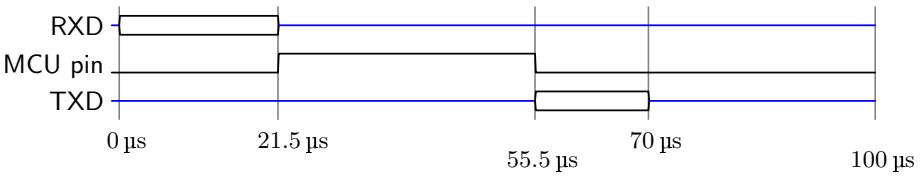


Figure 9.1: Measured timings on existing implementation

frames with the custom protocol. The test application sent Ethernet frames at a configurable rate, enabling measurements of the timings for protocol handling. A GPIO pin was toggled at the beginning and end of the interrupt service routine handling the protocol.

Receive and transmit channels were measured between the PHY and MCU with an oscilloscope with a bandwidth of 100 MHz. The intention of this measurement was not to distinguish between individual bits on the channel, but only to see when the line was idle or transmitting data. Measured timings are illustrated in Figure 9.2.

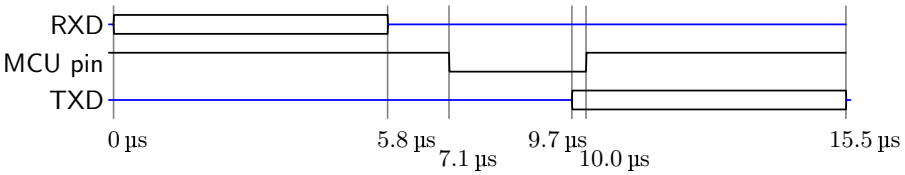


Figure 9.2: Measured timings basic Ethernet frames

9.2 Electromagnetic interference

For evaluation of high speed communication channels over twisted pair copper wires, measurements in a weld environment was performed. Different cable types were evaluated to assess the impact of shielding to EMS in the strong EMI fields within a power source.

It has previously been shown by Pritchard and Smith [23] that Unshielded Twisted Pair (UTP) cabling can have equally good EMI performance as Shielded Twisted Pair (STP) cabling. They also show that the quality of the shielding is important, and that a poorly terminated shield can potentially disturb the receiver circuit more than an unshielded cable setup.

Measurements were performed with isolated power supply to the prototype boards, as well as with power supply from the weld power source.

9.2.1 Isolated power supply Ethernet over twisted pair

Measurement setup for Ethernet in the power source was divided in different steps according to Table 9.2. During the test, communication frames were sent between two control boards with 81 B payload. One of the boards sent a frame every 40 µs to the other board, which performed a simple addition in one field of the payload and returned it back to the sender. This resulted in data on the

wire approximately 42 % of the time. The CRC was verified by the MAC on the receiver and any errors counted.

Once every second the current CRC error counters were printed over a serial UART channel connected to a laptop via a USB adapter. This output data was logged for later analysis. The setup is illustrated in Figure 9.3.

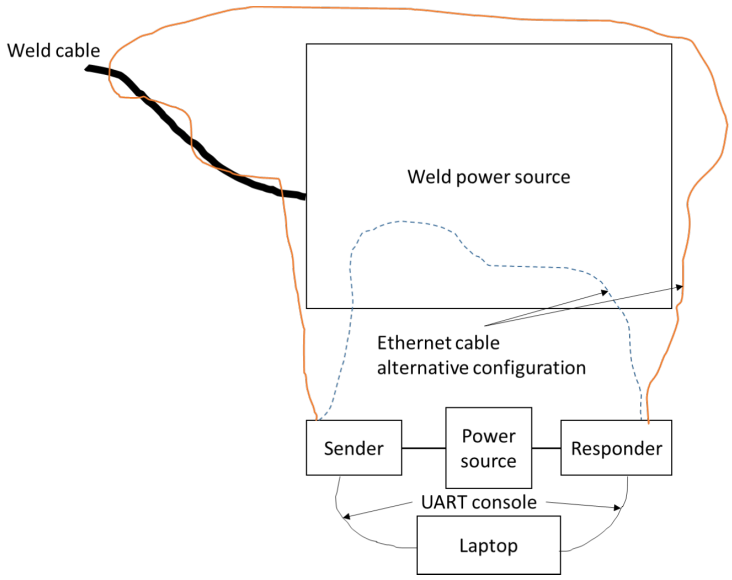


Figure 9.3: Simple Ethernet EMI evaluation measurement setup with independent power supply to communicating ECU boards

The power source used for these tests runs with an inverter frequency of 40 kHz. As seen in the test setup, the prototype boards with Ethernet communication were both connected to a separate potential isolated from the power source itself. A Metal Active Gas (MAG) weld process was used with a combination of wire dimension and shield gas composition that produced a weld current of approximately 125 A to 150 A. Welding was started three or four times for each cable alignment and welding approximately 20 s to 30 s at a time. The results of these tests showed no effect on the Ethernet communication, however noise was coupled back into the UART cabling for test setups 3, 5, 8 and 9.

9.2.2 Power source potential Ethernet over twisted pair

To evaluate the use of 100 kHz inverter frequency in combination with using the potential of the weld system, a test was set up using a prototype weld machine. The test was set up using the same ECUs and software as the test with the MAG weld power source. However, in this setup one of the ECUs was powered by the control power potential of the inverter. This test setup can be seen in Figure 9.4.

The weld process used was MMA welding, producing weld currents in the range of 150 A to 220 A. Welding was started three or four times for each cable alignment and welding approximately 20 s to 30 s at a time.

During active weld process disturbances were noticed on the current from the external power supply. These disturbances were traced to the ground loop

Test no	UTP	STP foil	Weld system	Cable placement
1	X		MAG	Inside power source, along outer border of inverter
2	X		MAG	Inside power source, three turns around outgoing positive pole, after inverter filter inductor
3	X		MAG	Inside power source, three turns around input cable to rectifying diode for weld current
4	X		MAG	Inside power source, three turns around outgoing negative pole, after inverter filter inductor
5	X		MAG	Outside power source, spiraling negative weld cable between power source and wire feeder 1.5 m
6		X	MAG	Inside power source, along outer border of inverter
7		X	MAG	Inside power source, three turns around outgoing positive pole, after inverter filter inductor
8		X	MAG	Inside power source, three turns around input cable to rectifying diode for weld current
9		X	MAG	Outside power source, spiraling negative weld cable between power source and wire feeder 1.5 m
10	X		MMA	Inside power source, along outer border of inverter
11	X		MMA	Outside power source, spiraling negative weld cable between power source and return clamp approximately 2 m
12	X		MMA	Inside power source, three turns around input cable to rectifying diode for weld current
13	X		MMA	Inside power source, three turns around input cable to rectifying diode for weld current
14	X		MMA	Outside power source, spiraling negative weld cable between power source and return clamp approximately 2 m
15		X	MMA	Inside power source, along outer border of inverter
16		X	MMA	Inside power source, two turns around input cable to rectifying diode for weld current

Table 9.2: Ethernet cable EMI test measurement setups

formed over the UART serial channels through the USB connections over the laptop. After the console to the ECU in the weld power source was disconnected, these disturbances were eliminated.

To test the behavior with Ethernet chassis ground isolated from board ground, the inductor between these two copper planes was removed for tests 13 through 16.

After rerouting the Ethernet cable for test number 14, the external ECU indicated CRC and receive errors for approximately 20 % of the packages continuously. The fault was traced to badly formed solder joints on the Ethernet connector and PHY. Re-soldering these components fixed these issues completely.

Other than the issues with the solder joints, the result of all these tests showed no errors on the Ethernet communication link. This test setup did not result in any bit errors on the UART channels either, however only one was connected for most of the tests.

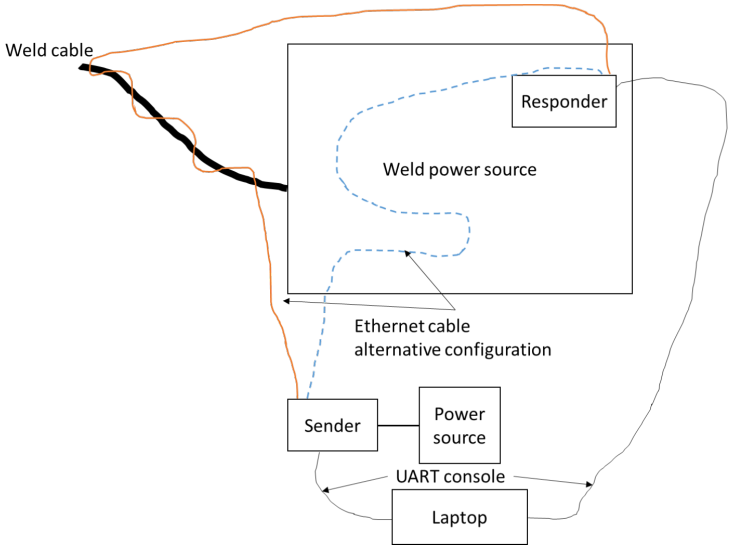


Figure 9.4: Simple Ethernet EMI evaluation measurement setup with one node powered by the weld system and the other by a separate power supply

10 Discussion

This section contains discussions related to measurements and suggested implementation alternatives. The project planning will also be discussed.

10.1 Hardware

Hardware aspects of the different communication solutions are discussed in the following sections.

10.1.1 Regulation loop communication

The investigations for the regulation loop communication indicate that either a synchronous serial channel such as SPI, or a more advanced line encoding such as Ethernet, is needed for the required throughput. An asynchronous protocol, such as a simple UART, requires high oversampling frequencies to avoid being sensitive to differences in clock frequencies on either side of the communication link.

The evaluations performed indicate that a copper Ethernet solution can be used. One important aspect of the evaluated hardware prototype is the extra common mode choke on the Ethernet data channels.

A large isolation signal transformer must be integrated on either side of the communication channel due to electrical isolation requirements. The evaluations were, however, performed with a smaller, standard, Ethernet signal transformer on both sides. A larger transformer can, due to having a larger transformer core, be more susceptible to the strong alternating magnetic fields present close to the SMPS transformers. This can be seen from Faraday's law and the relation between magnetic flux density and total flux. With an average magnetic flux density, $B(t)$, the total flux, $\Phi(t)$, through a surface area, A_c is

$$\Phi(t) = B(t)A_c \tag{10.1}$$

which together with Faraday's law gives the induced voltage at the ends of a conductor loop around the surface area

$$v(t) = \frac{d\Phi(t)}{dt} = A_c\frac{dB(t)}{dt} \tag{10.2}$$

This indicates that a larger transformer, with larger core and larger winding loops, can be more susceptible to noise induced by external alternating magnetic fields.

Another issue with copper Ethernet is the standard connectors, which might not be robust enough for long term use in a weld system. Connections might fail due to being exposed to a dusty environment or mechanical shock. A solution for that problem might be to use a more robust pin-header-like connector, with a firm snap lock feature.

To save on cost, not all four twisted pairs of the standard CAT5e cable are needed since only two of them carry the communication signals. Using a cable without the unused pairs might be beneficial in terms of EMI as well, since the extra wires can pick up more common mode noise, which needs to be fed to a return path on either side of the communication link.

An optical link, on the other hand, is immune to the high levels of EMI along the cables, and at the same time provides high galvanic isolation. For short link distances, plastic optical fiber is an alternative that is beneficial, in terms of cost, over glass fiber solutions. Standard Ethernet solutions for plastic optical fiber are, however, more expensive than copper Ethernet.

Instead of an Ethernet based line encoding system, other serializer/deserializer circuits are available. These circuits, however, are more expensive than a standard Ethernet PHY and also require handling of synchronization to operate properly.

For synchronous communication, the cheap optical modules from Industrial Fiberoptics are interesting because of the low price. These modules do however require biasing and amplification circuitry, for interfacing directly with MCU or FPGA I/O ports, which adds to the price and complexity. Another aspect with these modules is that their enclosures are not sealed or molded, which requires special attention in a PCB production line. Solder flux needs to be washed away such that it does not obstruct the optical lens of the module.

For use in a weld system these modules must also be evaluated with respect to dust entering the module. These aspects can be rectified by using molded optical modules instead, such as the ones available from Avago, or by using a careful PCB washing process and applying a coating on the PCB afterwards, sealing the gap between board and optical module.

Cable connection system of the optical cable is also important for two reasons: mechanical shock tolerance and dust resistance. The optical modules evaluated either had a mechanical connector attached to the cable, with a snap lock to the optical module (Versatile-Link), or a screw lock integrated in the module which tightened around the bare cable end. The screw lock with bare cable end system is cheaper since no connector is needed, and it might also be more resistant to dust entering the optical module, however further testing of this is required for a proper evaluation.

For integrated circuits needed for the communication system, one important design decision is which type of packaging the device is encapsulated in. In a system subjected to mechanical shocks and thermal variations, packages with pins, such as Quad Flat Package (QFP) and Small-Outline Integrated Circuit (SOIC), generally have better reliability than packages with solder balls, such as Ball Grid Array (BGA) [67]. The suggested small FPGA for the custom high-speed UART optical alternative in section 6.1.2, Lattice MachXO3, only comes in a small BGA package. The packaging of that FPGA is a disadvantage for that alternative.

One alternative to BGA packaging is Column Grid Array (CGA), where the balls are replaced by taller columns of solder and copper. These taller columns provide better strain relief for the package. CGA is generally used in high-reliability applications, such as the space industry, and are not generally available with electronic component distributors. CGA packages require the same fine-pitch PCB manufacturing process as BGA packages, and CGAs are more expensive since they are not produced in high volumes.

10.1.2 System communication

For system communication, it is clear from the comparison in section 6.2 that all considered alternatives, except possibly for CAN FD, cost several times that of

the currently implemented CAN system. Due to cost being such an important factor, a general switch from CAN to another system for all communication links is most likely not preferred. Instead, links that require higher speeds should be identified and specific alternatives for each link evaluated. In this way, only certain parts of the system need to carry the additional cost associated with the link alternative, such as the differentiation between real-time-regulation-loop communication and other system communication described earlier.

Having multiple different link alternatives, however, introduces more complexity in the system. Therefore the impact of software complexity has to be accounted for in a link alternative decision. For high-end products with higher performance requirements, a faster, but more expensive, system bus alternative could be considered to reduce complexity, but at a higher cost.

Any communication link alternative needs to fulfill the isolation requirements set by the weld system standard. This implies extra cost for each communication link, depending on the isolation level. For example, using optical cabling provides a very high level of isolation, whereas copper cabling requires isolation at each end of the communication link. Such bus isolators can take the form of isolation transformers, capacitive bus isolators, or optical bus isolators. In a weld system with high levels of EMI, especially magnetic fields from the power supply transformers, isolation transformers might exhibit high levels of EMS compared to capacitive and optical bus isolators. The evaluations performed on Ethernet indicates that the relatively small isolation transformer used did not impose a problem. A larger transformer, which is needed to fulfill the isolation requirements for certain links, however might pick up more EMI due to the larger transformer core. Optical links and isolators are, on the other hand, immune to EMI in the optical sections, but can be subjected to interference in the electrical parts, just like any other electronic component.

When selecting a system communication alternative, one important aspect is what level of interoperability is needed. In this report, only links between proprietary system components are considered. Therefore, a specific fieldbus protocol, such as EtherCAT or PROFINET, is not as important as if interoperability with third party components was to be considered. More flexibility can therefore be applied in combining physical signaling systems with communication protocols. Since the current system communicates using an implementation of the CANOpen protocol, a communication system which can utilize this protocol would require less development effort than a system utilizing a completely new protocol.

When considering communication link cabling, the evaluations performed indicate that, for copper cabling, differential signaling over twisted pair is needed. This is supported by the observations that, during the Ethernet evaluation tests, UART serial channels were affected by interference, whereas the Ethernet communication was not. The indicated interference on those UART channels might be explained by conducted CM noise through the ground loop generated by the connection from one test PCB, through the laptop, to the other test PCB.

To reduce EMI on the communication cables, shielded cables can be used. Such cables are more expensive than unshielded cables, and the evaluations performed indicate that for the tested conditions, the shield does neither improve nor degrade the communication performance.

When considering a system communication bus, the bus topology is an important aspect. For traditional communication bus systems, such as CAN and

FlexRay, all nodes are electrically connected together. This type of setup is cheap in terms of hardware since only one bus interface is needed on each node. These types of connections do, however, require careful design of bus topology and the related impedance matching terminations. In many cases these termination circuits is simply a resistor between the differential signal data lines, however for a network with several nodes having such resistors on all connections presents a too high load for the bus driver circuits.

Another aspect regarding traditional bus connections is relation between total wire length and maximum bus speed. This is especially important with the CAN, where message priority and arbitration takes place at the bit level. Because of this the signal needs to travel from a node to another and back within approximately 20 % of one bit time. Since there is a need of bus isolator circuits, which introduce further delays, the maximum bus length becomes a limiting factor for higher speeds. With a propagation delay of the isolator circuit of 50 ns, an assumed propagation velocity of the cabling of 5 ns/m, and a bus speed of 1 Mbit/s, the maximum bus length becomes

$$L_{max} = \frac{\frac{1\,\text{bit}}{1\,\text{Mbit/s}} \cdot 0.2 - 2 \cdot 50\,\text{ns}}{5\,\text{ns/m} \cdot 2} = 10\,\text{m}$$

which is too short for an external link between the power source and a remote wire feeder.

This calculation does, however, only affect the arbitration phase of the CAN communication. After the arbitration phase, any down-prioritized node backs off and retries communication at a later time. The CAN FD protocol can therefore use higher speeds after the arbitration, as long as reflections in bus stubs do not interfere with signal integrity.

Time-triggered bus communication systems, such as FlexRay, overcome this length limitation due to the need of bit synchronization. However, introduced logic for clock synchronization among nodes, combined with the safety requirements of the intended target systems of such communication solutions, results in expensive components.

Point-to-point link communication systems, such as Ethernet, integrate impedence matching circuitry for both ends of a communication link. Such systems are therefore easier to connect together in various topologies with respect to impedence matching. On the other hand, point-to-point link systems require dual connection ports for each node, or a central bus switch, adding to the overall system cost.

10.2 Software

This section will cover the system software and the communication protocol implementation.

10.2.1 Software implementation

After considering the time it takes to receive a frame with finding the start of frame and performing checksum calculations, adding the checksum calculations of sending one frame, the total protocol handling time adds up to 11.2 µs. Adding the weld regulation processing time of 10 µs gives a total of approximately 21 µs. This time is significantly less than the total measured processing

time of 34 µs. Most of this time was explained by analyzing the software, finding that during reception of a frame, it was copied in full several times before finally being used.

Instead of performing full copy operations, statically declared receive and transmit buffers could be utilized. Passing data between software libraries is then performed by passing pointers to the buffers instead, a scheme sometimes called zero copy. This scheme requires locking or ownership indication for the memory buffers to avoid memory access races.

The target MCU DMA blocks have the ability of performing double buffering in hardware [6]. This means that the DMA can be configured with pointers to two memory buffers, automatically switching between them when a transfer completes. This feature can be used to offload the software handling even more on links with high utilization.

10.2.2 Communication protocol

The timing measurements performed on the existing regulation loop implementation make it clear that protocol handling operations need to be optimized unless a more powerful and more expensive MCU is to be utilized. Since the regulation loop is carried on an internal link between completely proprietary components, the protocol can be adapted to the existing hardware instead of being generic. Padding can be inserted for the 16 bit data types in the protocol to align them on appropriate memory boundaries, or reordering of the fields can be performed, with memory boundaries in mind. Endianness for 16 bit data types can also be adjusted from network byte ordering, big endian, to the little endian used in the MCU by default. These optimizations minimize memory reordering operations, enabling direct use of protocol data from the receive memory buffer.

For general system communication, the protocol used does not impact system performance to the same degree as the high-frequency regulation loop due to a lower frequency of messages. Communication also takes place among multiple nodes, possibly with different system setups and performance. There is, therefore, a stronger requirement regarding communication stack portability than high performance. However, all nodes on the communication bus are still proprietary and well defined, minimizing the need to be fully standards compliant.

Another aspect affecting the system communication protocol is functional safety. To enable safety features, such as emergency stop, over the communication bus, a high level of functional safety is required. For a fully certified emergency stop functionality, safety standards such as IEC 61508 and IEC 61784-3 must be followed. There exist communication stacks with safety certifications, such as the openSAFETY [68] protocol, which can be implemented over any existing communication bus mixed with non-safety communications.

11 Project evaluation

This project started out with ambitious goals of investigating three different types of communication for use in a weld system: traditional wired, wired over weld cable, and wireless. The existing software and hardware was profiled and analyzed to identify bottlenecks and areas of improvement. An extensive study of the possible alternatives for high-speed real-time communication, as well as system communication, was performed. In parallel, a literature study regarding EMI and weld cable communication was performed. During this study, a patent was identified within the field of weld cable communication. An in-depth study of this patent was performed, to understand exactly what was protected by the patent.

A prioritization was made to focus on the alternatives in the order of regulation loop communication, system communication, wireless communication, and finally weld cable communication. A thorough study of alternatives for regulation loop communication and system communication was performed. Alternatives for wireless and weld cable communications, however, were only briefly investigated due to lack of time.

For lab measurements, an already available evaluation prototype board with Ethernet hardware could be utilized. Software for this board was implemented, and the setup was tested in a weld lab. The tests were performed to evaluate Ethernet communication with regards to the EMI levels in the system. During these lab measurements, only bit errors were measured. Voltages on the Ethernet wires were not measured, mainly because no actual communication error was triggered.

Overall, the project was considered valuable input by ESAB. The project will provide a basis for decisions regarding future communication alternatives.

12 Conclusion

This section will present conclusions based on the presentation and discussion in the previous sections.

12.1 Hardware

The choice of communication physical medium affects aspects such as EMS, galvanic isolation, and cost. With copper cabling, issues with galvanic isolation and EMI requires handling in the form of large isolation components and signal filtering. Optical cables, on the other hand, are immune to EMI and provide high levels of galvanic isolation, however optical solutions are generally more expensive than copper-based alternatives.

If copper cabling is to be used, differential signaling over twisted pair is the only viable alternative. Shielding might, however, be optional at least for the conditions tested. If shielding is to be used for connections between galvanically isolated regions, issues with ground loops and current return paths need to be handled.

The tests performed during this project indicated that Ethernet over copper cabling can be used for communication within the target weld system. Common mode chokes, however, are in the literature considered important for differential signaling systems to filter out common mode EMI.

For communication links with speeds higher than approximately 15 Mbd, simple oversampling receivers such as the UART either become sensitive to minor clock drift due to low oversampling, or need to run with a relatively high system clock with the need of more expensive hardware. This limitation makes the need for a more sophisticated line encoding, such as the one provided by the Ethernet standard, necessary for asynchronous communication. Therefore, the simple UART is not sufficient for the high-speed real-time communication link depicted in this project.

Synchronous serial communication with an explicit clock line, such as an SPI bus, was shown to be able to run at a rate high enough for the high-speed real-time communication link. This results in one extra wire needed, however the use of inexpensive plastic optic fiber components makes this alternative a viable option.

When considering general system communication, it was demonstrated that a faster communication system than the CAN bus, such as Flexray or standard Ethernet, resulted in a system several times more expensive than the current. The relatively new CAN FD and One-Pair EtherNet systems provide an interesting alternative for higher communication speeds. In the case of One-Pair EtherNet, the bus is electrically simplified with the use of point-to-point links.

12.2 Software

In a performance-constrained real-time system, it is important to account for processing overhead for communication protocols. Such processing overhead is especially important for links communicating data with high frequency, such as the regulation loop running at 20 kHz in the described system. The buffer handling, implemented with copy operations between operating system libraries,

proved too time consuming when increasing regulation loop frequency. Therefore, the concept of zero-copy for input and output message buffers was evaluated in the demonstration setups. The results from these tests show that the software is able to handle the target regulation loop frequency, given the optimizations proposed in this report.

For links with less strict real-time requirements, and with lower message rates, the same amount of optimizations are not needed. Communication among diverse system components instead has higher requirements regarding software portability and system interoperability. Therefore, handling of communication links with different requirements on speed and latency can be handled with different optimization strategies.

One important aspect for low-power embedded systems is to properly utilize the available hardware resources. Such resources include specialized hardware blocks, for example DMAs and CRC calculation.

12.3 Communication protocol

It was demonstrated that the dynamic components of the implemented communication protocol generated too much overhead when increasing the regulation loop frequency. For high-speed and high-frequency communication links, processing overhead of the communication protocol must therefore be optimized. If communication takes place among proprietary units, the protocol can be adapted for minimal processing overhead. Such optimizations include the use of static message frame lengths and static message data positions.

The described regulation loop communication link has an optimal message size of 16 B to properly utilize the DMA block in the MCU, for UART or SPI data paths. For Ethernet, the minimum frame length of 72 B can be used. Little endian for data fields in this protocol minimizes the need of data type processing in the MCU.

For links with lower real-time requirements, a more general communication protocol can be advantageous. A standardized protocol often provides available software stacks, which can provide message profiles and message generation for easier integration in an embedded system. With a standard protocol, interoperability among different units is also simplified.

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A Optical bias circuit calculations

This appendix contains calculations for component values in biasing circuits for Industrial Fiberoptics IF-E91D transmitter and IF-D91 receiver diodes. The reference circuits are shown in Figure 7.2a (transmitter) and Figure 7.2b (receiver).

The transmitting diode has a typical forward voltage drop $V_f = 1.38\,\mathrm{V}$. The target forward on current is $I_f = 20\,\mathrm{mA}$, and the target forward off maximum voltage is $V_{f_{off},max} = 1\,\mathrm{V}$. DC analysis of the transmitter circuit gives two corner cases, $V_{in} = V_{dd}$ and $V_{in} = V_{ss}$.

For $V_{in} = V_{dd}$ one arrives at the following:

$$V_{R_b} = V_{dd} - V_f = V_{R_{in}} \tag{A.1}$$

$$I_{R_b} = \frac{V_{R_b}}{R_b} \tag{A.2}$$

$$I_{in} = \frac{V_{R_{in}}}{R_{in}} \tag{A.3}$$

$$I_f = I_{R_b} + I_{in} = (V_{dd} - V_f)\left(\frac{1}{R_b} + \frac{1}{R_{in}}\right) \tag{A.4}$$

For $V_{in} = V_{ss}$ one arrives at the following:

$$I_f \approx 0\,\mathrm{mA} \tag{A.5}$$

$$V_f = V_{R_{in}} \tag{A.6}$$

$$R_{in,max} = \frac{R_b V_{f_{off},max}}{V_{dd} - V_{f_{off},max}} \tag{A.7}$$

Combining (A.4) and (A.7) gives:

$$R_b = \frac{(V_{dd} - V_f)\,V_{dd}}{I_f V_{f_{off},max}} \tag{A.8}$$

Which, given the constraints above, yields the following values:

$$R_b = 396\,\Omega \approx 470\,\Omega \tag{A.9}$$

$$R_{in,max} = 126\,\Omega \approx 120\,\Omega \tag{A.10}$$

The chosen values, selected from the E12 standard table, are shown as approximated values.

B Regulation loop alternatives BOM

The following table presents the bill of material for regulation loop alternatives. Component details can be found in Appendix D.

Alternative/component	QTY	price ($)	sum	total cost	relative total cost
Avago Versatile Link UART					
AFBR-1624Z	2	9.410	18.820		
AFBR-2624Z	2	10.730	21.460		
Optical Fiber HFBR-RLS001Z simplex Versatile Link connector 1m	2	3.130	6.260		
				46.54	1.00
Photodiode amplifier/comparator					
LT6268 OpAmp	1	4.190	4.190		
LT6752 Comparator	1	2.340	2.340		
Opamp discretes (3 resistors, 1 capacitor)	1	0.019	0.019		
Comparator discretes (2 resistors, 1 capacitor)	1	0.016	0.016		
				6.57	
Avago screw latch UART					
Optical transmitter Avago SFH757V (bare cable connection)	2	6.490	12.980		
Optical receiver Avago SFH250V (bare cable connection)	2	5.770	11.540		
Optical Fiber (only cable) Eska SH4001	2	0.560	1.120		
Transmitter bias 1 resistors	2	0.003	0.006		
Receiver amplifier	2	6.565	13.130		
				38.78	0.83
Industrial Fiberoptics screw latch UART					
Optical transmitter IF-E91D	2	2.730	5.460		
Optical receiver IF-D91	2	2.170	4.340		
Optical Fiber (only cable) Eska SH4001	2	0.560	1.120		
Transmitter bias and decoupling circuit, 2 resistors, 2 capacitors	2	0.216	0.432		
Receiver amplifier	2	6.565	13.130		
				24.48	0.53
External FPGA UART accelerator					
Optical transmitter IF-E91D	2	2.730	5.460		
Optical receiver IF-D91	2	2.170	4.340		
Optical Fiber (only cable) Eska SH4001	2	0.560	1.120		

Alternative/component	QTY	price ($)	sum	total cost	relative total cost
Transmitter bias and decoupling circuit, 2 resistors, 2 capacitors	2	0.216	0.432		
FPGA XO3L-1300	1	2.210	2.210		
Receiver amplifier	2	6.565	13.130		
				26.69	0.57
SERDES 10 b channel, copper with transformer					
Serializer TI SN65LV1023ADB	2	4.320	8.640		
Deserializer TI SN65LV1224BDB	2	4.100	8.200		
Ethernet Transformer 4500 Vrms	2	5.200	10.400		
CAT5e shielded, braded cable	1	3.330	3.330		
CM Choke	4	0.770	3.080		
Terminations 3x 100 nF X7R, 4x resistors	2	0.042	0.084		
CONN HEADER 4POS DUAL TIN SMD TE/AMP 3-794636-4	2	0.945	1.890		
CONN RCPT 3MM 4POS DL MATE-N-L TE/AMP 794617-4	2	0.215	0.430		
CONN SOCKET 20-24AWG TIN CRIMP TE/AMP 794606-1	8	0.026	0.208		
				36.26	0.78
SERDES 10b channel, optical Avago "RJ45"					
Serializer TI SN65LV1023ADB	2	4.320	8.640		
Deserializer TI SN65LV1224BDB	2	4.100	8.200		
Optical transceiver AFBR-5972Z	2	21.310	42.620		
Filter and termination, 7x 100 nF X7R, 2x 10 uF tantalelyt, 2x 1 uH ferrite, 5x resistors	2	0.685	1.370		
Optical Fiber (only cable) Eska SH4001	2	0.560	1.120		
Optical fiber cable connector duplex for AFBR-5972Z	2	0.750	1.500		
				63.45	1.36
Avago screw latch SPI					
Optical transmitter Avago SFH757V (bare cable connection)	3	6.490	19.470		
Optical receiver Avago SFH250V (bare cable connection)	3	5.770	17.310		
Optical Fiber (only cable) Eska SH4001	3	0.560	1.680		
Transmitter bias 1 resistors	3	0.003	0.009		
Receiver amplifier	3	6.565	19.695		
				58.16	1.25
Industrial Fiberoptics screw latch SPI					
Optical transmitter IF-E91D	3	2.730	8.190		
Optical receiver IF-D91	3	2.170	6.510		

Alternative/component	QTY	price ($)	sum	total cost	relative total cost
Optical Fiber (only cable) Eska SH4001	3	0.560	1.680		
Transmitter bias and decoupling circuit, 2 resistors, 2 capacitors	3	0.216	0.648		
Receiver amplifier	3	6.565	19.695		
				36.72	0.79
Avago screw latch alternating SPI					
Optical transmitter Avago SFH757V (bare cable connection)	2	6.490	12.980		
Optical receiver Avago SFH250V (bare cable connection)	2	5.770	11.540		
Optical Fiber (only cable) Eska SH4001	2	0.560	1.120		
Transmitter bias 1 resistors	2	0.003	0.006		
2:1 MUX SN74LVC2G157DCTR	1	0.150	0.150		
1:2 DEMUX SN74LVC1G18DCKR	1	0.080	0.080		
Receiver amplifier	2	6.565	13.130		
				39.01	0.84
Industrial Fiberoptics screw latch alternating SPI					
Optical transmitter IF-E91D	2	2.730	5.460		
Optical receiver IF-D91	2	2.170	4.340		
Optical Fiber (only cable) Eska SH4001	2	0.560	1.120		
Transmitter bias and decoupling circuit, 2 resistors, 2 capacitors	2	0.216	0.432		
2:1 MUX SN74LVC2G157DCTR	1	0.150	0.150		
1:2 DEMUX SN74LVC1G18DCKR	1	0.080	0.080		
Receiver amplifier	2	6.565	13.130		
				24.71	0.53
Fast Ethernet copper					
Ethernet PHY KSZ8081RNAIA	2	0.530	1.060		
RJ45 jack with LEDs	2	2.280	4.560		
Ethernet MAC IP core	1	1.090	1.090		
Bigger FPGA	1	4.870	4.870		
CM Choke	4	0.770	3.080		
Terminations 3x 100 nF X7R, 4x resistors	2	0.042	0.084		
Ethernet Transformer 4500 Vrms	2	5.200	10.400		
RJ45 shielded plug with latch	2	2.380	4.760		
CAT5e shielded, braded cable	1	3.330	3.330		
				33.23	0.71

Alternative/component	QTY	price ($)	sum	total cost	relative total cost
Fast ethernet POF Avago "RJ45"					
Ethernet PHY KSZ8041FTLI	2	2.210	4.420		
Optical transceiver AFBR-5972Z	2	21.310	42.620		
Optical fiber cable connector duplex for AFBR-5972Z	2	0.750	1.500		
Optical Fiber (only cable) Eska SH4001	2	0.560	1.120		
Filter and termination, 7x 100 nF X7R, 2x 10 uF tantalelyt, 2x 1 uH ferrite, 5x resistors	2	0.685	1.370		
Ethernet MAC IP core	1	1.090	1.090		
Bigger FPGA	1	4.870	4.870		
				56.99	1.22

C System communication alternatives BOM

The following table presents the bill of material for system communication alternatives. Component details can be found in Appendix D.

Alternative/component	QTY	price ($)	sum	total cost	relative total cost
Traditional CAN					
CAN Transceiver Ti SN65HVD1040	1	0.710	0.710		
Bus isolator TiISO7221A	1	1.170	1.170		
Connector header	1	0.945	0.945		
Termination (2 resistors)	1	0.006	0.006		
Common mode choke	1	1.850	1.850		
				4.68	1.00
CAN FD					
CAN FD Transceiver Microchip MCP2561/2FD	1	0.680	0.680		
Bus isolator TiISO7221A	1	1.170	1.170		
Connector header	1	0.945	0.945		
Termination (2 resistors)	1	0.006	0.006		
Common mode choke	1	1.850	1.850		
CAN FD controller (estimation)	1	2.000	2.000		
				6.65	1.42
Flexray					
FlexRay bus driver NXP TJA1081	1	1.760	1.760		
Common mode choke for FlexRay	1	1.010	1.010		
Bus isolator TiISO7221A (0-150 Mbps, 2.5 kVrms)	1	1.170	1.170		
Bus termination (2 resistors)	1	0.006	0.006		
Flexray MCU TMS570LS3137 (upgrade cost)	1	11.150	11.150		
				15.10	3.22
EtherCAT Master					
Ethernet PHY KSZ8081RNAIA	2	0.530	1.060		
RJ45 jack with LEDs	2	2.280	4.560		
CM Choke	2	0.770	1.540		
Terminations 3x 100 nF X7R, 4x resistors	1	0.042	0.042		
Ethernet transformer 1500 Vrms	1	3.480	3.480		
RJ45 shielded plug with latch	2	2.380	4.760		

Alternative/component	QTY	price ($)	sum	total cost	relative total cost
CAT5e shielded, braded cable	1	3.330	3.330		
Master stack	1				
				18.77	4.01
EtherCAT Slave					
Ethernet PHY KSZ8081RNAIA	1	0.530	0.530		
RJ45 jack with LEDs	1	2.280	2.280		
CM Choke	2	0.770	1.540		
Terminations 3x 100 nF X7R, 4x resistors	1	0.042	0.042		
Ethernet transformer 1500 Vrms	1	3.480	3.480		
RJ45 shielded plug with latch	2	2.380	4.760		
CAT5e shielded, braded cable	1	3.330	3.330		
EtherCAT slave controller Microchip LAN9252	1	8.180	8.180		
				24.14	5.16
Custom Ethernet master					
RJ45 jack with LEDs	1	2.280	2.280		
CM Choke	2	0.770	1.540		
Terminations 3x 100 nF X7R, 4x resistors	1	0.042	0.042		
Ethernet transformer 1500 Vrms	1	3.480	3.480		
RJ45 shielded plug with latch	1	2.380	2.380		
CAT5e shielded, braded cable	1	3.330	3.330		
Ethernet PHY KSZ8081RNAIA	1	0.530	0.530		
				13.58	2.90
Custom Ethernet slave					
RJ45 jack with LEDs	2	2.280	4.560		
CM Choke	4	0.770	3.080		
Terminations 3x 100 nF X7R, 4x resistors	2	0.042	0.084		
Ethernet transformer 1500 Vrms	2	3.480	6.960		
RJ45 shielded plug with latch	2	2.380	4.760		
CAT5e shielded, braded cable	2	3.330	6.660		
Micrel KSZ8852HLEWA 2-port Ethernet switch + host interface	1	8.070	8.070		
				34.17	7.30
BroadR-Reach master					
BroadR-Reach PHY (estimation)	1	0.000	0.000		

Alternative/component	QTY	price ($)	sum	total cost	relative total cost
Isolation capacitors (1.5 kV 0.1uF)	2	0.834	1.668		
Connector header	1	0.945	0.945		
Termination (2 resistors)	1	0.006	0.006		
CM Choke	1	0.770	0.770		
				3.39	0.72
BroadR-Reach slave					
BroadR-Reach PHY (estimation)	2	0.000	0.000		
Isolation capacitors (1.5 kV 0.1uF)	4	0.834	3.336		
Connector header	2	0.945	1.890		
Termination (2 resistors)	2	0.006	0.012		
CM Choke	2	0.770	1.540		
Micrel KSZ8852HLEWA 2-port Ethernet switch + host interface	1	8.070	8.070		
				14.85	3.17

D Component cost

The following table presents components and their associated list pricing.

Component	Supplier	Part number	Quantity	Cost ($)
MCU ST Microelectronics STM32F427ZI	Farnell	2333371	500+	9.330
MCU Texas Instruments TMS5703137	Digikey	296-41906-ND	1000+	23.710
RXoptics AFBR-1624Z	Farnell	2213640	5000+	9.410
TXoptics AFBR-2624Z	Farnell	2213642	5000+	10.730
Optical Fiber HFBR-RLS001Z simplex Versatile Link connector 1m	Farnell	1247699	1000+	3.130
FPGA LFXP2-5E-5TN144C	Farnell	1571999	1000+	10.190
FPGA LFXP2-8E-5TN144C	Farnell	1571999	1000+	15.060
FPGA XO3L-1300	Farnell	2460486	25+	2.210
2:1 MUX SN74LVC2G157DCTR	Farnell	2437225	30000+	0.150
1:2 DEMUX SN74LVC1G18DCKR	Farnell	2437159	30000+	0.080
Serializer TI SN65LV1023ADB	Farnell	8452296	3000+	4.320
Deserializer TI SN65LV1224BDB	Farnell	2075438	1500+	4.100
Optical transceiver AFBR-5972Z integrated connector POF (RJ45)	Farnell	2070243	600+	21.310
Optical fiber cable connector AFBR-4526Z (for AFBR-5972Z)	Farnell	2070245	4000+	0.750
Optical transceiver AFBR-5978Z SC connector POF	Farnell	1327489	200+	51.590
Optical transmitter IF-E91D Industrial Fiberoptics 100 Mb/s	DigiKey	FB134-ND	2500+	2.730
Optical receiver IF-D91 Industrial Fiberoptics 100 Mb/s	DigiKey	FB120-ND	2500+	2.170
Ethernet opto transceiver ST connector AFBR-5803TZ MM	Farnell	9450068	600+	19.220
Ethernet transformer 4500 Vrms WE 749014010	Farnell	1961666	600+	5.200
Common mode choke Ethernet WE 744230251	Farnell	1848964	1000+	0.770
Ethernet PHY KSZ8081RNAIA	Farnell	2345483	7000+	0.530
RJ45 jack with LEDs (AMP 6339191-1)	Farnell	2131151	4000+	2.280
RJ45 shielded plug with latch protector (HRS TM21P-88P)	Farnell	4127640	1000 +	2.380
CAT5e shielded, braded cable 4xtwisted pair 152 m / roll ALPHA WIRE 76021 BK002, Equivalent price per meter	Farnell	2131376	500+	3.330
Ethernet PHY KSZ8041FTLI	Farnell	2100383	5000+	2.210
Optical fiber cable ST duplex	Farnell	1300221	50+	6.400
Ethernet MAC/PHY controller MICROCHIP ENC424J600-I/PT	Farnell	1740226	100+	2.930
Ethernet MAC IP core Lattice TS-MAC-X2-U4, Single design license, cost/1000 units	DigiKey	TS-MAC-X2-U4-ND	1+	1093.000

Component	Supplier	Part number	Quantity	Cost ($)
Ethernet MAC IP core Lattice TS-MAC-X2-U4, unit cost at 1000 units				1.090
CAN transceiver Ti SN65HVD1040	Farnell	2335646	9000+	0.710
CAN FD transceiver Microchip MCP2561/2FD 8megabit/second	Farnell	2434896	100+	0.680
Bus isolator TiISO7221A (0-150 Mbps, 2.5 kVrms)	Farnell	1390651	900+	1.170
Bus isolator ADuM1201ARZ (0-25 Mbps, 2.5 kVrms)	Farnell	1078200	8000+	1.320
WE CM filter 744 227	Farnell	1636267	1000+	1.850
FlexRay bus driver NXP TJA1081	DigiKey	568-8753-2-ND	2000+	1.760
FlexRay bus driver ON Semiconductor NCV7383DB0R2G	Farnell	2424529	500+	1.830
Common mode choke for FlexRay Bourns DR331-474BE 470 µH	Farnell	2371283	7500+	1.010
FlexRay CC Infineon CIC310				
FlexRay CC Freescale MFR4310				
FlexRay CC IPextreme FRCC2100 (Verilog IP)				
Ethernet transformer 1500 Vrms EPCOS B78476A8247A003	Farnell	1644276	250+	3.480
EtherCAT slave controller Microchip LAN9252	Microchip	LAN9252TI/PT	5000+	8.180
RJ45 panel jack feedthrough AMPHENOL PCD RJF 544 2M1	Farnell	1462776	1+	34.360
RJ45 plug push/pull locking AMPHENOL PCD RJF5446	Farnell	1339818	100+	12.330
IEEE802.15.4 transceiver Atmel AT86RF231				
Optical fiber cable POF 1.0mmx1 / 2.2mm Eska SH4001 @2km, 500m/spool, price / m	Industrial Fiberoptics		4+	0.560
Resistor SMD 0603, 0805 (approx)				0.003
Capacitor ceramic 0603, 0805 0.1uF (approx)				0.010
Capacitor tantal elyt 0805, 1210 10 uF (approx)				0.200
Ferrite 1 uH, > 250 MHz resonanse frequency 0805 (approx)				0.100
Optical transmitter Avago SFH757V (bare cable connection)	DigiKey	516-2872-ND	5000+	6.490
Optical receiver Avago SFH250V (bare cable connection)	DigiKey	516-2283-ND	5000+	5.770
Comparator LM239DR (SOIC-8, cut tape)	DigiKey	296-14590-2-ND	1+	0.420
CONN HEADER 4POS DUAL TIN SMD TE/AMP 3-794636-4	DigiKey	A33236TR-ND	875+	0.945
CONN RCPT 3MM 4POS DL MATE-N-L TE/AMP 794617-4	DigiKey	A30294-ND	5000+	0.215
CONN SOCKET 20-24AWG TIN CRIMP TE/AMP 794606-1	DigiKey	A30305TR-ND	30000+	0.026
Linear Technology OpAmp LT6268	Farnell	2464182	100+	4.190
Linear Technology Comparator LT6752	Farnell	2471130	100+	2.340
Texas Instruments MCU with Flexray	Texas Instruments	TMS570LS3137 CPGEQQ1	1000+	20.480
Micrel KSZ8852HLEWA 2-port Ethernet switch + host interface	DigiKey	576-4846-ND	5000+	8.070
Kemet C2225C104KFRACTU 0.1uF ±10% 1.5kV X7R SMD2225	DigiKey	399-10501-2-ND	5000+	0.834

Component	Supplier	Part number	Quantity	Cost ($)
Avago AFBR-59F1Z Fast Ethernet POF transceiver, bare fiber clamp	Mouser	630-AFBR59F1Z	500+	16.054

Table D.1: Component cost