THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Characterization of Nanomaterials for Interconnect and Thermal Management in Electronic Packaging

Si Chen

Department of Microtechnology and Nanoscience (MC2)

BioNano Systems Laboratory

CHALMERS UNIVERSITY OF TECHNOLOGY

Göteborg, Sweden 2015

Characterization of Nanomaterials for Interconnect and Thermal Management in Electronic Packaging

Si Chen

ISBN: 978-91-7597-204-6

Doktorsavhandlingar vid Chalmers tekniska högskola

Ny serie nr 3885

ISSN 0346-718X

Technical Report MC2-310

ISSN 1652-0769

CHALMERS UNIVERSITY OF TECHNOLOGY

Department of Microtechnology and Nanoscience - MC2

BioNano Systems Laboratory

SE-412 96 Göteborg Sweden

Telephone +46 (0) 31-772 1000

Printed by Chalmers Reproservice

Göteborg, Sweden 2015

Abstract

Electronic packaging, protecting the fragile chip from atmosphere and providing the paths for signal transmission as well as heat dissipation, is one of the most important parts in electronic devices. The cost, dimensions, performance, and reliability of an electronic device therefore strongly depend on its packaging structures and materials. In recent years, the miniaturization and diversification of electrical devices, having increased packaging and power density, pose a serious challenge to the reliability of traditional packaging materials. To address this challenge, several nanomaterials were thus fabricated and used for either interconnection or heat dissipation in the electronic packaging.

For interconnection, vertically aligned carbon nanotubes (VACNT) grown with thermal chemical vapor deposition (TCVD) method were used as filling materials of through silicon vias (TSV). Meanwhile, vertically aligned carbon nanofibers (VACNF) fabricated with plasma enhanced chemical vapor deposition (PECVD) method were used as not only the bump material for chips, but also for the reinforcement material for solder joints. By using these carbon nanomaterials, some failure modes, such as burnout, electromigration, and coarseness, can be avoided. Besides carbon, alloy and semiconductor nanomaterials were also fabricated in this thesis for interconnection. Sn3.0Ag0.5Cu (SAC305) alloy and Bi_2Te_3 semiconductor nanopowders were mixed with traditional Sn58Bi and SAC305 lead free solders respectively in order to improve the shear strength and thermal fatigue resistance of solder joints. The dislocation movement and crack propagation can be effectively delayed by uniformly distributed nanoparticles in the solder matrix. However, it always shows a performance degradation when the content of nanoparticles passes a threshold. This phenomenon could be caused by increased voids and the agglomeration of nanoparticles in the solder matrix with increased content of nanoparticles.

For heat dissipation, a polyimide (PI) network enhanced indium thermal interface material (TIM) was developed as a passive heat dissipation solution, and meanwhile a nanostructured bulk thermoelectric (TE) material constructed of Ag and Bi_2Te_3 nanopowders is presented as an active heat dissipation solution. The mechanical properties of pure indium TIM can be improved by the PI network without any degradation of heat dissipation ability. This is attributed to the Ag-coated PI fibers which formed solid bonding with the indium matrix and constrained the crack propagation. For the TE material, the thermal conductivity of nanostructured Bi_2Te_3 samples was much lower than that of raw materials due to the increased phonon scattering at the grain boundaries, which consequently led to a higher figure of merit (ZT value).

Keywords: electronic packaging, nanomaterial, characterization, interconnect, heat dissipation, through silicon via, solder, thermal interface material, thermoelectric.

List of Publications

The thesis is based on the following papers:

Paper A: Through-silicon vias filled with densified and transferred carbon nanotube bundles

T. Wang, **S. Chen**, D. Jiang, Y. Fu, K. Jeppson, L. Ye, and J. Liu

IEEE Electron Device Letters, vol. 33, no. 3, pp. 420–422, 2012.

Paper B: Ultra-short vertically aligned carbon nanofibers transfer and application as bonding material

S. Chen, D. Jiang, C. Zandén, Z. Hu, Y. Fu, Y. Zhang, L. Ye, and J. Liu

Soldering & Surface Mount Technology, vol. 25, no. 4, pp. 242–250, Sep. 2013.

Paper C: A solder joint structure with vertically aligned carbon nanofibres as reinforcements

S. Chen, D. Jiang, L. Ye, and J. Liu

Electronics System-Integration Technology Conference (ESTC), 2014, 2014, pp. 1–6.

Paper D: A reliability study of nanoparticles reinforced composite lead-free solder

S. Chen, L. Zhang, J. Liu, Y. Gao, and Q. Zhai

MATERIALS TRANSACTIONS, vol. 51, no. 10, pp. 1720–1726, 2010.

Paper E: Sn-3.0Ag-0.5Cu nanocomposite solder reinforced with Bi_2Te_3 nanoparticles

S. Chen, X. Luo, D. Jiang, L. Ye, M. Edwards, and J. Liu

Accepted by the journal of IEEE Transactions on Components, Packaging and Manufacturing Technology.

Paper F: Characterization of mechanical and thermal performance of a novel nanocomposite thermal interface material for electronic packaging

S. X. Sun, **S. Chen**, C. Zandén, X. Luo, L. Ye, and J. Liu

Submitted.

Paper G: A high performance Ag alloyed nano-scale n-type Bi_2Te_3 based thermoelectric material

S. Chen, N. Logothetis, L. Ye, and J. Liu

Accepted by Materials Today: Proceedings.

Other journal and conference papers not included due to being out of the scope of this thesis:

Coffin-Manson equation of Sn-4.0Ag-0.5Cu solder joint

S. Chen, P. Sun, X. C. Wei, Z. N. Cheng, and J. Liu

Solder. Surf. Mt. Technol., vol. 21, no. 2, pp. 48–54, Apr. 2009.

Development and characterization of nano-composite solder

J. Liu, **S. Chen**, and L. Ye

Lead-Free Solders: Materials Reliability for Electronics, K. N. Subramanian, Ed. John Wiley & Sons, Ltd, 2012, pp. 161–177.

Selective growth of double-walled carbon nanotubes on gold films

Y. Fu, **S. Chen**, J. Bielecki, A. Matic, T. Wang, L. Ye, and J. Liu

Mater. Lett., vol. 72, pp. 78–80, 2012.

Formation of three-dimensional carbon nanotube structures by controllable vapor densification

T. Wang, D. Jiang, **S. Chen**, K. Jeppson, L. Ye, and J. Liu

Mater. Lett., vol. 78, pp. 184–187, 2012.

Paper-mediated controlled densification and low temperature transfer of carbon nanotube bundles for electronic interconnect application

D. Jiang, T. Wang, **S. Chen**, L. Ye, and J. Liu

Microelectron. Eng., vol. 103, pp. 177–180, 2013.

A highly conductive bimodal isotropic conductive adhesive and its reliability

D. Li, H. Cui, **S. Chen**, Q. Fan, Z. Yuan, L. Ye, and J. Liu

Ecs Trans., vol. 34, no. 1, pp. 583–588, Mar. 2011.

Study on the reliability of fast curing isotropic conductive adhesive

W. Du, H. Cui, **S. Chen**, Z. Yuan, L. Ye, and J. Liu

Ecs Trans., vol. 34, no. 1, pp. 805–810, Mar. 2011.

Ultrafast transfer of metal-enhanced carbon nanotubes at low temperature for large-scale electronics assembly

Y. Fu, Y. Qin, T. Wang, **S. Chen**, and J. Liu

Adv. Mater., vol. 22, no. 44, pp. 5039–5042, 2010.

Flip chip assembly using carbon nanotube bumps and anisotropic conductive adhesive film

X. Zhang, T. Wang, P. Berggren, **S. Chen**, and J. Liu

Ecs Trans., vol. 27, no. 1, pp. 825–830, Nov. 2010.

Thermal elastomer composites for soft transducers

S. Jeong, **S. Chen**, J. Huo, L. Gravier, K. Gamstedt, J. Liu, S. Zhang, Z. Zhang, Z. Wu

Accepted by the 18th International Conference on. Solid-State Sensors, Actuators and Microsystems (Transducers 2015).

Vertically stacked carbon nanotube based interconnects for TSV application

D. Jiang, W. Mu, **S. Chen**, Y. Fu, K. Jeppson, and J. Liu

IEEE Electron Device Letters, vol. PP, no. 99, pp. 1–1, 2015.

Abbreviations

IC - integrated circuit

CSP - chip scale packaging

WLP - wafer level packaging

POP - packaging on packaging

VACNT - vertically aligned carbon nanotube

TSV - through silicon via

VACNF - vertically aligned carbon nanofiber

HIS - integrated heatspreader

TIM - thermal interface material

TE - thermoelectric

CPU - central processing unit

SOP – system on packaging

DIP - dual in-line packaging

PGA - pin grid array

LGA - land grid array

BGA - ball grid array

PTH - pin through hole

PCB - printed circuit board

SMT - surface mount technology

PLCC - plastic leaded chip carrier

QFP - quad flat pack

CTE - coefficient of thermal expansion

PM - powder metallurgy

CVD - chemical vapor deposition

CDCA - consumable electrode direct current arc

TEM - transmission electron microscopy

SAC305 - Sn3.0Ag0.5Cu

EDX - energy dispersive X-ray spectrometry

IMC - intermetallic compound

ENIG - electroless nickel immersion gold

TC - thermal cycling

OM - optical microscopy

DSC - differential scanning calorimetry

ICP - MS - inductively coupled plasma - mass spectrometry

XRD - X-ray diffraction

PI - polyimide

ZT value - dimensionless figure of merit

IR - thermal infrared

MMC - metal matrix composite

Contents

Chapter 1 Introduction

1.1 Background

In recent years, electronic devices have become an essential part of people's life as we need them for work, study, and communication almost every day, which therefore brings a huge market and has boosted the development of electronic industry for decades, especially after the invention of transistor and integrated circuit (IC) [1], [2].

The IC industry has developed rapidly in past 50 years. The density of transistors on the IC doubled every two years according to the prediction of Moore [3]. Driven by the IC industry, the electronic packaging industry also developed quickly because the IC always needs the electronic packaging for mechanical support, signal transmission, and heat dissipation. Since the 1960s, packaging structures and materials have been updated many times in order to make electronic devices smaller and faster. Currently, in most advanced packaging structures, such as chip scale packaging (CSP), wafer level packaging (WLP), and packaging on packaging (POP), the interconnect dimension has shrunk to the micro- and nano-scale, at which the reliability of traditional materials is no longer satisfied. New interconnect materials are therefore urgently required. In addition to interconnection, heat dissipation is another critical issue with advanced packaging structures, especially when these packaging structures combine with a high power IC. The complex structure and materials in the packaging will lead to a high thermal stress and non-uniform heat distribution, which will degrade the reliability of electronic packaging and thus constrain the increase of device performance.

Nanomaterials have been suggested for the manufacturing of electronic devices nowadays due to their unique properties. However, the gap between nanoscience and nanotechnology has greatly limited the application of nanomaterials. For instance, the carbon nanotube, one of the most promising nanomaterials, was reported 25 years ago [4]. Thousands of books and articles have been published, in which the structures, properties, and potential applications of nanotubes have been described systematically. However, it is rare to see a commercial product in today's market due to the high costs for fabricating, controlling, and manipulating carbon nanotubes. In this context, this thesis attempts to combine the nanoscience and nanotechnology in electronic packaging field by using nanomaterials whose properties and performance will be characterized in the packaging structures.

1.2 Scope

Addressing two urgent issues of advanced electronic packaging, namely interconnect and heat dissipation, several nanomaterials were fabricated and characterized in this thesis. The potential applications of these nanomaterials are demonstrated in Figure 1.1. A pile of chips is attached on the substrate with nanocomposite solders. The signal transmission between chips can be carried out by using vertically aligned carbon nanotube (VACNT) filled

through silicon vias (TSVs), nanocomposite solder bumps, and vertically aligned carbon nanofibers (VACNFs). An integrated heatspreader (IHS) is pressed on the top of stacked chips for heat transfer. The gap between the IHS and the chips is filled with a nanocomposite thermal interface material (Nano-TIM) in which several thin-small nanostructured thermoelectric (TE) coolers are embedded for pumping heat from the hotspots. Above the IHS, a large nanostructured TE cooler sandwiched with two Nano-TIMs is placed between a heat sink and the IHS for increasing the cooling rate.

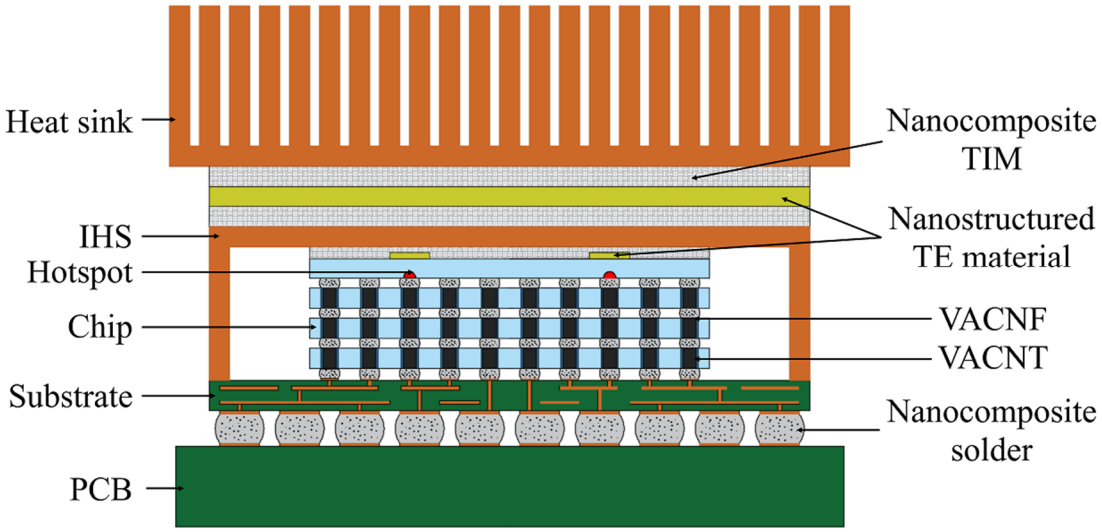


Figure 1.1: Potential applications of nanomaterials for advanced packaging

1.3 Outline

Based on the introduction in Chapter 1, the followed content of this thesis is divided into 5 chapters. Chapter 2 will give a brief introduction to electronic packaging and then review the development and challenges of advanced packaging. Chapter 3 will discuss the type, property, and application of nanomaterials. The fabrication processes for the nanomaterials used in this thesis will be also introduced. Chapter 4 will specify the characterizations and applications of the nanomaterials for interconnect. The content includes VACNT filled TSVs, VACNF bumps, VACNFs reinforced solder joint structure, and nanocomposite solders. In Chapter 5, two nanomaterials will be presented for heat dissipation in the electronic packaging. First of them is the Nano-TIM consisting of a polyimide (PI) network and indium metal. The mechanical properties of Nano-TIM will be mainly discussed. Another material discussed in this chapter is a nanostructured TE material, which is constructed of Bi_2Te_3 nanopowder and small amount of Ag nanoparticles. Chapter 6 will summarize the results presented in this thesis and give an outlook of nanomaterials.

Chapter 2 Electronic Packaging

Electronic packaging plays a critical role in electronic devices, and is responsible for signal transmission, heat dissipation, and mechanical support. The cost, performance, and dimension of electronic devices strongly depend on their packaging materials and structures. In the past decade, the development trends of consumer electronics can be summarized as dimensional minimization and functional diversification. A typical industrial case is the Apple iPhone, one of the most popular cellphone productions on the market. Its central processing unit (CPU) frequency increased about 4 times in last 10 years while the dimension (thickness) reduced almost half as shown in Figure 2.1. This remarkable achievement partially attributes to the application of advanced packaging technologies, such as POP and system on packaging (SOP).

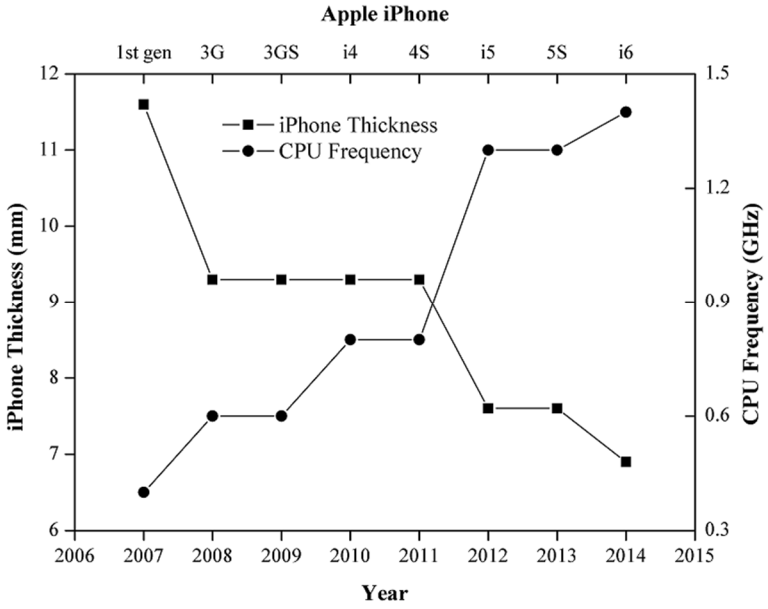


Figure 2.1: Development of the Apple iPhone

Another industrial case is from Intel, a giant of CPU manufacturing. In the Figure 2.2, the packaging density (pin number/packaging size) of Intel CPUs has continuously increased since 1970 and an exponential growth was presented after 2002. By 2010, the packaging density of Intel CPU has reached 100 cm^{-2}, almost 10 times higher than that of 1970. This high packaging density is definitely result of the development of CPU packaging structures, from dual in-line packaging (DIP) to pin grid array (PGA), land grid array (LGA), or ball grid array (BGA) packaging.

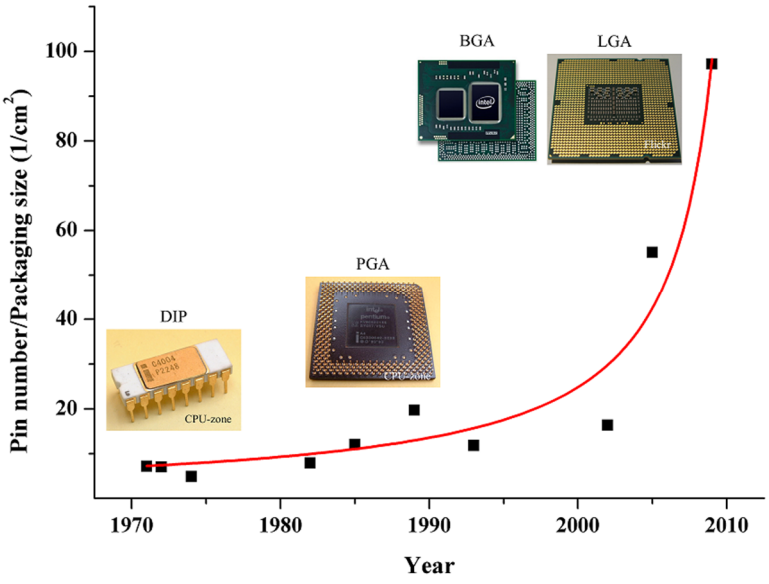


Figure 2.2: Packaging density of Intel CPUs

The structure of the electronic packaging is usually constructed with two packaging levels. The first level is called IC-level packaging, which directly interacts with ICs and protects ICs from various environmental impacts, such as moisture, dust, temperature, and force. The second level is named system-level packaging, which creates a platform on a system-level board for the communication between the packaged IC and other required components, such as resistor, capacitor, and diode. In particular, if more than one system-level board is included in a device, an extra packaging level is generally required for the signal transmission among the boards. It can be defined as third-level packaging. The hierarchy of electronic packaging is illustrated in Figure 2.3 [5].

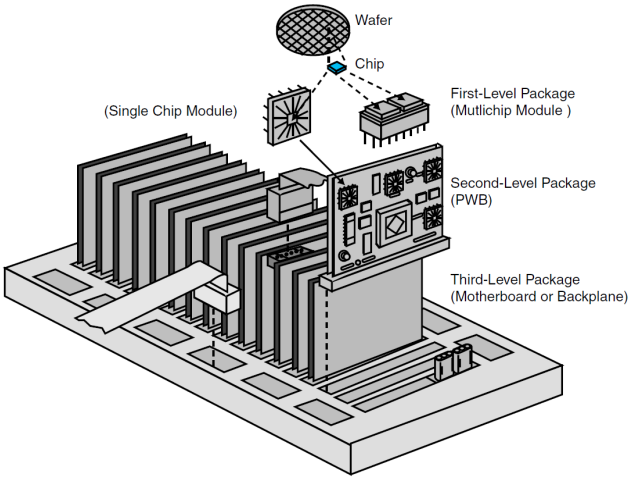


Figure 2.3: Packaging hierarchy

In the history of electronic packaging, hundreds of packaging structures have been developed for increasing the packaging density and shrinking the packaging size. Among them, wire-bonding with pin through hole (PTH) structure described in Figure 2.4 is one of the most typical combinations for the electronic packaging since 1970s. During the packaging process, the back-side of chip will be first attached on a lead-frame with the die-attach adhesive. Then, the pads on the chip surface will be connected with frame legs by using metallic wires. This technology is called wire-bonding. After wire-bonding, the chip and lead-frame will be encapsulated by the molding compound and form a DIP component. This DIP component will be assembled on a printed circuit board (PCB) by inserting and soldering its pins in the PCB holes.

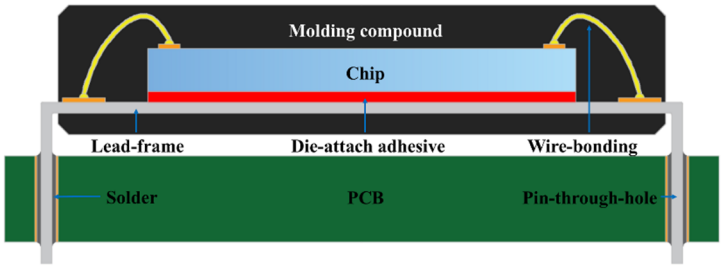


Figure 2.4: A DIP component assembled on the PCB with PTH system-level packaging.

Although wire-bonding with PTH structure has the advantage of cost, it is difficult to further increase the packaging density after 10 cm^{-2}. Therefore, the development of new structures and processes for high density packaging became a major topic in 1970s. During this period, a large number of new packaging structures were designed based on two creative technologies. One is flip-chip technology for IC-level packaging, and another is surface mount technology (SMT) for system-level packaging.

Flip-chip technology was developed by IBM in the 1960s and was used on the IBM System 3 mainframe computer in 1973 [6]. It is named flip-chip because the chip is turned face-down when compared to wire-bonding in which the chip is attached on the lead-frame face-up. In the flip-chip structure, solder balls and the substrate are generally used instead of wires and the lead-frame in the wire-bonding structure as shown in Figure 2.5.

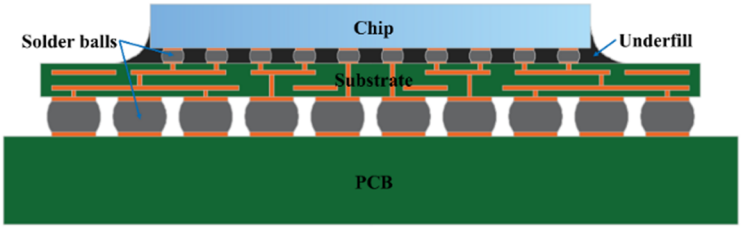


Figure 2.5: Flip-chip and surface mount technology.

SMT was invented in 1950s and started to be used in 1960s [7]. By using SMT, electronic components can be directly mounted on the PCB surface without pin-hole structures. The cost of manufacturing PCB was therefore greatly reduced as the fabrication processes related to the PCB holes were removed from the process line. Meanwhile, the required amount of PCB for a system was also reduced due to increased packaging density.

In order to meet the specifications of SMT, a huge number of component structures have been designed. Figure 2.6 gives the images of a typical PTH component (DIP) and three SMT components (PLCC - plastic leaded chip carrier, QFP - quad flat pack, BGA). Meanwhile, the Figure 2.6 also shows the relationship between the packaging size and the lead number for these four components [8] in which all SMT components have higher packaging density than PTH component. Furthermore, the BGA component owns the highest packaging density compared to other SMT components.

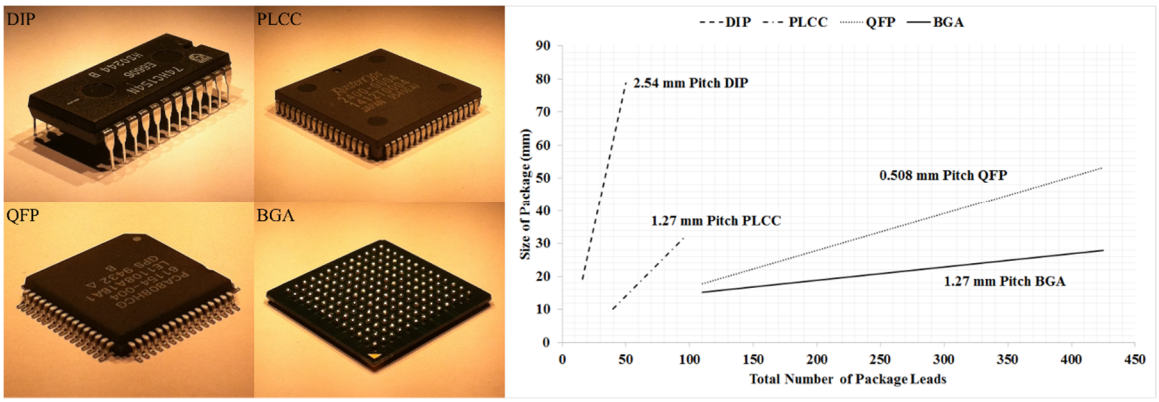


Figure 2.6: Images of typical PTH and SMT components and the relationship between packaging size and leads.

In recent years, the research of electronic packaging has begun to focus on 3-dimensional (3D) structures in order to increase the packaging density. Figure 2.7 lists two kinds of 3D packaging structures. One is formed by stacking packaged chips in the vertical direction,

which is named POP packaging. Another is constructed with a pile of chips and it is called a die stacking structure. The communication between the chips can be built-up by using wires at the peripheral areas of the chip surface or through vias inside the chips.

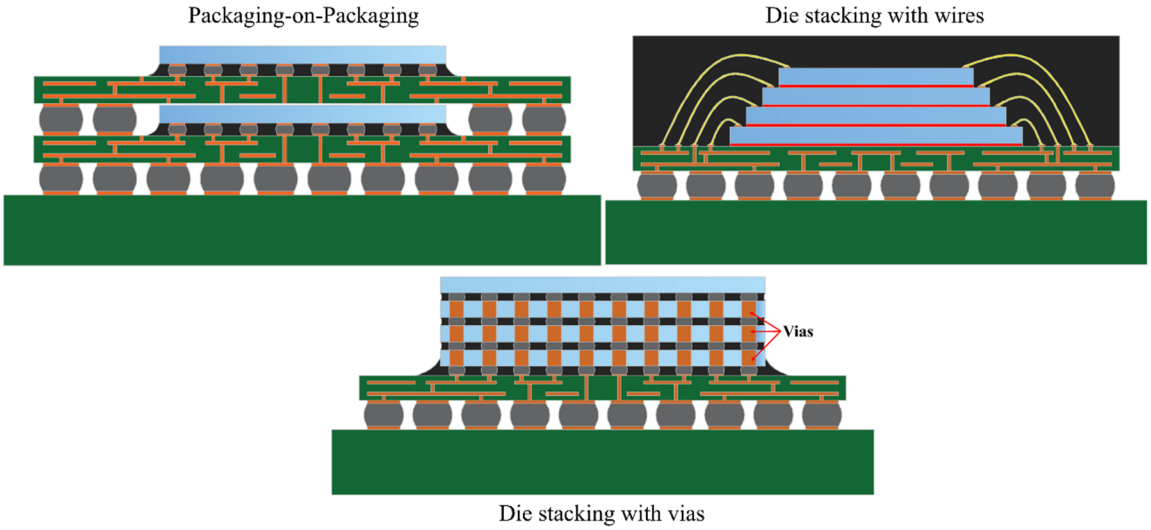


Figure 2.7: Typical structures of 3D packaging.

Although 3D packaging can greatly improve the packaging density, it has to face some challenges of packaging materials and processes. The first challenge is related to interconnect materials. Owing to the shrinkage of packaging size, the diameters of pads and vias are becoming smaller and smaller. According to the prediction of International Technology Roadmap for Semiconductors (ITRS) [9], the solder ball and via diameter in 3D packaging will be reduced to the range of micrometer as shown in Figure 2.8, which will lead to a series of reliability issues. For example, the thermal fatigue resistance and isothermal fatigue life of solder joints were severely degraded once the diameter of solder balls decreased to 170 μm [10].

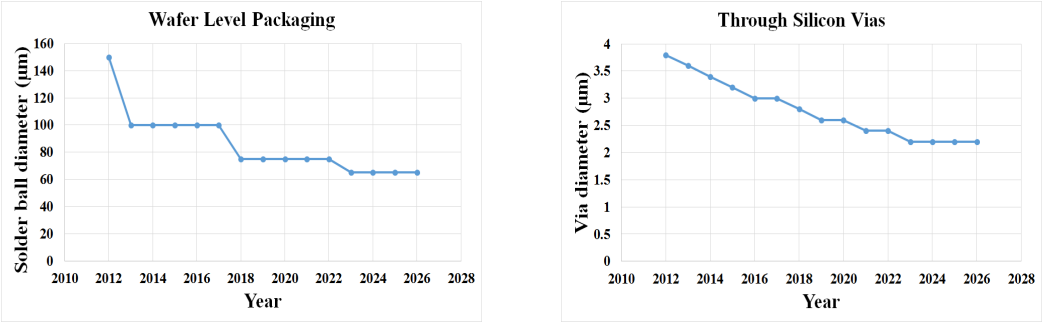


Figure 2.8: Development trends of solder ball and through silicon via diameters.

Another major challenge of 3D packaging is thermal management. Figure 2.9 shows the CPU power density in the past two decades [11]. The development of high frequency CPUs has slowed down since 2005 in order to keep the power density lower than 100 $W \cdot cm^{-2}$. It demonstrates the insufficient ability of current packaging technology to provide sufficient heat dissipation. Moreover, it is quite apparent that the thermal management issue will be more severe in a die stacked structure, in which the complex structure and small interconnect channels will dramatically slow the heat dissipation rate when compared to the single plane structure. For instance, the Cu filled TSV structure suffers from high thermal stress (>200 MPa) in the die stacked structure due to the large coefficient of thermal expansion (CTE) mismatch between Cu and Si (Cu: 17×10^{-6}/K, Si: 3×10^{-6}/K) as shown in Figure 2.10 (SEMATECH technical report).

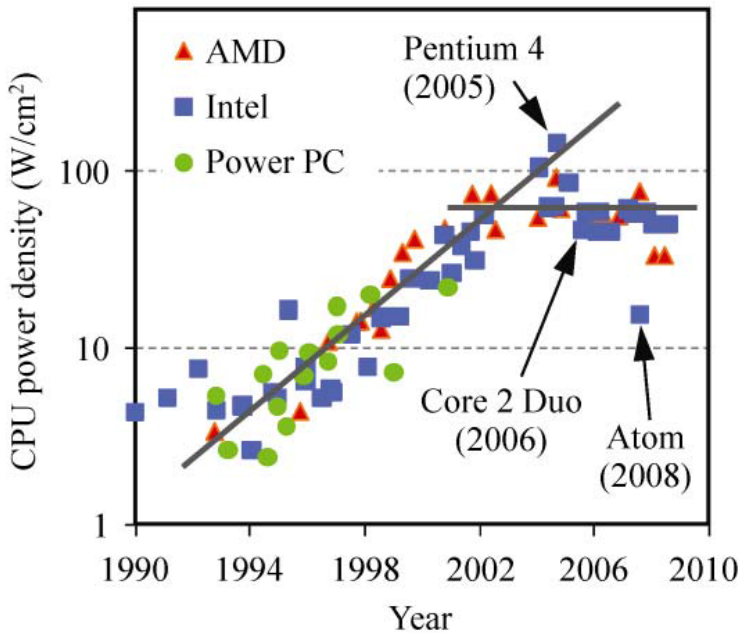


Figure 2.9: Development trend of CPU power density.

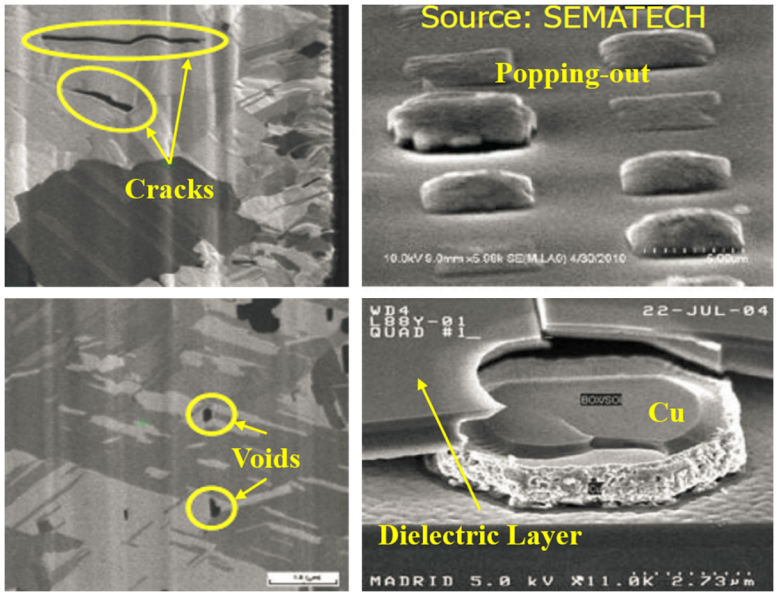


Figure 2.10: Defects in the Cu filled TSV due to high thermal stress.

As the traditional materials are becoming less able to meet the requirements of a high density packaging structure, new packaging materials with outstanding mechanical, electrical, chemical, and thermal properties will be highly desirable. Currently, nanomaterials are one of the most attractive materials for high density packaging. Their unique properties have been gradually discovered and proven in past several decades.

Chapter 3 Nanomaterials

Nano has become an increasingly used word and is most typically used to describe a substance that exhibits unique properties once the size shrinks below 100 nm (the nanoscale). One nanometer is equal to 10^{-9} meters, about 50 thousand times smaller than the diameter of a human hair [12]. Driven by the considerable interest in the nanoscale, two new research fields named nanoscience and nanotechnology have been established. According to the definition given by the Royal Society and Royal Academy of Engineering in the UK, nanoscience is the study of phenomena and manipulation of materials at atomic, molecular, and macromolecular scales, where properties differ significantly from those at a larger scale. Meanwhile, nanotechnologies are the design, characterization, production, and application of structures, devices, and systems by controlling shape and size on the nano-scale. These two new areas can be closely linked by the development of nanomaterials [13].

A nanomaterial is a material where some controllable relevant dimension is of the order of 100 nm or less [14]. Nanomaterials can be classified according to the number of dimensions as shown in Figure 3.1. Zero-dimensional (0D) nanomaterials means the materials are nanoscale in all dimensions. Nanoparticles are one of the most common 0D nanomaterials. One-dimensional (1D) nanomaterials are described as a material where one dimension is greater than nanoscale, such as nanowires and nanotubes. Carbon nanotube shown in the Figure 3.1 is a typical case of 1D nanomaterials. Two-dimensional (2D) nanomaterials usually relates to film materials where only the thickness must be in the nanoscale. Currently, single-layer graphene, consisting of only one layer of carbon atoms, has been regarded as one of the most promising 2D nanomaterials. 3D nanomaterials are defined as special bulk materials which are built with 0D, 1D, or 2D nanomaterials. 3D nanomaterials are sometimes quite similar to those normal bulk materials in appearance but have quite special microstructures and properties.

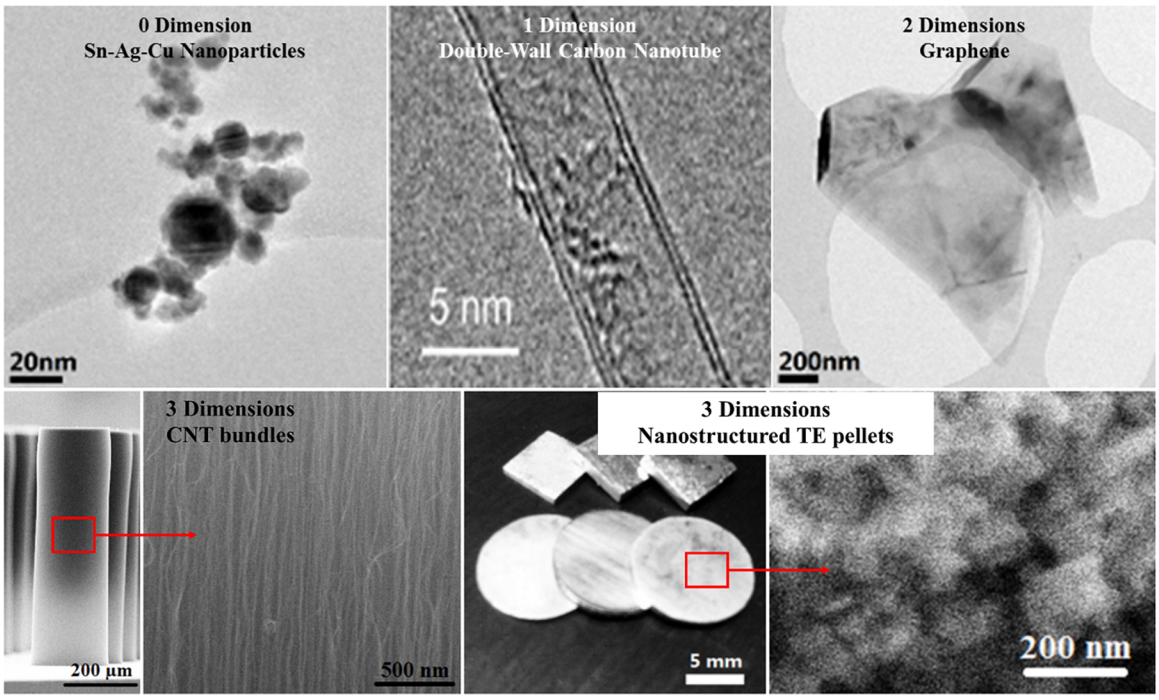


Figure 3.1: Types of nanomaterials classified by the number of dimensions.

Most nanomaterials have a large surface area which is the root of their many special properties. For instance, the melting point of metallic particles, such as Al [15], Sn [16], Sn-Ag-Cu [17], and Sn-Co-Cu [18], can be decreased by 10 - 100 °C by reducing the particle diameter to the nanoscale. This provides a huge benefit to powder metallurgy (PM) and the soldering industry. It has shown that the required process temperature for sintering Fe nanosized particles is almost 50 % lower than for large particles [19]. The temperature of soldering processes can also be decreased by using nanosized solder alloys. In the chemical industry, nanosized particles have been used as high efficiency catalysts due to their large surface area to the volume aspect ratio [20]. Besides their use as base materials, nanomaterials can also be used as effective reinforcement materials in a composite due to their small size and extraordinary properties. For instance, the strength of Cu was enhanced more than 2 times by using CNTs [21] or graphene [22] as reinforcement. The thermal conductivity of Ag filled conductive adhesive was approximately doubled by adding Ag-coated SiC nanoparticles [23].

As more and more unique properties of nanomaterials have been found and applied in different fields, various fabrication techniques of nanomaterials have been invented. Currently, the methods for fabricating nanomaterials can roughly divide into two techniques, namely top-down and bottom-up techniques. Top-down techniques are those in which the particles are fabricated from bulk material, and bottom-up techniques are those in which the particles are built atom by atom, or molecule by molecule [24]. The fabrication methods like ball-milling, mechanical exfoliation, Consumable electrode Direct Current Arc (CDCA), and electrospinning are typical top-down techniques. Meanwhile, chemical

vapor deposition (CVD) and the chemical reduction method are two popular bottom-up techniques. In the practice, shaping materials to the nanoscale is just first step for the application of nanomaterials. Post-processes, such as high temperature annealing and surface functionalization, are usually required in order to obtain high quality structures or achieve expected functions.

Chemical Vapor Deposition

CVD forms a thin film on the surface of a substrate through thermal decomposition or the reaction of gaseous compounds. The desired materials are deposited directly from the gas phase on to the surface of the substrate [28]. CVD is a common method for producing VACNT and VACNF. A major advantage of the CVD method for growing VACNT and VACNF is its compatibility with the standard lithography process. The carbon from source gases like C_2H_2 and CH_4 is deposited on the patterned catalyst particles for building CNT or CNF structures. The catalyst particles are generally formed by annealing a catalyst layer with the thickness of several nanometers at high temperature.

In this thesis, VACNT was synthesized with a thermal CVD (TCVD) method. A patterned catalyst layer, consisting of 10 nm Al_2O_3 and 1 nm Fe, was formed on a Si chip by using standard photolithography and evaporation processes. The growth process was finished in a commercial machine named Black Magic (Aixtron). The chip was first placed on a graphite heater and heated up to 500 °C at a rate of 300 °C/min in a 692 standard cubic centimeter per minute (sccm) H_2 flow and then annealed 3 min to form discrete catalyst particles. After that, the heater temperature was quickly raised to 700 °C. Meanwhile, a C_2H_2 flow of 200 sccm was injected to the growth chamber for CNT growth. The height of VACNTs is controlled by the growth time. When growth is finished, the Si chip with as-grown VACNTs were cooled down to the room temperature by using a 1000 sccm N_2 gas flow.

VACNFs were also grown by using Aixtron machine. A 7 nm Ni catalyst layer was evaporated on the chip before growth process. Then, a 5 min annealing step was carried out at 625 °C to form discrete Ni catalyst particles. During the annealing process, NH_3 gas was injected into the process chamber with 200 sccm flow rate for preventing the catalyst from oxidation. After the annealing process, the temperature of the heater was increased to 700 °C and a 40 sccm C_2H_2 gas flow was added as carbon source for VACNF growth. The 600 V DC plasma was applied to the growth process in order to promote the gas ionization.

The Figure 3.2 shows the growth process and morphology of as-grown VACNTs and VACNFs. The graphite heater is red in color due to the high process temperature. The blue plasma glow can be observed in the chamber of PECVD process. According to the scanning electron microscopy (SEM) images, the diameter and pitch between VACNFs are much larger than for VACNTs while the height is much shorter. This difference in morphology between VACNT and VACNF determines their specific applications and post-processes in this study.

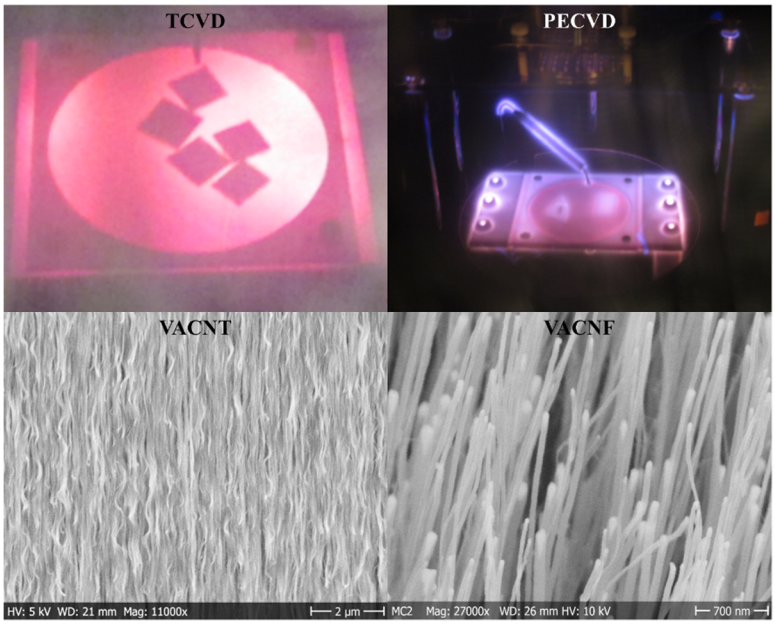


Figure 3.2: VACNTs and VACNFs fabricated with TCVD and PECVD method respectively

Consumable Electrode Direct Current Arc

CDCA is a promising top-down technique for fabricating nanomaterials in a large scale. This technique is originally invented for cutting and shaping hard or brittle materials for mechanical manufacturing. It was then applied for producing various fine powders since 1960s [25], such as metals [26][27], semiconductors [28], carbon [4][29], and even ceramic materials [30]. Figure 3.3 shows a typical manufacturing setup of the CDCA technique [31]. In principle, the arc (or a plasma channel) will be triggered once the dielectric liquid between two electrodes breaks down at high voltage. The tremendous energy and pressure near the arc can increase the surface temperature of the electrodes to around 10,000 K in only few microseconds [32]. As a result, the electrodes will be melted and evaporated. The molten part will quench in the dielectric liquid, forming microsized materials. Meanwhile, there will be nanosized materials in the evaporated part after solidifying in the dielectric liquid [33]. Although the setup of CDCA is simple, the process control is difficult. Many parameters, such as feeding speed, the distance between the electrodes, electrode diameter, power, and the viscosity of dielectric liquid, can significantly affect the quality and yield of nanomaterials. Therefore, each parameter must be carefully adjusted for different materials.

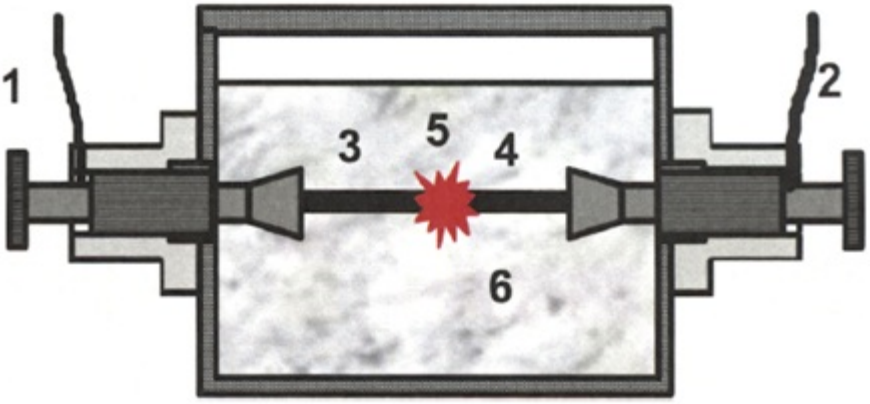


Figure 3.3: Schematic picture of CDCA set-up: (1) cathode, (2) anode, (3) and (4) electrodes, (5) spark, (6) dielectric coolant.

Electrospinning

Electrospinning technique is an old technique, the history of which can even date back to the 1745 when Bose described the formation of aerosols formed by electrical potentials on the surfaces of droplets. However, this technique has not been widely used for fabricating fibers until that Baumgarten reported on the electrospinning of acrylic microfibers and Larrondo and Manley reported a series of papers on the electrospinning of polymer melts in the 1970s [34]. Although the electrospinning technique has been around for hundreds of years its complex mechanism has only recently been explained in recent years with the assistance of a high speed camera. The basic setup and the mechanism of electrospinning are described in Figure 3.4. When a high voltage is applied between a metallic needle and a grounded conductive collector, the conical polymer droplet (Taylor cone [35]) will be formed at the nozzle of the needle due to the electrostatic force. If this electrostatic force overcomes the surface tension of the polymer solution, a liquid jet will be launched toward the collector. This electrically charged jet maintains a straight motion at the beginning of travel, and then will travel in an unstable bending motion due to the repulsive forces in the charged jet [36]. Owing to the continuous stretching and whipping during the travel from the needle and collector, this jet is finally shaped into a thin and long fiber, landing on the collector [37]. The right side of Figure 3.4 shows a SEM image of a PI film fabricated with the electrospinning technique. The average diameter of the fibers in this film is 780 nm [38]. The film was then heated at 320 °C for 1 hour in order to evaporate the residual solvent.

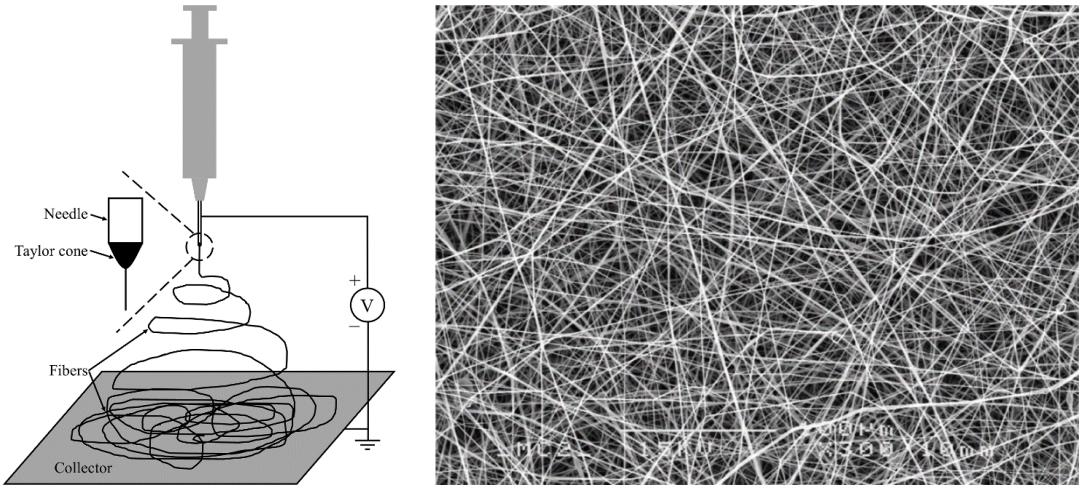


Figure 3.4: Basic electrospinning setup and PI network used in this thesis

In summary, the study of nanomaterials has achieved a lot of valuable results in recent years but some problems still need to be addressed. For example, the agglomeration of nanomaterials is still a critical issue in nanocomposite materials. Owing to the high surface energy [39], uniformly dispersed nanomaterials in nanocomposite materials is difficult to achieve. Although dispersants can be used on the surface of nanoparticles for breaking the agglomeration [40], [41], the effects of these dispersants on the properties of nanomaterials, such as conductivity and surface activity, must be carefully considered. Another critical problem of nanomaterials is related to the productivity and cost. Currently, some specific suppliers have started to provide commercial nanomaterials in the market, but the price is normally in the range of 10 to 100 USD/gram which is too high for the electronics industry, especially for the consumer electronic market.

Chapter 4 Interconnect

In electronic devices, signal transmission and mechanical connection are usually carried out by using interconnect materials, such as Cu traces, Au wires, conductive adhesives, and solder bumps. Therefore, interconnect materials play an important part in the electronic packaging. Every critical property of interconnect materials, such as melting point, surface energy, stiffness, mechanical strength, toughness, fatigue resistance, chemical resistance, temperature stability, electrical conductivity, maximum current density, and CTE, must be evaluated during the electronic packaging design. In this chapter, focusing on the reliability issues in the 3D packaging, two types of nanomaterials were manufactured and characterized. One of them is 1D carbon-based nanomaterials, including VACNT and VACNF. VACNTs were used as filling materials in TSVs, and VACNFs were used as bump materials for flip-chip technology as well as reinforcement materials for solder joint structure. Another material will be presented in this chapter is nanosized particles, which were mixed in the traditional lead-free solders in order to enhance the strength and thermal fatigue resistance of solder joints.

4.1 One-Dimensional Carbon Nanomaterials

CNT and CNF are two major 1D carbon nanomaterials. As far as the structure is concerned, both CNT and CNF can be described as a rolled graphene sheet. The difference is the rolling angle between the rolling axis and the sidewall. If this angle is equal to zero, the CNT structure can be formed, otherwise a conical structure will be presented. The CNF structure can be formed by stacking a pile of this kind of cones in one direction. The schematic pictures and transmission electron microscopy (TEM) images of CNT and CNF are shown in Figure 4.1.

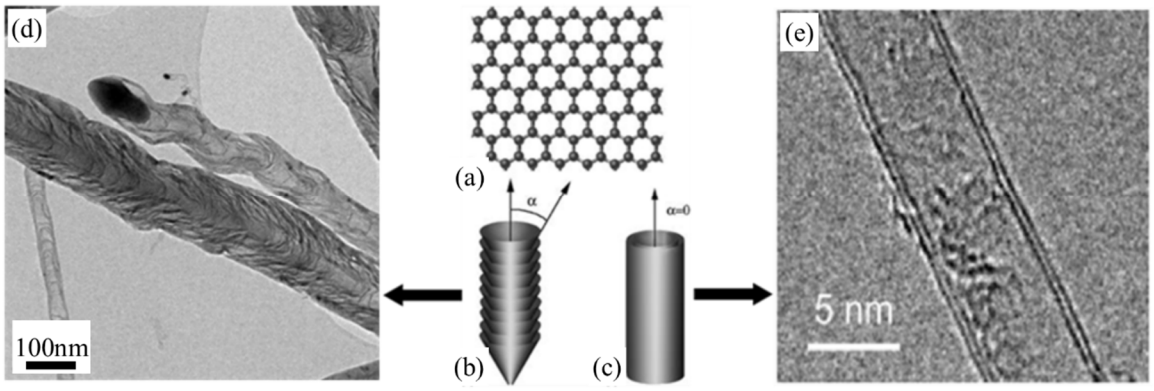


Figure 4.1: Schematic drawings of graphene (a), CNF (b) and CNT structure (c) [42]. TEM pictures of CNF (d) and CNT (e) [43].

Owing to the unique structures, CNT and CNF have many special properties which are needed for advanced packaging. Some of them are listed in Table 4.1 [44]–[48]. The nanosized diameter of CNT and CNF can satisfy the fine pitch requirement of high density packaging. Meanwhile, the high current density and thermal conductivity of CNT and CNF are benefit to high power devices. The low CTE, high strength, and lateral flexibility of 1D carbon nanomaterials are essential properties for building a high reliability device. In addition, some issues in traditional interconnect materials, such as electromigration, coarsening, and decomposition, can be addressed by using carbon materials due to their excellent stability.

Compared to CNT, CNF shows lower performance in terms of conductivity, stability, and reliability due to its cone-stacked structure. The angle of cone structure means that the charge transport direction is not only decided by the axial direction like CNT. The van der Waals bonding between cones also determines the mechanical strength cannot compare with covalent bonded CNT. Meanwhile, the chemical property of CNF is not so stable due to its exposed edges [42]. However, CNF still has the advantage of process compatibility [49]. The average diameter and spacing between CNFs is almost 10 times larger than CNT. Moreover, the aspect ratio of CNF is much smaller than CNT. These properties make CNF more compatible to traditional IC processes and convenient to be manipulated compared with CNT. For example, owing to the proper spacing and aspect ratio, the sputtering process can be an efficient method for coating CNF surface.

Table 4.1: Properties of CNT and CNF

Property	CNF	CNT
Average Diameter (nm)	55	4
Average Tube Spacing (nm)	300	20
Aspect Ratio	100	175000
Electrical Conductivity ($\times 10^6$ S·m^{-1})	2	0.1~1
Maximum Electric Current Density (x10^{6}A·cm^{-2})	3	4000
Thermal Conductivity (W·m^{-1}·K^{-1})	2000	3000-6000
Coefficient of Thermal Expansion (x10^{-6} K^{-1})	-1	-1.5±0.2
Tensile Strength (GPa)	8.7	150
Density (g·cm^{-3})	1.4~1.6	1.33~1.4

Although 1D carbon nanomaterials own many advantages, they also face a lot of difficult challenges in the practical application. First major challenge is the harsh growth condition. The growth temperature of carbon nanomaterials is usually higher than 600 °C which is a harmful temperature to most electronic materials. In recent years, some low temperature processes (around 150 to 200 °C) have been reported for CNF [50] and CNT [51] growth, but unsatisfied material quality constrains the application of these processes. Second challenge of 1D carbon nanomaterials is related to the inert surface of CNT and CNF. It is known that CNT and CNF need to bond with various metallic surfaces as the interconnect materials in the packaging structure. However, the solid bonding between carbon and metallic materials is difficult to be formed unless a metallic coating layer is used on the carbon surface. Currently, some wet chemical processes have been developed for coating vertically aligned [52] and discrete CNFs. These well coated CNTs and CNFs can be the promising materials for specific applications, such as making fuel cell or composite materials. However, wet coating processes are not suitable for IC-level packaging and can destroy the alignment of VACNTs and VACNFs or pollute the surface of ICs. Therefore, physical coating processes, such as sputtering or evaporation, appear to be more compatible with current IC fabrication processes. However, these processes can just work for those VACNTs and VACNFs with sparse distribution and small aspect ratio.

4.1.1 Post-processes for 1D carbon nanomaterials

Transfer Process

Owing to the high growth temperature, as-grown VACNT and VACNF have to be transferred from the growth chip to another chip. Currently, two transfer methods have been developed by Y. Fu, [53], S. Chen et al. [54]. One method is developed by using an indium layer on the target chips, and another is depended on the Au-Au bonding.

The indium layer assisted transfer process for VACNF transfer is described in Figure 4.2. In the beginning of the process, 20 nm Ti and 100 nm Au were sputtered on the surface of CNFs. After sputtering, the transfer step was carried out by using an indium coated target chip, as shown in Figure 4.2 (c), with a flip-chip bonder which can control heating temperature, time, and pressure. The thickness of indium layer is 1 μm. The Ti/Au coated VACNFs on the growth chip was pressed on the indium coated target chip with 5 MPa pressure at 160 °C. The duration of heating step is 20 s. In this period, indium melted and wetted the tip of the CNF, forming a bonding between indium layer and CNF. This bonding held the CNF and pulled it out from the growth chip during the separation step as shown in Figure 4.2 (e). The wetting area of indium on the CNF must be well controlled during the heating step. If the indium covers whole CNF and further spread to the surface of the Ti/Au coated growth chip, the reaction between indium and Ti/Au will cause the formation of the metallic bonding at the surface of growth chip. In this case, owing to the comparable bonding force at both sides of CNF, the complete transfer of VACNFs will be extremely difficult.

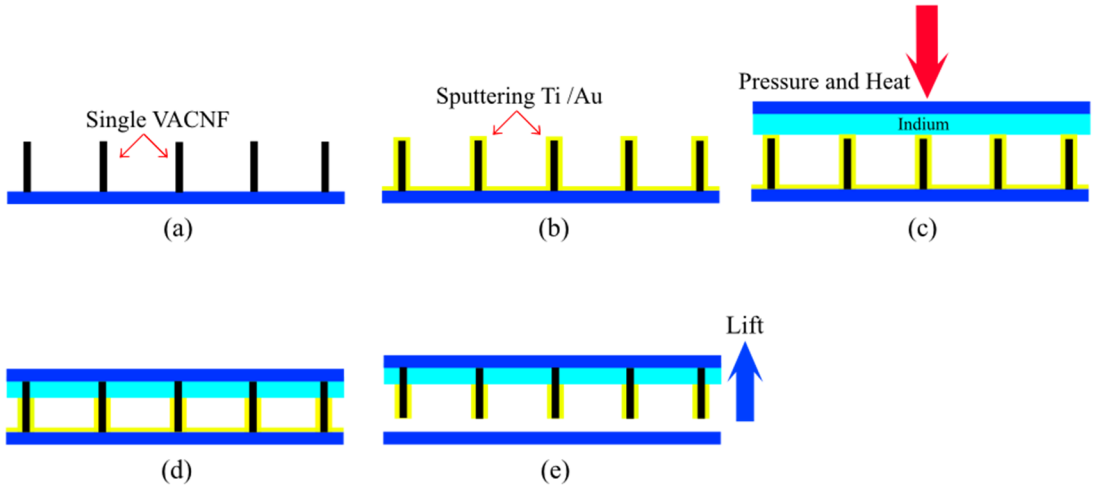


Figure 4.2: Schematic description for VACNF transfer process: (a) VACNFs were grown on the growth chip with PECVD method, (b) 20/100 nm Ti/Au metallic layer was coated on the surface of VACNFs with sputtering process, (c) target chip with 1 μm In layer was pressed on the growth chip with heating, (d) VACNFs were wetted by In at 160°C, (e) target chip was separated from the growth chip at room temperature.

The morphology of VACNFs before and after sputtering process is shown in Figure 4.3 (a) and (b). After sputtering, the VACNFs can still retain straight but the morphology has changed. The close-up views of VACNFs in Figure 4.3 (c) and (d) show that the VACNFs are well covered by metallic layer, and the average diameter of VACNFs was increased from 55 nm to 147 nm after the sputtering process as shown in Figure 4.3 (e) and (f). The 92 nm increasing at the diameter is consistent with the setting thickness of sputtering machine.

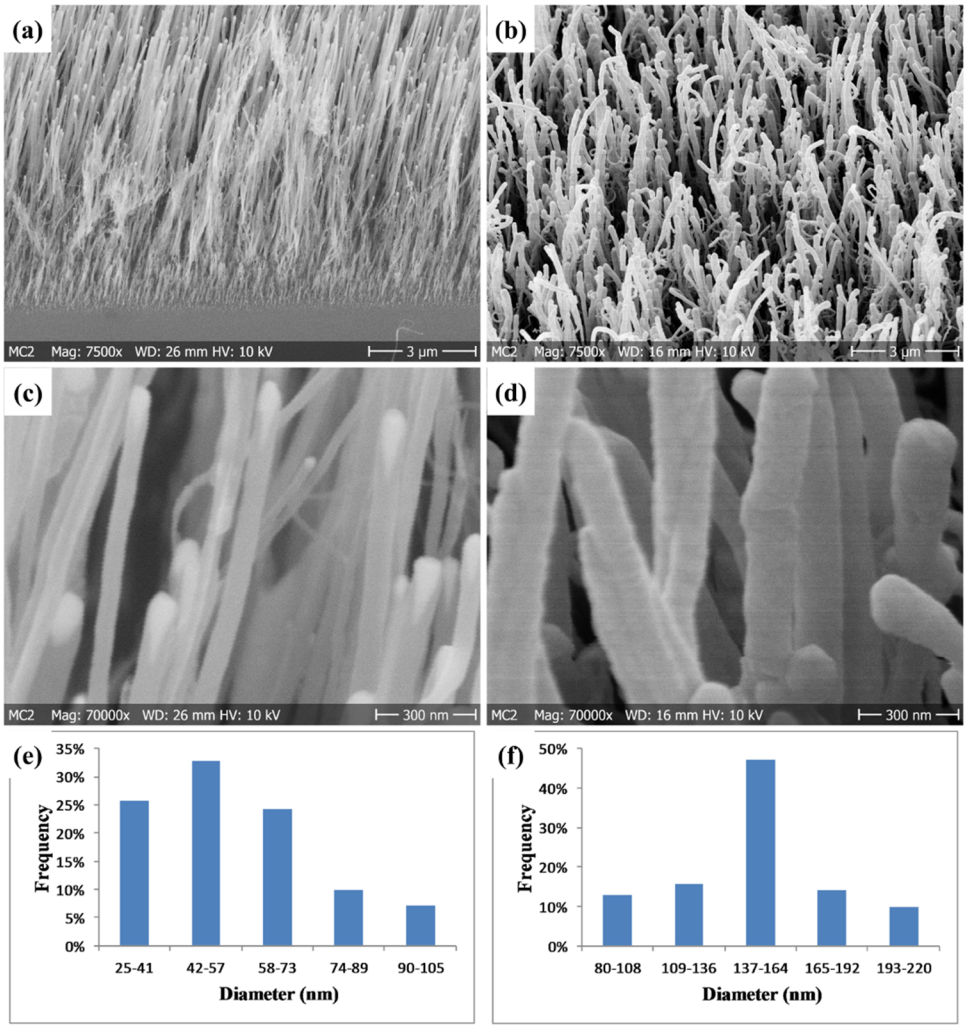


Figure 4.3: SEM pictures of VACNFs before (a) (c) and after (b) (d) Ti/Au sputtering process. Statistic of VACNF diameter before (e) and after (f) the sputtering process.

Figure 4.4 shows the VACNFs on the surface of the indium coated target chip after the transfer process. In the figure, most transferred VACNFs are still as straight as before. Furthermore, the tips of VACNFs have embedded into the indium layer at least 500 nm depth which gives a high transfer rate in this study.

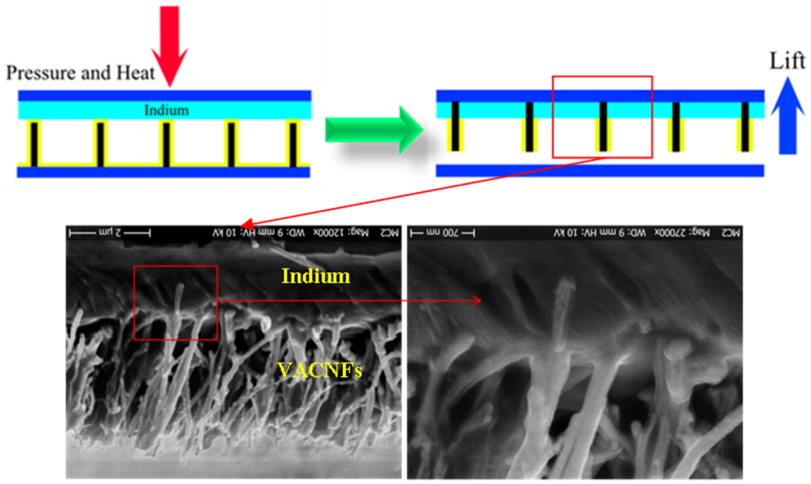


Figure 4.4: SEM observations of transferred VACNFs.

The processes for transferring VACNT bundles are quite similar to VACNFs. The process parameters for transferring VACNTs and VACNFs are listed in Table 4.2. Compared with VACNTs, shorter duration time is used for VACNFs due to the height limitation. The controllable height of VACNFs (around several micrometers) in this study is much shorter than that of VACNTs (several hundred micrometers), which extremely increases the sensitivity of transfer successful rate to the transfer parameters and conditions. As the VACNFs are so short, the dust at the surface of the chips can even affect the transfer result. Therefore, the process window for transferring VACNFs is quite narrow. Although researches have put a lot of effort into increasing the growth rate of VACNFs [42], the height of VACNFs is still limited in the range of several micrometers.

Table 4.2: Process parameters for transferring VACNT and VACNF

Transfer parameters	VACNT	VACNF
Temperature (°C)	170	160
Pressure (MPa)	6.4	5
Duration time (s)	120	20

Indium layer assisted transfer method is capable of transferring both VACNFs and VACNTs, but the high cost, oxidation [55], low strength [56], and low abundance [57] of indium are potential barriers of this method. Therefore, another transfer method depended on Au-Au bonding technique was studied. Figure 4.5 shows the VACNF transfer process with Au-Au bonding technique. VACNFs were grown on a patterned Si chip by using PECVD method as shown in Figure 4.5 (a). After the growth and sputtering process, the VACNFs were aligned and pressed to a target chip with Au pads by using the flip-chip bonder as shown in Figure 4.5 (c). The size of the Au pads on the target chip is 500 μm in

diameter. The optimized temperature, pressure, and duration time are set at 300 °C, 10 MPa, and 5 minutes respectively. After the bonding process, this target chip was separated from the growth chip once the temperature decreased to 40 °C as shown in Figure 4.5 (d).

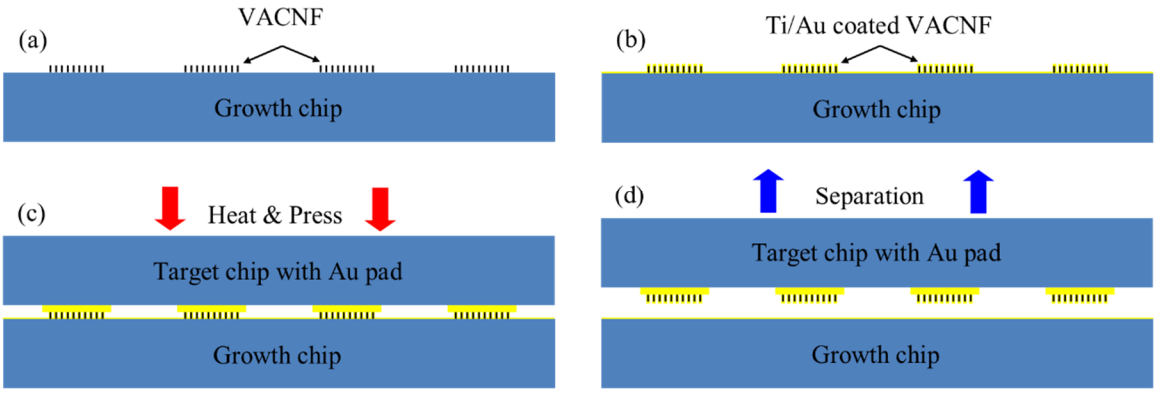


Figure 4.5: Au-Au bonding transfer process: (a) growing VACNFs with the PECVD method, (b) Ti/Au coating on the surface of each carbon nanofiber, (c) hot-pressing target chip on growth chip with flip-chip machine, (d) cold-separating target chip from growth chip.

Densification Process

The VACNT bundles fabricated with TCVD method are extremely loose materials in which more than 90 % of volume is occupied by the spacing between CNTs [58]. Apparently, this loose structure will decrease the performance related to the cross-section area, such as tensile stress and electrical conductivity. Unlike the VACNFs, the spacing between VACNTs is as narrow as 20 nm, at the same time, the aspect ratio of VACNTs can be as high as 175000. In this case, the spacing between CNTs is difficult to be full filled with physical method, like sputtering. Therefore, some research efforts begun to convert from filling the spacing to densifying the VACNT bundles. In this thesis, a vapor method was used for the densification of VACNT bundles. The VACNT bundles were exposed to the water diluted acetone at 75 °C. Once the acetone vapor condenses on the surface of CNT, CNTs will stick to each other due to the surface tension of acetone. After the acetone evaporates from VACNT bundles, a dry and densified VACNT bundles can be formed.

4.1.2 Applications of 1D Carbon Nanomaterials

CNT has many excellent properties, such as high current carrying capacity, thermal conductivity, Young's modulus, and lateral flexibility. These outstanding properties have been used in various fields in which many valuable results have been achieved. For instance, CNT has been used in the lead-free solders as reinforcement in order to increase the

mechanical performance [59], [60]. It was also used as thermal interface materials to fill the gap at the interface [61].

Application 1: Vertically aligned carbon nanotube filled through silicon vias

In recent years, CNT is considered as a promising filling material for the TSVs of die stacking structures. Table 4.3 lists several properties which should be considered as priorities for developing the filling materials of TSVs [44]–[46]. Compared with the properties of Cu, the properties of CNT show a clear advantage in every aspect except the electrical conductivity. CNT can stand high current density and transfer heat quickly. Meanwhile, CNT bundles have high mechanical strength and light weight which appear to be more and more important to recent consumer electronics.

Table 4.3: Comparison between copper and CNT

Property	Copper	CNT
Electrical Conductivity ($\times 10^6$ S·m^{-1})	59.6	0.1~1
Electric Current Density (x10^{6}A·cm^{-2})	0.1	4000
Thermal Conductivity (W·m^{-1}·K^{-1})	385	3000-6000
Coefficient of Thermal Expansion (x10^{-6} K^{-1})	17	-1.5±0.2
Tensile Strength (GPa)	0.22	150
Density (g·cm^{-3})	8.92	1.33~1.4

A series of processes described in Figure 4.6 were developed in order to fill the TSVs with VACNT bundles. The VACNT bundles grown with TCVD method were first densified with the vapor method and then transferred into the vias with indium layer assisted transfer method. After that, the space between VACNT bundles and the sidewall of vias is filled with benzocyclobutene (BCB) by using spinning coating process. The rugged surface shown in the Figure 4.6 (f) was then flatted by using a planarization process. Finally, a Ti/Au layer was deposited on the VACNT filled vias as metallic pads.

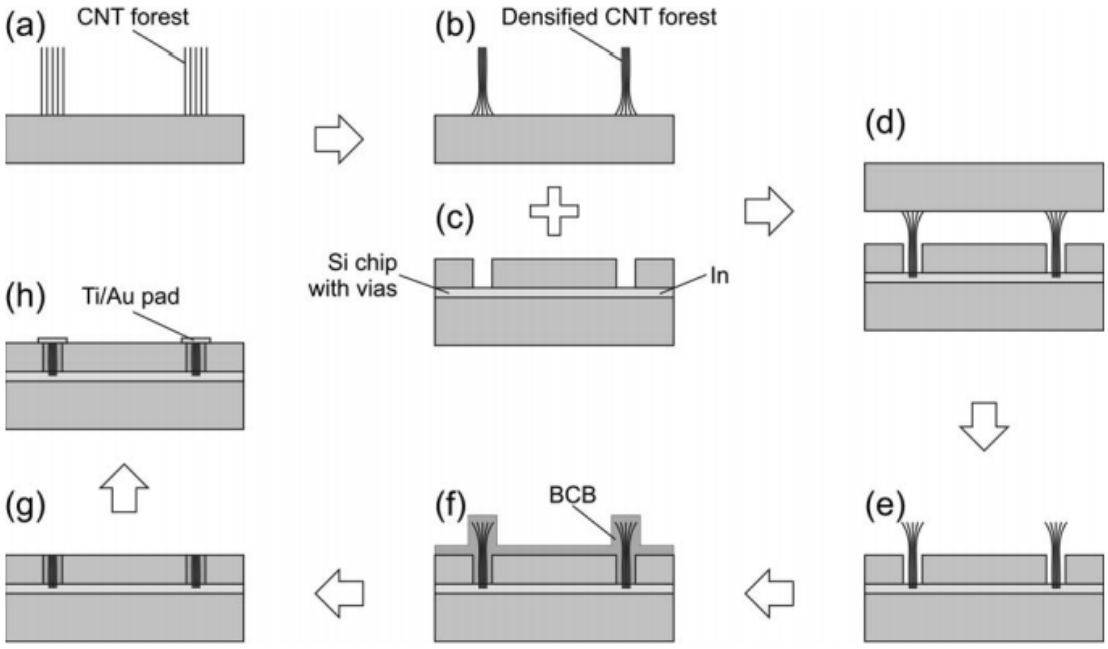


Figure 4.6: Process description of VACNT filled TSV. (a) VACNT growth with TCVD method; (b) VACNT densification with the vapor method; (c) target chip with the indium layer and vias; (d) and (e) VACNT transfer process; (f) filling gap between VACNT and via by using BCB; (g) planarization process; (h) Ti/Au deposited pads.

SEM observations of critical steps in the process are shown in Figure 4.7. Comparing Figure 4.7 (a) with (b), the shrinkage of VACNT bundles in diameter is as high as 70 %. The high magnification images of the sidewall of the VACNT bundles before and after densification are shown in Figure 4.7 (c) and (d). The number of the visible chinks on the sidewall of VACNT bundles was obviously decreased after the vapor densification process. Figure 4.7 (e) shows a densified VACNT bundle inside a via after the transfer process. The diameter of the via is 100 μm. The root of VACNT bundle (mushroom head shape) exposed from the via opening will be polished away with the planarization process. A Ti/Au pad formed on the top of via is shown in the Figure 4.7 (h), which will be used for making the bonding between TSVs and other materials, such as solders or conductive adhesives.

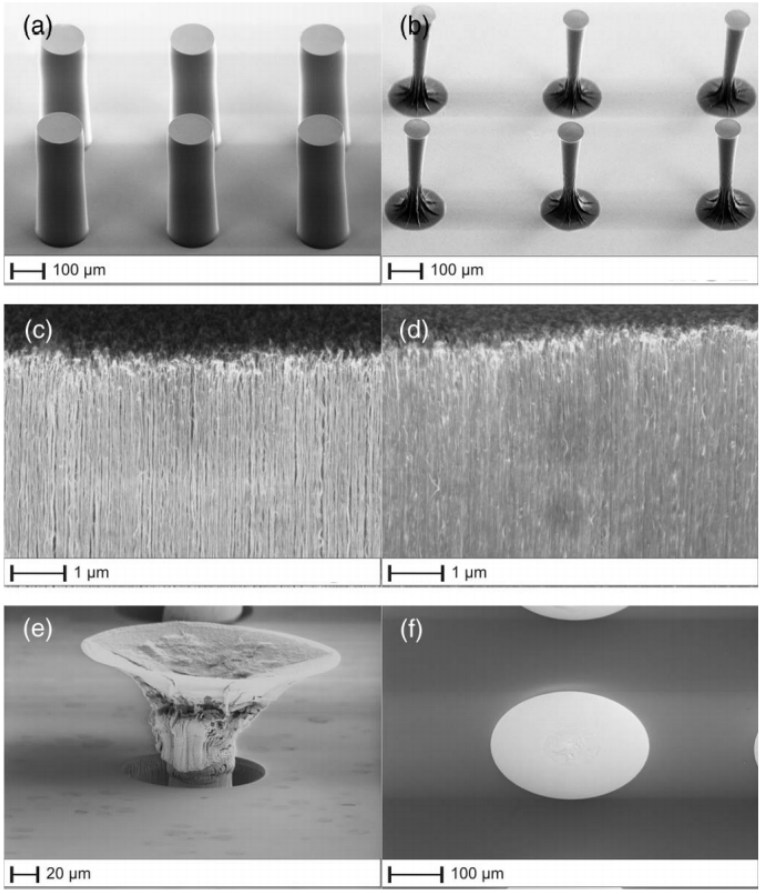


Figure 4.7: SEM images of critical steps in the process of VACNT filled vias. (a) as-grown VACNT bundles; (b) densified VACNT bundles; (c) and (d) VACNT sidewalls before and after densification process; (e) VACNT filled vias; (f) Ti/Au pads on the top of vias.

A cross-section of VACNT filled vias is shown in Figure 4.8 in which no obvious deformation of VACNT can be observed after transfer and planarization processes. Owing to the larger shrinkage at the CNT waist than the head, the CNT in the via shows a conical shape after removing the mushroom head. Figure 4.8 (b) shows the interface between the CNT and the Si chip. Although the structure of interface has been broken during polishing process, a bonding layer can be still recognized.

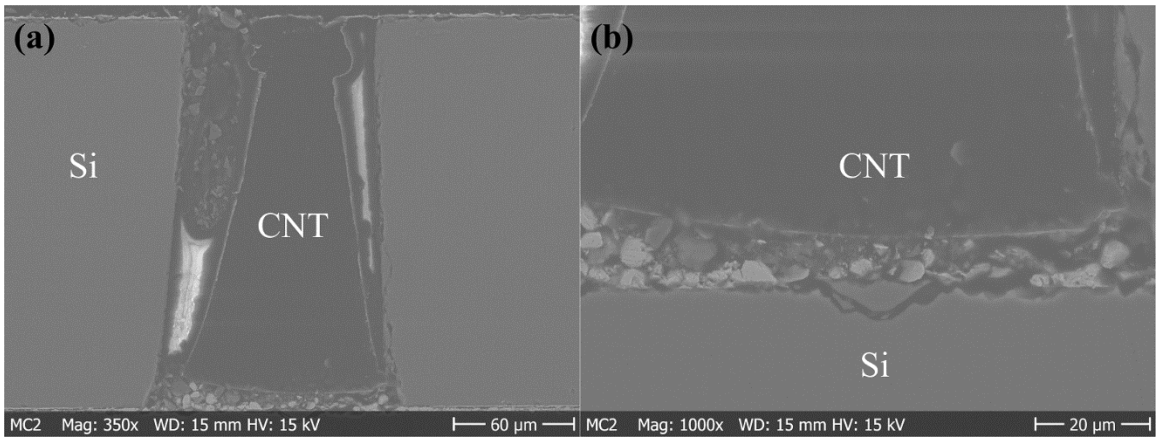


Figure 4.8: Cross-section of VACNT vias: (a) VACNT in the vias; (b) close-up view of CNT/Si interface.

The electrical performance of VACNT vias was measured with four probe method. Figure 4.9 exhibits an expected linear relationship between the current and voltage. The electrical resistivity of 3.9×10^{-5} Ω·m of VACNT vias was achieved, which is about an order of magnitude lower than that of un-densified VACNT filled vias.

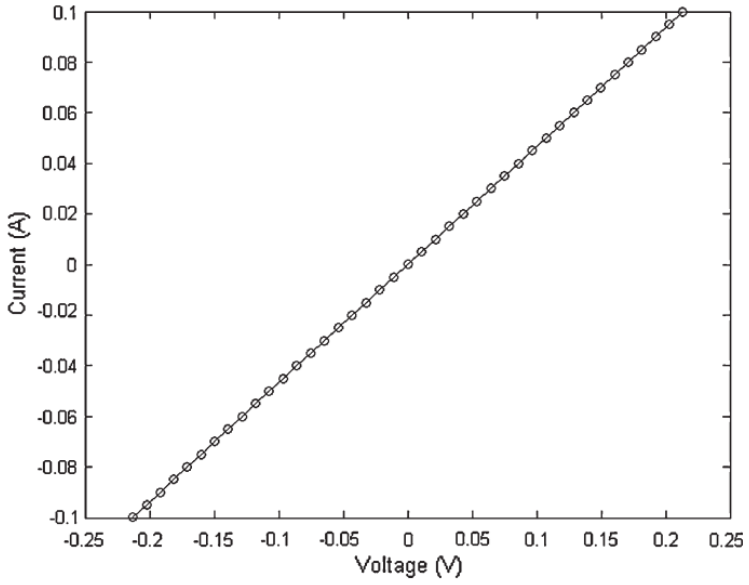


Figure 4.9: I-V curve of densified VACNT filled vias.

Application 2: Vertically aligned carbon nanofiber bumps

VACNF bumps were fabricated based on aforementioned growth and transfer processes. In order to measure the electrical and mechanical performance of VACNF bumps, two sample structures were designed. One is a bridge structure sample as shown in Figure 4.10 (a) and (b), which is used for electrical resistance measurement. This structure was formed by transferring the VACNFs to the two sides of a rectangular Si chip with the indium assisted transfer method and then mounting this Si chip on another two square Au coated Si chips with flip-chip bonder. Compared with the transfer process, the mounting process has a longer duration time and higher temperature and pressure in order to ensure the re-melted indium can wet entire CNF and reach the surface of Au coated square chips, forming a solid In-Au bonding. The cross-section of the bridge sample was shown in Figure 4.10 (c) and (d), in which the VACNFs are slight bent which is caused by the higher pressure loading in the mounting process. In addition to VACNFs, three traditional materials, Sn3.0Ag0.5Cu (SAC305), Ag filled conductive adhesive, and pure indium, were also tested with the same sample structure as VACNFs.

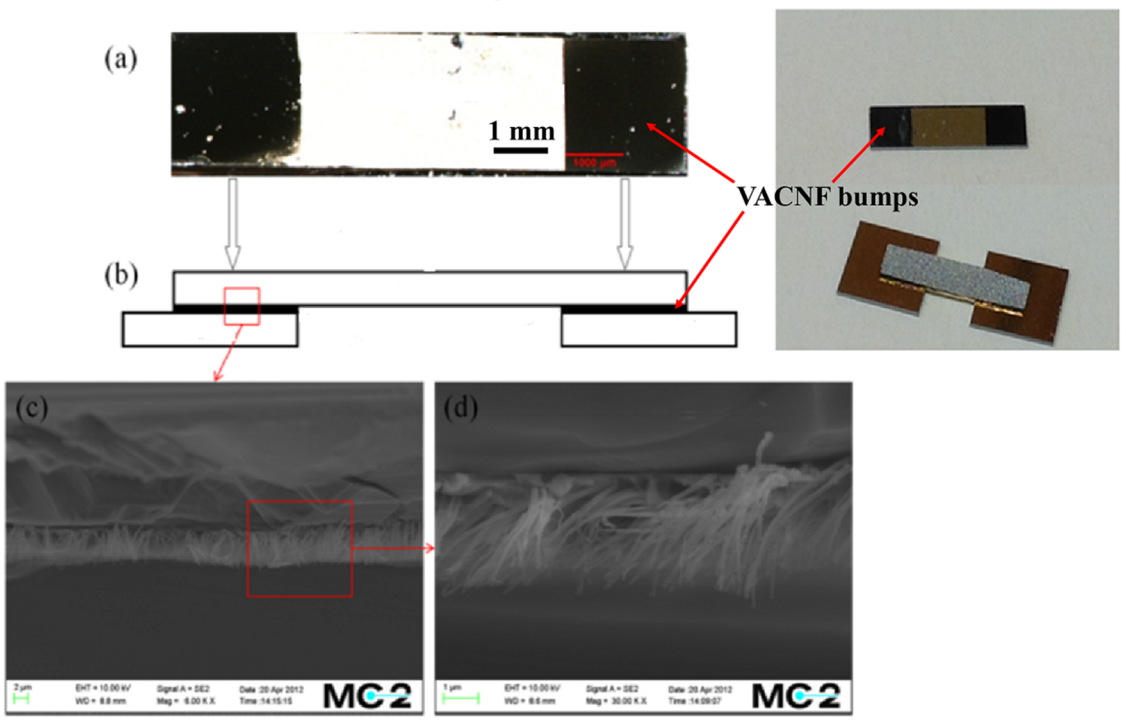


Figure 4.10: Bridge structure sample for electrical test: (a) indium coated rectangular Si chip with VACNF bumps, (b) schematic pictures of bridge structure sample, (c) SEM observation of the cross-section of VACNF bumps, and (d) close-up view of the red frame in the image (c).

Another sample structure used for shear test is a sandwich structure, as shown in Figure 4.11. The as-grown VACNFs were transferred to an indium coated Si substrate. Then, a gold coated square chip was mounted on the silicon substrate directly by using the same bonding process as the bridge sample.

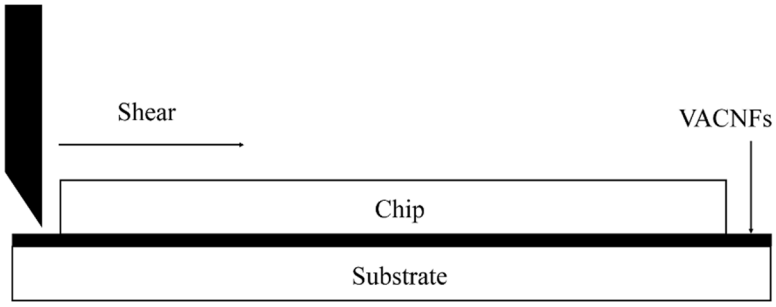
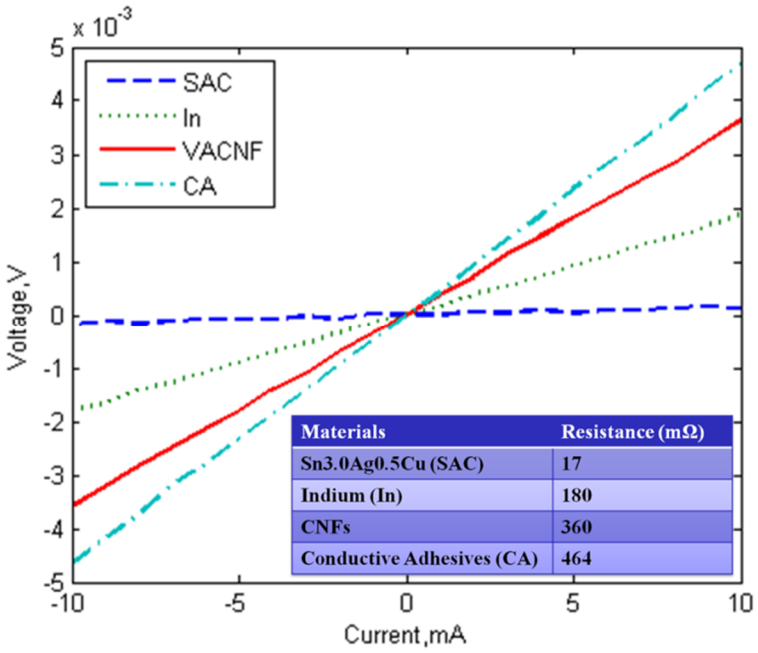


Figure 4.11: Sandwich structure for shear test

The results of electrical resistance test are shown in Figure 4.12. All samples can show a linear I-V curve. The inset table in Figure 4.12 displays the resistance of four kinds of interconnect materials. It indicates that the electrical performance of VACNFs is comparable with Ag filled conductive adhesive, but it is one order of magnitude lower than metallic materials.



Materials	Resistance (mΩ)
Sn3.0Ag0.5Cu (SAC)	17
Indium (In)	180
CNFs	360
Conductive Adhesives (CA)	464

Figure 4.12: The results of resistance measurement

The force-displacement relationship during the shear test was shown in Figure 4.13. All five VACNF samples show the similar force-displacement relationship. The force sharply dropped when the certain displacement was reached. It shows that the fracture mode of VACNF bump is close to brittleness fracture mode. According to the calculation, the average shear strength of VACNF bump is 1.5 MPa. Compared with our previous experimental results [62][63], this value is almost one order of magnitude lower than solders and conductive adhesives.

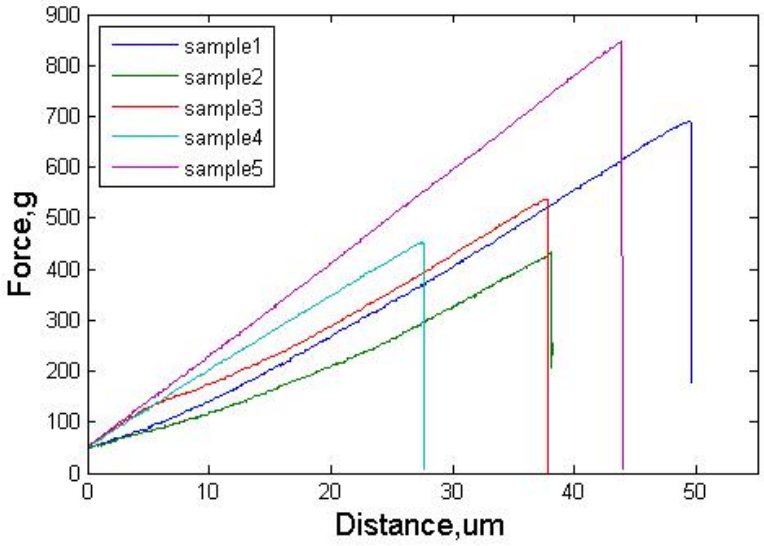


Figure 4.13: Force-distance relationship during shear test

The fracture surfaces after the shear test were observed by using SEM. Figure 4.14 (a) shows that the fracture surface at the chip side consists of two different areas. A close-up view near the boundary of these two areas is shown in Figure 4.14 (b). The VACNFs in the dark area and the Au coated Si surface in the bright area can be easily distinguished. According to the analysis of energy dispersive X-ray spectrometry (EDX), the VACNF surface (point 1) in Figure 4.14 (b) contains In-Au intermetallic compound (IMC) with the atomic ratio of 3:1 as shown in Table 4.4. Meanwhile, some small pieces (point 2 and 3) can be observed in both areas. They also include the In-Au IMC as the VACNF surface. It proves that the melted indium at the substrate side has crossed whole VACNF surface and begun to react with the Au at the Si chip side. Figure 4.14 (c) shows a high magnification picture of the VACNF area. Compared to as-coated VACNF, the surface of VACNF in Figure 4.14 (c) has become quite rough, which is another evidence for the reaction between Au and In on the VACNF surface during the bonding process. Figure 4.14 (c) also shows some broken VACNFs. The cross-section of these broken VACNFs presents a circular-hollow structure as shown in Figure 4.14 (d).

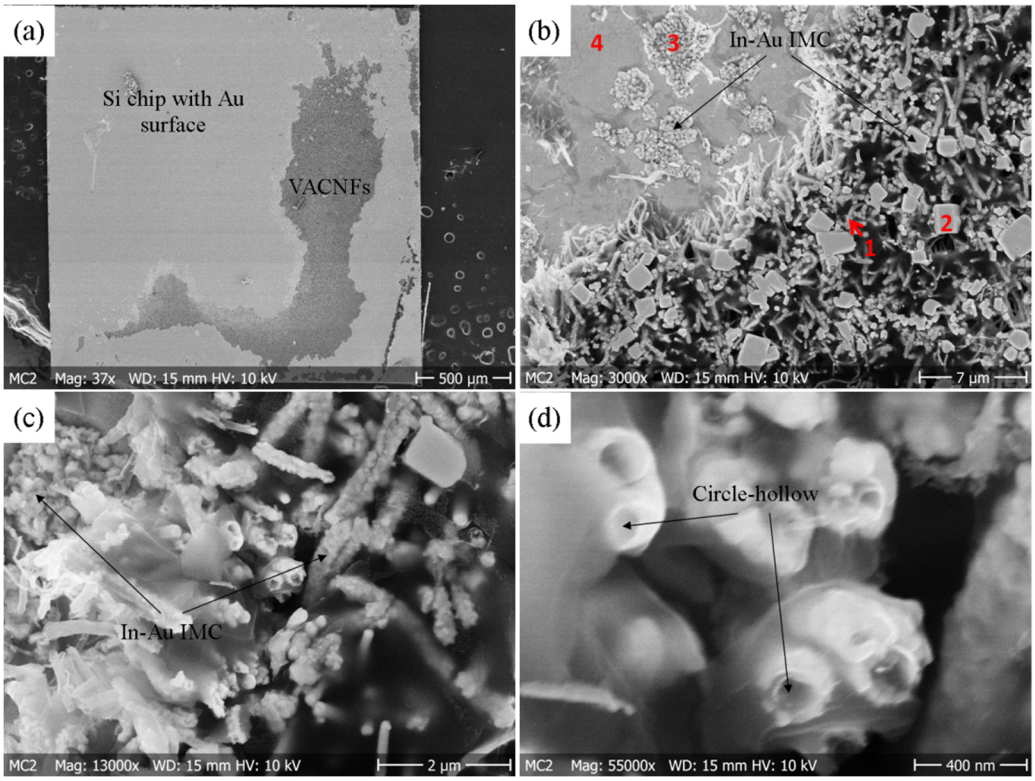
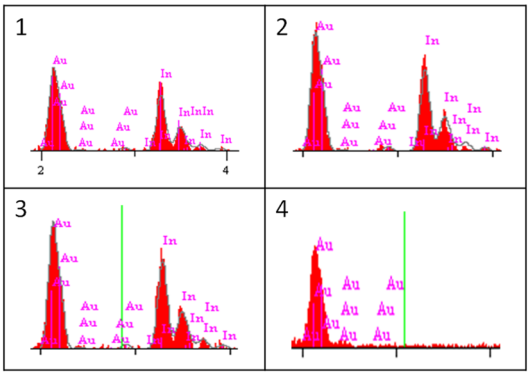


Figure 4.14: Chip side: (a) fracture surface at the chip side, (b) close-up view of the fracture surface, (c) close-up view of the VACNFs area, (d) circular-hollow structure on the cross-section of broken VACNF.

Table 4.4: EDX analysis on the fracture surface at the chip side



Point	In (at.%)	Au (at.%)
1	74	26
2	77	23
3	71	29
4	0	100

Figure 4.15 (a) shows the fracture surface at the substrate side, which agrees well with the surface pattern at the chip side. Figure 4.15 (b) shows a close-up view at the boundary of dark and bright area. In contrast to the chip side, the bright area is covered by VACNFs and the dark area is Si substrate surface. Some small pieces with broken VACNFs can be observed in the Si substrate surface. According to the high magnification image showing in Figure 4.15 (c), the sidewall of these broken VACNFs has been covered by rough In-Au IMC. Figure 4.15 (d) shows the small cones on the cross-section of broken VACNFs. This conical structure is consistent with the circular-hollow structure at the chip side. Combining the cross-section of broken VACNFs at the two sides, we can conclude that the VACNF is easy to be broken at the interface between the cones of CNF. This break structure of CNF was also observed by other researchers [64].

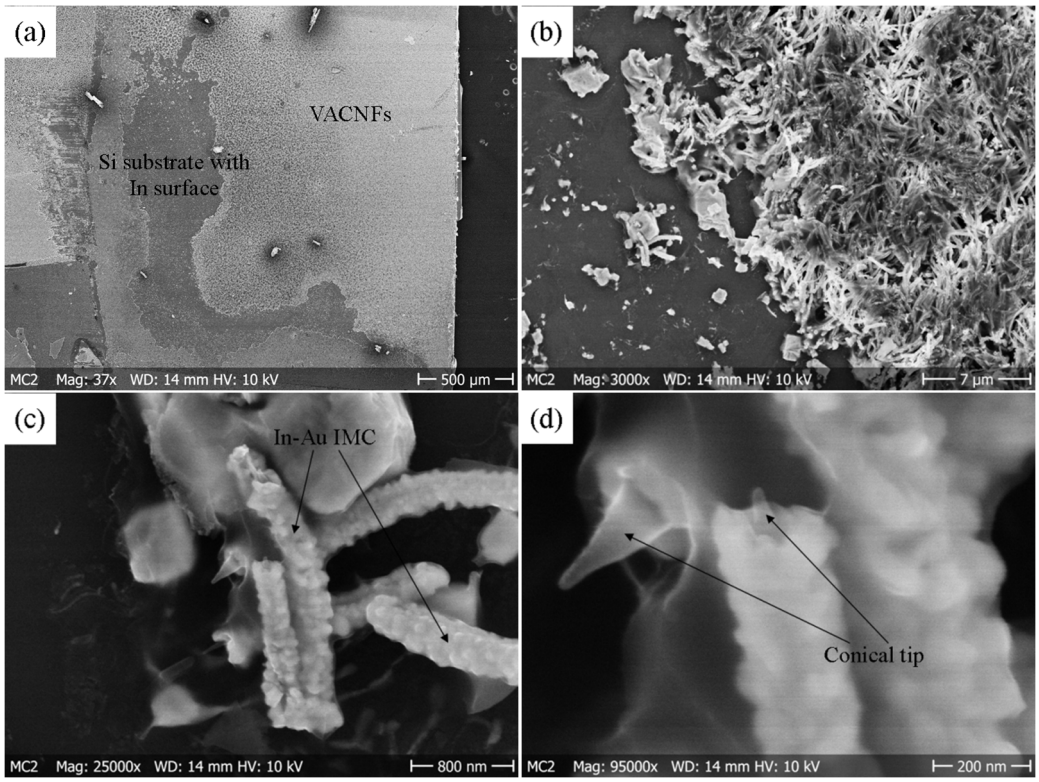


Figure 4.15: Substrate side: (a) fracture surface at the substrate side, (b) close-up view of the fracture surface, (c) close-up view of the broken carbon nanofiber, (d) conical structure on the cross-section of broken CNF.

In Table 4.4, the point 4 at the chip side only shows some Au peaks without In. It means that the distribution of IMC layer at the interface is discontinuous or not uniform. The possible reason could be attributed to the insufficient indium volume at the substrate side. During the transfer process, the indium will wet the tip of the VACNF as shown in Figure 4.16 (a). A part of indium will be consumed by reacting with Au at the VACNF surface.

After that, the indium will be further consumed during the bonding process in order to wet whole surface of the VACNF. Finally, the indium can reach to another side (chip side) and form IMC layer, as shown in Figure 4.16 (b). However, if the volume of indium is not enough, after bonding process, the left indium will be insufficient to form IMC layer with Au at the chip side, see Figure 4.16 (c). In this case, discontinuous IMC layer will be formed at the interface. Therefore, increasing the thickness of indium layer could be a possible way to form continuous and uniform IMC layer at the interface and then improve the electrical and mechanical performance of VACNF bumps. However, on the other hand, the cost will be further increased.

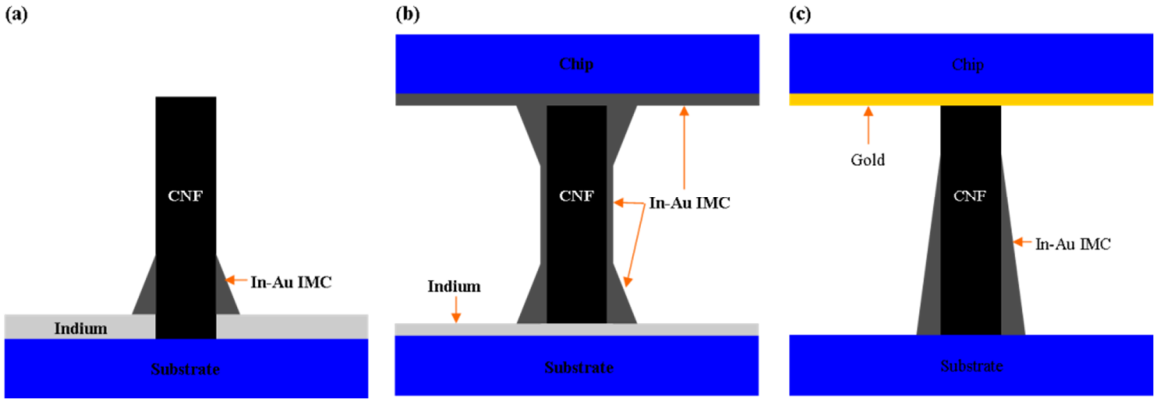


Figure 4.16: The status of IMC formation during the transfer and bonding process: (a) the formation of IMC at the tip of VACNF during transfer process, (b) continuous IMC layer can be formed at the chip side if sufficient indium can be supplied during the bonding process, (c) IMC layer cannot be formed at the chip side if without enough indium supply during the bonding process.

Application 3: Vertically aligned carbon nanofiber reinforced solder joint structure

Besides being used as bump materials, VACNFs are also used for enhancing the thermal fatigue resistance of traditional solder joint structure. The structure and fabrication processes of daisy-chain samples were shown in Figure 4.17. Each step in the process is described by a schematic drawing together with an optical microscopic image. At the beginning of the process, the VACNFs were grown on a patterned Si chip by using PECVD method as shown in Figure 4.17 (a). The diameter and pitch of the circles are 400 and 1000 μm respectively. Figure 4.17 (b) - (d) describe the VACNF transfer processes based on the Au-Au bonding method. Figure 4.17 (e) shows a FR4 substrate with Cu pads and electroless nickel immersion gold (ENIG) surface finish. After dispensing SAC305 solder paste on the Cu pads, the target chip shown in Figure 4.17 (d) was mounted on this substrate by using the flip-chip bonder as shown in Figure 4.17 (g). Lastly, by using a reflow solder process, a daisy-chain structured sample with VACNF/SAC305 solder joints was presented and shown in Figure 4.17 (h).

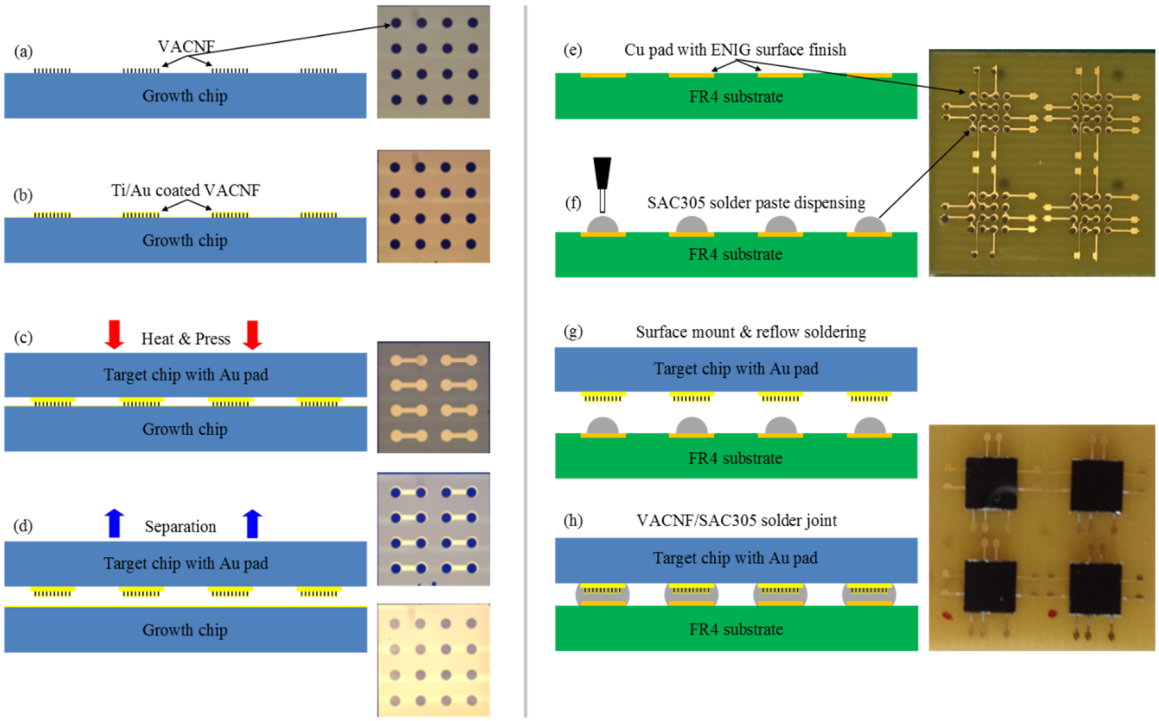


Figure 4.17: Assembly process of VACNF/SAC305 solder joint: (a) growing VACNFs with the PECVD method, (b) Ti/Au coating on the surface of each carbon nanofiber, (c) hot-pressing target chip on growth chip with flip-chip machine, (d) cold-separating target chip from growth chip, (e) FR4 substrate with Cu pad and ENIG surface finish, (f) dispensing SAC305 solder paste on the Cu pad with dispensing machine, (g) mounting target chip on FR4 substrate and running reflow process, (h) thermal cycling test sample with VACNF/SAC305 solder joints.

The temperature profile for thermal cycling (TC) test is shown in Figure 4.18. The temperature range of the TC test is -40 to 115 °C. The heating and cooling rate are both 31 °C/min. The duration time per cycle and the soak time at peak and valley of the profile were set to 30 and 10 minutes respectively. The temperature and sample resistance are recorded per minute by an Agilent 34972A Data Acquisition device. The sample will be regarded as failure if 5 consecutive events ($R > 1000\ \Omega$) are detected. Pure SAC305 solder joints were also tested with the same sample structure as VACNF/SAC305. The initial average resistance of VACNF/SAC305 and pure SAC305 samples is $58 \pm 28\ \Omega$ and $43 \pm 28\ \Omega$ respectively.

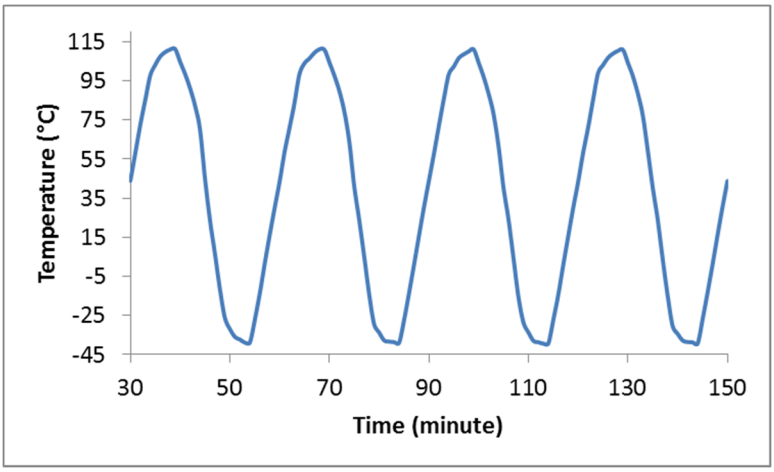


Figure 4.18: Recorded temperature profile in thermal cycling test

The relationship between the failure rate and the number of cycles is illustrated in Figure 4.19 (a). The failure rates for both samples rapidly increase after 300 cycles, but the failure rate of the VACNF/SAC305 sample is obviously lower than that of the SAC305 sample. The Weibull distributions of cumulative failure function for both samples are shown in Figure 4.19 (b). The shape parameters of the VACNF/SAC305 and SAC305 samples are 2.2 and 3.7 respectively. The characteristic life of the VACNF/SAC305 sample is 589 cycles, which is about 40% longer than that of SAC305 sample (409 cycles).

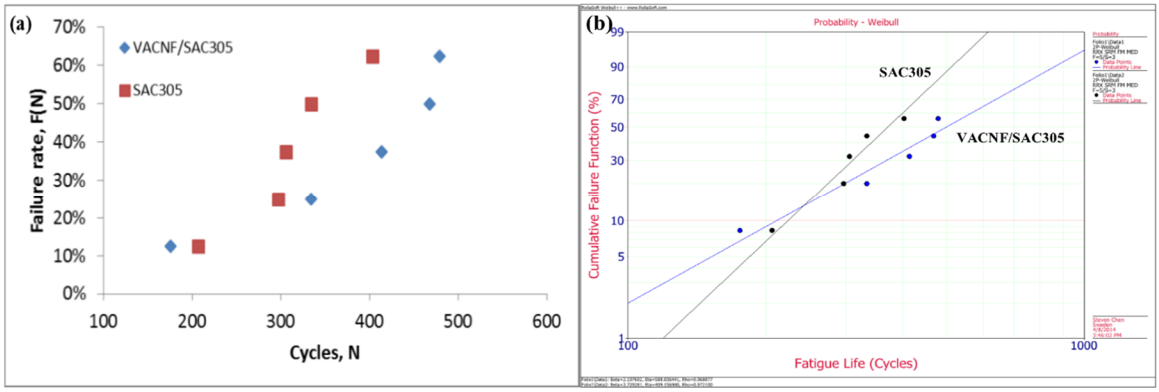
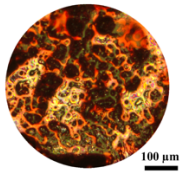
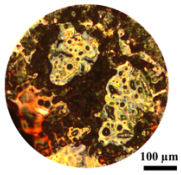
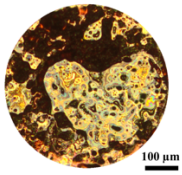
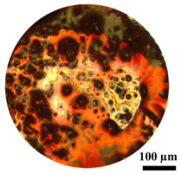
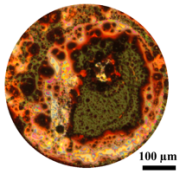
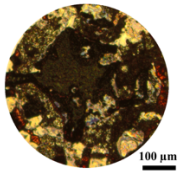
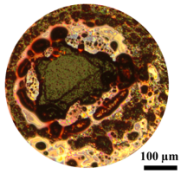
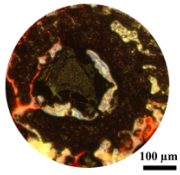


Figure 4.19: Results of thermal cycling test: (a) relationship between the failure rate and the number of cycles, (b) Weibull distribution of cumulative failure function.

The dye and pry method was used for failure analysis after the TC test. Table 4.5 shows the optical microscopy (OM) images of the fracture surfaces on the chip side. The observation was focused on the solder joints at the four corners of the chip which generally endure the highest stress and strain in the TC test. According to the area calculation of

colored region, the crack region of the SAC305 sample is obviously larger than that of the VACNF/SAC305, which means the speed of crack propagation in the VACNF/SAC305 solder joints is lower than SAC305. The aforementioned longer thermal fatigue life of the VACNF/SAC305 sample should be attributed to this lower crack propagation speed.

Table 4.5: Dye and pry analysis of fracture surfaces

SAC305					Average
Crack Area%	93.4	72.9	66.0	90.5	80.7
VACNF/ SAC305					Average
Crack Area%	65.7	6.6	80.8	75.6	57.2

After the OM analysis, the fracture surfaces of the VACNF/SAC305 solder joints were observed by SEM. Figure 4.20 (a) shows a hybrid morphology on the fracture surface of the chip side. Uncracked and cracked regions can be clearly distinguished. Figure 4.20 (b) and (c) are the close-up views of uncracked and cracked regions. In Figure 4.20 (b), some VACNFs are distributed on a rough surface. The subsequent EDX analysis only found Au and Sn elements from this rough surface without Ni or Ag, which implicates that the fracture surface in this region should be very close to the chip side. In Figure 4.20 (c), some VACNFs are distributed around a large bulk which consists of Sn and Ag, proving that the fracture surface in this region is located in the SAC305 solder. Two schematic pictures in Figure 4.20 (d) describe the formation process of this hybrid morphology. The red line in the left schematic picture represents the crack in the solder joint. During the thermal cycling, the crack is initially generated around the corner and propagated along the IMC layer. When the crack meets the VACNFs layer, it appears to bypass the VACNF/SAC305 region, which can reduce the propagation speed and change propagation path of cracks and consequently contributes a long thermal fatigue life to the solder joint. In this case, if the crack finally does not go through whole solder joint after thermal cycling, the cracked and uncracked regions will present a different fracture surface morphology after dye and pry as described in Figure 4.20 (d). The fracture surface of the cracked region was formed in the solder under the VACNFs on the chip side. Therefore, most VACNFs in this region are

invisible because covered by SAC solder after prying the chip off the substrate. However, some exposed VACNFs can be observed at the edge of the SAC305 solder bulk as shown in Figure 4.20 (c). Around the uncracked region, owing to the stronger bonding between the SAC305 solder and the surface of the VACNFs compared to the Au-Au bonding between the chip surface and the tip of the VACNFs, most VACNFs were removed from the chip surface and only a few VACNFs were left on the chip side as shown in Figure 4.20 (b).

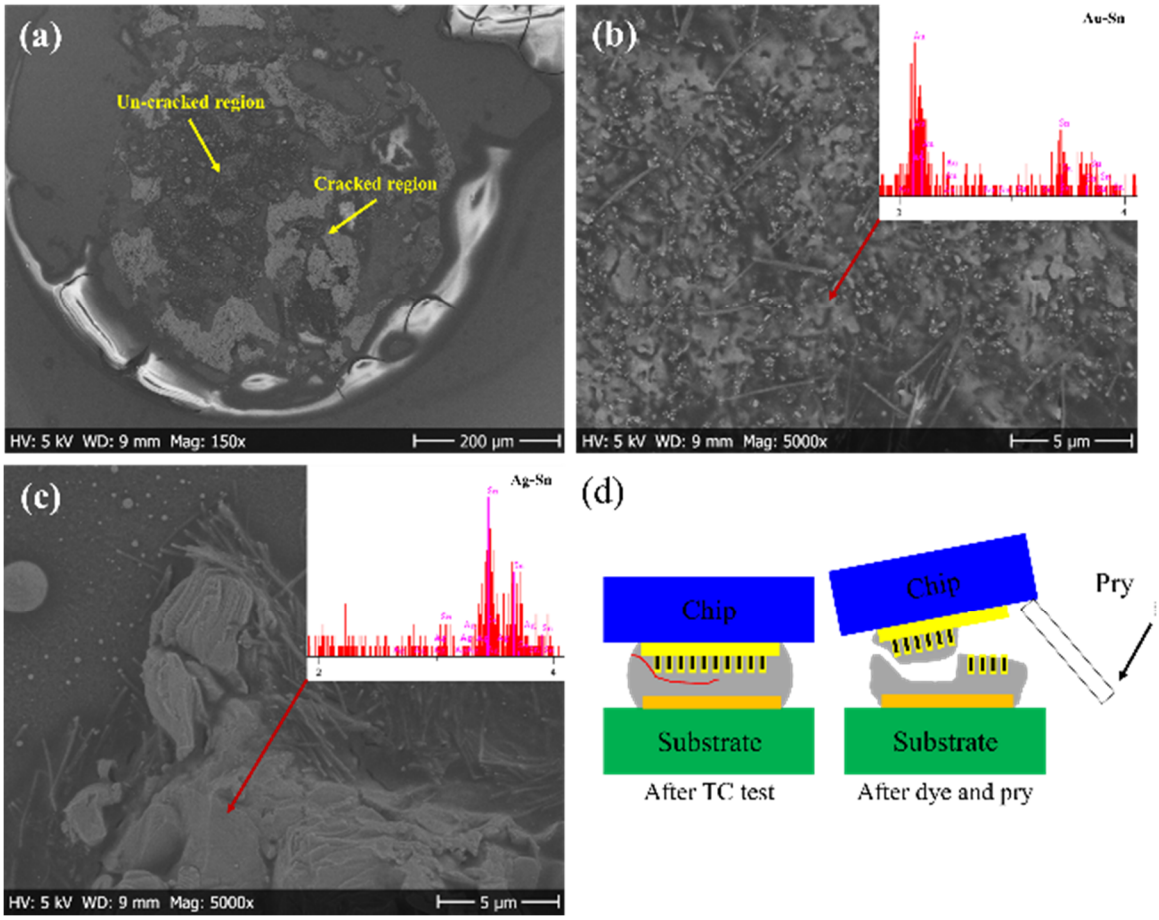


Figure 4.20: Fracture surface analysis of (a) chip side for VACNF/SAC305 sample, (b) and (c) close-up views of uncracked region and cracked regions in Figure 4. 20 (a) respectively, (d) schematic description of crack propagation.

The fracture surface on the substrate side is shown in Figure 4.21 (a). A large number of VACNFs can be found in the magnified image of the uncracked region as shown in Figure 4.21 (b). Most VACNFs in this region come from the chip side surface together with the SAC305 solder. In addition, we found some micro-cracks on the surface. Figure 4.21 (c) shows a close-up view of a micro-crack in which the VACNFs can be clearly observed

inside the SAC305 solder. In contrast to the uncracked region, only several VACNFs can be found in the cracked region as shown in Figure 4.21 (d) because most VACNFs still stayed on the chip side as we have mentioned before.

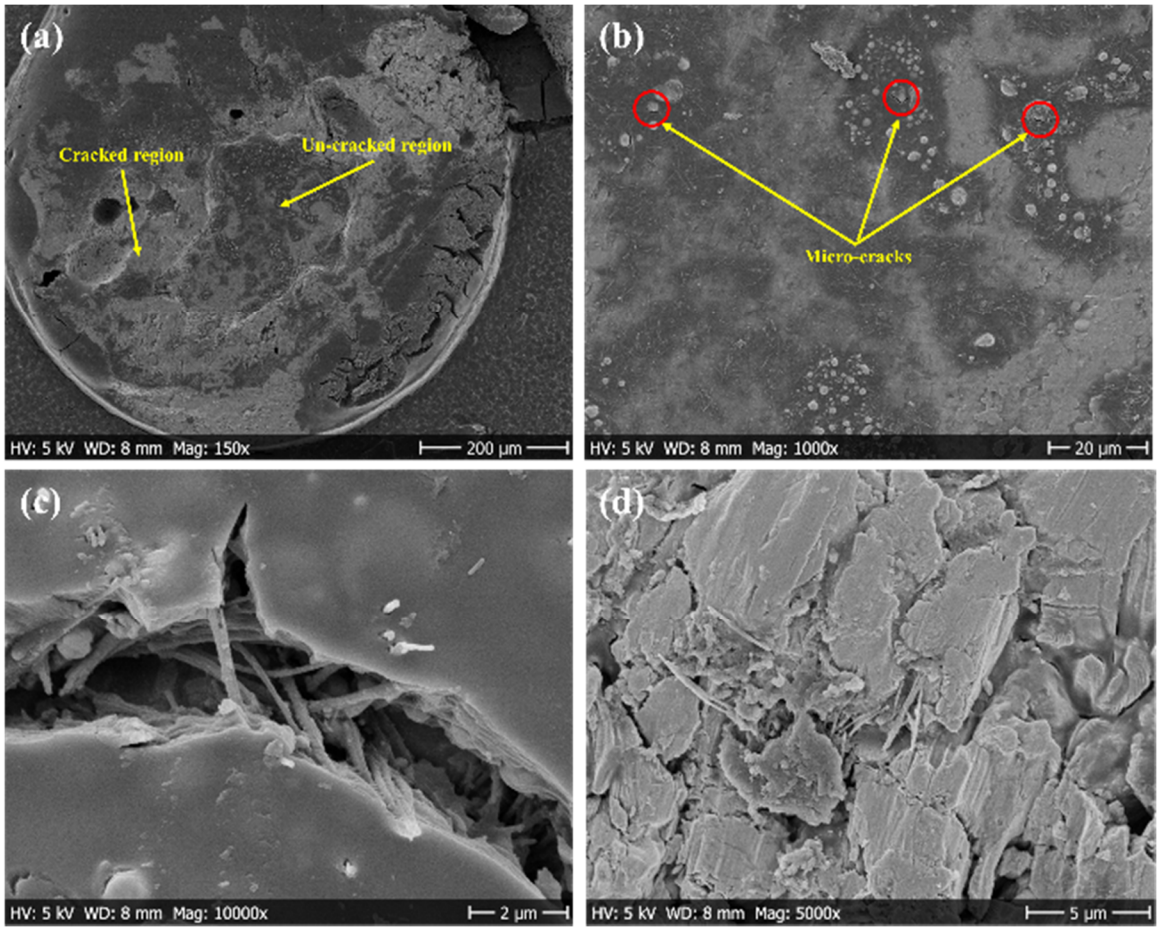


Figure 4.21: Fracture surface analysis of (a) substrate side for VACNF/SAC305 sample, (b) close-up view of uncracked region, (c) close-up view of micro-crack, and (d) close-up view of cracked region.

The SEM observation of the fracture surface of the SAC305 sample on the chip side was shown in Figure 4.22. The fracture surfaces of the SAC305 sample in the uncracked and cracked regions, shown in Figure 4.22 (b) and (c), are not as rugged as those of the VACNF/SAC305 sample. It reflects the fact that the crack propagation path in the solder joint of the SAC sample did not change significantly during the TC test. As a result, a straight crack path was presented, as per the description in Figure 4.22 (d), and which finally resulted in a shorter thermal fatigue life compared to the VACNF/SAC305 sample.

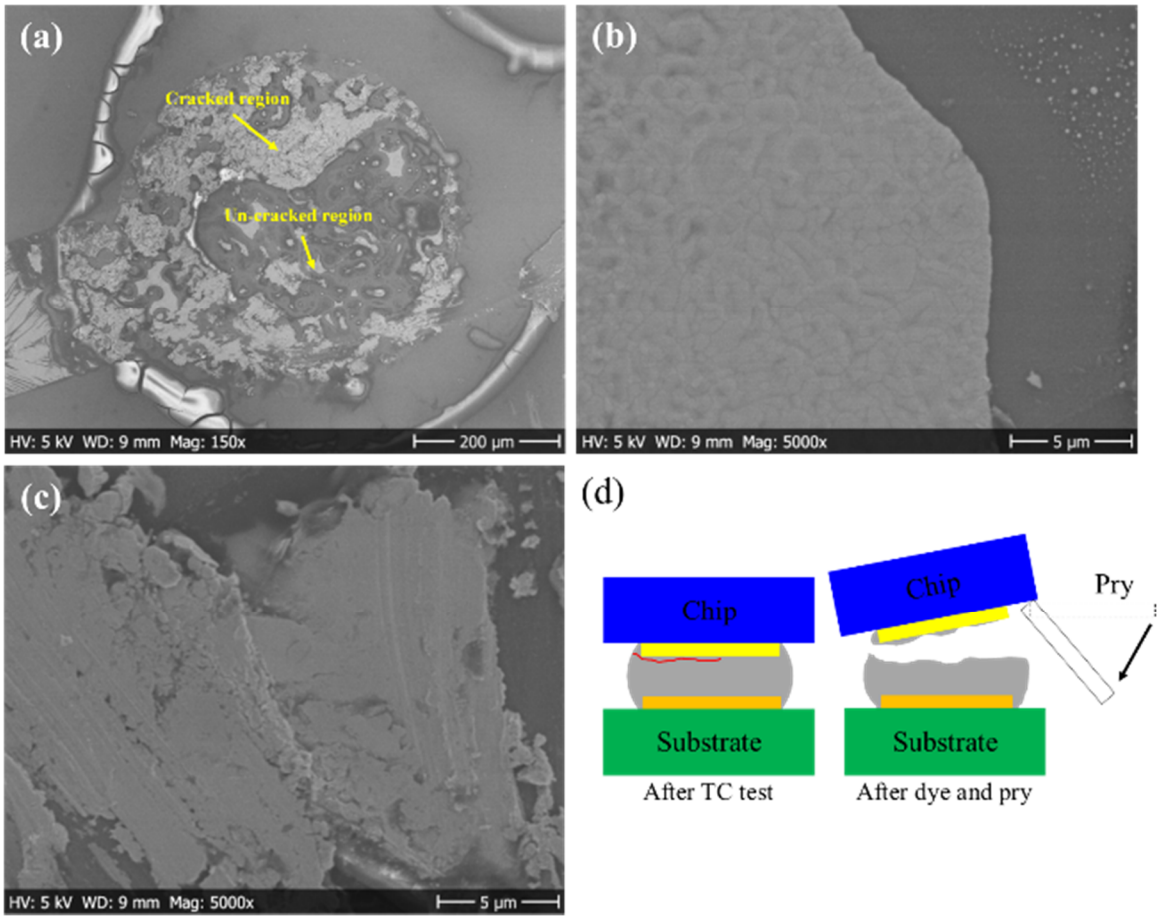


Figure 4.22: Fracture surface analysis of (a) chip side for the SAC305 sample, (b) and (c) close-up views of the uncracked region and cracked regions in Figure 4.22 (a) respectively, (d) schematic description of crack propagation.

In summary, during the TC test, the propagation of the cracks can be blocked when arriving the VACNF/SAC305 region. The cracks need to break or bypass the CNFs for further movement in the solder joint, which can delay the crack propagation and enhance the thermal fatigue resistance of the solder joint. Meanwhile, the cracks, initially generated in the VACNF/SAC305 region, whose growth can be limited by adjacent CNFs because these CNFs can prevent the formation of large cracks in the solder joint from small crack converging.

4.2 Nanocomposite solders

About twenty years ago, lead-free solders appeared in the electronics industry in order to replace toxic Sn-Pb solders. This substitution was regarded as a revolution of soldering industry. The materials, processes, and tests must be updated to meet the specifications of

lead-free solders. In Table 4.6, some commercial Sn-based lead-free solders are listed, in which Sn-Ag, Sn-In, and Sn-Bi systems have been widely used in the electronic industry, but the disadvantages of these lead-free solder systems still need to be addressed. One of possible solutions is to develop composite solders.

Table 4.6: Sn-based lead-free solder alloy systems.

System	*Advantage*	*Disadvantage*
Sn-Ag	Mechanical performance	High melting point
Sn-Cu	Economics	High melting point
Sn-Zn	Low melting point	Oxidation[65]
Sn-Bi	Low melting point	Brittleness[66]
Sn-In	Low melting point	High cost

Solders with intentionally incorporated reinforcements are termed composite solders [67]. The composite solder is a promising solder system, in which the reinforcements can effectively enhance the mechanical strength, increase the creep resistance, and stabilize the microstructure of solders. When the size of reinforcements decreases to the nanoscale, the composite solders can be called nanocomposite solders.

4.2.1 Literature review of nanocomposite solders

In the field of solder materials, various nanoparticles have been used for making nanocomposite solders as shown in Table 4.7. According to the type of nanoparticles, nanocomposite solders can be roughly divided into metallic and non-metallic nanoparticles reinforced nanocomposite solders. Metallic nanoparticles are usually more compatibility with solder matrix than non-metallic nanoparticles. However, the oxidation and coarsening issues are two major challenges of metallic nanoparticles. Compared to the metallic nanoparticles, non-metallic nanoparticles are more stable aspects of properties and structures, but the compatibility of non-metallic nanoparticles to solder matrix is not as good as metallic nanoparticles.

Table 4.7. Researches on nanocomposite solders (Since 2002)

Nanoparticles	*Matrix*	*Form*	*Improvement*
Metal			
Cu	Sn37Pb [68] [69]	Paste	Hardness, Strength, Creep
	Sn3.5Ag [70]	Bulk	Strength
	Sn3.5Ag [71]	Paste	Melting point, Wettability, Hardness
	Sn [72]	Bulk	Strength
Ag	Sn37Pb [73] [74]	Paste	Creep
	Sn0.7Cu [69]	Paste	Strength, Creep

	Sn9Zn [75]	Paste	Strength
	Sn3.0Ag0.5Cu [76]	Paste	Wettability
	Sn58Bi [77]	Paste	Electromigration
Al	Sn3.5Ag0.5Cu [78]	Paste	Strength, Microstructure
	Sn3.0Ag0.5Cu [79]	Paste	Microstructure, IMC layer, Hardness
Zn	Sn3.8Ag0.7Cu [80]	Paste	IMC layer
	Sn3.5Ag [81]	Paste	IMC layer
Mo	Sn3.8Ag0.7Cu [82] [83]	Paste	IMC layer IMC layer
Co	Sn3.8Ag0.7Cu [31] [32]	Paste	IMC layer, Microhardness
Sb	Sn9Zn [86]	Bulk	Microstructure, Strength
Ni	Sn3.8Ag0.7Cu [87]	Paste	IMC
Non-Metal			
TiO_2	Sn37Pb [88] [89]	Paste	Microstructure, Hardness, Creep
	Sn3.5Ag0.5Cu [90] [91]	Paste	IMC layer, Microstructure
	Sn3.5Ag0.5Cu [92]	Bulk	Microstructure, IMC layer, Strength
	Sn3.5Ag0.25Cu [93]	Bulk	Microstructure, Hardness, Strength
	Sn0.7Cu [94]	Paste	Microstructure, Strength
	Sn3.0Ag0.5Cu [95] [96] [97]	Paste	Microstructure, IMC layer, Hardness, Wettability
	Sn3.5Ag [98]	Bulk	Microstructure, Strength, IMC layer
Al_2O_3	Sn37Pb [89]	Paste	Creep
	Sn4In4.1Ag0.5Cu [99]	Bulk	Strength
	Sn0.7Cu [100]	Bulk	Strength
	Sn9Zn [101]	Paste	Microstructure, Strength, Hardness
	Sn3.5Ag0.5Cu [102]	Bulk	Microstructure, Wettability, Hardness
SnO_2	Sn3.5Ag [103]	Bulk	Hardness, Strength
$SrTiO_3$	Sn3.0Ag0.5Cu [104]	Paste	Microstructure, Strength
ZrO_2	Sn3.0Ag0.5Cu [105] [106]	Paste	Microstructure, IMC layer, Hardness, Strength
	Sn8Zn1Bi [107]	Paste	Microstructure, Hardness, IMC layer
FeO2	Sn3.0Ag0.5Cu [108]	Paste	Microstructure
ZnO	Sn57.6Bi0.4Ag [109]	Paste	IMC layer, Strength
SWCNT	Sn37Pb [110]	Bulk	Strength, Hardness
	Sn3.8Ag0.7Cu [59]	Bulk	Strength, Hardness
MWCNT	Sn3.5Ag0.7Cu [60]	Bulk	Wettability, Strength

The advantages of nanocomposite solders have been reported in many studies. According to the achievements listed in Table 4.7, the effects of nanoparticles on the solders are summarized in Figure 4.23 in which more than 70 % reports claimed that the mechanical strength of original solders can be enhanced by adding small amount of nanoparticles. Meanwhile, more than 50 % researchers found the refined microstructure in nanocomposite solders compared to original solders.

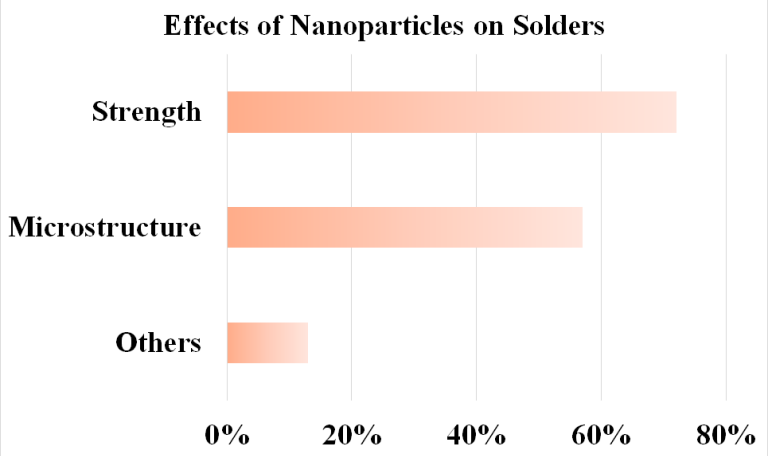


Figure 4.23: Statistic of nanoparticle effect on the solder

As we know, the mechanical strength of solders is closely related to the microstructures. Finer microstructure usually provides higher strength due to the lower speed of dislocation movement. Nanoparticles dispersed in the solder matrix is able to not only block the dislocation movement as secondary phase particles but also promote the formation of small grain size in solder matrix [90]. According to absorption theory, the nanoparticles can attach to the grain surface or boundary to decrease the surface activity and consequently limit the grain growth. In addition to absorption theory, increased nucleation sites provided by nanoparticles are another reason for the grain size decreasing [93], [104], [105].

Table 4.7 also provides the information about the form of nanocomposite solders. As final products, nanocomposite solders can be fabricated as paste or bulk. The paste is usually prepared by two mixing steps. The first step is to disperse nanoparticles into the low viscosity solder flux by using a high mixing speed, and the second step is to mix this nanoparticle/flux compound with large volume of microsized powder under a low mixing speed. For simplifying process, some researchers also directly add nanoparticles into the commercial solder paste to form nanocomposite solders. The bulk nanocomposite solder is generally produced by first mixing nanoparticles with microsized solder powder and then creating a bulk with sinter, extrusion or casting-cooling process. As far as the electronic packaging is concerned, the paste nanocomposite solder is more compatible with SMT.

Unfortunately, nanocomposite solders have not been fully accepted by industry due to some technical problems. For example, during the reflow process, nanoparticles are quite difficult to be kept in the original solder paste system. Plenty of nanoparticles are excluded from solders due to the property mismatch between nanoparticles and solder matrix. This exclusion issue could be also caused by an incompatible flux system. The nanoparticles could be regarded as impurities and removed from solder matrix by flux. This nanoparticle exclusion phenomenon has been mentioned in some studies [85], [111] and will undoubtedly impair the reinforcement effect of nanoparticles on the solder. Furthermore, this phenomenon can cause other problems, such as short circuit, contamination, voids, and head-in-pillow defects.

Another problem for nanocomposite solders is that the effect of nanoparticles on the thermal fatigue resistance of the solder joint is still unclear. In general, the nanoparticles dispersed in the solder matrix can delay the crack propagation and improve the thermal fatigue resistance. However, the nanoparticles sometimes also prompt crack initiation and decrease the thermal fatigue resistance due to the void, weak bonding, and large CTE mismatch between nanoparticles and solder matrix [62]. Therefore, the practical effect of nanoparticles on the thermal fatigue resistance is quite complex and strongly depends on the type and content of nanoparticles.

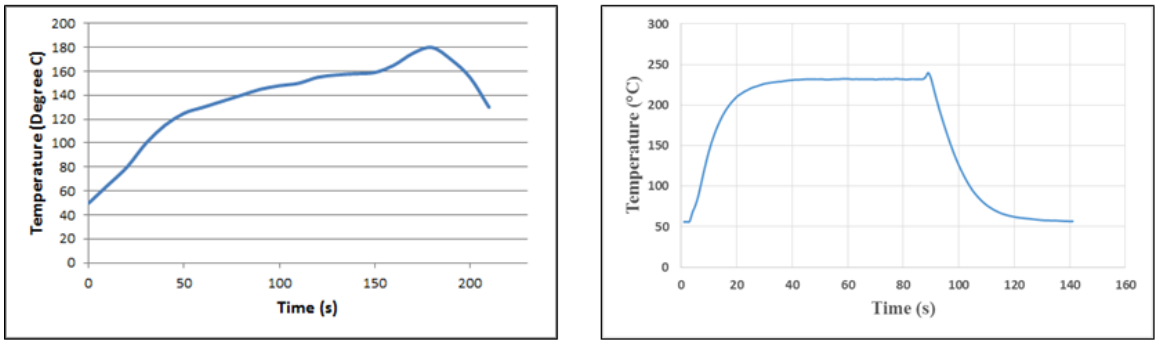
4.2.2 Two novel nanocomposite solders

Addressing on the challenges of nanocomposite solders, two novel nanocomposite solders were developed in this study. One of them consists of SAC305 nanoparticles and Sn58Bi solder matrix, which can be used as a low melting point lead-free solder in step soldering process. A major advantage of this nanocomposite solder is the good compatibility between nanoparticles and solder matrix. In addition, the melting point of SAC305 is 55 % higher than Sn58Bi, which can slow the nanoparticle growth during the reflow soldering process. Another nanocomposite solder is composed of Bi_2Te_3 nanoparticles and SAC305 solder matrix, which can be used as a high melting point lead-free solder. The density (7.6 $g \cdot cm^{-3}$) and CTE (17×10^{-6} K^{-1}) of Bi_2Te_3 [112] are quite close to that of the Sn-Ag-Cu alloy system (7.44 $g \cdot cm^{-3}$, 17.6×10^{-6} K^{-1}) [113], [114], which can provide potential benefit to controlling nanoparticle exclusion and improving thermal fatigue resistance. The experimental design and reflow profiles for two nanocomposite solders are shown in Figure 4.24.

Experimental Design

Nanocomposite Solder	Solder Matrix	Nanoparticles
SAC305/Sn58Bi	Sn-58Bi	Sn-3.0Ag-0.5Cu (1, 2, 3, 4 wt. %)
Bi2Te3/SAC305	Sn-3.0Ag-0.5Cu	Bi_2Te_3 (0.5, 1, 2 wt. %)

Soldering Reflow Profile for Nanocomposite Solder Paste



SAC305/Sn58Bi
Low Process Temperature

Bi2Te3/SAC305
High Process Temperature

Figure 4.24: Experimental design and reflow profiles for two nanocomposite solders

DSC analysis

The melting point, solidification, and composition of two nanocomposite solders were studied by using differential scanning calorimetry (DSC, Pyris 1, Perkin Elmer) after the reflow soldering process. The analysis results of SAC305/Sn58Bi and Bi_2Te_3/SAC305 nanocomposite solders are shown in Figure 4.25 and 4.26 respectively. In Figure 4.25, two endothermic peaks were observed on the DSC curve. The first peak appeared at 140 °C, which resulted from the melting of Sn58Bi. The second peak was present at 217.5°C, which was triggered by the melting of SAC305 nanoparticles. The latent heat of fusion (Delta H) value was shown beside each peak. The Delta H of SAC305 nanoparticles is 5.25 J/g, which agrees well with our previous work on Sn-Ag-Cu nanoparticles [33] and is 10 times smaller than microsized Sn-Ag-Cu solder alloy. It proves that SAC305 nanoparticles still retained in the solder system after the reflow soldering process.

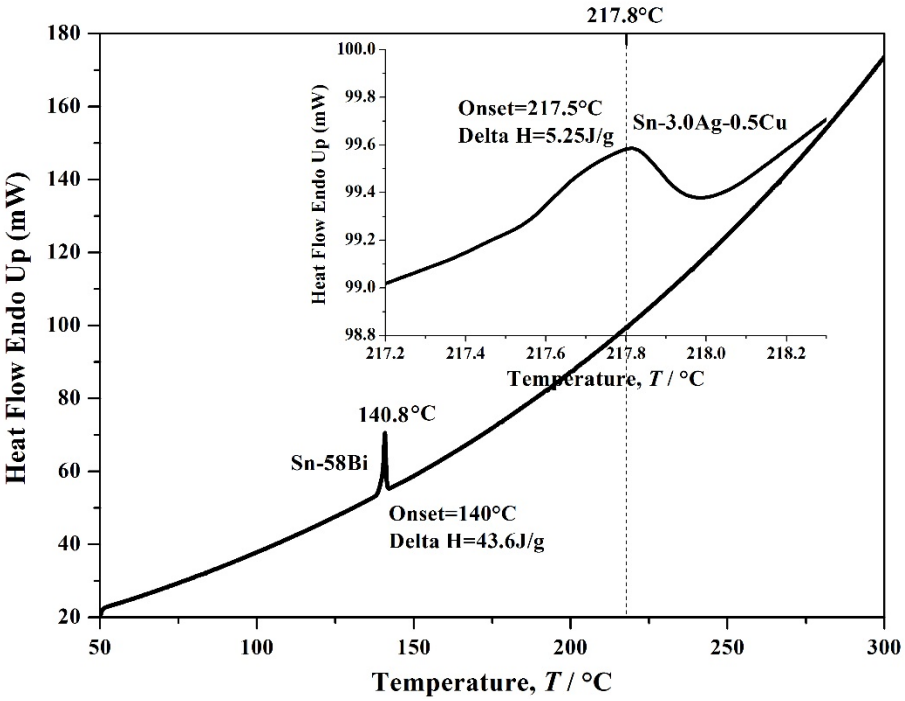


Figure 4.25: DSC curve of SAC305/Sn58Bi nanocomposite solder

In Figure 4.26, no melting point shift can be found after adding Bi_2Te_3 nanoparticles into SAC305 solder matrix. The onset melting temperature is 216.9 and 216.7 °C for the pure SAC305 and the nanocomposite solder respectively. In contrast to the melting process, the nanoparticles have a significant effect on the solidification process. The onset temperature of solidification for the nanocomposite solder is 199.6 °C which is 7.6 °C higher than the pure SAC305 solder (192 °C). Therefore, the undercooling of the pure SAC305 was reduced 7.8 °C by adding 1 wt. % Bi_2Te_3 nanoparticles. The reduced undercooling could be caused by the nanoparticles being dispersed in the SAC305 solder which provides extra nucleation sites and promotes the solidification process. The decreased undercooling after the addition of nanoparticles is also reported by Xu et al. for the case of a FeCo/SAC305 nanocomposite solder [108].

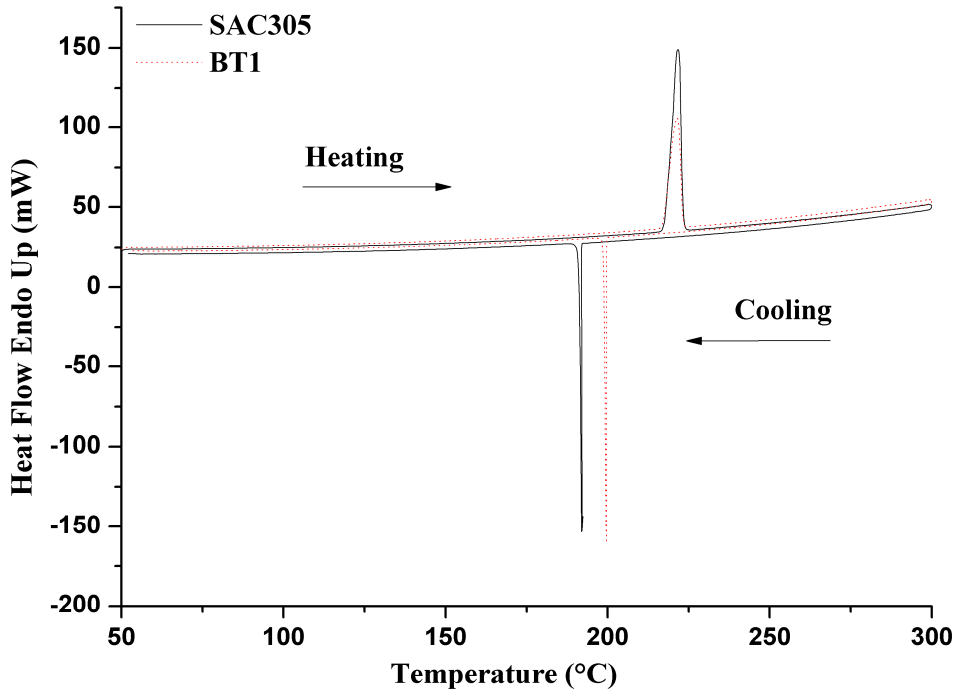


Figure 4.26: DSC measurement for SAC305 and 1 wt. % Bi_2Te_3/SAC305 solder.

ICP-MS analysis

An inductively coupled plasma-mass spectrometry (ICP-MS) device was employed to measure the content of the nanoparticles in the Bi_2Te_3/SAC305 solder bump after the reflow soldering process. The measured surface is located in the middle of the solder bump, and the test was repeated at four different points for each sample. Figure 4.27 shows that the content of the Bi_2Te_3 in the solder after the reflow process increases linearly with the addition of the Bi_2Te_3 nanoparticles. The Bi_2Te_3 content is 0.4 wt. % after the reflow soldering process for 0.5 wt. % nanocomposite solder, in other words, 80 % Bi_2Te_3 is retained in the solder. However, it should be noted that the percentage loss of nanoparticles increased to about 50 % when 1 wt. % of Bi_2Te_3 nanoparticles were added. Furthermore, the increased addition of Bi_2Te_3 nanoparticles resulted in a larger deviation in Bi_2Te_3 content in the solder after reflow. Potential causes for the large deviation in Bi_2Te_3 content include severe nanoparticle agglomeration and non-uniform distribution.

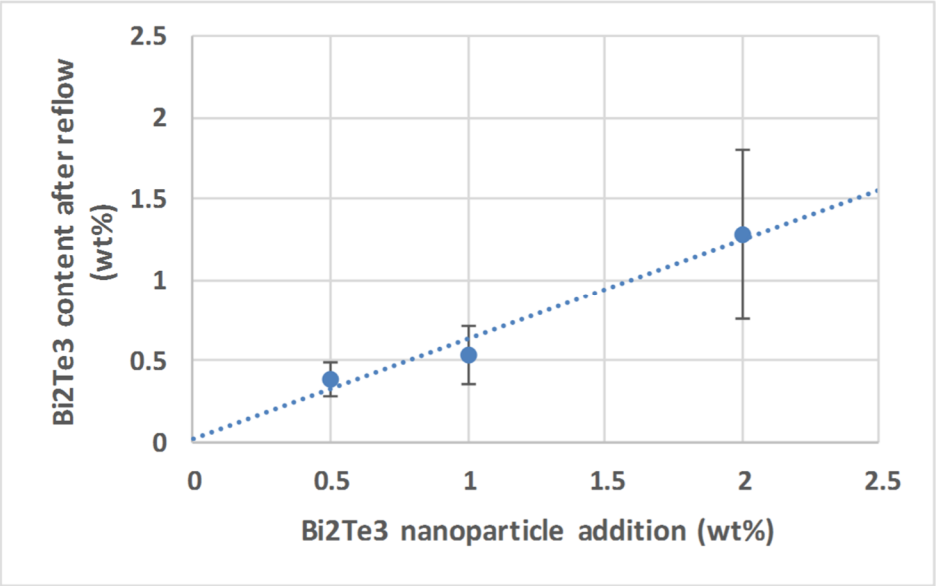


Figure 4.27: Measurement of Bi_2Te_3 content in the solder after reflow soldering.

Microstructure

The microstructure of SAC305/Sn58Bi and Bi_2Te_3/SAC305 nanocomposite solders with 1 wt. % nanoparticles are shown in Figure 4.28 and 4.29 respectively. In Figure 4.28, the typical eutectic Sn58Bi microstructure consisted of fine alternating lamellae of two constituent phases was observed. Compared to pure Sn58Bi solder, more nanosized particles were presented in Sn rich area of the nanocomposite solder. These extra nanosized particles should be contributed from SAC305 nanoparticles.

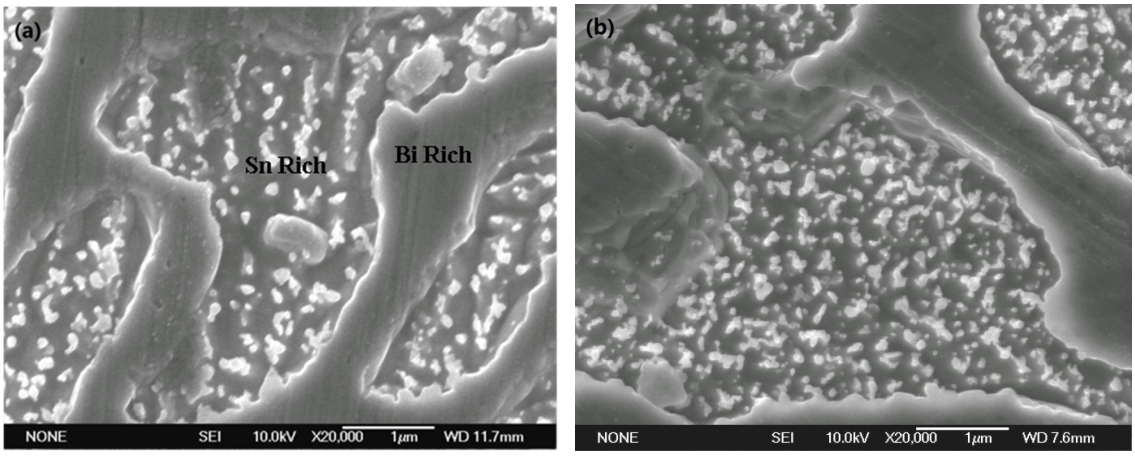


Figure 4.28: SEM observation on the cross-section of pure Sn58Bi solder (a) and nanocomposite solder with 1 wt. % nanoparticles (b).

The cross-section of Bi_2Te_3/SAC305 solder was shown in Figure 4.29. The Sn dendrite and Ag_3Sn/Sn eutectic area can be clearly distinguished from the images of all samples. In comparison to the pure SAC305 solder, Bi_2Te_3/SAC305 solders have finer microstructure in which circular and small Sn dendrites were present. It could be attributed to the aforementioned increase in nucleation sites and reduced undercooling caused by the addition of nanoparticles. It is known that Sn dendrites will form and grow rapidly during the solidification process, and the growth velocity of the Sn dendrites has an exponential relationship with the undercooling [115]. In this study, owing to the extra nucleation sites provided by the nanoparticles, the solidification process of the nanocomposite solder is faster than that of pure SAC305 solder, which shortens the growth time of Sn dendrites and results in smaller Sn dendrites.

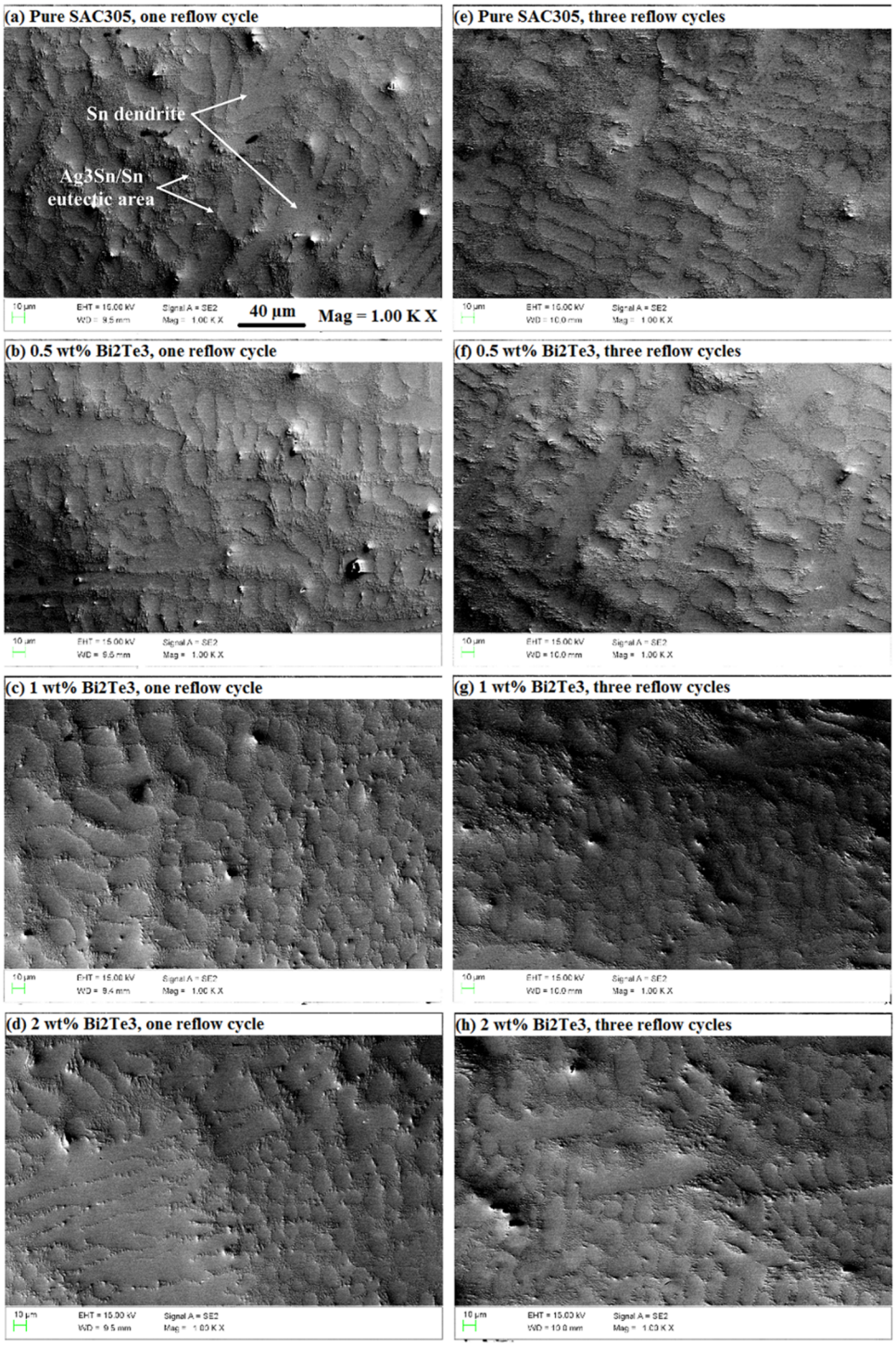


Figure 4.29: Cross-section images of pure SAC305 and Bi_2Te_3/SAC305 solder bumps after one (a-d) and three (e-h) reflow cycles.

In addition to the microstructure, the IMC layers of Bi_2Te_3/SAC305 solder joints were also observed with SEM. In order to make the IMC boundary clear, the cross-section of solder joints were etched in 5 % HCl acid for 10 seconds. Figure 4.30 shows the cross-section formed in all of the samples. After one reflow cycle, there are no obvious differences in IMC layer thicknesses between the pure SAC305 solder and the nanocomposite solders. However, after three reflow cycles, the IMC layer was found to have grown in all of the samples, but the layer thicknesses of nanocomposite solders were thinner than that of the pure SAC305.

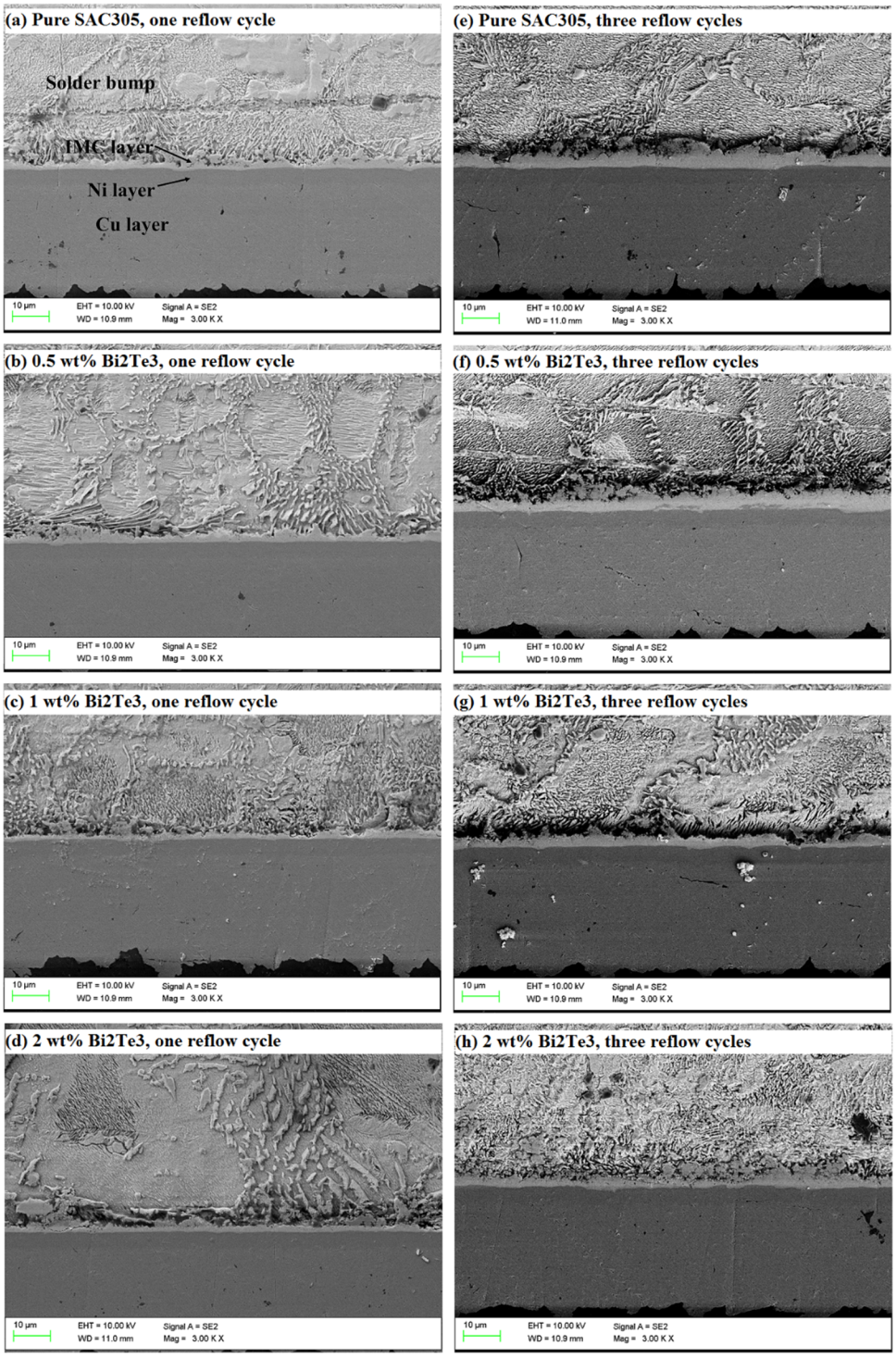


Figure 4.30: Cross-section images of pure SAC305 and Bi_2Te_3/SAC305 solder joints at the interface between solder bump and ENIG/Cu pad after one (a-d) and three (e-h) reflow cycles.

Figure 4.31 shows the measurements of the IMC layer areas after one and three reflow cycles. In the figure, the IMC areas of the nanocomposite solders are smaller than that of pure SAC305 solder. After three reflow cycles, the nanoparticles have a noticeable suppression effect on the IMC layer growth. The IMC layer area of nanocomposite solders is 40 % smaller than that of pure SAC305 solder when the content of nanoparticles reaches and exceeds 1 wt. %. It is known that the IMC layer is formed by the reaction between liquid solder and metallic pad at the interface during the soldering process. The metallic atoms from the pad diffuse through the IMC layer and keep reacting with the liquid solder, which leads to the growth of IMC layer. In this study, the Bi_2Te_3 nanoparticles near the interface reduce the reaction area, blocking the diffusion of metallic atoms from the pad, and subsequently results in a thinner IMC layer. This phenomenon has been well described in the literature, for example, for the interfacial reaction between Mo nanoparticles and Sn-3.8Ag-0.7Cu [82].

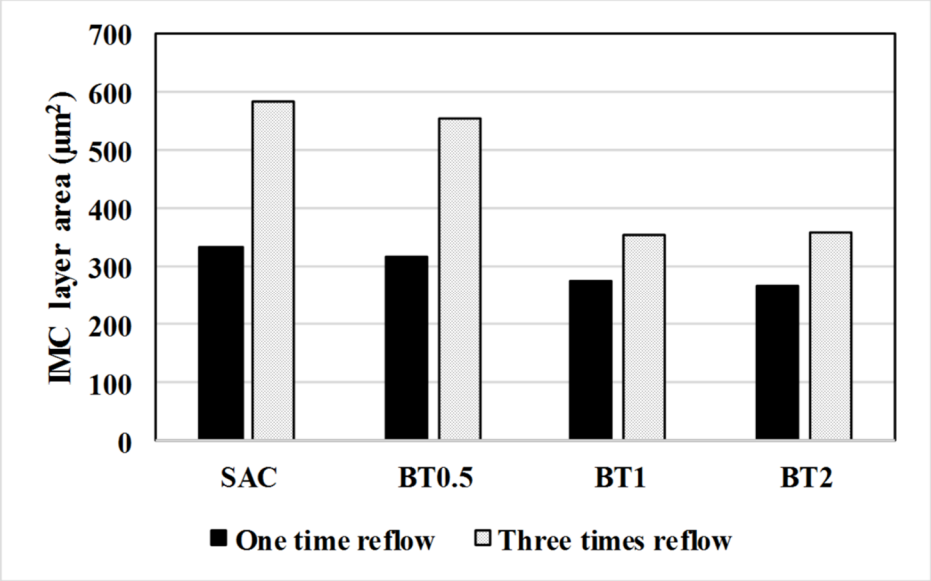


Figure 4.31: Measurement of IMC layer area.

TEM was used to observe the microstructures of nanoparticles and nanocomposite solders. In Figure 4.32, the average diameters of SAC305 and Bi_2Te_3 nanoparticles are both smaller than 50 nm. However, both of nanoparticles grew to 100 - 200 nm in diameter after the reflow soldering process, which could be caused by the grain coarsening or the reaction between nanoparticles and the solder matrix. For example, part of Bi_2Te_3 nanoparticles have reacted with SAC305 lead-free solder during the soldering process and formed Sn-Te IMC, which has been proven by X-ray diffraction (XRD) and EDX analysis. Besides nanoparticles, Figure 4.32 also shows some dislocation arrays, the movement of which was stopped by the nanoparticles dispersed in the solder matrix.

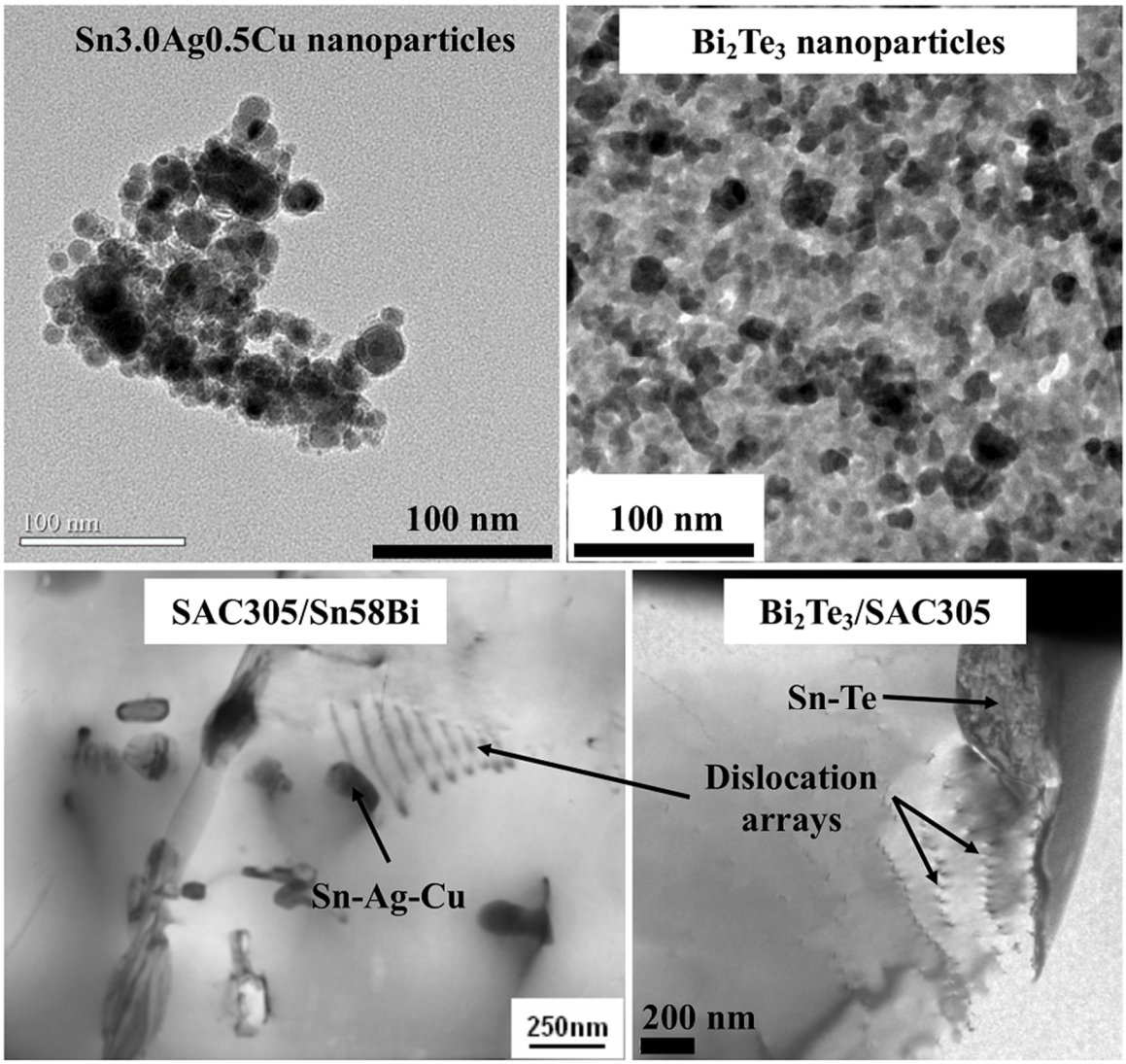


Figure 4.32: TEM observation of nanocomposite solders

Shear Strength

The shear strength of both lead-free solders can be increased by adding small amount of nanoparticles as shown in Figure 4.33. The enhanced shear strength can be explained by the dispersion strengthening theory, for which the nanoparticles dispersed in the solder matrix can impede the motion of dislocations during the shear test.

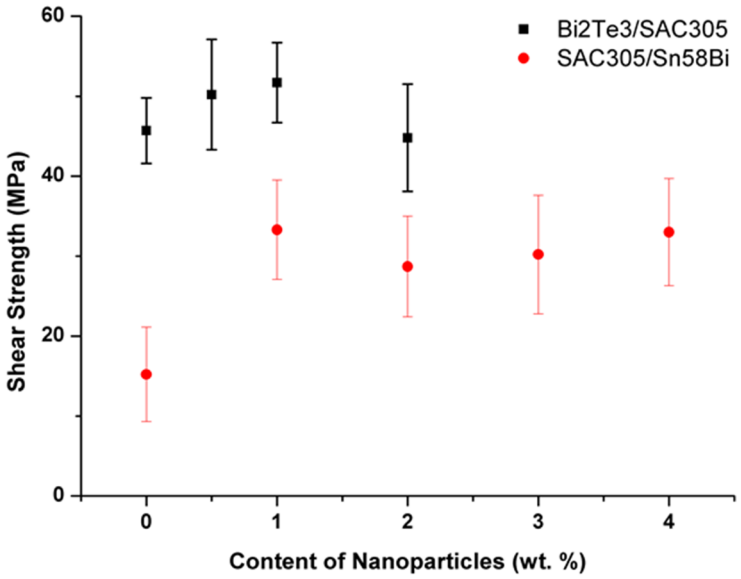


Figure 4.33: Relationship between shear strength and content of nanoparticles

However, the shear strength appears to stop further increase from adding more than 1 wt. % of nanoparticles, which could be caused by increased voids in the solder matrix. According to the results of X-ray detection on Bi_2Te_3/SAC305 nanocomposite solders as shown in Figure 4.34, the increasing of nanoparticles causes an increase of the void content, which offsets the reinforcement effect of nanoparticles and decrease the shear strength of solder joints. The increase of void rate should be caused by the increase of entrapped flux, the outgassing of entrapped flux is directly responsible for the formation of major voids, and a lower void content means a smaller amount of entrapped flux [116]. In the nanocomposite solders, the nanoparticles block the outgassing of flux in the reflow soldering process and subsequently increase the entrapped flux. Therefore, the content of nanoparticles must be controlled in certain level. In this thesis, a degradation of the shear strength was observed in both nanocomposite solders when the content of nanoparticles reached 2 wt. %. The recommended content of nanoparticles in the solder matrix is therefore in the range of 0.5 to 1 wt. %.

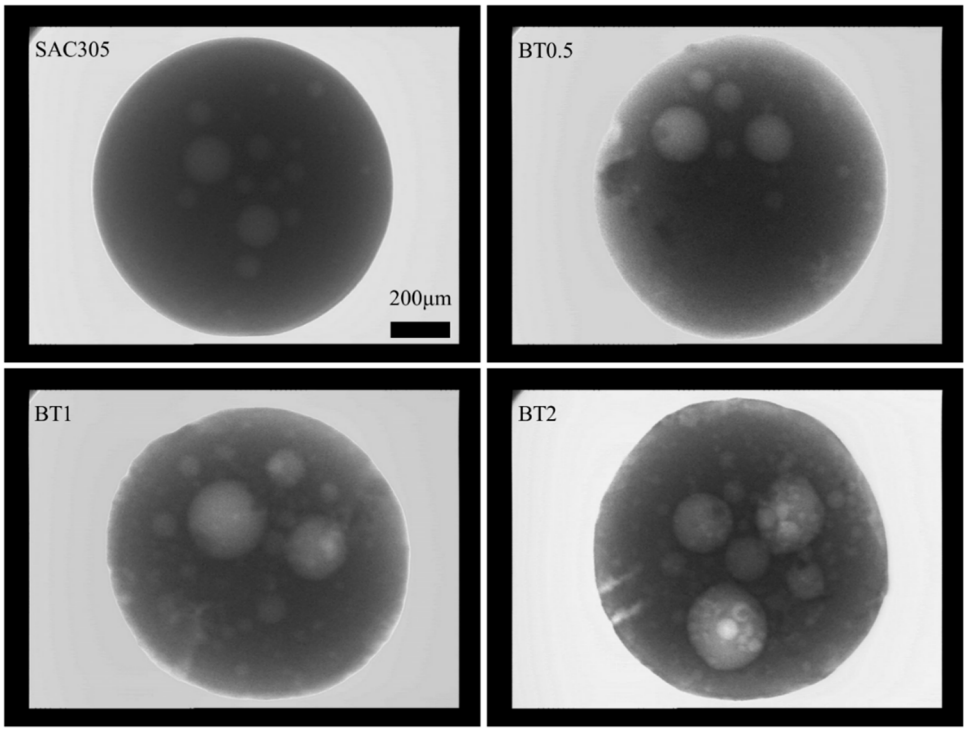


Figure 4.34: X-ray inspection images of solder bumps with nanoparticle content of 0, 0.5, 1, and 2 wt. % respectively.

Thermal fatigue

Thermal fatigue is a major failure mode for solder joint. The temperature variation caused by switch on/off or atmosphere change can make stress increased in the solder joint due to CTE mismatch between different materials. Thermal fatigue failure could be more serious in nanocomposite solders than pure solders due to the CTE mismatch between nanoparticles and solder matrix which causes the stress to concentrate at the nanoparticle/solder interface. If the bonding strength between the nanoparticles and solder matrix is insufficient, an initial crack will be formed at the interface during thermal cycling test, which will reduce the solder joint reliability. Therefore, the thermal cycling test is an essential step in quantifying the thermal fatigue resistance of the nanocomposite solder.

The test board for TC test is shown in Figure 4.35. Each board includes fifty chip resistors, namely one hundred solder joints. The contact resistances of each SAC305/Sn58Bi solder joint was measured outside the thermal cycling chamber with four probe method at room temperature after 260, 320, 380, 440, 500 cycles. For Bi_2Te_3/SAC305 nanocomposite solder, the entire circuit resistance of the test board was monitored by using an Agilent 34972A Data Acquisition system during the thermal cycling test until 1000 cycles.

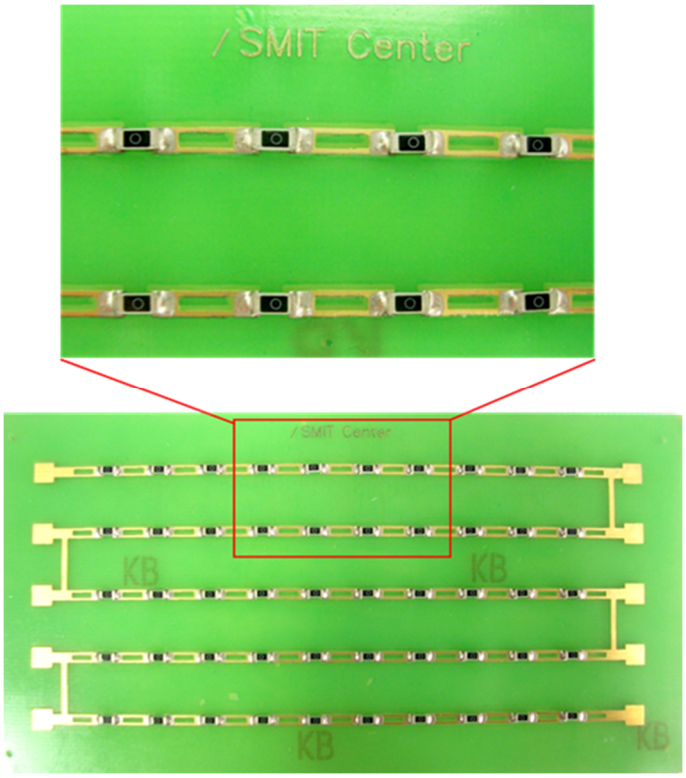


Figure 4.35: Test board for thermal cycling test.

Figure 4.36 shows the variation of electrical resistance of solder joints during the thermal cycling tests. Both nanocomposite solders survived after thermal cycling test (failure criterion: R > 1000 Ω), showing a promising thermal fatigue resistance, which is attributed to the good compatibility of nanoparticles to the solder matrix as well as the fine microstructure of nanocomposite solders.

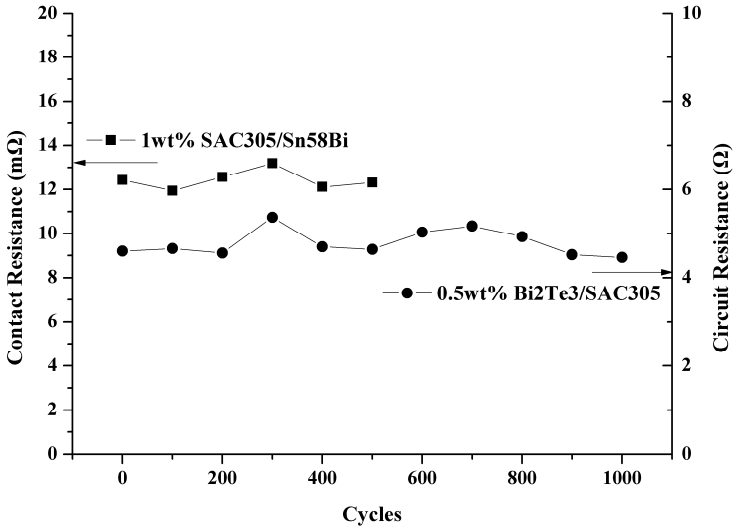


Figure 4.36: Variation of electrical resistance during thermal cycling test.

Chapter 5 Thermal Management

Thermal management is a critical part for designing electronic devices as the performance of a device can be significantly affected by its work temperature. For example, the reliability of circuits (transistors) is exponentially dependent on the operating temperature of the junction. Only 10 - 15 °C temperature rising can result in the half decreasing of device lifetime. In addition to the lifetime, the operating speed of the microprocessor also related to the operating temperature. At lower operating temperatures, microprocessors can operate at higher speeds due to reduced gate delay [117]. However, with the increasing of power density of ICs and miniaturization of packaging dimension, it is extremely hard to control the operating at low temperature. According to the report from ITRS 2012, the maximum junction temperature is still as high as 100 °C, and this high temperature will be kept in future 10 years. In 3D packaging structures, the problem of thermal management is more severe than normal structures due to the complex structure and high packaging density.

Currently, there are two major urgent issues related to the heat dissipation of 3D packaging structures. One is the various interfaces in the structure, such as Si chip/IHS interface or IHS/heat spreader interface. The high thermal resistance at the interface caused by surface roughness can significantly reduce the efficiency of heat transfer, and therefore have been identified as one of the main bottlenecks for developing high power devices [9]. In order to reduce the thermal resistance at the interface, one of effective solutions is to fill the gap between two surfaces by using thermal interface materials, as shown in Figure 5.1.

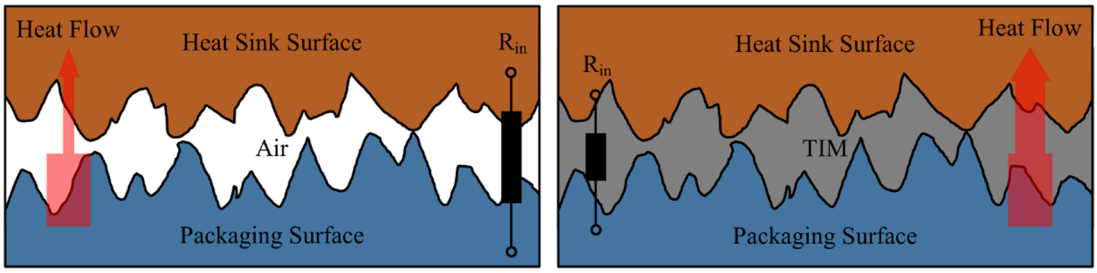


Figure 5.1: Effect of TIM at the interface between heat sink and packaging.

In recent years, a variety of TIMs have been developed and reported. Figure 5.2 lists several popular TIMs in recent market and their thermal conductivity [118]. In the figure, indium shows a huge advantage of thermal conductivity compared to grease, gel, or phase change non-metallic TIM, the thermal conductivity of indium TIM can be as high as 86 W/m·K. However, soft indium together with its large CTE mismatch to Si chip and Cu heat sink lead to a potential risk to the bonding strength and system thermal fatigue resistance.

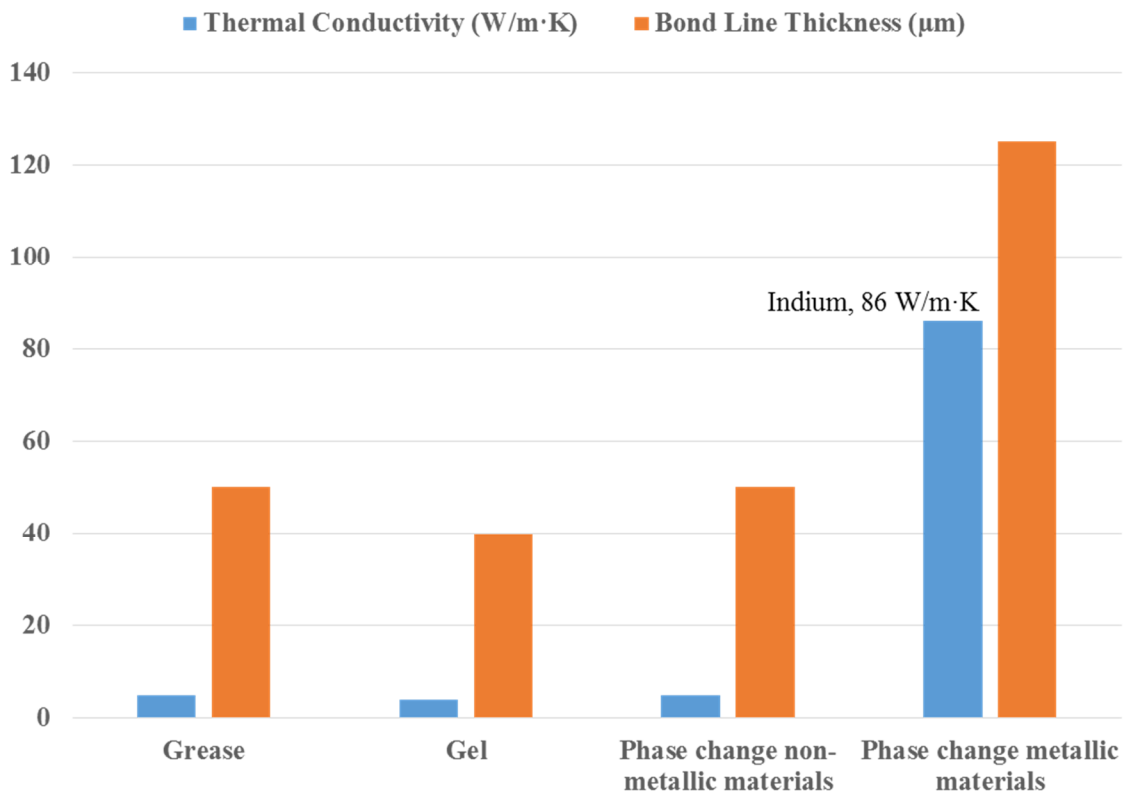


Figure 5.2: Thermal conductivity and bond line thickness of several TIMs.

Addressing the weakness of indium, a novel nanocomposite thermal interface material (Nano-TIM) will be presented in this chapter. This TIM consists of metallic indium and a silver coated polyimide (PI) network. The polymer network defines the geometry of TIM, such as the shape and bond line thickness. Meanwhile, the metallic part is responsible for heat transfer.

Another urgent issue on 3D packaging structures is related to hotspots which are generally caused by the non-uniform power distribution on ICs and complex packaging structures. The temperature of hotspots can be much higher than the average temperature of whole system. Therefore, the overall reliability of devices is typically constrained by the hotspots on the ICs rather than the average temperature [119]. One of the solutions to promote the heat dissipation at the hotspots is using thermoelectric coolers, which can be put on the top of hotspots and pump the heat actively from the hotspots to the TIM, IHS and heat sink. A typical structure of TE cooler is shown in Figure 5.3. It usually consists of alternative n- and p-type TE legs and two ceramic substrates. Once the current goes through the TE legs, the heat can be pumped from one side to another, forming a temperature difference between two sides.

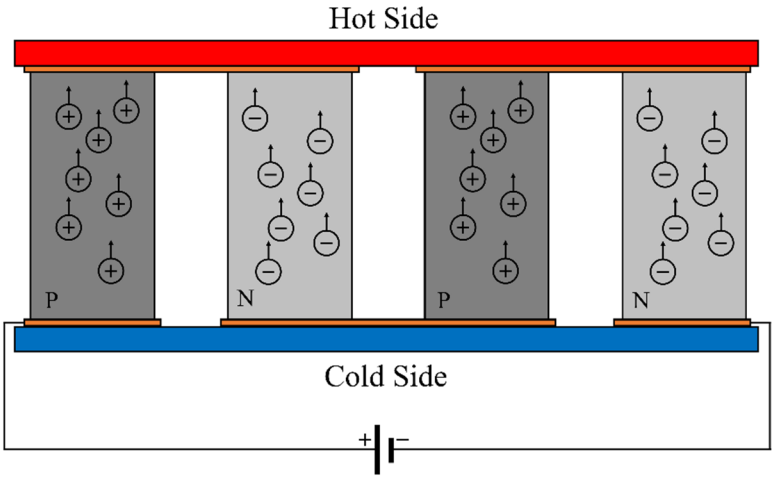


Figure 5.3: Schematic picture of a TE cooler.

The efficiency of a TE cooler is evaluated by a dimensionless figure of merit (ZT value) which is defined as:

$$ZT = \frac{S^2 \sigma}{k} T$$

where S is the Seebeck coefficient, σ is the electrical conductivity, k is the thermal conductivity, and T is the average temperature between hot and cold surfaces. Currently, Bi_2Te_3 and its alloys have been regarded as one of the best TE materials because of high ZT value at the room temperature [120]. Actually, the ZT value of bulk Bi_2Te_3 based materials had been limited at 1 for decades until introducing nanomaterials in TE materials. According to the report, by hot-pressing p-type Bi-Sb-Te nanopowders fabricated with ball-milling method, the ZT value of 1.2 was achieved at 25 °C. The nanostructured materials can effectively scatter the phonons at the boundaries, decrease lattice thermal conductivity, and consequently increase the ZT value [121]. In recent years, plenty of studies have demonstrated that the utilization of nanotechnology can improve the performance of Bi_2Te_3 based TE materials [122], [123], [124].

Although the performance of TE materials has been improved with nanotechnology, the productivity of Bi_2Te_3 based nanopowders is still a bottleneck for industry application. Therefore, a low cost and high productivity fabrication process was developed in this study. By using Bi_2Te_3 nanopowders prepared with the new process, a silver alloyed nanostructured n-type Bi_2Te_3 TE bulk material was developed as a demonstrator.

5.1 Metal matrix nanocomposite thermal interface material for passive heat dissipation

Sample preparation

The processes of the Nano-TIM preparation can be shown in three steps. First, the PI network was fabricated by using electrospinning technology. Secondly, Ag was coated on the surface of the fibers in the network. Finally, the liquid indium was infiltrated in this Ag coated PI network by using an infiltration machine. The fabrication processes and thermal measurement methods were developed by Dr. Björn Carlberg and Dr. Carl Zandén in our group. The detailed description about processes and measurement methods could be found in their Ph.D thesis and publishes [125], [126]. In this thesis, the work is focused on the mechanical performance evaluation and the practical application of Nano-TIM as die-attach materials.

Ag-coated PI network and a piece of Nano-TIM are shown in Figure 5.4 (a) and (b) respectively. The average diameter of the fibers is 895 ± 175 nm. After the infiltration process, the fibers are covered by indium, being invisible from the top surface. The thickness of Nano-TIM can be controlled during infiltration process. In this study, 50 µm Nano-TIM was selected and used for mechanical tests.

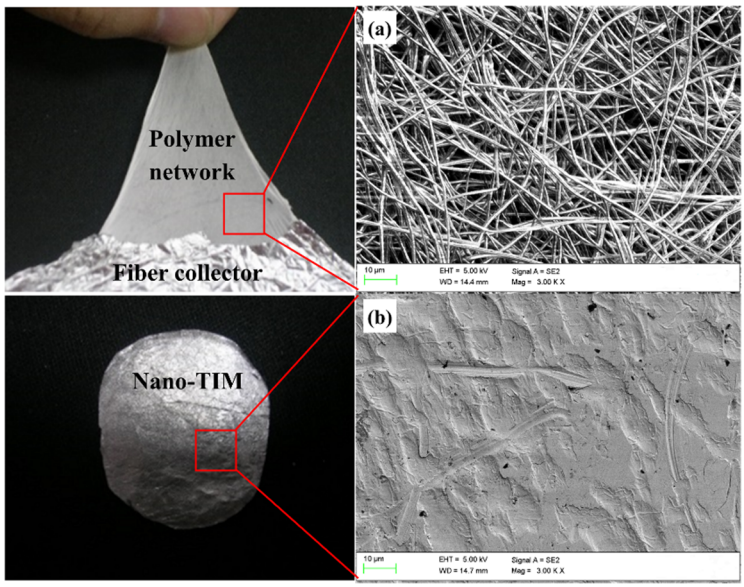


Figure 5.4: (a) PI network formed with electrospinning process and (b) a piece of Nano-TIM fabricated with infiltration process.

In this study, different sample structures and setups were designed for different tests. Figure 5.5 (a) shows a sandwich structured sample for shear test. A piece of Nano-TIM was firstly

placed on a Cu pad with ENIG surface finish. A 2 × 2 mm Si chip with Ti/Au (20/100 nm) surface finish was then pressed on the Nano-TIM at 180 °C with 0.4 MPa of pressure for 1.5 minutes. After that, this sandwich structure was cooled down to the room temperature in the air. The shear test on this sandwich structure was executed by using a DAGE-4000PSY shear tester. The shear speed and height were set at 200 µm/s and 100 µm respectively. In order to evaluate the effect of the fibers on the Nano-TIM, pure indium TIM was also tested with the same sample geometry. Finally, 10 samples were prepared and tested for both materials.

Figure 5.5 (b) shows the sample structure of thermal interface resistance measurement. A piece of Nano-TIM was sandwiched between two 8 × 8 mm^2 Cu/ENIG pieces and reflowed with the same processes as shear test sample. The pure indium samples were prepared as reference. In total 4 samples were prepared for each case. The thermal interface resistance was measured by using a commercial xenon flash instrument (LFA447, Netzsch).

The heat dissipation effect of Nano-TIM was investigated by using a thermal infrared (IR) camera. The test setup is shown in Figure 5.5 (c). The power chip with a hot spot was attached onto a copper heat sink with TIM materials. The IR camera was then used to test the heat spreading map of the power chip with 10 W loading. The hotspot temperature and heat distribution of the power chip were captured by IR camera after the samples stabilized at the thermal equilibrium for 2 min.

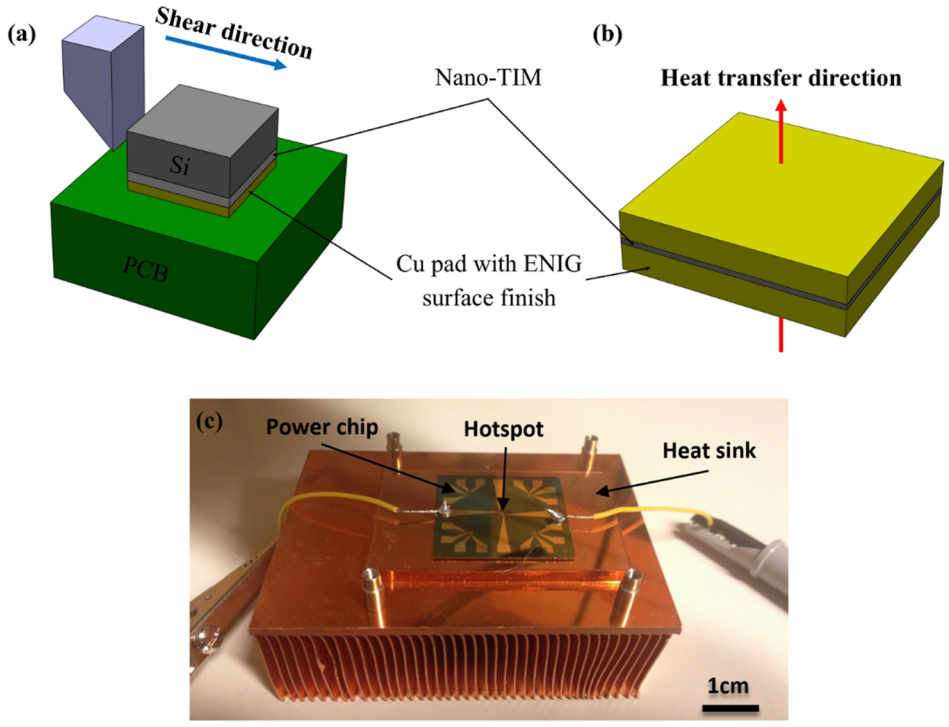


Figure 5.5: Sample structures for (a) shear test, (b) thermal interface resistance measurement, and (c) thermal infrared test.

Microstructure

Figure 5.6 (a) shows the cross-section of pure indium at the interface between the TIM and Cu/ENIG pad. No special objects can be observed in the indium matrix except some Si pieces which are formed during the cross-section making process. In Figure 5.6 (b), the polymer fibers can be observed in the indium matrix. There are no visible voids that can be detected in the figure, indicating that the porous polymer network has been completely filled with indium after the infiltration process. In general, the porous PI network is extremely difficult to be fully wetted and filled by metallic materials due to the inert nature of PI and the narrow gap between the PI fibers. However, Nano-TIM presented in this study was coated by silver which can significantly improve the wettability of liquid indium to the PI surface.

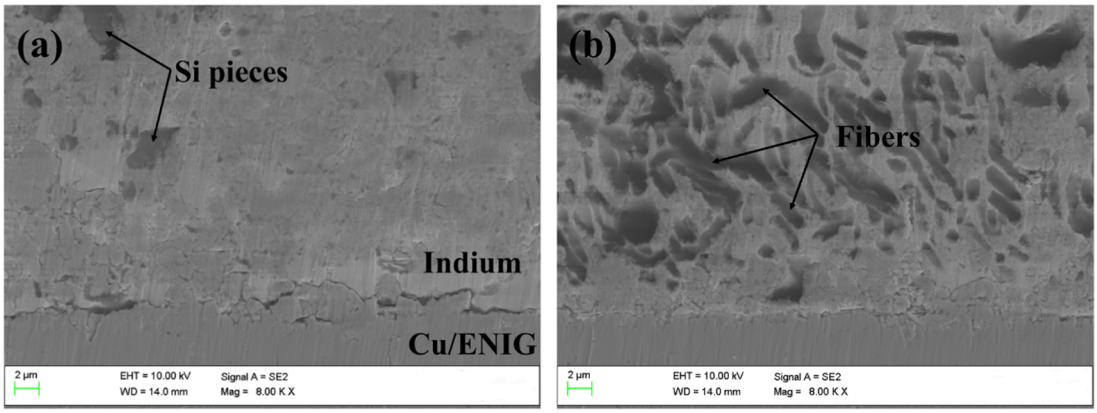


Figure 5.6: Cross-sections of (a) pure indium and (b) Nano-TIM with Cu/ENIG pad.

Shear test

Figure 5.7 shows the results of shear test for Nano-TIM and pure indium samples. The average shear strength of Nano-TIM is 15 % higher than that of pure indium, which could be attributed to the reinforcement effect of Ag coated PI fibers. The dislocation movement in the Nano-TIM was impeded by those Ag coated fibers, which limits the crack initiation and propagation during shear test and subsequently increases the shear strength of pure indium.

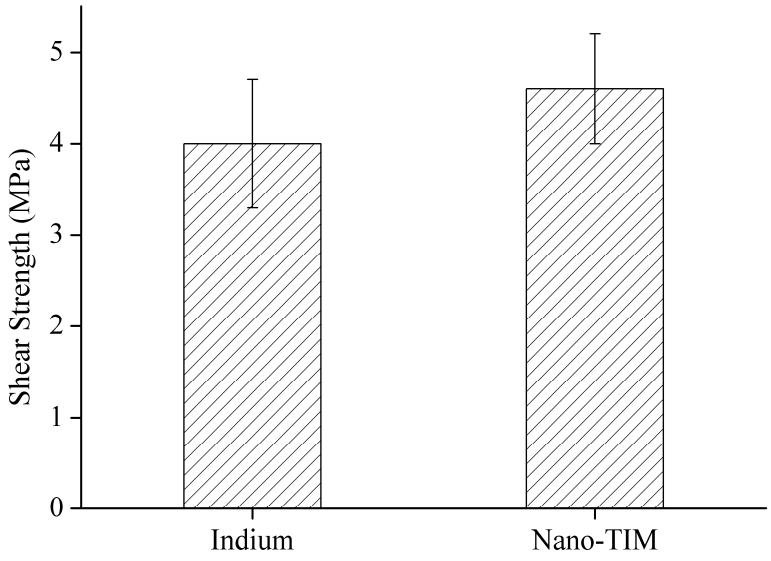


Figure 5.7: Results of shear test

Figure 5.8 shows the fracture surface after the shear test. The fracture surface of pure indium in Figure 5.8 (a) is composed of dimples, showing a typical ductile fracture mode. In Figure 5.8 (b), the fracture surface of Nano-TIM also shows the ductile fracture mode, but the microstructure is much finer than that of pure indium. Compared to the pure indium, the dimple size and elongation of the Nano-TIM is much smaller, which could be caused by the PI network.

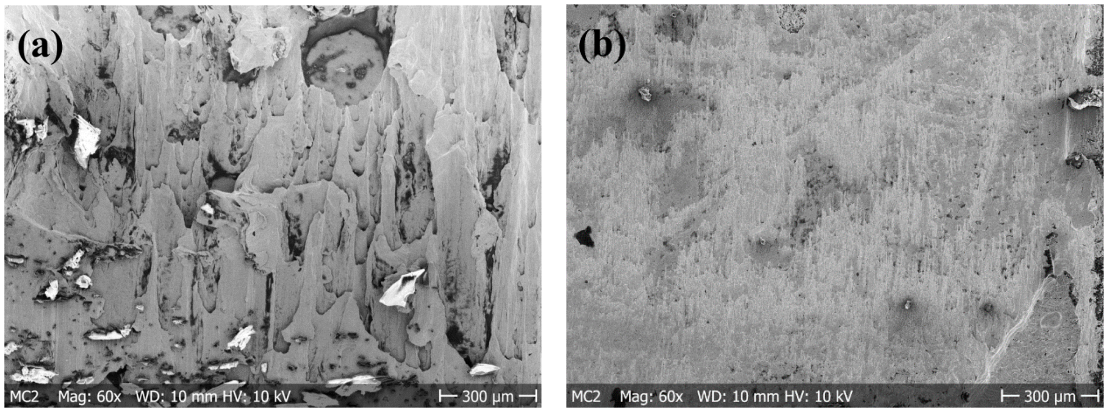


Figure 5.8: Fracture surface of (a) pure indium and (b) Nano-TIM after shear test.

Thermal interface resistance measurement

Figure 5.9 shows the measurement result for pure indium TIM and Nano-TIM. The average thermal interface resistance of Nano-TIM in the vertical direction is 2.2 $K \cdot mm^2 \cdot W^{-1}$, which

is even lower than that of pure Indium (2.6 $K \cdot mm^2 \cdot W^{-1}$). It indicates that the polymer network in the Nano-TIM at least would not degrade the heat dissipation efficiency at interfaces. As we know, the Nano-TIM developed in this study can be roughly categorized to a metal matrix composite (MMC), in which the thermal conductivity mainly depends on the movement of electrons. As the Ag coated PI fibers in the Nano-TIM can form a solid interface with the indium matrix and Cu/ENIG pads, the influence of PI fibers on the thermal interface resistance can be effectively reduced.

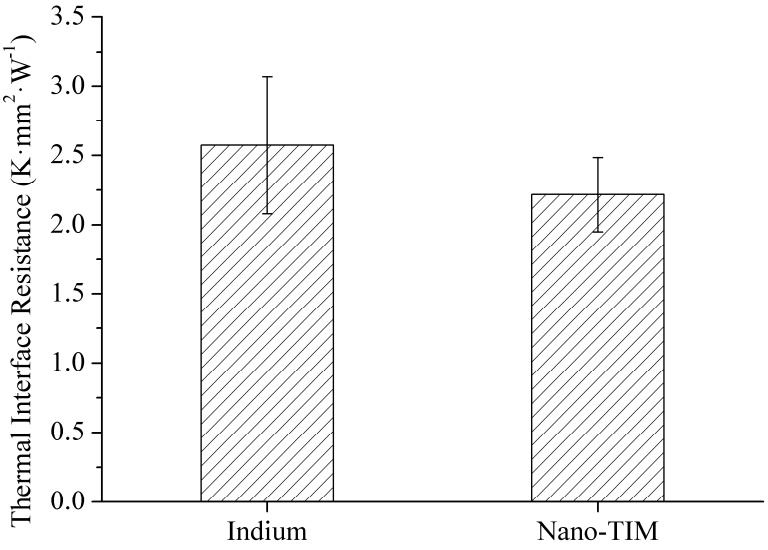


Figure 5.9: Results of thermal interface resistance measurement

Thermal cycling test

Figure 5.10 (a) shows the variation of thermal interface resistance during the TC test. In the figure, pure indium and Nano-TIM both survived after 1000 cycles, despite there being an obvious increase in thermal interface resistance after 100 cycles which is likely caused by the formation of small cracks in the structure during the thermal cycling test. The average increase of thermal interface resistance is shown in Figure 5.10 (b). The increase rate of thermal interface resistance of Nano-TIM is 50 % lower that of pure indium, which shows a promising thermal fatigue resistance of Nano-TIM. The low increase rate of thermal interface resistance of Nano-TIM can be attributed to the reinforcement effect of the PI fibers. Theoretically, under certain strain rate loading (low speed), the stress in the material will be concentrated at the tips of the initial cracks. When this stress at the tip reaches the maximum atomic bond strength, the crack will propagate through the solid and fracture it [127]. The initial cracks formed in the materials are potentially caused by any mechanism that results from sufficiently high local stresses. Examples are high-density dislocation structures formed near surfaces during fatigue, stress concentration in brittle particles due to the strain incompatibility at the interface between the particle and the

deforming metal matrix and grain-boundary triple points [38]. In the Nano-TIM, the dislocation movement near the fibers could be impeded at the fiber/indium boundary, which can constrain the initial crack formation during the fabrication process and the thermal cycling test. The crack propagation during TC test can also be limited by Ag coated fibers in the Nano-TIM. When cracks arrive the interface between the fiber and the matrix, they either cut the Ag coated PI fibers or bypass the fibers along the interface, which will lead to more energy consumption and slower crack propagation. According to a previous study on the tensile stress of Nano-TIM [128], the fiber was broken when the crack arrived the fiber/matrix interface, demonstrating the good bonding quality between the fiber and the indium in the Nano-TIM. In addition, the flexible PI network distributed in the indium matrix could decrease the stress concentration at the interface, which may also help delay the crack propagation in the structure.

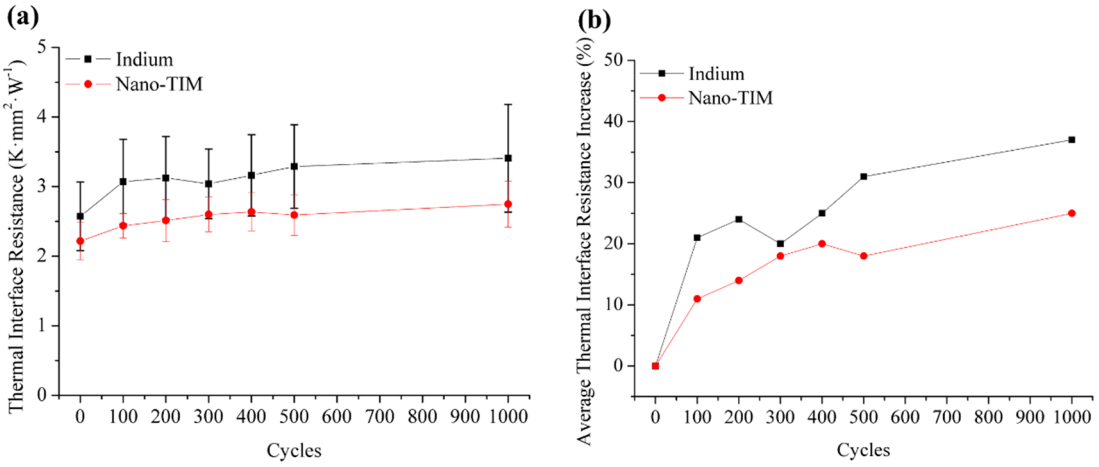


Figure 5.10: Thermal interface resistance measurement after 100, 200, 300, 400, 500, and 1000 temperature cycles.

Thermal infrared camera test

Figure 5.11 shows the temperature distribution of the power chips. A hotspot is designed at the center of the chip. Comparing Figure 5.11 (a) with (b) and (c), the hotspot area of the chip without TIM is obviously larger than the chip with TIM. Figure 5.11 (d) shows that the maximum temperature of the chip without TIM is almost 30 °C higher than the chips with TIM, showing the effect of TIM on increasing the efficiency of heat dissipation. Comparing Figure 5.11 (b) with (c), the temperature distribution of Nano-TIM sample is almost as the same as that of pure indium TIM sample. The similar temperature distribution between Nano-TIM and pure indium indicates that the PI network in the indium matrix would not noticeably degrade the heat dissipation ability of pure indium.

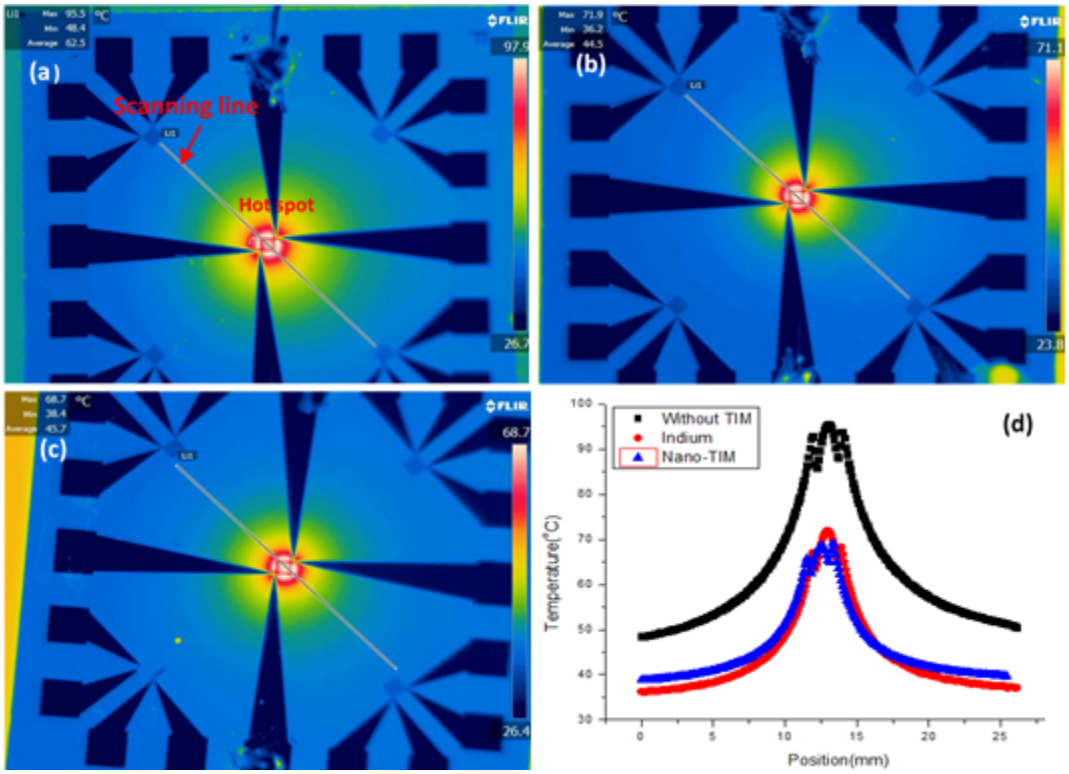


Figure 5.11: IR test results: temperature distribution of the chip (a) without TIM, (b) with pure indium, and (c) with the Nano-TIM; (d) temperature distribution along the line direction shown in Figure 5.11 (a, b, c).

5.2 Nanostructured thermoelectric material for active heat dissipation

Nanopowder characterization

The composition and structure of Bi_2Te_3 ingot and nanopowders were analyzed by XRD with CuKα radiation (λ = 1.54 Å). The XRD patterns of the Bi_2Te_3 ingot and the powder are shown in Figure 5.12. Four peaks at 27.663° (plane spacing = 3.222 Å), 38.072° (2.362), 40.912° (2.204), and 45.072° (2.010) can be observed in the figure area for both ingot and powder sample. These peaks agree with the Bi_2Te_3 PDF card JCPDS 00-015-0863 (27.6632°, 3.222, hkl=015; 37.8332°, 2.3760, hkl=1, 0, 10; 41.1466°, 3.293, hkl=110; 44.5759°, 2.031, hkl=0, 0, 15). This shows that, after the fabrication process, the produced nanopowders still retain the structure of Bi_2Te_3, but the peak width of the nanopowders is clearly broader than that of the ingot, which implies that the grain size of the nanopowders is smaller than those in original ingot.

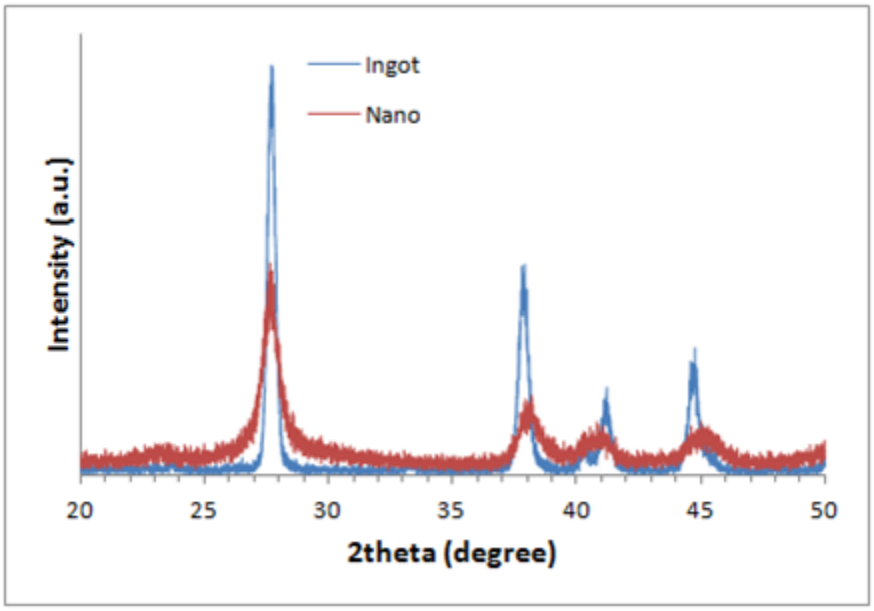


Figure 5.12: XRD patterns of Bi_2Te_3 ingot and nanopowders

Characterization of nanostructured Bi_2Te_3 TE pellets

The Bi_2Te_3 nanostructured TE pellets shown in Figure 5.13 were prepared by first dispersing certain amount of Ag nanoparticles (0, 5, 7.5, 10, and 20 wt. %) and Bi_2Te_3 nanopowders in ethanol with ultrasonic and then annealing in nitrogen atmosphere to get dry powder mixture. After that, the mixed nanopowders were cold-pressed with the pressure of 0.62 GPa for 5 minutes and then moved to the nitrogen oven for hot-pressing. The pressure, temperature, and duration time for hot-pressing are 70 MPa, 300 °C, and 2 hours respectively.

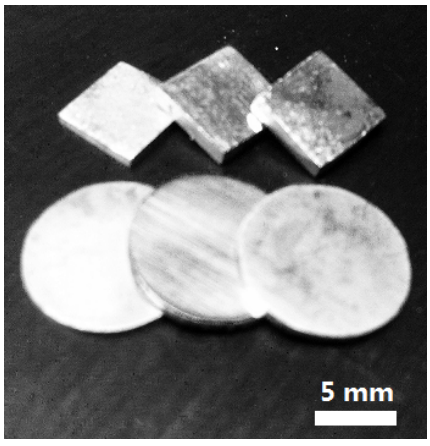


Figure 5.13: Circle and square TE pellets

The microstructure and the composition of Bi_2Te_3 ingot and TE pellets were analyzed by using SEM and EDX respectively. Figure 5.14 shows the microstructure of Bi_2Te_3 ingot (a) and Bi_2Te_3 pellets with 0, 7.5, and 20 wt. % of Ag nanoparticles (b-d). The flat and continuous lamella structure of Bi_2Te_3 is clearly shown in Figure 5.14 (a). In contrast to the ingot, the microstructure of Bi_2Te_3 pellets is quite rough, especially for the pellet with 20 wt. % of Ag nanoparticles. A large void with 10 µm length can be seen in Figure 5.14 (d). In addition, some microsized lamella Bi_2Te_3 pieces (about 5 µm) can be observed in the nanostructured TE pellets, showing a process issue for the nanoparticle fabrication which needs to be improved in future study. However, for nanostructured TE materials, these microsized particles could also be a benefit of decreasing the lattice thermal conductivity as they can scatter those phonons with a long mean free path [129].

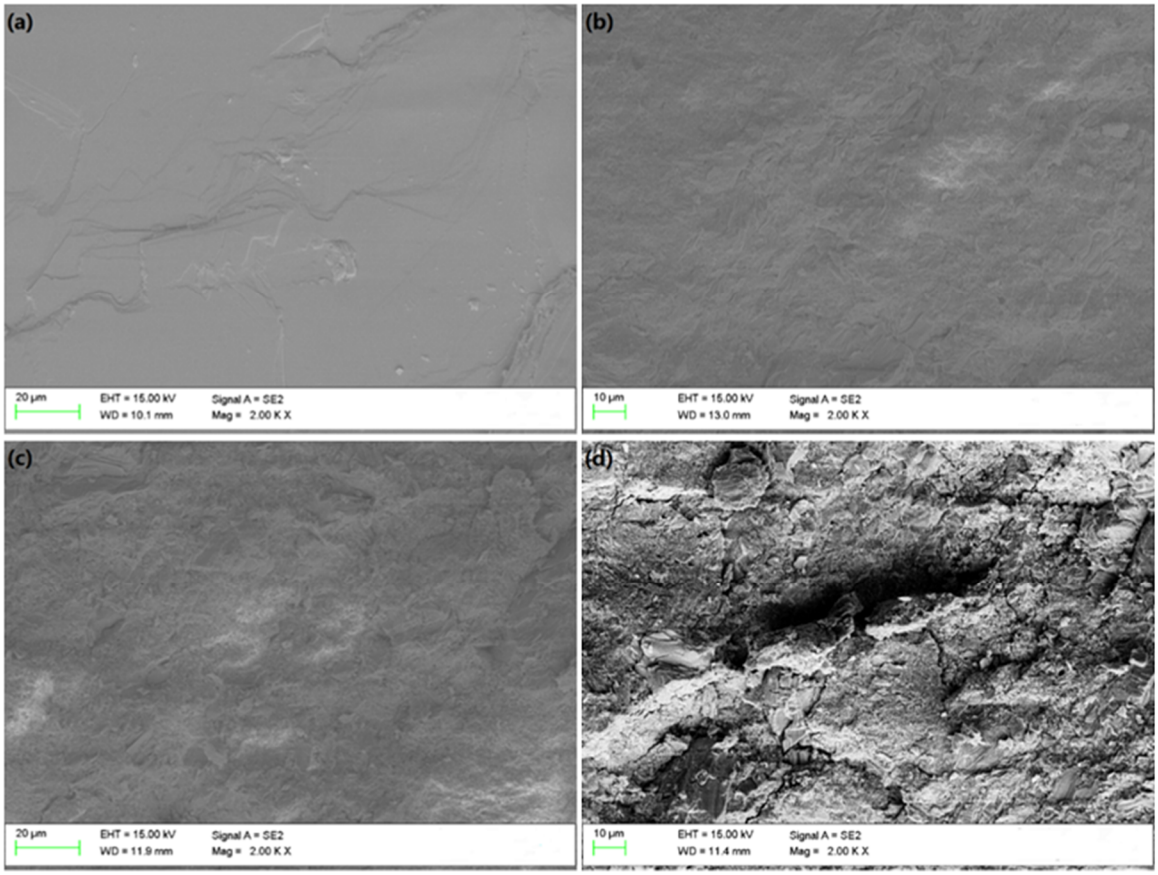


Figure 5.14: SEM images at 2000×: (a) Bi_2Te_3 ingot, (b) pure Bi_2Te_3 pellet, (c) Bi_2Te_3 pellet with 7.5 wt. % Ag nanoparticles, and (d) Bi_2Te_3 pellet with 20 wt. % Ag nanoparticles.

The high magnification SEM images are shown in Figure 5.15. Figure 5.15 (a) shows the lamella structure of Bi_2Te_3 ingot. Figure 5.15 (b-d) indicate the microstructure of TE pellets

in high magnification images, in which most particles are smaller than 200 nanometers, which indicates that the grain growth of Bi_2Te_3 nanoparticles is not significant during the hot-pressing process. However, unlike the smooth and dense Bi_2Te_3 ingot, a lot of tiny voids with the diameter of 100 - 200 nm are detected in the nanostructured pellets, which could decrease the electrical conductivity of TE pellets. Besides the morphology, the composition of the ingot and the pellets were also studied. Several points (circular marks in the figure) were picked up from Figure 5.15 and analyzed by using EDX. The EDX analysis results show that the ingot and pure Bi_2Te_3 pellet only include the element of Bi and Te. Meanwhile, the Bi-Te-Ag could be found in the Ag alloyed Bi_2Te_3 pellets as shown in Figure 5.15.

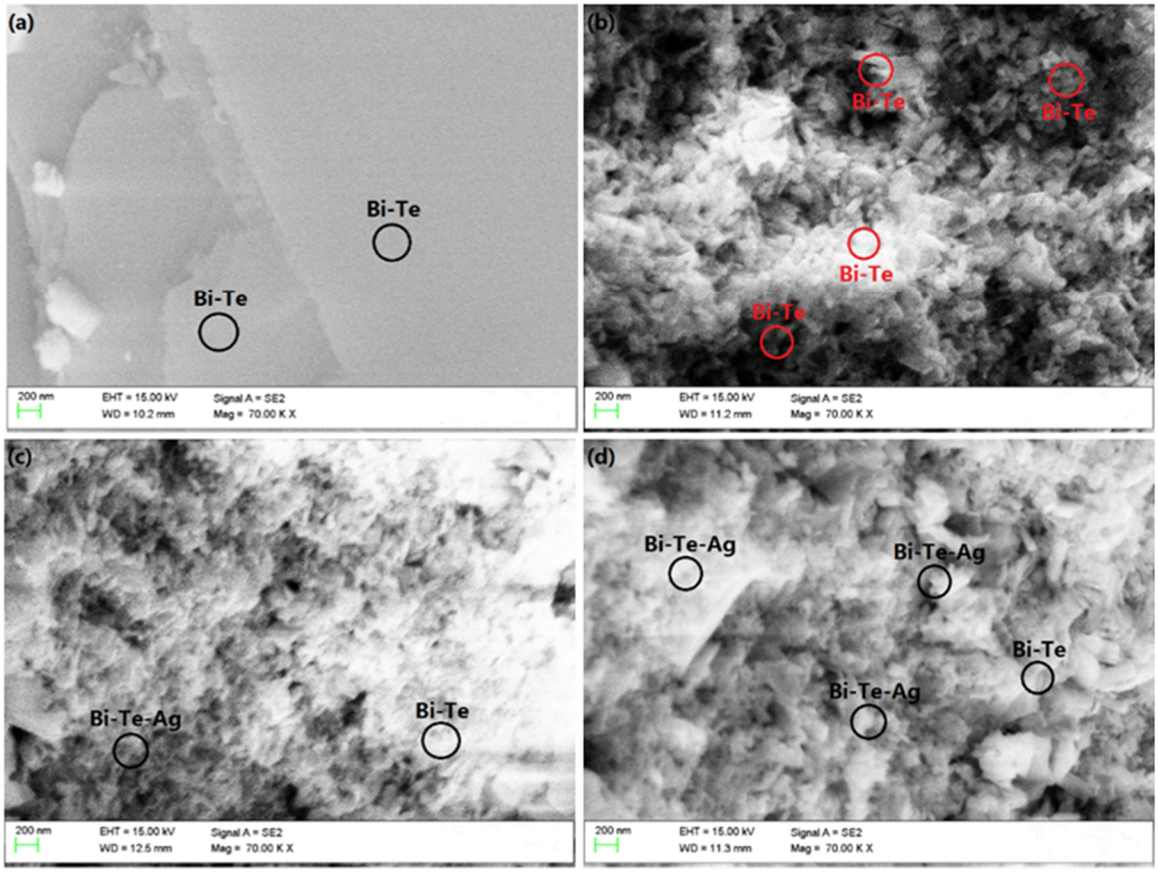


Figure 5.15: SEM images at 70000×: (a) Bi_2Te_3 ingot, (b) pure Bi_2Te_3 pellet, (c) Bi_2Te_3 pellet with 7.5 wt. % Ag nanoparticles, and (d) Bi_2Te_3 pellet with 20 wt. % Ag nanoparticles.

In order to further study the distribution of Ag nanoparticles in the nanoscale Bi_2Te_3 pellets, the Ag element mapping was carried out on Figure 5.14 by using EDX. The analysis results are shown in Figure 5.16. Small amount of Ag could be found in the ingot and pure nanostructured Bi_2Te_3 pellet in spite of the absence of Ag nanoparticles. The Ag in the

ingot and the pure Bi_2Te_3 pellet could come from the noise of the EDX or the contamination during the manufacturing process. Compared to the ingot and pure Bi_2Te_3 pellet, much more Ag can be detected in the Ag alloyed Bi_2Te_3 pellets as shown in Figure 5.16 (c) and (d). However, the distribution of Ag is not so uniform, which could be caused by the agglomeration of Ag nanoparticles in the pellets.

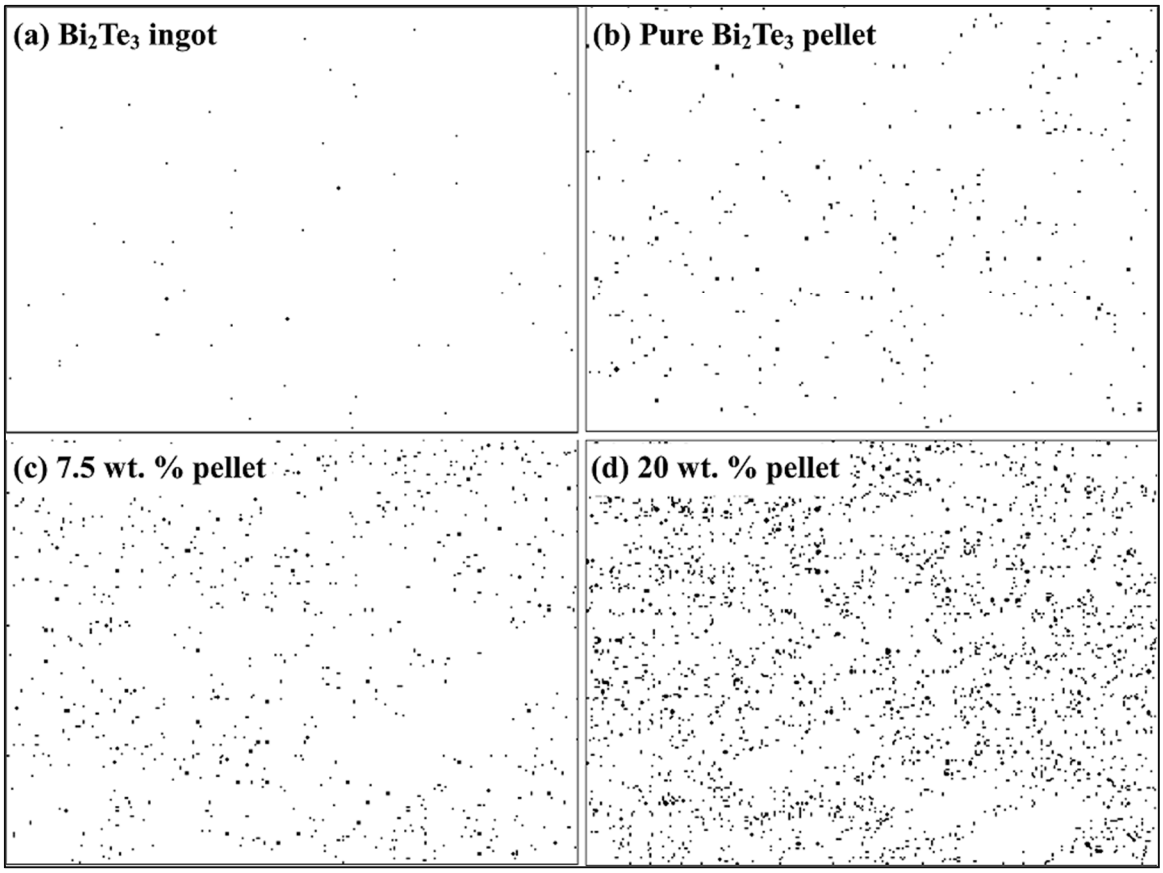


Figure 5.16: EDX mapping for Ag element in 2000× SEM images: (a) Bi_2Te_3 ingot, (b) pure Bi_2Te_3 pellet, (c) Bi_2Te_3 pellet with 7.5 wt. % Ag nanoparticles, and (d) Bi_2Te_3 pellet with 20 wt. % Ag nanoparticles.

Performance Evaluation of Ag Alloyed Bi_2Te_3 Pellets

The performance of Ag alloyed nanostructured n-type Bi_2Te_3 at 300 K were summarized in Figure 5.17. Figure 5.17 (a) shows the measurement results of electrical conductivity. In principal, the electrical conductivity of Bi_2Te_3 could be increased by Ag addition due to the increase of carrier density. However, it is extremely tricky to obtain appropriate content of Ag nanoparticles in nanostructured Bi_2Te_3 matrix for the best Seebeck coefficient and electrical conductivity due to the influence of interface between particles and the voids in the structure. The interface and the voids could be a dominant factor to the performance of

nanostructured TE materials. In this study, the electrical conductivity of pure Bi_2Te_3 is 0.68 $\times 10^5$ $S \cdot m^{-1}$, which is close to the measurement of a previous study [130]. This implies a good bonding between Bi_2Te_3 nanoparticles and a low oxidation level after cold- and hot-pressing process. The electrical conductivity was double increased by adding 5 wt. % of Ag nanoparticles. As the Ag atoms dispersed in the Bi_2Te_3 structure usually behave as donors [131], the carrier concentration in the TE sample will be increased, which will lead to the increase of electrical conductivity. However, it is failed to further increase the electrical conductivity by adding more Ag nanoparticles. Conversely, the electrical conductivity decreased when more than 10 wt. % Ag nanoparticles were added. The decrease of the electrical conductivity could be caused by the increased voids in the structure. In addition to the voids, some researchers claimed that surplus Ag atoms will take the place of Bi sites in the Bi_2Te_3 lattice and then act as acceptors instead of donors, which therefore leads to the decrease of electrical conductivity [132].

Unlike the electrical conductivity, no obvious variation in Seebeck coefficient was observed with the content of Ag nanoparticles as shown in Figure 5.17 (b). As we know, the Seebeck coefficient strongly depends on the Fermi level, which in turn depends upon the carrier concentration, the carrier effective mass, and the temperature [133]. In general, Seebeck coefficient tends to decrease when the carrier concentration increases. However, the experimental result in our test does not follow this trend. The reason is still not clear. In fact, in addition to the carrier concentration, the Seebeck coefficient is also affected by other complex factors, such as the interaction between carriers and phonons, the interface, and voids in the structure. Therefore, the further study is necessary to explain this phenomenon.

The results of thermal conductivity measurement are shown in Figure 5.17 (c). The thermal conductivity of pure nanostructured Bi_2Te_3 pellet is as low as 0.646 $W \cdot m^{-1} \cdot K^{-1}$, which is much lower than that of bulk Bi_2Te_3 (1.5-2 $W \cdot m^{-1} \cdot K^{-1}$) [134]. The low thermal conductivity of nanostructured materials has been well discussed in another study [135]. Thermal conductivity consists of lattice thermal conductivity and electronic thermal conductivity. Owing to the increased grain boundary in the nanostructured materials, the phonon scattering at the grain boundaries is enhanced, which could significantly reduce the lattice thermal conductivity. In our study, this low thermal conductivity was further decreased to 0.493 $W \cdot m^{-1} \cdot K^{-1}$ after the addition of 5 wt. % Ag nanoparticles. Although the Ag nanoparticles in the structure could increase the electronic thermal conductivity, the increased defects and voids due to the Ag nanoparticles will also enhance the phonon scattering and then reduce the lattice thermal conductivity. Therefore, small volume Ag nanoparticles will lead to larger decrease of the lattice thermal conductivity compared to the increase of electronic thermal conductivity. If the content of Ag nanoparticles continues to increase, the electronic thermal conductivity will replace the lattice thermal conductivity as the dominant in the total thermal conductivity. Then, the variation of the thermal conductivity will obey the Wiedemann-Franz law. As shown in Figure 5.17 (c), when adding 20 wt. % Ag nanoparticles in the Bi_2Te_3 nanopowders, the thermal conductivity climbed to 0.57 $W \cdot m^{-1} \cdot K^{-1}$ due to the increase of electronic thermal conductivity.

The ZT value was calculated according to the measurement results of the electrical conductivity, Seebeck coefficient, and thermal conductivity. As shown in Figure 5.17 (d), the best ZT value achieved in this study is 1.48 at 300 K from the nanostructured sample with 7.5 wt. % Ag nanoparticles, which is close to state-of-the-art of 1.8 [124]

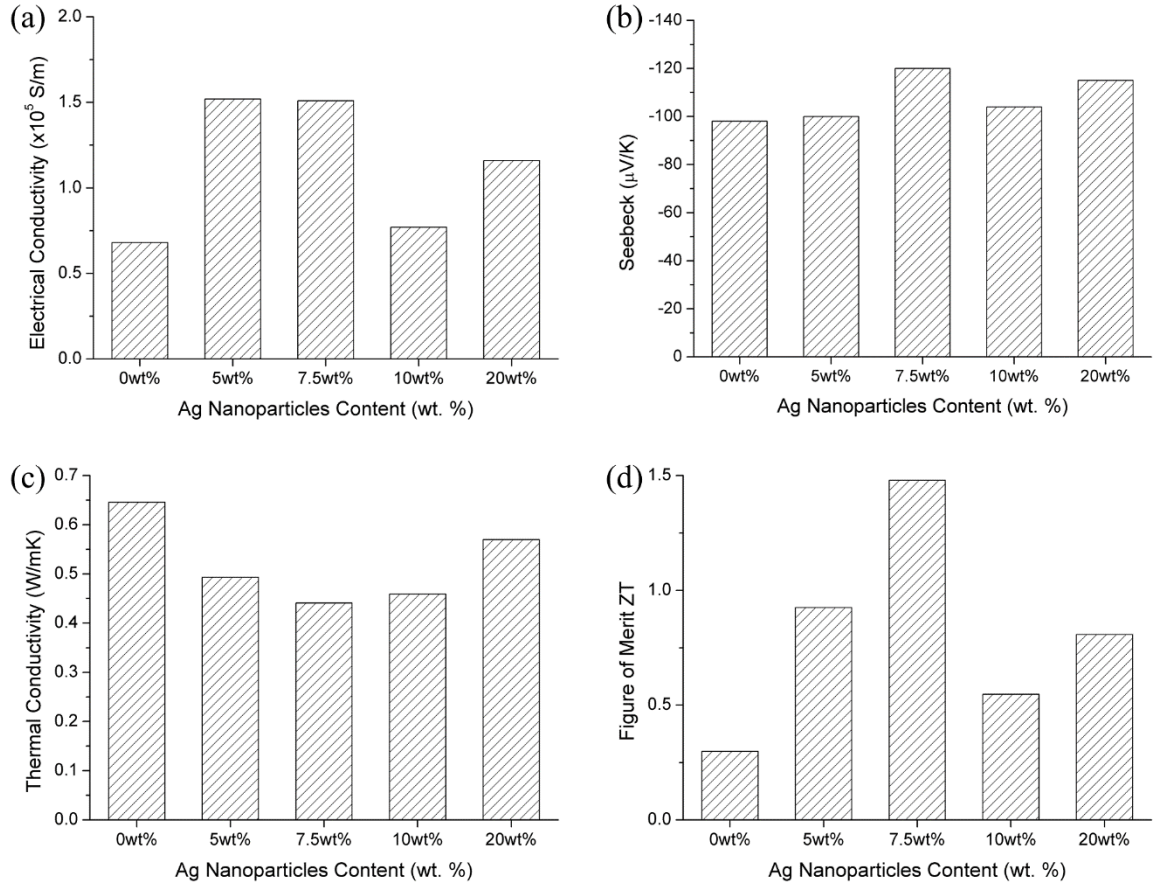


Figure 5.17: Experimental results of Ag alloyed nanostructured n-type Bi_2Te_3 pellets at room temperature (300 K): (a) electrical conductivity, (b) Seebeck coefficient, (c) thermal conductivity, and (d) Figure of Merit ZT.

Chapter 6 Conclusions and Outlook

In this thesis, 5 types of nano-based materials, VACNT, VACNF, SAC305 and Bi_2Te_3 nanoparticles enhanced solders, and polymer-indium composite, were fabricated and characterized; addressing the challenges of high density packaging aspects of interconnects and thermal management technologies.

VACNT bundles grown with the TCVD method were transferred from the growth chip to the TSVs after the densification process. The electrical resistivity of VACNT filled vias can be as low as 3.9×10^{-5} Ω·m. Another 1D carbon nanomaterial, VACNFs grown with PECVD method, were used as bump materials, instead of solders, on the chip surface. A series of post-processes, such as surface coating and transfer processes, were developed in order to form bumps. However, the electrical conductivity and shear strength of these VACNF bumps were both one order of magnitude lower than SAC305 solders. This low electrical and mechanical performance of VACNF bumps could be caused by its intrinsic cone-stacked structure and weak bonding between the cones. Besides the use as bumps, VACNFs were also used as a reinforcement layer in the solder joint structure. The thermal fatigue resistance of SAC305 solder joint can be increased 40 % by using a VACNF layer on the chip side. In summary, compared to traditional interconnect materials, such as Cu and solders, 1D carbon nanomaterials are more advantageous in aspects such as dimension, current density, stability, weight, and thermal fatigue resistance. However, the electrical conductivity and bonding strength of VACNTs and VACNFs are still lower than those traditional materials and need to be further improved in future work. The efforts can be focused on carbon surface functionalization, reducing structural defects, or developing nanocomposite materials.

In addition to develop new types of interconnect materials, the study in this thesis also includes improving traditional materials with nanomaterials. Two traditional lead-free solders, Sn58Bi and SAC305 were mixed with SAC305 and Bi_2Te_3 nanoparticles respectively, forming two nanocomposite solders, in order to enhance the mechanical performance. The experimental results show that the shear strength of the solders was increased by adding nanosized particles. The nanoparticles distributed in the solder matrix can constrain the dislocation movement as secondary phase particles, as well as promoting a fine microstructure as by acting as absorption materials or through extra nucleation sites. As the mismatch between solder matrix and nanoparticles has been designed to be as small as possible, no degradation of thermal fatigue resistance has been detected from the two nanocomposite solders during thermal cycling tests. Although some valuable results have been achieved in this work, several problems with nanocomposite solders still need to be solved. For example, it is still difficult to retain all nanoparticles within the solder matrix after the reflow soldering process, even though the mismatch between nanoparticles and the solder matrix has been reduced. Moreover, the void content of nanocomposite solder is quite high compared to pure lead-free solders, which in turn limits the volume of nanoparticles that can be added to the nanocomposite solders.

Thermal management, as another challenge of the 3D packaging, is also covered by this thesis. Focusing on decreasing the thermal interface resistance and increasing the heat dissipation, a novel Indium/PI network TIM and a nanostructured TE material were developed. The major work related to TIMs in this thesis is to evaluate their mechanical performance in practical applications. The test results show that the shear strength and thermal fatigue resistance of a pure indium TIM can be improved by using Ag coated PI network without any loss of heat dissipation efficiency. For nanostructured TE bulk materials, the peak ZT value of Ag alloyed Bi_2Te_3 material was as high as 1.4, which is quite close to the state-of-the-art of n-type TE materials. Combining this TE material with a large scale fabrication process currently being developed in BNSL at Chalmers, means that it will have a bright future in the thermal management industry. The next step in TE materials research will be focused on developing bulk p-type TE materials and assembling a TE cooler with a high coefficient of performance (COP).

Acknowledgements

First of all, I would like to express my gratitude to my supervisor Prof. Johan Liu for giving me an opportunity to study and work in such a wonderful, exciting, and challenging group. With his guidance, help, and encourage, I have gradually made sense of science, technology and industry. I would also like to thank my co-supervisors Dr. Lilei Ye and Prof. Yan Zhang for their sincere guidance and help on my research, experiment, and thesis.

I would like to present many thanks to all of my colleagues in BioNano Systems Laboratory: Dr. Murali Murugesan, Dr. Michael Edwards, Dr. Xin Luo, Dr. Zhili Hu, Nan Wang, Yong Zhang, Wei Mu, Shuangxi Sun, Changhong Zhao, Andreas Nylander, and Josef Hansson. Special thanks are given to: Dr. Teng Wang for selflessly teaching me all his skills and knowledge on carbon nanotubes, Nikolaos Logothetis for his great assistance on my experimental work, Dr. Yifeng Fu for his suggestions and help on the growth of carbon nanotubes, Dr. Björn Carlberg for his professional guidance on equipment operation and excellent work on lab maintenance, Di Jiang for his help on the design and fabrication of my test samples, Dr. Carl Zandén for his help and comment on my experimental design and result analysis.

I greatly appreciate the staff who serve in our cleanroom. Thanks for their work on the machine training and maintenance. Here I would like to especially thank Ulf Södervall, Kajia Matikainen, Karin Hedsten, Henrik Frederiksen, Bengt Nilsson, Piotr Jedrasik, Göran Alestig, Johan Andersson, Mats Hagberg, and Mahdad Sadeghi for their help on instrument training and process trouble shooting in my work. I also would like to thank Carl Magnus and Mats Myremark for their mechanical support on my experiment.

I would like to thank SSF programs “Carbon Based 3D GaN High Speed Electronics System” and “Scalable Nanomaterials and Solution Processable Thermoelectric Generators”, EU FP7 programs “Smartpower” and “Nanoteg” as well as NSFC, Shanghai Science and Technology Commission and China Scholarship Council for their support and funding.

Last but not least, I would like to thank my wife, parents, sister, and niece for their love, understanding, forgiveness, and support.

References

[1] M. Riordan, "The lost history of the transistor," *IEEE Spectrum*, vol. 41, no. 5, pp. 44–49, May 2004.

[2] J. S. Kilby, "Miniaturized electronic circuits," US3138743 A, 23-Jun-1964.

[3] G. E. Moore, "Cramming More Components Onto Integrated Circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, 1998.

[4] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, no. 6348, pp. 56–58, Nov. 1991.

[5] R. Tummala, *Fundamentals of Microsystems Packaging*, 1st ed. McGraw-Hill Professional, 2001.

[6] "Flip Chip Assembly," in *Integrated Circuit Packaging, Assembly and Interconnections*, Springer US, 2007, pp. 169–191.

[7] R. P. Prasad, "Introduction to Surface Mount Technology," in *Surface Mount Technology*, Springer US, 1997, pp. 3–50.

[8] C. A. Harper, Ed., *Electronic packaging and interconnection handbook*, 4. ed. New York ; London: McGraw-Hill, 2005.

[9] ITRS, "International technology roadmap for semiconductors 2007 edition - assembly and packaging," tech. rep., 2007.

[10] S.-Y. Jang, T.-S. Park, Y.-S. Kim, J.-W. Jeong, J.-J. Bang, and D.-K. Kang, "Wafer level package solder joint reliability study for portable electronic devices," in *Proceedings - Electronic Components and Technology Conference*, 2005, vol. 1, pp. 660–664.

[11] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Res.*, vol. 3, no. 3, pp. 147–169, Mar. 2010.

[12] W. Luther, "Nanomaterials," in *Technology Guide*, H.-J. Bullinger, Ed. Springer Berlin Heidelberg, 2009, pp. 38–41.

[13] M. J. Pitkethly, "Nanomaterials – the driving force," *Materials Today*, vol. 7, no. 12, pp. 20–29, Dec. 2004.

[14] D. K. T. Ramesh, "Nanomaterials," in *Nanomaterials*, Springer US, 2009, pp. 1–20.

[15] J. Sun and S. L. Simon, "The melting behavior of aluminum nanoparticles," *Thermochimica Acta*, vol. 463, no. 1–2, pp. 32–40, Oct. 2007.

[16] S. L. Lai, J. Y. Guo, V. Petrova, G. Ramanath, and L. H. Allen, "Size-Dependent Melting Properties of Small Tin Particles: Nanocalorimetric Measurements," *Phys. Rev. Lett.*, vol. 77, no. 1, pp. 99–102, Jul. 1996.

[17] Y. Gao, C. Zou, B. Yang, Q. Zhai, J. Liu, E. Zhuravlev, and C. Schick, "Nanoparticles of SnAgCu lead-free solder alloy with an equivalent melting temperature of SnPb solder alloy," *Journal of Alloys and Compounds*, vol. 484, no. 1–2, pp. 777–781, Sep. 2009.

[18] C.D. Zou, Y.L. Gao, B. Yang, Q.J. Zhai, C. Andersson, and J. Liu, "Melting temperature depression of Sn-0.4Co-0.7Cu lead-free solder nanoparticles," *Soldering & Surface Mount Tech*, vol. 21, no. 2, pp. 9–13, Apr. 2009.

[19] "Advantages and Limitations Using Nano sized Powders on the Powder Injection M oulding Process: A Review." [Online]. Available: http://www.academia.edu/332063

8/Advantages_and_Limitations_Using_Nano_sized_Powders_on_the_Powder_Injection_Moulding_Process_A_Review. [Accessed: 08-Mar-2015].
[20] A. Z. Moshfegh, "Nanoparticle catalysts," *J. Phys. D: Appl. Phys.*, vol. 42, no. 23, p. 233001, Dec. 2009.
[21] S. I. Cha, K. T. Kim, S. N. Arshad, C. B. Mo, and S. H. Hong, "Extraordinary Strengthening Effect of Carbon Nanotubes in Metal-Matrix Nanocomposites Processed by Molecular-Level Mixing," *Adv. Mater.*, vol. 17, no. 11, pp. 1377–1381, Jun. 2005.
[22] K. Chu and C. Jia, "Enhanced strength in bulk graphene–copper composites," *Phys. Status Solidi A*, vol. 211, no. 1, pp. 184–190, Jan. 2014.
[23] N. Wang, M. Murugesan, L. Ye, B. Carlberg, S. Chen, and J. Liu, "Reliability investigation of nano-enhanced thermal conductive adhesives," in *Proceedings of the IEEE Conference on Nanotechnology*, 2012.
[24] J. Liu, S. Chen, and L. Ye, "Development and Characterization of Nano-Composite Solder," in *Lead-Free Solders: Materials Reliability for Electronics*, K. N. Subramanian, Ed. John Wiley & Sons, Ltd, 2012, pp. 161–177.
[25] I. A. Bucklow and L. E. Drain, "Spark erosion in liquid argon," *J. Sci. Instrum.*, vol. 41, no. 10, p. 614, Oct. 1964.
[26] Y. Tokoi, Y. M. Izuari, T. Suzuki, T. Nakayama, H. Suematsu, and K. Niihara, "Preparation of Alumina Nanoparticles by Pulsed Wire Discharge in Water," *IOP Conf. Ser.: Mater. Sci. Eng.*, vol. 18, no. 6, p. 062021, Oct. 2011.
[27] J.-K. Lung, J.-C. Huang, D.-C. Tien, C.-Y. Liao, K.-H. Tseng, T.-T. Tsung, W.-S. Kao, T.-H. Tsai, C.-S. Jwo, H.-M. Lin, and L. Stobinski, "Preparation of gold nanoparticles by arc discharge in water," *Journal of Alloys and Compounds*, vol. 434–435, pp. 655–658, May 2007.
[28] S.-M. Liu, M. Kobayashi, S. Sato, and K. Kimura, "Synthesis of silicon nanowires and nanoparticles by arc-discharge in water," *Chem. Commun.*, no. 37, pp. 4690–4692, Sep. 2005.
[29] N. Sano, H. Wang, I. Alexandrou, M. Chhowalla, K. B. K. Teo, G. a. J. Amaratunga, and K. Iimura, "Properties of carbon onions produced by an arc discharge in water," *Journal of Applied Physics*, vol. 92, no. 5, pp. 2783–2788, Sep. 2002.
[30] D. Delaportas, P. Svarnas, I. Alexandrou, A. Siokou, K. Black, and J. W. Bradley, "γ-Al2O3 nanoparticle production by arc-discharge in water: in situ discharge characterization and nanoparticle investigation," *J. Phys. D: Appl. Phys.*, vol. 42, no. 24, p. 245204, Dec. 2009.
[31] C. Andersson, C. Zou, B. Yang, Y. Gao, J. Liu, and Q. Zhai, "Recent advances in the synthesis of lead-free solder nanoparticle," in *Electronics System-Integration Technology Conference, 2008. ESTC 2008. 2nd*, 2008, pp. 915–922.
[32] D. W. Rudorff, "Principles and Applications of Spark Machining," *Proceedings of the Institution of Mechanical Engineers*, vol. 171, no. 1, pp. 495–511, Jun. 1957.
[33] W. Guan, S. C. Verma, Y. Gao, C. Andersson, Q. Zhai, and J. Liu, "Characterization of Nanoparticles of Lead Free Solder Alloys," in *Electronics Systemintegration Technology Conference, 2006. 1st*, 2006, vol. 1, pp. 7–12.
[34] J. H. Wendorff, S. Agarwal, and A. Greiner, *Electrospinning: Materials, Processing, and Applications*. John Wiley & Sons, 2012.

[35] G. Taylor, “Disintegration of Water Drops in an Electric Field,” *Proceedings of the Royal Society of London A: Mathematical, Physical and Engineering Sciences*, vol. 280, no. 1382, pp. 383–397, Jul. 1964.
[36] D. H. Reneker, A. L. Yarin, H. Fong, and S. Koombhongse, “Bending instability of electrically charged liquid jets of polymer solutions in electrospinning,” *Journal of Applied Physics*, vol. 87, no. 9, pp. 4531–4547, May 2000.
[37] D. Li and Y. Xia, “Electrospinning of Nanofibers: Reinventing the Wheel?,” *Adv. Mater.*, vol. 16, no. 14, pp. 1151–1170, Jul. 2004.
[38] B. Carlberg, J. Liu, and L.-L. Ye, “Polymer nanofiber based continuous metal phase composite for thermal management applications,” in *Electronic System-Integration Technology Conference (ESTC), 2010 3rd*, 2010, pp. 1–6.
[39] *Nanoparticles : Properties, Classification, Characterization, and Fabrication*. Hauppauge, NY, USA: Nova Science Publishers, Inc., 2009.
[40] L. Zhou, H. Zhang, H. Zhang, and Z. Zhang, “Homogeneous nanoparticle dispersion prepared with impurity-free dispersant by the ball mill technique,” *Particuology*, vol. 11, no. 4, pp. 441–447, Aug. 2013.
[41] E. Amstad, T. Gillich, I. Bilecka, M. Textor, and E. Reimhult, “Ultrastable Iron Oxide Nanoparticle Colloidal Suspensions Using Dispersants with Catechol-Derived Anchor Groups,” *Nano Lett.*, vol. 9, no. 12, pp. 4042–4048, Dec. 2009.
[42] A. V. Melechko, V. I. Merkulov, T. E. McKnight, M. A. Guillorn, K. L. Klein, D. H. Lowndes, and M. L. Simpson, “Vertically aligned carbon nanofibers and related structures: Controlled synthesis and directed assembly,” *Journal of Applied Physics*, vol. 97, no. 4, pp. 041301–041301–39, Feb. 2005.
[43] Y. Fu, S. Chen, J. Bielecki, A. Matic, T. Wang, L.-L. Ye, and J. Liu, “Selective growth of double-walled carbon nanotubes on gold films,” *Materials Letters*, vol. 72, pp. 78–80, 2012.
[44] A. Agarwal, S. R. Bakshi, and D. Lahiri, *Carbon Nanotubes: Reinforced Metal Matrix Composites*. CRC Press, 2010.
[45] B. Q. Wei, R. Vajtai, and P. M. Ajayan, “Reliability and current carrying capacity of carbon nanotubes,” *Applied Physics Letters*, vol. 79, no. 8, pp. 1172–1174, Aug. 2001.
[46] Y. Maniwa, R. Fujiwara, H. Kira, H. Tou, H. Kataura, S. Suzuki, Y. Achiba, E. Nishibori, M. Takata, M. Sakata, A. Fujiwara, and H. Suematsu, “Thermal expansion of single-walled carbon nanotube (SWNT) bundles: X-ray diffraction studies,” *Phys. Rev. B*, vol. 64, no. 24, p. 241402, Nov. 2001.
[47] M. Suzuki, Y. Ominami, Q. Ngo, C. Y. Yang, A. M. Cassell, and J. Li, “Current-induced breakdown of carbon nanofibers,” *Journal of Applied Physics*, vol. 101, no. 11, p. 114307, Jun. 2007.
[48] “Introduction to Nanofiber Materials | Materials science,” *Cambridge University Press*. [Online]. Available: http://www.cambridge.org/us/academic/subjects/engineering/materials-science/introduction-nanofiber-materials. [Accessed: 21-Nov-2014].
[49] Q. Ngo, A. M. Cassell, A. J. Austin, J. Li, S. Krishnan, M. Meyyappan, and C. Y. Yang, “Characteristics of aligned carbon nanofibers for interconnect via applications,” *IEEE Electron Device Letters*, vol. 27, no. 4, pp. 221 – 224, Apr. 2006.

[50] S. Hofmann, C. Ducati, J. Robertson, and B. Kleinsorge, "Low-temperature growth of carbon nanotubes by plasma-enhanced chemical vapor deposition," *Applied Physics Letters*, vol. 83, no. 1, pp. 135–137, Jul. 2003.
[51] E. Dervishi, A. R. Biris, J. A. Driver, F. Watanabe, S. Bourdo, and A. S. Biris, "Low-temperature (150 °C) carbon nanotube growth on a catalytically active iron oxide–graphene nano-structural system," *Journal of Catalysis*, vol. 299, pp. 307–315, Mar. 2013.
[52] K. M. Metz, K.-Y. Tse, S. E. Baker, E. C. Landis, and R. J. Hamers, "Ultrahigh-Surface-Area Metallic Electrodes by Templated Electroless Deposition on Functionalized Carbon Nanofiber Scaffolds," *Chem. Mater.*, vol. 18, no. 23, pp. 5398–5400, Nov. 2006.
[53] Y. Fu, Y. Qin, T. Wang, S. Chen, and J. Liu, "Ultrafast Transfer of Metal-Enhanced Carbon Nanotubes at Low Temperature for Large-Scale Electronics Assembly," *Advanced Materials*, vol. 22, no. 44, pp. 5039–5042, 2010.
[54] S. Chen, D. Jiang, C. Zande´n, Z. Hu, Y. Fu, Y. Zhang, L. Ye, and J. Liu, "Ultra-short vertically aligned carbon nanofibers transfer and application as bonding material," *Soldering & Surface Mount Technology*, vol. 25, no. 4, pp. 242–250, Sep. 2013.
[55] J. Kim, H. Schoeller, J. Cho, and S. Park, "Effect of Oxidation on Indium Solderability," *Journal of Elec Materi*, vol. 37, no. 4, pp. 483–489, Dec. 2007.
[56] H. Qiuping, X. Gaowei, Q. Gang, Y. Yuan, and L. Le, "Electroplated indium bump arrays and the bonding reliability," *J. Semicond.*, vol. 31, no. 11, p. 116004, Nov. 2010.
[57] U. Schwarz-Schampera, "Indium," in *Critical Metals Handbook*, G. Gunn, Ed. Oxford: John Wiley & Sons, 2013, pp. 204–229.
[58] A. A. Puretzky, D. B. Geohegan, S. Jesse, I. N. Ivanov, and G. Eres, "In situ measurements and modeling of carbon nanotube array growth kinetics during chemical vapor deposition," *Applied Physics A*, vol. 81, no. 2, pp. 223–240, Jul. 2005.
[59] K. M. Kumar, V. Kripesh, and A. A. O. Tay, "Single-wall carbon nanotube (SWCNT) functionalized Sn–Ag–Cu lead-free composite solders," *Journal of Alloys and Compounds*, vol. 450, no. 1–2, pp. 229–237, 2008.
[60] Y. D. Han, S. M. L. Nai, H. Y. Jing, L. Y. Xu, C. M. Tan, and J. Wei, "Development of a Sn–Ag–Cu solder reinforced with Ni-coated carbon nanotubes," *J Mater Sci: Mater Electron*, vol. 22, no. 3, pp. 315–322, Mar. 2011.
[61] R. Prasher, "Thermal Interface Materials: Historical Perspective, Status, and Future Directions," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1571–1586, Aug. 2006.
[62] S. Chen, L. Zhang, J. Liu, Y. Gao, and Q. Zhai, "A Reliability Study of Nanoparticles Reinforced Composite Lead-Free Solder," *MATERIALS TRANSACTIONS*, vol. 51, no. 10, pp. 1720–1726, 2010.
[63] W. Du, H. Cui, S. Chen, Z. Yuan, L. Ye, and J. Liu, "Study into high temperature reliability of isotropic conductive adhesive," in *2011 12th International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP)*, 2011, pp. 1 –3.
[64] T. Ozkan, M. Naraghi, and I. Chasiotis, "Mechanical properties of vapor grown carbon nanofibers," *Carbon*, vol. 48, no. 1, pp. 239–244, 2010.

[65] K.-L. Lin, K.-I. Chen, H.-M. Hsu, and C.-L. Shi, "Improvement in the properties of Sn-Zn Eutectic based Pb-free solder," in *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*, 2003, pp. 658–663.
[66] S. Kikuchi, M. Nishimura, K. Suetsugu, T. Ikari, and K. Matsushige, "Strength of bonding interface in lead-free Sn alloy solders," *Materials Science and Engineering: A*, vol. 319–321, pp. 475–479, 2001.
[67] F. Guo, "Composite lead-free electronic solders," in *Lead-Free Electronic Solders*, Springer US, 2007, pp. 129–145.
[68] D. Lin, G. . Wang, T. . Srivatsan, M. Al-Hajri, and M. Petraroli, "The influence of copper nanopowders on microstructure and hardness of lead–tin solder," *Materials Letters*, vol. 53, no. 4–5, pp. 333–338, 2002.
[69] Y. Shi, J. Liu, Y. Yan, Z. Xia, Y. Lei, F. Guo, and X. Li, "Creep Properties of Composite Solders Reinforced with Nano- and Microsized Particles," *Journal of Elec Materi*, vol. 37, no. 4, pp. 507–514, Apr. 2008.
[70] P. Babaghorbani, S. M. L. Nai, and M. Gupta, "Integrating copper at the nanometer length scale with Sn–3.5Ag solder to develop high performance nanocomposites," *Materials Science and Technology*, vol. 25, no. 10, pp. 1258–1264, 2009.
[71] A. Nadia and A. S. M. A. Haseeb, "Understanding the effects of addition of copper nanoparticles to Sn-3.5 Ag solder," *Soldering & Surface Mount Technology*, vol. 23, no. 2, pp. 68–74, Apr. 2011.
[72] M. E. Alam and M. Gupta, "Effect of addition of nano-copper and extrusion temperature on the microstructure and mechanical response of tin," *Journal of Alloys and Compounds*, vol. 490, no. 1–2, pp. 110–117, 2010.
[73] J. P. Liu, F. Guo, Y. F. Yan, W. B. Wang, and Y. W. Shi, "Development of creep-resistant, nanosized Ag particle-reinforced Sn-Pb composite solders," *Journal of Elec Materi*, vol. 33, no. 9, pp. 958–963, Sep. 2004.
[74] Y. Shi, J. Liu, Z. Xia, Y. Lei, F. Guo, and X. Li, "Study on creep characterization of nano-sized Ag particle-reinforced Sn–Pb composte solder joints," *J Mater Sci: Mater Electron*, vol. 21, no. 3, pp. 256–261, Mar. 2010.
[75] A. K. Gain, Y. C. Chan, A. Sharif, N. B. Wong, and W. K. C. Yung, "Interfacial microstructure and shear strength of Ag nano particle doped Sn–9Zn solder in ball grid array packages," *Microelectronics Reliability*, vol. 49, no. 7, pp. 746–753, 2009.
[76] K. Bukat, M. Koscielski, J. Sitek, M. Jakubowska, and A. Mlozniak, "Silver nanoparticles effect on the wettability of Sn-Ag-Cu solder pastes and solder joints microstructure on copper," *Soldering & Surface Mount Technology*, vol. 23, no. 3, pp. 150–160, Jun. 2011.
[77] S. Ismathullakhan, H. Lau, and Y. Chan, "Enhanced electromigration reliability via Ag nanoparticles modified eutectic Sn–58Bi solder joint," *Microsyst Technol*, vol. 19, no. 7, pp. 1069–1080, Dec. 2012.
[78] A. K. Gain, T. Fouzder, Y. C. Chan, A. Sharif, N. B. Wong, and W. K. C. Yung, "The influence of addition of Al nano-particles on the microstructure and shear strength of eutectic Sn–Ag–Cu solder on Au/Ni metallized Cu pads," *Journal of Alloys and Compounds*, vol. 506, no. 1, pp. 216–223, 2010.
[79] A. K. Gain and Y. C. Chan, "The influence of a small amount of Al and Ni nano-particles on the microstructure, kinetics and hardness of Sn–Ag–Cu solder on OSP-Cu pads," *Intermetallics*, vol. 29, pp. 48–55, 2012.

[80] Y. H. Chan, M. M. Arafat, and A. S. M. A. Haseeb, "Effects of reflow on the interfacial characteristics between Zn nanoparticles containing Sn-3.8Ag-0.7Cu solder and copper substrate," *Soldering & Surface Mount Technology*, vol. 25, no. 2, pp. 91–98, Apr. 2013.
[81] A. S. M. A. Haseeb, Y. M. Leong, and M. M. Arafat, "In-situ alloying of Sn–3.5Ag solder during reflow through Zn nanoparticle addition and its effects on interfacial intermetallic layers," *Intermetallics*, vol. 54, pp. 86–94, Nov. 2014.
[82] M. M. Arafat, A. S. M. A. Haseeb, and M. R. Johan, "Interfacial reaction and dissolution behavior of Cu substrate in molten Sn-3.8Ag-0.7Cu in the presence of Mo nanoparticles," *Soldering & Surface Mount Technology*, vol. 23, no. 3, pp. 140–149, Jun. 2011.
[83] A. S. M. A. Haseeb, M. M. Arafat, and M. R. Johan, "Stability of molybdenum nanoparticles in Sn–3.8Ag–0.7Cu solder during multiple reflow and their influence on interfacial intermetallic compounds," *Materials Characterization*, vol. 64, pp. 27–35, 2012.
[84] A. S. M. A. Haseeb and T. S. Leng, "Effects of Co nanoparticle addition to Sn–3.8Ag–0.7Cu solder on interfacial structure after reflow and ageing," *Intermetallics*, vol. 19, no. 5, pp. 707–712, 2011.
[85] S. L. Tay, A. S. M. A. Haseeb, and M. R. Johan, "Addition of cobalt nanoparticles into Sn-3.8Ag-0.7Cu lead-free solder by paste mixing," *Soldering & Surface Mount Technology*, vol. 23, no. 1, pp. 10–14, Feb. 2011.
[86] I. Shafiq, Y. C. Chan, N. B. Wong, and W. K. C. Yung, "Influence of small Sb nanoparticles additions on the microstructure, hardness and tensile properties of Sn–9Zn binary eutectic solder alloy," *J Mater Sci: Mater Electron*, vol. 23, no. 7, pp. 1427–1434, Jul. 2012.
[87] S. L. Tay, A. S. M. A. Haseeb, M. R. Johan, P. R. Munroe, and M. Z. Quadir, "Influence of Ni nanoparticle on the morphology and growth of interfacial intermetallic compounds between Sn–3.8Ag–0.7Cu lead-free solder and copper substrate," *Intermetallics*, vol. 33, pp. 8–15, 2013.
[88] D. C. Lin, G. X. Wang, T. S. Srivatsan, M. Al-Hajri, and M. Petraroli, "Influence of titanium dioxide nanopowder addition on microstructural development and hardness of tin–lead solder," *Materials Letters*, vol. 57, no. 21, pp. 3193–3198, 2003.
[89] Y. Shi, J. Liu, Z. Xia, Y. Lei, F. Guo, and X. Li, "Creep property of composite solders reinforced by nano-sized particles," *J Mater Sci: Mater Electron*, vol. 19, no. 4, pp. 349–356, Apr. 2008.
[90] L. C. Tsao, "Suppressing effect of 0.5 wt.% nano-TiO2 addition into Sn–3.5Ag–0.5Cu solder alloy on the intermetallic growth with Cu substrate during isothermal aging," *Journal of Alloys and Compounds*, vol. 509, no. 33, pp. 8441–8448, 2011.
[91] L. C. Tsao, "Evolution of nano-Ag3Sn particle formation on Cu–Sn intermetallic compounds of Sn3.5Ag0.5Cu composite solder/Cu during soldering," *Journal of Alloys and Compounds*, vol. 509, no. 5, pp. 2326–2333, 2011.
[92] S. Y. Chang, C. C. Jain, T. H. Chuang, L. P. Feng, and L. C. Tsao, "Effect of addition of TiO2 nanoparticles on the microstructure, microhardness and interfacial reactions of Sn3.5AgXCu solder," *Materials & Design*, vol. 32, no. 10, pp. 4720–4727, 2011.

[93] L. C. Tsao and S. Y. Chang, "Effects of Nano-TiO2 additions on thermal analysis, microstructure and tensile properties of Sn3.5Ag0.25Cu solder," *Materials & Design*, vol. 31, no. 2, pp. 990–993, 2010.
[94] L. C. Tsao, C. H. Huang, C. H. Chung, and R. S. Chen, "Influence of TiO2 nanoparticles addition on the microstructural and mechanical properties of Sn0.7Cu nano-composite solder," *Materials Science and Engineering: A*, vol. 545, pp. 194–200, 2012.
[95] A. K. Gain, Y. C. Chan, and W. K. C. Yung, "Microstructure, thermal analysis and hardness of a Sn–Ag–Cu–1 wt% nano-TiO2 composite solder on flexible ball grid array substrates," *Microelectronics Reliability*, vol. 51, no. 5, pp. 975–984, 2011.
[96] Y. Tang, G. Y. Li, and Y. C. Pan, "Influence of TiO2 nanoparticles on IMC growth in Sn–3.0Ag–0.5Cu–xTiO2 solder joints in reflow process," *Journal of Alloys and Compounds*, vol. 554, pp. 195–203, 2013.
[97] Y. Li, X. Zhao, Y. Liu, Y. Wang, and Y. Wang, "Effect of TiO2 addition concentration on the wettability and intermetallic compounds growth of Sn3.0Ag0.5Cu–xTiO2 nano-composite solders," *J Mater Sci: Mater Electron*, vol. 25, no. 9, pp. 3816–3827, Jun. 2014.
[98] S. Y. Chang, C. C. Jain, T. H. Chuang, L. P. Feng, and L. C. Tsao, "Effect of addition of TiO2 nanoparticles on the microstructure, microhardness and interfacial reactions of Sn3.5AgXCu solder," *Materials & Design*, vol. 32, no. 10, pp. 4720–4727, 2011.
[99] X. Zhong and M. Gupta, "High Strength Lead-Free Composite Solder Materials using Nano Al2O3 as Reinforcement," *Advanced Engineering Materials*, vol. 7, no. 11, pp. 1049–1054, 2005.
[100] S. M. L. Nai, J. V. M. Kuma, M. E. Alam, X. L. Zhong, P. Babaghorbani, and M. Gupta, "Using Microwave-Assisted Powder Metallurgy Route and Nano-size Reinforcements to Develop High-Strength Solder Composites," *J. of Materi Eng and Perform*, vol. 19, no. 3, pp. 335–341, Apr. 2010.
[101] T. Fouzder, A. K. Gain, Y. C. Chan, A. Sharif, and W. K. C. Yung, "Effect of nano Al2O3 additions on the microstructure, hardness and shear strength of eutectic Sn–9Zn solder on Au/Ni metallized Cu pads," *Microelectronics Reliability*, vol. 50, no. 12, pp. 2051–2058, 2010.
[102] L. C. Tsao, S. Y. Chang, C. I. Lee, W. H. Sun, and C. H. Huang, "Effects of nano-Al2O3 additions on microstructure development and hardness of Sn3.5Ag0.5Cu solder," *Materials & Design*, vol. 31, no. 10, pp. 4831–4835, 2010.
[103] P. Babaghorbani, S. M. L. Nai, and M. Gupta, "Development of lead-free Sn-3.5Ag/SnO2 nanocomposite solders," *J Mater Sci: Mater Electron*, vol. 20, no. 6, pp. 571–576, Jun. 2009.
[104] T. Fouzder, I. Shafiq, Y. C. Chan, A. Sharif, and W. K. C. Yung, "Influence of SrTiO3 nano-particles on the microstructure and shear strength of Sn–Ag–Cu solder on Au/Ni metallized Cu pads," *Journal of Alloys and Compounds*, vol. 509, no. 5, pp. 1885–1892, 2011.
[105] A. K. Gain, T. Fouzder, Y. C. Chan, and W. K. C. Yung, "Microstructure, kinetic analysis and hardness of Sn–Ag–Cu–1 wt% nano-ZrO2 composite solder on OSP-Cu pads," *Journal of Alloys and Compounds*, vol. 509, no. 7, pp. 3319–3325, 2011.
[106] A. K. Gain, Y. C. Chan, and W. K. C. Yung, "Effect of additions of ZrO2 nano-particles on the microstructure and shear strength of Sn–Ag–Cu solder on Au/Ni

metallized Cu pads," *Microelectronics Reliability*, vol. 51, no. 12, pp. 2306–2313, 2011.
[107] C. Peng, J. Shen, and H. Yin, "Influences of ZrO2 nano-particles on the microstructures and microhardness of Sn8Zn1Bi–xZrO2/Cu solder joints," *J Mater Sci: Mater Electron*, vol. 24, no. 1, pp. 203–210, Jan. 2013.
[108] S. Xu, A. H. Habib, A. Prasitthipayong, and M. E. McHenry, "Effects of FeCo magnetic nanoparticles on microstructure of Sn-Ag-Cu alloys," *Journal of Applied Physics*, vol. 113, no. 17, p. 17A301, May 2013.
[109] N. Wu, S. Ismathullakhan, and Y. C. Chan, "Effect of 1 wt% ZnO nanoparticles addition on the microstructure, IMC development, and mechanical properties of high Bi content Sn–57.6Bi–0.4Ag solder on Ni metalized Cu pads," *J Mater Sci: Mater Electron*, vol. 25, no. 5, pp. 2169–2176, Mar. 2014.
[110] K. M. Kumar, V. Kripesh, and A. A. O. Tay, "Influence of single-wall carbon nanotube addition on the microstructural and tensile properties of Sn–Pb solder alloy," *Journal of Alloys and Compounds*, vol. 455, no. 1–2, pp. 148–158, 2008.
[111] M. M. Arafat, A. S. M. A. Haseeb, and M. R. Johan, "Interfacial reaction and dissolution behavior of Cu substrate in molten Sn-3.8Ag-0.7Cu in the presence of Mo nanoparticles," *Soldering and Surface Mount Technology*, vol. 23, no. 3, pp. 140–149, 2011.
[112] L. M. Pavlova, Y. I. Shtern, and R. E. Mironov, "Thermal expansion of bismuth telluride," *High Temp*, vol. 49, no. 3, pp. 369–379, Jun. 2011.
[113] *Processing and Fabrication of Advanced Materials XIII: Proceedings of a Conference Organized by National University of Singapore, Singapore Institute of Manufacturing Technology, Co-sponsored by American Society for Materials International (ASM Int.) (The Materials Information Society), Held December 6-8, 2004 at Pan-Pacific Hotel, Singapore*. World Scientific, 2005.
[114] K. J. Puttlitz and K. A. Stalter, *Handbook of Lead-Free Solder Technology for Microelectronic Assemblies*. CRC Press, 2004.
[115] D. Swenson, "The effects of suppressed beta tin nucleation on the microstructural evolution of lead-free solder joints," in *Lead-Free Electronic Solders*, Springer US, 2007, pp. 39–54.
[116] N.-C. Lee, *Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies*. Newnes, 2002.
[117] X. C. Tong, "Thermal Interface Materials in Electronic Packaging," in *Advanced Materials for Thermal Management of Electronic Packaging*, Springer New York, 2011, pp. 305–371.
[118] J. P. Gwinn and R. L. Webb, "Performance and testing of thermal interface materials," *Microelectronics Journal*, vol. 34, no. 3, pp. 215–222, Mar. 2003.
[119] A. L. Moore and L. Shi, "Emerging challenges and materials for thermal management of electronics," *Materials Today*, vol. 17, no. 4, pp. 163–174, May 2014.
[120] H. J. Goldsmid, "Applications of Thermoelectric Refrigeration," in *Thermoelectric Refrigeration*, Springer US, 1964, pp. 210–223.
[121] B. Poudel, Q. Hao, Y. Ma, Y. Lan, A. Minnich, B. Yu, X. Yan, D. Wang, A. Muto, D. Vashaee, X. Chen, J. Liu, M. S. Dresselhaus, G. Chen, and Z. Ren, "High-Thermoelectric Performance of Nanostructured Bismuth Antimony Telluride Bulk Alloys," *Science*, vol. 320, no. 5876, pp. 634–638, May 2008.

[122] X. B. Zhao, X. H. Ji, Y. H. Zhang, T. J. Zhu, J. P. Tu, and X. B. Zhang, "Bismuth telluride nanotubes and the effects on the thermoelectric properties of nanotube-containing nanocomposites," *Applied Physics Letters*, vol. 86, no. 6, p. 062111, Feb. 2005.
[123] R. Venkatasubramanian, E. Siivola, T. Colpitts, and B. O'Quinn, "Thin-film thermoelectric devices with high room-temperature figures of merit," *Nature*, vol. 413, no. 6856, pp. 597–602, 2001.
[124] H.-J. Kim, G. C. King, Y. Park, K. Lee, and S. H. Choi, "Thermoelectric Performance Enhancement by Surrounding Crystalline Semiconductors with Metallic Nanoparticles," Jul. 2011.
[125] B. Carlberg, "Integration of Nanofibrous Materials in Microsystem Applications – Process Development and Characterization," Doctoral thesis, Chalmers University of Technology, 2012.
[126] C. Zandén, "Functional Fiber Based Materials for Microsystem Applications," Doctoral thesis, Chalmers University of Technology, 2014.
[127] R. W. Cahn and P. Haasen, *Physical Metallurgy*. Elsevier, 1996.
[128] X. Luo, "Characterization of nano-scale materials for interconnect and thermal dissipation application in electronics packaging," Doctoral thesis, Chalmers University of Technology, 2014.
[129] K. Biswas, J. He, I. D. Blum, C.-I. Wu, T. P. Hogan, D. N. Seidman, V. P. Dravid, and M. G. Kanatzidis, "High-performance bulk thermoelectrics with all-scale hierarchical architectures," *Nature*, vol. 489, no. 7416, pp. 414–418, Sep. 2012.
[130] J. P. Fleurial, L. Gailliard, R. Triboulet, H. Scherrer, and S. Scherrer, "Thermal properties of high quality single crystals of bismuth telluride—Part I: Experimental characterization," *Journal of Physics and Chemistry of Solids*, vol. 49, no. 10, pp. 1237–1247, 1988.
[131] J. Navrátil, I. Klichová, S. Karamazov, J. Šrámková, and J. Horák, "Behavior of Ag Admixtures in Sb2Te3and Bi2Te3Single Crystals," *Journal of Solid State Chemistry*, vol. 140, no. 1, pp. 29–37, Oct. 1998.
[132] J. Yang, R. Chen, X. Fan, S. Bao, and W. Zhu, "Thermoelectric properties of silver-doped n-type Bi2Te3-based material prepared by mechanical alloying and subsequent hot pressing," *Journal of Alloys and Compounds*, vol. 407, no. 1–2, pp. 330–333, Jan. 2006.
[133] David Emin, "Effects of Charge Carriers'Interactions on Seebeck Coefficients," in *Thermoelectrics Handbook*, 0 vols., CRC Press, 2005, pp. 5–1–5–7.
[134] C. B. Satterthwaite and R. W. Ure, "Electrical and Thermal Properties of Bi2 Te3," *Phys. Rev.*, vol. 108, no. 5, pp. 1164–1170, Dec. 1957.
[135] M. Scheele, N. Oeschler, K. Meier, A. Kornowski, C. Klinke, and H. Weller, "Synthesis and Thermoelectric Characterization of Bi2Te3 Nanoparticles," *Adv. Funct. Mater.*, vol. 19, no. 21, pp. 3476–3483, Nov. 2009.