

# Hysteresis modeling in graphene field effect transistors

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Graphene field effect transistors with an  $Al_2O_3$  gate dielectric are fabricated on H-intercalated bilayer graphene grown on semi-insulating 4H-SiC by chemical vapour deposition. DC measurements of the gate voltage  $v_g$  versus the drain current  $i_d$  reveal a severe hysteresis of clockwise orientation. A capacitive model is used to derive the relationship between the applied gate voltage and the Fermi energy. The electron transport equations are then used to calculate the drain current for a given applied gate voltage. The hysteresis in measured data is then modeled via a modified Preisach kernel. © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4913209>]

## I. INTRODUCTION

Graphene has attracted a great deal of interest from diverse range of disciplines due to its unique band structure and electron transport properties. A wide range of graphene based technologies, including electrochemical sensors,<sup>1</sup> infrared detectors,<sup>2</sup> and field effect transistors (FETs), have been presented. Particular interest has been directed towards the development of a graphene based technology for high frequency electronic devices. Though frequently observed,<sup>3-7</sup> a theoretical treatment of field effect hysteresis in graphene FETs has not yet been presented in the context of experimental data.

The field effect hysteresis is not unique to graphene. Gate hysteresis has been observed in a variety of semiconductor materials, such as AlGaAs/GaAs heterostructures,<sup>8,9</sup> AlGaN/GaN MOS heterostructures,<sup>10</sup> and (4,6)H-SiC MOS structures.<sup>11,12</sup> The hysteresis in MOS structures is usually attributed to charge trapping at the semiconductor/dielectric interface, ion drift within the insulator, or space charge effects related to dielectric polarization. Charge trapping generates a hysteresis of anti-clockwise orientation,<sup>9,13</sup> whereas polarization and space charge effects generate a hysteresis with clockwise orientation.<sup>14</sup> Technology development often aims at the elimination of hysteretic phenomena for the purpose of reducing bias dependent instabilities. In addition to providing insight into the origin of the hysteresis effect, an accurate model based on first principles provides a deeper understanding into the device physics and electron transport properties of MOS structures.

Hysteresis is observed in graphene field effect transistors (GFETs) of many types, including exfoliated flakes,<sup>4,15</sup> transferred large area layers on  $SiO_2$  and  $SiO_2/Si_3N_4$ ,<sup>16</sup> and as-grown layers SiC grown by chemical vapour deposition (CVD)<sup>17</sup> and sublimation. In this work, a drain hysteresis of similar character is clearly seen in H-intercalated CVD bilayer GFETs when measuring the drain current ( $i_d$ ) as a function of gate voltage ( $v_g$ ). In the absence of hysteresis, the drain current density ( $\mathbf{J}$ ) may be calculated from the electron ( $n$ ) and hole ( $p$ ) densities by the following equation:

$$\mathbf{J} = e[\mu_n n(\epsilon_f) + \mu_p p(\epsilon_f)]\mathbf{E}. \quad (1)$$

The electron and hole densities are themselves a function of the Fermi energy ( $\epsilon_f$ ). During FET operation,  $\epsilon_f$  is modulated by  $v_g$ . In Eq. (1),  $e$  is the fundamental charge,  $\mu_{n,p}$  are the electron and hole mobilities, and  $\mathbf{E}$  is the electric field applied between source and drain.

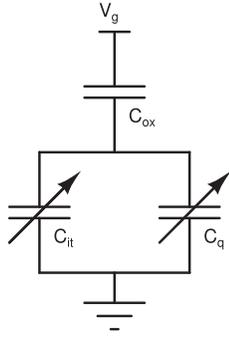
The objective of this work is to extend Eq. (1) to include a hysteretic effect and to apply quantitative hysteresis models to GFET data. In Sec. II, the metal/oxide/semi-metal (MOS<sub>m</sub>) system is modeled as a capacitive divider, and a relation expressing the dependence of  $\epsilon_f$  on  $v_g$  is presented. The current saturation observed in graphene is modeled by considering Fermi level pinning interface effects. In Sec. III, the hysteresis is introduced by considering a hysteretic Fermi energy  $\mathcal{P}[\epsilon_f]$ . The operator  $\mathcal{P}$  is a modified Preisach kernel which generates a hysteresis on  $\epsilon_f$ . Given  $\mathcal{P}[\epsilon_f]$ , it is straightforward to calculate the hysteretic current density via substitution of  $\mathcal{P}[\epsilon_f]$  for  $\epsilon_f$  in Eq. (1). Details regarding device fabrication and material/device characterization are presented in Sec. IV. Additional details regarding the computational implementation of the Preisach kernel and hysteresis optimization are also presented. In Secs. V and VI, this model is applied to DC and low-frequency (LF) hysteresis measurements on the GFETs, and the resulting non-linear GFET models obtained from hysteresis optimization are shown. In Sec. VII, the physical origin of the hysteresis is discussed in the context of the experimental results.

## II. CAPACITANCE MODELING

To generate  $\mathcal{P}[\epsilon_f]$ , it is necessary to find the relationship between the Fermi energy and gate voltage. A common approach is to model the MOS<sub>m</sub> structure as a capacitive divider (Figure 1).<sup>18</sup> Here,  $C_{ox}$ ,  $C_q$ , and  $C_{it}$  represent the oxide, density of states (i.e., quantum), and interface charge capacitances per unit area, respectively.

The following relation follows from voltage division:

$$\frac{\partial v_{\epsilon_f}}{\partial v_g} = \frac{C_{ox}}{C_{ox} + C_{it} + C_q}. \quad (2)$$

FIG. 1. The capacitive divider model for the graphene MOS<sub>m</sub> system.

Here,  $v_{\epsilon_f} = e\epsilon_f$  represents the voltage at the graphene dielectric interface.  $C_q$  is obtained by differentiating the carrier density with respect to energy ( $C_q = \partial_v Q = e\partial_\epsilon(en)$ )<sup>19,20</sup>

$$\begin{aligned} e^2\partial_\epsilon n &= e^2\partial_\epsilon \int \rho(\epsilon)f(\epsilon : \epsilon_f, \beta)d\epsilon \\ &\approx e^2 \int \rho(\epsilon)\delta(\epsilon - \epsilon_f)d\epsilon \\ &= e^2\rho(\epsilon_f). \end{aligned} \quad (3)$$

In Eq. (3), the carrier density  $n(\epsilon_f)$  is expressed as the product of the density of states in graphene  $\rho(\epsilon)$  and the Fermi Dirac distribution  $f(\epsilon : \epsilon_f, \beta)$ , where  $\beta = (k_b T)^{-1}$ . The integral is evaluated via the zero temperature approximation such that  $\partial_\epsilon f(\epsilon : \epsilon_f, \beta) \approx \delta(\epsilon - \epsilon_f)$ .

In AB-stacked bilayer graphene, the density of states is calculated from a tight binding Hamiltonian with one interlayer coupling term ( $\gamma_\perp$ ). The case of monolayer graphene is obtained by considering  $\gamma_\perp = 0$ . Taking the total density of states to be the sum of the low and high energy approximations gives the following:<sup>21–23</sup>

$$\rho(\epsilon) = \frac{g_s g_v}{2\pi} \frac{1}{(\hbar v_f)^2} \left[ |\epsilon_f| + \frac{\gamma_\perp}{2} \right]. \quad (4)$$

Here,  $\hbar$  is the reduced Planck constant,  $g_{s,v}$  are the spin and valley degeneracies,  $v_f = 10^8$  cm/s is the Fermi velocity in graphene, and  $\gamma_\perp \approx 0.4$  eV is the interlayer coupling constant.<sup>21</sup> In graphene, the ideal  $C_q$  exhibits a linear dependence on  $\epsilon_f$ . It is useful to introduce a constant for the prefactor in Eq. (4)

$$\eta = \frac{g_s g_v}{2\pi} \frac{1}{(\hbar v_f)^2}. \quad (5)$$

The capacitance due to interface charge may be obtained similarly by  $C_{it} = \partial_v Q_{it} = e^2 D_{it}(\epsilon_f)$ . Substituting for  $C_q$  and  $C_{it}$  in Eq. (2) leads to the resulting differential equation

$$\frac{\partial v}{\partial \epsilon} = \frac{1}{e} \left\{ 1 + \frac{e^2}{C_{ox}} [\rho(\epsilon) + D_{it}(\epsilon)] \right\}. \quad (6)$$

Substituting for  $\rho(\epsilon)$  and integrating over  $\epsilon \in [0, \epsilon_f]$  and  $v \in [v_D, v_g]$  yields the following relation between the Fermi energy and the applied gate voltage:

$$\Delta_e v = \epsilon_f + \frac{e^2 \eta}{2C_{ox}} (\epsilon_f^2 + \epsilon_f \gamma_\perp) + \frac{e^2}{C_{ox}} \int_0^{\epsilon_f} D_{it} d\epsilon_f. \quad (7)$$

Here,  $\Delta_e v = e(v_g - v_D)$ , where  $v_D$  is the Dirac voltage (i.e., the gate voltage where  $\epsilon_f = 0$ ). In Secs. II A and II B, two solutions to Eq. (7) are presented. In Sec. II A, the case of a constant  $D_{it}$  is examined, and in Sec. II B, the case of an empirically modeled  $D_{it}$  is considered. The empirically modeled case is selected to generate Fermi level pinning.

### A. Constant $D_{it}$

In order to obtain a closed form solution to Eq. (7), it is useful to select a  $D_{it}(\epsilon_f)$  to be a constant  $D_{it}^0$ . In this case, it is possible to obtain an analytic expression for Fermi energy as a function of gate voltage  $v_g$ :

$$\Delta_e v = \left[ 1 + \frac{e^2}{C_{ox}} \left( \frac{\eta \gamma_\perp}{2} + D_{it}^0 \right) \right] \epsilon_f + \left[ \frac{e^2 \eta}{2C_{ox}} \right] \epsilon_f^2. \quad (8)$$

Solving for  $\epsilon_f$  yields the following quadratic relation:

$$\epsilon_f = \frac{1}{2a} \left[ \pm \sqrt{4a\Delta_e v + b^2} - b \right], \quad (9)$$

where the constants are given by the following:

$$\begin{aligned} a &= \frac{e^2 \eta}{2C_{ox}} \\ b &= \left[ 1 + \frac{e^2}{C_{ox}} \left( \frac{\eta \gamma_\perp}{2} + D_{it}^0 \right) \right]. \end{aligned} \quad (10)$$

The effect of the quantum capacitance is to introduce a  $\epsilon_f \propto \sqrt{\Delta_e v}$  such that there is a weak saturating behavior in  $\epsilon_f$ . The Dirac voltage introduces a shift into the function and can be estimated from experimental data. Reducing  $C_{ox}$  and increasing  $D_{it}^0$  have the same effect of increasing  $b$ , which results in reduced gate control over  $\epsilon_f$ .

### B. The Lorentz- $\delta$ model

Experimental results suggest that the saturation of  $\epsilon_f$  is much stronger than  $\sqrt{\Delta_e v}$  for large gate voltages. This Fermi level pinning effect can be introduced by considering a charge density at the graphene dielectric interface  $\sigma_{it}(\epsilon_f) = e \int_0^{\epsilon_f} D_{it}$ . The interface charge density is modeled by two  $\delta$ -function like Lorentzian distributions located at ( $\epsilon_0^i > 0$ ) and ( $\epsilon_0^i < 0$ ). The distributions have additional broadening which is also modeled by a Lorentzian distribution

$$D_{it} = \sum_{n,p} D_{it,0}^i \mathcal{F}(\epsilon_f : \epsilon_0^i, \gamma_0^i) + D_{it,\delta}^i \mathcal{F}_\delta(\epsilon_f : \epsilon_0^i, \gamma_\delta^i). \quad (11)$$

Here,  $\mathcal{F}(\epsilon_f : \epsilon_0^i, \gamma_0^i)$  is a Lorentzian distribution centered on  $\epsilon_0^i$  with a width of  $\gamma_0^i$

$$\mathcal{F}(\epsilon_f : \epsilon_0^i, \gamma_0^i) = \frac{1}{\pi \gamma_0^i \left[ 1 + \left( \frac{\epsilon_f - \epsilon_0^i}{\gamma_0^i} \right)^2 \right]}. \quad (12)$$

The sum in Eq. (11) extends over two indices,  $n$  and  $p$ , representing pinning during electron ( $\epsilon_f > 0$ ) and hole conduction ( $\epsilon_f < 0$ ), respectively. With the Lorentz- $\delta$  model, Eq. (7) becomes a transcendental equation which must be solved numerically. To achieve the Lorentz- $\delta$  effect, one requires that  $\gamma_\delta^i \ll \gamma_0^i$ . This model is generally considered to be valid if the following holds for a given time varying gate voltage:

$$\epsilon_0^p < \epsilon_f < \epsilon_0^n. \quad (13)$$

When  $v_g$  becomes large, the narrow Lorentzian distributions cause a rapid increase in  $D_{it}$ . This forces  $\epsilon_f$  to plateau near  $\epsilon_0^n$  and  $\epsilon_0^p$  (Figure 2). The saturating behavior of  $\epsilon_f$  manifests as a saturation in the electron and hole densities generating current saturation in the device. The choice of the Lorentz- $\delta$  model implies that the source of  $D_{it}$  is a resonant process. In particular, the two narrow peaks are associated with discrete energy levels at which fixed charge is generated. Although the Lorentz- $\delta$  model is semi-empirically motivated, a context can be provided (see Sec. VII B).

### III. HYSTERESIS MODELING

Given  $D_{it}$ , it is possible to calculate the Fermi energy  $\epsilon_f$  and drain current density  $\mathbf{J}$  as a function of gate voltage. The hysteresis is then introduced into  $\mathbf{J}$  by considering a hysteretic Fermi energy. This is done by evaluating a Preisach kernel  $\mathcal{P}$  on the non-hysteretic Fermi energy. Let  $\epsilon_f^0 \in [0, t)$  represent a time varying Fermi energy in absence of hysteresis. A hysteretic Fermi energy is then represented by

$$\epsilon_f = \mathcal{P}[\epsilon_f^0]. \quad (14)$$

Such an operator was first introduced by Preisach in 1935 to describe the hysteresis in the magnetization as a function of the applied magnetic field.<sup>24</sup>

#### A. The functional relay

In modeling the graphene FET, the Preisach kernel  $\mathcal{P}$  is constructed via a linear superposition of *functional relays*  $\mathcal{R}_{\epsilon_-, \epsilon_+}$ :

$$\mathcal{R}_{\epsilon_-, \epsilon_+}[\epsilon_f^0 : \alpha] = A \begin{cases} \alpha \epsilon_f^0 - 1, & \text{if } \epsilon < \epsilon_- \\ \alpha \epsilon_f^0 + 1, & \text{if } \epsilon > \epsilon_+ \\ \alpha \epsilon_f^0 + \kappa, & \text{otherwise.} \end{cases} \quad (15)$$

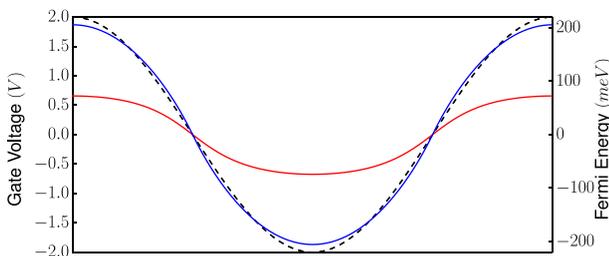


FIG. 2.  $\epsilon_f$  shown as a function of  $v_g$  in the absence of the Lorentz- $\delta$  effect (blue) and in the Lorentz- $\delta$  model (red) for a sinusoidal gate voltage with an amplitude of 2 V (dashed). The blue curve demonstrates the  $\sqrt{\Delta_g v}$  dependence of  $\epsilon_f^0$  on  $v_g$ , while the red curve shows a Fermi level pinning effect which is symmetric about  $\epsilon_f = 0$ .

Here,  $\kappa = -1$  if  $\epsilon_f^0$  crosses the threshold  $\epsilon_-$ ,  $\kappa = 1$  if  $\epsilon_f^0$  crosses the threshold  $\epsilon_+$ , and  $A$  is a scaling parameter such that  $\mathcal{R}_{\epsilon_-, \epsilon_+}[\epsilon_f^0 : \alpha]$  is defined over the same range as  $\epsilon_f^0$ . The introduction of the term  $\alpha \epsilon_f^0$  is a divergence from the traditional Preisach model for  $\alpha > 0$ . The effect of  $\alpha$  is to build the behavior of  $\epsilon_f^0$  into the relay operator. As  $\alpha \rightarrow \infty$ . and  $A \rightarrow \alpha^{-1}$ , then  $\mathcal{R}_{\epsilon_-, \epsilon_+}[\epsilon_f^0 : \alpha] \rightarrow \epsilon_f^0$ . The action of the functional relay on a given  $\epsilon_f^0(v_g)$  is shown in Figure 3. Here,  $\epsilon_f^0(v_g)$  is a solution to Eq. (7) in the case of a Lorentz- $\delta$  model obtained from measured GFET data (Fig. 4).

The functional relay operator is alternatively defined in terms of its mean value  $\epsilon_0 = (\epsilon_- + \epsilon_+)/2$  and half width  $\epsilon_\delta = (\epsilon_+ - \epsilon_-)/2$ . This form of the relay is what commonly appears in the Preisach kernel

$$\mathcal{R}_{\epsilon_-, \epsilon_+}[\epsilon_f^0 : \alpha] = \mathcal{R}_{\epsilon_0 - \epsilon_\delta, \epsilon_0 + \epsilon_\delta}[\epsilon_f^0 : \alpha]. \quad (16)$$

#### B. The Preisach kernel

The Preisach kernel is obtained by integrating over an infinite number of functional relay elements of mean value  $\epsilon_0$  and half width  $\epsilon_\delta$ .<sup>25</sup> The functional relay parameter  $\alpha$  is considered to a constant of the kernel<sup>25,26</sup>

$$\mathcal{P}[\epsilon_f^0] = \int_0^\infty \int_{-\infty}^\infty \omega(\epsilon_0, \epsilon_\delta) \mathcal{R}_{\epsilon_0 - \epsilon_\delta, \epsilon_0 + \epsilon_\delta}[\epsilon_f^0 : \alpha] d\epsilon_0 d\epsilon_\delta. \quad (17)$$

The kernel is evaluated by breaking the time varying Fermi energy  $\epsilon_f^0(t)$  into monotonically increasing  $\epsilon_f^+(t)$  and decreasing  $\epsilon_f^-(t)$  steps. In order for the model to be fully determined, it is necessary to select a weighting function  $\omega(\epsilon_0, \epsilon_\delta)$  (see Sec. III C)

$$\mathcal{P}[\epsilon_f^0] = A \int_{\epsilon_f^+(t)} [\alpha \epsilon_f^0 + 1] \omega(\epsilon_0, \epsilon_\delta) d\epsilon_0 d\epsilon_\delta + A \int_{\epsilon_f^-(t)} [\alpha \epsilon_f^0 - 1] \omega(\epsilon_0, \epsilon_\delta) d\epsilon_0 d\epsilon_\delta. \quad (18)$$

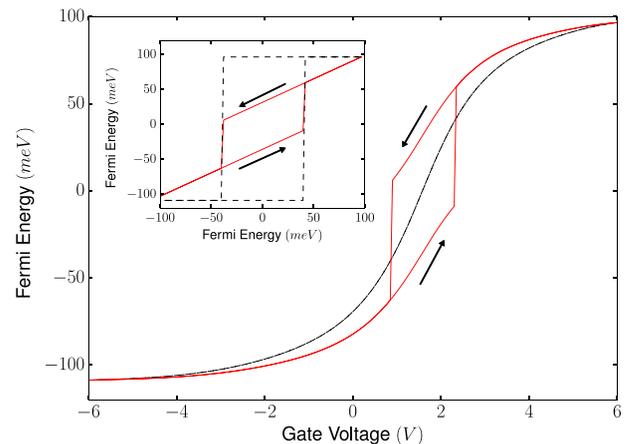


FIG. 3. The characteristic of a functional relay operator ( $\alpha = 20.0$ ) on a typical  $\epsilon_f^0(v_g)$  in  $[v_g, \epsilon_f^0]$  plane for  $\epsilon_0 = 0$  meV and  $\epsilon_\delta = 40$  meV. (Inset) The same relay plotted in the  $[\epsilon_f^+, \epsilon_f^-]$  plane (red) and the analogous case of a pure Preisach relay  $\alpha = 0.0$  (dashed). Arrows indicate the direction of traversal for monotonically increasing/decreasing inputs.

The integrals over monotonically increasing and decreasing sections of  $\epsilon_f^0$  yield the lower and upper branches of the hysteresis, respectively. This allows for an intuitive interpretation of the behavior of  $\mathcal{P}[\epsilon_f^0]$ . Generally,  $\mathcal{P}[\epsilon_f^0]$  describes nested hysteresis loops with ascending and descending branches. Note that the scaling factor  $A$  is selected such that the endpoints of ascending and descending branches of  $\mathcal{P}[\epsilon_f^0]$  are equivalent to those of  $\epsilon_f^0$ . Once the hysteretic Fermi energy is found, it is possible to calculate the channel carrier density as a function of gate voltage

$$n = \eta \int_0^\infty \left[ \epsilon + \frac{\gamma_\perp}{2} \right] f(\epsilon : \epsilon_f, \beta) d\epsilon. \quad (19)$$

The hole density  $p$  is obtained via transforming  $(\epsilon, \epsilon_f) \rightarrow (-\epsilon, -\epsilon_f)$  and performing integration over  $\epsilon \in [0, -\infty)$ . Given the carrier density, it is possible to calculate the current density

$$\mathbf{J} = e[\mu_n n(\mathcal{P}[\epsilon_f^0]) + \mu_p p(\mathcal{P}[\epsilon_f^0]) + \mu_r p_r] \mathbf{E}. \quad (20)$$

Here,  $\mu_n$  and  $\mu_p$  are the electron and hole low field mobilities. Since the electron and hole densities inherit hysteretic behavior via  $\mathcal{P}[\epsilon_f^0]$ , it follows that the current density is also hysteretic. The current density in absence of hysteresis is recovered by substituting  $\epsilon_f^0$  for  $\mathcal{P}[\epsilon_f^0]$  in Eq. (20). The current density relationship also includes a parasitic source/drain conductance term  $\sigma_r = e\mu_r p_r$ , where  $p_r$  is the parasitic carrier density.<sup>27</sup>

### C. The weighting function $\omega(\epsilon_0, \epsilon_\delta)$

The behavior of the hysteresis operator is determined by the weighting function  $\omega(\epsilon_0, \epsilon_\delta)$ . The purpose of  $\omega(\epsilon_0, \epsilon_\delta)$  is to assign a normalized weight to the functional relay located at  $\mathcal{R}_{\epsilon_0 - \epsilon_\delta, \epsilon_0 + \epsilon_\delta}$ . In most hysteretic models, the density function is assumed to be an analytic function in the  $[\epsilon_0, \epsilon_\delta]$  plane. Common choices include the elliptic Gaussian,<sup>28</sup> the Lorentz distribution,<sup>29</sup> and the Derivative Arc Tangent (DAT) function.<sup>30</sup> Discrete density functions have also been successfully used to describe hysteretic systems.<sup>31</sup> In this work, a novel approach based on error functions is used. The Preisach measure is assumed to obey the separation ansatz

$$\omega(\epsilon_0, \epsilon_\delta) = \omega_0(\epsilon_0) \omega_\delta(\epsilon_\delta). \quad (21)$$

The terms  $\omega_0$  and  $\omega_\delta$  describe how the functional relays are distributed in terms of energy and half-width. The  $\omega_0$  term describes where the dominant contribution to the hysteresis is in energy, while  $\omega_\delta$  along with the functional relay parameter  $\alpha$  describes the degree of hysteresis opening. For GFET hysteresis modeling, the difference of two Gaussian cumulative distribution functions is chosen for  $\omega_0$  and  $\omega_\delta$

$$\omega_{0,\delta} = \frac{1}{2} \left[ \operatorname{erf} \left( \frac{\epsilon_{0,\delta} - \epsilon_{0,\delta}^0}{\sqrt{2}\sigma_{0,\delta}^0} \right) - \operatorname{erf} \left( \frac{\epsilon_{0,\delta} - \epsilon_{0,\delta}^1}{\sqrt{2}\sigma_{0,\delta}^1} \right) \right]. \quad (22)$$

It is important that  $\epsilon_{0,\delta}^i$  and  $\sigma_{0,\delta}^i$  are selected such that  $0 < \omega(\epsilon_0, \epsilon_\delta) < 1$  for all  $\epsilon_0$  and  $\epsilon_\delta$ . This ensures that all relays in the Preisach kernel have the same orientation.

## IV. METHODS

Graphene monolayers plus a carbon buffer layer are grown on semi-insulating  $1 \text{ cm}^2$  4H-SiC substrates in a CVD reactor by thermal decomposition of  $\text{C}_3\text{H}_8$ .<sup>32</sup> The samples are then *in-situ* intercalated with hydrogen to produce quasi-free standing bilayer graphene.<sup>33</sup> GFETs are then fabricated via electron beam lithography (EBL) as shown in Figure 4.<sup>34</sup> The most relevant step in the fabrication in this work is the deposition of the  $\text{Al}_2\text{O}_3$  gate dielectric. Atomic layer deposition (ALD) of  $\text{Al}_2\text{O}_3$  is performed via thermal decomposition of  $\text{Al}_2(\text{CH}_3)_6$  and  $\text{H}_2\text{O}$ . Deposition begins with electron beam evaporation and subsequent oxidation at  $180^\circ\text{C}$  of 1–2 nm of Al metal. This yields a nucleation layer  $\approx 2\text{--}3$  nm in thickness. This step is needed in order to provide adequate nucleation for the subsequent ALD growth.<sup>35</sup> The process then continues with the deposition of an additional 10 nm of  $\text{Al}_2\text{O}_3$  by ALD at  $300^\circ\text{C}$ . Generally, this method produces a low quality  $\text{Al}_2\text{O}_3$  film which is polycrystalline to amorphous in nature. In this work, Al was chosen as a gate metal in order to minimize the gate leakage current  $i_g$ .

All measurements are performed at low drain bias in order to probe the low field regime. Measuring at low drain bias also reduces the stress on the device during measurement, and minimizes the coupling effect between the gate and drain biases. H-intercalated devices are typically p-type and exhibit carrier densities on the order of  $1 \times 10^{13} \text{ cm}^{-2}$ . Measurements on six separate  $100 \times 100 \mu\text{m}^2$  Van der Pauw structures are performed using a Biorad HL5500PC Hall System in order to determine the average low field Hall mobility  $\mu_p$  and carrier density  $n_p$  of the material. The contact resistance  $r_c$  is obtained by measuring several transfer length method (TLM) structures fabricated on the same chip. The intrinsic electric field is then calculated by accounting for nonzero  $r_c$  (Eq. (23))

$$|\mathbf{E}| = \left[ v_d - i_d \left( \frac{r_c}{w_{ch}} \right) \right] \frac{1}{l_{ch}}. \quad (23)$$

The relative permittivity of the oxide is estimated ( $\epsilon_r$ ) via MOS capacitance measurements on identically grown  $\text{Al}_2\text{O}_3$  films on Si. The dimensions of the devices measured in this work along with several other important parameters are

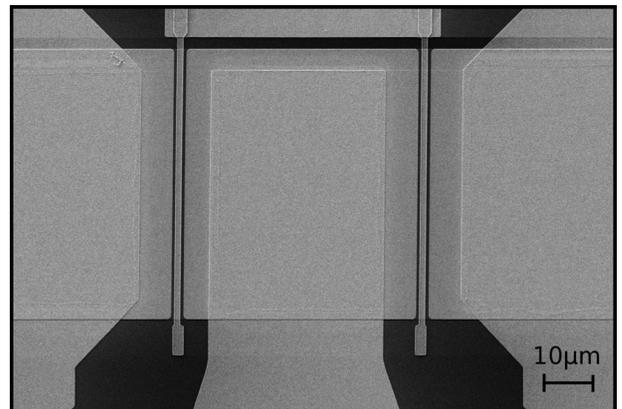


FIG. 4. A scanning electron micrograph of an Al gated  $2 \times 50 \mu\text{m}$  co-planar GFET used for DC/LF hysteresis measurements and modeling.

TABLE I. The measured device parameters needed for hysteresis modeling.  $l_g$  is the gate length,  $l_{ch}$  is the source-drain distance,  $w_{ch}$  is the channel width,  $t_{ox}$  is the oxide thickness, and  $\epsilon_r$  is the relative permittivity of the gate dielectric. Additionally,  $\mu_p$  is the Hall mobility,  $n_p$  is the carrier density,  $r_c$  is the contact resistance. The maximum gate leakage  $i_g$  is also shown.

Device		Measured			
$l_g$	1.0	( $\mu\text{m}$ )	$\mu_p$	1980	( $\text{cm}^2/\text{V s}$ )
$l_{ch}$	2.5	( $\mu\text{m}$ )	$n_p$	1.01	( $10^{13}\text{cm}^{-2}$ )
$w_{ch}$	50	( $\mu\text{m}$ )	$r_c$	150	( $\Omega\cdot\mu\text{m}$ )
$t_{ox}$	13.0	(nm)	$i_g$	$\leq 5$	(pA)
$\epsilon_r$	6.0				

shown in Table I. It is important to note that there is a degree of non-uniformity in the device properties. The minimum (maximum) mobility of the Hall structures was 1760(2200)  $\text{cm}^2/\text{V s}$ , and the minimum(maximum) carrier density was  $0.96 \times 10^{13}$  ( $1.09 \times 10^{13}$ )  $\text{cm}^{-2}$ . Similar variations were observed in other parameters.

Hysteresis modeling and parameter optimization are computationally challenging. Each iteration in the optimization routine consists of testing  $2^n$  complete hysteresis curves against measured data, where  $n \geq 9$  is the total number of parameters in the optimization. Furthermore, the generation of each hysteresis curve requires the summing over a large number ( $\geq 16^4$ ) of functional relays. In order to overcome these challenges, a massively parallel computation scheme employing a graphics processor (nVidia GeForce 640GT GPU) was developed. The Preisach operator (Eq. (18)), hysteresis scaling, and calculation of the carrier densities (Eq. (19)) are implemented in single CUDA (Compute Unified Device Architecture) kernel. A tail recursive entropy minimizing optimization algorithm is implemented using a custom built Python C extension. Each step in the optimization routine involves  $2^n$  calls to the CUDA kernel.

Standard routines seek to optimize  $\alpha$  along with the eight constants of  $\omega(\epsilon_0, \epsilon_\delta)$ . Using this method, each recursive step in the standard optimization routine is of order 5 s and adequate convergence is typically achieved in  $< 100$  iterations. The GPU implemented kernel offers a speed improvement of  $\approx 1000\times$  compared to traditional CPU implementations, thus allowing for rapid optimization cycles despite the large number of parameters in the model and the complexity of the Preisach kernel. Once optimized values are obtained, the same CUDA kernel is used to generate high precision hysteresis curves with  $\geq 16^5$  functional relays in  $\leq 500$  ms.

## V. DC HYSTERESIS MODELING

DC hysteresis measurements are performed on bilayer graphene FETs using a semiconductor parameter analyzer (HP-4156B) at 300 K with an integration time of 20 ms per bias point. The gate bias is swept repeatedly in the forward and reverse direction, and the extrema of the sweep are increased from  $\pm 1$  V to  $\pm 6$  V in intervals of 1 V, and the sweep rate is held constant at 4.87 V/s for all hysteresis curves. The drain bias ( $v_d$ ) is kept at a low constant value of

50 mV. The DC measurements are made in order to determine whether the observed hysteresis consists of nested loops, such as those described by a Preisach operator. Each measurement consists of multiple sweeps in order to probe the reversibility of the physical process which generates hysteresis. From these measurements, it is also possible to estimate the parameters of  $D_{it}$  and to assess the general behavior of  $\omega(\epsilon_0, \epsilon_\delta)$ . Other parameters, such as the majority/minority carrier mobilities  $\mu_p$  and  $\mu_n$ , the parasitic conductivity  $\sigma_r$ , and the Dirac Voltage  $v_D$ , are also extracted via accurate models of measured data.

To generate a hysteresis model,  $\epsilon_f^0(v_g)$  and  $\mathbf{J}$  are first calculated in the absence of the hysteresis for an initial  $D_{it}$  (Eqs. (7) and (20)). By comparing these results to measured data,  $\mu_{n,p}$ ,  $\sigma_r$ ,  $v_D$ , and  $D_{it}$  can be estimated prior to hysteresis optimization. Generally, a Lorentz- $\delta$  model is assumed for  $D_{it}$ . An optimization routine is performed on  $\mathbf{J}$  in order to find appropriate values for  $\omega(\epsilon_0, \epsilon_\delta)$  and  $\alpha$ . The optimization process usually includes modifications to  $\mu_{n,p}$ ,  $\sigma_r$ , and  $v_D$  from the initial modeling in absence of hysteresis. This modeling procedure is repeated for each curve in the data set for a fixed  $D_{it}$ .

Once an accurate fit has been achieved for each measured hysteresis curve, a final model can be obtained by averaging over the parameters of each modeled curve. This final averaged model then serves as a general model of the device in the absence of hysteretic effects. The hysteresis is then included by considering  $\omega(\epsilon_0, \epsilon_\delta)$  and  $\alpha$  from the optimization of each curve. The parameters extracted from hysteresis modeling of the measured data shown in Figure 5 are given in Table II. The model parameters define  $i_d(v_g)$  in the absence of hysteretic effects.

Using the parameter values from Table II and the density functions obtained from the optimization of each hysteresis curve, the hysteretic/non-hysteretic Fermi energy and current density are calculated as shown in Figure 6. The Preisach kernel generates nested hysteresis loops in the Fermi energy which in turn leads to hysteretic current loops which closely resemble the measured data shown in Figure 5.

The shape of  $\omega(\epsilon_0, \epsilon_\delta)$  indicates which functional relays are most active in the Preisach kernel. Figure 7 shows  $\omega(\epsilon_0, \epsilon_\delta)$  for the  $[-6, 6]$  V DC hysteresis sweep shown in Figure 5. It should be noted that all hysteresis sweeps in Figure 5 are modeled using similar  $\omega(\epsilon_0, \epsilon_\delta)$ . The shape of  $\omega(\epsilon_0, \epsilon_\delta)$  indicates strong hysteretic activity when  $\epsilon_f = 0$  changes sign indicating that the hysteresis is maximally open near  $v_D$ .

The mean Dirac voltage ( $v_D$ ) extracted from the hysteresis curves in Fig. 5 is 1.77 V. This global  $v_D$  defines the point of minimum conduction in absence of hysteresis. In the DC data, the extracted  $v_D$  generally falls between the two minima of the measured hysteresis curves. In the modeling of individual hysteresis curves, a drift of the Dirac point towards negative bias is observed for increasing sweep amplitude. This drift is attributed to the accumulation of positive charge at the graphene/dielectric interface. The hole mobility  $\mu_p$  obtained from the extraction is consistent with the Hall measurements obtained from separate Van der Pauw

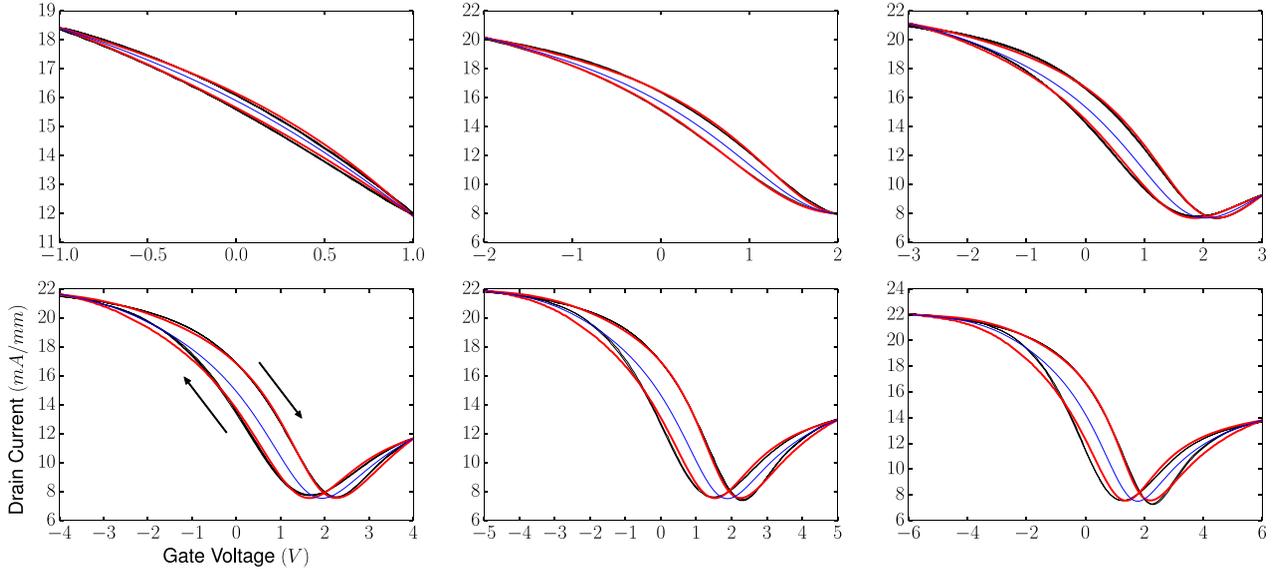


FIG. 5. Measured and modeled hysteresis curves for hysteretic  $v_g$  sweeps of increasing amplitude for a bilayer GFET. Each panel shows the measured data (black), the result of hysteresis modeling and optimization (red), and the calculated current in the absence of hysteretic effects (blue). The extrema of the sweeps range from  $\pm 1$  V (top left) to  $\pm 6$  V (bottom right). The drain bias is maintained at a constant 50 mV for the entire data set. Arrows indicate the orientation of the hysteretic effect, and all hysteresis curves are obtained at a constant sweep rate of 4.87 V/s.

TABLE II. The mean parameter values for the device model extracted for the DC hysteresis curves shown in Figure 5. Values for  $D_{it}^0$  and  $D_{it}^\delta$  are given in  $10^{13}$  ( $\text{cm}^{-2}$ ). The maximum opening of the modeled hysteresis  $\Delta_v$  of the  $[-5,5]$  V curve is also tabulated.

$D_{it}^p$			$D_{it}^n$			Material		
$\epsilon_0^p$	-110	(meV)	$\epsilon_0^n$	102	(meV)	$\mu_p$	1690	( $\text{cm}^2/\text{V s}$ )
$\gamma_0^p$	20	(meV)	$\gamma_0^n$	25	(meV)	$\mu_n$	1100	( $\text{cm}^2/\text{V s}$ )
$\gamma_\delta^p$	1.4	(meV)	$\gamma_\delta^n$	2.5	(meV)	$\sigma_r$	0.114	( $\text{k } \Omega^{-1}$ )
$D_{it,0}^p$	2.25	( $\text{cm}^{-2}$ )	$D_{it,0}^n$	2.25	( $\text{cm}^{-2}$ )	$v_D$	1.77	(V)
$D_{it,\delta}^p$	2.75	( $\text{cm}^{-2}$ )	$D_{it,\delta}^n$	2.75	( $\text{cm}^{-2}$ )	$\Delta_v$	0.93	(V)

structures. An electron mobility of  $\mu_n = 1100 \text{ cm}^2/\text{Vs}$  is also obtained from the modeled data. This conduction asymmetry between majority and minority carriers in graphene is also observed in other work.<sup>36,37</sup>

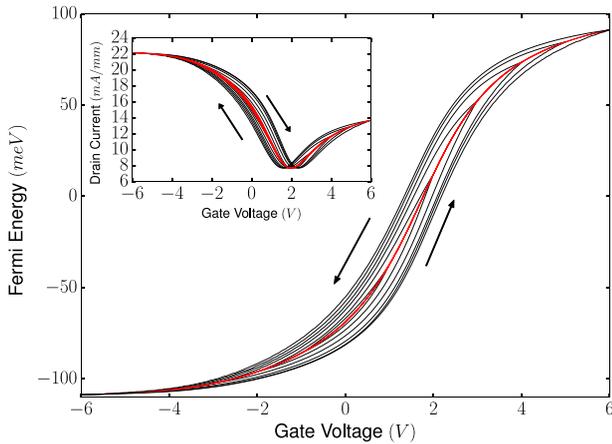


FIG. 6. The calculated behavior of the Fermi energy  $\epsilon_f$  as a function of gate voltage with (black) and without (red) the hysteretic effect. The model is generated with the parameters shown in Table II. (Inset) The current density is calculated from  $\epsilon_f$  with (black) and without (red) the hysteretic effect.

## VI. LOW FREQUENCY MEASUREMENTS

The field effect hysteresis in GFETs often depends on the rate at which  $\epsilon_f^0$  changes. In this case, the Preisach kernel  $\mathcal{P}[\epsilon_f^0, \omega]$  includes a dependence of frequency  $\omega$ . Many hysteretic physical systems are not rate independent, and measurements performed as a function of sweep rate may be used to probe the underlying physics of hysteresis generation.

In order to assess the rate dependent properties of the observed hysteresis in graphene FETs, low frequency large signal measurements are performed. The gate bias is swept using a large signal (10 V peak to peak) sinusoid via a signal generator (Agilent 33 250 A). The time varying gate voltage  $v_g(t)$  and drain current  $i_d(t)$  are then monitored using an oscilloscope (Agilent MSO6034A). Hysteresis curves are generated by plotting the voltage waveform against the current waveform. The rate dependence of the hysteretic effect is

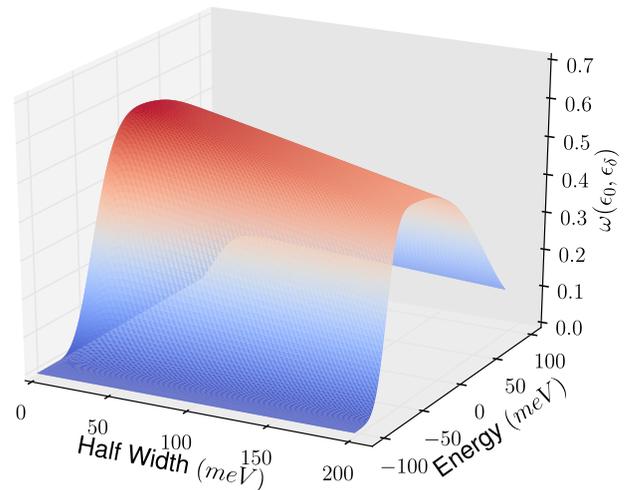


FIG. 7. A plot of the optimized density function  $\omega(\epsilon_0, \epsilon_\delta)$  for the  $[-6, 6]$  V DC hysteresis sweep shown in Figure 5.

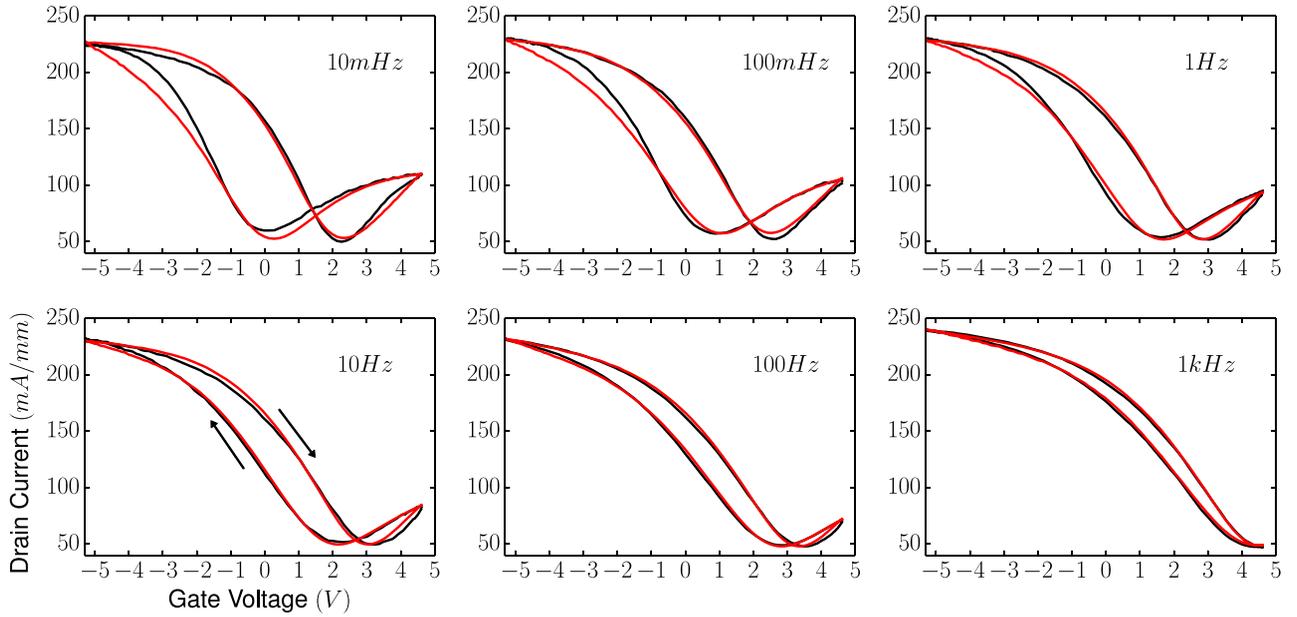


FIG. 8. Measured (black) and modeled (red) hysteresis curves. The plots show a weakly rate dependent hysteretic response of the drain current for an applied sinusoidal gate voltage with an amplitude of 5 V for several frequencies ranging from 10 mHz to 1 kHz. The calculated hole(electron) mobilities are 2548(1101)  $\text{cm}^2/\text{V s}$ . The applied drain bias is 250 mV for all sweeps.

observed by increasing the frequency of the applied gate voltage from 10 mHz to 1 kHz. In these experiments, a larger constant bias of 250 mV is applied to the drain in order to obtain acceptable resolution in the current waveform. All measurements are performed at 300 K. The large signal response of a second GFET is shown in Figure 8, and each hysteresis curve is modeled in a similar manner as was done for the DC measurements.

The parameters obtained from modeling of LF hysteresis curves measured on the second GFET are shown in Table III. The results from hysteresis modeling indicate graphene with a hole(electron) mobility of 2548(1100)  $\text{cm}^2/\text{Vs}$ . Upon comparison with the device shown in Table II, this GFET demonstrates a higher mobility, a reduced Fermi level pinning effect, and remarkable symmetry in  $D_{it}$ . The higher mobility device in Table III demonstrates a similar parasitic conductivity  $\sigma_r$  to the device modeled in Table II. This trend is observed in most devices. The maximum opening of the LF hysteresis curves  $\Delta_v$  is 1.69 V at 100 mHz, which is more severe than what is observed in the DC hysteresis measurements (0.93 V at 243 mHz for the  $\pm 5$  V sweep). Additionally, the hysteresis curves in both measurements are

TABLE III. The mean parameter values for the device model extracted for the low frequency large signal hysteresis curves shown in Figure 8. Values for  $D_{it}^p$  and  $D_{it}^n$  are given in  $10^{13}(\text{cm}^{-2})$ .  $v_D$  and the functional relay parameter  $\alpha$  are reported at 10 mHz/1 kHz.

$D_{it}^p$		$D_{it}^n$		Material		
$e_0^p$	-170 (meV)	$e_0^n$	170 (meV)	$\mu_p$	2548	( $\text{cm}^2/\text{V s}$ )
$\gamma_0^p$	158 (meV)	$\gamma_0^n$	89 (meV)	$\mu_n$	1101	( $\text{cm}^2/\text{V s}$ )
$\gamma_\delta^p$	17 (meV)	$\gamma_\delta^n$	10 (meV)	$\sigma_r$	0.172	( $\text{k } \Omega^{-1}$ )
$D_{it,0}^p$	1.73 ( $\text{cm}^{-2}$ )	$D_{it,0}^n$	1.45 ( $\text{cm}^{-2}$ )	$v_D$	0.49/4.10	(V)
$D_{it,\delta}^p$	2.68 ( $\text{cm}^{-2}$ )	$D_{it,\delta}^n$	1.95 ( $\text{cm}^{-2}$ )	$\alpha$	0.48/7.67	

morphologically identical, suggesting that the physical mechanism of hysteresis generation is the same in both devices. However, the variations in the DC and LF model parameters suggest that this effect is non-uniform.

LF hysteresis measurements reveal two rate dependent effects which are modeled by allowing all parameters to vary with frequency. First, the hysteresis is observed to slowly narrow with increasing frequency. Hysteresis modeling shows that the functional relay parameter  $\alpha(\omega)$  acquires a strong frequency dependence, while other model parameters vary only weakly with frequency. This gradual narrowing with increasing frequency assigns a time constant with large dispersion to the physical mechanism responsible for hysteresis generation. The maximum opening of the hysteresis  $\Delta_v$  decreases from 2.35 V at 10 mHz to 0.65 V at 1 kHz. Additionally, the device exhibits a drift in  $v_D$  towards positive bias with increasing frequency (approximately 0.5 V/decade) which is more severe than what is observed in the DC measurements. As in the DC case, this shift in  $v_D$  is attributed to the accumulation of fixed positive charge at the graphene/dielectric interface at low frequency.

This represents a major divergence from the case of electrolyte gated graphene flakes on  $\text{SiO}_2$  where very strong rate dependence is observed with top gating. In Ref. 4, hysteresis collapse leading to orientation reversal is observed with *decreasing* sweep rate from 62.5 mHz to 4.2 mHz. In Ref. 4, the hysteresis is attributed to competing charge transfer to and from the graphene layer which describes very slow time constants. In the case of the devices presented in this work, hysteresis narrowing occurs gradually over five orders of magnitude in frequency. This property of *weak rate dependence*, consistent orientation, and approximate symmetry in  $D_{it}$  suggests a different physical mechanism for hysteresis generation.

## VII. DISCUSSION

The hysteresis curves presented in this work are representative of what is observed in many graphene FETs. It is significant that the drain hysteresis appears in many GFET designs on various materials and substrates to varying degree. In order to generate a hysteretic Fermi energy, there must be a hysteretic charge density  $\sigma_{it}$  at the graphene/dielectric interface. The hysteresis in graphene FETs is commonly attributed to the accumulation of charge at the graphene/dielectric interface due to trap states. Other possible mechanisms include a leakage current induced hysteresis or a space-charge induced hysteresis. In Secs. VII A and VII B, these physical mechanisms behind the weakly rate dependent hysteresis are explored in the context of measurement data.

### A. Gate current measurements

Measurements of the gate leakage current  $i_g(v_g)$  are performed in order to assess whether the leakage current contributes to the hysteretic behavior observed in the  $i_d(v_g)$  curves.  $i_g(v_g)$  measurements are performed using a Keithley 4200 SCS parameter analyzer. In order to obtain high current resolution, a current preamplifier is used to measure  $i_g$ .  $i_d(v_g)$  hysteresis curves are simultaneously measured at  $v_d = 50$  mV. All curves are measured with and without microscope illumination (Figure 9). A strong dependence of the magnitude gate current is observed between illuminated and un-illuminated measurements, while the  $i_d(v_g)$  hysteresis curves show no such dependence.

The  $i_g(v_g)$  hysteresis curves indicate that the gate leakage in the device is a predominantly a photoinduced effect.<sup>38</sup> At negative bias, photons of energy  $\epsilon_\gamma = \hbar\omega$  generate hot electrons in the gate metal which are then injected into the conduction band of the dielectric due to the applied electric field. These electrons are either scattered into trap states in the dielectric or tunnel through the oxide. When positive bias is applied, the trapped carriers are released by the light. Additionally, the  $i_g(v_g)$  do not demonstrate closure indicating

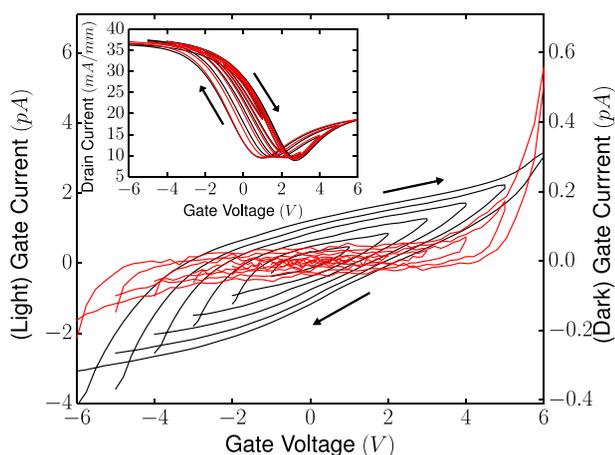


FIG. 9.  $i_g(v_g)$  hysteresis measurements for a GFET device with (black) and without (red) illumination. (Inset)  $i_d(v_g)$  hysteresis measurements taken for  $v_d = 50$  mV taken concurrently with the  $i_g(v_g)$  curves with (black) and without (red) illumination.

that negative charge has accumulated in the dielectric over the course of the sweep. In the absence of light, the  $i_g(v_g)$  hysteresis collapses and only a negligible leakage current  $\leq 1$  pA is observed. Most importantly, the  $i_g(v_g)$  measurements show that carrier injection from the gate metal into the oxide does not contribute to the properties of the  $i_d(v_g)$  hysteresis curves.

### B. Further observations

Gate current measurements indicate that  $\sigma_{it}$  likely originates at the graphene/dielectric interface. The sign of  $\sigma_{it}$  may be inferred by examining the orientation of the hysteresis. On sweeping  $v_g$  from positive bias to negative bias and back to positive bias, the  $i_d$  of the return sweep is to the right of the initial sweep thus describing a hysteresis of clockwise orientation. This implies that negative charge accumulates at the interface when sweeping toward negative bias. Similarly,  $\sigma_{it}$  is positive when the orientation of the sweep is reversed. It is significant that the sign of  $\sigma_{it}$  follows  $v_g$  as this is what is expected from space charge effects and opposite to what is expected when carriers from the graphene layer are trapped at interface states. Additionally, all of the measured hysteresis curves shown in Figures 5 and 8 all consist of multiple sweeps and demonstrate very consistent closure. It is significant that the hysteresis demonstrates closure upon completing each sweep. This reversibility property is closely related to weak rate dependence, and supports a space charge/polarization hypothesis. The Fermi level pinning is approximately symmetric about  $\epsilon_f = 0$  in both modeled devices indicating that  $\sigma_{it}(\epsilon_f) \approx -\sigma_{it}(-\epsilon_f)$  such that  $D_{it}(\epsilon_f) \approx D_{it}(-\epsilon_f)$ . This approximate symmetry in  $\sigma_{it}$  observed in the modeled devices further supports a polarization related effect as  $\sigma_{it}$  should be symmetric around  $v_D$ . Fermi level pinning then occurs symmetrically about  $v_D$  when  $\sigma_{it}$  becomes comparable to the charge due carriers in the channel.

The Lorentz- $\delta$  model implies that the hysteretic component of the polarization is due to some resonant process occurring at the graphene/dielectric interface or entirely within the dielectric. Although crystalline  $Al_2O_3$  is not ferroelectric, CV measurements of evaporated  $Al_2O_3$  films embedded with metal nanoparticles (nps) reveal a strong hysteresis of clockwise orientation, while complementary measurements on evaporated  $Al_2O_3$  films grown without metal-nps reveal no hysteresis.<sup>39</sup> Similar results have been observed in  $SiO_2$  films with embedded  $Si$ -nps.<sup>40</sup> A similar process may be responsible for the ferroelectric-like hysteresis observed in the GFET devices presented in this work. In this case,  $Al$ -nps may be introduced unintentionally at the graphene/dielectric interface via incomplete oxidation of the  $Al$  nucleation layer thus generating a space charge hysteresis similar to what is observed in Refs. 39 and 40. Furthermore, the  $Al_2O_3$  ALD layers grown on graphene are also highly amorphous such that they may also contribute to the hysteretic effect. Under this hypothesis, it is not surprising that the space charge effect generates a weakly rate dependent hysteresis described by a time constant of large dispersion. A validation of this hypothesis, as well as effects arising from trapping the graphene/substrate interface, requires further

investigation via low temperature CV measurements of  $Al_2O_3$  films grown on various types of graphene layers.

## VIII. CONCLUSION

The current hysteresis curves in GFETs with  $Al_2O_3$  gate insulator may be modeled by an weakly rate dependent Preisach kernel with functional relays. The properties of the hysteresis are examined, and the hysteresis is attributed to space charge generation in the dielectric layer which occurs during the polarization of the gate oxide. This assumption is supported by the consistent closure of the hysteresis for repeating sweeps of the gate voltage, weak rate dependence of the hysteretic effect up to 1 kHz, and approximate symmetry in  $D_{it}(\epsilon_f)$ .

## ACKNOWLEDGMENTS

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