

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Self-Switching Diodes for Zero-Bias Terahertz Detection

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Abstract

The self-switching diode (SSD) has been investigated as a potential terahertz detector in recent years. The SSD accomplishes a non-linear current-voltage relation through a field-effect, which enables detection at zero bias from microwave up to terahertz frequencies. In this work, SSDs were realised in two new materials; InAs and graphene. InGaAs SSDs were also fabricated. The effect of geometrical and material parameters on SSD detector performance under zero bias were for the first time described by an analytical model, and confirmed by experiment.

InAs SSDs were fabricated in an InAs/AlSb heterostructure. A noise equivalent power (NEP) of 150-200 pW/Hz^{1/2} was observed at 2-315 GHz with a 50 Ω source. InGaAs SSDs fabricated in an InGaAs/InAlAs heterostructure exhibited an NEP of 40-150 pW/Hz^{1/2} at 2-315 GHz with a 50 Ω source, the lowest NEP reported for any SSD in this frequency range. An InAs SSD integrated with a spiral antenna and silicon lens demonstrated an NEP of less than 4.4 nW/Hz^{1/2} at 600 GHz.

SSDs require a deep submicron isolation pattern which presents a major fabrication challenge in the InAs/AlSb heterostructure due to the oxidation sensitivity of the thick AlSb buffer layer. An SSD process was developed that allowed the fabrication of InAs/AlSb isolation patterns with feature sizes down to 35 nm.

Graphene SSDs were demonstrated for the first time. The SSD was based on epitaxial graphene on silicon carbide. A flat NEP of 2.4 nW/Hz^{1/2} was measured from 1 to 67 GHz using a 50 Ω source.

An analytical model of the SSD was derived to explain the influence of geometrical and material parameters. The model predicted that lowering the two-dimensional electron gas carrier concentration in the heterostructure increased the responsivity and reduced the NEP of the SSD zero-bias detector. Device simulations and measurements confirmed the predictions. Further, the model, together with experiments, showed that to minimize NEP there is an optimum number of channels and optimal channel length. The frequency dependence of SSD detectors was described using a small-signal equivalent circuit, which reproduced the measured responsivity up to 315 GHz. The highest cut-off frequency of InAs SSDs was estimated to 775 GHz.

Keywords: InAs, SSD, self-switching diode, graphene, InGaAs, zero-bias, detector, terahertz, noise-equivalent power.

List of publications

Appended papers

This thesis is based on the following papers.

- [A] **A. Westlund**, P.-Å. Nilsson, P. Sangaré, G. Ducournau, C. Gaquière, L. Desplanque, X. Wallart, and J. Grahn, “Nanochannel diodes based on InAs/Al₈₀Ga₂₀Sb heterostructures: Fabrication and zero-bias detector properties,” *Journal of Vacuum Science and Technology B*, vol. 33, p. 021207, 2015.

- [B] **A. Westlund**, P. Sangaré, G. Ducournau, P.-A. Nilsson, C. Gaquière, L. Desplanque, X. Wallart, and J. Grahn, “Terahertz detection in zero-bias InAs self-switching diodes at room temperature,” *Applied Physics Letters*, vol. 103, no. 13, p. 133504, Sep. 2013.

- [C] **A. Westlund**, P. Sangaré, G. Ducournau, I. Iñiguez-de-la-Torre, P.-Å. Nilsson, C. Gaquière, L. Desplanque, X. Wallart, J.-F. Millithaler, T. González, J. Mateos, and J. Grahn, “Optimization and Small-Signal Modeling of Zero-Bias InAs Self-Switching Diode Detectors,” *Solid State Electronics*, vol. 104, Feb. 2015.

- [D] **A. Westlund**, I. Iñiguez-de-la-Torre, P.-Å. Nilsson, T. González, J. Mateos, P. Sangaré, G. Ducournau, C. Gaquière, L. Desplanque, X. Wallart, and J. Grahn, “On the effect of δ -doping in self-switching diodes,” *Applied Physics Letters*, vol. 105, no. 9, p. 093505, Sep. 2014.

- [E] **A. Westlund**, M. Winters, I. G. Ivanov, J. U. Hassan, P.-Å. Nilsson, E. Janzén, N. Rorsman, and J. Grahn, “Graphene self-switching diodes as zero-bias microwave detectors,” *Applied Physics Letters*, vol. 106, p. 093116, 2015.

Other papers

The following papers are not appended to this thesis, either due to contents overlapping with the appended papers, or due to contents not related to this thesis.

- [a] **A. Westlund**, G. Moschetti, H. Zhao, P.-A. Nilsson, and J. Grahn, “Fabrication and DC characterization of InAs/AlSb self-switching diodes,” in *24th International Conference on Indium Phosphide and Related Materials*, Santa Barbara, CA, USA, 2012, pp. 65–68.
- [b] **A. Westlund**, G. Moschetti, P.-A. Nilsson, J. Grahn, L. Desplanque, and X. Wallart, “Cryogenic DC characterization of InAs/Al₈₀Ga₂₀Sb self-switching diodes,” in *25th International Conference on Indium Phosphide and Related Materials*, Kobe, Japan, 2013.
- [c] **A. Westlund**, G. Moschetti, H. Zhao, P.-Å. Nilsson, and J. Grahn, “InAs Self-Switching Diodes for THz Detection,” *GigaHertz Symposium*, Stockholm, Sweden, 2012.
- [d] **A. Westlund**, P.-Å. Nilsson, J. Grahn, “Fabrication and Characterization of InGaAs/InAlAs Slot diodes,” in *37th Workshop on Semiconductor Devices and Integrated Circuits held in Europe*, Catania, Italy, 2011.
- [e] **A. Westlund**, P.-A. Nilsson, P. Sangaré, G. Ducournau, C. Gaquière, and J. Grahn, “Zero-Bias Self-Switching In₆₅Ga₃₅As Channel Diodes for Terahertz Detection,” submitted to *26th International Conference on Indium Phosphide and Related Materials*, Santa Barbara, CA, USA, 2015.
- [f] G. Ducournau, **A. Westlund**, P. Sangaré, C. Gaquière, P.-Å. Nilsson, J. Mateos, and J. Grahn, “200 GHz communication system using unipolar InAs THz rectifiers,” in *38th International Conference on Infrared, Millimeter, And Terahertz Waves*, Tucson, AZ, USA, 2013.
- [g] L. Q. Zhang, Y. Alimi, C. Balocco, H. Zhao, **A. Westlund**, G. Moschetti, P.-A. Nilsson, J. Grahn, and A. M. Song, “Fabrication of novel unipolar nanodiodes in InAs/AlSb for microwave detection,” in *36th International Conference on Infrared, Millimeter, and Terahertz Waves*, 2011.

- [h] J. Mateos, J. F. Millithaler, I. Iniguez-de-la-Torre, A. Iniguez-de-la-Torre, B. G. Vasallo, S. Perez, T. Gonzalez, P. Sangare, G. Ducournau, C. Gaquiere, Y. Alimi, L. Zhang, A. Rezazadeh, A. M. Song, **A. Westlund**, and J. Grahn, “Room temperature THz detection and emission with semiconductor nanodevices,” in *Spanish Conference on Electron Devices*, 2013, pp. 215–218.
- [i] Ó. García-Pérez, J. Mateos, S. Pérez, **A. Westlund**, J. Grahn, T. González, “Experimental Analysis of Shot-Noise Suppression in InGaAs/InAlAs Recessed Planar Diodes at Room Temperature”, in *International Conference on Noise and Fluctuations (ICNF)*, Xi’an, China, 2015.
- [j] Ó. García-Pérez, J. Mateos, S. Pérez, **A. Westlund**, J. Grahn, T. González, “Shot-noise suppression effects in InGaAs planar diodes at room temperature”, in *19th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures*, Salamanca, Spain, 2015.
- [k] I. Íñiguez-de-la-Torre, A. Rodríguez, **A. Westlund**, Ó. García-Pérez, S. García, P-Å. Nilsson, J. Grahn, T. González, J. Mateos and S. Pérez, “Temperature and Surface Traps Influence on the THz Emission from InGaAs Diodes”, in *19th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures*, Salamanca, Spain, 2015.
- [l] I. Íñiguez-de-la-Torre, **A. Westlund**, J. Grahn, T. González and J. Mateos, “Zero-Bias THz Detection in InAs Nano-Diodes at Room Temperature”, in *19th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures*, Salamanca, Spain, 2015.
- [m] Y. Alimi, C. Balocco, L. Q. Zhang, H. Zhao, **A. Westlund**, G. Moschetti, and P. Nilsson, “Fabrication of Novel Unipolar Nanodiodes in InAs / AlSb Heterostructure,” in *UK Semiconductor*, 2011.

Theses

- [n] A. Westlund “Novel Terahertz Emitters and Detectors: InGaAs Slot Diodes and InAs Self-Switching Diodes” Thesis for the degree of Tekn. Lic., Chalmers University of Technology, 2012.

As part of the author’s doctoral studies, some of the work presented in this thesis has previously been published in [n]. Figures, tables and text from [n] may therefore be fully or partly reproduced in this thesis.

Abbreviations and notations

Abbreviations

2DEG	Two-dimensional electron gas
AlGaSb	Aluminium gallium antimonide
AlSb	Aluminium antimonide
BCB	Benzocyclobutene
CMOS	Complimentary metal-oxide semiconductor
CVD	Chemical vapour deposition
DC	Direct current
FET	Field-effect transistor
GaAs	Gallium arsenide
HEMT	High-electron-mobility-transistor
InAs	Indium arsenide
InGaAs	Indium gallium arsenide
MBE	Molecular beam epitaxy
MC	Monte Carlo
MOSFET	Metal-oxide semiconductor FET
NEP	Noise-equivalent power
PECVD	Physically enhances chemical vapour deposition
RF	Radio frequency
RFID	Radio frequency identification card
RIE	Reactive ion etch
SEM	Scanning electron microscopy
SSD	Self-switching diode

Notations

β_{opt}	Responsivity with optimal RF-match
$\beta_{50\Omega}$	Responsivity with 50 Ω source
NEP_{opt}	Noise-equivalent power with optimal RF-match
$NEP_{50\Omega}$	Noise-equivalent power with 50 Ω source

V_{th}	Threshold voltage
V_T	Thermal voltage
V_D	Drain voltage
I_D	Drain current
k	Boltzmann's constant
n	Gate ideality factor
R_0	Zero-bias resistance
L	Channel length
W	Channel width
W_v	Width of trench separating gate and channel
W_h	Width of trench separating gate and source
C_h	Gate capacitance
C_v	Capacitance between drain and source
C_p	Equivalent parasitic capacitance
S	Separation of channels
W_{mesa}	Mesa width
L_{mesa}	Contact separation
C_{pad}	Pad capacitance
L_{pad}	Pad inductance
R_{s1}	Parasitic series resistance
R_{s2}	Parasitic series resistance
T	Physical temperature
f_c	Cut-off frequency

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Chapter 1

Introduction

Detection in the terahertz (0.3 THz-3 THz) regime has been of importance to astronomy and spectroscopy for decades [1]. While space science has historically been the main driving force [2], there has been an increasing interest from new fields such as security [3] and data communication [4]. As a result, existing as well as new types of detectors operating at terahertz frequencies are constantly being developed for larger bandwidth and lower noise.

Low-noise detection in the terahertz regime is often accomplished with square-law-detectors such as the Schottky diode detector [5–7]. Zero-bias operation offers reduced $1/f$ noise [8]. Lately, metal-oxide-semiconductor field-effect transistors (MOSFETs) have been explored as a terahertz detector [9–11]. A less explored device with potential for zero-bias terahertz detection is the self-switching diode (SSD) [12]. The SSD generates a nonlinear current-voltage relationship (I-V) through a field effect. When the first SSD was presented, it was described as a field-effect transistor with nanometer sized channels and lateral gates connected to the drain, forming a two-terminal diode [12]. The non-linear I-V enables square-law detection, and SSDs using the two-dimensional electron gas (2DEG) of III-V heterostructures have been utilised for direct detection [13, 14]. Under cryogenic conditions, detection has been demonstrated up to 2.5 THz using InGaAs SSDs [13]. At room temperature, zero-bias direct detection has been demonstrated up to 1.5 THz with GaAs SSDs [14] and 0.3 THz with GaN SSDs [15].

Previous SSDs for terahertz detection were fabricated in GaN, InGaAs or GaAs heterostructures [14–16]. In this thesis, SSDs are realised in two new materials: InAs and graphene. InAs has a bulk electron mobility over three times larger than GaAs [17] which potentially means improved high-frequency performance. Monte Carlo (MC) simulations have predicted lower roll-off of responsivity in InAs SSDs than in InGaAs SSDs. InAs is preferably grown on an AlSb buffer, which is chemically unstable in air and water. In this work, a special InAs SSD process was developed that allowed deep submicron structures to be defined in the InAs/AlSb heterostructure for successful SSD detection experiments.

Graphene has recently received huge interest due to its high intrinsic mobility [18] and unique physical properties such as optical transparency [19]. The first realization and characterization of graphene SSDs is presented in this work [20, 21].

The first SSDs were fabricated in InGaAs/InAlAs heterostructures using wet etching [16, 22]. This thesis presents InGaAs SSDs where the channels are instead fabricated by a dry-etch process. In the first room-temperature terahertz measurements on InGaAs SSDs at 2-315 GHz, a new state-of-the-art noise equivalent power for SSDs was observed across the entire frequency range.

Prior to this thesis work, the influence of doping and design parameters on noise performance in SSD detectors had not been studied. In this thesis, a physics-based model for the SSD is derived by viewing the SSD as a MOSFET. The effects of doping and geometry are explained through the model, and studied in Monte Carlo simulations and detector experiments on SSDs.

This thesis is organised as follows. Chapter 2 presents the background to square-law detectors and SSD direct detectors including an overview of state-of-the-art detectors. In chapter 3, models for the SSD operating as MOSFETs in both the triode region and sub-threshold region are derived along with an equivalent small-signal circuit of the SSD. Implications of the model are discussed. In chapter 4, the fabrication processes for each material system is presented. Chapter 5 covers the DC and RF characterisation and comparison of SSDs in the three materials InGaAs, InAs and graphene. In chapter 6, the model's predictions of design dependence are evaluated with measurements and MC simulations. Finally, the thesis is summarised in chapter 7, and recommendations for the future development in the field of SSD zero-bias THz detection are given in chapter 8.

Chapter 2

Background

SSDs are in this thesis investigated as square-law detectors. A square-law detector produces a current or voltage proportional to the square of the amplitude of an applied oscillating voltage, that is, an absorbed radio-frequency (RF) power. Both heterodyne detectors and direct detectors employ square-law detectors, see Fig. 2.1. The heterodyne detector consists of a local oscillator and mixer that down-converts the radio-frequency (RF) signal, which is then detected by a square-law detector. In a direct detector, the RF signal is applied directly to the square-law detector. The heterodyne detector can provide high spectral resolution and phase information, however, is limited in bandwidth by both the mixer and square-law detector. The direct detector is only limited by the square-law detector. Direct detectors are therefore typically more broadband than heterodyne detectors.

This chapter covers the theory of direct detection with square-law detectors, previous work on SSDs as detectors, and the state-of-the-art for zero-bias terahertz detectors.

2.1 Theory of zero-bias detection

Any diode with a nonlinear I-V relationship may act as a square-law detector under small-signal conditions. On the following pages the figures-of-merits responsivity and noise-equivalent power are introduced, and the potential for low noise detection at zero bias explained.

2.1.1 Responsivity

The basis for direct detection is that a difference in incident RF power (ΔP_m) on the detector causes a corresponding shift in voltage across the device (ΔV), see Fig. 2.1 (a). The ratio

$$\beta = \Delta V / \Delta P_{in} \quad (2.1)$$

is called voltage responsivity, from here on referred to simply as ‘responsivity’.

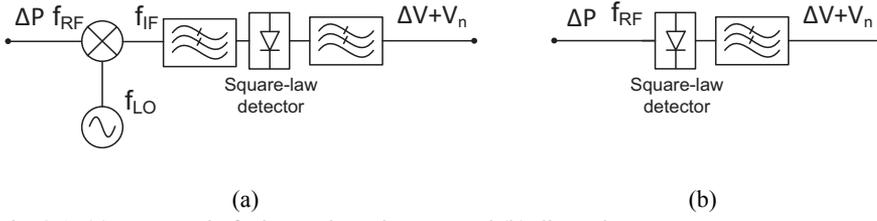


Fig. 2.1: (a) Front-end of a heterodyne detector and (b) direct detector.

The non-linearity of the I-V of a diode translates directly into a responsivity. If the ΔP_{in} is incident on the diode and the diode is optimally matched, the absorbed power is $\Delta P_{abs} = \Delta P_{in}$. In small-signal operation, the diode then generates a voltage

$$\Delta V = -\frac{1}{2} R_D \gamma \Delta P_{abs} \quad (2.2)$$

across the terminals [23], where R_D is the differential intrinsic resistance and

$$\gamma = \frac{d^2 I}{dV^2} / \frac{dI}{dV} \quad (2.3)$$

The quantity γ is referred to as ‘curvature’ or ‘curvature coefficient’ [24]. The responsivity with an optimum match is thus (ignoring the sign of ΔV)

$$\beta_{opt} = \frac{1}{2} R_D \gamma \quad (2.4)$$

When the detector is not matched and instead driven by a source with an RF impedance Z_s , the responsivity is found as

$$\beta_{Z_s} = \beta_{opt} (1 - |\Gamma|^2) \quad (2.5)$$

from the reflection coefficient $\Gamma = (Z_{diode} - Z_s) / (Z_{diode} + Z_s)$ where Z_{diode} is the impedance of the diode.

It follows from (2.2) that increasing R_D enhances β_{opt} . However, large R_D makes an impedance matching network narrowband and lossy, limiting the power transfer from source to detector. For $R_D \gg Z_s$, at low frequencies and with no matching network, (2.5) is reduced to

$$\beta_{Z_s} = 2Z_s \gamma \quad (2.6)$$

which notably is independent of R_D .

2.1.2 Noise-equivalent power

In addition to ΔV , a noise voltage V_n arises across the diode’s terminals. In general, several noise sources can be expected to contribute to V_n in a semiconductor diode.

Johnson-Nyquist noise appears across any conductor or semiconductor at thermal equilibrium due to thermal agitation of the carriers, and its root mean square voltage is [25]

$$V_{J-N} = \sqrt{4kTB R_D} \quad (2.7)$$

where k is Boltzmann's constant, T the physical temperature, and B the post-detection bandwidth [22].

Flicker noise is a group of known and unknown noise sources commonly observed in semiconductor devices. The flicker noise is represented by a noise voltage [26]

$$V_{1/f} = K_f V^x f^y \quad (2.8)$$

where K_f is a device-specific constant. Typically $x = 2$ and $y = -1$, explaining why flicker noise is often called "1/f noise". Flicker noise has been observed as both related to bulk phenomena such as mobility fluctuations [27] and interface phenomena [28].

Lastly, carriers crossing a potential barrier at random times generate a shot noise term [29]:

$$V_{shot} = 2qIB \quad (2.9)$$

where q is the elementary charge. Notably, shot noise is independent of temperature and device parameters. The total noise voltage is found as [8]

$$V_n^2 = V_{J-N}^2 + V_{1/f}^2 + V_{shot}^2 \quad (2.10)$$

In zero-bias detectors, both shot noise and flicker noise are greatly reduced compared to biased detectors, since $V = 0$ and $I = 0$ in the absence of incident power. During detection, ΔV will self-bias the diode and cause both flicker noise and shot noise, although the shot noise in practical conditions is much smaller and hence usually ignored [8, 23, 30]. A good first-order estimation of noise in zero-bias detectors is to consider the low-power limit, where ΔV is arbitrarily low and only Johnson-Nyquist noise is present [31, 32].

The noise equivalent power (NEP) is commonly defined as the ΔP_{abs} for which $\Delta V = V_n$ [23]. With an optimum lossless match, considering only Johnson-Nyquist noise, the NEP per $\text{Hz}^{1/2}$ post-detection bandwidth of a zero-bias detector is found as

$$NEP_{opt} = \sqrt{4kTR_0}/\beta_{opt} \quad (2.11)$$

where R_0 is the zero-bias resistance. When the diode is driven by a limited source impedance, the NEP is instead calculated as

$$NEP_{Z_s} = \sqrt{4kTR_0}/\beta_{Z_s} \quad (2.12)$$

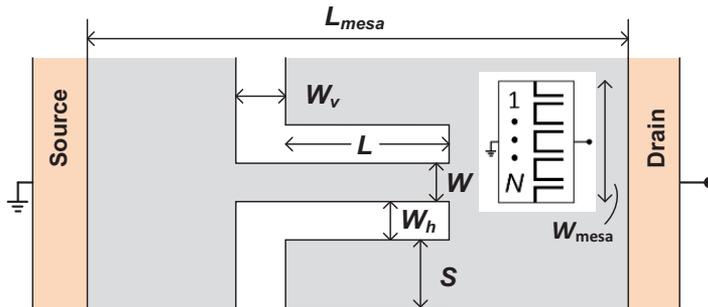


Fig. 2.2: Schematic layout of an SSD, viewed from the top, with geometrical definitions. Grey fields corresponds to semiconductor whereas white fields are isolating trenches etched in the heterostructure. Design parameters are channel width (W), trench widths (W_v , W_h), channel separation S , mesa width W_{mesa} and mesa length L_{mesa} . The thickness of the sheet is Z . An SSD consists of N channels in parallel as illustrated in the inset. [C]

2.2 Self-switching diodes

The first SSD was demonstrated in 2003 by Aimin Song et al. [12]. SSD is characterised by an etched pattern of conductive and isolating regions as illustrated in Fig. 2.2. The isolating trenches define nanometre-sized channels that connect the diode terminals denoted source and drain. In Song's paper, the device principle was explained as that of a field-effect transistor (FET), see Fig. 2.3 (a). The flanges between the channels act as gates, connected to the drain. The source is grounded. At zero-bias, a depletion region forms around the etched trenches, making the effective channel width, W_{eff} , smaller than W . For negative bias (Fig. 2.3 (b)), the gates act to deplete the channel, restricting current flow. Conversely, for a positive bias (Fig. 2.3 (c)), depletion is reduced, facilitating current flow. Thus, a non-linear I-V curve is created.

SSDs have been investigated in several applications. When first introduced, the SSD was presented as a rectifying diode [12]. With a slight variation of the trench design and by adding a terminal, a logic OR gate was constructed [12]. In device simulations, it has been demonstrated that the trench structure of the SSD can facilitate Gunn oscillations in the channel, making the SSD oscillate at frequencies beyond 100 GHz [33–35]. This phenomenon has however not yet been demonstrated in experiments. SSDs have also been employed in heterodyne detection [36]. However, the most investigated application of the SSD has been as a zero-bias direct detector of from microwave up to the terahertz regime [16].

The most notable direct detection result was reported for a zero-bias GaAs SSD in a quasi-optical configuration, where an NEP of 330 pW/Hz^{1/2} was reached at 1.5 THz [14]. A cryogenic InGaAs SSD was demonstrated at 2.5 THz [13]. GaN

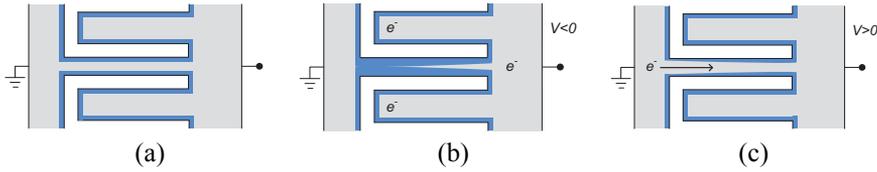


Fig. 2.3: Schematic top view of an SSD at thermal equilibrium. The SSD is formed by etching a trench (white areas) into a semiconductor (grey), in this example n-type. A depletion region forms next to etched areas (blue). (b) In reverse bias the channel is pinched. (c) In forward bias the channel is opened further.

SSDs were demonstrated with a zero-bias NEP_{opt} of 140-280 pW/Hz^{1/2} in the range 140-315 GHz [15].

The SSD layout permits numerous options in device design such as number of channels and geometrical dimensions in channel and trench. Notably, before this work, there has been no study, neither in experiments nor in simulations that reported on the relationship between the SSD design and NEP of the SSD detector.

2.3 Materials for SSDs

SSDs can be fabricated in any semiconductor material through a single etch. For example, silicon [37] and low-cost polymers [38], in transparent semiconductors such as indium-tin-oxide (ITO) [39] and ZnO [40]. However, SSDs in those materials have only been demonstrated up to 50 MHz [40].

SSDs for terahertz detection have used 2DEGs in III-V heterostructures based on compound semiconductors such as In(Ga)As, GaAs or GaN [14–16]. By separating electrons from donors, a 2DEG provides both high electron mobility and high sheet carrier concentration [41]. 2DEGs are frequently used in electronics, the most prominent example being high-electron mobility transistors (HEMTs) [42].

The material's influence on the responsivity of SSDs have been studied in Monte Carlo (MC) simulations [43, 44]. The MC simulation method solves the full Boltzmann's transport equation in the time domain, making it suitable for studying nanometre-sized devices [45]. MC simulated detection of SSDs with the same design but different materials is presented in Fig. 2.4. InAs SSDs operate at almost double the frequency of GaAs SSDs. The simulations are two-dimensional, meaning that the structure has a cross-section as in Fig. 2.2 while being infinitely thick. Therefore, parasitics such as capacitance through a substrate, which may affect SSD considerably, are not taken considered. Nevertheless, Fig. 2.4 indicates that under the same conditions, InAs SSDs operate at higher frequencies than GaAs SSDs and InGaAs SSDs.

In this thesis SSDs in InAs, InGaAs and graphene are studied. InGaAs has previously been employed in SSDs [16, 22]. In₆₅Ga₃₅As can be grown

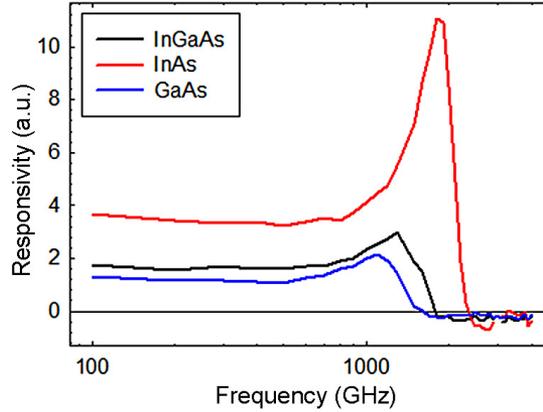


Fig. 2.4: Rectified current of SSDs as found through sinusoidal voltage excitation in Monte Carlo simulations. Simulations courtesy of Dr. Ignacio Iñiguez-de-la-Torre [91].

pseudomorphically on an InAlAs buffer and InP substrate, whereas InAs can be grown on an AlSb buffer. InAs has a drastically higher bulk mobility than $\text{In}_{65}\text{Ga}_{35}\text{As}$ ($33\,000\text{ cm}^2/\text{Vs}$ vs. $18\,000\text{ cm}^2/\text{Vs}$) making InAs more suited for high-frequency applications. $\text{In}_{65}\text{Ga}_{35}\text{As}$ channels are used in state-of-the-art low noise HEMTs (InP HEMTs) [46], whereas down-scaled InP HEMTs for high-frequency operation have increased indium content. Using thin ($\sim 3\text{ nm}$) InAs channels, HEMTs and monolithic microwave integrated circuits (MMICs) operating beyond 1 THz have been achieved [47]. The high mobility of InAs makes it attractive also for SSD.

Graphene has in the last years attracted huge interest in the scientific community due to its electronic properties. In exfoliated graphene, sheet carrier mobilities $>200\,000\text{ cm}^2/\text{Vs}$ have been observed under cryogenic conditions [18]. Graphene can be grown epitaxially over large surfaces on a SiC substrates [48]. By hydrogen intercalation, wafers of quasi-free-standing bilayer graphene are obtained. Further, graphene can be made at low cost [19] and is highly optically transparent [21].

Before this thesis work, no graphene SSD had been presented in the scientific literature. Two properties of graphene make it relevant for SSDs. Although graphene is a zero-bandgap material, graphene exhibits a maximum sheet resistance for a certain gate voltage, the Dirac voltage V_{Dirac} , when used as a transistor channel. Therefore a nonlinear I-V may be expected from SSDs in graphene.

The other aspect of graphene relevant to SSDs is the concept of nanoribbons. Narrow (20 nm) strips of graphene have been shown to exhibit a small (100 meV) band gap [49]. Since SSDs involve nanometre-sized channels, simulations on graphene SSDs have shown an enhanced rectification for width-induced band gaps, which could improve responsivity of graphene SSDs [50].

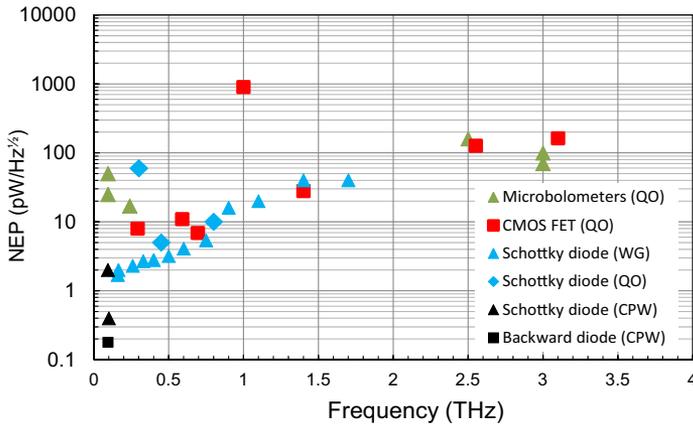


Fig. 2.5: State-of-the-art direct terahertz detectors at room-temperature. Shown are Schottky diodes mounted in a waveguide (WG) [53], in quasi-optical configuration (QO) [32, 92, 93], in on-wafer measurements (CPW) [6, 54], CMOS FET (QO) [11], microbolometers (QO) [94–98], and heterostructure backward diodes [24].

2.4 State-of-the-art direct terahertz detectors

An overview of NEP of state-of-the-art direct detectors at room temperature is provided in Fig. 2.5. The metal-semiconductor (Schottky diode) detector is more than a hundred years old [51, 52], and today provide state-of-the-art NEP up to and beyond 1 THz with zero-bias [32, 53], both in quasi-optical configurations and on-wafer [54]. Recent progress on Schottky diodes has been made using semimetal-semiconductor contacts, reaching an NEP of 0.4 pW/Hz^{1/2} at 100 GHz [54]. Zero-bias Schottky diodes have been integrated in metamorphic HEMT (mHEMT) monolithically microwave integrated circuits (MMIC) [6].

Heterostructure backward diodes produce larger curvatures than Schottky diodes, which resulted in an NEP of 0.18 pW/Hz^{1/2} measured at 94 GHz [24].

Microbolometers provide state-of-the-art at direct detection at frequencies beyond 2 THz by measuring the resistance of temperature-sensitive elements. Microbolometers have the drawback of requiring a bias and has a response time of milliseconds, slower than Schottky diodes [9].

In the last ten years, CMOS FETs (complimentary metal-oxide-semiconductor field-effect transistor) have emerged as promising detectors [55]. Although the FETs are biased with a gate voltage, they draw zero bias current, enabling low noise. An NEP close to Schottky diode has in the last years been demonstrated from a few hundred GHz to 4.3 THz, using moderate gate lengths of 150 nm [11, 56]. The high performance and easy integration with other CMOS technologies opens for low-cost terahertz detector arrays [57].

Chapter 3

SSD models for zero-bias detection

A model puts experimental observations into context and enables prediction of future experiment outcomes. An electrical model of an SSD is essential in the understanding of how and to what extent geometrical and material parameters affect key detector properties such as responsivity and NEP.

Prior to this work, no model for the SSD as detector had been presented. When the self-switching diode was first introduced, its function was conceptually explained through the analogy of an enhancement-mode FET [12]. Åberg et al. later modelled the I-V of silicon-based SSDs based on FET-equations, and their model is briefly reviewed here [58]. The Shockley diode equation has also been used to describe the I-V of SSDs, however without any connection to design or detector properties [22].

This chapter presents a physics-based model which predicts both responsivity and NEP of SSDs based on design and material parameters. The model, which was introduced in [C] and [D], is derived by applying the FET equations differently than Åberg et al. [12]. As a result, also the theoretical maximum responsivity of SSDs can be calculated. An equivalent circuit is introduced to describe the frequency dependence of SSD detectors. The model is evaluated in chapter 6.

In the first section of this chapter, the source of the nonlinear I-V curve is analysed by studying the intrinsic SSD channel, as done in [D]. Depending on bias conditions, the SSD is treated as an FET operating in either the triode region or sub-threshold region. The influence of design parameters on the I-V curve is derived.

In the second section, SSDs are studied as zero-bias detectors. The design and material dependence of detector properties such as responsivity and NEP is analysed. Parasitic elements are taken into account to describe the variation of responsivity over frequency [C].

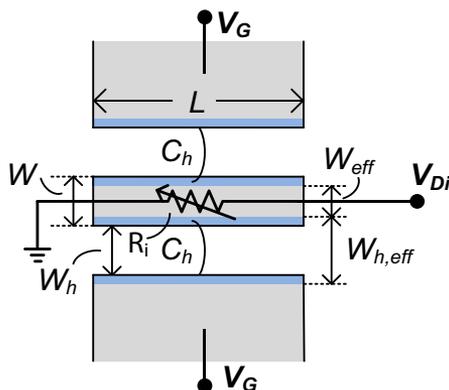


Fig. 3.1: Equivalent circuit in a top view of an SSD channel. The channel is separated from the gates by isolating trenches. Lateral depletion forms around trenches (blue). Fictional V_g terminals are introduced in the theoretical analysis of the SSD as a FET with lateral gates.

3.1 Intrinsic SSD models

A schematic design of a single intrinsic SSD channel is shown in Fig. 3.2. Fictional gate terminals with potential V_g are introduced in Fig. 3.2. The capacitance C_h is essential in creating a nonlinear I-V, by coupling the field from the gates to the channels, thereby regulating the intrinsic channel resistance R_i .

3.1.1 The SSD model by Åberg et al.

Åberg et. al made the first physical model of the I-V of SSDs [58]. Equations similar to the ones for MOSFETs are used to express the drain current in an SSD channel as

$$I_D = \begin{cases} -K(V_{Di} - V_{tn})^2, & \text{for } V_{Di} < V_{tn} \\ 0 & \text{for } V_{tn} < V_{Di} < V_{tp} \\ K(V_{Di} - V_{tp})^2, & \text{for } V_{Di} > V_{tp} \end{cases} \quad (3.1)$$

where $K = \mu_n C_h / L$, q is the elementary charge and μ_n the mobility of electrons in the channel. V_{tn} and V_{tp} are negative and positive threshold voltages. In for example forward bias, I_D is modelled as a FET in saturation mode when $V_{Di} > V_{tp}$, and vice versa for reverse bias. Below threshold though, the current is simply set to zero. This model is therefore not applicable for SSDs for zero-bias detection.

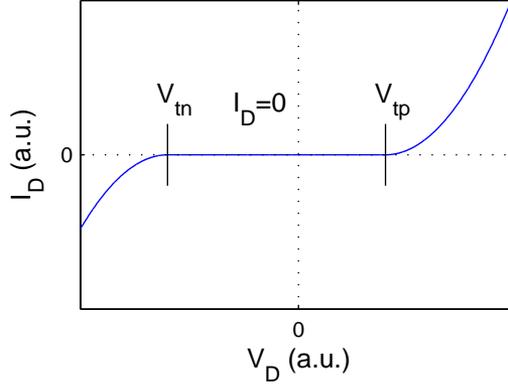


Fig. 3.2: Åberg et al.'s model for the I-V of an SSD. The current is modelled as zero between the positive and negative threshold voltages V_{tp} and V_{tn} which makes the model inapplicable for zero-bias detectors.

3.1.2 Triode-region SSD model

When the channel is under strong inversion, such as a 2DEG at equilibrium, the SSD can be expected to behave as a depletion mode MOSFET. Applying a voltage to V_g modulates the channel resistance R_i . Assuming that the channel is operating in the triode region, I_D is found as [59]

$$I_D = NK \left[\left(\frac{qn_s W_{eff}}{2C_h Z} + V_G \right) V_{Di} - \frac{V_{Di}^2}{2} \right] \quad (3.2)$$

where n_s is the sheet electron concentration in the channel. W_{eff} is an effective channel width, here introduced to take into consideration that depletion layers may form at the channel sidewalls. W_{eff} is related to W as

$$W_{eff} = W - W_o$$

where W_o is a constant [15]. Consequently, $W_{h,eff} = W_h + W_o$, see Fig. 3.1.

From (3.2), a threshold voltage may be identified as

$$V_{th} = -\frac{qn_s W_{eff}}{2C_h} \quad (3.3)$$

The conditions to be fulfilled for (3.2) to hold may now be expressed as (a) the transistor is operating in the triode region ($V_g - V_{th} \gg V_{ds}$ and $V_g \gg V_{th}$), (b) μ_n is field-independent ($V_{Di} \approx 0$ V), and (c) that the long-channel approximation is valid. For the special case of zero-bias operation ($V_{Di} \approx 0$ V), the condition (a) may be expressed as $V_{th} \ll 0$ V.

By recognizing that $V_g = V_{Di}$, (3.2) can now be rewritten as

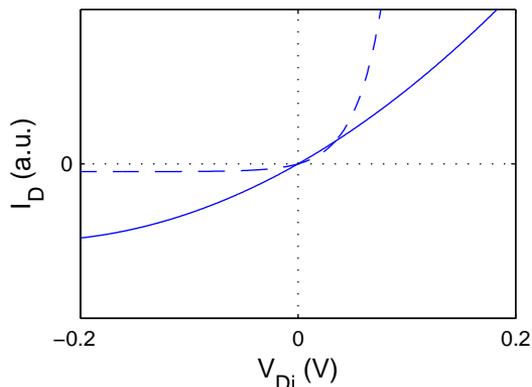


Fig. 3.3: I-V curves as predicted by (solid line) the triode-region SSD model and (dashed line) the subthreshold SSD model. Parameters used are $V_{th} = -0.25$ V for the triode region model and $V_{th} = 0$ V for the subthreshold model.

$$I_D = NK \left(\frac{V_{Di}}{2} - V_{th} \right) V_{Di} \quad (3.4)$$

An example of an I-V produced by (3.4) is plotted in Fig. 3.3.

3.1.3 Sub-threshold SSD model

For $V_{th} \gg V_{Di}$, and long-channel conditions, the transistor is operating in the sub-threshold region, meaning the channel is either in weak inversion or depleted. For the drain current of a MOSFET in subthreshold operation is [60]

$$I_D = \frac{N}{L} I_0 \exp\left(\frac{V_g - V_{th}}{nV_T}\right) \left(1 - \exp\left(-\frac{V_{Di}}{V_T}\right)\right) \quad (3.5)$$

which for $V_g = V_{Di}$ and for simplicity the gate ideality constant $n = 1$ simplifies to

$$I_D = \frac{N}{L} I_0 \exp\left(-\frac{V_{th}}{V_T}\right) \left(\exp\left(-\frac{V_{Di}}{V_T}\right) - 1\right) \quad (3.6)$$

where I_0 is a process-dependent constant and V_T the thermal voltage $V_T = kT/q$.

The triode-region FET model is compared to the sub-threshold FET model in Fig. 3.3. The former exhibits a quadratic I-V whereas the latter an exponential I-V. Both models display nonlinear I-V curves around $V_{Di} \approx 0$ V, which enables zero-bias detection with SSDs.

3.2 The SSD as a zero-bias detector

3.2.1 Responsivity and NEP

The non-linearity of the I-V of an SSD translates directly into a responsivity for a detector application. By applying the general theory of square-law detectors in section 2.1 on the triode-region FET model (3.4), the zero-bias responsivity and NEP can be expressed in terms of design parameters.

The intrinsic channel resistance R_i and the intrinsic curvature γ_i are found simply as

$$R_i = \left(\frac{dI_D}{dV_{Di}} \right)^{-1} = \frac{1}{NK(V_{Di} - V_{th})} = \{V_{Di} = 0\} = \frac{L}{qn_s W_{eff} \mu_n N} \quad (3.7)$$

and

$$\gamma_i = \frac{d^2 I_D / dV_{Di}^2}{dI_D / dV_{Di}} = \frac{1}{(V_{Di} - V_{th})} = \{V_{Di} = 0\} = \frac{2C_h}{qn_s W_{eff}} \quad (3.8)$$

These two quantities R_i and γ_i form the basis of the following analysis. Inserting (3.7)-(3.8) into (2.4)-(2.6) and (2.11)-(2.12), the following relationships are obtained:

$$\beta_{opt} = C_h \frac{L}{\mu_n N} \frac{1}{(qn_s W_{eff})^2} \quad (3.9)$$

$$\beta_{Zs} = Z_s C_h \frac{4}{qn_s W_{eff}} \quad (3.10)$$

$$NEP_{opt} = \frac{1}{C_h} \sqrt{4kT} \sqrt{\frac{\mu_n N}{L}} (qn_s W_{eff})^{3/2} \quad (3.11)$$

$$NEP_{Zs} = \frac{1}{2C_h Z_s} \sqrt{kT} \sqrt{\frac{L}{\mu_n N}} \sqrt{qn_s W_{eff}} \quad (3.12)$$

In equations (3.9)-(3.12) it is assumed that detection is performed at low frequencies and that no parasitic elements are at play. In the next section, the responsivity and NEP of a realistic SSD at high frequencies are studied.

3.2.2 Equivalent circuit of an SSD

The frequency dependence of an SSD is found by calculating the power coupled into the intrinsic channel (P_{Ri}) in relation to the total absorbed power (P_{abs}). The expression for β_{opt} in (2.4) is modified to

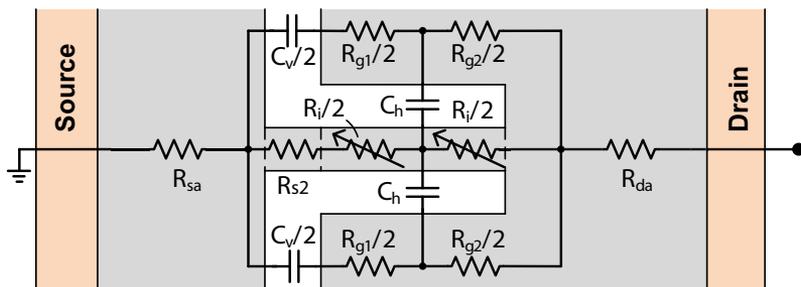


Fig. 3.4: Elements of the small-signal model as defined in a single-channel SSD. [C]

$$\beta_{opt} = \frac{1}{2} R_i \gamma_i F \quad (3.13)$$

where $F = P_{Ri}/P_{abs}$.

A number of parasitic elements degrade the SSD's responsivity and NEP. In Fig. 3.4, elements of an equivalent small-signal model are defined in an SSD with a single channel. The capacitance C_v appears across the trench drawn vertically in Fig. 3.4. C_v is the main parasitic element. A fair assumption is that C_v is roughly proportional to the W_{mesa} , which is roughly proportional to N , the number of channels.

To find the frequency response of SSDs, a simplified version of the small-signal model is used, as shown in Fig. 3.5. For the designs in this work, the designs in this thesis, R_{g1} and R_{g2} may be neglected since $W \ll S$ and thus $R_{g1} + R_{g2} \ll R_i$. In Fig. 3.4, the capacitances C_v and C_h are represented by a single capacitance C_h in parallel to R_i and R_{g2} . (A more accurate model would consider C_v and C_h separately.) By representing all capacitances in the SSD with C_p , F is slightly underestimated at high frequencies but the parameter extraction process simplified.

The zero-bias resistance R_0 is related to the other resistances in Fig. 3.3-3 as

$$R_0 = R_i + R_{sa} + R_{da} + R_{s2} \quad (3.14)$$

Empirical measurements of sheet resistance R_{sh} can be used to calculate R_i and R_{s2} . At zero-bias, the small-signal value of R_i is found as

$$R_i = \frac{R_{sh}L}{NW_{eff}} \quad (3.15)$$

R_{s2} represents the part of the channels that cross the vertical trench and is modelled as

$$R_{s2} = \frac{R_{sh}W_v}{NW_{eff}} \quad (3.16)$$

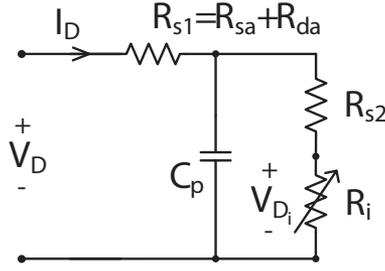


Fig. 3.5: Simplified small-signal circuit of an SSD.

The parasitic source-side and drain-side access resistances R_{sa} and R_{da} , respectively, represent the mesa resistance on the two sides of the channel. $R_{s1} = R_{sa} + R_{da}$ may vary with W somewhat due to current crowding at the entry of the channels. R_{s1} and R_{s2} are here considered linear.

The coupling factor F in (3.13) can now be calculated as

$$F = \frac{R_i}{R_i + R_{s1} + R_{s2}} \cdot \frac{1}{1 + \frac{R_{s1}(R_i + R_{s2})^2 C_p^2 \omega^2}{R_i + R_{s1} + R_{s2}}} \quad (3.17)$$

which at low frequencies is reduced to $F = R_i / (R_i + R_{s1} + R_{s2})$.

A detector's frequency dependence is often described by a "cut-off frequency" f_c . The definition of f_c is the frequency for which the power delivered to R_i is halved when the SSD is driven by a constant voltage source [61]:

$$f_c = \frac{1}{2\pi R_{s1} C_p} \left(1 + \frac{R_{s1}}{R_i + R_{s2}} \right) \quad (3.18)$$

Often, (3.18) is written simply as $f_c = 1 / (2\pi R_{s1} C_p)$, assuming $R_{s1} \ll (R_i + R_{s2})$. f_c is commonly applied to Schottky diodes and other diodes that can be described with an R-C network [6, 62].

3.2.3 Implications from model on SSD design

Certain conclusions regarding optimisations of SSDs can be drawn from the triode-region SSD model derived above. Analyzing the influence of device design on detector properties is simplified by studying the low-frequency performance as described by (3.7)-(3.12), with negligible parasitics.

In general it can be noted that increasing γ_i has only positive effects on NEP or responsivity. Increasing R_i improves β_{opt} and $NEP_{opt} (\propto \sqrt{R_i})$, however, affects NEP_{Zs} negatively and complicates an input match network. It follows from (3.7) and (3.8)

that C_h is the only parameter that increases γ_i without increasing R_i . C_h can be increased for example by minimizing W_h .

Next are two parameters that affect R_i and γ_i equally: W_{eff} and n_s . By reducing W and the channel doping, responsivity and NEP improve both with optimal matching and with a limited source impedance.

Three parameters affect only R_i and not γ_i : L , N and μ_n . The ratio $L/(N\mu_n)$ should be maximised to increase R_i and thus minimise NEP_{opt} . High R_i does however have negative effects on NEP_{Zs} through increased thermal noise. Further, N strongly affects the minimum mesa width and thus C_p , pad capacitance and the high-frequency response. Through careful examination of (3.7)-(2.12) it follows that μ_n should in fact be maximised and L minimised (without voiding the long-channel condition). The choice of N is then a trade-off between NEP_{opt} , $NEP_{50\Omega}$, responsivity and high-frequency performance, as discussed in chapter 6.

An interesting observation is that in sub-threshold operation, β_{opt} and $\beta_{50\Omega}$ are inversely proportional to T , while independent of T in the triode region. n_s , the only material parameter that affects responsivity in the triode region, is very weakly affected by T in III-V 2DEGs [63, 64].

When $V_{th} \rightarrow 0$ V, (3.8) suggests γ_i grows infinitely. But (3.8) was derived for an SSD channel operating in the triode region. For $V_t \approx 0$ V and $V_t \ll 0$ V, the SSD channel is instead operating in weak inversion and the sub-threshold model is more applicable. It follows from (3.6) and (2.3) that for $V_{th} < 0$ V, γ_i takes on a maximum value

$$\gamma_{i,max} = \frac{q}{kT} = \{T = 300 \text{ K}\} = 38.7 \text{ V}^{-1} \quad (3.19)$$

which translates to a maximum responsivity of 3870 V/W when driven by a 50 Ω source. The same $\gamma_{i,max}$ is observed in ideal Schottky diodes [59]. Thus, the maximum zero-bias curvature in an SSD is identical to the maximum curvature of a Schottky diode.

3.3 Summary

A model for the I-V of the intrinsic SSD channels was derived by considering the SSD an FET operating in either the triode region or sub-threshold region. Responsivity and NEP were expressed in terms of SSD design parameters. Trench width, channel width and carrier concentration were identified as the most important design parameters to optimise performance. Electron mobility was found to not affect responsivity, only NEP. Channels should be just long enough to exhibit long-channel behaviour. With the sub-threshold SSD model, it was shown that the theoretical maximum unmatched responsivity for an SSD equals that of the Schottky diode.

Chapter 4

Self-switching diode fabrication

SSDs are formed through a single etch of nanometre-sized into a single sheet of semiconductor. It was shown in chapter 3 that the lowest NEP is expected from SSDs with narrow channels defined by narrow etched trenches, meaning that an optimised fabrication process is essential for improving detector performance.

This chapter presents the fabrication processes for SSDs using the three different channel materials investigated in this thesis: InAs [A-D], InGaAs [e] and graphene [E]. InAs SSDs were fabricated in an InAs/Al₈₀Ga₂₀Sb heterostructure for InAs' high mobility. InGaAs SSDs were fabricated in an In₆₅Ga₃₅As/InAlAs heterostructure using a dry-etch process for comparison with previously demonstrated InGaAs SSDs based on wet-etched channels [14]. Graphene SSDs were fabricated in epitaxial graphene on SiC, which can be grown on wafer-scale [65]. A physical characterisation of SSDs fabricated in all three materials is presented.

4.1 InAs SSDs

InAs SSDs are expected to show less roll-off than InGaAs SSDs. However, InAs is grown pseudomorphically on AlSb which is tremendously sensitive to oxidation, and therefore presents a substantial technological obstacle in device fabrication [66]. InAs SSDs had been presented, but never in a process with stable devices [g,m]. The problem of instability is here addressed both through design of the epitaxial layers and through preventative measures in the device fabrication process. This process was developed for producing the deep submicron isolation patterns needed for InAs SSDs, while protecting the device from oxidation [A].

4.1.1 Epitaxial engineering

The design of the epitaxial structure is the first step for successful fabrication of InAs SSDs. By introducing a fraction of gallium into AlSb and forming the ternary

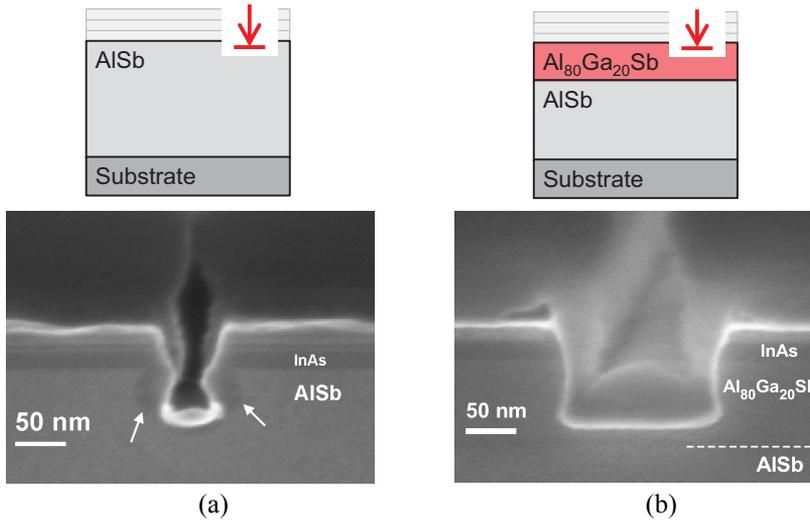


Fig. 4.1: Two candidate buffer designs for the InAs SSD process: (a) A pure AlSb buffer showing significant oxidation and (b) a buffer with 100 nm $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ just below the InAs channel, which was used in the final fabrication. In the final process, the coverage of the silicon nitride was much improved, see section 4.1.2.

compound $\text{Al}_x\text{Ga}_{1-x}\text{Sb}$, the chemical stability is improved considerably also for moderate Ga contents [67]. Although Ga is known to be more conductive than AlSb, a mixed AlSb/ $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ buffer is commonly used in InAs/AlSb devices such as HEMTs [67, 68]. However, a transistor biased for amplification has per definition much higher current per device width than a zero-biased InAs SSD. The leakage is thus more significant in an InAs SSD. The buffer design in InAs SSDs is a trade-off between chemical stability and electrical isolation [67].

Two investigated buffer designs are shown in Fig. 4.1 together with scanning electron microscopy (SEM) images of trenches passivated with silicon nitride. The cross-sections in Fig. 4.1 were prepared by fabricating long trenches and subsequently breaking the substrate perpendicularly to the trenches. None of the samples were subject to wet chemistry, and both were cut and imaged within minutes following the etch and subsequent passivation. The etched AlSb layer in Fig. 4.2 (a) shows a clearly oxidised area around the trenches. The $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ in Fig. 4.2 (b) exhibits considerably less oxidation. Hence, even though the parallel conduction may be increased by replacing AlSb with $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$, it is motivated by the dramatic increase in stability.

An early InAs SSD showed that an isolation resistance $>100 \text{ M}\Omega/\text{sq}$ across a $0.1 \times 30 \mu\text{m}$ isolating trench would produce a leakage current on the same level as single SSD channel at zero-bias [a]. The design in Fig. 4.1 (b) yielded an isolation

Table I: Epitaxial structure of InAs SSDs. Samples with and without δ -doping were studied.

Layer	Material	Thickness
Cap layer	InAs, Te: $1 \times 10^{19} \text{ cm}^{-3}$	5 nm
Protection layer	$\text{In}_{50}\text{Al}_{50}\text{As}$	4 nm
Barrier	$\text{Al}_{80}\text{Ga}_{20}\text{Sb}$	8 nm
δ -doping	Te: $0\text{-}1 \times 10^{12} \text{ cm}^{-2}$	
Spacer	$\text{Al}_{80}\text{Ga}_{20}\text{Sb}$	5 nm
Channel	InAs	15 nm
Buffer	$\text{Al}_{80}\text{Ga}_{20}\text{Sb}$	100 nm
Metamorphic buffer	AlSb	1000 nm
Smoothing layer	GaAs	300 nm
Substrate	S.I. GaAs (001)	500 μm

resistance of $>1 \text{ G}\Omega/\text{sq}$ across etched trenches, which was sufficient both in terms of isolation and stability.

The heterostructure used for fabrication of InAs SSDs in [A-D] is described in Table I. The structure was grown by molecular beam epitaxy (MBE) on a GaAs substrate. $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ was preferred over AlSb in three layers affected by the trench etch: The barrier, the spacer and the top part of the buffer. An $\text{In}_{50}\text{Al}_{50}\text{As}$ protection layer was placed on top of the $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ barrier. This layer allows the InAs cap layer to be etched away without exposing $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ to air.

4.1.2 Fabrication process

Trenches are in this process fabricated by dry etching. Ion implantation is an attractive alternative for AlSb materials since exposure of the buffer can be completely avoided [69, 70], and has been used for GaN/AlGaN SSDs [15]. However, ion implantation in InAs/AlSb structures causes transitions between isolating regions and unperturbed lattice over hundreds of nanometres, meaning limited resolution [71]. Since SSDs benefit from nanometre-sized trenches, and nanometre-sized channels, sharper transitions between conductive and isolating regions are needed. Ion implantation is therefore not suited for InAs/AlSb SSDs. Instead, a dry-etch process with *in situ* encapsulation with silicon nitride deposited with plasma-enhanced chemical vapour deposition (PECVD) was further developed [68].

It has been shown in elevated-temperature life-testing that $\text{Al}_{70}\text{Ga}_{30}\text{Sb}$ encapsulated with PECVD-grown silicon nitride does, in fact, oxidise after some time [72]. It is therefore relevant to grow a thick silicon nitride layer. The process in [68] uses lift-off of the deposited silicon nitride, which limits either thickness or

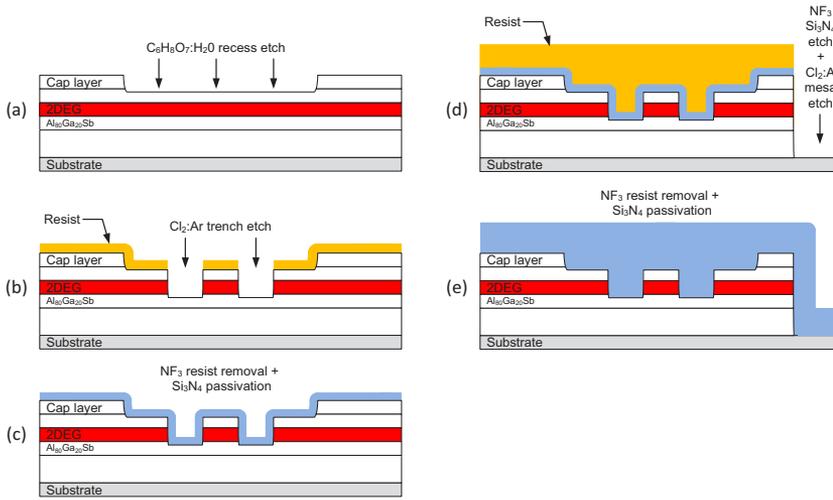


Fig. 4.2: Schematic view of the trench and mesa fabrication in InAs SSDs. (a) Recess in cap layer etched with citric acid, (b) dry etch of trenches, (c) in situ removal of resist and temporary silicon nitride encapsulation, (d) dry etch of mesas and (e) in situ removal of resist and temporary passivation and subsequent deposition of silicon nitride.

resolution. The process in [68] was in [A] further developed to include *in situ* resist removal, allowing silicon nitride of arbitrary thickness to be deposited as protection against oxidation. Since no lift-off is required, the improved process simultaneously allows nanometre-sized features and thick silicon nitride layers.

Fabrication of InAs SSDs starts with the formation of annealed Pd/Pt/Au ohmic contacts and Ti/Au metal pads. Then follows the formation of the active device and mesa isolation as described below and illustrated in Fig. 4.2.

- Recess etch:** A recess is etched in the cap layer using a citric acid solution. The purpose of the etch is to prevent parallel conduction through the cap layer in the SSD channels.
- Trench etch:** Trenches are patterned by e-beam lithography. Trenches are then formed through a time-controlled etch with a highly directional Cl₂:Ar reactive ion etch (RIE) process. The etch is stopped just below the InAs 2DEG, reaching the Al₈₀Ga₂₀Sb buffer. The resist is then removed in situ with an NF₃ RIE process, which does not etch III-V semiconductors [73].
- Early-passivation of trenches:** A 25 nm layer of silicon nitride is grown using through plasma enhanced chemical vapour deposition (PECVD) to temporarily encapsulate and electrically passivate the etched surfaces. Thus, the oxidation-prone Al₈₀Ga₂₀Sb and AlSb layers

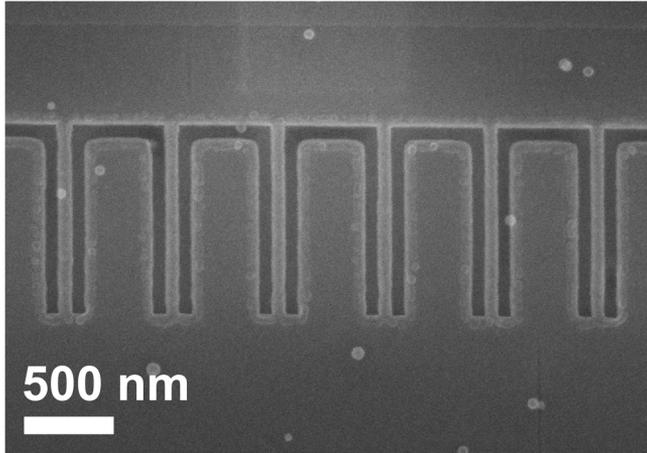


Fig. 4.3: A scanning electron micrograph (SEM) of an InAs SSDs with temporary encapsulation of 25 nm silicon nitride, corresponding to Fig. 4.2 (c). The imaged SSD channels were designed for $W=45$ nm.

are never exposed to air through the etch, resist removal, and passivation steps.

- d. **Mesa etch:** Mesas are patterned in resist, covering all active device areas and metal pads. The 25 nm silicon nitride layer is etched using the NF_3 RIE process in step b). The sample is etched down to the GaAs substrate with a Cl_2 :Ar RIE/ICP process. Using the aforementioned NF_3 RIE etch process, also the remaining resist and the 25 nm silicon nitride previously deposited to protect the etched trenches is removed.
- e. **Final passivation:** A new, 150 nm thick silicon nitride layer is grown. The silicon nitride completely fills the etched trenches and covered the mesa sidewalls.

A top-view SEM-image of an InAs SSD after step *c* is shown in Fig. 4.3. The trenches are clearly defined and uniformly etched, suggesting that the narrower trenches could be fabricated with the same process.

A cross-section of finalised SSD channels is shown in Figs. 4.4-5, imaged via scanning transmission electron microscopy (STEM). Fig. 4.5 shows how the silicon nitride completely fills the etched trenches. The trench etch reached through the InAs channel, thereby creating an isolating pattern. The channel was designed for $W=50$ nm, which corresponds to the width of the top of the physical InAs channel. Furthermore, Fig. 4.4 reveals that the physical InAs channel has a slightly trapezoidal cross-section with a 70 nm wide base. The $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ barrier on top of the InAs

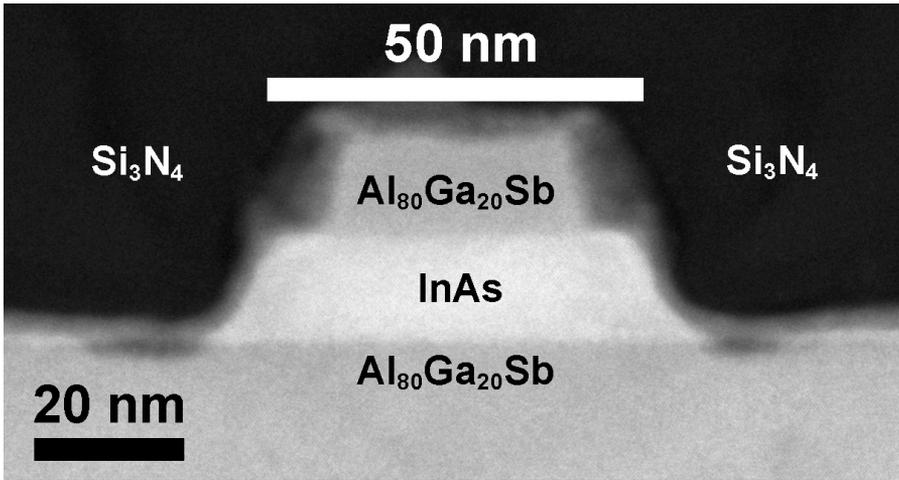


Fig. 4.4: STEM cross section of an SSD channel, cut along the [110] direction, with final passivation and encapsulation of silicon nitride corresponding to Fig. 4.2 (e). Isolation is achieved since the etch reaches through the InAs 2DEG. The imaged channel was designed for channel width $W=50$ nm.

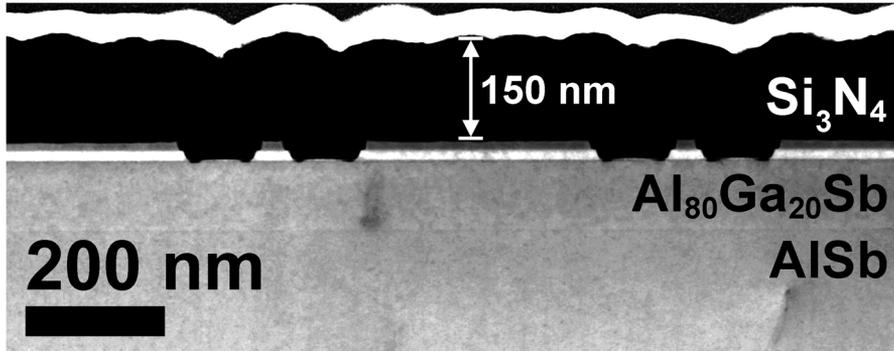


Fig. 4.5: An overview of two InAs SSD channels and the profile of the silicon nitride, imaged via STEM.

channel was somewhat overetched and 35 nm wide, 15 nm narrower than the rest of the channel.

A photo of an InAs SSD is available in Fig. 4.7 (a). A structure used for coplanar RF measurements is shown in Fig. 4.7 (b). Similar structures were used for SSDs in all three materials. An approximately 70 μm transmission line was used to provide a partial RF match.

W_{eff} in InAs SSDs was determined by plotting the zero-bias resistance R_0 and zero-bias conductance $1/R_0$ versus W , see Fig. 6. W_{eff} is the W for which the conductance reaches zero. A function of the form $R'_0 = a + b/(W - W_o)$ was fitted to

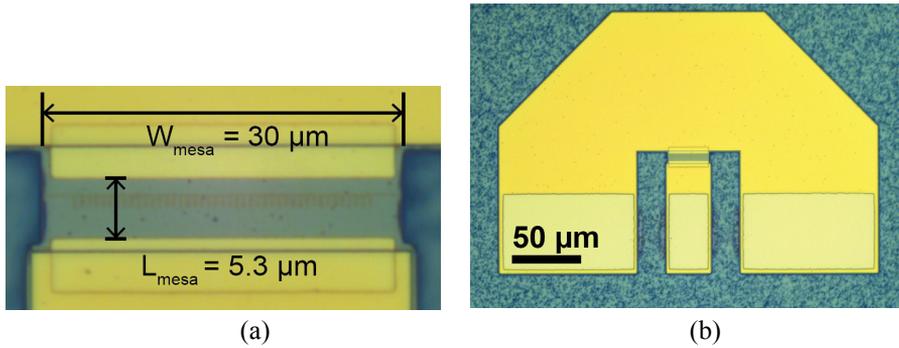


Fig. 4.7: (a) Micrograph of an InAs SSD. (b) Pad structure used in on-wafer RF measurements of InAs SSDs.

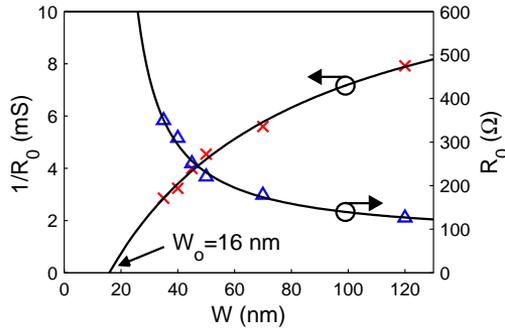


Fig. 4.6: Zero-bias resistance R_0 (triangles) and zero-bias conductance $1/R_0$ (crosses) versus W in InAs/AlSb SSDs. Extrapolation of R_0 and $1/R_0$ (solid lines) determined the effective channel width W_{eff} . [A]

R_0 , where a and b are constants. Extrapolating R_0' gives $W_o=16$ nm. Although the edges of the InAs channels in Fig. 4.4 are not perfectly sharp, the physical width is not significantly less than W , suggesting that W_o is to a large part due to depletion by surface charge.

InAs surfaces may exhibit either accumulation or depletion layers [23]. The type of layer and its magnitude can be affected by several factors such as passivation, etch chemistry and ion energy. A positive W_o indicates that with this process a depletion layer is formed at the channel sidewalls. Since the responsivity in SSDs at zero-bias is increased for narrow channel widths, an effective channel width smaller than the physical width is favourable for SSDs in detector applications.

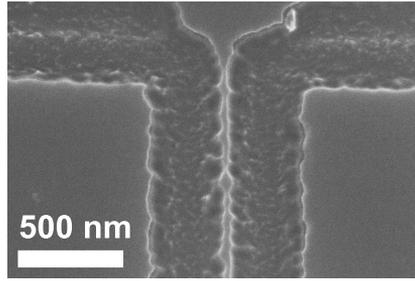


Fig. 4.8: Top-view of wet-etched InGaAs SSD channel. Sample courtesy of Prof A. Song [99].

4.2 InGaAs SSDs

The $\text{In}_{65}\text{Ga}_{35}\text{As}/\text{InAlAs}$ heterostructure is an established material system for SSDs [12, 16]. In contrast to InAs/AlSb , $\text{InGaAs}/\text{InAlAs}$ does not suffer from oxidation issues and SSDs can therefore be fabricated with well-known processing concepts. Wet-etched InGaAs SSDs, and GaAs SSDs, have been used in several experiments, also at terahertz frequencies [13, 16]. An example of a wet etched SSD channel is shown in Fig. 4.8. The roughness of the channel is of the same order as the channel width. In this thesis, however, InGaAs SSDs were fabricated by dry etching, for better control of channel width.

The MBE-grown pseudomorphic $\text{In}_{65}\text{Ga}_{53}\text{As}/\text{InAlAs}$ structure used for InGaAs SSDs in this thesis is shown in Table II. Identical structures are used for low-noise InP HEMTs [46]. After deposition of Ti/Pt/Au contacts and Ti/Au pads, the trenches and SSD channels were formed. Trenches were patterned with e-beam lithography and etched using the same RIE recipe as for InAs SSDs [A]. The InGaAs SSDs were taken out of the etch chamber, cleaned from resist with a solvent, and passivated with 25 nm silicon nitride using the same recipe as for InAs SSDs [A].

An example of a dry-etched InGaAs SSD channel is given in Fig. 4.9. Compared to the wet-etched channels in Fig. 4.8, the roughness is negligible and resolution greatly increased.

The channel in Fig. 4.9 was designed for $W = 100$ nm. The physical of the $\text{In}_{65}\text{Ga}_{53}\text{As}$ layer is 85 nm (top) and 100 nm (bottom). From Fig. 4.10, a $W_o = 29$ nm is extracted, indicating an effective width $W_{eff} = W - 29$ nm. The difference between physical width and W_{eff} is $\sim 15\text{-}30$ nm, suggesting that the depletion layer at the surface is the same as for InAs.

Table II: Epitaxial structure of InGaAs SSDs.

Layer	Material	Thickness
Cap layer	In ₅₃ Ga ₄₇ As, Si: $1 \times 10^{19} \text{ cm}^{-3}$	5 nm
Protection layer	In ₅₂ Al ₄₈ As	4 nm
Barrier	In ₅₂ Al ₄₈ As	8 nm
δ -doping	Si: $5 \times 10^{12} \text{ cm}^{-2}$	
Spacer	In ₅₂ Al ₄₈ As	5 nm
Channel	In ₆₅ Ga ₃₅ As	15 nm
Buffer	In ₅₂ Al ₄₈ As	500 nm
Substrate	S.I. InP (001)	400 μm

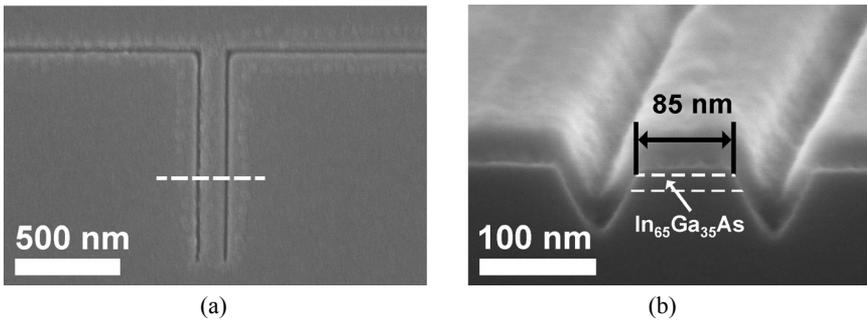


Fig. 4.9: (a) Top-view SEM of a dry-etched InGaAs SSD channel after passivation with 25 nm silicon nitride. (b) Cross-section SEM of an SSD channel designed for $W=100$ nm.

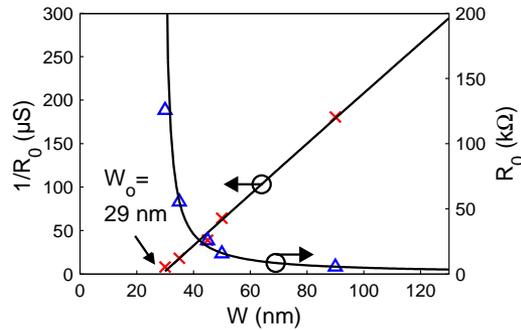


Fig. 4.10: Zero-bias resistance R_0 (triangles) and zero-bias conductance $1/R_0$ (crosses) versus W in InAs SSDs. Extrapolation of R_0 and $1/R_0$ (solid lines) determined the effective channel width W_{eff} .

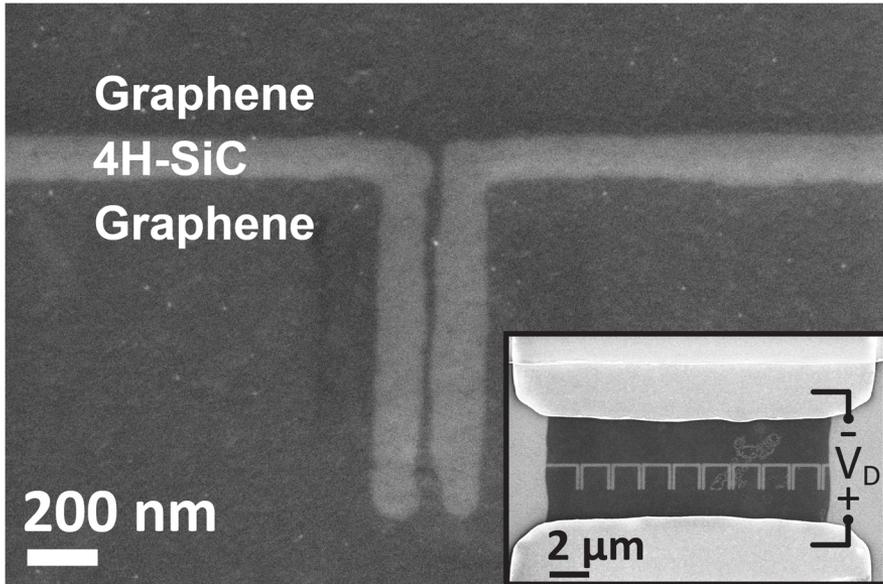


Fig. 4.11: Scanning electron micrograph (SEM) of a single SSD channel etched in as-grown bilayer graphene on SiC. The narrowest width of the depicted channel is 15 nm. The inset shows the SSD design used in the RF detection experiments, with 9 parallel channels.

4.3 Graphene SSDs

Graphene exhibits the highest mobility when produced through exfoliation of graphite, which yields small sample sizes [74]. With graphene grown epitaxially on SiC, wafer-scale graphene is obtained, which is more suited for production of electronic devices [48]. Graphene SSDs were therefore fabricated from epitaxial graphene on SiC.

The graphene was obtained as follows. A carbon buffer layer and a graphene monolayer were grown on the Si-face of 4H-SiC at 1400 °C in a horizontal hot-wall chemical vapour deposition (CVD) reactor [75]. One sample underwent hydrogen intercalation, in which the carbon buffer layer was released from the SiC. Hence, quasi-free standing bilayer graphene was obtained [48, 76, 77]. Micro-Raman spectra confirmed the expected number of graphene layers in both samples.

The processing began by patterning the isolating trenches with e-beam lithography [E]. A short (5 s) O_2 plasma was used to etch the graphene. Ohmic contacts (Ti/Au) were deposited and mesa defined using an O_2 plasma [78]. After depositing contact pads (Ti/Au) the SSDs were covered in benzocyclobutene (BCB) [78]. BCB was used to encapsulate and preserve the graphene.

Table III: Summary of transport parameters extracted from Hall measurements on samples that had undergone the developed SSD processes. For the InAs SSD and InGaAs SSD samples, the measurements were performed on etched and passivated areas. For graphene, the areas were coated with BCB.

Channel	δ -doping (cm^{-2})	R_{sh} (Ω/sq)	n_s ($\times 10^{12} \text{cm}^{-2}$)	μ_n (cm^2/Vs)
InAs	0	165	1.5	26 000
InAs	1×10^{12}	140	2.7	17 000
InGaAs	5×10^{12}	480	0.90	15 000
Graphene, as-grown	—	6500	0.69	1 400
Graphene, H-interc.	—	300	20^1	1 100

¹Hole concentration, p_s .

Fig. 4.11 shows a scanning electron micrograph of an SSD fabricated in epitaxial graphene. The inset shows an SSD design used for the RF detection experiment reported on in this thesis, with nine channels in parallel to reduce resistance and NEP.

4.4 Transport properties

The materials used for fabrication of SSDs will affect how the SSDs perform as detectors. Of special relevance is sheet electron mobility μ_n and sheet carrier concentration n_s . Hall measurements performed on samples prepared exactly as the surface of the etched SSD channels are presented in Table III. Due to the deep quantum well in InAs/AlSb structures, a significant n_s is reached even without δ -doping, which is expected [64]. The n_s reached in the InGaAs process is somewhat lower than what is reached with the same structure when silicon nitride is deposited at high temperature instead of room temperature [63].

While the as-grown sample was n-type, the H-intercalated sample was strongly p-type, thus exhibiting hole conduction [78]. From the n_s presented in Table III, the Fermi energies were estimated to $\varepsilon_f = 88$ meV for the as-grown sample and $\varepsilon_f = -366$ meV in the H-intercalated sample [79]. The change from n-type to p-type upon intercalation, and the observed mobilities, are expected from the literature [78].

4.5 Summary

An epitaxial structure and fabrication process was developed that enabled fabrication of the first InAs SSDs, on an AlSb buffer. Through *in situ* resist removal and encapsulation with silicon nitride, channels down to 35 nm wide were fabricated without exposure to air.

A process for dry etched InGaAs SSDs was presented with which dramatically narrower and smoother trenches and channels could be etched compared to wet

etched SSDs. The first graphene SSDs were fabricated through dry-etch of graphene grown epitaxially on SiC.

Samples that underwent all three processes exhibited transport properties expected from the literature.

Chapter 5

Characterisation of zero-bias SSD detectors

The fabricated SSDs have been characterised using DC measurements and RF measurements, performed on-wafer and in quasi-optical configuration [A-E, e]. On-wafer measurements provide more accurate measurements of device performance, whereas quasi-optical measurements at higher frequencies better emulate possible terahertz applications of SSDs.

In previous works, MC simulations had shown that SSDs with an InAs channel may show less roll-off of responsivity at high frequencies than SSDs in other III-V, see chapter 2. Detection with wet-etched GaAs SSDs had been demonstrated at 1.5 THz [14] and at 110 GHz with wet-etched InGaAs SSDs [16]. Graphene SSDs had been studied in simulations, however, never demonstrated in electrical measurements [80].

In this chapter, the first RF characterization of InAs SSD and dry-etched InGaAs SSDs are presented, with on-wafer measurements up to 315 GHz. The first graphene SSDs are characterized up to 67 GHz, on-wafer. Using quasi-optical measurements, detection is demonstrated at 200 GHz and 600 GHz with InAs SSDs. InAs SSDs are also employed in an imaging application at 200 GHz.

5.1 InAs SSDs

Throughout chapter 5 and 6, a reference InAs SSD design is used. Only deviations from this design are noted. Referring to Fig. 2.2, the reference design is $W = 45$ nm, $N = 43$, $L = 1000$ nm, $W_v = W_h = 100$ nm, $S = 350$ nm, $W_{\text{mesa}} = 30$ μm and $L_{\text{mesa}} = 5.3$ μm . The fabrication process was described in chapter 5, and used no δ -doping in the InAs/AlSb heterostructure unless otherwise stated.

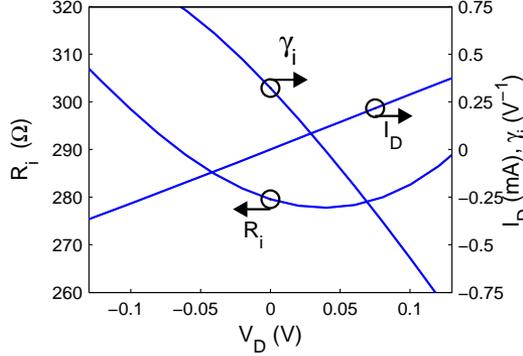


Fig. 5.1: Measured current (I_D), differential resistance (R_i), and curvature (γ_i) for an InAs SSD with $W = 35$ nm and $N = 43$ [C].

5.1.1 DC Characterisation

The basis for detection in the SSD is the nonlinear I-V characteristic of the intrinsic channel. To study the intrinsic channel, $V_{Di} = V_D - I_D(R_{s1} + R_{s2})$ was calculated, where R_{s1} was measured on a mesa without etched trenches to $R_{s1} = 40 \Omega$, and R_{s2} calculated through (3.14) using design parameters and R_0 . With V_{Di} , intrinsic channel resistance (R_i), and intrinsic curvature (γ_i) for an InAs SSD were plotted in Fig. 5.1, together with the drain current I_D . While the I-V appears almost linear in the graph, a nonlinearity is revealed through R_i and γ_i . Fig. 5.1 shows that R_i is slightly lower in forward bias than backward bias, thereby demonstrating rectifying behaviour of InAs SSDs. More precisely, the non-zero γ_i at $V_D = 0$ V enables detection at zero-bias.

The parameters relevant for zero-bias detection extracted from Fig. 5.1 are $R_i = 281 \Omega$ (12 k Ω per channel) and $\gamma_i = 0.32 \text{ V}^{-1}$, both for $V_D = 0$ V. From (2.3), the expected zero-bias responsivity with a 50Ω source is $\beta_{50\Omega} = 16 \text{ V/W}$.

5.1.2 RF Characterisation

On-wafer measurements of responsivity of InAs SSDs was performed using a vector network analyzer with frequency extenders as a signal source. Measurements were performed in three different bands (2-50 GHz, 140-220 GHz and 240-315 GHz), with an available power varying from $1.7 \mu\text{W}$ to $8.6 \mu\text{W}$. The measurement structure contained a short coplanar waveguide, see Fig. 4.7 (b), which provided a partial RF match. Further details are available in [B].

Measured responsivity of InAs SSDs ($\beta_{50\Omega}$) of two different W is presented in Fig. 5.2. $NEP_{50\Omega}$ was estimated from R_0 and $\beta_{50\Omega}$ using (2.12) and is shown in Fig. 5.3.

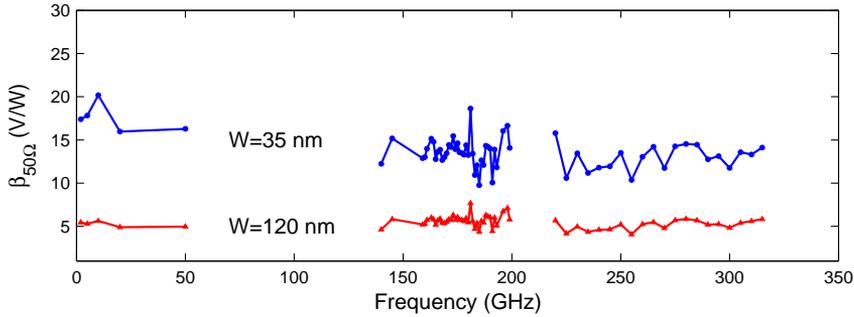


Fig. 5.2: Responsivity ($\beta_{50\Omega}$) of InAs SSDs measured on-wafer with a $50\ \Omega$ source [B].

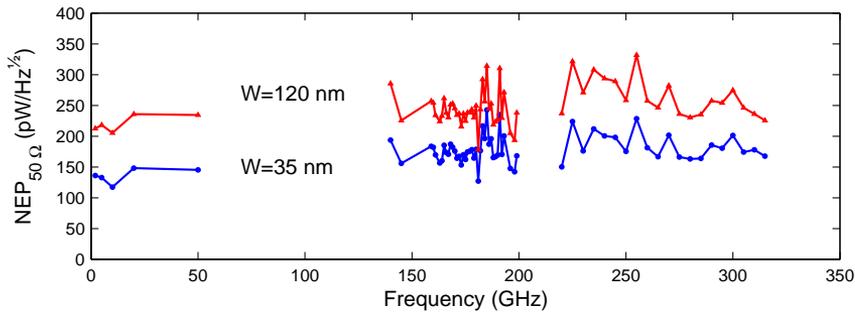


Fig. 5.3: Estimated $NEP_{50\Omega}$ of InAs SSDs when driven by a $50\ \Omega$ source. Calculated based on $\beta_{50\Omega}$ and R_0 ($350\ \Omega$ and $125\ \Omega$ for $W = 35\ \text{nm}$ and $W = 120\ \text{nm}$, respectively) and $T=300\ \text{K}$.

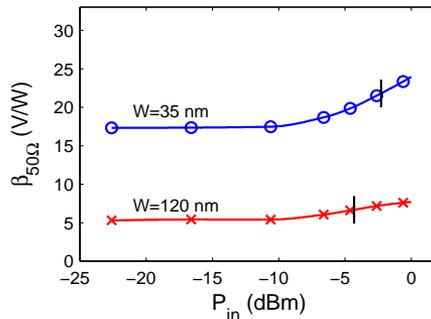


Fig. 5.4: Deviation of linear response in InAs SSDs at high available power P_{in} , measured on-wafer at $2\ \text{GHz}$. The vertical bars show where $\beta_{50\Omega}$ has expanded by $1\ \text{dB}$.

Notably, no strong roll-off of $\beta_{50\Omega}$ was observed up to $315\ \text{GHz}$. As predicted by (3.2)-(3.13), a smaller W and thus smaller W_{eff} resulted in higher $\beta_{50\Omega}$ and lower $NEP_{50\Omega}$. The $\beta_{50\Omega}$ for $W = 35\ \text{nm}$ at low frequencies was close to $16\ \text{V/W}$ as predicted from Fig. 5.1, demonstrating consistency between RF and DC measurements for the same SSD.

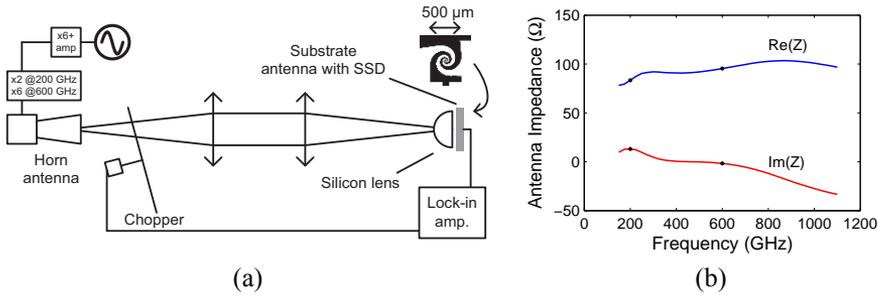


Fig. 5.5: (a) Setup used for quasi-optical measurements at 200 GHz and 600 GHz [B]. (b) Simulated antenna impedance.

At high incident powers, the SSDs deviate from a linear response. In Fig. 5.4, measured $\beta_{50\Omega}$ is plotted versus available power P_{in} at 2 GHz. The measured $\beta_{50\Omega}$ differs from the small-signal value by 1 dB at P_{in} of -2.3 dBm and -4.3 dBm for W of 35 nm and 50 nm, respectively. In comparison, the responsivity for Schottky diodes and Sb-based tunnel diodes reach 1 dB compression at < -20 dBm. The relatively weak nonlinearity (γ_i) of the I-V in InAs/AlSb SSDs explains why it remains linear at relatively high powers.

To investigate responsivity at higher frequencies, a quasi-optical measurement was performed at 200 GHz and 600 GHz using the setup in Fig. 5.5 [B]. A detector was constructed from an InAs SSD with an integrated, circularly polarised substrate antenna [81]. The InAs SSD was designed for $N = 11$ and $W = 65$ nm. I-V provided $R_0 = 580 \Omega$ and an expected $\beta_{opt} = 53$ V/W. A silicon lens was placed firmly against the backside of the substrate with the InAs SSD. Detected voltage was measured using a lock-in amplifier, thereby presenting a high DC-load. The transmitter radiated a vertically polarised beam through a horn antenna. The incident power was measured by replacing the receiver with an Erickson PM4 power meter with a horn antenna. At 200 GHz and 600 GHz the average power was 1.15 mW and 7 μ W, respectively. By using the power detected this way, the optical responsivity of the system was 2.1 V/W and 0.70 V/W at 200 GHz and 600 GHz, respectively. The associated NEP was 1500 pW/Hz $^{1/2}$ and 4400 pW/Hz $^{1/2}$. The quasi-optical measurements showed that InAs SSDs provide a responsivity at 600 GHz that is of the same order of magnitude as the responsivity at 200 GHz.

Compensating for optical losses from polarisation mismatch (50 %), and reflection at the air-Si interface (30 %), NEP of the InAs SSD with silicon lens is calculated to 500 pW/Hz $^{1/2}$ and 2.0 V/W at 200 and 600 GHz, respectively [82].

Wet-etched GaAs/AlGaAs SSD have demonstrated an NEP of 330 pW/Hz $^{1/2}$ at 1.5 THz in quasi-optical measurements, when the power absorbed by the antenna was estimated [14]. If the whole beam and no optical losses are taken into account,

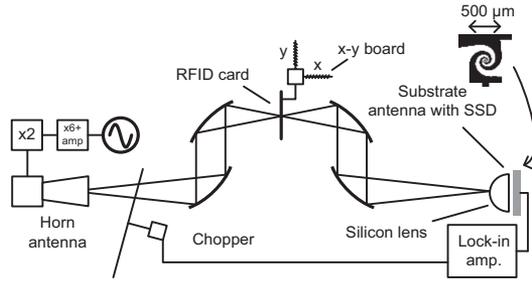


Fig. 5.6: Setup used for imaging at 200 GHz with an InAs SSD. Spherical mirrors focused the beam on the target and the detector.

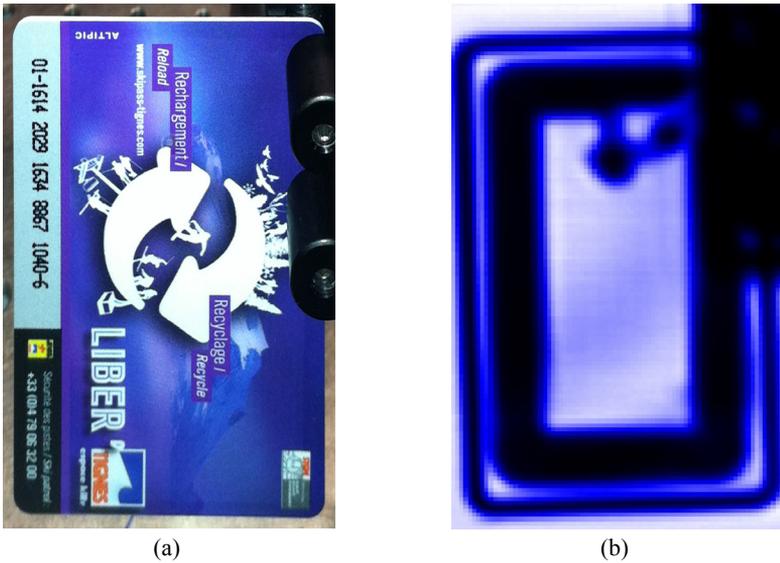


Fig. 5.7: (a) An RFID card and (b) its image at 200 GHz, measured using an InAs SSD.

equivalent to the procedure for the InAs SSD presented here, the NEP was instead $80000 \text{ pW/Hz}^{1/2}$ [83].

With the same detector used for quasi-optical detection ($N = 11$, $W = 65 \text{ nm}$), the setup in Fig. 34 was used to image a radio frequency identification (RFID) card. The imaging experiment was performed at 200 GHz with an output power of 1.15 mW. The beam was focused on the radio frequency identification (RFID) card shown in Fig. 35. The card was moved in a grid pattern and the output voltage ΔV in the SSD was recorded for every point. Plotting the signal strength versus position resulted in the image shown in Fig. 5.7. The plastics of the card is transparent to the radiation and thus imaged bright, while whereas metal antenna and microchip are reflective and appear dark.

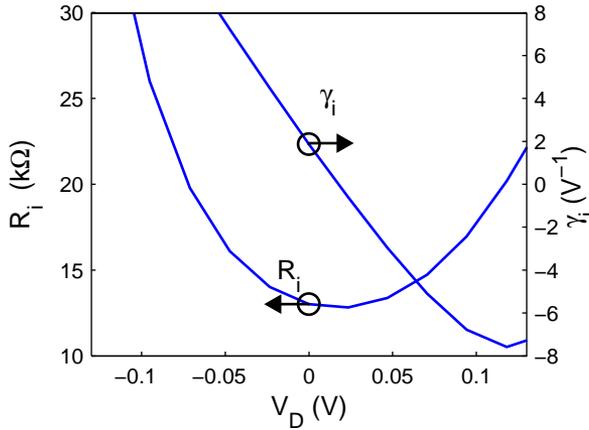


Fig. 5.8: Differential resistance (R_D), and curvature γ_i for an InAs SSD with $W = 50$ nm and $N = 5$. [e]

5.2 InGaAs SSDs

5.2.1 DC Characterisation

DC measurements of an InGaAs SSD are shown in Fig. 5.8. The design was $L = 1000$ nm, $S = 2000$ nm, $W_v = W_i = 50$ nm, $W_{\text{mesa}} = 15$ μm and $L_{\text{mesa}} = 5.3$ μm . R_{s1} , measured without etched trenches, was 200 Ω .

In Fig. 5.8, InGaAs SSDs exhibit DC characteristics qualitatively very similar to InAs SSDs, such as non-zero γ_i at zero bias and the asymmetry of R_i . The absolute values differ: For InGaAs, $R_i = 13$ $\text{k}\Omega$ (65 $\text{k}\Omega$ per channel) and $\gamma_i = 2.0$ V^{-1} at zero bias. From (2.3), $\beta_{50\Omega} = 200$ V/W is expected from the I-V of the InGaAs SSD in Fig. 5.8.

5.2.2 RF Characterisation

Responsivity of InGaAs SSDs was measured in the same way as for InAs SSDs [B]. Measured $\beta_{50\Omega}$ is presented in Fig. 5.9 and estimated $\text{NEP}_{50\Omega}$ in Fig. 5.10. The $\text{NEP}_{50\Omega}$ noted for InGaAs SSDs with $W=50$ nm, $40\text{-}150$ $\text{pW}/\text{Hz}^{1/2}$, is the lowest values reported for any SSD within the entire measured range. The stronger roll-off compared to InAs SSDs is expected from the higher R_{s1} .

The roll-off of $\beta_{50\Omega}$ in Fig. 5.9 is somewhat more pronounced than for InAs SSDs. For $W=50$ nm, the $\beta_{50\Omega}$ at low frequencies is about 300 V/W , corresponding to $\gamma_i = 3$ V^{-1} , which is considerably higher than the 200 V/W predicted from DC

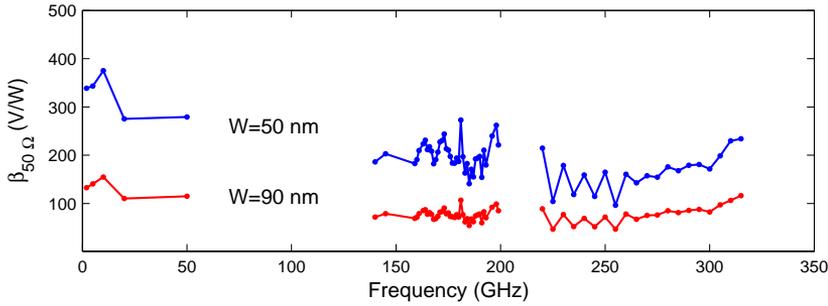


Fig. 5.9: Responsivity ($\beta_{50\Omega}$) of InGaAs SSDs when driven by a $50\ \Omega$ source.

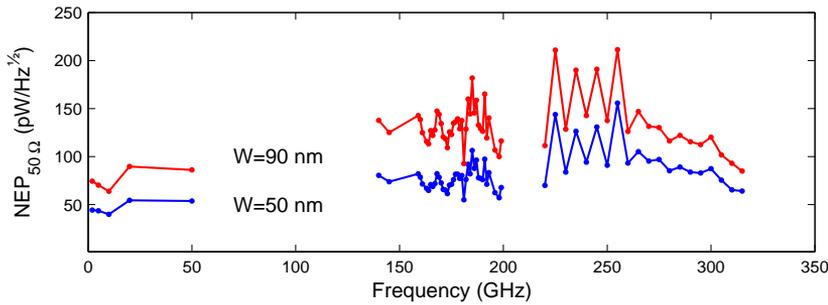


Fig. 5.10: Estimated $\text{NEP}_{50\Omega}$ of InGaAs SSDs when driven by a $50\ \Omega$ source. Calculations based on $\beta_{50\Omega}$ and R_0 ($14\ \text{k}\Omega$ and $6.1\ \text{k}\Omega$ for $W = 50\ \text{nm}$ and $W = 90\ \text{nm}$, respectively).

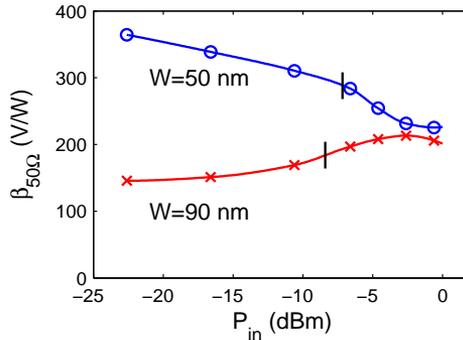


Fig. 5.11: Deviation of linear response in InGaAs SSDs at high available power P_{in} , on-wafer at 2 GHz. Verticals show where $\beta_{50\Omega}$ deviates by 1 dB from its value for the lowest P_{in} .

measurements in Fig. 5.10. The reason is this discrepancy is not understood, but could be due to self-heating in the channels in DC measurements.

The deviation from a linear response in InGaAs SSDs at high powers is shown in Fig. 5.11. The InGaAs SSDs reach 1 dB deviation at $-7.1\ \text{dBm}$ and $-8.4\ \text{dBm}$ for $W = 50\ \text{nm}$ and $W = 90\ \text{nm}$. Some compression and expansion of $\beta_{50\Omega}$ has already set

in for the lowest P_{in} and $W = 35$ nm, why the compression point for $W = 50$ nm is likely lower than what is extracted from Fig. 5.11. The deviation from a linear response sets in for lower powers in InGaAs SSDs than InAs SSDs, a consequence of the stronger nonlinearity of the I-V in InGaAs SSDs.

5.3 Graphene SSDs

5.3.1 DC Characterisation

Graphene SSDs were fabricated from both as-grown monolayer graphene, and H-intercalated graphene. This way, both n-type and p-type material was obtained, which from (2.3) is expected to lead to γ_i and thus $\beta_{50\Omega}$ of opposite signs. If $\beta_{50\Omega}$ of opposite signs is observed, it can be concluded that the SSDs operates as intended also in graphene.

DC measurements of SSDs fabricated from as-grown and H-intercalated graphene are shown in Fig. 5.12. The design was $N=9$, $W_v = W_h = 130$ nm and W varying from 15 to 40 nm, as shown in Fig. 4.11. For the as-grown sample, $\gamma = 0.024$ V⁻¹ and $R_\theta = 67$ k Ω was obtained at zero-bias. The expected $\beta_{50\Omega}$ was -2.4 V/W. For the H-intercalated sample, the corresponding figures were $\gamma = -0.022$ V⁻¹ and $R_\theta = 4.2$ k Ω , with an associated $\beta_{50\Omega}$ of 2.2 V/W. DC measurements thus show opposite signs of $\beta_{50\Omega}$ in the two different graphene SSD samples as expected.

In the graphene SSD process, a roughness of the etched channels was observed, see Fig. 4.11, leading to a degraded γ . A single-channel on the H-intercalated single demonstrated, $\gamma = -0.1$ V⁻¹ and $R_\theta = 9.2$ k Ω showing that higher responsivities are possible.

Graphene SSDs exhibit DC characteristics that both resemble and differ from InAs and InGaAs SSDs. The basic operation is the identical: Taking the n-type as-grown sample as an example, the lateral gates at forward bias act to increase electron density and reduce R_D , see Fig. 5.12 (a). At (weak) reverse bias, electron density is decreased and R_D increased. In the hydrogen-intercalated p-type sample (Fig. 5.12 (b)), holes are majority carriers and the operation reversed.

A difference between graphene SSDs, and InAs and InGaAs SSDs, is revealed in Fig. 5.12 (a). Again using the n-type as-grown sample as an example, R_D exhibits a local maxima when biased at the Dirac voltage $V_{Dirac} = -70$ mV, see Fig. 5.12 (a). As described in chapter 2.3, a maximum in R_D is indeed expected for a certain V_D which brings the Fermi level in the SSD channels to the Dirac point. For the as-grown sample, the Fermi level was estimated to 86 mV from Hall measurements, which corresponds well to the observed V_{Dirac} in both magnitude and polarity. For the

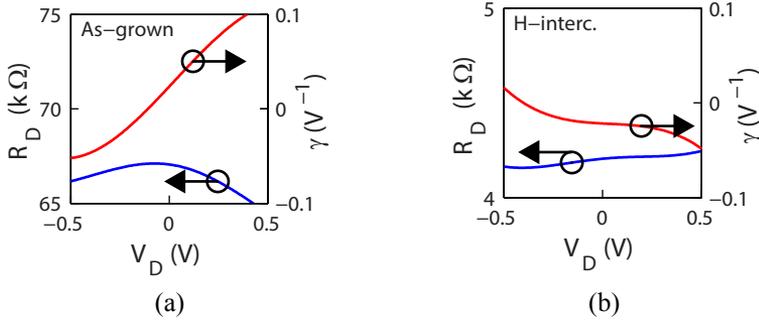


Fig. 5.12: Differential resistance (R_D), and curvature (γ) for SSDs with nine channels ($N=9$) fabricated on (a) as-grown monolayer and (b) hydrogen-intercalated bilayer graphene. [E]

hydrogen-intercalated sample, Fig. 5.12 (b) shows that V_{Dirac} is expected at a positive bias outside the measured range, in qualitative agreement with the Fermi level - 366 mV acquired from Hall data.

5.3.2 RF Characterisation

Responsivity of graphene SSDs at RF was measured on-wafer from 1 to 67 GHz. A 70 μm coplanar access line was used, similar to what was used for InAs SSDs. The available power at the probe tip was 3 μW to 24 μW across the measured band. The DC voltage generated by the SSD was measured with a voltmeter.

The measured responsivity is presented in Fig. 4. Both samples exhibited a flat responsivity from 1 to 67 GHz, with an average $\beta_{50\Omega}$ of 3.9 V/W and -4.2 V/W for the hydrogen-intercalated and as-grown samples, respectively. As expected from DC measurements, the two samples exhibited $\beta_{50\Omega}$ of similar magnitude but opposite polarity. The opposite polarity of the detected voltage between the as-grown (n-type) and H-intercalated (p-type) shows that the detection is due to the SSD structure and not due to other phenomena.

Estimated $NEP_{50\Omega}$ is shown in Fig. 5.13. The average $NEP_{50\Omega}$ was 2.2 $\text{nW}/\text{Hz}^{1/2}$ and 8.2 $\text{nW}/\text{Hz}^{1/2}$ for the H-intercalated and as-grown samples, respectively. While $\beta_{50\Omega}$ was similar in both devices, R_0 and therefore $NEP_{50\Omega}$ was considerably lower in the H-intercalated sample.

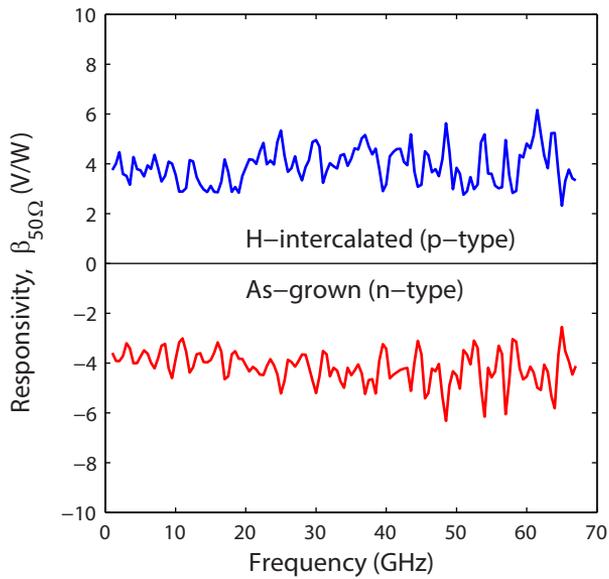


Fig. 5.13. Responsivity of SSDs fabricated in as-grown monolayer graphene and hydrogen-intercalated bilayer graphene. [E]

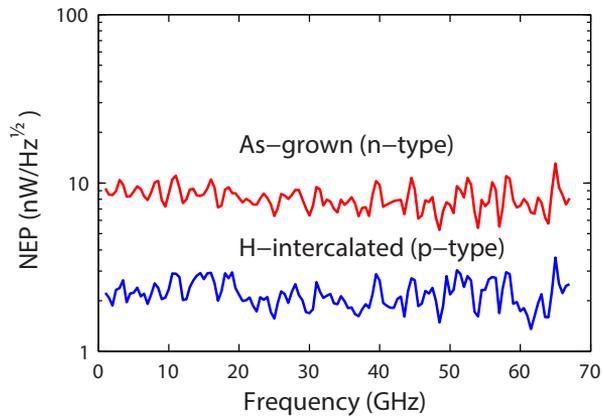


Fig. 5.14. Estimated NEP of SSDs in as-grown monolayer graphene and hydrogen-intercalated bilayer graphene. [E]

Table IV: Figures of merit from DC and on-wafer RF measurements of zero-bias SSDs presented in this thesis compared to previous works.

Ref.	Technology	γ_i (V ⁻¹)	R_i ($N=1$) (k Ω)	$NEP_{50\Omega}$ ($N=1$, 0 Hz) (pW/Hz ^{1/2})	RF meas. freq. (GHz)	$\beta_{50\Omega}$ (V/W)	$NEP_{50\Omega}$ (pW/Hz ^{1/2})
[e]	InGaAs/InAlAs	3.0 ¹	65	110	2-315	350-100	40-150
[A-D]	InAs/AlSb	0.32	12	440	2-315	17-13	150-200
[E]	Graphene (H-interc.)	0.022	37	11000	1-67	3.9	2200
[E]	Graphene (As-grown)	0.024	67	14000	1-67	4.2	8200
[E]	Graphene (H-interc.)	0.1	9	1200	-	-	-
[15]	GaN/AlGaIn	1 ¹	22	190	20-315	100-20	190-950
[22]	InGaAs/InAlAs	1.4	13600	3400	1-110 ²	160 ²	65 ²
[16]	InGaAs/InP	0.1 ¹	>11000	>42000	1-110	10-5	>10000
[14]	GaAs/AlGaAs	1.9	400	520	1500	-	-

¹ Estimated as $\gamma_i = \beta_{50\Omega}/2Z_s$, see (2.6).

² Low-frequency design (explicit data beyond 3 GHz not disclosed).

5.4 Comparison of SSD performance

DC and RF properties of SSDs presented in this thesis is compared to previous works in Table IV. The estimated $NEP_{50\Omega}$ of the InGaAs SSDs constitutes the state-of-the-art $NEP_{50\Omega}$ up to 315 GHz among SSDs from any other design and technology. InAs SSDs exhibit the second-lowest $NEP_{50\Omega}$ in the measured range. InAs SSDs also show the least roll-off of any SSD consistent with the MC simulations in Fig. 2.4.

For comparison, the traditional Schottky diode exhibits $R_0 \approx R_i = 2.6$ k Ω and $\gamma_i = 34$ V⁻¹, which through (2.6) and (2.12) yields a low-frequency $\beta_{50\Omega}$ of 3400 V/W and $NEP_{50\Omega} = 2$ pW/Hz^{1/2} [7].

The $NEP_{50\Omega}$ for the SSDs listed in Table IV is heavily affected by the N used in each design. While N is easily changed, γ_i and R_i per channel is limited by the SSD process and associated materials. The potential of each SSD process in Table IV may be compared by studying $NEP_{50\Omega}$ for $N=1$ at low frequencies. InGaAs SSDs show the lowest $NEP_{50\Omega}(N=1)$ of any SSD process, followed by the GaN/AlGaIn SSDs, both with dry-etched trenches.

The benefit of dry-etched trenches is revealed by comparing $NEP_{50\Omega}(N=1)$ of the InGaAs SSDs in this thesis to the wet-etched SSDs in [22], [16] and [14]. While γ_i may reach similar values, the resistance per channel in wet-etched SSDs is dramatically higher, likely due to non-uniform channels, and results in $NEP_{50\Omega}(N=1)$ more than ten times higher than dry-etched trenches.

The $NEP_{50\Omega}(N=1)$ of all technologies in Table IV can be improved upon: For example, in the H-intercalated graphene SSDs, W_h was relatively large (~ 200 nm). By reducing W_h and improving the uniformity of the channels, graphene SSDs could potentially surpass $NEP_{50\Omega}(N=1)$ of InAs SSDs. Regardless of fabrication process, a matching network would reduce the NEP of an SSD-based detector at the desired measurement frequencies.

5.5 Summary

Characterisation of InGaAs SSDs yielded state-of-the-art $NEP_{50\Omega}$ for SSDs. The first demonstration of both InAs SSDs and graphene SSDs as microwave detectors was presented.

InGaAs SSDs exhibited an NEP of 40-150 pW/Hz^{1/2} over the range 2-315 GHz with a 50 Ω source, which is the lowest NEP measured for any SSD in the range. InAs SSDs exhibited an NEP of 150-200 pW/Hz^{1/2} across the same band, with lower high-frequency roll-off than InGaAs SSDs. Graphene SSDs showed an NEP of 2200 pW/Hz^{1/2} from 1 to 67 GHz.

InAs SSDs were implemented in quasi-optical measurements, yielding an optical NEP of lower than 1500 pW/Hz^{1/2} and 4400 pW/Hz^{1/2} at 200 GHz and 600 GHz, respectively.

Chapter 6

Optimisation of SSDs for zero-bias detection

The design of an SSD strongly affects the SSD's detector properties at microwave frequencies and beyond. It has previously been reported in literature that narrower channels improved responsivity in matched SSD detectors [15]. In MC simulations, ways to increase responsivity have been studied [84, 44, 85, 43]. No other design dependencies than channel width has been studied experimentally, and more importantly, no investigations have reported on the SSD design dependence of NEP, the most important property of direct detectors.

In this chapter, the influence of doping, channel width, channel length, and number of channels on responsivity and NEP of SSDs is investigated. The models derived in chapter 3 are compared to DC and RF measurements on InAs SSDs, and MC simulations [C,D].

First, SSD channels are optimised based on the triode-region SSD model's predictions regarding doping, channel width and channel length. MC simulations are used to study InAs SSDs in ideal conditions and at doping levels that yield close to maximum theoretical responsivity.

Next, the channel length and number of channels in InAs SSDs are optimized, comparing measurements and models.

Lastly, the equivalent circuit of SSDs presented in Fig. 3.5 is used to model the responsivity of SSDs up to 315 GHz. Approaches for optimisation of SSDs for terahertz frequencies are discussed.

6.1 Doping and channel Width

It was shown in chapter 3 that according to the triode-region FET model, n_s and W have similar effects on the SSDs responsivity and NEP. In this section, the influence of n_s and W is studied first through the model's predictions, then through MC simulations, and lastly through DC and RF measurements.

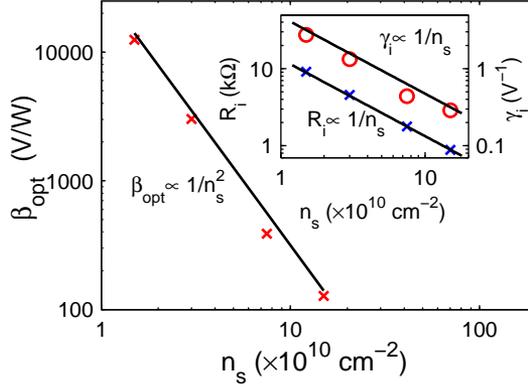


Fig. 6.1: Intrinsic β_{opt} obtained from 2-D Monte Carlo simulations (crosses) of an InAs SSD and the triode-region SSD model (solid line) as a function of n_s . The inset shows simulated R_i (crosses) and γ_i (circles), and modelled counterparts. [D]

Recalling from (3.7) and (3.8), the triode-region FET model says that at zero-bias,

$$R_i \propto \frac{1}{n_s W_{eff}} \quad (6.1)$$

and

$$\gamma_i \propto \frac{1}{n_s W_{eff}} \quad (6.2)$$

and thus, $\beta_{opt} = \frac{1}{2} R_i \gamma_i \propto 1/(n_s W_{eff})^2$. Reducing n_s and W_{eff} thus has the effect of increasing both R_i and, more importantly, γ_i .

A physical SSD is affected by processes variations and phenomena such as charges at the etched interfaces. MC simulations allow (6.1) and (6.2) to be evaluated under ideal conditions.

The MC simulations of InAs SSDs were set up in the following way. A single InAs SSD with a cross-section as shown in Fig. 3.4 was simulated in two dimensions, meaning all fields were in the horizontal plane. The channel was designed with $L = 900$ nm, $Z = 15$ nm, $W_v = W_h = 100$ nm, $W = 35$ nm and a carrier concentration N_D such that $N_D Z = n_s$, where $n_s = 1.5 \times 10^{10}$ cm $^{-2}$. W and n_s were then varied independently. Since no surface charge was placed on the channel sidewalls, meaning $W_{eff} = W$. The current was scaled by Z and $N = 43$ to obtain I_D . R_{s1} and R_{s2} were extracted from the simulation at low V_D and used to calculate $V_{Di} = V_D - I_D(R_{s1} + R_{s2})$. From the extracted I_D - V_{Di} -relationship, γ_i , R_i and intrinsic β_{opt} were calculated

according to (3.7)-(3.13). The MC simulation exhibited $\mu_n = 28000 \text{ cm}^2/\text{Vs}$ which

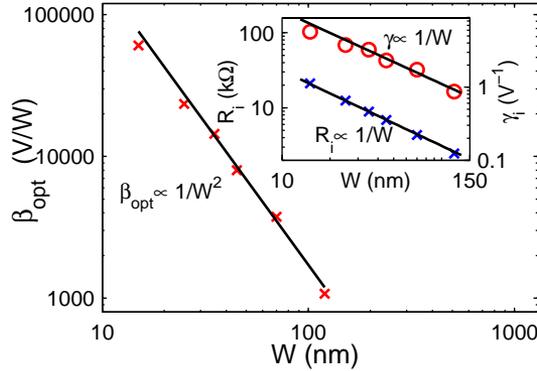


Fig. 6.2: Intrinsic β_{opt} obtained from 2-D Monte Carlo simulations (crosses) of an InAs SSD and the triode-region SSD model (solid line) as a function of n_s . The inset shows simulated R_i (crosses) and γ_i (circles), and modelled counterparts. [D]

was used for calculating the modelled values [86]. Since the MC simulations were two-dimensional C_h was found as $C_h = \epsilon_0 Z / W_h$, where ϵ_0 is the permittivity of vacuum. More details are available in [86].

The n_s - and W -dependence suggested by (6.1)-(6.2) is compared to MC simulations in Fig. 6.1. In the inset, the same comparison is made for R_i and γ_i . The model accurately predict the variation of both β_{opt} and its constituents R_i and γ_i . In Fig. 6.2, the W -dependence is compared in the same fashion, also with a good agreement between simulation and model. Thus, it can be concluded that the MC simulations confirm the triode region SSD model with respect to n_s and W .

To experimentally verify the influence of n_s and W_{eff} , InAs SSDs based on the reference design mentioned in section 5.1 were fabricated, with varying W and with and without δ -doping. Hall measurements are available in Table III.

Figures 6.3-6.5 compares RF and DC measurements of the InAs SSDs to the triode-region SSD model. Zero-bias β_{opt} , NEP_{opt} and $NEP_{50\Omega}$ were calculated using (2.4)-(2.5) and (2.11)-(2.12), based on $\beta_{50\Omega}$ and S_{11} measured on-wafer at 50 GHz and R_0 from DC measurements. γ_i was calculated from β_{opt} using (3.13). Modelled values were found through (3.7)-(3.17) based on parameters acquired predominantly from design and material properties: n_s and μ_n was acquired from Hall measurements. W_{eff} was defined as $W_{eff} = W - 16 \text{ nm}$ as found from Fig. 4.6, and consequently, $W_{h,eff} = W + 16 \text{ nm}$. $2C_h$ was found from a model of the capacitance to ground in a co-planar transmission line with the dimensions W_{eff} , $W_{h,eff}$, and L , and the relative dielectric constant of AlSb, $\epsilon_{AlSb} = 10.9$ [87, 88]. R_{s1} was measured on a structure without patterned trenches to 40Ω and 27Ω on the low- and high-doped samples, respectively. Thus, only two parameters were made based on measurements of the InAs SSDs: R_{s1} and W_{eff} .

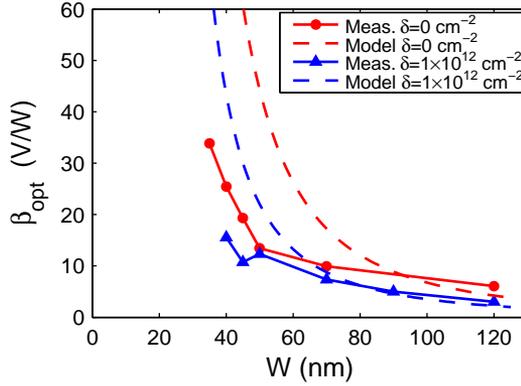


Fig. 6.3: Responsivity with an optimally matched source (β_{opt}) measured at 50 GHz on SSD from samples with and without doping, compared to modelled values. [C]

Measured β_{opt} for SSDs with different W on the two samples is compared to β_{opt} from the triode-region SSD model in Fig. 6.3. Measured β_{opt} is increased for small W . More importantly, the low-doped sample exhibits a significantly higher β_{opt} than the high-doped sample. For the smallest W available on both samples, $W = 40$ nm, the difference in measured β_{opt} is a factor 1.6x, compared to a factor 2x predicted by the model. Moreover the model overestimates the responsivity for small values of W . However, the relative dependencies of both W and n_s is described well by the model.

More information about the mechanics behind an increased β_{opt} is revealed by studying Fig. 6.4. SSDs on the two samples exhibit similar R_i . The model predicts $R_i \propto 1/(\mu n_s)$, and since the high-doped sample exhibited lower μ_n , see Table III, the sheet resistance was similar in both samples.

Although R_i was similar in both samples, the difference in γ_i is significant. This is expected since $\gamma_i \propto 1/n_s$, and independent of μ_n . From the measured n_s , γ_i is expected to be 1.8x larger in the high-doped sample than the low-doped sample. For $W = 40$ nm, the different in measured γ_i is 1.4x. The agreement is even better for $W = 120$ nm. The W -dependence of γ_i is exaggerated by the model, which led to β_{opt} being overestimated in Fig. 6.3. Qualitatively, the model is correct: From largest to smallest W , γ_i increased by 20 % in both samples.

The C_h obtained from [87] and used in the model is shown in Fig. 6.4 (b). C_h is reduced for small W , which somewhat counteracts the positive effects on responsivity of reducing W .

Finally, the effect of varying n_s and W on $NEP_{50\Omega}$ and NEP_{opt} is studied in Fig. 6.5. Measurements show that designs with smaller W effectively reduce both $NEP_{50\Omega}$ and NEP_{opt} .

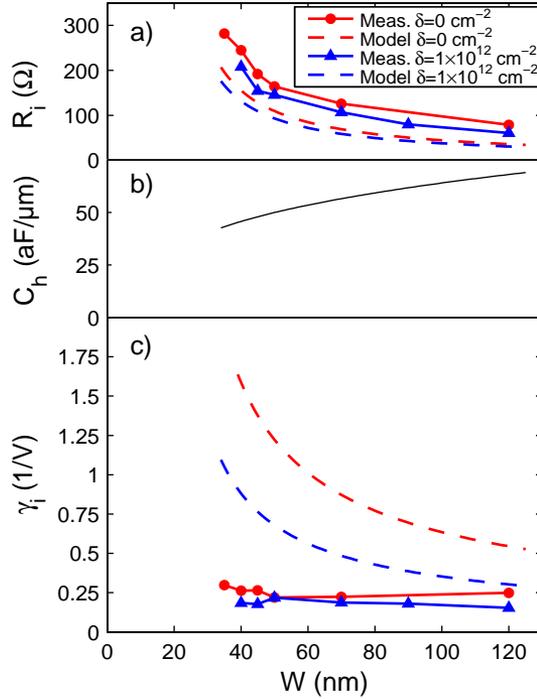


Fig. 6.4: Intrinsic channel resistance (R_i), capacitance C_h and intrinsic curvature (γ_i) at zero bias, as obtained from DC measurements, and modelled values. [C]

The model described the influence of δ -doping on NEP well. For $W = 40$ nm in Fig. 6.5, the low-doped sample showed a 33 % lower NEP_{opt} compared to the high-doped sample (130 pW/Hz^{1/2} and 87 pW/Hz^{1/2}, respectively), whereas the model predicted a 46 % reduction. Hence, both measurements and model show that reduced δ -doping improves both responsivity and NEP in SSDs.

Prior to this work, all SSDs for terahertz detection in the literature have been designed for high electron concentration, either by including δ -doping [14, 16], or in the case of GaN SSDs, using thick AlGaIn barrier layers [15]. Hence the conclusion in this thesis that reducing n_s improves NEP of SSD zero-bias detectors is in direct contradiction to what has been assumed previously.

The demonstrated influence of n_s makes 2DEG structures a questionable choice for SSDs. Since removing the δ -doping of InAs SSDs caused reduced NEP, it is desirable to fabricate SSDs in a structure that does not yield as high n_s for non-intentionally doped samples, while still exhibiting similar μ_n . Since the motivation for using a 2DEG is to have high n_s and μ_n simultaneously, it can be argued that another InAs structure than the InAs/Al₈₀Ga₂₀Sb quantum well may yield better NEP.

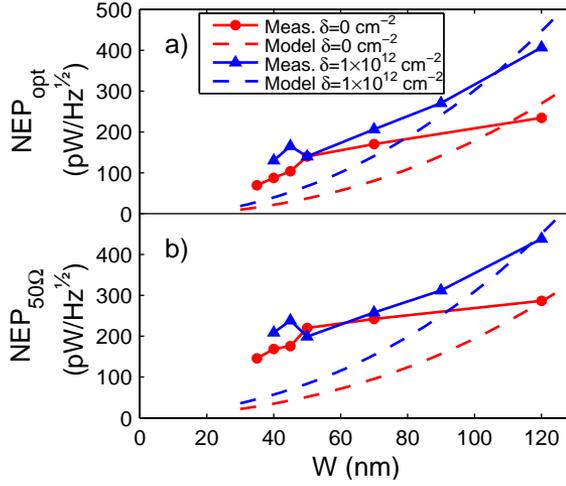


Fig. 6.5: (a) Estimated NEP_{opt} and (b) $NEP_{50\Omega}$ at 50 GHz for the low-doped and high-doped samples compared to modelled counterparts. [C]

6.2 Maximum responsivity

It was noted in section 3.1 that when V_{th} in a zero-bias SSD approaches 0 V, the triode-region SSD model is no longer expected to be valid. For $V_{th} \gg 0$ V, the sub-threshold SSD is a better hypothesis.

To evaluate SSDs with positive V_{th} , MC simulations of InAs SSDs with the same configuration as in section 3.1 was used. By reducing n_s , V_{th} becomes increasingly more positive. Extracted parameters are presented in Fig. 6.6. For high n_s , the SSD channel is in the triode-region as was shown in Fig. 6.1. For sufficiently low n_s , the SSD channel enters sub-threshold conditions. In the sub-threshold region, both model and measurement show that γ_i and $\beta_{50\Omega}$ are independent of n_s (and thus V_{th}). From (3.19) and (2.6), $\gamma_i = q/kT = 38.7 \text{ V}^{-1}$ and $\beta_{50\Omega} = 3870 \text{ V/W}$. The simulations exhibit $\gamma_i \approx 20 \text{ V}^{-1}$ and $\beta_{50\Omega} = 2000 \text{ V/W}$. The difference between simulations and measurements may be due to that W_h is of the same order as W , making the gates less efficient ($n > 1$).

An interesting effect is seen for $NEP_{50\Omega}$ in Fig. 6.6 (a). There is an n_s , and thereby V_{th} , for which $NEP_{50\Omega}$ exhibits a minimum. The minimum $NEP_{50\Omega}$ is reached for slightly higher n_s (and thus slightly more negative V_{th}) than what yields maximum $\beta_{50\Omega}$. Simulated $NEP_{50\Omega}$ in Fig. 6.6 (a) seems to suggest the minimum occurs approximately where the triode-region and sub-threshold SSD models yield the same γ_i , which by equating (3.8) and (3.19) is found as $V_{th} = -kT/q$. For lower n_s , further reduction of n_s increases R_i , whereas γ_i is fairly constant, which degrades $NEP_{50\Omega}$.

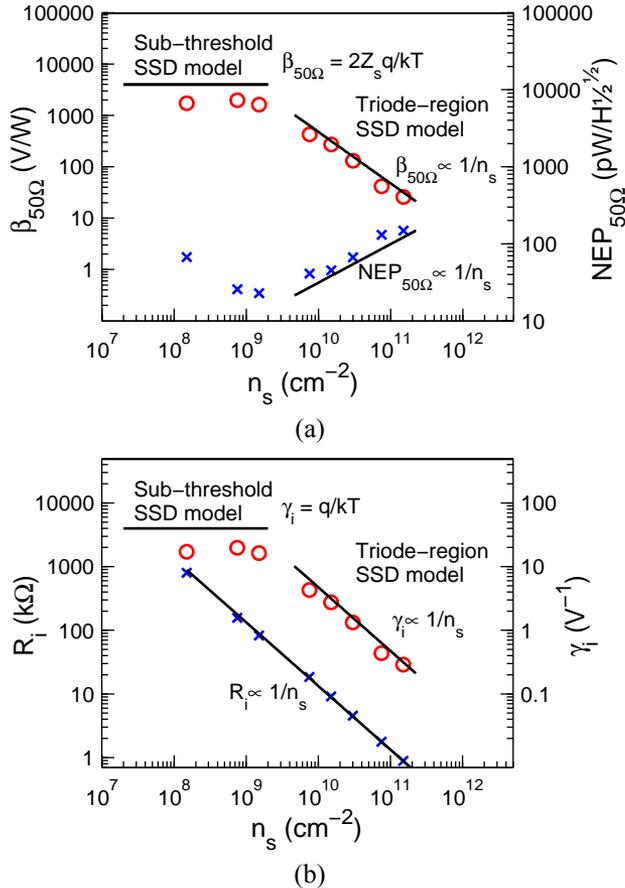


Fig. 6.6: (a) $\beta_{50\Omega}$ (circles) and $NEP_{50\Omega}$ (crosses) obtained from 2-D Monte Carlo simulations and (b) the associated R_i (crosses) and γ_i (circles). Solid lines show modelled values. Simulations by Dr. Ignacio Iñiguez-de-la-Torre.

according to (2.12). There is thus always an optimum channel design, which can be accomplished through the right choice of n_s , C_h and W .

In the design of an SSD, V_{th} can not be controlled independently. In three-terminal MOSFET detectors which operate in a similar way, V_{th} is set arbitrarily while still drawing zero bias current [10]. In such detectors, choosing V_{th} has indeed the same effect as selecting n_s for the zero-bias SSD detector; see Fig. 6.6 (a). In [10], it is said about NMOS detectors with positive V_{th} that “*minimum NEP usually requires a somewhat higher [gate voltage] than required for maximum [responsivity]*”. In zero-bias SSDs, instead of setting the gate voltage, the SSD has to be designed for a desired V_{th} .

6.3 Channel length

Both the triode-region model and the sub-threshold model requires the long-channel approximation to be valid, meaning the channel length L has to be sufficiently long. By extracting γ_i for different L , the minimum L for which the long-channel condition is valid is found. In Fig. 6.7, γ_i and other SSD properties are calculated from DC and RF measurements using the equivalent circuit in Fig. 3.5. Measurements are performed at 2 GHz, meaning C_p can be neglected.

In Fig. 6.7 (a), the modelled γ_i is independent of L , as in (3.7). The value 0.27 V^{-1} is extracted in section 6.4. The model predicts that R_i is simply proportional to L , which is supported by the measurements. More importantly, Fig. 6.7 (a) shows weak L dependence for $L > 1000 \text{ nm}$, and decreased γ_i for $L < 1000 \text{ nm}$. Measurements thus support the analytical result that γ_i is independent of L , for sufficiently large L .

Responsivity and NEP versus L are studied in Fig. 6.7 (b)-(c). The model reproduces the measurements in Fig. 6.7 (b)-(c) except when short-channel effects are present. Increasing L improves β_{opt} and NEP_{opt} . Also $\beta_{50\Omega}$ benefits from increased L . Modelled $NEP_{50\Omega}$ display a minimum for $L = 2200 \text{ nm}$, after which the $NEP_{50\Omega}$ increases due to increased thermal noise, as shown in (3.12). However both measured and modelled $NEP_{50\Omega}$ shows little improvement once long-channel conditions are achieved, for $L > 1000 \text{ nm}$.

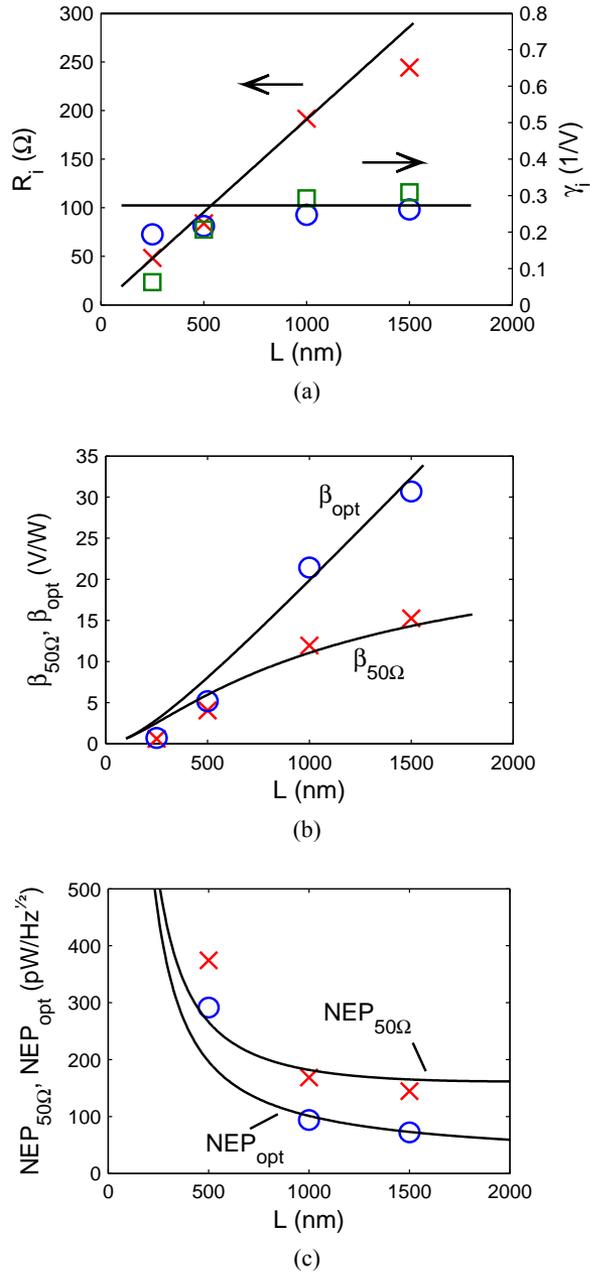


Fig. 6.7: (a) R_i (crosses) and γ_i (circles) as derived from DC- measurements at zero bias for varying L . Other design parameters were according to the reference design. Also shown is γ_i as derived from RF measurements (squares). (b) Measured $\beta_{50\Omega}$ and β_{opt} (c) Measured $NEP_{50\Omega}$ (crosses) and NEP_{opt} (circles). Solid lines in (a) to (c) represent the small-signal values derived from the triode-region SSD model. RF measurements performed at 2 GHz. [C]

6.4 Number of channels

In the same way as for L -dependence in section 6.3, the measured N -dependence of detector parameters compared to the model in Fig. 6.8. The modelled N -dependence of both R_i and γ_i matches measurements well, see Fig. 6.8 (a). An average $\gamma_i = 0.27 \text{ V}^{-1}$ was extracted from RF-measured γ_i . Since γ_i is independent of N , any N -dependence of responsivity and NEP is due to changes in R_i .

Measured and modelled responsivity and NEP are compared in Fig. 6.8 (b)-(c). For a matched detector, low N is beneficial, resulting in both higher β_{opt} and NEP_{opt} . The model predicts $\beta_{opt} \propto 1/N$ and $NEP_{opt} \propto \sqrt{N}$ with $R_{s1} = R_{s2} = 0 \text{ } \Omega$. Fig. 6.8 (b) shows that also $\beta_{50\Omega}$ is increased somewhat for low N . As shown in (2.6), $\beta_{50\Omega}$ is in fact expected to be independent of N when $R_0 \gg Z_s$. An important observation is that $NEP_{50\Omega}$ exhibits a minimum for $N = 28$. For larger N , $NEP_{50\Omega}$ is degraded by low $\beta_{50\Omega}$, and for smaller N by increased thermal noise due to increased R_0 . Moreover, the minimum in $NEP_{50\Omega}$ is not very sharp: for any N in the range 18 to 54, $NEP_{50\Omega}$ deviates from the optimum value by less than 10 %.

The agreement between model and measurements in Fig. 6.7-7 motivates an estimation of the maximum obtainable performance with the InAs SSDs fabrication process outlined in section 3.1. For $W = 35 \text{ nm}$, $\gamma_i = 0.35$ was extracted, for which the model predicts $\beta_{opt} = 1900 \text{ V/W}$, $NEP_{opt} = 7.7 \text{ pW/Hz}^{1/2}$ and $R_0 = 13 \text{ k}\Omega$ at low frequencies for an InAs SSD with $N=1$.

It was concluded in section 5.4 that the InGaAs SSD process in this thesis yielded the lowest $NEP_{50\Omega}(N=1)$ of any SSD process at low frequency, $110 \text{ pW/Hz}^{1/2}$. It would therefore be interesting to estimate the $NEP_{50\Omega}$ expected with $N = 43$ and $W_{mesa} = 15 \text{ } 30 \text{ } \mu\text{m}$, as for InAs SSDs in this thesis. Considering (3.12), a low-frequency $NEP_{50\Omega} = 20 \text{ pW/Hz}^{1/2}$ could be expected.

6.5 Frequency dependence

The parasitic capacitance C_p was in section 3.2 identified as the main reason for degrading responsivity of SSDs at high frequencies. In Fig. 6.9, C_p is extracted from SSDs with different W through S-parameter optimisation of modelled S_{11} to measured S_{11} . The pad parameters L_{pad} and C_{pad} were extracted from measurements on open- and short-circuited pads. Resistances were found from DC-measurements. The C_p extracted from the SSD with absent channels ($W = 0 \text{ nm}$) is identical to the capacitance C_v as defined in the full equivalent circuit in Fig. 3.4. The fact that C_p for $W = 0 \text{ nm}$ was so similar to C_p for $W = 70 \text{ nm}$ motivates the simplification of representing all parasitic capacitance with C_p in Fig. 3.5: C_h can not easily be distinguished from C_v in measurements.

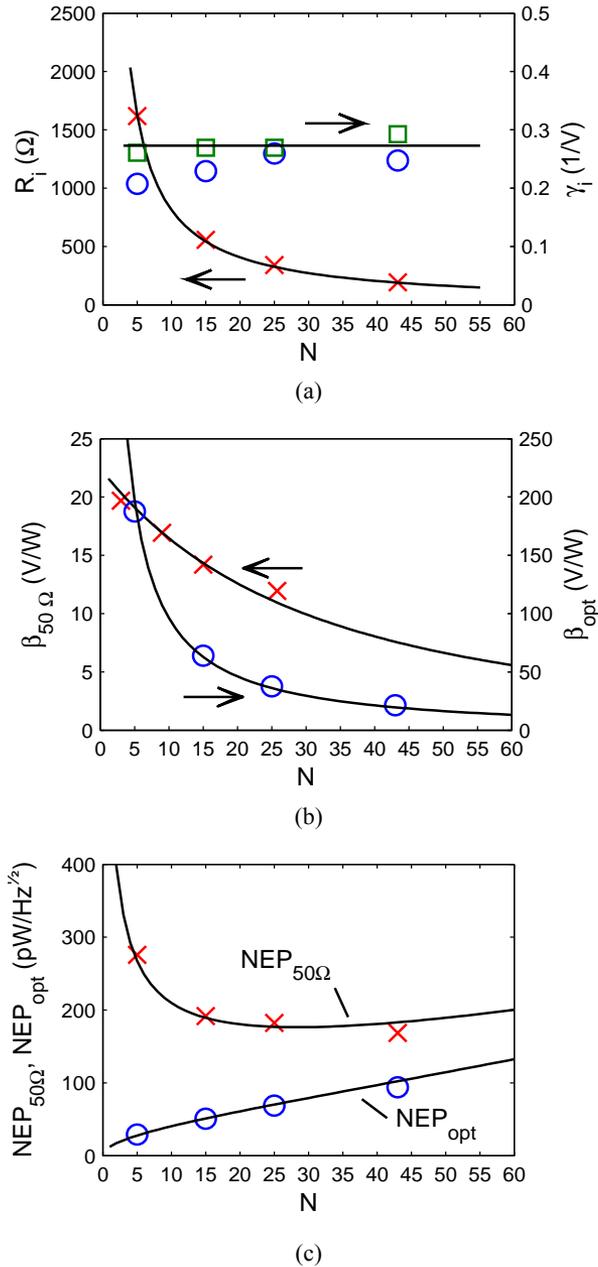


Fig. 6.8: (a) R_i (crosses) and γ_i (circles) as derived from DC-measurements at zero bias for varying N . Other design parameters were according to the reference SSD design. Also shown is γ_i as derived from RF measurements (squares). (b) Measured $\beta_{50\Omega}$ and β_{opt} . (c) Measured $NEP_{50\Omega}$ (crosses) and NEP_{opt} (circles). Solid lines in (a) to (c) represent the small-signal values derived from the triode-region SSD model. RF measurements performed at 2 GHz. [C]

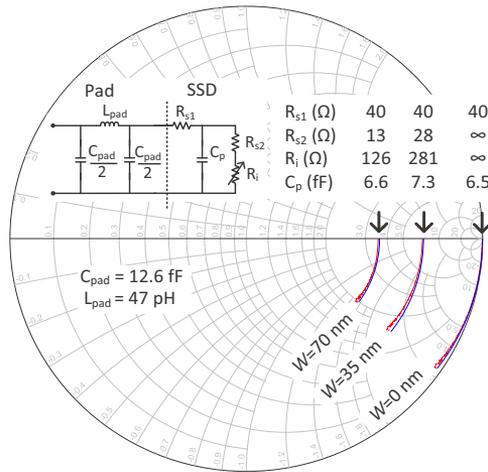


Fig. 6.9: Measured S_{11} for SSDs with three different W (red) and calculated from the small signal model (blue) using the listed model parameter values. The pad is modelled with a π -network. For $W = 0$ nm, the channels are absent and R_i and R_{s2} are modelled as infinite resistances. Frequency 0.25-50 GHz. [C]

The ultimate motivation of the equivalent circuit Fig. 3.5 is to model the SSD's behaviour at high frequencies. In Fig. 6.10 and Fig. 6.11, measured β_{opt} and NEP_{opt} is compared to modelled β_{opt} . The model accurately describes the measured variations, and captures the stronger roll-off of β_{opt} for $W = 35$ nm than for $W = 70$ nm. Thus, the developed equivalent circuit can be said to model the responsivity of SSDs up to 315 GHz.

Using the values in Fig. 6.9, the cut-off frequency f_c can now be calculated using (3.18) to 775 GHz and 615 GHz for $W = 35$ nm and $W = 70$ nm, respectively. MMIC Schottky diodes have demonstrated similar values, 665 GHz [6].

N can be expected to have a strong but indirect influence on high-frequency responsivity. To start with, only a small variation of C_p was seen between devices in Fig. 6.9. In general, C_p can be expected to depend mainly on W_{mesa} and L_{mesa} , however, it has not been investigated in this thesis. To minimise C_p , an SSD should be designed with a minimum W_{mesa} . Thus, in a well-designed SSD, $W_{mesa} \propto N$. At the same time, it can be expected that R_{s1} , R_{s2} and R_i all are proportional to $1/N$. With this in mind, inspection of (3.18) shows that f_c is independent of N . Still, an SSD for terahertz detection should likely be designed with N as small as is possible without increasing $NEP_{50\Omega}$ as shown in section 6.4. The reason is that for low N , the pad can be made more narrow, which reduces C_{pad} . Moreover, membrane technology has the potential of reducing both C_p and C_{pad} [89]. In a real system, both the reactive elements in the SSD itself and the pad should be minimised to maximise the bandwidth of the detector.

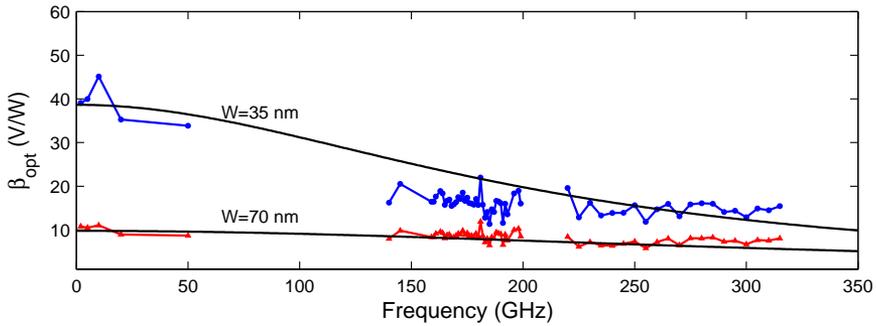


Fig. 6.10: Measured responsivity β_{opt} for SSDs with two different W and modelled (solid lines) using values from Fig. 6.9, with γ_i as a fitting parameter.

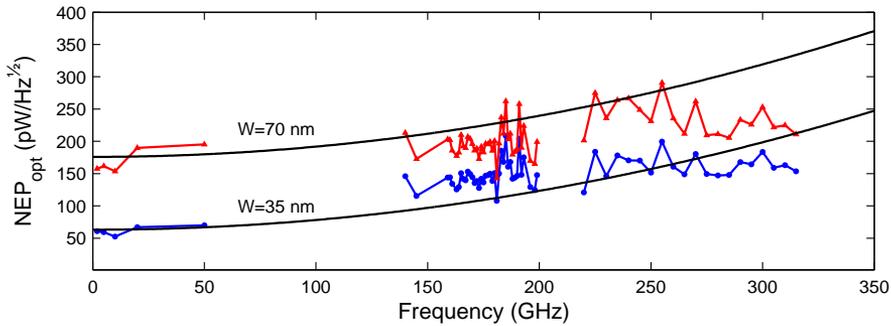


Fig. 6.11: Estimated NEP_{opt} for SSDs with two different W and as modelled (solid lines) using values from Fig. 6.9, with γ_i as a fitting parameter.

6.6 Summary

Before this thesis work, it has been assumed that high carrier concentration beneficial in SSDs for zero-bias detection. Here, it was shown by RF measurements, MC simulations and device modelling that the opposite is true. At the same time, the relevance of the proposed triode region FET-based SSD model was established. It was also demonstrated how detector responsivity saturated for sufficiently low carrier concentrations, as predicted by the sub-threshold SSD model. The existence of an optimum carrier concentration for low NEP was revealed.

The triode-region SSD model and equivalent circuit correctly described the experimental observations from design variations in channel width, channel length and number of channels. A minimum channel length ($1 \mu\text{m}$) for the InAs SSD process used here was identified, as well as an optimum number of channels (18). The responsivity was accurately modelled up to 315 GHz as demonstrated by measurements.

Chapter 7

Conclusions

SSDs with InAs, InGaAs and graphene channels were explored as potential zero-bias terahertz detectors. The demonstrated InGaAs SSD advanced the state-of-the-art for low-noise detection using SSDs. Through modelling, measurements and simulations, a powerful set of tools for further optimisation of SSDs was provided.

The first InAs SSDs were fabricated by implementing a new process technique for fabrication of the nanometre-sized isolation pattern required for SSDs in the chemically unstable but electrically promising InAs/Al₈₀Ga₂₀Sb heterostructure.

SSDs were characterised by DC and RF in on-wafer and quasi-optical measurements. InGaAs SSDs exhibited state-of-the-art NEP for SSDs, estimated to 40-150 pW/Hz^{1/2} for 2-315 GHz with a 50 Ω source. The weakest roll-off of responsivity at high frequencies was observed for InAs SSDs, which exhibited a cut-off frequency of 600 GHz. In quasi-optical measurements, an InAs SSD detector reached an NEP of 4400 pW/Hz^{1/2} at 600 GHz. Graphene SSDs showed the potential of reaching similar NEP as InAs SSDs, and showed a flat responsivity from 1 to 67 GHz.

An analytical model was derived which described how the SSD design affect detector properties. Responsivity of InAs SSDs up to 315 GHz was reproduced by an equivalent small-signal circuit. The model and experiments showed that SSD channels should be designed for low electron concentration to reduce NEP, whereas SSD have previously always been designed for high electron concentration. The model and Monte Carlo simulations showed how the responsivity saturates for sufficiently low carrier concentrations, theoretically reaching the responsivity of Schottky diodes. For a certain carrier concentration, a minimum, process-dependent NEP is reached. Furthermore, the model and measurements for various SSD designs showed that for a certain process and application, there is an optimum channel length and number of channels for best detector performance in terms of responsivity and NEP.

Chapter 8

Future outlook

This thesis has presented studies on a relatively novel and immature semiconductor device for zero-bias detection, the SSD. In order to successfully compete with established technologies such as the Schottky diode, the SSD must be improved even more than what was done in this thesis work. The results here, however, show that much progress can be made before the theoretical limit is reached. With the presented model, it was for example predicted that an InGaAs SSD with more channels would yield an NEP of $20 \text{ pW/Hz}^{1/2}$ with a $50 \text{ } \Omega$ source at low frequencies.

The MC simulations for InAs SSDs predicted a flat responsivity up to $> 2 \text{ THz}$ by neglecting capacitance through the substrate. The capacitance through the substrate could be reduced through membrane technology, as is done for Schottky diodes [89]. Further, MC simulations assumed an infinitely thick SSD. Yet, all SSDs in the literature, and also in this thesis have been fabricated in thin semiconductor sheets using 2DEGs. This thesis showed that this may not be desirable. By switching to for example a silicon-based technology, thick channels with deep trenches could be manufactured with large precision [90]. Further, the electron concentration can be made drastically lower in silicon than in III-V 2DEGs.

The SSD was in this thesis treated as a transistor with gate connected to drain. A natural way to further examine the model would be to fabricate a three-terminal SSD. When the gate can be biased independently, the threshold voltage can be extracted. Another approach could be to add a back gate to a conventional SSD structure. Sweeping the back-gate bias would then be equivalent to sweeping the doping, allowing the minimum NEP for a certain SSD process to be extracted.

The large advantage for the SSD lies in its simplicity: it can be fabricated through a single etch in a sheet of semiconductor. SSDs have indeed been demonstrated in low-cost polymer technologies [38] and transparent indium-tin-oxide [39], up to 50 MHz . The graphene SSD technology demonstrated in this thesis could therefore be an alternative for low-cost detector applications, potentially in the terahertz regime.

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Paper A

Nanochannel diodes based on InAs/Al₁₈₀Ga₂₀Sb heterostructures: Fabrication and zero-bias detector properties

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L. Desplanque, X. Wallart, and J. Grahn

Journal of Vacuum Science & Technology B, vol. 33, p. 021207, 2015.

Paper B

Terahertz detection in zero-bias InAs self-switching diodes at room temperature

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L. Desplanque, X. Wallart, and J. Grahn

Applied Physics Letters., vol. 103, no. 13, p. 133504, 2013.

Paper C

Optimization and Small-Signal Modeling of Zero-Bias InAs Self-Switching Diode Detectors

A. Westlund, P. Sangaré, G. Ducournau, I. Iñiguez-de-la-Torre, P.-Å. Nilsson, C. Gaquière, L. Desplanque, X. Wallart, J.-F. Millithaler, T. González, J. Mateos, and J. Grahn

Solid-State Electronics., vol. 104, pp. 79–85, Feb. 2015.

Paper D

On the effect of δ -doping in self-switching diodes

A. Westlund, I. Iñiguez-de-la-Torre, P.-Å. Nilsson, T. González, J. Mateos, P. Sangaré, G. Ducournau, C. Gaquière, L. Desplanque, X. Wallart, and J. Grahn

Applied Physics Letters, vol. 105, no. 9, p. 093505, Sep. 2014.

Paper E

Graphene self-switching diodes as zero-bias microwave detectors

A. Westlund, M. Winters, I. G. Ivanov, J. U. Hassan, P.-Å. Nilsson, E. Janzén, N. Rorsman, and J. Grahn

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