Passive Reciprocal high-pass/low-pass 4-bit phase shifter at 2.45 GHz

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***Abstract*— This paper presents the design, fabrication and measurement of a low cost, reciprocal 4-bit phase shifter at 2.45 GHz ISM band using COTS components. High-pass/low-pass filters in π configuration are used to implement the phase shifter bit sections. SPDT switches are realized with BAP51 dual PIN diodes, with resonant inductors in the off-state to provide high isolation. The driver circuit consisting of 74AHC240 octal buffer/inverter was implemented to switch the PIN diodes and control the phase states. A compact layout of the 4-bit phase shifter and driver circuitry was fabricated on a 4-layer FR4 substrate. The total size of the PCB board was 4.9x5.3 cm. The measurement results showed an RMS phase error better than 4.1°, insertion loss better than 8.8 dB and return loss better than 13 dB. The maximum power consumption of the 4-bit phase shifter was 80 mW.**

***Keywords*— ISM band, phase shifter, p-i-n diodes**

I. INTRODUCTION

Phase shifters are an active area of research in modern transceiver systems. They find their applications in almost all communication systems such as smart antennas in base stations, mobile phones and wireless LAN. However phase shifters are mainly used for electronic beam steering in phased array antenna systems of radars and satellites [1].

Modern phase shifter designs are focusing on improving insertion loss, broad bandwidth, switching speed, size and financial cost. There are numerous topologies for implementing the phase shifter such as switched transmission line, loaded line, reflection type, high-pass/low-pass and all-pass network [2]. In all these phase shifter topologies, switch is implemented using either PIN diodes or FETs. PIN diodes have the advantage of simple biasing network and lower cost.

In this work a 4-bit phase shifter was designed for the ISM band covering 2.4-2.5 GHz, using PIN diodes and high-pass/low-pass topology. The control circuitry was implemented using 74AHC240 octal buffer/inverter IC suitable for switching the 16 phase states in a 4-bit phase shifter.

II. PHASE SHIFTER DESIGN

The design approach was to select a suitable phase shifter topology, SPDT switch and control circuit, with respect to design specifications, such as, operating frequency of 2.4–2.5 GHz, 4 bit sections, RMS phase error of less than 5°, insertion loss less than 9 dB, return loss above 10 dB, small size, low cost and reciprocity.

A. Topology: High-Pass/Low-Pass Filters

High-pass/low-pass phase shifters were first introduced in [3]. This topology was considered suitable for implementation at ISM frequencies, due to better performance in terms of return loss, insertion loss, and compact size with respect to other phase shifter topologies. Other topologies involving transmission lines for phase shifting resulted in long transmission line lengths at lower GHz frequencies.

The high-pass filter in π configuration consists of series capacitor and shunt inductors, and the low-pass filter consists of a series inductor and shunt capacitors. The insertion phase undergoes a phase advance in high-pass filter and a phase delay in low-pass network. Phase shift was obtained by switching between the high-pass and low-pass filter. To provide return path for the DC current and for the implementation of PIN diode switches, a large value of DC blocking capacitor can be used in the high-pass filter. Fig. 1 shows the schematic for one complete bit section of the phase shifter.

Momentum and Monte Carlo simulations were performed using Agilent ADS 2009, for individual as well as combined

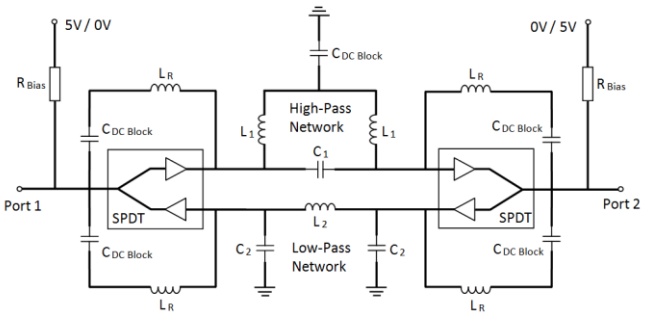

Fig. 1. Schematic showing one bit section of the 4-bit phase shifter

phase shifter design. The simulations were also performed for the 24 different bit arrangements, the 4 bit sections can be cascaded with each other. Bit arrangement of 45°-90°-22.5°-180° showed optimum performance of RMS phase error.

For the filter networks and resonant inductors discrete capacitors and multilayer inductors from Murata GQM18 and LQG18 series were used. Multilayer inductors are low cost as compared to wire wound and thin film inductors. Murata GRM18 series capacitors were used for DC blocking at appropriate places in the cascaded 4-bit phase shifter. Table I

shows the discrete component values used for the design of each bit section.

TABLE I
HIGH-PASS/LOW-PASS FILTER COMPONENT VALUES

Bit Section	L1 (nH)	C1 (pF)	L2 (nH)	C2(pF)
22.5°	27	27	1.5	0.5
45°	22	3.9	1.5	0.8
90°	4.7	2.2	1.5	1.3
180°	1.5	1.8	1.8	2.4

B. SPDT Switch

The SPDT switch was implemented using BAP51 dual PIN diodes. Each bit has 2 SPDT switches and the complete 4-bit phase shifter has 8 SPDT switches. The BAP51 dual PIN diode has an on-state resistance of 3.6 Ohm and off-state capacitance of 0.3 pF. The off-state capacitance was resonated at 2.45 GHz with 12 nH inductor to provide high isolation and avoid signal leakage.

C. Control Circuit

The driver control circuit controls the 16 states of the 4-bit phase shifter. 74AHC240 octal buffer/inverter was used for controlling the dual-diode switch in each bit section. The 74AHC240 operates with CMOS input levels. The advantage of using CMOS logic level buffer/inverter driver was that, it accepts lower signal levels and convert them to regulated 5V output voltage level. Power consumption is also lower in CMOS compared to TTL.

III. FABRICATION

Fig. 2 shows the fabricated 4-bit phase shifter with driver control circuit. A 4-layer FR4 substrate with 1mm thickness was used for layout and fabrication. The top layer is RF layer. Layer 2 is the RF and DC ground, 0.28 mm from the top layer. Layer 3 is the digital control layer used for routing the control signal from the octal buffer/inverter driver to the diode switch. Layer 4 is also ground layer.

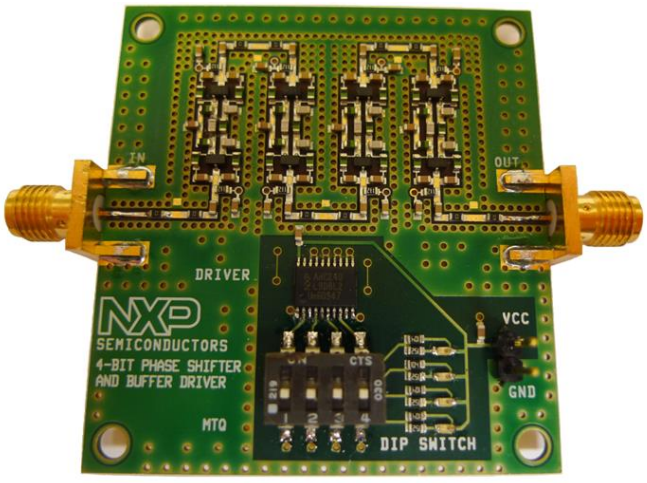

Fig. 2. Fabricated 4-bit phase shifter and driver control circuitry.

For compact size, the filter networks were placed vertically. Via holes providing uniform grounding were placed at regular intervals along the transmission line. and on the circuit board. For discrete capacitors and inductors, 0603 Murata chips were mounted on PCB circuit through standard soldering process. The dimension of the PCB board is 4.9x5.3 cm.

IV. MEASUREMENT RESULTS

Measurements were performed for the 4-bit phase shifter using R&S ZVA 24 Network Analyzer. Fig. 3-7 shows the measurement results for the 4-bit phase shifter design.

RMS phase error is the main figure of merit determining the performance of a phase shifter. Fig. 3 shows the measurement result for RMS phase error of the 4-bit phase shifter. The minimal RMS phase error slightly outside the ISM frequency band is due to use of standard inductor or capacitor values in the Murata component series.

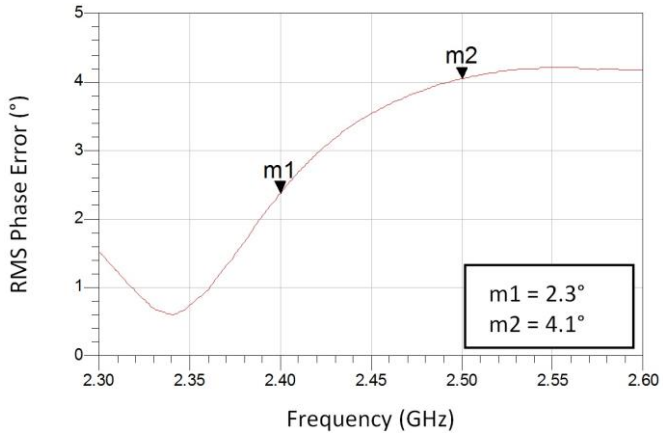

Fig. 3. Measurement result for RMS phase error of the 4-bit phase shifter.

Fig. 4 shows the measurement result for insertion loss. The main contribution in insertion loss comes from the on-state resistance of the PIN diode, where each PIN diode contributes around 1 dB insertion loss. The maximum insertion loss is of

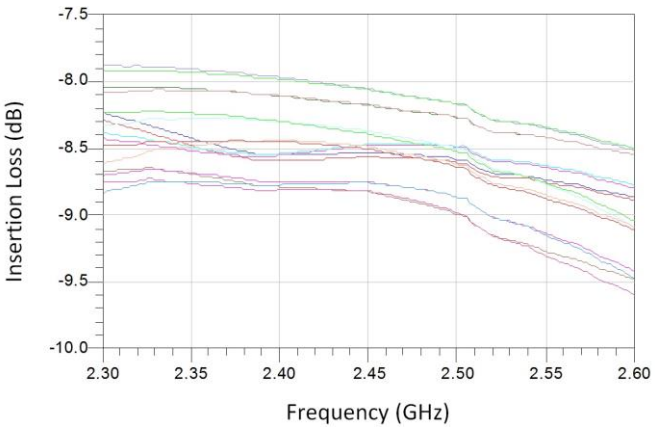

Fig. 4. Measurement result for insertion loss of the 16 phase states.

the phase shifter is 8.8 dB.

Fig. 5-6 shows measurement result for the input and output return loss, which is better than 13 dB and 16 dB respectively. The return loss is comparatively better than the reported phase shifter designs summarized in Table II, due to the use resonant approach. The power consumption of the 4-bit phase shifter was 80 mW, where each bit section consumes around 19.5 mW.

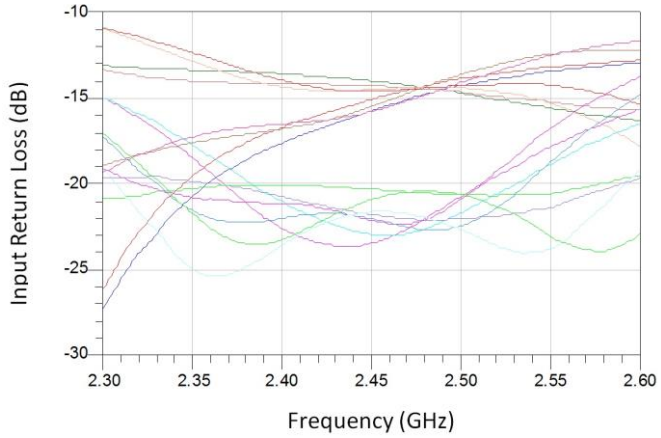

Fig. 5. Measurement result for input return loss.

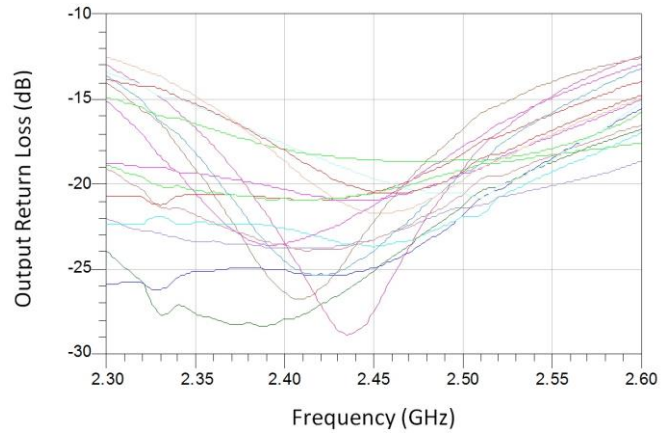

Fig. 6. Measurement result for output return loss of the 4-bit phase shifter.

V. CONCLUSION

The design, fabrication and measurement of a low cost, passive, reciprocal, 4-bit phase shifter is presented. The phase shifter network was based on high-pass/low-pass filter topology in π configuration. COTS components are used for implementing the filter networks, as well as SPDT PIN diode switches and control circuit. The fabrication was performed on FR4 substrate. Measurement results showed RMS phase error of 4.1°, insertion loss of 8.8 dB and return loss of 13 dB.

TABLE II
COMPARISON OF PHASE SHIFTER DESIGNS

Ref.	Type	Switch	Freq. (GHz)	Bits	RMS PE (°)	IL (dB)	RL (dB)
[4]	MMIC-AP	GaAs - pHEMT	S- band	5	2.8	7	9.5
[5]	MMIC-HP/LP	GaAs - pHEMT	1.4 - 2.4	4	3	3.2	9.5
[6]	PCB-TL	GaAs MMIC	1.0 - 2.0	4	3.6	4.0	15
[7]	PCB-TL	PIN diode	2.0 - 3.6	1	7	0.7	11
[8]	Discrete-HP/LP-BP-AP	GaAs MMIC	0.5 - 1.1	4	6	2.5	13
[9]	Discrete-AP	PIN diode	2.0 - 4.0	4	6	12.5	10
This Work	Discrete-HP/LP	PIN diode	2.4 - 2.5	4	4.1	8.8	13

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