A 474 GHz HBV Frequency Quintupler Integrated on a 20 μm Thick Silicon Substrate

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***Abstract*—We present a silicon integrated Heterostructure Barrier Varactor (HBV) frequency quintupler (×5) operating between 440 GHz and 490 GHz. By epitaxial transfer of InP-based HBV material structure onto silicon-on-insulator (SOI), a uniform and accurate thickness (20 μm) of the frequency quintupler chip is achieved. In a single stage this device delivers 2.8 mW of output power at 474 GHz, when pumped with 400 mW at 94.75 GHz, corresponding to conversion efficiency of 0.75%. The present device exhibits a 3-dB bandwidth of 4%.**

***Index Terms*—Compound semiconductors, epitaxial transfer, frequency multipliers, heterostructure barrier varactors, monolithic integrated circuits, sub-microwave diodes, submillimetre wave, THz sources, wafer bonding.**

I. Introduction

A COMMON METHOD to generate power at THz frequencies is to use a single stage, or a chain of frequency multipliers [1]. These are often based on transistors [2], [3], Schottky diodes [4] or heterostructure barrier varactors (HBVs) [5]–[8] on GaAs or InP substrates. In comparison with transistor and Schottky diode devices, the HBV generates only odd harmonics of the input signal, which reduces the number of idler frequencies for high order frequency multipliers [9]–[11]. Because of the symmetrical differential capacitance and anti-symmetric current-voltage (I-V) characteristics, HBV-based frequency multipliers do not require a DC bias. For these reasons the complexity of HBV-embedded circuitry can be greatly reduced.

An early example of InP-based single barrier varactor frequency quintupler at 170 GHz showed a flange-to-flange efficiency of 0.78% [12]. Further development of the discrete diode technology and use of an epitaxial stack of several barriers resulted in 11% conversion efficiency at 100 GHz [13], 60 mW of output power at 175 GHz [14], and 5 mW at 210 GHz [15]. These circuits utilize a flip chip assembled HBV diode on a microstrip circuit. However, at the frequencies beyond 300 GHz high assembly accuracy is required, thus monolithic device integration with the circuit gives better results and reproducibility [16]. Along with that, the monolithic integrated circuit approach becomes beneficial when the substrate thickness is reduced to micrometer levels [7]. However, GaAs and InP are brittle materials, such that when mechanically thinned they are not easy to handle nor assemble. Furthermore, the thinning process does not assure a uniform and accurate thickness of the circuit substrate. Beside poor mechanical properties of GaAs and InP, these materials are characterized by a low thermal conductivity (κ). Thus the heat dissipation from the active device is limited, which consequently affects the overall multiplier performance [17].

Considering the mechanical and thermal constraints of the HBV frequency multipliers, use of silicon as a host substrate could be beneficial. Silicon is a low cost material. It has excellent mechanical properties that can be exploited through MEMS fabrication techniques, which allows the realisation of complex structures, i.e., membranes, integrated antennas and waveguides [18]–[21]. High thickness accuracy can be achieved when a silicon-on-insulator (SOI) substrate is used [22], and processes like mechanical lapping or dicing can be replaced with a silicon reactive ion etching technique. Moreover, in comparison with GaAs and InP, Si has a better thermal conductivity ($\kappa = 160\ \mathrm{W \cdot m^{-1} \cdot K^{-1}}$), that results in an improved device performance when operated at high power levels [23], [24]. All of these factors make silicon a suitable substrate candidate for high power mm-wave and THz applications. The integration of III-V semiconductors with silicon is possible by epitaxial growth and transfer methods [25]–[29].

In this paper we present a silicon integrated HBV-based frequency quintupler (×5) for 474 GHz, optimized for commercial 94 GHz power amplifiers. The HBV epitaxial material structure was transferred onto SOI using a low-temperature plasma-assisted wafer bonding technique [30]. The substrate thickness for the microstrip circuitry was defined from a 20 μm thick and high resistivity device layer of the SOI wafer. The peak output power of 2.8 mW was measured at 474 GHz. The device provides enough power for various applications across the frequency range 440–490 GHz. The measurement results are compared with theoretical estimations. It is shown that the limiting factor for high power operation of this diode is the thermal resistance, rather than electrical properties such as high conduction current or breakdown voltage.

II. Quintupler Design

A. Device Design

Because of the high input power that the circuit is aimed management is important. Simultaneously there is a limit to how

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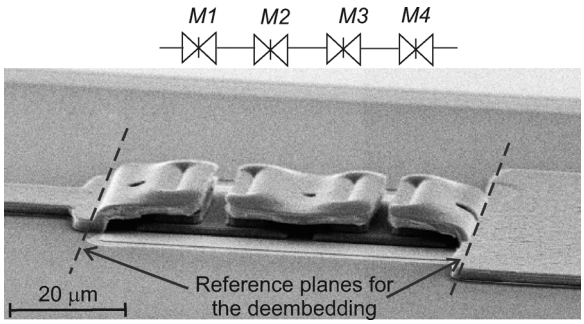

Fig. 1. SEM image of four mesas HBV diode including the air-bridge connections to the microstrip circuit.

large the device area can be, and how far apart the individual mesas can be positioned, without sacrificing the power conversion efficiency. Therefore, the optimal design is a trade-off between these two conflicting limitations.

The HBV material structure was optimized for low conduction current, thus maximized breakdown voltage per barrier [31], [32]. Details of the epitaxial structure can be found in [7]. The device was optimized with the self-consistent electro-thermal model presented in [33] and harmonic balance simulation techniques. The HBV diode consists of four mesas connected in series, resulting in total 12 barriers (3 barriers/mesa), as shown in Fig. 1 The first two mesas (*M1*, *M2*) are larger than the two other mesas (*M3*, *M4*), hence the voltage swing over the individual mesas is distributed evenly, and the maximum current through the device is kept within the limits set by the doping concentration in the modulation layers and the electron saturation velocity [31]. Designed dimensions of the mesas are 261 μm^2, 232 μm^2, 203 μm^2 and 203 μm^2 for the *M1*, *M2*, *M3* and *M4* mesa, respectively.

B. Circuit Design

The microstrip circuit components were designed with circuit simulator and 3-D electromagnetics simulation tools. Power dissipation in the silicon substrate, due to the conductivity and dielectric losses, was included assuming a loss tangent of 10^{-4}.

The signal at the fundamental frequency (ω_0) is coupled to the circuit with a waveguide probe as marked in Fig. 2(a). The input matching is realized with a symmetric pair of open-stubs in combination with a segment of 50 Ω microstrip line. The open-stubs also act as stop-filters for the third and fifth harmonic. The generated signal at the fifth harmonic is coupled to the output waveguide with a waveguide probe, noted in Fig. 2(a). The output probe acts as an open stub for the fundamental frequency and for the third harmonic, providing RF ground at these frequencies.

The detailed circuit dimensions are given in Fig. 2(a), and the image of the circuit assembled in the waveguide block is shown in Fig. 2(b). The final chip area is 0.27 mm^2, and it is bonded to the circuit channel with a solder paste. The input waveguide is a standard WR-10. The output waveguide dimensions are 0.22 mm×0.44 mm (WR-1.7), and it was designed to cut-off the idler signal ($3\times\omega_0$) for an input signal below 98 GHz. The circuit channel dimensions are 0.7 mm×0.2 mm×0.1 mm (length × width × height). The design dimensions of the circuit channel connecting the input and output waveguides assure

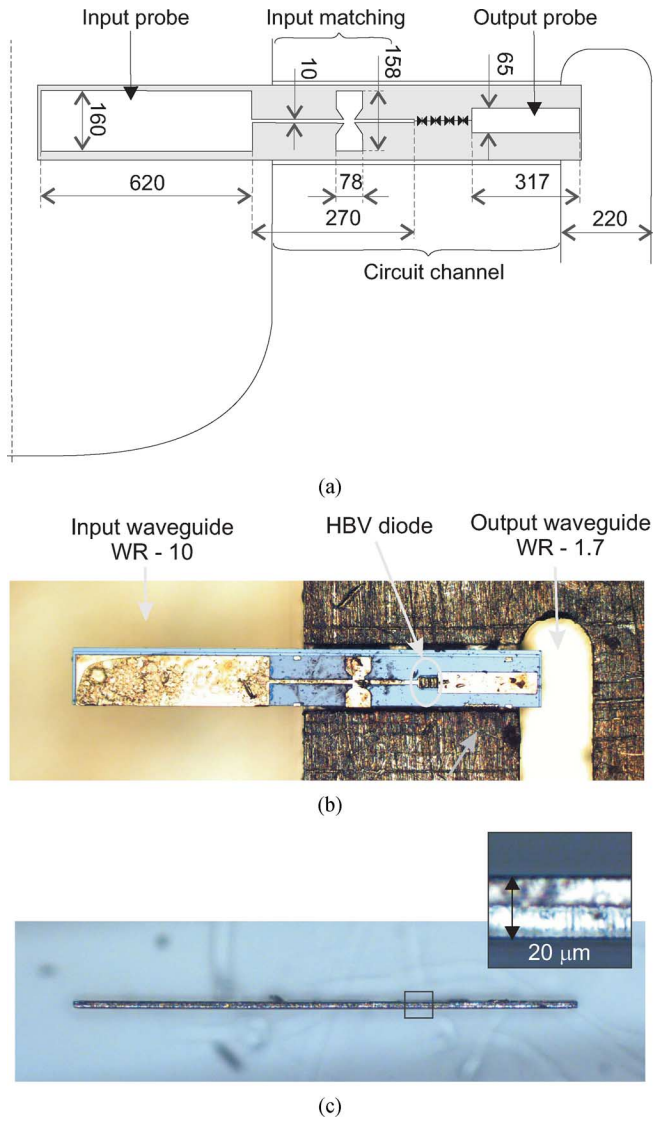

Fig. 2. (a) Layout of the frequency quintupler (all dimensions are in μm). (b) Microscope image of the quintupler chip assembled in the waveguide split-block, and (c) side view of the chip. Chip dimensions are 1.5 mm×0.18 mm×0.02 mm (length × width × thickness).

that the higher order modes at frequencies up to 600 GHz are effectively cut-off. The simulated optimum embedded impedances for the diode at a fundamental frequency of 95 GHz, at the reference planes marked with the dashed lines in Fig. 1, are $Z_1 = 8 + 40i$ [Ω], $Z_3 = -4.5i$ [Ω], and $Z_5 = 136 - 31i$ [Ω], respectively. In Fig. 3, the Smith chart with simulated input and output reflection coefficients for embedded circuits are shown.

III. Fabrication

A. Epitaxial Transfer

An $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/AlAs$ material structure for the HBV diodes was grown by molecular beam epitaxy on a lattice matched 3" InP substrate. This material was transferred onto the SOI substrate using a process of low-temperature plasma-assisted wafer bonding [30]. The epitaxial transfer process parameters can be found in [34]. An SOI wafer consists of three layers; a 300 μm thick silicon handle, followed

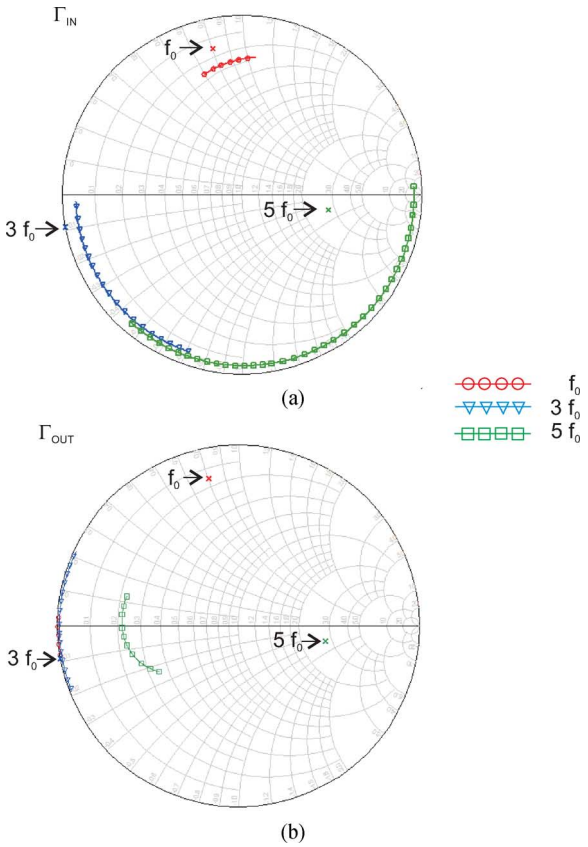

Fig. 3. Smith chart showing (a) input and (b) output reflection coefficients, Γ_{IN} and Γ_{OUT}, for the embedding circuits (system impedance: $\mathrm{Z}_0 = 50\ \Omega$). The frequency sweep is $f_\circ \in (88, 100)$ GHz. $\times$ marks the estimated optimum embedded impedances for the diode at 95, 285, and 475 GHz.

by a 1 μm buried oxide, and a 20 μm thick, high resistivity ($\rho = 10\,000\ \Omega$ cm) silicon device layer. Wafer bonding is followed by the wet etch removal of InP substrate in HCl:H_2O (1:5) solution that exposes the epitaxial material. Subsequently, the SOI wafer with the HBV structure is diced into 20×20 mm^2 chips.

B. Device and Circuit

The fabrication process of the integrated frequency quintupler circuits begins with HBV diode mesas definition. Details of the diode structure are shown in Fig. 5(c). In the first photolithography step openings for the ohmic contacts are patterned. The ohmic contact metallization consists of Ni/Ge/Au (100 Å/500 Å/1500 Å) with additional 2000 Å layer of Ti. The titanium layer is used as a mask for dry etching of the mesas. The ohmic contact metallization evaporation is followed by a lift-off process, and annealing at 270°C for 60 s in N_2 atmosphere. The mesas are first dry etched in CH_4 atmosphere, and subsequently wet etched in H_2SO_4:H_2O_2: H_2O (1:4:200) in order to remove damage from the dry etching on the mesa side walls. During the dry and wet etching the cross section dimensions of the mesas were reduced by approximately 1 μm on each side. Diode formation is followed by electrical isolation of the mesas. Isolation involves a photolithography step and wet chemical etching of 1 μm thick $In_{0.53}Ga_{0.47}As$ buffer layer in H_3PO_4:H_2O: H_2O (1:1:25). A 100 nm thick SiO_2 is deposited

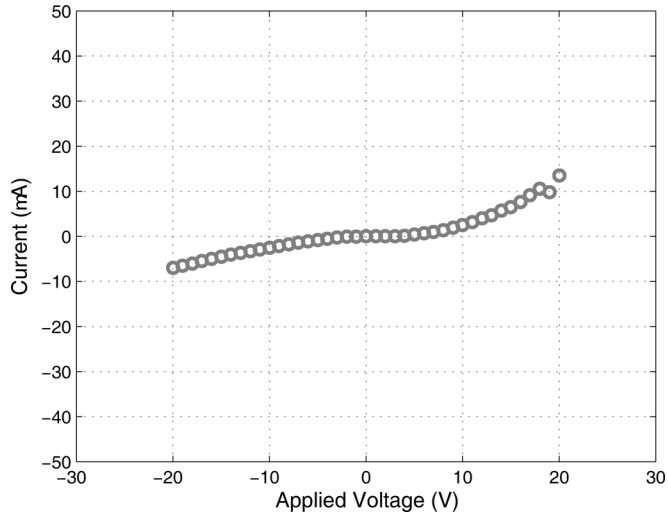

Fig. 4. Measured current–voltage characteristics of the present HBV diode. The measurements were performed at room temperature and in dark conditions.

on the silicon substrate by reactive sputtering. This layer acts as a passivation and reduces the surface conductivity.

Prior to electroplating of the microstrip circuit elements and air-bridge connections to the diode a PMGI DUV resist is applied. Subsequently, a seed layer comprised of Ti/Au (10 nm/100 nm) is DC-sputtered on the chip surface. In following photolithography step the electroplating area defining air-bridge connections and microstrip components is patterned. Then a 2 μm thick gold layer is electroplated. The seed layer is etched using the ion beam sputtering, and the PMGI layer is desolved in warm photoresist remover.

The measured current–voltage (I–V) curve of the final device, using a semiconductor device analyser (Agilent B1500A) is shown in Fig. 4. I–V characterization was performed at room temperature and in dark conditions. Measured low conduction current of the device across a wide voltage range ensures varactor mode operation even at high input power levels.

C. Backside Processing

In Fig. 5(a)–(b), the process flow of the backside fabrication is outlined. Prior to the backside processing, the devices and circuits are first protected with a thick resist, and then mounted topside-down on a sapphire carrier wafer with an adhesive layer, see Fig. 5(a). Then, the silicon handle wafer is dry etched in SF_6 atmosphere. The high selectivity towards SF_6 dry etching between silicon and silicon dioxide ensures that the etching process will stop when the buried oxide is reached. Subsequently, the buried oxide is wet etched in the buffer oxide etchant solution. After removing the silicon handle and the buried oxide the chip is first patterned using IR backside alignment. Ti/Au (5 nm/200 nm) backside metallization is e-beam evaporated. Afterwards, a thick photoresist is used to pattern the chip backside. This photoresist serves as an etch mask protecting the circuits area. The exposed trenches are dry etched by deep reactive ion etching (Bosch process) [35], separating individual circuits. After etching, the individual circuits are released from the carrier wafer by dissolving the protecting resist in warm acetone.

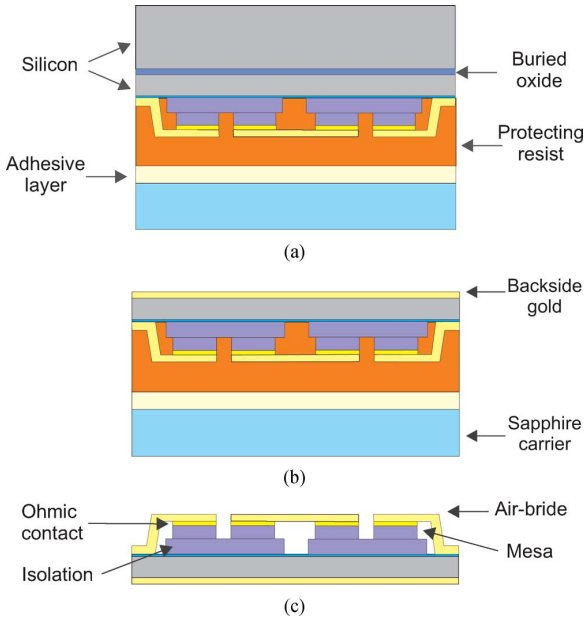

Fig. 5. Process steps for 20 μm thick circuits. (a) Topside-down mounting on a carrier wafer. (b) Dry etch removal of the bulk silicon handle, followed by wet etch of the buried oxide. Subsequently, the backside metallization is deposited. The silicon is patterned with a thick resist, and the individual circuits are defined with the Bosch process. (c) After dissolving the protecting resist and release of the circuits from the carrier. (NB! The drawings are not in scale.).

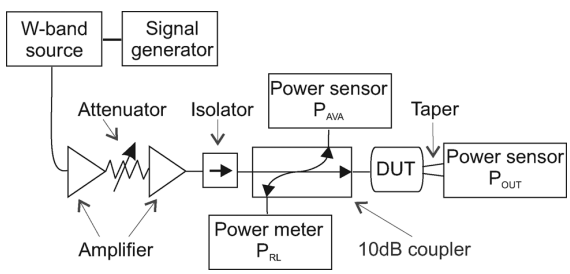

Fig. 6. Diagram of the frequency multiplier measurement setup.

IV. RF Characterization

A. Measurement Setup

A diagram of the RF characterization setup is shown in Fig. 6. The input signal was provided by an Agilent E8257D power generator, followed by a $\times$ 6 W-band frequency extender from Agilent/OML with 7 dBm of output power. This signal was amplified with a setup consisting of two series connected GaN power amplifiers from Wasa Millimeter Wave AB. The 3 dB bandwidth for each of the power amplifiers in the chain is 12 GHz. The amplifiers are biased with $\mathrm{V_{DC}} = 13$ V and $\mathrm{I_{DC}} = 0.6$ A. The input power into the second amplifier was adjusted with an attenuator. The amplifiers chain was used to feed and provide input power signal to the frequency multiplier. To minimize the effects of high VSWR, an isolator is used. Moreover, a 10 dB directional coupler is used to accurately monitor and control the available power (P_{AVS}) as well as probing the reflected power (P_{RL}). P_{AVS} and P_{RL} were monitored with the Agilent power meter (E4418B) and Erickson PM4 power meter, respectively. The output power from the frequency multiplier at the fifth harmonic was measured with an additional Erickson PM4 power meter. A WR-1.9 to WR-10 waveguide taper was used to adapt the sensor waveguide (WR-10) to the quintupler (DUT) output waveguide (WR-1.7).

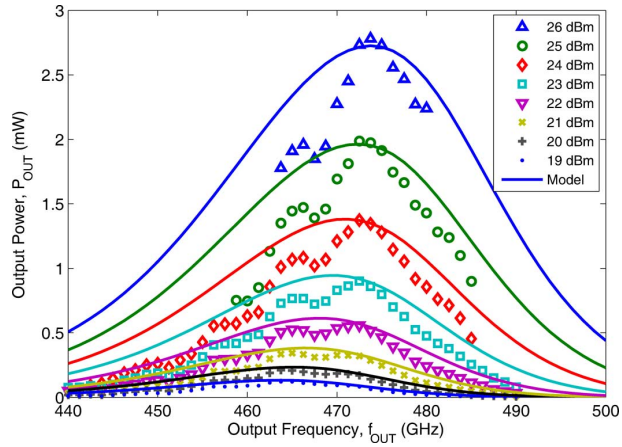

Fig. 7. Measured output power versus output frequency for constant available input power levels from the amplifiers chain. The measurements data is given as discrete points, while the solid lines correspond to simulation results.

B. Results

The output power measurements were performed for constant available input power (P_{AVS}) levels, ranging from 19 to 26 dBm, with 1 dBm increment. The input frequency was swept from 88 to 98 GHz with 0.25 GHz steps. Due to the limitations of the available power from the amplifier some of the frequency points for P_{AVS} beyond 21 dBm are omitted.

In Fig. 7, the measured output power at the fifth harmonic (P_{OUT}) versus the output frequency for different P_{AVS} levels are plotted. The measured data is compared with the harmonic balance simulation results. The peak output power of 2.8 mW was measured at 474 GHz for 26 dBm of P_{AVS}. The 3 dB bandwidth for the device is estimated to 4% (20 GHz).

In addition to this measurement, the frequency quintupler was characterized at 474 GHz. The PAVS was swept from 18 to 26 dBm with 0.5 dBm increments. Obtained P_{OUT} and corresponding conversion efficiency are shown in Fig. 8. Maximum conversion efficiency measured for the device is 0.75%.

V. Discussion

To better understand the device performance under high RF input power levels, the quintupler performance was analysed with harmonic balance simulations together with a simplified HBV electro-thermal model [33]. Due to the etching process the mesa areas were reduced to approximately 192, 165, 138, and 138 μm^2, respectively, for the *M1*, *M2*, *M3* and *M4*, respectively. Hence, the differential capacitance at zero bias (C_{MAX}) was estimated to 25 fF. For the simplicity, the junction temperature is assumed to be equal in all mesas, and a non-linear thermal conductivity is neglected. The series resistance (R_S) is calculated as

$$R_s\left(T\right) = R_c + \underbrace{R_{active}\left(T\right) + R_{\mathrm{contact}}\left(T\right) + R_{\mathrm{spread}}\left(T\right)}_{R_{\mathrm{semiconductor}}}\ [\Omega] \quad (1)$$

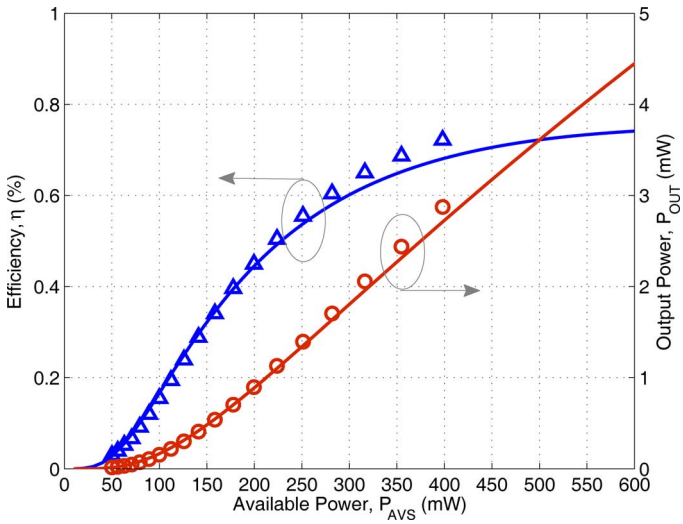

Fig. 8. Measured (symbols) and simulated (solid) conversion efficiency and output power at 474 GHz versus Available input power at 94.75 GHz.

where R_c is the contact resistance, R_{active} is the active layer resistance, R_{contact} is the contact layer resistance, and R_{spread} is the spreading resistance in the buffer. We neglect the frequency dependence through skin and proximity effects on the series resistance [36], [37]. As a rule of thumb, the temperature dependence can be approximated as [23]

$$R_s(T) = \underbrace{R_{s,T_0}}_{R_s \text{ at } T_0} \left(\underbrace{\frac{1}{4}}_{R_c} + \underbrace{\frac{3}{4}\frac{T}{T_0}}_{R_{\text{semiconductor}}} \right) \ [\Omega] \qquad (2)$$

where R_{s,T_0} is the parasitic series resistance at the ambient temperature ($T0 = 295$ K), and T is the elevated junction temperature due to the dissipated power. In this case, with rather low conversion efficiency, the dissipated power is almost equal to the absorbed RF power, P_{IN}. Hence, the junction temperature can be estimated as

$$T = T_0 + P_{IN} R_{\text{thermal}} \ [\text{K}] \qquad (3)$$

where R_{thermal} is the thermal resistance.

Based on reverse engineering, a good agreement between measured and simulated multiplier performance was achieved for R_{s,T_0} equal to 8.6 Ω, and an overall average R_{thermal} equal to 260 K/W, see Figs. 7 and 8 These values are in good agreement with analytical and numerical predictions.

The temperature distribution within the device, based on solving the heat equation using a 3D finite element method (Ansys mechanical), for a dissipated power of 250 mW is shown in Fig. 9. We assume a linear thermal conductivity (κ) for all materials. The heat source is located in the mesas volume, and the waveguide block is set to be at the ambient temperature. Due to the structure symmetry, only half of the geometry is simulated. Moreover, the thermal resistance between the bonded $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$/AlAs epi-layer and silicon substrate is assumed to be negligible. From Fig. 8 it

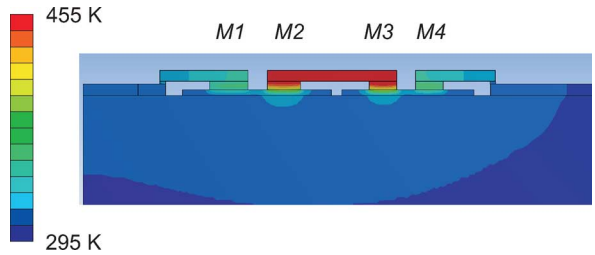

Fig. 9. Cross section of the structure showing temperature distribution in the device at 250 mW dissipated power. The ambient temperature is 295 K.

is clear that the overall temperature rise in active regions is very high with a large difference between inner and outer mesas, which are mainly due to a large thermal gradient in the $In_{0.53}Ga_{0.47}As$ material ($\kappa = 5\ \text{W} \cdot \text{m}^{-1}\text{K}^{-1}$). This indicates that the power handling capability and performance of this device is determined by the thermal rather than the electrical limitations (maximum voltage swing at 500 mW for this diode is ± 16 V). Rigorous analysis of the multi-mesa diode multiplier needs to include the effect of different junction temperatures and nonlinear material thermal conductivities, as introduced for multi-anode Schottky diode multipliers [38]. The poor thermal conductivity of ternary compounds ($In_{0.53}Ga_{0.47}As$) is a main limiting factor for lattice matched InP HBV diode multipliers and suggests further research on higher thermal conductivity materials such as GaAs or GaN based HBVs.

VI. Conclusion

We have demonstrated a silicon-integrated HBV-based frequency quintupler for 500 GHz. This device represents the highest reported frequency of operation for HBV-based frequency multipliers.

By integrating III–V compound semiconductor material structures onto a silicon substrate, with a predefined thickness using SOI wafers, one can benefit from the excellent mechanical properties of silicon such as robustness, and high precision of the final substrate thickness. The latter is absolutely crucial for achieving accurate control of the microstrip circuit. Moreover, the presented silicon platform can be used for advanced integration schemes and scaled to several THz.

Finally, the high power handling capability in combination with a high multiplication factor makes HBV quintuplers an attractive compact solution for terahertz signal generation. The high multiplication factor means that it can substitute two frequency doublers in cascade, or a doubler and a tripler in a LO chain, which makes it a competitive and cost effective solution. The development of solid-state power sources (several watts) at *W*-band frequencies (GaN technology) warrents further research on high power diode multipliers for terahertz frequencies

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