1.6 GHz Low-Power Cross-Correlator System Enabling Geostationary Earth Orbit Aperture Synthesis

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***Abstract*—We present a 64-channel cross-correlator system for space-borne synthetic aperture imaging. Two different types of ASICs were developed to fit into this system: An 8-channel comparator ASIC implemented in a 130 nm SiGe BiCMOS process technology performs A/D conversion, while a single 64-channel digital cross-correlator ASIC implemented in a 65 nm CMOS process performs the signal processing. The digital ASIC handles 2016 cross-correlations at up to 3.6 GS/s and has a power dissipation of only 0.13 mW/correlation/GHz at a supply voltage of 1 V. The comparator ASIC can handle sample rates of at least 4.5 GS/s with a power dissipation of 47 mW/channel or 1 GS/s with a power dissipation of 17 mW/channel. The assembled system consists of a single board measuring a mere 136×136 mm^2 and weighing only 135 g. The assembled system demonstrates crosstalk of 0.04% between neighboring channels and stability of 800 s. We provide ASIC and system-board measurement results that demonstrate that aperture synthesis can be a viable approach for Earth observation from a geostationary Earth orbit.**

***Index Terms*—Cross-correlator, comparator, interferometry, synthetic imaging, space application.**

I. Introduction

SATELLITE observation of the Earth's atmosphere has proven very significant for weather predictions and climate modeling. Today, most weather satellites operate in the infrared or visible light spectrum, which means that there is a lack of data on water vapor and temperature distributions in cloud formations into which such instruments cannot penetrate. Observations in the microwave range, on the other hand, can easily penetrate clouds, thus closing this gap in data availability.

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As compared to lower orbits, atmospheric observations carried out from a Geostationary Earth Orbit (GEO) give the advantage of decreased turn-around times and continuous coverage. However, since there is an inverse relationship between aperture and beam width, GEO measurements performed in the microwave region (especially near 50 GHz which allow for temperature sounding) would require very large apertures if performed using a parabolic reflector to scan the Earth's surface: The beam width angle and the distance to the object of observation together set the maximum resolution that can be achieved. For example, a 30 km resolution of the Earth when observed in the 50 GHz band from GEO would require an aperture of around 8 meters. Deploying such large antennas in space is an extremely challenging problem.

In the area of ground-based radio astronomy, *aperture synthesis* has long been used as a way to reduce sizes of antennas while attaining angular resolutions far beyond what any single real-aperture antenna could achieve. The aperture-synthesis approach uses an array of antennas distributed in a pattern and applies signal processing algorithms on the sampled signals. The longer distances between antennas—the baselines—determine the resolution of the image, while the shorter baselines determine the field of view. Hence, a large number of antennas in a well-defined array is required for a high performance and an evenly distributed sensitivity.

A large number of antennas in combination with a relatively high sampling frequency produces an immense amount of sampled data. Downlinking these uncompressed data to Earth would require digital bandwidths of hundreds of Gb/s. Applying cross-correlation, which is an integrating function, means that the amount of data can be reduced by a factor of several hundred thousand. Performing cross-correlation before downlinking the data to Earth is, thus, essential for making aperture synthesis in space a viable option.

We present a cross-correlator system which reconciles strict budgets on size, weight and component power dissipation with the need for high performance and many channels. Based on two types of ASICs, our cross-correlator system demonstrates that an aperture-synthesis approach can become a viable option for an Earth-observing microwave sounder in GEO. The ASICs have each been briefly reported previously [1], [2]; this article additionally provides a full system description and reports extensive chip- and system-level measurements which verify our approach.

II. Cross-Correlator Theory

Cross-correlation is a measurement of the similarity of two signals (f and g) at different time lags between them. The cross-correlation function is evaluated for f and g by multiplying and integrating the two for a time lag of t applied to one of them:

$$(f \star g)(t) = \int_{-\infty}^{\infty} f^*(\tau) g(\tau + t) d\tau. \tag{1}$$

An interferometer measures the interference pattern between antenna pairs (or baselines). In an XF type cross-correlator [3], the cross-correlations associated with these baselines are used to sample visibilities, $V(u, v)$, in the uv-plane which constitutes the spatial Fourier transform of the brightness temperatures, $T(x, y)$, in the image plane:

$$T(x, y) = \int \int V(u, v) e^{-2\pi i(ux+vy)} du dv. \tag{2}$$

In the digital domain, the cross-correlation function for a time lag of m is:

$$(f \star g)[m] = \frac{1}{N} \sum_{n=0}^{N-1} f[n] g[n + m]. \tag{3}$$

The main requirements of a cross-correlator system (as used in an interferometer) include; number of cross-correlations, bandwidth, dynamic range, stability and efficiency. The number of antenna elements required to achieve the resolution target mentioned in Section I is typically in the range of around 30 up to a few hundred, putting the number of cross-correlations in the order of tens of thousand. The required bandwidth is usually in the range of 0.5–2 GHz. The dynamic range depends on system operation and lies in the range of 30–45 dB depending on instrument topology and post processing. The stability requirement will depend on the required signal-to-noise ratio (SNR), and is in the order of a few seconds.

When implementing (3), some design choices become important: The analog signals have to be sampled and quantized, and the integration length has to be limited due to time constraints. The radiometer equation [4] gives the root-mean-square (RMS) noise, σ_T, of a simple, total power radiometer system: $\sigma_T = T_{\mathrm{sys}}/\sqrt{\tau B}$. Both integration time, τ, and RF bandwidth, B, can be increased to mitigate the effect of system noise temperature, T_{sys}, on the RMS noise and, hence, SNR. An increasing integration time will additionally have the effect of reduced data rate, although at the expense of temporal resolution. An increased bandwidth improves the SNR while requiring higher performance, resulting in an increased power dissipation in the digital correlator back end. Furthermore, signal bandwidth is not unlimited. In a typical XF cross-correlator system, a common clock for sampling and cross-correlation sets the upper limit not only for the signal bandwidth, but also for the base time unit in the cross-correlator. The time lags, m, are thus multiples of one clock cycle and the actual integration time is the integration steps, N, divided by clock frequency. The number of time lags and the bandwidth used determines spectral resolution and range.

Instead of achieving spectral resolution using time lags, a radiometer may be configured with filters, dividing the signal into sub-bands and process these in parallel (with a power penalty) or sequentially (with a penalty in temporal resolution). This solution will also help relaxing the performance requirements of any one cross-correlator, if the spectral range of interest is very wide, while incurring a penalty in SNR due to the bandwidth reduction. To further reduce power dissipation, the sub-band width may be narrower than each interval. For example, observations at 183 GHz of an 8 GHz band can be covered by four sub-bands, each narrower than 2 GHz. In such cases, the maximum bandwidth for the cross-correlator may be set by required spectral resolution. Additionally, for a digital cross-correlator, quantization will cause some amount of sensitivity degradation [5]. Naturally, all design choices affect system complexity and power dissipation.

The same cross-correlator, implementing the function of (3), can be used in both a real and a complex mode. In the complex mode, the mixer in the system front-end uses both 0 and 90 degree LO-phases (I and Q) for which four different cross-correlations are calculated: $I \star I, I \star Q, Q \star I$ and $Q \star Q$. This complex mode in effect doubles both bandwidth and spectral resolution, but each receiver element occupies double the number of cross-correlator input channels requiring close to four times the amount of logic for signal processing. The number of cross-correlations grows as $C(C-1)/2$, where C is the number of input channels.

III. Related Work

Correlators for ground-based astronomy are large systems. The Very Large Array in New Mexico, which was upgraded under the Expanded Very Large Array initiative [6], now consists of 8192 cross-correlator ASICs distributed across 128 boards and 16 racks (neglecting signal conditioning, digitizing, etc.). While ground-based correlators have few restrictions on power dissipation, weight or size, much stricter system budgets and constraints apply to applications in a space environment. While providing enough power is always a difficulty, the dissipation of the heat generated can prove an even greater challenge. In the vacuum environment of space all heat generated has to be transferred to the surface of the satellite and then radiated away. Minimizing power dissipation is critically important for heat management and, thus, instrument weight.

A 2D synthetic aperture radiometer for Earth observation—the Microwave Imaging Radiometer with Aperture Synthesis (MIRAS)—was launched in 2009 on the European Space Agency's (ESA) Soil Moisture and Ocean Salinity (SMOS) satellite [7]. Although it is the first such instrument to be launched into space, it was deployed in a low Earth orbit. It has 72 receivers observing in an RF band between 1400 and 1427 MHz. The intermediate frequency (IF) bandwidth is 27 MHz [8].

Two microwave-sounding instrument concepts involving aperture synthesis in GEO are currently being proposed; the Geostationary Atmospheric Sounder (GAS) [9] and the Geostationary Synthetic Thinned Array Radiometer (GeoSTAR) [10]. The microwave receivers of these instruments will be mounted in a three-arm, Y-shaped configuration, on foldable booms. Both instruments will monitor temperature and water vapor distributions in the Earth atmosphere.

Two prototypes have been developed under the GeoSTAR initiative. The GeoSTAR II prototype [11] succeeding GeoSTAR I [12] has three arms, each with 16 antenna elements where the previous had eight. The same cross-correlator was used for both prototypes. While designing the cross-correlator for GeoSTAR I, low cost was prioritized over low power, hence it is FPGA based. Furthermore, this GeoSTAR cross-correlator uses 8 bit A/D converters, due to product availability; the signals are then mapped to single-bit. This cross-correlator operates at a clock frequency of around 200 MHz.

For GAS, a first flight demonstrator has been discussed. This demonstrator would use 32–64 receiver elements per band at 50 and 183 GHz with IF bandwidths of 1 GHz, pushing the cross-correlator's performance and power requirements orders of magnitude further. Flight instruments of GAS and GeoSTAR, using in excess of 100 receiver elements/band, will further compound the demands. Both of these instruments can take advantage of the work presented here.

IV. System Architecture

A cross-correlator system essentially comprises A/D conversion and signal processing. We developed ASICs for A/D conversion [2] and cross-correlation [1] separately. While integration of both on a single die would have offered some advantages, there are good reasons for splitting sampling and cross-correlation into different ASICs. First, the need for channel isolation to avoid crosstalk from digital to analog is a major issue. With analog processing on a separate ASIC, isolation is much easier to achieve. Second, the use of separate ASICs allows for selecting independent process technologies for A/D and digital system portions. Third, including all comparator features on a single, 64-channel, die would make for a severely pad-limited design, unnecessarily increasing cost. Finally, developing two different ASICs is also a question of risk reduction and modularity, since other system configurations can be constructed out of these ASICs and any of them can be independently upgraded where and when required. Since the signal processing complexity grows with almost the square of the number of channels, whereas the A/D conversion complexity grows linearly, we can construct systems with double the number of input channels without needing to perform A/D conversion twice for all inputs, as opposed to the single die alternative.

The cross-correlator ASIC takes 64 one-bit single-ended inputs, performs cross-correlations, and supports data read out through a serial interface. The comparator ASICs perform one-bit A/D conversion for eight different channels. To enable system integration, added features include: 1) per-channel DC offset calibration, which reduces offsets in the cross-correlation results and makes it possible to reduce system power dissipation by lowering input swings to levels otherwise not detectable; 2) sample clock return, which simplifies system integration as the comparator ASIC has outputs matching the input configuration of the cross-correlator; 3) pins for controlling output drive strength and internal bias, which help to tune power/performance levels if required.

To demonstrate a complete system which can perform measurements within an interferometer, a 64-channel cross-correlator system has been assembled on a single board. Fig. 1 shows the system schematic. The target performance of this system is a 1 GHz sampling frequency; sampling a signal of 500 MHz bandwidth. The single-ended inputs, arriving from an IF system, are converted to differential signals using transformers and connect directly to the board's comparators. Comparator offset tuning is controlled by 4-channel, 256-step programmable potentiometers. Sample clock is supplied externally and split to the eight different comparator ASICs. The cross-correlator ASIC is single-ended and does not feature internal termination, thus, the outputs of the comparators are externally terminated and only one wire from each differential pair is connected to the correlator.

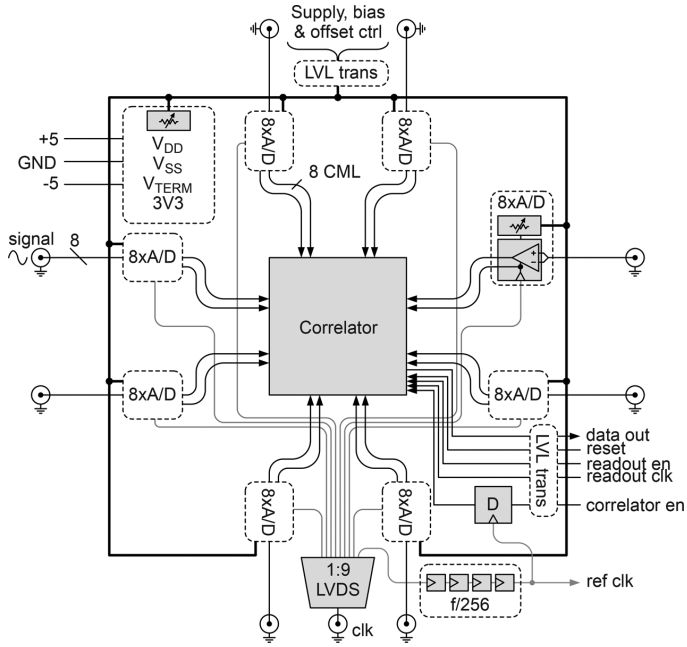


Fig. 1. System schematic.

The difference in fabrication process technology means that comparators and cross-correlators operate at different supply voltage levels. While this arrangement brings the advantage of tuning power/performance independently via voltage scaling, it requires level translation. To avoid extra circuitry, we use a power supply scheme where the comparator is negatively fed and the cross-correlator positively fed. The comparator ASIC uses current-mode logic (CML) output drivers that are terminated to a positive voltage, V_{TERM}, independent from the rest of the comparator supply. This voltage can be controlled in such a way that the comparator ASIC's output swing is centered around the cross-correlator ASIC's input threshold level. The 65 nm CMOS process used for the cross-correlator has nominal voltages rated at both 1 and 1.2 V, while the comparator is designed to operate with a supply in the range of -2.5 to -3.3 V.

The termination voltage, cross-correlator supply, comparator supply, and biases are all programmable through the same interface as the programmable potentiometers which set the input voltage offset. All potentiometers have non-volatile memories which means the programming interface can be disconnected once tuning has been performed. An additional, independent interface handles cross-correlation timing and data readout. To

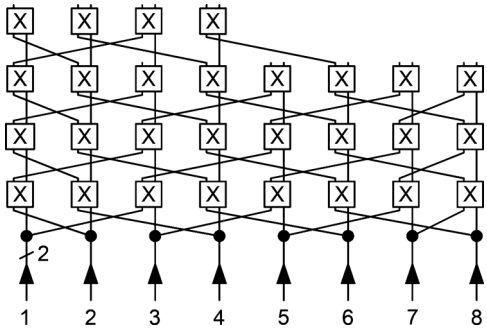


Fig. 2. Routing pattern of cross-correlator with eight inputs.

keep correlation timing within single cycle accuracy, the enable signal is latched by a reference clock generated by dividing the sampling clock by 256.

All signal paths, both before and after digitizing, are length matched to reduce signal time skew. Similarly all clock distribution after splitting (except the reference clock) is length matched to achieve simultaneous sampling of all signals. The fully populated board uses 8 metal layers, measures 136×136 mm^2, and weighs only 135 g.

V. Circuit Implementation

In the following, we will describe the detailed implementation of the two ASICs that constitute the core functionality of the cross-correlation system.

A. Cross-Correlator ASIC

The 64-input cross-correlator ASIC computes cross-correlations for all baselines (2016 in total). Single-bit products in the cross-correlations cause an overall SNR reduction of a factor of 0.64 compared with the infinite-precision case [5]. Since the targeted instruments do not require the extra spectral resolution offered by an increased number of lags, this ASIC does not feature any time lags (Section II).

The data-flow architecture routes every two-input combination to a cross-correlator cell, while maintaining the timing between clock and data that is key to high performance. The cross-correlator ASIC uses an architecture, shown in Fig. 2, in which each data signal is routed together with its own clock. Initially the data signal is split into two paths; using the convention of Fig. 2, one is going straight up and one is traveling sideways. At each cell, the clocks from the two incoming signals converge in a simple C-element and data are synchronized with the merged clock. Then, the clock is once again split into two and routed with the corresponding data to the next row above. The entire chip will, in the ideal case, operate as a row-wise synchronous, column-wise asynchronous circuit, giving the additional advantage of reducing current spikes and power supply noise.

Verification of the synchronization scheme described above was performed before manufacturing using Monte-Carlo simulation of a single two-input cross-correlator section including routing to the next one. For each simulation run, the timing from input to output was recorded. A mean of 175 ps and a standard deviation of 4.8 ps for a normal distribution were extracted. Additionally, RC-corner extraction was performed to find the metal wire delay standard deviation of 3.2 ps. These values combined made for a simple timing model of the block. Using MATLAB, we could then estimate the impact of the synchronization scheme on a full-scale ASIC, randomizing delays for every block throughout the circuit and comparing results with and without de-skew enabled. This approach also made it possible to examine what level of performance we could expect from ASICs with different number of inputs and draw conclusions on how the architecture scales. A similar cross-correlator, without the clock merging, would have its maximum time skews increased by a factor of 1.5 with every doubling of the number of inputs and, hence, a performance reduction on the same scale. The clock merging ensures that the maximum skew instead increases with a factor of less than 1.2 per doubling. At 64 inputs, the maximum time skew would be 2.4 times higher without clock merging than with clock merging.

Data inputs are arranged in groups of eight, where each group has a separate clock input. Each data group is routed together to one side of the cross-correlator, where the clock is split up to give each data its own clock. All group paths are length matched with respect to the other groups and along the way D-flip-flops limit timing skews between clocks and data.

Each cross-correlator cell (Fig. 3) consists of synchronization logic, a multiplier, an integrator, and readout logic. Since signals are single-bit, the multiplier is implemented as a dynamic 2-input XOR gate. The first six bits of the integrator consist of a prescaler with high-speed semi-static toggling flip-flops, whose values are not included in the readout. The remaining 24 bits are read out, making for a total integration depth of 30 bits. A select bit ripples through the ASIC, for each stop applying a new 24 bit value to a parallel MUX bus connecting to a read-out SPI.

Most transistors in the data flow core, up to the first flip-flop of the 24 bit integrator, are implemented using low-V_T high-speed transistors, while the remainder of the integrator (including readout logic) is implemented using high-V_T transistors. The complete cross-correlator ASIC consists of roughly 3 million transistors and has a size of 3 mm^2.

B. Comparator

Fig. 4 shows the 8-channel comparator ASIC that was designed specifically for the purpose of digitizing the signals in the cross-correlator system. Each input signal is amplified by two Gilbert gain cells [13] (Fig. 5) and then sampled by a D-flip-flop. The outputs are driven by CML drivers. Both calibration and signal inputs initially pass through emitter followers to move the input range to encompass the ground level, around which system input signals are centered.

Gilbert gain cells have the advantage of a very flat frequency response. Current amplification, A_I, is given by the relationship between outer (I_E) and inner (I_B) transistor pair currents: $A_I = 1 + I_E/I_B$. The 3-dB bandwidth is given by the current amplification and the transition frequency (f_T) of the transistors: $f_{3\,\mathrm{dB}} = f_T/A_I$. Thus, bandwidth has to be carefully balanced against amplification. In the implemented comparator, I_E and I_B are the same, giving a current gain of 2. The transition frequency of the transistors depends on the process technology's maximum f_T and the bias current. Conversion from

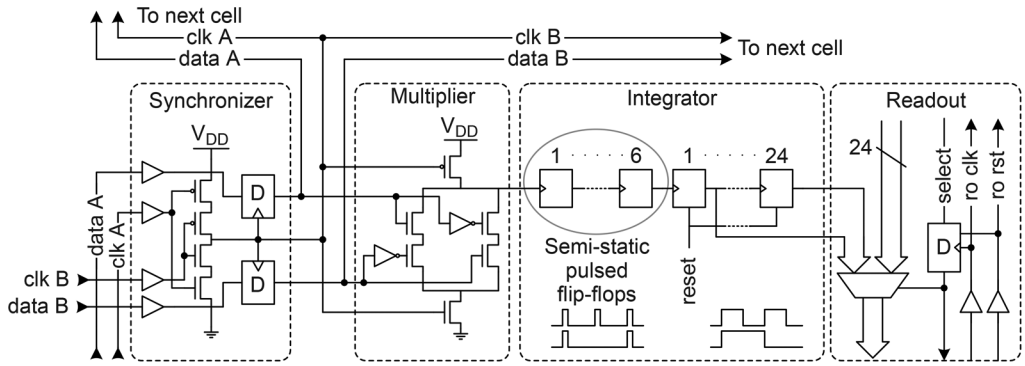


Fig. 3. 2-input cross-correlator cell schematic.

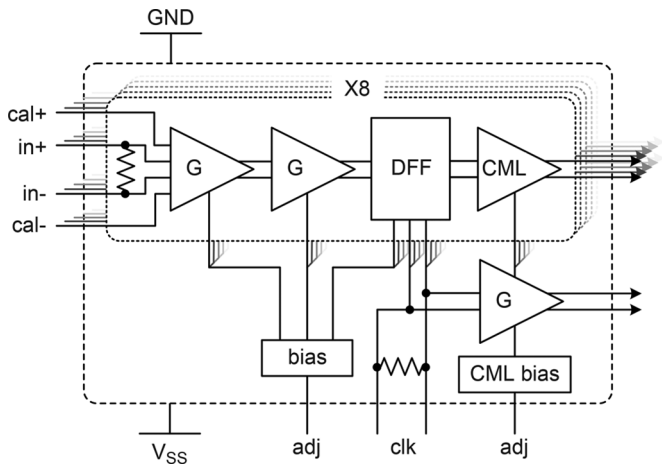


Fig. 4. Comparator schematic.

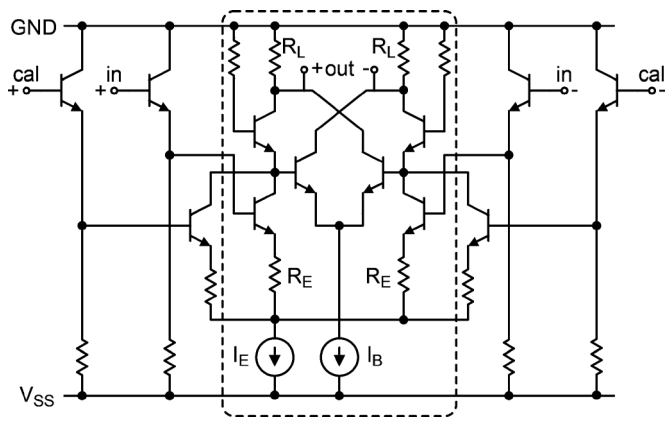


Fig. 5. Gilbert gain cell (inside marking) including offset calibration inputs and emitter followers (outside marking).

current amplification to voltage amplification is given as the relationship between load (R_L) and emitter (R_E) degeneration resistors: $A_v = A_I(R_L/R_E)$. The voltage output of the first Gilbert cell is coupled to the input of the next. Similarly to the cross-correlator ASIC and the system board, signal paths within the comparator, including clocks, are length matched to reduce timing skews. Common-centroid design practices are used throughout the circuit to minimize offset drifts caused by temperature gradients.

The comparator is implemented in a BiCMOS 130 nm SiGe process with a maximum f_T of 230 GHz. Apart from the high performance, there are several other advantages with this process. BiCMOS simplifies implementation of a high-precision low-power comparator since it offers good device matching [14]. Furthermore, the choice of a SiGe HBT process technology over a Si BJT is advantageous in space applications since it has a higher radiation tolerance. SiGe HBT shows lower current gain degradation due to neutron radiation [15], whereas both SiGe HBT and Si BJT show only minor degradations from ionizing radiation [16]. A previous test of almost identical Gilbert cell based mixer designs showed both lower power dissipation and better noise figure for an implementation in a bipolar SiGe process over a CMOS process [17].

VI. Results

Board and die photos of all implemented parts are shown in Fig. 6(a). The picture of the cross-correlator board (Fig. 6(a)) shows how the comparators are placed in a ring around the central cross-correlator ASIC. Along the edge, signal transformers and MMCX-contacts are mounted. All clock distribution and offset calibration are placed on the reverse side of the board.

Numerous tests were performed, on both ASICs separately and on the integrated system. When results differ between ASIC tests and system tests, the performance limitations lie in other system components on the board. Since the integrated system is designed with a 1 GHz clock rate goal and without specific restrictions on the power budget, other components were selected accordingly.

A. Cross-Correlator

For performance tests, the cross-correlator ASIC was rigged with fixed inputs, i.e., each input channel is tied to either low or high for the duration of the test, guaranteeing a predetermined output pattern of zero and full correlations. This way, any failing cross-correlator functionality is observed as a deviation from that pattern, which then serves as the pass/fail criterion. While this means the zero-counting cross-correlators are not fully tested, it still gives a good test coverage since the most performance-critical aspect—the clock distribution—has to be functional throughout the ASIC to pass the test. In terms of parameter ranges, supply voltage was varied between 0.8 and 1.4 V, while clock frequency was varied between 0.1 and 4 GHz, see Fig. 7. The semi-static prescaler flip-flops in the integrators limit the clock frequency downwards. At 1 V, the cross-correlator ASIC was operational between 0.3 and 2.7 GHz. For

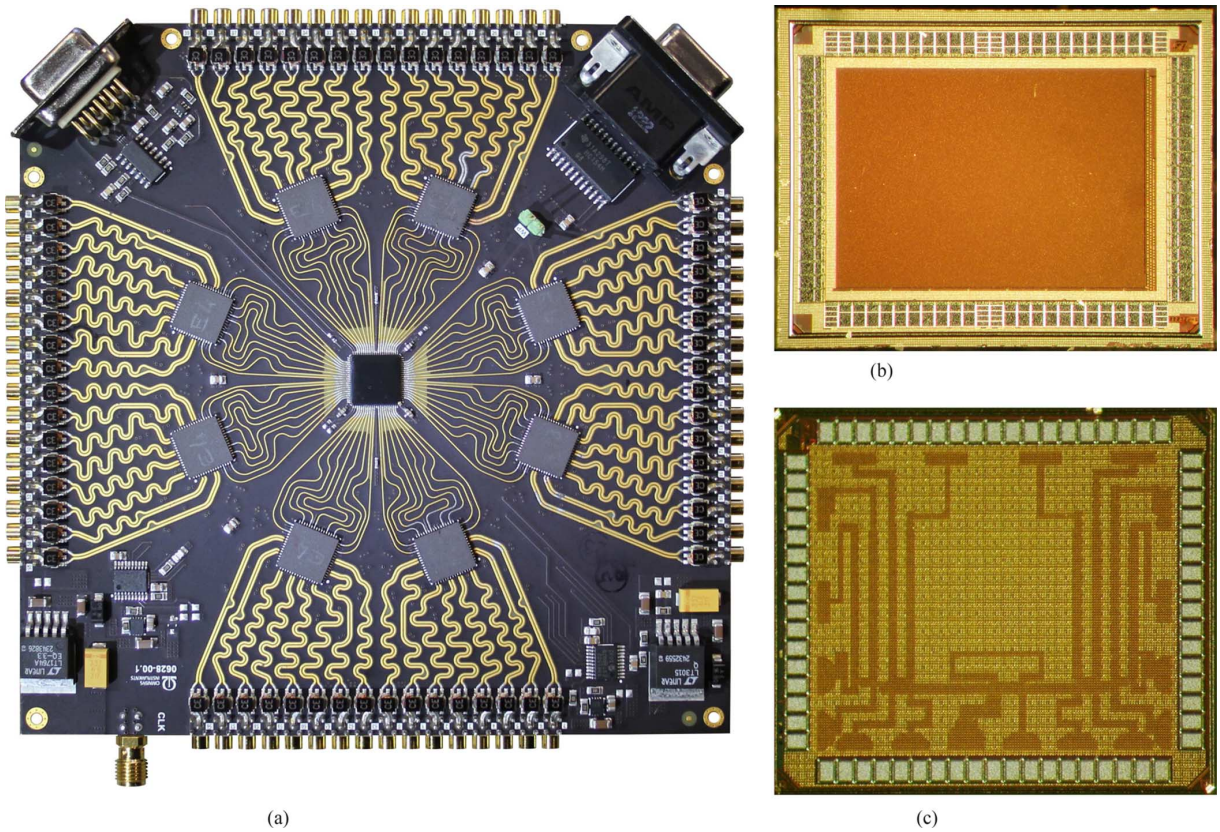


Fig. 6. Board and die photos. (a) Cross-correlator board. (b) Digital cross-correlator die. (c) Comparator die.

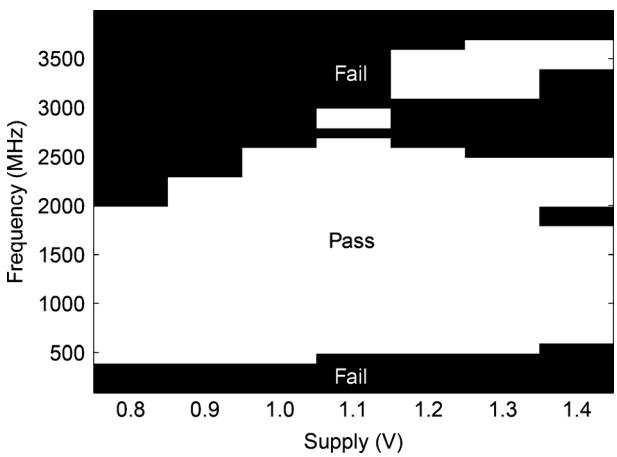


Fig. 7. Cross-correlator ASIC performance.

the higher supply voltage of 1.2 V, occasional errors occurred between 2.6 and 3.1 GHz, however the cross-correlator ASIC demonstrated functionality up to 3.6 GHz. Deteriorated clock signals found during high-frequency probing suggest that the board used for the standalone cross-correlator ASIC evaluation was the performance bottleneck.

To obtain high overall system performance, the system must handle not only internal clock skews but also external ones. It can be expected that for a skew of close to half a period, the cross-correlator will cease to function. Consequently, a test was carried out where half of the cross-correlator clock inputs were time delayed. Here, for a clock rate of 1 GHz, the cross-correlator ASIC stopped functioning for delays above 180 ps. Due to the way the ASIC is routed, this experiment tests the skew margin for only 64 of the 2016 individual C-elements. Because there are only eight external clock signals, however, only 448 C-elements are placed in locations sensitive to external skew.

Due to limitations in the separate cross-correlator ASIC test setup (toggling signals cannot be applied to all 64 inputs), the power dissipation values had to be derived from measurements for two cases: 1) All inputs were fixed. 2) Toggling inputs were applied to 16 of the 64 inputs. In the satellite application context, it can be expected that all inputs are randomly toggling, so this is the case we present. A power efficiency metric is given as mW/ch/GHz, where ch refers to output channels, that is, cross-correlation products. Results are listed in Table I. Also listed are figures for a previous generation FPGA-based cross-correlator with similar specifications [18] and the MIRAS Correlator and Control Unit (CCU) [8]. Our ASIC demonstrates orders of magnitude higher efficiency than both of these (0.13 as opposed to 7.5 or 60 mW/ch/GHz). The CCU unit does, however, also handle instrument control and data transmission, accounting for part of the power dissipation.

B. Cross-Correlator Radiation Test

Two cross-correlator ASICs were subjected to radiation tests to evaluate robustness in space environment. A range of different ion beams from a number of different angles were used, covering effective linear energy transfer (LET) levels from 0.106 MeVcm^2/mg (He at 0 degree angle of incidence) to 44.6 MeVcm^2/mg (Ag, 0 degrees). Higher incidence angles (θ) are usually used to increase effective LET as $1/\cos(\theta)$, based

TABLE I
CROSS-CORRELATOR POWER DISSIPATION MEASUREMENTS AND COMPARISONS

Measure	Power (W)	Efficiency (mW/ch/GHz)
1 V	0.53 (2 GHz)	0.13
1.2 V	0.80 (2 GHz)	0.2
Idle 1 V	0.04	
FPGA	5-10 (330 MHz)	7.5-15
MIRAS	34 (55.84 MHz)	60

on a longer path through the setup-sensitive volume. In our case no clear connection between single-event upset (SEU) rate and angle of incidence could be detected, indicating a failing of the inverse cosine assumption for small feature sizes [19].

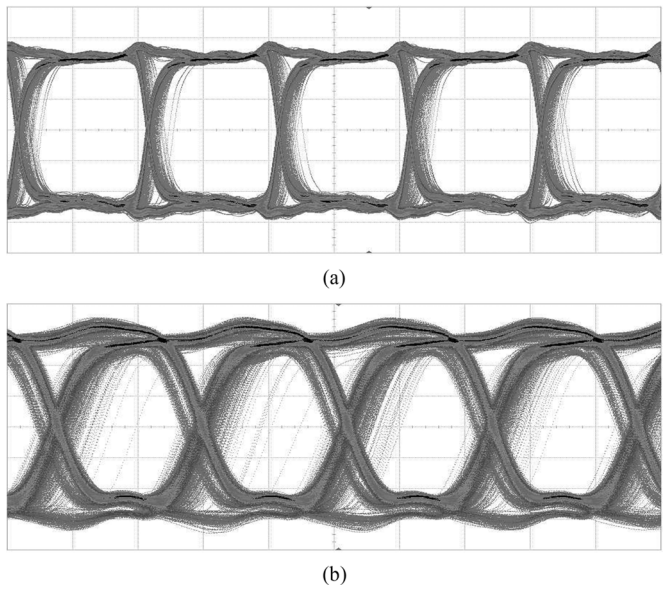
Testing was performed using the same method as for the functionality testing, that is, by applying a known input pattern and observing deviations from expected output values. Two types of failures were observed; single correlation value failures, caused by upsets in the integrators, and jumbled readout order, caused by upsets in the readout select registers or the readout counter. Identifying the two types of failures makes it possible to evaluate integrators and readout logic separately, evaluating probability of SEUs with different severity.

While radiation testing of structures such as memories is quite straightforward, testing integrators is a bit more tricky. A single strike may cause a chain reaction, flipping any number of more significant bits within the integrator, depending on the current state. Differentiating this from multiple strikes in the same integrator may not always be possible. Thus the number of SEUs measured may differ slightly from actual number of SEUs suffered. To get an accurate measurement of the SEU rate, a method based on counting number of clusters with erroneous bits was used rather than just comparing correlation values. Cross-section data for every level of LET was calculated as the number of SEUs divided by effective particle fluence, which is the number of ions per cm^2. The cross-section data was entered into ESA's Space Environment Information System [20] (SPENVIS) to assess the corresponding SEU rate in GEO. Galactic cosmic ray fluxes were based on CREME96 [21], and the SEU rate was calculated for a one-year mission average.

An enclosure thickness of 5 mm would provide good structural stability and thermal conductivity. With such a casing, the mission-average SEU rate would come to $15 \cdot 10^{-3}$ SEU/day/ASIC for integrators and $0.3 \cdot 10^{-3}$ SEU/day/ASIC for readout logic. The two cross-correlator ASICs were subjected to a total ionizing dose (TID) of 69 and 102 krad, respectively, without any noticeable performance degradation. With the same amount of protection, a ten-year mission in GEO corresponds to a TID of roughly 60 krad in an exposed environment and down to an order of magnitude lower when surrounding objects and placement within the satellite is accounted for [22]. The 65 nm process technology used is expected to provide a relatively high TID tolerance [23].

C. Comparator

The comparator ASIC was evaluated in a temperature-controlled environment. The tests were performed on both a naked die mounted to an RF-PCB and a QFN-packaged chip mounted on a similar board. Both showed very similar performance. Utilizing the bias and supply voltage scaling capability, two modes, that is, low power (LP) and high performance (HP), were tested. The LP mode was tuned for a 1 GHz sample clock requirement driving a 200 mV output swing over 100 Ω termination, while the HP mode was tuned for the same output swing and maximum performance where transistors are biased such that their f_T lies close to maximum for the BiCMOS process.



(a)

(b)

Fig. 8. Eye diagrams of comparator data output. (a) LP mode at 1 GHz sampling frequency. (b) HP mode at 4.5 GHz sampling frequency.

Eye diagrams for sampling of an 80 $\mathrm{mV_{p\text{-}p}}$ signal at each of the two modes are shown in Fig. 8. The LP mode (Fig. 8(a)) diagram is based on a sampling clock of 1 GHz (performance target) and a single-ended CW of 325 MHz as input signal (with the other terminal tied to ground). The HP mode diagram is based on a sample clock of 4.5 GHz and an input signal of 1.5 GHz. Since the sample clock and the input signal were not phase locked, some of the samples occur very close to the CW zero transition, prolonging the time of metastability. This is visible as stray traces through the center of the eye diagrams in Fig. 8(b).

The input offset voltages were measured for a few of the inputs. As expected from the Monte-Carlo simulations performed before tapeout, all these voltages stayed within 10 mV. The temperature-dependent input offset drift was also tested at eleven different temperatures between 0 and 50 °C, as shown in Fig. 9. The total offset variation was below 0.2 mV, while the overall temperature drift (using a linear approximation) was less than 2 μV/°C.

An analysis on the noise-induced jitter was performed by applying a large scale low-frequency (100 kHz) common-mode (CM) signal on the signal input (Fig. 10(a)), clock input (Fig. 10(b)) and power supply (Fig. 10(c)). Noticeable CM-induced jitter is seen only for LP mode where CM power is significantly above differential input power.

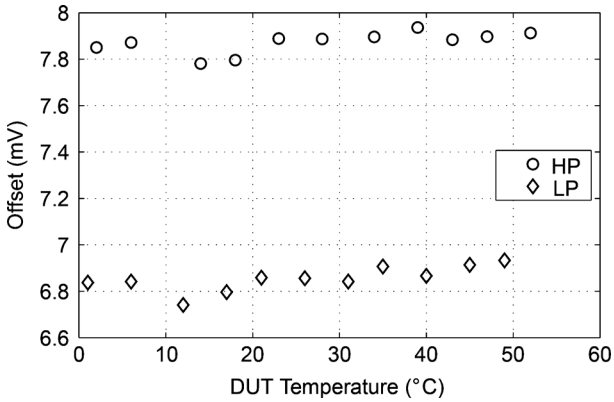


Fig. 9. Temperature offset drift.

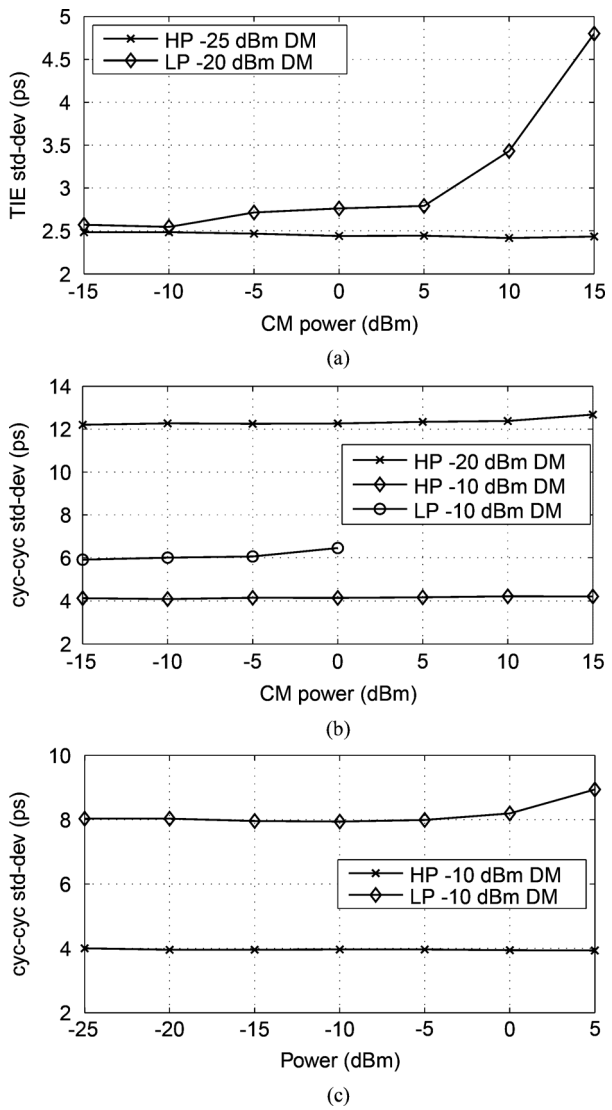


Fig. 10. Jitter analysis. (a) Input CM induced jitter measured as standard deviation of the time interval error (TIE) on the data output. (b) Clock CM induced jitter measured as standard deviation of the cycle-to-cycle jitter on the clock output. LP mode starts failing above 0 dBm CM power. (c) Power supply induced jitter measured as standard deviation of the cycle-to-cycle jitter on the clock output.

The power dissipation for the comparator ASIC was measured against the ground line, which serves as the positive supply. The CML drivers are terminated to 0.6 V. Results are listed in Table II.

TABLE II
COMPARATOR POWER DISSIPATION MEASUREMENTS

Mode	Current (mA)	Power (mW)	Efficiency (mW/ch)
LP	31	78	10
HP	93	307	38
LP w CML	49	133	17
HP w CML	111	377	47

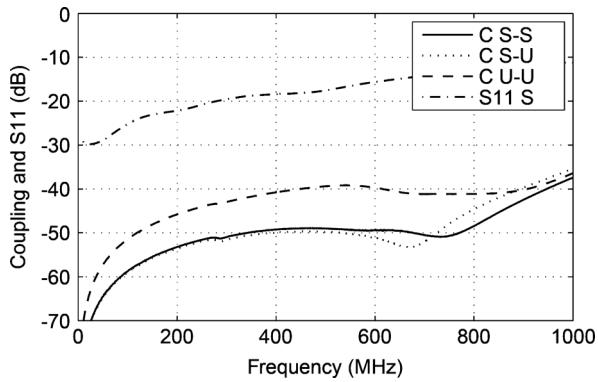


Fig. 11. Coupling (C) between two neighboring channels with both shielded transformers (S-S), with one of them unshielded (S-U), no shielding (U-U) and S11 of one shielded channel.

D. Cross-Correlator System

Crosstalk between channels is a major concern in a cross-correlator system. Crosstalk was measured using two uncorrelated noise sources connected to different input channels. Due to the circuit implementation, where multiplication is performed by an XOR gate, it can be expected that cross-correlation of inputs connected to same source gives values close to 0, while cross-correlation between different sources is close to 50% of full count. The results were then converted to a scale, where 100% equals full correlation and 0% equals no correlation. Most of the crosstalk on the cross-correlator board was found to be occurring between input transformers as these are mounted side-by-side. Shielding of the transformers make measured correlation between neighboring different-source input channels drop from 0.09% to 0.04%. Correlation between same-source channels was consistently above 96%. Variations between inputs on both board and test setup as well as timing variations account for the non-ideal correlation.

Fig. 11 shows the result of S-parameter measurements. Channel-to-channel coupling is measured as an S21 parameter between input ends of two neighboring channels; while not exactly capturing crosstalk coupling, the measurement strategy gives a good indication of it. The measurements revealed that for the operating range of 10–500 MHz, adding transformer shielding to one channel makes this coupling drop with 8 dB which further supports the above drop in correlation. Shielding the second channel only has an effect for frequencies above 500 MHz. S11 stays below -20 dB for the inputs with transformer shielding.

An Allan variance [24] test, Fig. 12, shows that for 25 cross-correlation channels, a stability of up to 800 s is achieved. As the integration time required for a cross-correlation system is on the order of a few seconds, this gives the system a good stability margin.

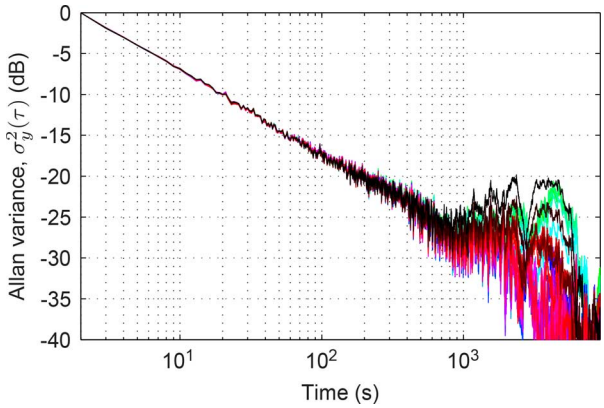


Fig. 12. Allan variance for 25 cross-correlator channels.

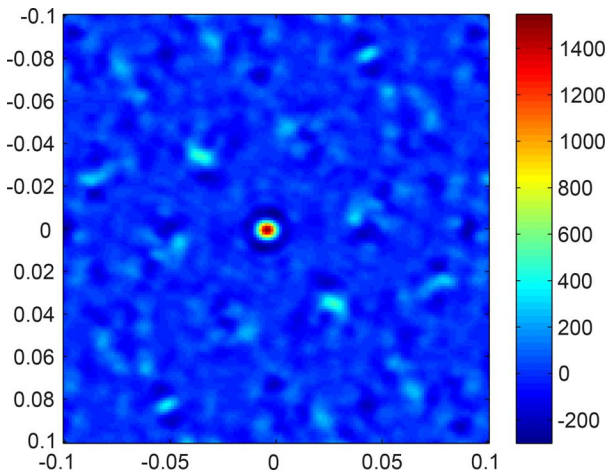


Fig. 13. Measured image of the sun (central dot). The scale is in Kelvin, while the X and Y axes are in radians.

The power dissipation of the cross-correlator system is heavily dependent on bias and voltage scaling. For the high-performance mode, as used in the crosstalk measurements, the board showed a power consumption of 19 W, of which a significant proportion was dissipated by linear regulators. Since the assembled board, as a demonstrator of the comparator and cross-correlator ASIC capabilities, was optimized for performance rather than power, the system's total power dissipation can be significantly reduced by making different component choices. The maximum clock frequency for the board was measured to 1.6 GHz, limited by the clock splitter rated at 1.5 GHz.

Fig. 13 shows the result of solar imaging using the cross-correlator board connected to the GeoSTAR II prototype described in Section III, replacing the previous cross-correlator. The observation frequency is 165 GHz. The interferometer instrument is presently under development and is only partially populated, with 30 out of a designed 48 receivers. Thus, this array is missing numerous interferometer baselines, which leads to the irregular point-spread function evident in Fig. 13. This point-spread function matches the predicted response—given the missing samples—to within 2% of the expected magnitude. Furthermore, comparison observation performed with the old prototype cross-correlator also exhibits a good match at the 2% level.

VII. Conclusion

We have designed a cross-correlator system, including two custom-made ASICs, and tested these for power dissipation, performance, and analog characteristics. Additionally, radiation test results for the digital core have been presented. Our prototype clearly demonstrates the feasibility of the synthetic aperture approach, where cross-correlation has been considered the most challenging problem to resolve. We have demonstrated a cross-correlator orders of magnitude lighter and more power efficient than what has previously been launched such as the 11.2 kg MIRAS CCU (which does not include A/D conversion). Adding a 5 mm thick aluminum casing around the cross-correlator board, as suggested in Section VI-B, would make for a mass of this system of around 0.7 kg.

The advances presented here affect the design focus for future space-borne cross-correlator systems. As long as power dissipation, mass and size can be reduced enough to make an aperture synthesis instrument feasible, other performance metrics of the system will gain precedence. For example, some penalty in power, size, and mass due to using A/D conversion on separate ASICs may be justified by gains in other metrics, such as crosstalk isolation.

Our choice of single-bit resolution during correlation is key to our achieved performance per power and per weight. A still-modest two-bit, three-level, quantization would increase sensitivity degradation from 0.64 to 0.81 [5] but also cause the number of pads and cross-correlator logic area to double. Two-bit signals would also introduce A/D converter linearity issues. Some of the lost SNR can be regained by oversampling, using the available performance overhead with a corresponding reduction of the maximum on-chip integration time, avoiding the need for extra logic and input pads. Power dissipation will, however, increase with clock frequency.

The 30 bit correlator counters let us use integration times of up to one second at 1 GHz. Where further integration time is required (such as for GAS), this can instead be performed outside the cross-correlator ASIC. Integration time and bandwidth is typically set by end user requirements based on temporal and spectral resolutions, respectively.

Future flight instruments will require many more channels. This will increase power dissipation, size and mass of the cross-correlator system. Several cross-correlator ASICs and/or increasing number of channels per ASIC will be required as well as more A/D converters and supporting electronics. The performance/power figures demonstrated in our design study show that the concept of a GEO-based interferometer for Earth observation is now a viability.

Acknowledgment

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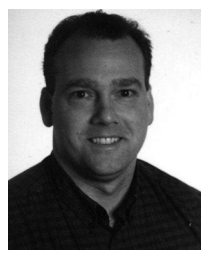

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