THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Design of High Linearity MMIC Power Amplifiers for Space Applications

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Abstract

The high linearity performance in satellite transmitters is receiving increasing attention due to the demands of higher data rates in satellite communication links. During the last decade, digital communication links in satellite system have been replacing the previous analog links increasing the channel efficiency by allocating multiple carriers in the transponder bandwidth. However, multicarrier transponders require high linearity performance in the transmitter. In addition, a highly reliable operation is required for space applications to ensure a lifetime that typically exceeds 15 years. This is achieved by avoiding stress to the device, operating it far below the process maximum ratings and keeping the junction temperature under control.

This thesis presents the design strategy for GaAs pHEMT MMIC high linear power amplifiers intended for multicarrier operation at C and extended C-band. An investigation in junction temperature prediction methods is provided and applied during the amplifier design. A careful device selection method is described with the target to fulfill the electrical and reliability requirements. The circuit design is focused on high linearity. A non-linear transistor model accurately predicts harmonic generation and intermodulation products. This allows optimization of the bias point and output load for high linearity. The amplifiers have been characterized in terms of S-parameters, single tone output power and two tone output power. In addition, infrared temperature measurements have been performed at transistor and chip level.

The circuits are fabricated in a 250nm GaAs pHEMT technology having a cut-off frequency of 45 GHz. A maximum OIP3 of 41.7 dB at 4.5 GHz was measured and gain above 28 dB was observed in an octave band between 3 and 6 GHz. The measured 1dB compression point is 26.7 dBm. The power consumption is less than 2.5 W and measured junction temperature is 112 °C.

Keywords Power amplifier, GaAs, pHEMT, C-Band, non-linear modeling, Junction temperature, reliability, Infrared measurements

List of Publications

Appended papers

The thesis is based on the following papers.

[A] O. Silva, I. Angelov, H. Zirath, and N. Rorsman, "High linearity MMIC power amplifier design with controlled junction temperature," in *Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), 2014 International Workshop on*, 2014, pp. 1-3.

[B] O. Silva, I. Angelov and H. Zirath "Octave band linear MMIC power amplifier with +40dBm OIP3 for high reliability space applications", Submitted to *IEEE Transactions on Microwave Theory and Techniques,* October 2014.

Abbreviations

8PSK	Eight phase shift keying
BPSK	Binary phase shift keying
CAD	Computer aided design
DoD	Department of defense (U.S.A)
DUT	Device under test
EM	Electromagnetic
GaAs	Gallium arsenide
GaN	Gallium nitride
GEO	Geosynchronous Earth orbit
GPS	Global positioning system
GLONASS	Global navigation satellite system
HEO	High Earth orbit
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
IF	Intermediate frequency
IR	Infrared
ISS	International space station
LEO	Low Earth orbit
LNA	Low noise amplifier
MEO	Medium Earth orbit
MMIC	Monolithic microwave integrated circuit
MoM	Method of moments
PA	Power amplifier
QPSK	Quadrature phase shift keying
RF	Radio frequency
SiGe	Silicon germanium
TTC&M	Tracking, telemetry command & monitoring
TWTA	Traveling wave tube amplifier

Contents

Chapter 1

Introduction

1.1 Motivation

High linearity performance is essential to push the capabilities of modulation and transponders channels efficiency in order to achieve higher data rates in communication links. The space environment, in addition, set tough requirements for devices on board. It is critical to guarantee a long life and high reliability design. This is achieved by avoiding stress to the device, operating it far below the process maximum ratings. In the recent years, Monolithic Microwave Integrated Circuits (MMICs) have found their way into the space applications looking for reduction of size and mass, and improved reliability and reproducibility. The junction temperature of the active component is the main contributor to the wearing and failures and its control is a requirement to achieve high reliability [1]. High linearity of the transmitter is the main parameter to be improved in order to transmit data in multicarrier operation and use complex modulation techniques.

1.2 Satellite communications overview

Satellite communications were described first time in October 1945 when Arthur C. Clarke published a paper titled: *Can rocket stations give world-wide radio coverage?* [2]. Later in 1957, the Sputink 1 was launched by the former Soviet Union representing the starting point of satellite communications [3]. During the decade of the 1960's a rapid development of space technology was driven by a global demand on communications along with political considerations.

Subsequent developments in electronics and space science boosted the growth of satellites for communication, different constellation orbits, and geosynchronous satellites. Finally, the satellite system Intelsat III was established in 1969 with a constellation covering the entire globe but the Polar Regions. Since then, an increasing demand on telecommunications evolved from telephone to television and

internet traffic. Along with it, the satellite communication industry has grown giving place to spacecraft operators lead by Intelsat Ltd. and SES S.A., and navigation systems as GPS in the United States, GLONASS in Russia and most recently GALILEO in Europe.

Typically, a satellite has one or many on-board transponders consisting of a receiver, an IF processor and a transmitter. In a single transponder satellite link, the signal goes through the receiver antenna, the low noise amplifier (LNA), a down-converter mixer, the demultiplexers, intermediate frequencies (IF) amplifiers, up-converting mixers, high power amplifiers (PA), multiplexers and the transmitter antenna (Figure 1). Local oscillators and power supplies are also needed for the transponder operation.

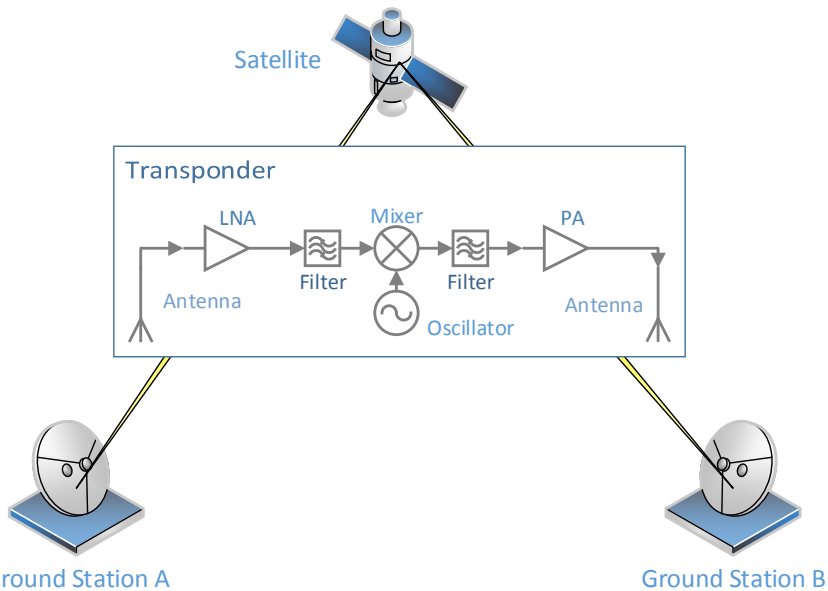

Figure 1. Simplified single conversion transponder satellite system.

An additional payload unit consists of the Telemetry, Tracking, Command and Monitoring (TTC&M) equipment. This system is the interface between the satellite and the base station for supervision and maintenance of the spacecraft and is vital for the operation of the satellite, if it does not work properly it will directly imply a failed mission [4]. The telecommand signals use a dedicated transponder during the launch and early stages of operation. After the satellite starts operation, these signals are allocated within the communications bands using a transponder system such as described before.

The growth in the space industry has also motivated a higher demand on the specifications for electronic circuits. Each of the blocks conforming the communications payload of the satellite consist of different circuits that should fulfill the electric and reliability requirements. MMICs have shown to be a good technology for these specific applications. However, the thermal behavior of MMIC devices is critical as the reliability decreases with increasing junction temperature [5]. Some of the frequency bands used for satellite systems are located in the L, S, V and Q bands. Still, the most used bands are in the C-band (4 – 6 GHz), K_u-band (12 – 14 GHz) and K_a-band (20 – 30 GHz) where the MMIC technology has been replacing traveling wave tube amplifiers (TWTAs). However, for high power levels, TWTAs are still used because it is difficult to generate such power level in semiconductor technologies with the required linearity specification.

More complex modulation methods are desired to increase the data capacity of the channels. Often the 8-Phase Shift Keyed (8PSK), Quadrature Phase Shift Keyed (QPSK) or even a Bi-Phase Shift Keyed (BPSK) modulation is used. More complex schemes of modulation are not used since the high level of attenuation in the atmosphere makes it difficult to demodulate the signal with high accuracy. The composite signal formed by adding different carries has a variable amplitude resulting in generation of intermodulation products and channel efficiency reduction. With the change towards digital communication in satellites, even the analog TV broadcasting that was earlier transmitted in C-band, is being replaced by digital signals at Ku-Band for new services such as high definition TV [6]. This development increases the need to improve the channel efficiency of satellite links.

1.3 Thesis contribution and outline

This thesis presents design considerations for reliable linear amplifiers integrating three strategies:

1. Junction temperature prediction
2. Device modeling
3. Circuit design.

An insight into these areas is given and the design technique is described and demonstrated in two GaAs C-Band power amplifiers.

In chapter 2, the effects of the space environment will be described and how it affects the operation and reliability of the devices. Methods for accurate prediction of junction temperature are explained together with techniques for infrared

temperature measurements. Chapter 3 describes the sources of non-linearities in the active devices and the modelling approach for highly linear circuits. In chapter 4, the design of power amplifiers is explained in detailed. Finally, conclusions and future work are outlined in the chapter 5.

Chapter 2

Space and Reliability

2.1 Space Environment

Most of satellites are placed into orbits about 400km above the earth. The height of the orbit is defined by the physics governing celestial mechanics. The mass of the satellite determines the speed at which it should travel to keep a constant height. The centrifugal force is in opposite direction to the force due to the gravitational attraction, the equilibrium between those two forces leads to a stable orbit. Different orbital heights exist, the geostationary orbit (GEO) is located at 35,786 km above the earth's equator. Above GEO, the orbits are called high earth orbits (HEO). Below GEO, the medium earth orbits (MEO) are placed between 2,000 km to 35,786 km. Under 2,000 km down to 160 km are named low earth orbit (LEO). The majority of artificial satellites are locate in the range of the LEO orbits, included the International Space Station (ISS) that orbits at around 420 km with an average speed of 7,7 km/s [6]. The environment where the satellites operate is characterized by a total vacuum and high sun radiation where there are constant risks of malfunctions or accidents. The extreme temperature changes when a direct sight of sun or when it is shadowed are considered in the spacecraft design. The electronic circuits cannot operate at such wide range of temperatures, and thermal controls keep the electronic circuits within an acceptable margin.

The signal sent from or to the satellites travels through the atmosphere. Many phenomena can affect the signals and possibly result in loss of data. From these phenomena the rain attenuation is the main contributor. Rain causes significant attenuation, especially in the microwave and millimeter frequencies. At 10 GHz the attenuation caused by heavy rain is about 2 dB meanwhile at Ka-bands it increases to 5 dB.

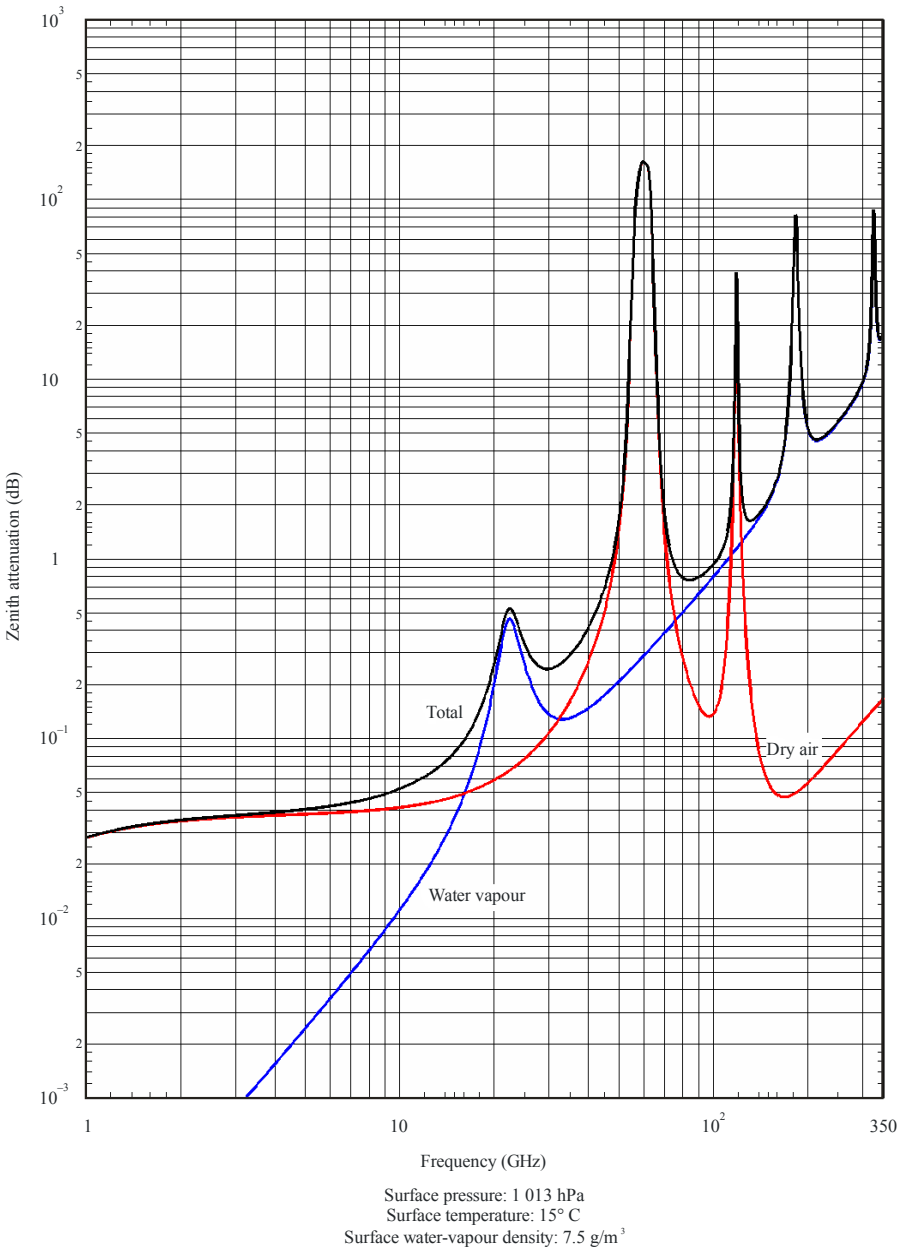

Figure 2. Total, dry and water vapor zenith attenuation from sea level. From Figure 6 of [7], reproduced with permission. The curves represents the attenuation due to oxygen, water molecules and the sum of both cases with the characteristics of pressure, temperature and density defined under the graphic.

The signals are also attenuated by interaction with molecules in the atmosphere proportionally to the square of the distance travelled. At specific frequencies, resonant absorption increases the attenuation producing peaks on the zenith path. The oxygen molecules in the air create resonant absorption peaks around 60 GHz and 118.75 GHz while the water vapor molecules create peaks at 22.24, 183.3 and 325.2 GHz (figure 2). The K-bands have been allocated to avoid the first water vapor peak giving the index *under* and *above* to the K_u and K_a bands respectively. The 60 GHz band is suitable for inter-satellite links where the atmosphere provides a screen against the terrestrial systems interferences.

The space qualification tests are made to understand the failure mechanisms and determine the reliability of MMICs. GaAs MMICs have been widely used in space industry, a general guideline for space qualification was set by NASA, JPL and the DoD [8]. The primary failure of GaAs MMICs occurs when the metals deposited in the ohmic contacts diffuses into the substrate, and the Ga or the As diffuses to the metal. This is caused mainly due to thermal stress.

Space qualification includes mechanical tests where high vibrations and g-forces experienced during the launch are simulated. Under this test mechanical fixtures as wire-bonds, mechanical joints and packages are stressed. In addition, all the electronic components are DC and RF tested under vacuum at a wide temperature and bias ranges to verify its functionality.

2.2 Reliability Considerations

In satellite communication systems, reliability is a critical consideration in the design. Once the satellite is launched, there is very little possibility to carry out reparations. Failures should be avoided and backup systems are often implemented. Normally, the life time of a satellite system should be over 15 years under the harsh space environment. The satellite manufacturers need to provide a product lifetime expectancy to their customers and insurance companies. The reliability calculations aim to determine the probability of functionality after a defined time period.

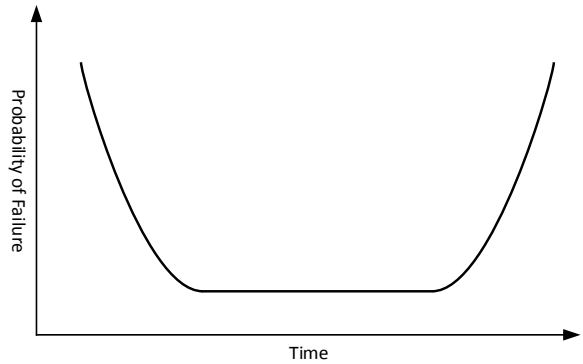

Figure 3. Bathtub curve. Probability of failure against time

The reliability of a component is characterized by the "bathtub" curve (Figure 3). At the beginning of the lifetime, there is a high rate of failure due to defects in the fabrication or the materials. After this period, a lower and stable failure rate will remain until failures start to be more common due to ageing.

The initial period where the probability of failure is high is eliminated in a "burn-in" period. Failures in the device are induced with high temperatures and overrated voltage conditions for 100 to 1000 hours. In this way the remaining devices will start operation in the satellites in the lower part of the bathtub.

The reliability of a device is defined as the ratio between the number of survivors (N_s) at a given time (t) and the number of devices at the beginning of the test (N_0):

$$R(t) = \frac{N_s(t)}{N_0} \tag{2.1}$$

The probability of any of the devices to fail will therefore be defined as the average of the failure rate. The failure rate is the inverse of the average reliability or mean time to failure MTTF:

$$MTTF = \frac{1}{N_0}\sum_{i=1}^{N_0} t_i \tag{2.2}$$

Where t_i is the time of failure of the *i*th device tested. The failure rate is defined as:

$$\lambda = \frac{1}{MTTF} = \frac{1}{N_s}\frac{dN_f}{dt} \tag{2.3}$$

Where N_f is the number of devices that failed after the time t. Using equation 2.1 in 2.3 gives:

$$\lambda = -\frac{1}{N_0 R}\frac{d}{dt}(N_0 R) = -\frac{1}{R}\frac{dR}{dt} \tag{2.4}$$

The equation 2.4 can be solved for $R(t)$:

$$R(t) = e^{-\lambda t}$$

Thus the reliability depends exponentially on the MTTF and decreases with time following the bathtub curve [6].

High temperature stress tests are commonly used to measure reliability. A failure criteria is defined for the transistors. For instance, a specific change of the output power or gain, or a change in the drain or collector current. The plot of failures describes a lognormal distribution (figure 4).

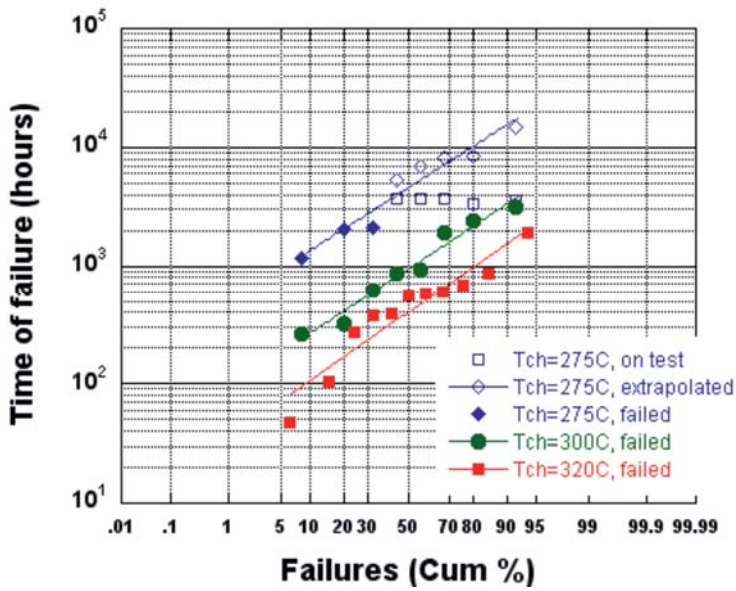

Figure 4. Failure time for three temperature levels on a GaAs pHEMT at X-band. Copyright ©IEEE Reprinted with permission from [9]

This is repeated for different temperatures until 50% of the samples fail. At each temperature, the MTTF is calculated and it is extrapolated to the range of temperatures where the device will be used. The extrapolated MTTF is plotted in a logarithmic scale against temperature following the shape of the Arrhenius plot

(figure 5). The slope of the curve corresponds to the activation energy E_a of the dominant mechanism of failure and it represents a measure of how effectively a mechanism utilizes thermal energy [1].

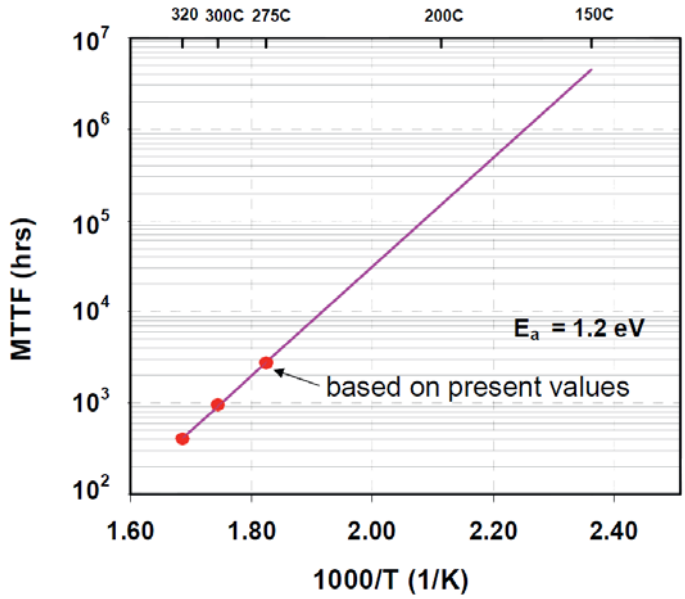

Figure 5. Arrhenius MTTF extrapolation based on 3 temperature levels. Copyright ©IEEE Reprinted with permission from [9].

The methods described here give indications of which devices are critical in the lifetime expectancy on a system. In satellite communications redundancy is a strategy to avoid a system level failure using more devices. The design should provide backup units that give an alternative path to the signal in case of a failure without affecting the normal operation. This is commonly seen in amplifiers used in transponders as these are known to have limited lifetime. Parallel units are added and the signal is divided between them under normal operation, but in case of a failure any of the branches will be able to support the normal operation of the system.

2.3 Junction Temperature Prediction

With the important effect that the junction temperature has on reliability, there is a big interest in its accurate prediction. Different approaches have been proposed for thermal modeling of the devices applying analytical solution or numerical methods

as finite difference, finite element or boundary element. In general, all the used methods involve approximations in terms of material properties and device geometry. Isothermal and adiabatic surfaces are assumed in order to reduce the complexity of the calculations. From these techniques, the boundary element method is well suited for accurate prediction of the MMIC junction temperature [10-12]. Another approach uses specialized thermodynamic software as ANSYS, Abaqus or Harvard TAS to simulate the thermal behavior of the structure [13]. These methods require a high amount of calculations and many times knowledge that is out of the scope of the MMIC designer. In addition, the actual operating temperature, will depend on thermal resistances in the practical mounting condition. For this reason practical ways for predicting the junction temperature are desired in MMIC design.

One methods is using Fukui curves [14]. These curves show the thermal resistance as a function of the channel temperature with the back plate temperature as parameter. Using empirical results based on the change of gate voltage and drain currents due to temperature changes, an expression for the absolute thermal resistance is found as function of the transistor geometry:

$$\theta = {T_{ch}}^{0.87} \frac{z^{0.25}}{4z} \left(\frac{t}{d}\right)^{0.4} log\left(\frac{1.7\,t}{L}\right) \tag{2.5}$$

Where z is the total gate width, L the gate length, t the thickness and T_{ch} the channel temperature calculated from the electrical response FET.

A set of Fukui curves can be created for a specific process after measure the channel (figure 6). The thermal resistance R_{TH} is given for a 1 mm gate width, so to calculate the junction temperature the following equation is applied:

$$T_{ch} = T_o + R_{TH}\left(\frac{1000}{n*W_g}\right) P_{diss} \tag{2.6}$$

Where T_o is the back plate temperature, n the number of fingers and W_g the unit gate width.

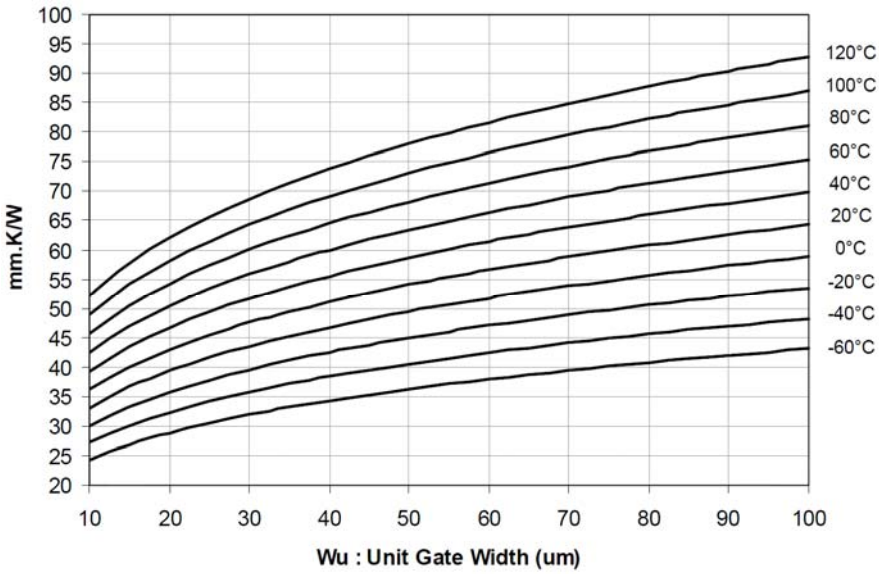

Figure 6. Thermal resistance as a function of the unit gate width and temperature for the UMS PPH25X process. Reproduced with approval from [15]

Another method proposed by Darwish [16] presents a closed form expression for the thermal resistance of multifinger FET structures. The expression is derived from the physical model for temperature behavior based on the three dimensions Laplace equation, the geometry is treated as ellipsoids and cylindrical thermal surfaces using cylindrical coordinates. The model has been tested against FEM and MoM (Method of Moments) simulators showing very good agreement with an accuracy of 2%. The absolute thermal resistance of the device θ can be calculated as:

$$\theta = \frac{1}{\pi W_g \kappa} ln\left(\frac{V[f(g[\sqrt{2s}]+1)]}{V[f(g[L_g])]}\right) + \frac{1}{2\pi s\kappa} ln\left(\frac{h(2.3t)}{h(s)}\right) \tag{2.7}$$

Where

$$h(x) = \frac{\sqrt{1+g(\sqrt{2x})}+1}{\sqrt{1+g(\sqrt{2x})}-1} \tag{2.8}$$

$$V(z) = \frac{z-1}{z+1} \tag{2.9}$$

$$f(w) = \sqrt{\frac{\sqrt{w}+1}{\sqrt{w}-1}} \tag{2.10}$$

$$g(y) = \left(\frac{W_g}{y}\right)^2 \tag{2.11}$$

The dimensions t, s, W_g and L_g are defined in figure 7 and κ corresponds to the thermal conductivity of the substrate. The temperature of the channel is therefore

$$T_{ch} = \theta P_{diss} \tag{2.12}$$

Where P_{diss} is the total dissipated power.

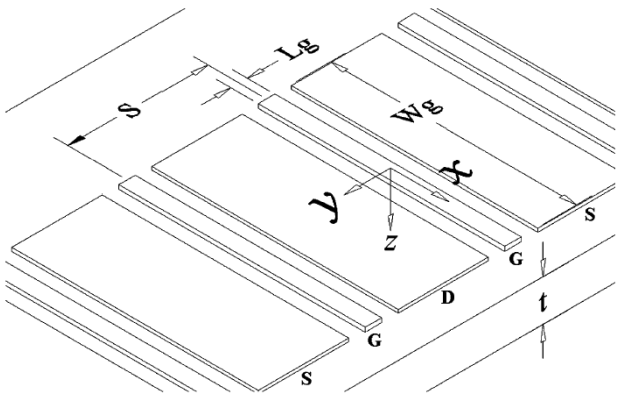

Figure 7. FET and Gate dimensions of the geometry used for thermal modeling. Copyright ©IEEE Reprinted with permission from [16]

Kirchoff's transformation should be applied since κ is temperature dependent. Using equation 2.13 for GaAs in equation 2.12 gives the final channel temperature equation:

$$\kappa(t) = 568.73\, T^{-1.23}\, W/(cm\, K) \tag{2.13}$$

$$T_{ch} = \left({T_o}^{-0.23} - 0.23(\theta P_{diss}){T_o}^{-1.23}\right)^{(-1/0.23)} \tag{2.14}$$

Experimentally is very difficult to measure the temperature exactly under the gate and it is important to understand how the temperature changes as function of the distance from the channel. Given a channel temperature T_{ch}, it is possible to calculate the temperature after a displacement d/2 from the channel as:

$$T_{d/2} = T_{ch} - \frac{P_{diss}}{\pi W_g \kappa} \ln\left(\frac{d}{L_g}\right) \tag{2.15}$$

Similar compact or closed expression models are described for different type of devices in [17-20]. These closed expressions can be used in microwave CAD software to include the thermal consideration in the circuit optimization and thus, saving time in the design process.

In reality, the MMIC chip is commonly assembled on a copper lead frame. When packaged it will be soldered over a PCB carrier that is mounted on a metallic carrier heat sink as shown in Figure 8.

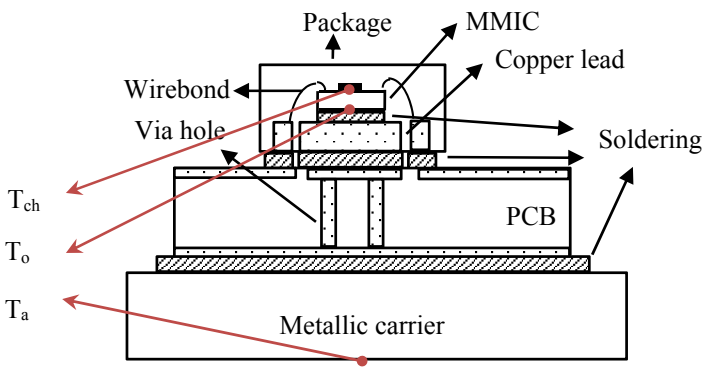

Figure 8. Cross section of an assembled packaged MMIC indicating the ambient (T_a) backside (T_o) and junction (T_{ch}) temperatures.

The working temperature or ambient temperature (T_a) is typically the rating specified in the system. The channel temperature (T_{ch}) is limited by the reliability requirement. The backside temperature of the MMIC (T_o) depends on the thermal resistances of the intermediate layers. Therefore, knowledge of the chip physical assembly is required to determine the maximum temperature gradient between channel and backside temperature (T_{ch}-T_o) required to ensure high reliability.

The equivalent thermal resistances of the intermediate layers are given by:

$$R_{th-i} = \frac{1}{\kappa_i}\left(\frac{h}{s}\right) \tag{2.16}$$

Where κ_i is the thermal conductivity of the material, h the thickness of the layer and s the cross section area participating in the heat conduction. With the thermal resistances, the temperature gradients are calculated as function of the dissipated

power (P_{diss}). The relation between the channel and the backside temperature can be calculated as:

$$T_{ch} - T_o = R_{th-GaAs}\, P_{diss} \tag{2.17}$$

And the backside to ambient temperature:

$$T_o - T_a = R_{th-eq}\, P_{diss} \tag{2.18}$$

Where R_{th-eq} is the sum of the thermal resistances of the different layers in the heat conduction path.

The desired channel temperature is defined by the lifetime required by the design and therefore the relation T_c-T_a is a given design parameter. From the previous relations we can calculate the gradient temperature between the channel and the MMIC backside:

$$\begin{aligned} T_{ch} - T_o &= (T_{ch} - T_a) - (T_o - T_a) \\ T_{ch} - T_o &= (T_{ch} - T_a) - R_{th-eq}\, P_{diss} \end{aligned} \tag{2.19}$$

For a given maximum channel temperature, equation 2.19 can be rewritten as:

$$\Delta T_{cho-max} = \Delta T_{cha-max} - R_{th-eq}\ P_{diss-max}\ [\mathrm{K}] \tag{2.20}$$

With $\Delta T_{cho-max}$ and $\Delta T_{cha-max}$ the maximum gradients between channel to backside, and channel to ambient temperatures respectively. The equation 2.20 can be used as a condition to ensure a reliability specification.

2.4 IR Temperature Measurements

Measurement techniques

The infrared microscopy is a direct temperature measurement technique measuring the radiance produced by an object due to its heat. The software supplied with the camera translates the measured radiance intensity and compares it with a reference to determine the temperature profile of the object. The reference takes account for the emissivity of the surface. The main drawback of this technique is the spatial resolution of the camera. The transistor heat sources are in the orders of

nanometers. The actual reading of temperature corresponds to the average of the area limited by the resolution of the infrared camera, typically 1-5 microns. Other limitations of the IR measurements are the error added by air-bridges over the channel and the high temperatures required for accurate measurements. The temperature resolutions achieved by IR measurements are in the range of 1 K.

When the heat sources have small dimensions as the channel of a typical transistor, this will add errors in the measurement and it is desired to make a calculation of the heat distribution within the dimension of a pixel [21]. Considering the geometry shown in Figure 7, it is possible to determine the thermal resistance of a single gate transistor according to equation 2.7:

$$\theta = \frac{1}{\pi W_g \kappa} ln\left(\frac{8t}{\pi L_g}\right) \tag{2.21}$$

The formula describes the exponential dependence of the temperature with the gate length and thickness. Based on this, the temperature profile as a function of the distance from the gate is:

$$T(z) = \frac{1}{\pi W_g \kappa} \ln\left(\frac{t}{z}\right) \tag{2.22}$$

Note the similarity with the equation 2.15 for the case of a multifinger device.

Figure 9 shows the steep temperature gradient close to the channel. The heat source is dimensionally very small compared to the radius of the spatial resolution of the infrared measurement and therefore the temperature is averaged and can be calculated as

$$T_{avg} = T_{ch} R_{IR} \tag{2.23}$$

Where R_{IR} is a correction factor for the infrared measurement depending of the shape of the sensor.

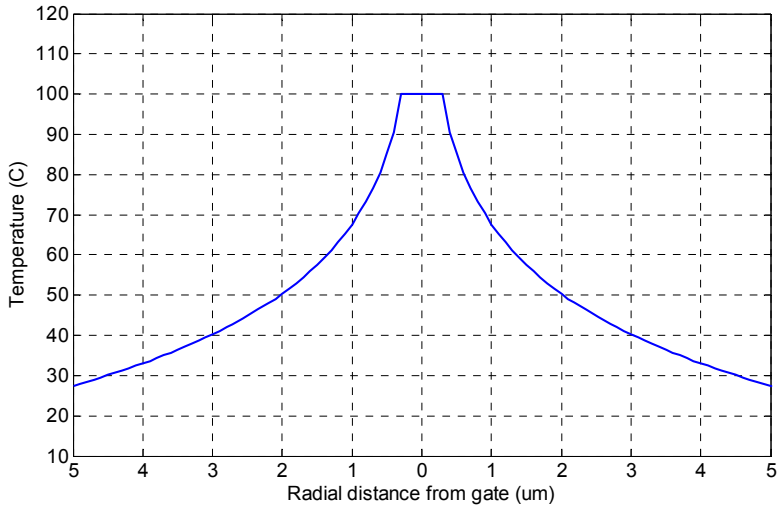

Figure 9. Generic temperature profile showing the exponential drop describe in equation 2.22

Assuming a circular area with radius r centered on the heat source the R_{IR} ratio is defined as:

$$R_{IR} = \frac{2}{\pi r}\left(L_g + \frac{\pi r/2}{\ln\left(\frac{8t}{\pi L_g}\right)} \ln\left(\frac{t}{0.35r}\right)\left(1 - \frac{2L_g}{\pi r}\right)\right) \tag{2.24}$$

And for a LxL square area is:

$$R_{IR} = \frac{1}{\ln\left(\frac{8t}{\pi L}\right)}\left(\ln\left(\frac{8t}{\pi L}\right) - \frac{L_g}{L} + 1\right) \tag{2.25}$$

Among other techniques commonly used to measure the channel temperature is the *thermo-reflectance thermography*. This measures the change of the reflectivity of a surface due to a change in temperature. When coupled with a high magnification microscope it gives good accuracy in the measurement. Another method is the *liquid crystal thermography* that uses the known phase transition of a crystal to determine the temperature of the channel. The small crystals are located in a thin layer over the region to be measured, the surface is illuminated with polarized light, and the reflection is measured. The optical properties of the crystal change with temperature and it becomes brighter or darker. The reporte temperature resolution is in the range of 1 mK [22]. Other methods as *fluorescent microthemography*, *scanning thermal microscopy*, *optical beam deflection*, *Raman spectroscopy* and *scanning force microscope* are described in literature [22-24].

Device Measurements

Measurements were done to verify the presented models. The IR thermography was done using the infrared microscope from Quantum Focus Instruments *Infrascope III*. Equipped with LN_2 cooled detector. IR light was collected by a SiGe 15x lens with working distance 15 mm. This system is built with automatic emissivity correction in real time allowing true temperature images. The spatial resolution is 2.5 µm and the image pixel resolution is 1.6 µm.

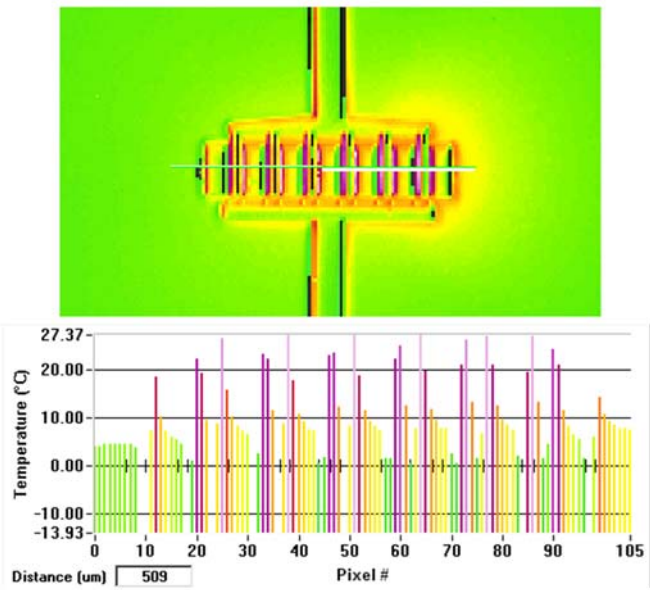

Figure 10. IR image and transversal measured temperature for a PPH25X 12 x 80 µm transistor.

A pHEMT GaAs transistor with 12 fingers of 80 µm from the PPH25X process of United Monolithic Semiconductors was measured at backside temperature of 80 °C. As shown in figure 10, the highest temperature under the central gates is 107 °C. The bias point was changed in order to determine the curve at different dissipated power levels. In figure 11 is shown how the Darwish and Fukui prediction methods fall within 3 degrees of accuracy.

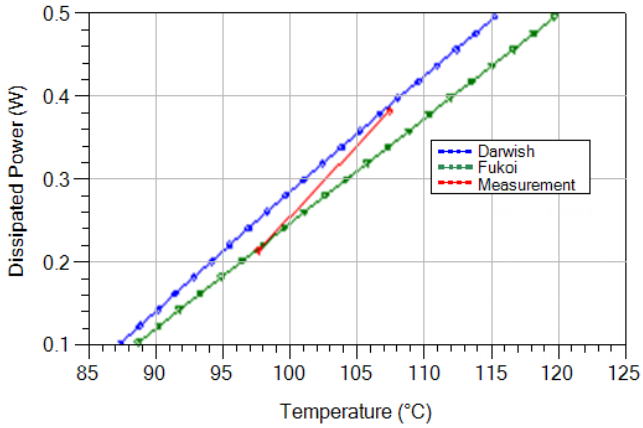

Figure 11. Junction Temperature prediction and measurement at a backside temperature of 80°C for 12 x 80 um devices.

Chapter 3

Device Modeling for Linearity

3.1 Device Modeling and characterization

Successful design of high linear circuits requires a transistor model that can accurately predict the intermodulation products generated by nonlinearities in the device. In general, the models used in nonlinear CAD simulators are based on empirical extraction and fitting of DC and small signal measured data. This approach offers good results in many applications. However, the intermodulation products are not necessarily accurately predicted. A model for facilitating circuit design for linearity must provide main functions with continuous high order derivatives. The model can be improved by fitting large signal measurements data covering a range around the quiescent point where also the bias and the S parameter should be valid.

Large signal network analyzers (LSNA) measure the magnitude and phase of the incident and reflected signals in the DUT ports. The complex data acquired in the measurement can be transformed to time domain waveforms used to compute nonlinear models [25]. The LSNA covers regions of the Smith chart in a dynamic way, this is especially important power amplifiers design.

One desirable feature in a transistor model, is the consideration of self-heating effects due to the power dissipated by the device. The electrical performance is affected by self-heating in different ways. as an example, in GaAs HBTs the current gain is decreased [26]. Self-heating and its effects on electrical performance are interdependent; the self-heating depends on the dissipated power which in turn is affected by temperature. The equations describing this phenomena are nonlinear, adding complexity to the simulation and the model.

For the circuits designed in this thesis, a large signal modeling was developed. In addition to the standard IV and S-Parameters measurements, the model was refined and verified by utilizing an active load pull system based on the Maury MT4464 LSNA. A set of measurements were performed to extract the model parameters under large signal conditions [27]:

- Active load pull: this measurement is based on the concept of reflection coefficient as the ratio between the incident and reflected waves at a determined port. The wave generated by the DUT is directed to a circulator with a 50 Ohm termination and a reflected wave is generated and injected at the output. The control of the power ration between the 2 signals creates a sweep of the load around the smith chart.
- Power spectrum: In this measurement a 50 Ω load is used and the different harmonics generated are measured for different bias points.
- Active Load: In order to evaluate the performance of the device in the knee of the DC characteristic a special measurement is designed where the load sweeps along the real impedance axis changing the load line slope for the same bias point.

With the data collected from the large signal measurement, fitting and optimization is performed to refine the large signal model. The modeling of the device is based on the Chalmers model [27] where the gate control is defined as function of drain voltage and current (V_{pk} and I_{pk}) at maximum transconductance:

$$I_d = I_{pk}\big(1 + tanh(\psi)\big)\,(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{3.1}$$

Where,

$$\psi = P1\big(V_{gs} - V_{pk}\big) + P2\big(V_{gs} - V_{pk}\big)^2 + P3\big(V_{gs} - V_{pk}\big)^3 + \cdots \tag{3.2}$$

The peak voltage, drain current and its derivatives respect to the gate voltage are well defined and coupled to measured values. This model predicts accurately the small signal and large signal behavior of the transistors used in this work.

The main variables of the model are temperature dependent and modeled using linear functions [28]:

$$P(t) = P_0 + A_1 \Delta T \tag{3.3}$$

Where P_0 is the parameter value at room temperature, ΔT is the temperature difference with the ambient temperature and A_1 is the linear temperature coefficient found empirically for each parameter.

3.2 Source of non-linearities

The circuits in papers A and B were designed using a 0.25 μm GaAs pHEMT space qualified technology. It is a mature and stable process and fulfills the requirements to be a space qualified. It delivers a power density up to 900 mW/mm. The technology utilizes a 70 μm thick substrate with a double 0.25 μm T shaped aluminum gate [15]. The active device is an AlGaAs-InGaAs-GaAs pseudomorphic HEMT as shown in figure 12.

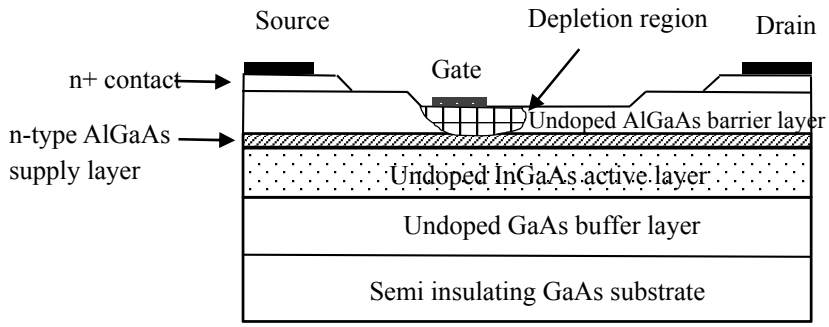

Figure 12. Diagram of AlGaAs-InGaAs-GaAs pHEMT structure.

The most basic characterization of a transistor is the I-V characteristic, corresponding to the drain current relations with the drain and gate terminal voltages (figure 13). Since the main non-linearities are contained in these relations, a correct I-V characterization of the transistor is the first step into an accurate non-linear model.

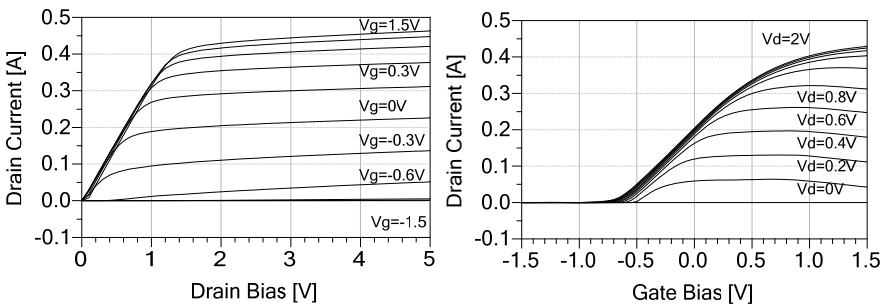

Figure 13. Drain current modelled as function of drain bias and gate bias for a GaAs pHEMT transistor 12x 80 μm.

The non-linear behavior in the I-V characteristic of the transistors can be described with the concepts of harmonic and intermodulation distortion. In the first case, the harmonic distortion, refers to the non-linear components generated by the device when a single tone signal is injected. If we assume the relation of the input and the output as:

$$V_{out} = f(V_{in}) \tag{3.4}$$

Where the signal $V_{in}$is formed by a DC level with a single tone:

$$V_{in} = V_{dc} + V_p \cos(\omega t) \tag{3.5}$$

The resulting output can be expressed as:

$$V_{out} = a_0 + v_{out} \tag{3.6}$$

With v_{out} corresponding to the output of the single tone that can be expanded as a Taylor series:

$$v_{out} = a_1 v_p cos(\omega t) + a_2 {v_p}^2 cos^2(\omega t) + a_3 {v_p}^3 cos^3(\omega t) + \cdots \tag{3.7}$$

$$= a_1 v_p cos(\omega t) + \frac{1}{2} a_2 {v_p}^2 [1 + cos(2\omega t)] + \frac{1}{4} a_3 {v_p}^3 [3cos(\omega t) + cos(3\omega t)] + \cdots \tag{3.8}$$

Organizing the components for each frequency up to the third order, the output voltage is:

$$v_{out} = \frac{1}{2} a_2 {v_p}^2 + \left[a_1 v_p + \frac{3}{4} a_3 {v_p}^3\right] cos(\omega t) + \frac{1}{2} a_2 {v_p}^2 [cos(2\omega t)] + \frac{1}{4} a_3 {v_p}^3 [cos(3wt)] \tag{3.9}$$

In the equation 3.9 is demonstrated that for a single tone input, the output spectrum contains components generated at integer products of the input tone frequency. At the frequency corresponding to the input tone, the amplitude is determined by the coefficients a_1 and a_3, normally the value of a_3 is lower compared to a_1 but with opposite sign. At higher levels of v_p, a_3 influences the output leading to gain compression [29]. The elements of the Taylor expansion represents the high order derivatives of the transfer function.

The harmonics produced by a single tone can be easily filtered out as they occur at frequencies out of the band. However, when the input is formed by more tones there are harmonics generated close to the fundamental frequency. Using the Taylor expansion the output spectrum is calculated in the same way as above:

$$v_{out} = a_2 {v_p}^2 + \left[a_1 v_p + \frac{9}{4} a_3 {v_p}^3\right] cos(\omega_{1,2} t) + \frac{1}{2} a_2 {v_p}^2 [cos(2\omega_{1,2} t)] + \frac{1}{4} a_3 {v_p}^3 [cos(3\omega_{1,2} t)] + a_2 {v_p}^2 [cos(\omega_2 t - \omega_1 t)] + \frac{3}{4} a_3 {v_p}^3 [cos(2\omega_{2,1} t - \omega_{2,1} t)] \quad (3.10)$$

The equation 3.10 has components in the frequencies $\omega_1, \omega_2, 2\omega_1, 2\omega_2, 3\omega_1, 3\omega_2, \omega_1 + \omega_2, \omega_2 - \omega, 2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. The last 3 components are the base-band tone and both third order intermodulation tones (IM3) respectively. Expanding our analysis to higher orders will result in additional intermodulation tones as $3\omega_1 - 2\omega_2$ and $3\omega_2 - 2\omega_1$ known as the fifth order intermodulation tones (IM5). The base-band tone requires special attention as it can downconvert unwanted signals to the desired baseband frequencies. The elements of the expansion that define the intermodulation distortion are also defined by the derivatives of the transfer function, showing their importance for modeling purposes. To illustrate the intermodulation distortion a measurement of the fundamental, the 2nd and 3rd order IMD is plotted in figure 14 as function of the input power in an amplifier.

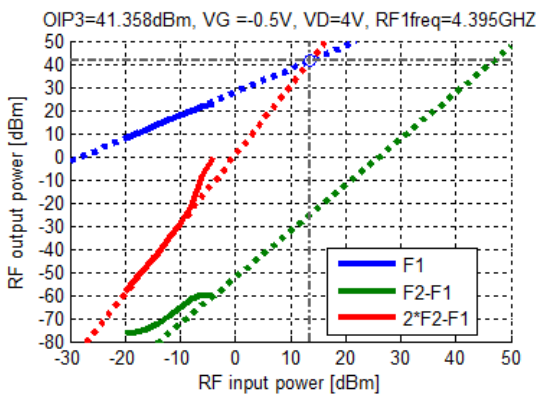

Figure 14. Measured fundamental, second and third order intermodulation products as function of input power in a power amplifier.

The top blue line corresponds to the fundamental output power at 4.395 GHz, the green line at the bottom is the 2nd order intermodulation product at 10 MHz and the middle red line is the 3rd order product at 4.415 GHz. The dotted lines are the linear extrapolations with the corresponding slope at the linear region. The OIP3 is calculated as the intercept point between the fundamental and 3rd order extrapolation lines.

The model capacitances C_{gs} and C_{gd} have a strong dependence on bias affecting the linear behavior of the device, therefore a transistor model intended for linearity should accurately describe these nonlinear elements. Examples of the modeled capacitances variations as function of drain bias for different gate bias are shown in figures 15 and 16 for a GaAs pHEMT transistor.

In these plots, the capacitances vary with both the gate and drain bias. Its modeling will influence the accuracy to predict harmonic and intermodulation distortions. The capacitances of the nonlinear model use the same type of continuous functions as the current:

$$C_{gs} = C_{gs0}\big(1 + tanh(\psi_1)\big)\big(1 + \tanh(\psi_2)\big) \tag{3.11}$$

$$C_{gd} = C_{gd0}\big(1 + tanh(\psi_3)\big)\big(1 - \tanh(\psi_4)\big) \tag{3.12}$$

with,

$$\begin{aligned}
\psi_1 &= P_{0gsg} + P_{1gsg}\,V_{gs} + P_{2gsg}\,{V_{gs}}^2 + P_{3gsg}\,{V_{gs}}^3 + \cdots \\
\psi_2 &= P_{0gsd} + P_{1gsd}\,V_{ds} + P_{2gsd}\,{V_{ds}}^2 + P_{3gsd}\,{V_{ds}}^3 + \cdots \\
\psi_3 &= P_{0gdg} + P_{1gdg}\,V_{gs} + P_{2gdg}\,{V_{gs}}^2 + P_{3gdg}\,{V_{gs}}^3 + \cdots \\
\psi_4 &= P_{0gdd} + (P_{1gdd} + P_{1cc}\,V_{gs})V_{ds} + P_{2gdd}\,{V_{ds}}^2 + P_{3gdd}\,{V_{ds}}^3 + \cdots
\end{aligned} \tag{3.13}$$

The ψ_i elements are related to the gate and drain voltages and its cross coupling dependences [30].

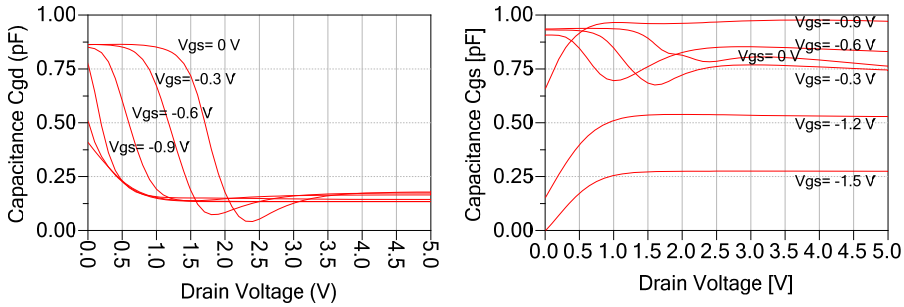

Figure 15. (left) C_{gd} model capacitance and (right) C_{gs} model capacitances variations as function of drain bias for a 12 x 80 µm GaAs pHEMT transistor. Gate bias sweep is from -1 to 1 V.

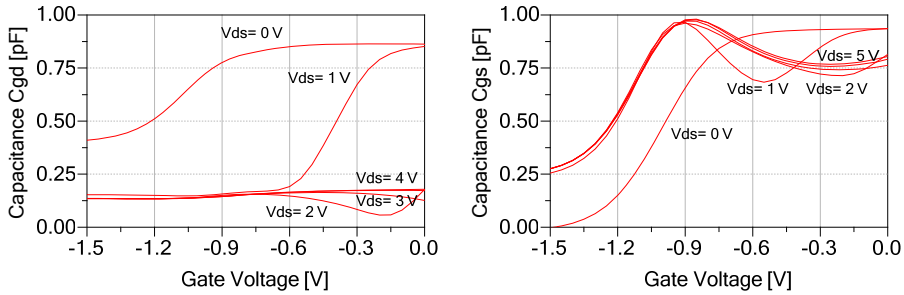

Figure 16. (left) C_{gd} model capacitance and (right) C_{gs} model capacitances variations as function of gate bias for a 12 x 80 µm GaAs pHEMT transistor. Drain bias sweep is from 0 to 5 V.

In this way, the model allows to analyze the variations of these non-linear elements according to the bias point. When examining closely the plots on figures 15 and 16, C_{gd} capacitance presents less variations at typical drain bias higher than 3 V. Meanwhile, C_{gs} capacitance shows stronger dependence with the gate bias.

A similar analysis can be done on the transconductance variation. The shapes shown in figure 17 suggest a strong non-linear dependence of the transconductance with the gate bias. The bell shape typical of a GaAs HEMT device represents a non-linear response of the active device. Consequently, it is important to select a bias point according to the transconductance variations. In this example, a gate bias around -0.5 V and drain bias higher than 3 V reduce the effect of the non-linear transconductance and capacitances.

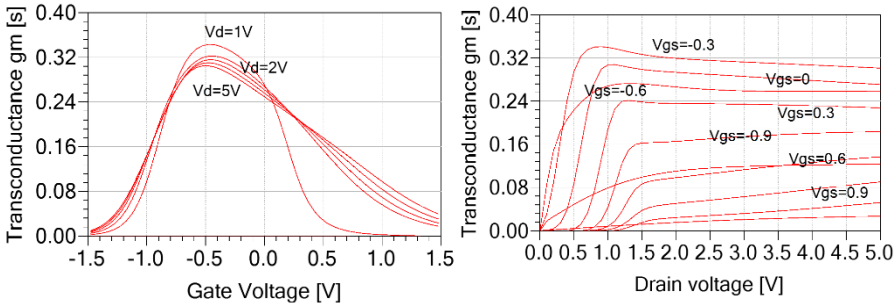

Figure 17. Model transconductance gm as function of (left) gate bias and (right) drain bias for a GaAs pHEMT transistor 12x 80 µm.

The transconductance, and the output conductance can also be affected by frequency dispersion. This is characterized by differences between DC and RF operation. Dispersion can be caused due to imperfections or defects in the semiconductor materials and the channel itself. These imperfections create states that can capture and release electrons or holes changing the charge density in the channel, known as charge-trapping effects. Other cause for transconductance and output conductance dispersion is due to thermal effects especially in power transistors [31].

From the discussion above, the nonlinear elements of the model should consider charge conservation, dispersive effects and show consistency with the small signal parameters. With such model, a precise analysis of the non-linear response of the transistor as function of bias point, the load impedances and load terminations can be performed as starting point for designing high linear amplifiers.

Chapter 4

Design of High Linear Power Amplifiers

On a Satellite link, multiple channels are amplified using a single wideband power amplifier, what is known as multicarrier amplification. The power amplifier operates at back-off, below its maximum output power, typically at 16 dBm, in order to maintain linearity and to reduce intermodulation products. The power amplifiers presented in this work are aimed to be used in a multicarrier satellite link, where the special conditions explained in chapter 2 and 3 should be considered. The design of these type of circuits push the designer to consider tradeoffs between output power, gain, linearity, DC consumption, bias and junction temperature to ensure high reliability. For instance, a typical requirement is that transistors should operate at less than 75% of its maximum DC ratings.

4.1 Transistor Selection

The device size is the first choice where all the tradeoffs mentioned are taking place and will affect the topology and performance of the power amplifier. DC power consumption and reliability are important limitations in this decision. In section 2.3 the prediction methods for junction temperature were explained using closed expressions and parametric plots. Using the information in the plot of the figure 6, it is possible to determine the temperature increment in the channel as function of the gate width W_u, the number of fingers N and the dissipated power P_{diss}:

$$\Delta T_{ch} = \left[\frac{R_{th}*1000}{N*W_u}\right] P_{diss} \tag{4.1}$$

The thermal resistance R_{th} is extracted directly from the plot for a given backside temperature. In this way, different transistors sizes can be evaluated in a fast approach. The characteristics of the MMIC assembly are known and an empirical definition for the maximum allowed temperature increment was provided following the shape of equation 2.20:

$$\Delta T_{cho-max} = 32 - 30P_{diss}\ [\mathrm{K}] \tag{4.2}$$

The factor of value 30 accompanying the dissipated power in equation 4.2, corresponds to the equivalent thermal resistance of the materials involved in the assembled MMIC as explained in section 2.3. The constant value 32 which units are Kelvin, is the maximum junction temperature difference referred to the metal plate. The criteria for reliability given for the design is a maximum junction temperature over the back plate of 32 °C or 112 °C assuming 80 °C in the backside . The designs made in this thesis will follow this condition.

Using equation 4.1 together with 4.2 and assuming 80 °C in the backside, specific values for the maximum dissipated powers can be calculated for each combination of gate width and number of fingers following Fukui relations:

$$P_{diss-max} = \frac{32}{\left[\frac{R_{th}*1000}{N*W_u}+30\right]} \tag{4.3}$$

Table I shows thermal resistance, maximum dissipated power and maximum temperature increment for different device sizes.

Table I. Maximum dissipated power for different transistor sizes

W_u [µm]	N	R_{th} [$KW^{-1}mm$]	$P_{diss-max}$ [mW]	$\Delta T_{cho-max}$ [K]	$\Delta T_{cho-calc}$ [K]
40	10	64	168	26,95	23,12
40	12	64	196	26,12	22,45
60	10	72	213	25,60	21,88
60	12	72	246	24,62	21,03
80	10	77	253	24,40	21,05
80	12	77	290	23,29	20,07

An additional calculation using the relation described in equations 2.7 to 2.14 is done to corroborate the results in table I. The backside temperature used is 80 °C. For comparison, the calculated temperature increment is shown in the last column of table I. A difference between 3 to 4 °C is found between both methods, this is also noticed in figure 11.

A large device is desired as it dissipates heat more efficiently and also offers higher power. However, with a larger device, the capacitances also increase, making it more difficult to design broadband amplifiers and therefore a compromise should be considered. An evaluation of the device electric performance for specific bias points is done in the next sections to determine the choice of the transistor size. The DC consumption at the bias point chosen should not exceed the maximum dissipated power calculated.

Bias point

For high linearity a class A amplifier is desired. The bias point is located in the middle of the load-line. The swing at the input of the transistor makes the bias point move around the linear region avoiding saturation and pinch off regions. This makes the output current waveform ideally sinusoidal. The main drawback is a low drain efficiency with a theoretical maximum of 50%. A Class B amplifier biased at the pinch-off has a reduced gain of 6 dB compared to class A. Its output waveform is a half wave rectified sinusoidal creating odd order harmonics at the output. The main advantage is a higher drain efficiency, theoretically 78.6%. A class AB amplifier is biased for a conduction angle between 180 and 360 degrees, allowing compromises between output power, efficiency and linearity. Commonly, it is biased close to pinch off (*deep AB)*. The fundamental component in class AB is larger than in class A and B and the efficiency approaches the class B as the bias closes to pinch off. The level of the harmonics depends directly on the conduction angle. Figure 18 shows the DC, fundamental and harmonics for different conduction angles. Class C operation has a considerable reduction of output power, as well as higher level of harmonics.

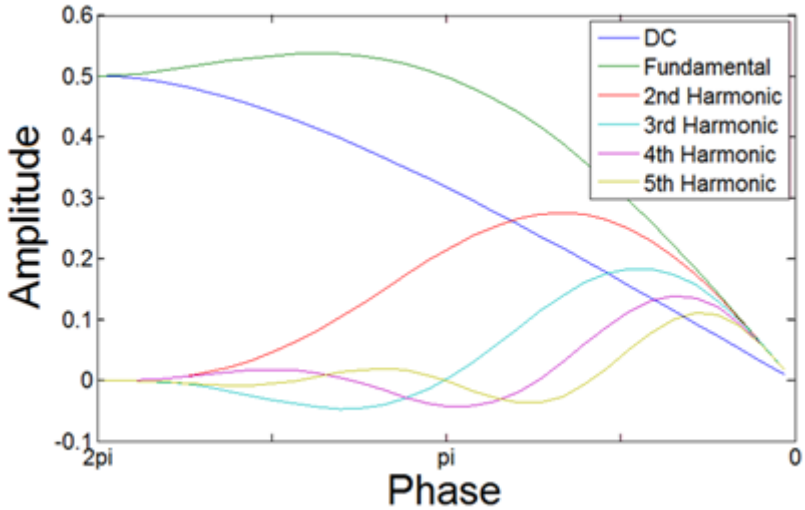

Figure 18. Fundamental and harmonics as function of the conduction angle.

For drain bias above 3 V, the non-linear capacitances and tranconductance of the model present less variations (figures 15, 16 and 17). For this reason, the drain bias chosen is 4 V. The maximum dissipated power calculated in previous section, is used to choose a bias point for the transistors. The gate bias chosen is –0.45 V corresponding to a deep class AB. As seen in figure 13, the drain current is 85 mA which result in a dissipated power of approximately 344 mW. Following the plot in figure 10, the channel temperature is less than 105 °C, still below the allowed 112 °C limit.

Load impedance optimization

With the bias chosen for a specific transistor size, 1-tone and 2-tone load pull simulations are performed to evaluate the optimum loads for the transistor. A central frequency of 4 GHz in the C – band is used for the harmonic balance simulations.

The most common figure of merit to evaluate the linearity of a transmitter is the output third order intercept point (OIP3). It is dominated by the linearity performance of the last stage. Figure 19 shows the output power and third order intermodulation (IMD3) contours for a 12 x 80 μm transistor with a drain bias 4 V and -0.45 V at the gate.

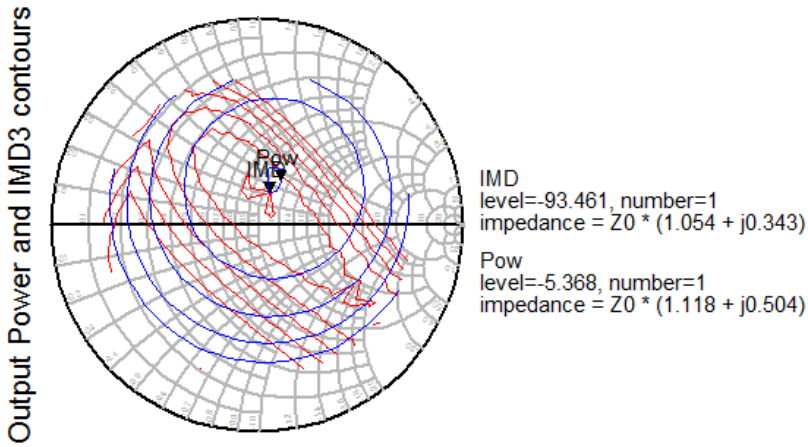

Figure 19. OIP3 and IMD3 contours from 2-tone simulations for a 12 x 80 µm transistor size.

The optimum loads for output power (Pow) and linearity (IMD) are located close to each other in the smith chart. The optimum load for linearity is chosen where the OIP3 is 37.9 dBm. A power sweep determines the 1 dB compression point 21.7 dBm with transducer gain of 13.6 dB. The calculated input impedance is 5.25 +j 17.62 Ω.

Considering the behavior of the non-linear elements described in the previous sections, an additional analysis of the OIP3 response as function of the bias operation is implemented (figure 20). As expected, the linearity is sensitive to variations in the gate bias.

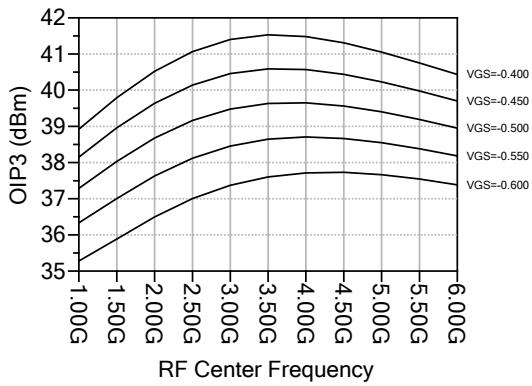

Figure 20. Third order intercept point (OIP3) for a GaAs pHEMT transistor 12 x 80 µm. The drain bias is 4 V and loads were chosen according to 2-tone load pull simulations.

Once the device size for the last stage is chosen, a power budget determines the number of transistors and stages required for the gain and power specifications. A first stage is realized with a single transistor with the purpose to achieve higher gain. The last stage provides 13.6 dB gain resulting in a required input power that can be provided by a single transistor. The power budget in figure 21, shows the corresponding power levels at different points of the amplifier.

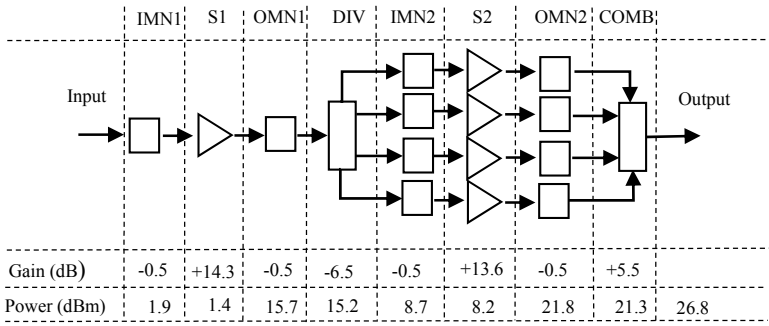

Figure 21. Amplifier power budget

In the power budget losses of 0.5 dB are assumed for the matching networks, the divider and the combiner. An output power of 15.7 dBm is required in the first stage. This power should be obtained in the linear region of the transistor to avoid compression. For that reason, the 1dB compression point of the first stage should be at least 3 dBm over the required power. The size selection for the first stage was done following the analysis explained before. A 12 x 60 µm transistor satisfies the power requirements keeping the reliability under control. The bias point is chosen to be a class AB with V_{ds}= 4 V and Ids = 63 mA. The resulting DC power is 253 mW. The calculated junction temperature is 101.6 °C with 80 °C back plate temperature. This falls below the reliability conditions presented in table I. Table II summarizes the chosen transistor characteristics.

Table II. Summary of the transistor size selection

W_u [µm]	N	Gain [dB]	P_{1db}[dBm]	$T_{ch-calc}$ [°C]	Z_s [Ω]	Z_l[Ω]
60	12	14.3	19.03	101.6	4.11 - j16.56	70.5 + j35.97
80	12	13.6	21.77	103.9	5.25 – j13.04	52.95 + j17.62

4.2 Amplifier Topology

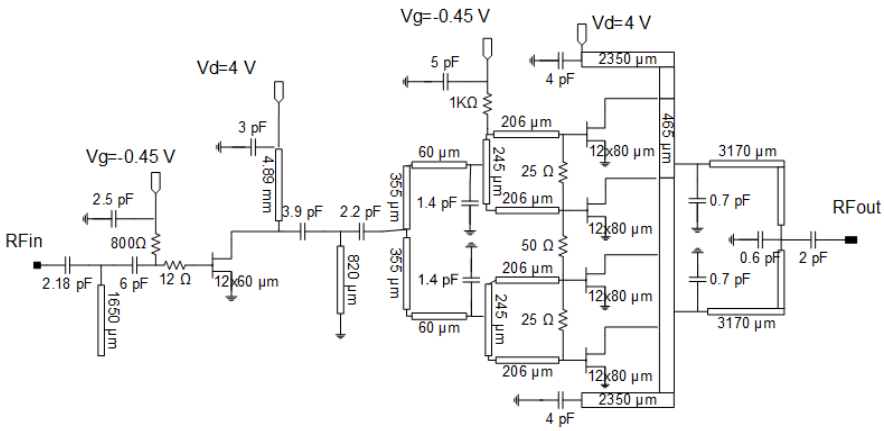

Figure 22. Schematic of the high linear power amplifier in Paper A

In Papers A and B, two similar GaAs power amplifiers are presented. Both designs have a two stage topology with a last stage using a bus-bar combining four transistors at the output [32]. The drain supply for the last stage is fed from the edge of the bus-bar. The schematic for the power amplifier in Paper A is shown in figure 22. The power amplifier in paper B has small changes in the topology (Figure 23). On-chip resistors were added to the drain bias networks to lower the Q value of the resonance circuit formed when adding probe or wire-bond inductances. This was motivated by a resonance detected in the drain bias for the first circuit. The matching and interstage networks were optimized to improve the bandwidth and flatness of the gain response. All the passive blocks of the linear amplifier were realized using distributed stubs, lumped capacitors and thin film resistors available in the design kit.

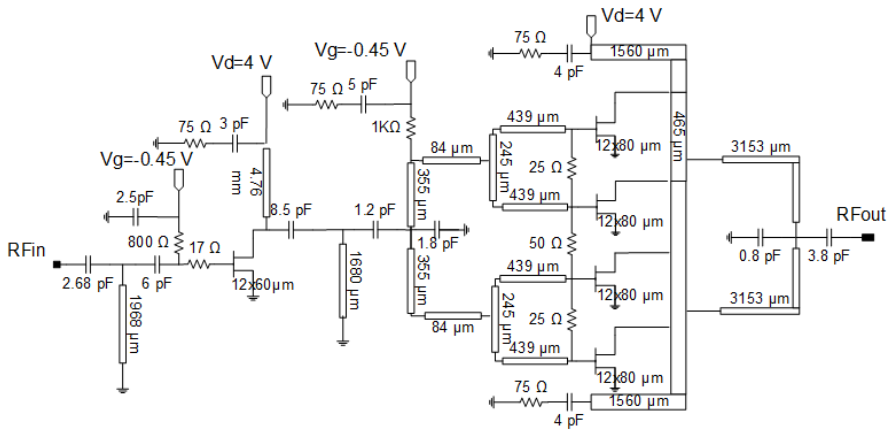

Figure 23. Schematic of the high linear power amplifier in Paper B

Busbar Combiner

The output combiner plays an important role in the power amplifier design. For the circuits presented in this work, a bus-bar was chosen to combine the power at the output. A bus-bar combiner, is a wide line which feeds the DC current to all the devices (figure 24). The RF power is combined by pairs at the symmetric points J and K along the busbar for the transistor pairs A-B and C-D respectively. The matching is done using transmission lines and shunt capacitors that are placed at these points. Under the assumption that the distance between the devices is small enough compared to the RF signal wavelength, the points U, V and W act as virtual open circuits. The distance between the transistors can be chosen accordingly to the spatial conditions of the layout and the width of the busbar should be enough to handle the current to the transistors. The input signals at the ports A to D, should be equal in phase and amplitude to ensure that there is no RF current flowing between the ports. A tree structure is used to combine the J and K outputs and for output matching. The tree structure preserves symmetry which is necessary for in-phase power combination [32].

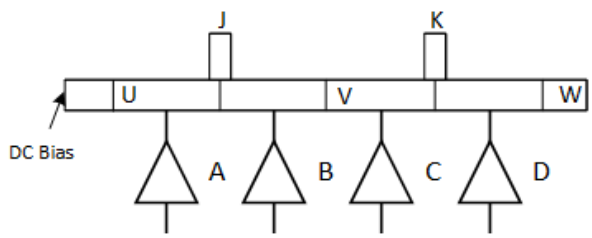

Figure 24. Busbar RF combining and virtual open circuit points.

The two main advantages of this combiner are the direct path to DC for all the transistors and the compact area used to combine several transistors in one single line. At either of the ends, a quarter wavelength line is used for DC feed the transistors. Depending on the frequency, this could result in a length physically not realizable on chip and therefore it is reduced from its optimal length deteriorating the RF decoupling of the bias network. Therefore, special care should be given to the design of drain bias circuit, and if necessary, external circuitry is added to ensure an RF decoupling and avoid resonances.

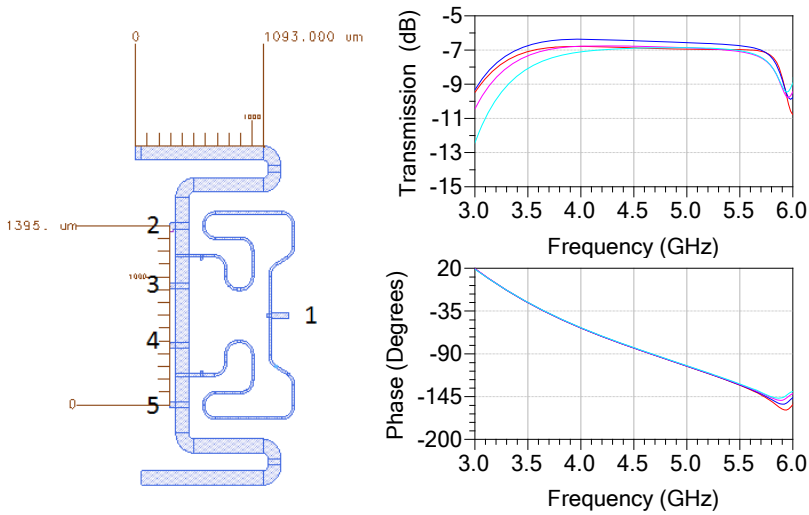

Figure 25. Busbar layout and EM simulation results for the amplifier of the paper A.

Figure 25 shows the layout of the busbar and the tree combining structure used in the amplifier A. An electromagnetic simulation is necessary to take into account possible coupling between the transmission lines and edge capacitances in the thick busbar. The target of the matching was to transform the 50 Ω load to the optimal calculated for the transistors. The EM simulations shows a good balance in phase and an unbalance of 0.8 dB in amplitude for the transmitted signals from the inputs (2, 3, 4 and 5) to the output port 1. The main cause of unbalances in the busbar combiner is due to the reduction of the quarter wavelength of the bias line. At 4 GHz, this line should be 6.6 mm length, which is excessively long for MMIC implementation and is reduced to 2.3 mm in this case. This reduction will also translate in an unsufficient RF decoupling from the bias network. As shown in the schematic (figure 23), the capacitors of the tree structure were modified to improve the bandwidth. Also, resistors were added after the decoupling capacitors to lower the Q value of the resonance circuit in the bias networks.

Matching Networks

The input matching consist of T networks with 2 capacitors in series and a parallel stub as shown in figure 26. The matching was done by optimizing the return loss transforming the input impedance of the first stage amplifier to an equivalent source impedance of 50 Ω. A 12 Ω resistor is added in series at the input of the transistor to ensure unconditional stability operation.

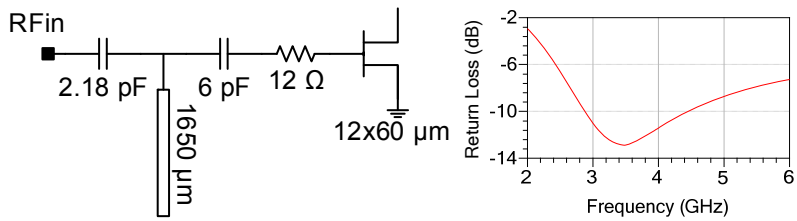

Figure 26. Schematic of the input matching network and return loss simulation for the amplifier in paper A.

For the interstage matching, there are direct and indirect techniques to get a good match. In the direct case, the two impedances, the output impedance of the first stage and the input impedance of the second one, are used to design a network that bring one to the other in the Smith chart. The indirect method defines an intermediate impedance and match independently each stage to this impedance. This will eliminate the intermediate terminations and connect the stages directly. The indirect method was used in this work with an intermediate impedance of 50 Ω. The target of the matching network was to transform the input impedances of the second stage transistor to the desired load for the first stage. The interstage matching network is formed by the output DC block capacitor of the first stage, a parallel stub and the tree structure divider (figure 27). The divider network should keep phase and amplitude balance in the four paths of the RF signal. The parallel resistors between the divider branches are to avoid odd mode instabilities, a detailed explanation is given later in this chapter.

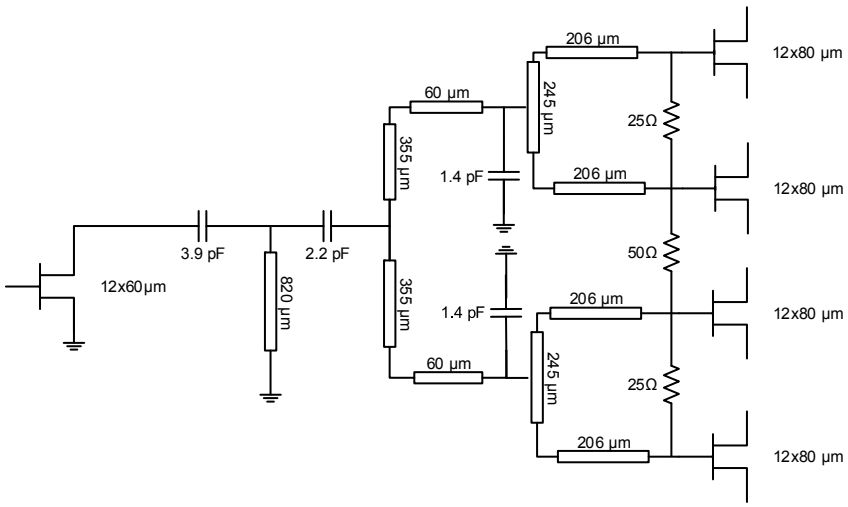

Figure 27. Interstage matching schematic for amplifier A.

The matching networks for the amplifier B, were optimized to improve the amplifier bandwidth and achieve a flattened small signal gain. The return loss in figure 28 compared to the amplifier A input matching shows an improvement in bandwidth. This will be reflected in the amplifier small signal gain.

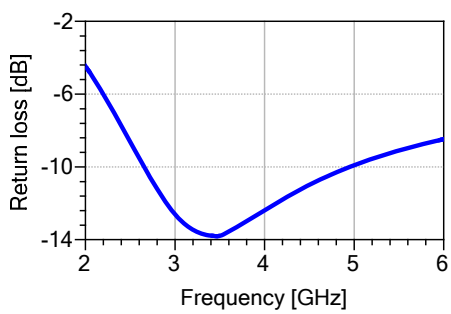

Figure 28. Improved return loss bandwidth in amplifier B

DC Feed

For amplifier A, the biasing networks were done for both gates through series GaAs resistances and shunt decoupling capacitors. In the drain of the first stage, a quarter wavelength transmission line with decoupling capacitor was used. The drains at the output stage are fed via the busbar and a capacitor is placed in shunt at the point where the dc pad is connected.

The measured S21 for amplifier A, shows an unexpected notch in the small signal gain close to 4.4 GHz (figure 29). Different possible causes were analyzed in measurements and simulations and it was determined that the notch was due to resonances in the bias networks.

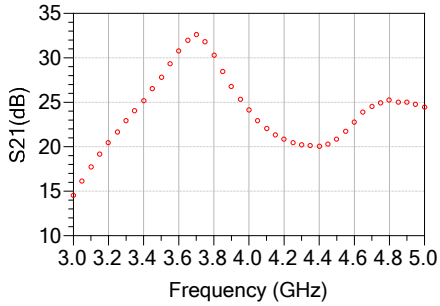

Figure 29. Expected and measured small signal parameters of the amplifier A. Note the notch at 4.3GHz

An ideal feed network formed by a quarter wavelength stub at the center frequency is analyzed presenting a high impedance for the RF signal (figure 30). The capacitor to ground represents a short-circuit for the RF signal but the quarter wave transforms it to an ideally open circuit.

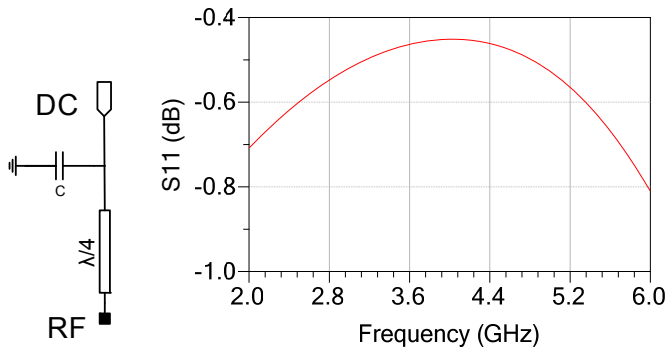

Figure 30. Ideal bias network at 4GHz. Schematic and simulation

Any additional component connected to the DC bias terminal will be invisible for the RF frequency. In reality, there are reasons why it does not happen. Firstly, even when the transmission line corresponds to a quarter wavelength, it requires a large capacitor value. In MMIC circuits the capacitance is limited to tens of pico-farads. Secondly, at RF frequencies, a real capacitor does not have a pure capacitive behavior. Finally, the via-hole used for grounding add parasitic inductances and

resistances to the network. Therefore, the RF ground is not ideal and additional elements connected after the DC pad will affect the RF signal.

DC probes or wire-bonds are commonly used to access the DC pads of the MMIC chip. These elements will introduce an extra parasitic inductance in the range between 0.2 nH to 1 nH to the bias network. Using the capacitor and via-hole models provided and including the wire-bond equivalent inductance, the same bias network is simulated in figure 31. In the simulation a resonance appears in the operation band.

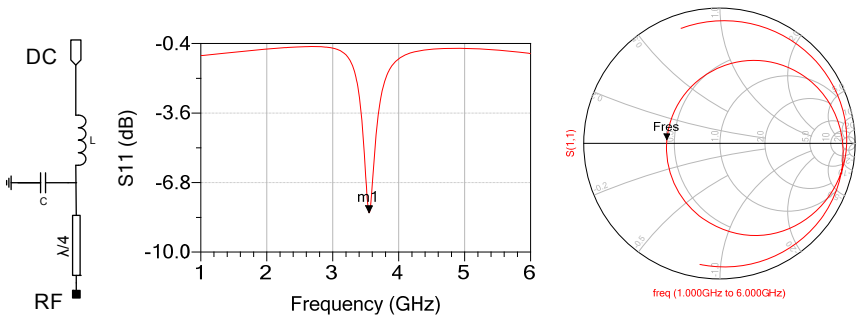

Figure 31. Ideal bias network at 4 GHz including real components and wirebond inductance. Schematic and simulation

This effect was also affecting the bias of the second stage with more severity due to the length reduction of the transmission line. Despite the efforts using external circuitry, the notch remains in the small signal and large signal response of the amplifier as will be shown in the amplifier results section. A new bias network was designed for the amplifier in paper B (Figure 32). A resistor in series to the capacitor was added to lower the Q factor of the resonance circuit, all the parasitic inductances were included in the simulation environment, as well as the external circuitry. This also permits to control the effect of reducing the length of the transmission line in the second stage bias network.

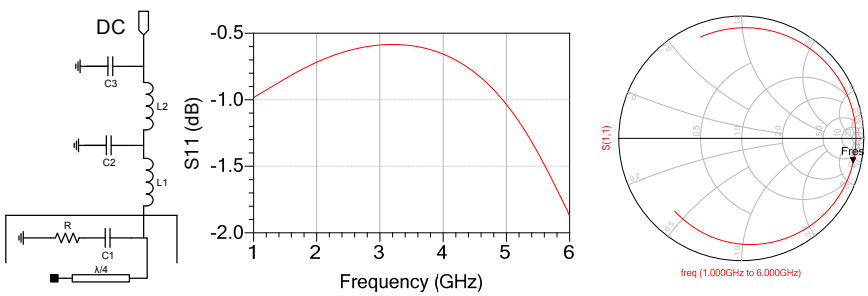

Figure 32. Complete bias network Schematic and simulation of the amplifier B.

The capacitor C1 and the resistor R are placed on the MMIC. The inductance L1 corresponds to the wire-bond or the probe inductance. The capacitance C2 simulates a thin film single layer capacitor, in the range of hundreds of pico-farads, soldered near the MMIC. Capacitance C3 relates to a surface mounted capacitors in the range of tenths of micro-farads interconnected to C2 with a transmission line corresponding to an inductance L2. As shown in the simulation result, a high impedance is seen by the RF port in the frequency of interest.

4.4 Stability Analysis

Circuit stability in power amplifiers should be given special care. The stability can be analyzed through the K-factor [33], when is greater than one the transistor is unconditionally stable and any impedance of the smith chart is suitable for matching.

$$K = \left(\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2-|S_{21}S_{12}|}\right) \tag{4.4}$$

Where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.5}$$

When the k-factor is smaller than one there is an area in the Smith chart that should be avoided. This area is limited by the stability circles, which can be calculated with the following equations:

$$C_s = \frac{(S_{11} - \Delta S_{22}{}^*)^*}{|S_{11}|^2 - |\Delta|^2}$$
$$R_s = \left|\frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|}\right|$$

$$C_l = \frac{(S_{22} - \Delta S_{11}{}^*)^*}{|S_{22}|^2 - |\Delta|^2}$$
$$R_l = \left|\frac{S_{12}S_{21}}{|S_{22}|^2-|\Delta|}\right| \tag{4.6}$$

Where C_s and C_l are the centers of the circles and R_s and R_l their corresponding radius. Note that these expressions are made with the S-Parameters of the transistor, so they describe the stability for a specific bias point. If the input signal is large the swing at the input of the transistor should be taken into account. A set of S-parameters

around the nominal bias pointwould determine more accurately the stability region of the transistor.

The K-factor method is often used but it is not enough to warrant stability in structures as the output combiner or interstage network where many parasitic loops can be formed [34]. The K-factor method only addresses even mode oscillations but other modes could be present. In particular, when using several transistors in parallel and with the need of a combiner structure, it is more likely to have odd mode oscillations. An analysis is made to find the values of the parallel resistors added between the branches at the input of the output stage of the amplifier [35].

A combination of four parallel transistors can create the same number of oscillation modes, one even mode and three odd modes. The even mode was addressed with the K-factor analysis. The odd modes were analyzed using small signal simulations and Z parameters in a circuit removing the transistors and separating the input and output passive structures (figure 33). The input and output ports of the amplifier are terminated with source (R_S) and load resistances (R_L) respectively. The ports 1 to 4 are the ports where the active devices were disconnected. For the input network (left side), the ports 1-4 correspond to the gate terminals of the transistors, meanwhile for the output network (right side) correspond to the drain terminals.

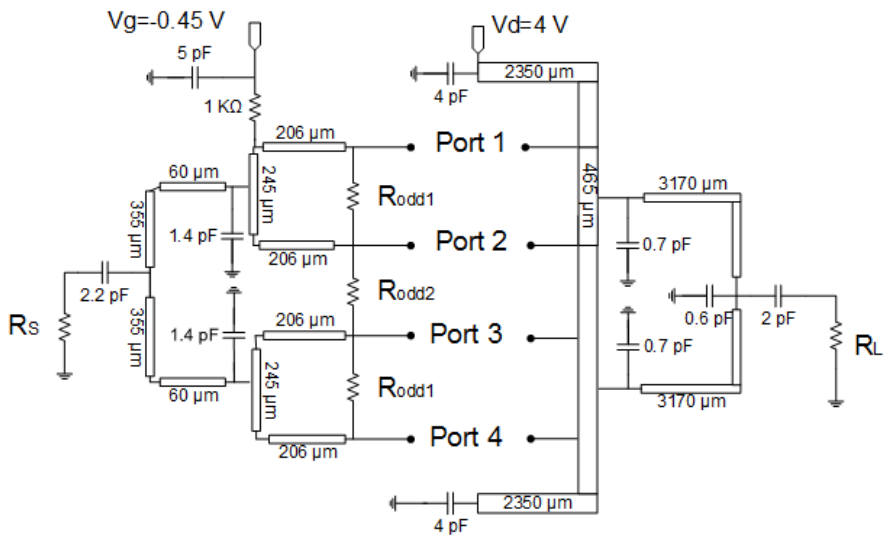

Figure 33. Input and output circuits used for mode odd analysis.

For each half, the Z parameters have different values but the Z matrix corresponds to a symmetric matrix given by:

$$Z = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{13} \\ Z_{13} & Z_{23} & Z_{22} & Z_{12} \\ Z_{14} & Z_{13} & Z_{12} & Z_{11} \end{bmatrix} \tag{4.7}$$

The associated eigenvalues are:

$$\begin{aligned} Z_e &= Z_{11} + Z_{12} + Z_{13} + Z_{14} \\ Z_{o1} &= Z_{11} - Z_{12} - Z_{13} + Z_{14} \\ Z_{o2} &= Z_{11} - Z_{14} + b_1(Z_{12} - Z_{13}) \\ Z_{o3} &= Z_{11} - Z_{14} + b_2(Z_{12} - Z_{13}) \end{aligned} \tag{4.8}$$

Where

$$\begin{aligned} b_1 &= \frac{-\frac{\beta}{\alpha} + \sqrt{\left(\frac{\beta}{\alpha}\right)^2 + 4}}{2} \\ b_2 &= \frac{-\frac{\beta}{\alpha} + \sqrt{\left(\frac{\beta}{\alpha}\right)^2 + 4}}{2} \\ \beta &= 2(Z_{23} - Z_{14}) \\ \alpha &= Z_{12} - Z_{13} \end{aligned} \tag{4.9}$$

Each of the eigenvalues represents one of the oscillations modes, one even and three odd modes. In order to check stability, the Z parameter eigenvalues are used to identify the conditions for negative resistance oscillations:

$$\begin{aligned} &Re\{Z_{ei} + Z_{eo}\} < 0 \; and \\ &Im\{Z_{ei} + Z_{eo}\} = 0 \end{aligned}$$

$$\begin{aligned} &Re\{Z_{oi} + Z_{oo}\} < 0 \; and \\ &Im\{Z_{oi} + Z_{oo}\} = 0 \end{aligned} \tag{4.10}$$

The subscripts *e* and *o* make reference to the even or odd mode being analyzed and the *i* and *o* subscripts relate to the input or output half of the circuit. If the conditions described in equation 4.10 are met, an oscillation in that mode will occur at that frequency. In that case, odd mode resistors are added and tuned to remove the negative resistance.

An initial analysis found that 2 of the odd modes met the oscillation conditions. All oscillation modes were suppressed by adding 25 Ω and 50 Ω for the R_{odd1} and R_{odd2} resistors respectively. Figure 34 shows the odd mode Z_{o3} without the resistors and how the oscillation conditions are not met when the resistors were added.

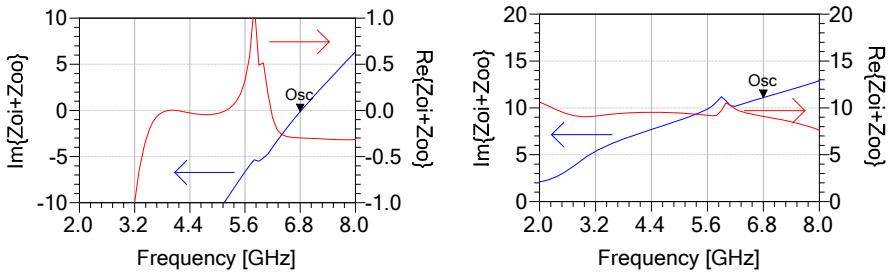

Figure 34. Z_{o3} oscillation mode condition with (right) and without (left) odd resistors.

4.5 Amplifier Results

Amplifier Paper A

The fabricated amplifier in paper A shown in figure 35, was measured with an Agilent E8361A at the designed bias condition to extract the small signal parameters. The amplifier exhibits a small signal gain of more than 30 dB and an input return loss below 10 dB. Using signal generators and a spectrum analyzer, the 1dB compression power is larger than 26 dBm and the OIP3 is above 40 dBm with 2 tones separated by 10 MHz. The resonances found in the bias network discussed in section 4.2 creates an unwanted effect at 4.5 GHz in the output power and is also present in the OIP3 measurement (figure 36). The temperature was measured at 80 °C backside as shown in figure 9 in section 2.4

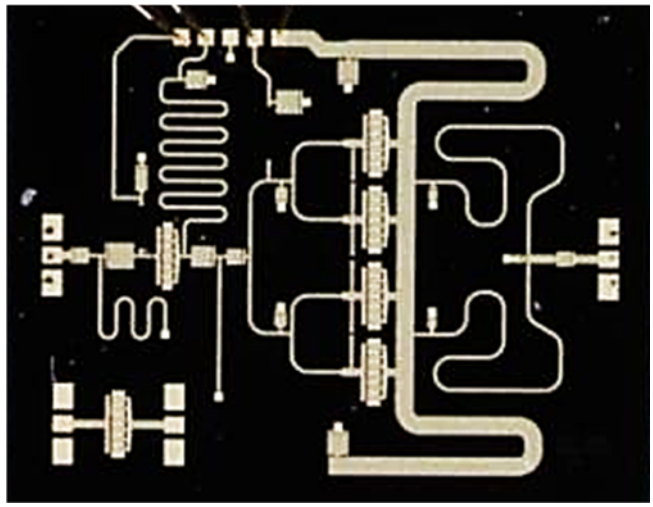

Figure 35. Chip photograph of the fabricated power amplifier for Paper A and the chip dimension is 3570 x 2810 μm^2.

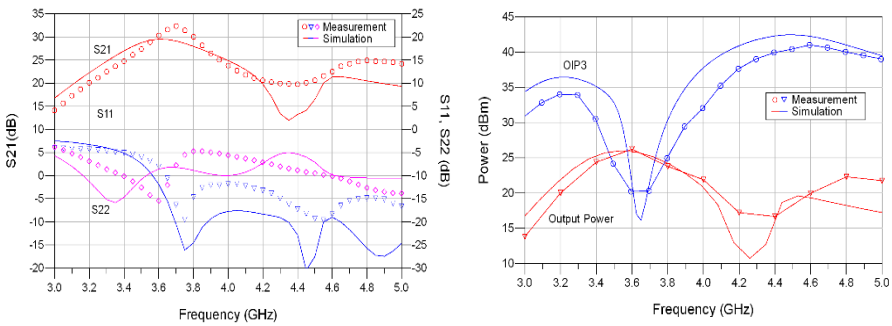

Figure 36. (left) S-Parameters and (right) output power and OIP3 simulations and measurements for the linear power amplifiers in Paper A

Amplifier Paper B

A photograph of the amplifier in paper B is shown in figure 37. The measured S-parameters shows a flattened gain above 25 dB in the frequency band between 3 to 6 GHz. The main differences compared to the previous amplifier are the improved bandwidth and the bias network correction. The 1dB compression point is at 26.7 dBm and the OIP3 is above 40 dBm in the frequency band of interest, reaching a maximum of 41.7 dBm at 4.5 GHz. The measured results match the simulation with good agreement. Figure 38 presents the small signal and power measurement results.

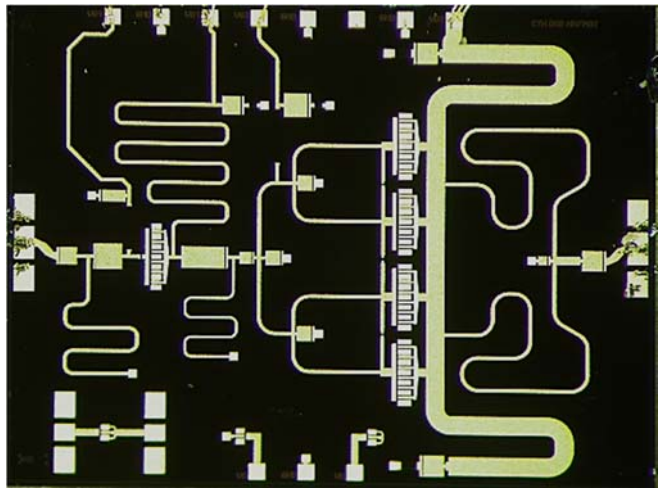

Figure 37. Chip photograph of the fabricated power amplifier for Paper B. The chip dimension is 4000 x 3000 μm^2.

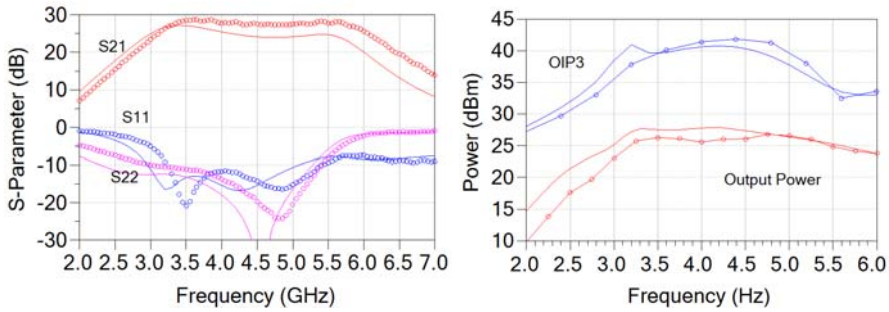

Figure 38. (left) S-Parameters and (right) output power and OIP3 simulations and measurements for the linear power amplifier in Paper B

The power amplifier is measured using an infrared microscope at 80 °C backside temperature (figure 39). A thermal coupling between the transistors at the middle of the last stage is observed. A high resolution IR image of the second transistor from the top in the last stage is also shown. The measured peak temperature is 112 °C for a dissipated power of 415 mW. The transistor temperature at the first stage was measured with a corresponding peak of 107 °C for a dissipated power of 311 mW.

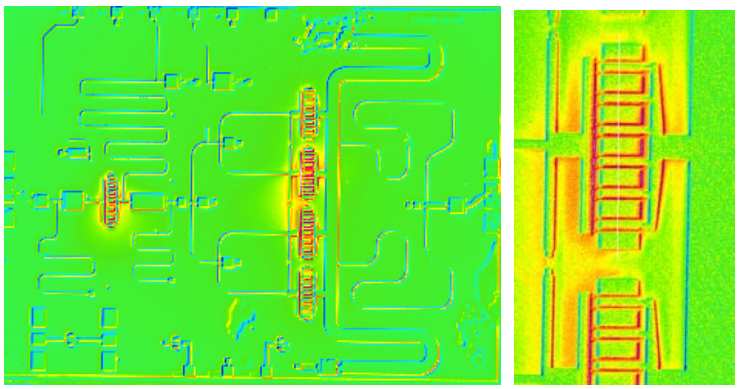

Figure 39. (left) MMIC power amplifier IR image and (right) output stage transistor IR image at 80 °C backside temperature.

In power amplifiers, the increase in active device size leads to a potentially higher output power and higher OIP3. An interesting figure of merit for the evaluation of linearity for amplifier designs is the ratio between OIP3 and 1dB compression point (P1dB) at the fundamental frequency. In table III, published GaAs C-Band power amplifiers with reported OIP3 are listed for comparison. The figure of merit OIP3/P1dB is shown in the last column. Only the references 36 and 38 report junction temperatures, correspondingly 158 °C and 125 °C. In addition, to keep low DC consumption and lower complexity, the circuits presented in this thesis do not use additional circuitry for linearization.

Table III. Published C-Band GaAs linear power amplifiers

	Technology	Freq. (GHz)	Gain (dB)	Bias (V/mA)	P1dB (dBm)	OIP3 (dBm)	OIP3/P1dB
[36]	GaAs HFET 0.5 µm	5.5-7.1	15	8/1300	36	50	14
[37]	GaAs pHEMT 0.5 µm	5.8	14	5/110	27	37,5	10,5
[38]	GaAs pHEMT 0.15 µm	5.2	15	4	13,3	22,5	9,2
[39]	GaAs pHEMT 0.4 µm	3.3-3.8	30.4	8/700	34	43,5	9,5
[40]	GaAs	4.9-8.5	20	5/98	19	31	12
[41]	GaAs pHEMT 0.15 µm	11-15	16	3/150	23	35	12
[42]	GaAs pHEMT 0.15 µm	17-27	19	4,5/890	28,5	38	9,5
Paper A	GaAs pHEMT 0.25 µm	3,8	33	4/560	24	36,7	12,7
Paper B	GaAs pHEMT 0.25 µm	3-6	33	4/580	26,6	41,7	15,1

Chapter 5

Conclusions and Future Work

The aim of this thesis was to give an insight about the design for high linear power amplifiers for space applications. An overview about the special conditions of the space environment and how it affects the design is provided. Special emphasis is given to reliability considerations and the device MTTF calculations. In addition, models for accurate prediction of junction temperature were explained and verified with IR measurements.

A systematic procedure to determine the active device size in order to deal with tradeoffs between the electrical performance and reliability is proposed and demonstrated.

For the foundry process used, a nonlinear HEMT model was extracted and successfully used for the amplifier designs. An analysis of the non-linear elements in the model and its variations with bias is underlined as a fundamental element in the high linear amplifier designs.

Also, a method to determine the optimum loads and bias operation point is described. Additional studies in the busbar combining structure, feed networks, and odd modes stabilization were presented as tools for power amplifier design.

Two highly linear C-band GaAs power amplifiers for multicarrier satellite links were presented. The power amplifiers succeeded reaching an OIP3 over The OIP3 is 15 dB higher than the output power at its 1 dB compression point.

Despite the dominant preference of GaAs circuits in the satellite industry, there are recent advances towards the inclusion of GaN amplifiers. A K- Band linear amplifier was published with a 4 W output power and 40 dBm OIP3 [43]. A GaN amplifier in a Darlington Cascoded topology is demonstrated by Kobayashi in [44]

at 18 GHz with a 1 dB compression point of 31 dBm and OIP3 > 40 dBm. This trend creates opportunities to elaborate research on circuit design, GaN devices reliability and temperature management at chip level. GaN based circuits can be an attractive choice for higher frequencies in the Ku bands used in satellite communications where the power performance of GaAs starts to deteriorate. However, there has been very few investigation regarding reliability of GaN based MMICs. Recently AlGaN/GaN on SiC technology has been reported to be evaluated for space missions [45]. One of the first reports in reliability of GaN MMICs shows a lifetime above 10^5 h at a channel temperature of 200 °C [46].

Highly linear amplifiers require the study of the non-linear phenomena involved at transistor level. Further analysis should be done evaluating the model elements and their influence in the linear behavior of the transistor. Additional studies can be performed on the linear response variations due to temperature and self-heating of transistors. Finally, specialized linear topologies can be tested such as feedback or analog predistortion, where the power consumption is not severely increased but the linearity is improved.

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