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Advanced Transmitter Architectures Based on Switch Mode Power Amplifiers

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Abstract

Nowadays the main driving parameters for the research in radio transmitters in wireless infrastructure are energy efficiency, frequency agility, and integration. This thesis presents new solutions at the device waveform-, circuit-, and transmitter level which exploit the inherent high efficiency potential of switch-mode power amplifiers (SMPAs) for realization of energy efficient, wide-band, highly integrated transmitters for wireless communication applications.

In the first part of the thesis, a continuum of novel high efficiency class-E power amplifier modes are derived, significantly extending the known SMPA design space. In contrast to conventional SMPA modes, the new continuum allows some variation for the switch impedances, providing important possibilities on wide-band SMPA designs. This is experimentally verified in a 1 W SiGe BiCMOS SMPA design having a drain efficiency of above 70% over a 1.3-2.2 GHz bandwidth.

In the second part a novel combiner synthesis technique is developed that enables realization of wide-band highly efficient outphasing transmitters. The technique is based on the calculation of the combiner network parameters from the boundary conditions required for highly efficient switch-mode operation of the transistors in each branch. The approach is validated in a CMOS-GaN outphasing transmitter design providing a peak output power of 44±0.2 dBm and a 7.5 dB output power back-off efficiency exceeding 52% over a 750-1050 MHz bandwidth. It is further shown that the same theoretical approach can also be used for design of Doherty PA combiner networks. A 28 W 3.5 GHz Doherty PA is designed and manufactured for experimental verification providing a record-high power added efficiency of 51% at an adjacent channel leakage ratio (ACLR) of -50 dBc with carrier-aggregated 100 MHz LTE test signals.

In the third part a new SMPA topology particularly suitable for amplification of RF pulse-width modulation (RF-PWM) signals is presented. In classical pulse width modulated SMPAs the varying pulse width leads to switching losses and hence efficiency degradation. We present an electronically tunable load output network that alleviates this problem. A 10 W 2 GHz CMOS-GaN RF-PWM transmitter demonstrator is constructed and characterized to demonstrate the feasibility of the proposed technique. ACLR after digital predistortion linearization is -45 dBc at a drain efficiency of 67% with W-CDMA communication signals.

The solutions presented in this thesis will facilitate realizations of frequency agile, energy efficient and highly integrated/digitalized radio transmitters for future wireless communication systems.

Keywords: Bandwidth, class-E, combiner, energy efficiency, outphasing, SMPA

List of Publications

Appended Publications

This thesis is based on the work contained in the following papers.

[A] M. Özen, R. Jos, and C. Fager, "Continuous Class-E Power Amplifier Modes," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.59, no.11, pp.731-735, Nov. 2012

[B] M. Özen, M. Acar, M. P. van der Heijden, M. Apostolidou, D. M. W. Leenaerts, R. Jos, and C. Fager, "Wideband and Efficient Watt-level SiGe BiCMOS Switching Mode Power Amplifier Using Continuous Class-E Modes Theory," accepted for presentation at *IEEE Radio Frequency Integrated Circuits Symposium*, Tampa, USA, June 2014.

[C] M. Özen, Mark P. van der Heijden, M. Acar, R. Jos, and C. Fager, "Wideband Combiner Synthesis for Class-E Outphasing Transmitters," *Manuscript*.

[D] M. Özen and C. Fager, "Symmetrical Doherty Amplifier with High Efficiency over Large Output Power Dynamic Range," accepted for presentation at *IEEE MTT-S International Microwave Symposium*, Tampa, USA, June 2014.

[E] M. Özen, R. Jos, C. M. Andersson, M. Acar, and C. Fager, "High-Efficiency RF Pulsewidth Modulation of Class-E Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol.59, no.11, pp.2931-2942, Nov. 2011

[F] M. Özen, C. M. Andersson, T. Eriksson, M. Acar, R. Jos, and C. Fager, "Linearization Study of a Highly Efficient CMOS-GaN RF Pulse Width Modulation Based Transmitter," *European Microwave Conference*, pp.136-139, Amsterdam, The Netherlands, Nov. 2012.

Other Publications

The following paper has been published but is not included in the thesis. The content partially overlaps with the appended papers or is out of the scope of this thesis.

[a] M. Schoukens, M Özen, C. Fager, M. Thorsell, G. Vandersteen, Y. Rolain, "Modeling a broadband Doherty power amplifier using a parallel Wiener-Hammerstein model," *The 33th Benelux Meeting on Systems and Control*, Heijen, The Netherlands, March 2014.

[b] C. Fager , D. Gustafsson, M. Özen, C. M. Andersson, M. P. van der Heijden, M. Acar, R. Jos, T. Emanuelsson, T. Wegeland, T. Eriksson, D. Kuylenstierna, "Efficient and Wideband Power Amplifiers for Wireless Infrastructure Applications," GigaHertz Symposium, Göteborg, Sweden, March 2014.

[c] S. Lai, D. Kuylenstierna, M. Özen, M. Hörberg, N. Rorsman, I. Angelov, H. Zirath, "Low Phase Noise GaN HEMT Oscillators With Excellent Figures of Merit," *IEEE Microwave and Wireless Components Letters*, no. 99, pp. 1-3, 2014.

[d] C. M. Andersson, M Özen, D. Gustafsson, K. Yamanaka, E. Kuwata, H. Otsuka, M. Nakayama, Y. Hirano, I. Angelov, C. Fager, N. Rorsman, "A packaged 86 W GaN transmitter with SiC varactor-based dynamic load modulation," *European Microwave Conference* , pp.136-139, Nürnberg, Germany, Nov. 2013.

[e] M. Özen and C. Fager, "Amplifier Apparatus and Method," *Patent application*, PCT/EP2013/071631, Oct. 2013.

[f] M. Özen, C. M. Andersson, M. Thorsell, K. Andersson, N. Rorsman, C. Fager, M. Acar, M. P. van der Heijden, R. Jos, "High efficiency RF pulse width modulation with tunable load network class-E PA," First place of best paper award, *IEEE Wireless and Microwave Technology Conference*, April 2011.

Abbreviations and Notations

Abbreviations

ACLR	Adjacent Channel Leakage Ratio
AD-PLL	All-Digital Phase-Locked-Loop
AWG	Arbitrary Waveform Generator
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DPD	Digital Pre-distortion
EER	Envelope Elimination and Restoration
GaN	Gallium Nitride
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
LTE	Long Term Evolution
LTE-A	Long Term Evolution Advanced
MIMO	Multiple Input Multiple Output
NMSE	Normalized Mean Square Error
OFDM	Orthogonal Frequency Division Multiplexing
OPBO	Output Power Back Off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PWM	Pulse Width Modulation
RBS	Radio Base Station
RF	Radio Frequency
RF-DAC	Radio Frequency Digital-to-Analog Converter
RF-PWM	Radio Frequency Pulse Width Modulation
SiC	Silicon Carbide
SiGe	Silicon Germanium
SMPA	Switch Mode Power Amplifier
W-CDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
ZVDS	Zero Voltage Derivative Switching
ZVS	Zero Voltage Switching

Notations

B	Susceptance
C	Capacitance
C_{out}	Output capacitance
d	Duty cycle
G	Conductance
i_D	Drain current waveform
i_S	Switch current waveform
I_{max}	Transistor maximum current capability
L	Inductance
n	Harmonic index
Q_L	Loaded quality factor
R	Resistance
R_{on}	Switch on resistance
U	Power utilization factor
v_D	Drain voltage waveform
v_S	Switch voltage waveform
V_{BR}	Breakdown voltage
V_{DD}	Drain bias
X	Reactance
ϵ_r	Relative dielectric constant
η	Drain efficiency
η_{tot}	Line-up efficiency
f	Frequency
f_{maxCE}	Class-E maximum operating frequency
I_{max}	Transistor maximum current capability
i_{Smax}	Maximum switch current
P_{out}	Output power
P_{peak}	Peak output power
θ	Outphasing angle
U	Power utilization factor
v_{Smax}	Maximum switch voltage
ω	Angular frequency
Z_n^S	Harmonic switch impedances

Contents

Chapter 1

Introduction

1.1 Motivation

Wireless technology is simplifying our daily life in an unprecedented way and also bringing in many new kinds of entertainment. Unlike the old days, we thereby do not need a cable connection to make a phone call or to access internet. Developments in screen technologies and processors has enabled advanced, data intense entertainment applications, like high quality video streaming, online video gaming etc., to be run even on handheld devices. Many new unconventional communication applications are also emerging in parallel to the fast development of the wireless technology. For instance, in remote health-care applications, biomedical signals captured from the patients body are directly transmitted to a hospital server for health monitoring [1]. Car-to-car communication systems is another example which has high potential to decrease number of accidents and to reduce traffic jams [2]. Wireless technology can also be used with smart lighting systems to control the city lights in a much more effective way to save energy [3].

In the past year 2013, the wireless data traffic has almost doubled compared to the year before. It is expected that this trend will continue and global mobile data traffic is predicted to grow more than 11-fold between 2013 to 2018 [4]. Surely an expanded use of mobile internet and rapid customer adoption of smart phones is the driving force behind this trend. A variety of techniques are now being explored to meet the demand for increased capacity and energy efficiency in future mobile wireless networks [5].

To cope with the demands for higher data rates, wireless providers has begun to introduce smaller cells in their networks. Densely populated areas, e.g. public transport hubs, shopping malls etc., are thereby served locally by small pico/femto cell base stations. Significant amount of mobile data traffic can thus be offloaded from the macro cell, resulting in higher data rates for the end user.

Another enabler to increase the mobile communication speed is to use multiple antenna systems, also known as multiple-input multiple-output (MIMO) systems. MIMO systems provide very high spectral efficiencies by simultaneously transmitting multiple independent data streams in the same channel [6]. MIMO technology is becoming mature and is already being used in current

and emerging wireless standards like Long-term Evolution (LTE) and LTE-Advanced (LTE-A). Currently, the number of antennas in MIMO systems are modest, where the most modern standard LTE-A allows using a maximum of 8 antennas. A new paradigm for MIMO systems that is now being intensively studied is to incorporate very large antenna arrays (hundreds to thousands of antennas), so called massive MIMO. In addition to benefits of conventional MIMO, the use of large antenna arrays enables the transmitted signal energy to be focused to the specific areas where the users are located. Thereby, great improvements in throughput and radiated signal efficiency is expected [7].

The traditional approach to increase the capacity is to allocate more spectrum. Several new wireless communication bands have therefore been made available to meet the rapidly growing demand for network capacity. For instance, in LTE standard, 44 different frequency bands are utilized within 700 MHz-3.5 GHz frequency range. At present, the available spectrum is shared in a static way, i.e. each operator is assigned to fixed bands. On the other hand, dynamic spectrum allocation techniques are emerging, which aim to utilize the spectrum in a more efficient and opportunistic manner [8]. Dynamic allocation is considered as one of the key technologies to meet the demands for higher capacity in a cost effective way. This would, however, inevitably require frequency agile wireless front end technology.

In summary, there are now several techniques that are being investigated to meet the demand for improved capacity in mobile wireless networks. Key technologies include the use of heterogeneous networks with small cells, base stations with many more antennas, and a wider range of frequency bands. Next, we will discuss the impact that these techniques have on the transmitter research needed.

1.2 Transmitters Demands

The largest operational cost for the cellular network providers is the electrical energy costs. In a mobile network infrastructure, radio base stations (RBS) consume most of the energy and thus also makes the highest contribution to the total CO_2 emission [9]. The transmitter unit, which is responsible for generation of high power information carrying electromagnetic radio frequency (RF) signal, is the most power hungry unit in a RBS. Further, the footprint and energy consumption of the power supply and cooling units also scales with the energy consumption of the transmitter unit. Therefore, increasing the efficiency of the transmitter unit can greatly reduce the overall energy consumption, size, manufacturing cost and environmental footprint of RBS units and the mobile network as a whole.

Consequently, energy efficiency has been the main drive parameter for radio transmitter research for many years. Much research has been done on efficiency enhancement techniques to reduce the energy consumption of transmitters when dealing with high peak-to-average power ratio (PAPR) modern communication signals [10]. Nowadays, due to increasing number of frequency bands used in the standards, transmitters that can maintain high energy efficiency over large RF bandwidths are further demanded. Such components reduce infrastructure manufacturers product diversity and thus cut the man-

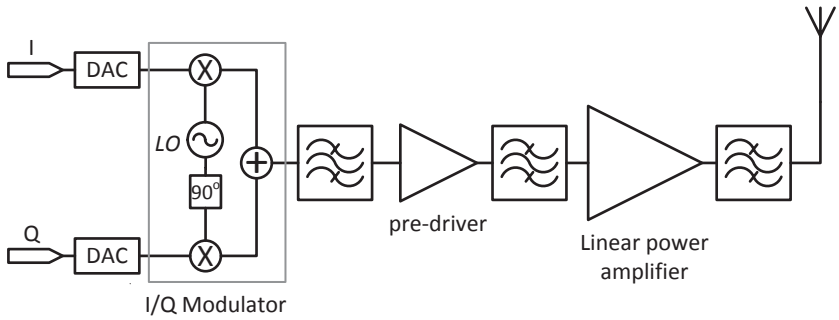


Figure 1.1: A simplified block diagram of conventional up-conversion transmitter architectures.

ufacturing costs significantly. In addition, implementation of the future infrastructure that supports dynamic spectrum allocation will not be possible without wide RF bandwidth transmitters.

Expanding deployments of small-cell and increasing number of antennas in base stations has increased the radio transmitter volumes drastically. The cost and integration are therefore also becoming very important parameters for transmitter modules. For instance, building a massive MIMO system with hundreds of antennas in a cost efficient way would not be possible without highly integrated, inexpensive transmitters.

In summary, energy efficient, frequency agile, highly integrated low cost transmitters are highly demanded for realization of future wireless infrastructures.

1.3 Digital Transmitters Architectures

A block diagram of conventional up-conversion transmitter is shown in Fig. 1.1. In such transmitters, base band signal processing is performed in the digital domain, whereas up-conversion and modulation are done in the analog domain. The digital baseband circuitry is nowadays implemented in low-voltage deep sub-micron CMOS processes, which often does not have any analog extensions. Use of deep sub-micron CMOS processes enables very high level of integration in digital circuitry, however it complicates implementation of the traditional analog circuits [11,12]. Hence, there has been a growing interest on architectural solutions for implementing RF functionalities using digital building blocks. Such solutions may enable integration of the RF signal generation chain into digital baseband processor of the transmitters, thus saving cost and footprint.

In digital-intense transmitter architectures, a switch mode power amplifier (SMPA) is used in conjunction with a digital modulator circuit. In single bit modulation schemes the amplitude information is encoded into pulse properties. The most commonly used 1-bit coding techniques are, $\Delta\Sigma$ modulation, carrier pulse width modulation (PWM) and RF pulse-width modulation (RF-PWM) [13]. A generic block-diagram of single-bit digital transmit-

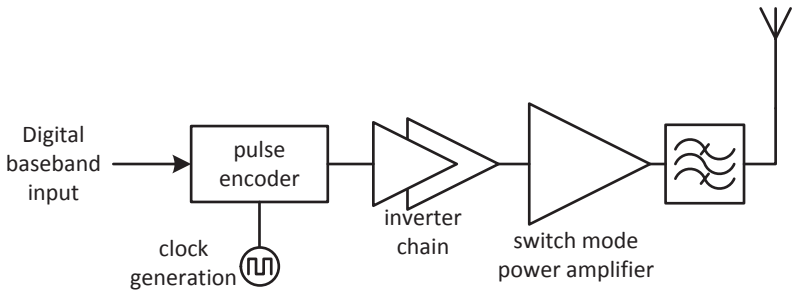


Figure 1.2: A generic block diagram for single-bit digital transmitter architecture.

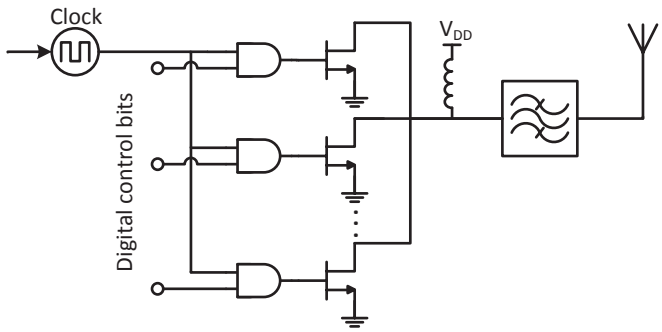


Figure 1.3: Multi-bit RF digital to analog converter (RF-DAC).

ter architectures is shown in Fig. 1.2. In multi-bit modulation schemes, the SMPA is operated as a multi-bit RF digital-to-analog-converter (RF-DAC). The output amplitude is thereby controlled by regulating the number of active transistors [14], see Fig. 1.3. In addition to these solutions, outphasing transmitter architectures also have interesting features from integration point of view. In outphasing transmitters, two phase modulated signals are post-PA combined for achieving amplitude modulation at the antenna. Using two all-digital phase locked-loops (AD-PLL) for signal generation and SMPAs for amplification, outphasing transmitters can be implemented using digital only blocks in CMOS technology [15].

In contrast to conventional transconductance based class-AB PAs, SMPAs theoretically provide 100% DC to RF conversion efficiency. However, when SMPAs are incorporated into a transmitter architecture, modulation involved typically violates the proper switch mode operation and thus the losses in them increases significantly. Therefore, in practice, when dealing with spectrally efficient high peak to average power ratio (PAPR) signals, the efficiency is much lower than the theoretical limit. Further, it is also challenging to maintain the efficiency of digital transmitters versus frequency due to inherent narrow band behavior of SMPAs.

In order to realize highly efficient, frequency agile, low cost digital transmitters, the losses in SMPAs associated with amplitude modulation and change of the operating frequency has to be well understood and addressed.

1.4 Thesis Contributions

This thesis focuses on the theory, design and practical realization of SMPAs that are compatible with digital transmitter architectures. New solutions at the device waveform-, circuit-, and transmitter level are presented which exploit the inherent high efficiency potential of SMPAs for realization of energy efficient, wide-band, highly integrated practical transmitters for wireless communication applications. Three distinct contributions are made to the field of SMPAs and digital transmitter architectures.

The first contribution is at transistor waveform level. Class-E is the best known SMPA due to its high efficiency and simple realization. In conventional well-established class-E analysis, an open circuit second harmonic load impedance is assumed for the transistor. In [Paper A], it is analytically shown that the high efficiency can actually be achieved for an arbitrarily selected second harmonic impedance. The derivation therefore reveals a continuum of novel class-E PA modes, enabling comprehensive waveform engineering for performance optimization in specific applications. Furthermore, the theoretical derivation provides important possibilities for wide-band SMPA synthesis. [Paper B] presents an experimental verification of the hypothesis in [Paper A] that the continuum can enable high efficiency operation over wide bandwidth. Upon studying the theory and design of wide-band highly efficient SMPAs, we will move towards energy efficient amplitude modulation of SMPAs over large RF bandwidths.

The outphasing transmitter architecture is considered as one of the promising candidates to meet transmitter demands [10]. Appealing efficiency numbers [16] and high level of integration [17] have been demonstrated with outphasing transmitters. However, maintaining high efficiency over a large RF bandwidth remains an open issue. The fundamental limiting factor is related to the narrow bandwidth of conventional Chireix outphasing combiners [18]. In [Paper C] a novel wide-band combiner design methodology is derived for SMPA based outphasing transmitters. The technique is based on the calculation of the combiner network parameters from the boundary conditions required for highly efficient switch-mode operation of the transistors in each branch. The combiner is then synthesized to realize the calculated network parameters across the band. A wide-band CMOS-GaN demonstrator is manufactured for experimental realization. As a side-track it is further shown in [Paper D] that the same theoretical approach can also be used for design of Doherty PA combiner networks.

We also studied the RF-PWM technique for energy efficient amplitude modulation of SMPAs. The main principle of RF-PWM is to vary the duty cycle (pulse width) of a carrier frequency pulse train according to the envelope of the signal. A challenge associated with RF-PWM architecture is however that conventional SMPAs (e.g. class-E, class-D) suffer from severe switching losses when amplifying RF-PWM signals. In [Paper E], a novel SMPA topology is derived that is particularly suitable for energy efficient amplification of RF-PWM signals. It is analytically shown that high efficiency can be maintained over a wide power dynamic range if the imaginary part of the class-E load impedance is varied along with the duty cycle. A 2 GHz CMOS-GaN RF-PWM transmitter demonstrator is constructed and characterized with realistic

communication signals to demonstrate the feasibility of the proposed technique [Paper F].

The solutions presented in this thesis will facilitate realizations of frequency agile, energy efficient and highly integrated/digitalized radio transmitters for future wireless communication systems.

1.5 Thesis Organization

This thesis is organized as follows: In Chapter II, theory and practical realization of switch mode power amplifiers is reviewed. Chapter III treats the theory of continuous class-E modes and its practical use. The theory and practical realization of wide-band class-E outphasing transmitters is treated in Chapter IV. Chapter V is devoted to tunable load network class-E PAs for energy efficient amplification of RF pulse width modulation signals. Finally, conclusions and future work are given in Chapter VI.

Chapter 2

Switch Mode Power Amplifiers

In digital transmitters, the SMPA unit mainly determines the overall efficiency and the RF bandwidth. A good understanding of SMPA operating principles is therefore key to successful design and realization of high performance digital transmitters.

In this chapter, fundamental operating principles of switch-mode PAs and the best known SMPA classes of operation, class-E,F, and D, will be reviewed. A special emphasis is given to class-E PAs since the contributions of this thesis strongly relate to them.

2.1 Power Amplifier Operating Modes

2.1.1 Transconductance Mode Power Amplifiers

In Fig. 2.1, the output voltage-current relation, I-V curve, of an idealized transistor is shown. In conventional linear PAs, the transistor device is operated in the active and pinch-off regions of the I-V curve as a voltage dependent

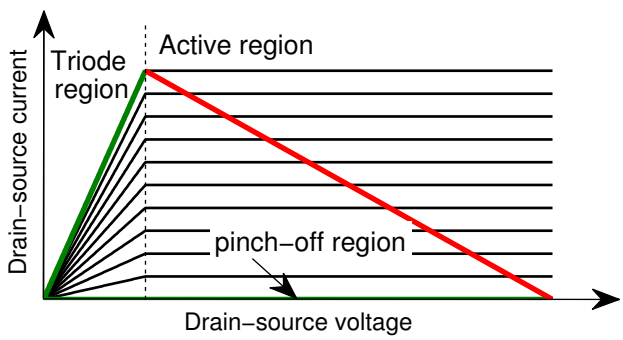
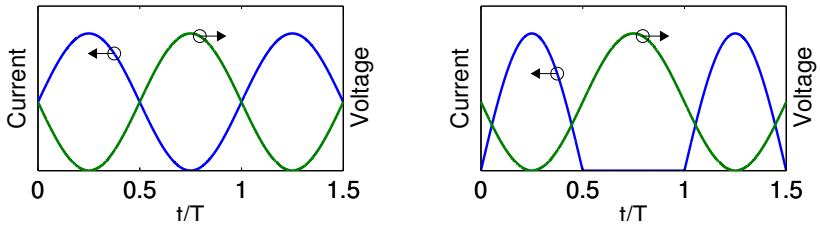


Figure 2.1: Example load lines for transconductance mode (red) and switch mode (green) power amplifiers.



(a) class-A (b) class-B

Figure 2.2: Drain waveforms of conventional transconductance based power amplifiers.

current source. This general mode of operation is referred as *transconductance mode*. Such an operation scheme may provide a good linearity, but will also yield simultaneously high voltage and large current. The power waste in a transistor due to voltage-current overlap follow as:

$$P_{loss} = \frac{1}{T}\int_{T} v_D(t) i_D(t) dt \tag{2.1}$$

where v_D and i_D are the drain voltage and current waveforms, respectively. The overlap between current and voltage drain/collector waveforms must therefore be minimized to get low losses and high efficiency.

The waveforms of PAs operating in the conventional transconductance modes class-A and class-B are shown in Fig. 2.2. These modes theoretically provide 50% and 78.5% drain efficiencies respectively, for an ideal transistor with zero knee-voltage.

2.1.2 Switch Mode Power Amplifiers

In switch-mode PAs, the transistor is operated in the triode and pinch-off regions. This results in a very low voltage-current overlap, see Fig. 2.1. SMPAs theoretically provide 100% efficiency for an ideal transistor with zero knee-voltage.

A simplified switching transistor model is shown in Fig. 2.3. R_{on} represents the device on-resistance corresponding to the triode region, while C_{out} represents the device output capacitance in the pinch-off region. In SMPAs, voltage-current overlap across R_{on} during the on-state of the switch is a major source of losses. The losses in R_{on} are given by:

$$P_{R_{on}} = \frac{1}{T}\int_{T} i_S^2(t) R_{on} dt \tag{2.2}$$

Discharge of the output capacitance C_{out} at the switching instances can also be a major loss source in SMPAs, especially at high frequencies. Capacitive power losses follow as

$$P_C = f_o \frac{1}{2} C_{out} V_{sw}^2 \tag{2.3}$$

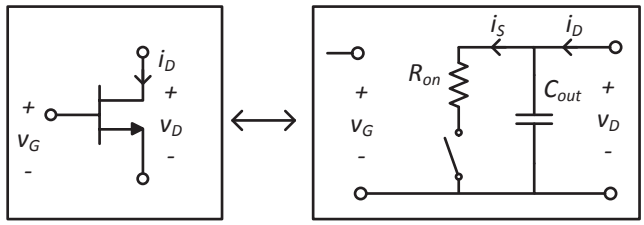


Figure 2.3: A simplified switching transistor model. R_{on} and C_{out} represent the on-resistance and output capacitance of the device respectively.

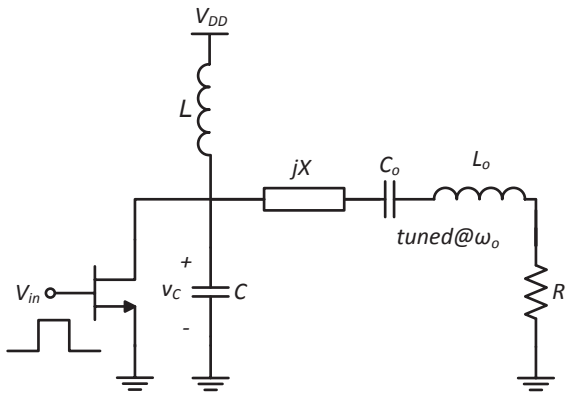


Figure 2.4: Schematic of class-E PAs.

where V_{sw} is the voltage across the output capacitor C_{out} at the turn-on moments of the switch and f_o is the operating frequency.

As seen from (2.2)-(2.3), the transistor losses in an SMPA depend on the device technology and the waveform shapes.

Different operating classes have been defined for SMPAs where each mode provides different waveforms. The best-known switch-mode classes of operation, class-E,F,D, will be reviewed in the next sections. Class-E PAs are studied more thoroughly since the work presented in this thesis strongly relate to them.

2.2 Class-E Power Amplifiers

Class-E is a single ended SMPA consisting of an active switching device and a load network to shape the switch waveforms, see Fig. 2.4. The load network is designed to satisfy the following switching conditions to ensure low switching losses [19]:

$$v_C(t)\Big|_{t=\frac{2\pi}{\omega_0}} = 0 \tag{2.4}$$

$$\frac{dv_C(t)}{dt}\Big|_{t=\frac{2\pi}{\omega_0}} = 0 \tag{2.5}$$

where $v_C(t)$ is the voltage across the capacitor C shown in Fig. 2.4. The condition given in (2.4) is named zero voltage switching (ZVS), which is meant to prevent losses due to discharge of capacitor C at off-to-on switching instances. The condition given in (2.5) is named zero voltage derivative switching (ZVDS). Note that, from Kirchhoff's current law, current through C is transferred to the switch at off-to-on transition instances. ZVDS is therefore necessary to prevent a high current to flow through an unsaturated transistor during transitions [20].

The series resonant filter in the load network, which is tuned at ω_o, is meant to suppress the harmonic currents. The reactive element X is therefore only effective for the fundamental tone.

Design of class-E PAs requires the circuit values $\{L, C, X, R\}$ to be calculated to satisfy the ZVS and ZVDS switching conditions. In the original work of Sokal, it is assumed that L in Fig. 2.4 has an infinite inductance and therefore only carries a DC component [19]. This assumption greatly simplifies the circuit analysis. However, it has later been shown that, class-E PAs with finite feed inductance gives much better design flexibility and also better performance.

In the following sections, first, design of conventional class-E PAs, so called class-E with RF-choke feed inductance, is treated. Next, design of class-E PAs with finite feed inductance is treated, following the historical development of the class-E theory.

2.2.1 Class-E Power Amplifiers with RF-choke Feed Inductance

A thorough analysis of class-E PAs with RF-choke feed inductance can be found in [21]. Here, only the results will be used to outline the design steps. The following assumptions made for the circuit analysis are however important to mention:

- The transistor is replaced with an ideal switch for the analysis, see Fig. 2.5. The switch has a zero on-resistance and infinite off-state resistance.

- Reactive elements are lossless and the only loss occur in the load resistance R.

- The current flowing through the load resistance is a pure sinusoid at the switching frequency. This assumption is valid only if the loaded quality factor (Q_L) of the series LC filter is infinite. The loaded quality factor is defined as $Q_L = \omega_o L_o/R$ where $\omega_o = 1/\sqrt{L_o C_o}$.

The switch duty cycle (d) is defined as the on-duration of the switch normalized to the RF period. Class-E PAs can in principle be realized at any switch duty cycle [21], but a duty cycle of 50% is conventionally used for easier drive signal generation, e.g. by using a sinusoidal input signal. According to the circuit analysis, the required C and X values at 50% switch duty cycle

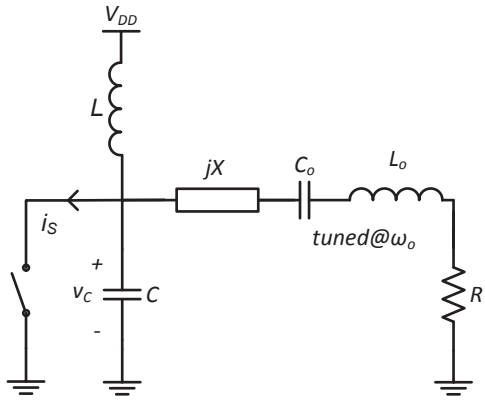


Figure 2.5: Idealized schematic of class-E PAs.

are given by:

$$C = \frac{0.1836}{\omega_o R} \tag{2.6}$$

$$X = 1.14R \tag{2.7}$$

The corresponding normalized switch waveforms are shown in Fig. 2.6.

The values of V_{DD} and R should be known for a complete design. The supply voltage V_{DD} should be determined considering that the maximum value of the switch voltage (v_{Cmax}) should not exceed the breakdown voltage (V_{BR}) of the device. From the analysis of class-E v_{Cmax} is determined as:

$$v_{Cmax} = 3.56V_{DD} \tag{2.8}$$

The load resistance R is dependent on output power level and V_{DD}:

$$R = 0.58\frac{V_{DD}^2}{P_{out}} \tag{2.9}$$

It is also important to know the maximum value of the switch current (i_{Smax}) to determine the required transistor size. The expression for i_{Smax} is given by

$$i_{Smax} = 1.66\frac{V_{DD}}{R} \tag{2.10}$$

Alternatively the load resistance R also can be determined to maximize the output power for a given device size using (2.10).

The values of L_o and C_o can be calculated using the selected Q_L value. As mentioned previously, the circuit analysis assumes that no harmonic current flows through the load resistance. Higher values of Q_L will therefore better approximate the ideal waveforms. In practice, Q_L values in the order of $10-20$ already yield almost ideal waveforms [22].

The power utilization factor (U) quantifies the maximum output power for given device current and breakdown voltage, and is for an ideal RF choke feed

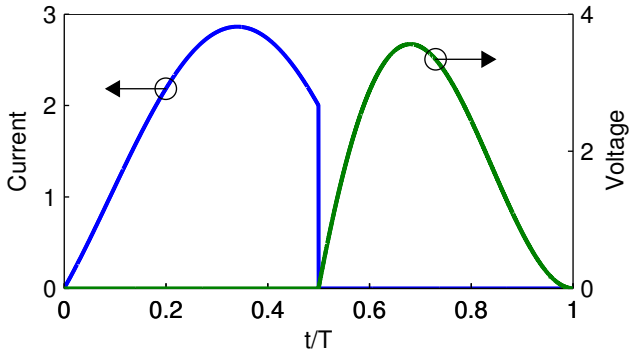


Figure 2.6: Normalized conventional class-E voltage, v_C/V_{DD}, and current, i_S/I_o, waveforms.

class-E PA given by:

$$U = \frac{P_{out}}{v_{Cmax} i_{Smax}} = 0.0981 \tag{2.11}$$

In practice, if the required C is smaller than the device output capacitance C_{out}, class-E mode can not be realized. This fact sets a maximum limit for the operating frequency (f_{maxCE}):

$$f_{maxCE} = 0.063 \frac{I_{max}}{C_{out} V_{BR}} \tag{2.12}$$

where I_{max} is the maximum current capability of the device. Observe that, f_{maxCE} is independent of the device size and is therefore universal for a given device technology.

2.2.2 Class-E Power Amplifiers with Finite Feed Inductance

Since Sokal introduced the class-E concept [19], different variants have been proposed to improve the performance in terms of maximum operating frequency and power utilization factor. The best known variants are even harmonic resonant and parallel circuit class-E PAs. In even harmonic resonant class-E, it is assumed that the feed inductor resonates out the capacitor C at an even harmonic of the carrier frequency, i.e. $2n\omega_o = 1/\sqrt{LC}$, where n is a positive integer number [23]. The values of $\{C, X, R\}$ are then calculated to satisfy the switching conditions. In parallel circuit class-E, the component X is assumed to be a short circuit [24] and required values of $\{C, L, R\}$ are calculated.

Design equations and performance of class-E variants, including the conventional solution, are summarized in Table 2.1. As seen from the table, even harmonic resonant class-E has the highest f_{maxCE} though the lowest U. Parallel circuit class-E has the highest U and provides 1.75 times higher f_{maxCE} than class-E with RF-choke.

Table 2.1: Summary of design formulas and performance figure of merits for different class-E variants. $\bar{f}_{maxCE} = f_{maxCE}/(\frac{I_{max}}{C_{out}V_{BR}})$

	Conventional [21] RF-Choke	parallel circuit [24]	even harmonic [23] resonant ($n = 1$)
q	0	1.412	2
$\omega_o RC$	0.1836	0.685	0.071
X/R	1.14	0	-4.903
v_{Smax}/V_{DD}	3.56	3.65	3.78
i_{Smax}/I_o	2.86	2.65	3.99
RP_{out}/V_{DD}^2	0.58	1.365	0.056
f_{maxCE}	0.063	0.11	0.191
U	0.0981	0.1036	0.066

In Table 2.1, the term q denotes the normalized resonant frequency of the circuit formed by parallel connection of feed inductance L and C, see Fig. 2.4:

$$q = \frac{1}{\omega_o\sqrt{LC}} \tag{2.13}$$

2.2.3 Generalized Class-E Design Equations

In [25], Acar *et al.* proved that the class-E switching conditions can actually be satisfied for arbitrary values of q. The derived design equations and the waveform expressions have the following forms:

$$C = \frac{1}{\omega_o R}K_C(d,q) \tag{2.14}$$

$$X = RK_X(d,q) \tag{2.15}$$

$$R = \frac{V_{DD}^2}{P_{out}}K_P(d,q) \tag{2.16}$$

$$v_C(t) = V_{DD}v(d,q,t) \tag{2.17}$$

$$i_S(t) = \frac{V_{DD}}{R}i(d,q,t) \tag{2.18}$$

where the functions $\{K_C, K_X, K_P, v, i\}$ can be found in [25], and also in [Paper E, Section III][1]. The variable d represents the switch duty cycle, e.g. $d = 1$ corresponds to 100% duty cycle. Examples of normalized switch waveforms for different q values are shown in Fig. 2.7.

Free selection of q gives extra flexibility for the design, where its optimal value is dependent on the design considerations. For instance, q can be selected to maximize the power utilization factor yielding minimum possible device size for a given output power level. The power utilization factor is plotted versus q in Fig. 2.8 and is maximum at approximately $q = 1.5$. Once q is known,

[1] The equations derived in [Paper E] have an extra independent variable k to parameterize the voltage slope at off-to-on instances, k must therefore be set to zero to achieve (2.14)-(2.18)

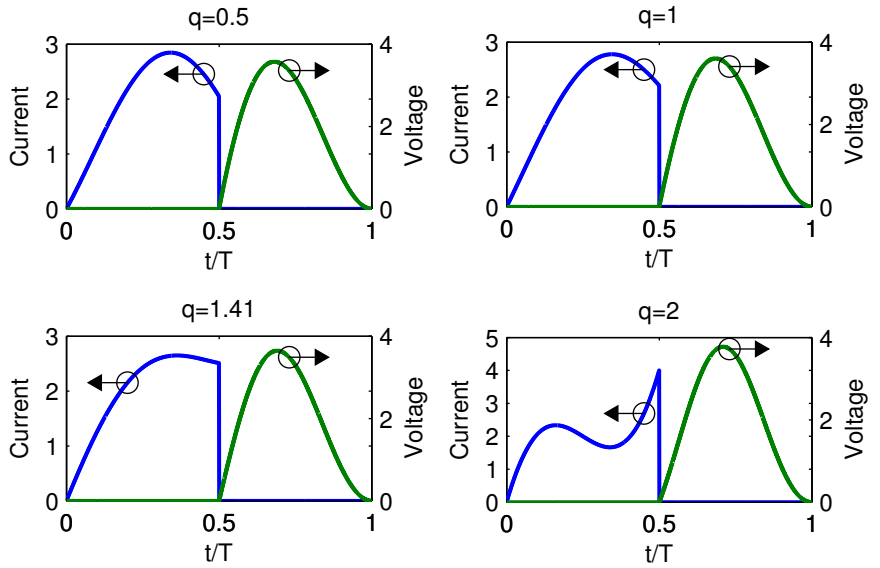


Figure 2.7: Normalized voltage and current waveforms, v_C/V_{DD} and i_S/I_o respectively, for different q values.

V_{DD} can be determined from (2.17) considering that the maximum value of v_C should not exceed the switch breakdown voltage. Values of C, X, R and L are found by using (2.14)-(2.16) and (2.13), respectively.

It may also be desirable to fully absorb C by the device output capacitance C_{out} for a minimum complexity of the load network realization. This implies $C = C_{out}$ and allows q, V_{DD} and R to be solved from (2.14),(2.16) and (2.17). The remaining circuit element values X and L are then easily calculated using found values of q and R.

It is useful to know values of f_{maxCE} versus q for a specific technology. The corresponding expression of f_{maxCE} is easily derived using (2.14)-(2.18):

$$f_{maxCE} = \frac{K_C v_{Cmax}}{2\pi R i_{Smax}} \frac{I_{max}}{V_{BR} C_{out}} \tag{2.19}$$

Note that, the first term in the expression on the right hand side depends purely on q and the second on the device technology parameters. Normalized f_{maxCE} is plotted versus q also in Fig. 2.8. As seen from the figure, although both f_{maxCE} and U increase until approximately $q = 1.5$, there is a compromise between them for higher q values.

So far the theory of class-E PAs and its well-known variants has been reviewed. In the next section, their practical realization at GHz frequencies will be discussed.

2.2.4 Class-E at Microwave Frequencies

At microwave frequencies, the effect of parasitics in real capacitors and inductors become quite significant. Real components therefore exhibit non-ideal

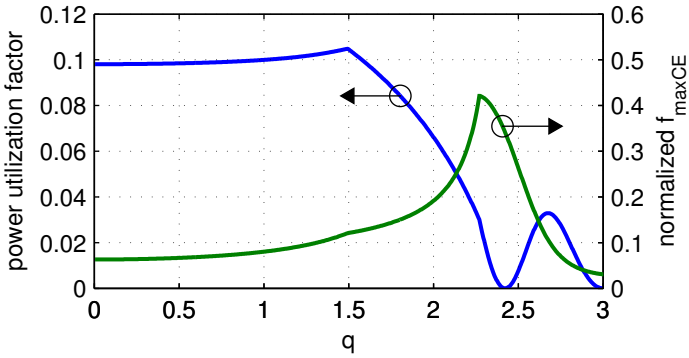


Figure 2.8: Power utilization factor and f_{maxCE} normalized with device technology factor ($I_{max}/V_{BR}C_{out}$) versus q at 50% duty cycle.

frequency responses. As an example, realization of the tuned LC filter seen in the ideal schematic of class-E PAs is therefore not very practical at microwave frequencies. In addition, the package and intrinsic device parasitics significantly influence the impedance levels at microwave frequencies. Their effect therefore has to be compensated for during the design, thus further complicating the realization of ideal lumped-element class-E load networks.

In practical microwave class-E PAs, the load network is therefore designed to provide a finite number of necessary harmonic impedances and is often realized using transmission line networks. For the conventional class-E case, the fundamental tone switch impedance is equal to a parallel connection of the impedances $1/(j\omega_o C)$ and $R + jX$. The higher order harmonic impedances are provided by the capacitor C. The necessary class-E harmonic loading conditions then follow as:

$$Z_n^S = \begin{cases} (1.52 + j1.11)R, & n = 1 \\ -j5.45R/n, & n > 1 \end{cases} \tag{2.20}$$

where n represents the harmonic index, see also Fig. 2.9. Harmonic loading conditions of other class-E variants can be calculated in a similar way.

Raab has theoretically shown that, for the conventional class-E mode, the fundamental tone and second harmonic switch impedances mainly determine the efficiency and output power [26]. Simulations with realistic device models also show that control of third and higher harmonic impedances only slightly change the efficiency in class-E PAs [27]. Therefore, in practical RF class-E realizations, typically only the fundamental tone and second harmonic impedances are controlled to achieve a good complexity-performance trade-off.

2.3 Class-F Power Amplifiers

Class-F is another type of a single ended switch-mode PA. In class-F PAs even and odd harmonics are terminated with short and open circuits respectively by using multiple resonators in the load network, see Fig. 2.10(a). In this way, the voltage and current waveforms are shaped towards a square wave and

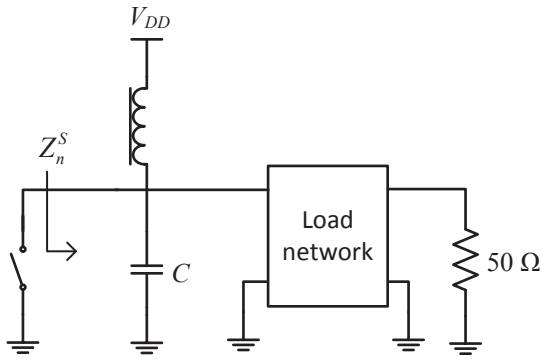


Figure 2.9: A generic single ended switch mode power amplifier schematic. Term Z_n^S denotes the impedance provided by the load network at $n\omega_o$, where n is the harmonic index.

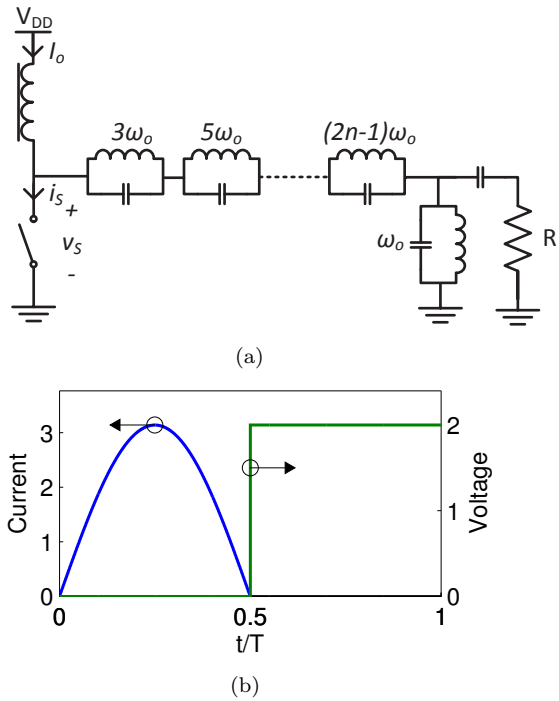


Figure 2.10: (a) Schematic of a class-F PA. (b) DC normalized ideal class-F voltage (v_S) and current (i_S) waveforms.

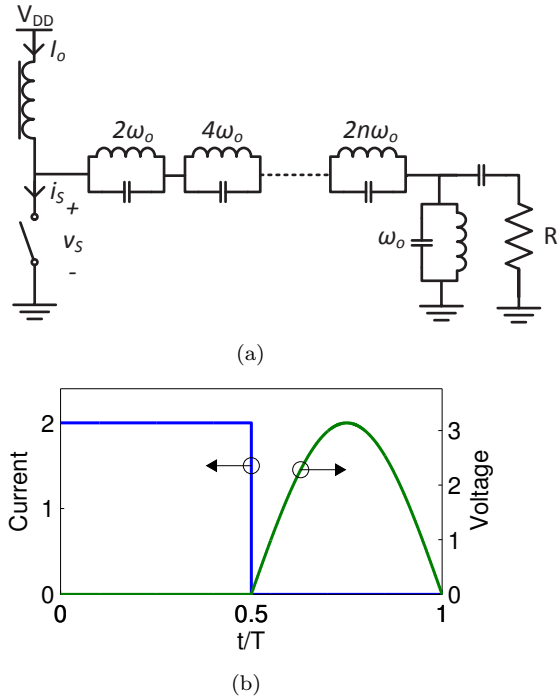


Figure 2.11: (a) Schematic of an Inverse class-F PA. (b) DC normalized ideal inverse class-F voltage (v_S) and current (i_S) waveforms.

a half-wave rectified sinusoid, respectively, see Fig. 2.10(b). The flat voltage waveform of class-F PAs results in a very high power utilization factor (0.159), which is 27% higher than that of the class-A mode (0.125). On the other hand, the voltage waveforms do not satisfy the ZVS condition, which may cause high switching losses at microwave frequencies.

Realization of ideal class-F waveforms require an infinite number of resonators in the load network. Therefore, in real applications, only an approximation of the ideal waveforms can be realized. Typically, controlling up-to 3^{rd} harmonic gives a good complexity-performance trade off for class-F PAs [26, 28].

2.4 Inverse Class-F Power Amplifiers

Inverse class-F mode (class-F^{-1}) is dual of class-F, where the voltage and current waveforms are interchanged, see Fig. 2.11(b). Class-F^{-1} operation requires even and odd harmonics to be terminated with open and short circuits respectively. Class-F^{-1} mode also provides a power utilization factor of 0.159. As seen from Fig. 2.11(b), class-F^{-1} mode satisfies the ZVS condition in contrast to class-F mode, which is an advantage for achieving high efficiency operation at microwave frequencies. In fact, comparative studies in the literature shows that, in practical RF SMPAs, the class-F^{-1} tuning scheme provides superior efficiency compared to the class-F tuning [28, 29].

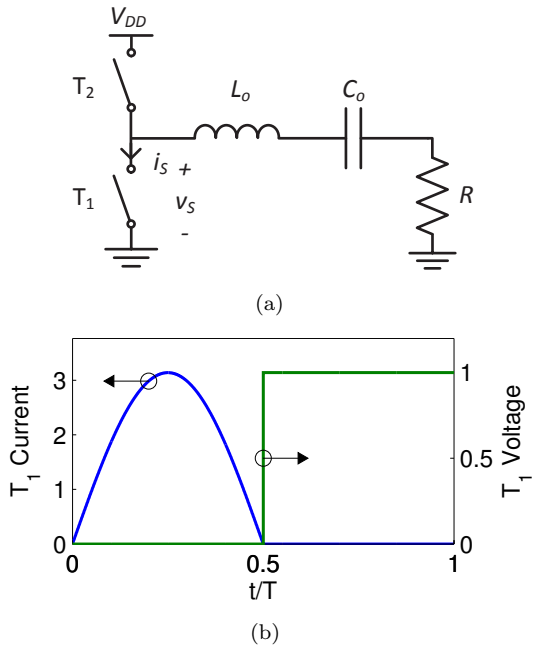


Figure 2.12: (a) Schematic of a class-D PA. (b) DC normalized class-D voltage (v_S) and current (i_S) waveforms.

It is worth mentioning that, in general, due to the lack of a simple circuit implementation, class-F and class-F^{-1} PAs are not preferred at frequencies where a lumped element class-E realization is possible.

2.5 Class-D Power Amplifiers

Class-D amplifiers consist of a pair of active devices that operate in push-pull mode and a tuned series LC filter that is connected in series with the load, see Fig. 2.12(a). In a class-D PA the drain node v_S is clamped to V_{DD} during half of the RF period and to the ground for the other half of the period. The switch voltage waveform v_S should therefore be a square wave. Ideally, the tuned filter will force a purely sinusoidal current through the load, i.e. when the Q of the filter is infinitely large. During half a period, the load current will complete its path through the switch that is in the on-state. Hence, a half-rectified sinusoidal current should flow through the switches. The ideal Class-D switch waveforms are shown in Fig. 2.12(b), which are the same as the ideal class-F waveforms. The class-D therefore also provides a power utilization factor of 0.159.

Studying frequency domain characteristics of the class-D may explain why the waveforms are same as class-F waveforms. In a class-D PA, the switches experience short terminations at the even harmonics due to push-pull operation of the active switches. The odd harmonic impedances, on the other hand, are set to open circuit by the tuned LC filter. The devices in a class-D PA

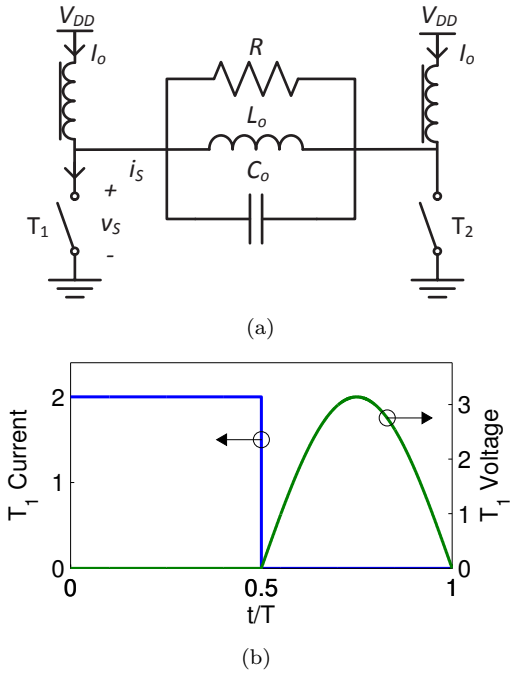


Figure 2.13: (a) Schematic of an inverse class-D PA. (b) DC normalized inverse class-D voltage (v_S) and current (i_S) waveforms.

in fact experience class-F harmonic loading conditions. Class-D is therefore considered as push-pull counter-part of class-F PAs. The main advantage of class-D realization is that it requires only one resonator circuit for harmonic filtering/tuning. On the other hand, Class-D requires two active devices that are operated in the push-pull mode.

Class-D is not very suitable for high frequency RF applications since its voltage waveform does not satisfy the ZVS condition. However, at low frequencies, it offers attractive possibilities for achieving high power and high efficiency without generating excessive voltage swings [30, 31].

2.6 Inverse Class-D Power Amplifiers

A schematic of inverse class-D (class-D^{-1}) is shown in Fig. 2.13(a). In class-D^{-1} PAs, a floating load is connected between the drain terminals of a differential switch-pair. A parallel LC tuned filter is connected in shunt to the load resistance for harmonic filtering. Ideally, the filter behaves as an open circuit at the carrier frequency and act as a short circuit at the harmonics of the carrier. During half a period, DC currents that flow through the RF chokes will combine into the switch that is at the on-state. The current waveforms should therefore be square shaped. The tuned filter will enforce a sinusoidal current through the load resistance. The differential voltage waveform between the drain terminals should thus be a sinusoidal signal. During half a cycle, the on-state switch will hold zero voltage across it, while the off-state switch will

experience half of a sinusoid. The voltage waveform across the devices should therefore be half-rectified sinusoidal signals. Ideal class-D^{-1} drain waveforms are shown in Fig. 2.13(b), which are the same as the class-F^{-1} waveforms. It can easily be shown that the switches in a class-D^{-1} PA experience class-F^{-1} loading conditions.

The class-D^{-1} voltage waveforms satisfy the ZVS condition and its flat current waveform yields a very high power utilization factor (0.159). The class-D^{-1} is therefore very suitable for realization of high output power, highly efficient RF SMPAs [32–35]. Further, the class-D^{-1} also provides important possibilities for wide-band SMPA realizations [36]. In a class-D^{-1} PA, the switches ideally experience open terminations at the even harmonics due to push-pull operation of the active switches. This simplifies the second harmonic control versus frequency. At high frequencies, the output capacitances tend to behave as short-circuits and provides nearly-optimal third harmonic impedances for the switches. Realization of the optimal harmonic impedances versus frequency is thus relatively easy for the class-D^{-1}, making it preferable for wide-band applications.

2.7 Summary and Discussion

In this chapter, fundamental operating principles of switch-mode PAs and the best known SMPA classes of operation have been reviewed. Each operation mode requires a certain set of harmonic drain terminations, where the fundamental tone and second harmonic impedances are the most important for the performance.

Operation modes that satisfy ZVS condition (class-E, class-F^{-1}, class-D^{-1}) are advantageous for achieving high efficiency at microwave frequencies. In the next chapter, a continuum of novel ZVS-ZVDS power amplifier modes will be presented, significantly extending the known SMPA design space.

Chapter 3

Continuous Class-E Power Amplifier Modes

As discussed in the previous chapter, development of the class-E theory essentially boils down to finding different combinations of component values $\{L, C, X, R\}$ that satisfy the switching conditions. In this chapter, a new dimension is brought to the class-E theory and the design space is thereby significantly extended.

The outline of the chapter is as follows: First, a continuum of novel class-E modes will be presented, which are analytically derived in [Paper A]. Next, two applications of the new theory will be discussed. These are RF waveform engineering for further efficiency improvement of SMPAs and wide-band SMPA design. Finally, experimental results of a watt-level 1.3-2.2 GHz SiGe BiCMOS continuous class-E modes PA demonstrator will be presented.

3.1 Continuous Class-E Modes Theory

Harmonic switch loading conditions of conventional class-E PAs were calculated in the previous chapter as:

$$Z_n^S = \begin{cases} (1.52 + j1.11)R, & n = 1 \\ -j5.45R/n, & n > 1 \end{cases} \tag{3.1}$$

where n represents the harmonic index. Note that, Z_n^S denote the necessary impedances at the switch reference plane, see Fig. 3.1.

Recently, there have been studies on manipulation of the harmonic switch impedances of class-E PAs in order to further improve the performance in terms of the efficiency and the output power. For class-E PAs, the second harmonic switch impedance Z_2^S has the highest impact on the performance among the harmonic impedances [26]. In [37], Z_2^S is set to an open circuit and it was assumed that the higher order harmonics are terminated with the capacitance C. The complex fundamental tone switch impedance and the value of C are thereafter calculated to satisfy the switching conditions. The resulting operation mode was named class-E/F$_2$ since Z_2^S is manipulated to

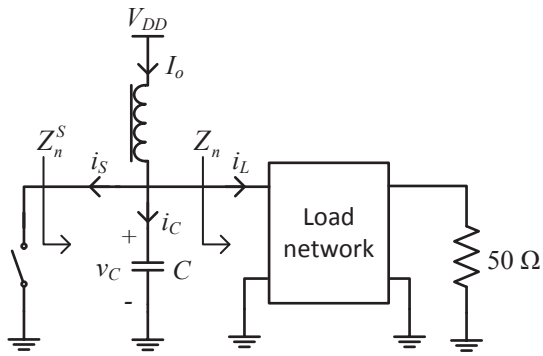
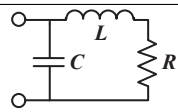
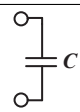
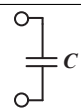
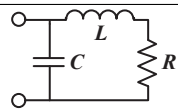
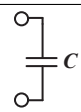
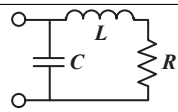
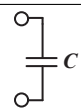
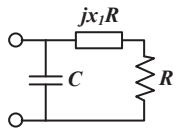
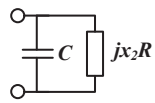
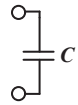


Figure 3.1: Generic single ended switch mode power amplifier schematic. Term Z_n denotes the impedance provided by the load network at $n\omega_o$, where n is the harmonic index.

Table 3.1: Impedance tuning specifications for different class-E variants

	ω_o	$2\omega_o$	$n\omega_o$, $n > 2$
Class-E [21]			
Class-E/F$_2$ [37]		**open-circuit**	
Class-EF$_2$ [38]		**short-circuit**	
Continuous class-E			

that of the class-F^{-1} mode. Kaczmarczyk introduced the class-EF_2 concept in [38]. It was shown that the class-E switching conditions can also be satisfied when Z_2^S is set to a short circuit.

In [Paper A], a generalized analysis of class-E is presented. It is analytically shown that the class-E switching conditions can be satisfied for an arbitrarily selected reactive second harmonic switch impedance. The derivation therefore reveals a continuum of novel class-E PA modes, where the class-E, class-EF_2 and class-E/F_2 become subsets of the continuum, see also Table 3.1. The results of the analysis in [Paper A] are summarized in the next section.

Cripps *et al.* have previously shown that class B efficiency can be maintained over a continuum of solutions by utilizing appropriate reactive second harmonic impedances [39,40]. The continuous class-E modes theory can therefore be seen as switch-mode counterpart of Cripps' theory on the continuous transconductance PA modes.

3.1.1 Design Equations and Waveforms

The analysis in [Paper A] is done by referring to the generic SMPA schematic shown in Fig. 3.1. The following assumptions are made for the circuit analysis:

1. The switch is on during $0 \leq t < \pi/\omega_o$ and off during $\pi/\omega_o \leq t < 2\pi/\omega_o$.

2. The switch is lossless, i.e. it has a zero on-state resistance and infinite off state resistance.

3. The load matching network shown in Fig. 3.1 consists of only reactive lossless passive components.

4. The load matching network provides a fundamental impedance of $Z_1 = (1 + jx_1)R$ and second harmonic impedance of $Z_2 = jx_2R$. Higher order harmonic impedances are open circuited: $Z_n = \infty$, $n > 2$.

Note that assumptions 1-3 are made also for the analysis of conventional class-E PAs, see Chapter 2. The novelty of the derivation is thus revealed by the last assumption $Z_2 = jx_2R$. This is in contrast to the conventional analysis where Z_2 is set to infinity.

The circuit design parameters, i.e. expressions of $\{x_1, x_2, C\}$, are derived as functions of only one independent variable, ϕ_1, which denotes the phase of the fundamental tone load current. The design equations therefore reveal continuous class-E solutions, which are expressed as functions of ϕ_1, noting that $\phi_1 = 57.5^o$ corresponds to the conventional class-E solution. The circuit design parameters are given by:

$$x_1(\phi_1) = \frac{16\pi \cos^2\phi_1 \cot\phi_1 + 2\pi \sin 2\phi_1 + 3\pi^2 - 32}{12\pi \cos^2\phi_1} \tag{3.2}$$

$$x_2 = \frac{\pi \sec^2\phi_1}{24(\pi - 2\tan\phi_1)}\Big[4\sin\left(2\tan^{-1}(2\cot\phi_1)\right) + 3\pi + 2\Big(\cos\left(2\tan^{-1}(2\cot\phi_1)\right) - 2\Big)\tan\phi_1\Big] \tag{3.3}$$

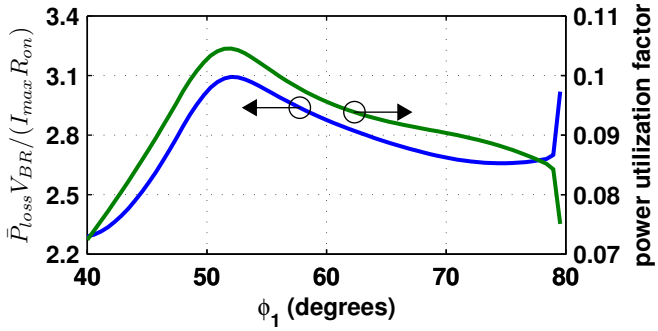


Figure 3.2: Normalized ohmic losses, $\bar{P}_{loss}V_{BR}/(I_{max}R_{on})$, and power utilization factor, both versus ϕ_1.

$$C = \frac{2}{\pi\omega_o R}\cos^2\phi_1 \tag{3.4}$$

The switch current and voltage expressions have also been derived as functions of ϕ_1:

$$i_S(t) = \frac{V_{DD}}{R}\frac{4}{\pi^2}\Big[\cos\phi_1\Big(\pi\cos\left(2\omega_o t - \tan^{-1}(2\cot\phi_1)\right)\sqrt{1+4\cot^2\phi_1} - 4\sin 2\omega_o t\Big) - \pi\cos(\omega_o t+\phi_1) + 4\sin\phi_1\sin^2\omega_o t\Big]\sin\phi_1 \tag{3.5}$$

$$v_C(t) = \frac{V_{DD}}{\pi}\tan\phi_1\big[4\omega_o t\tan\phi_1 + (4\pi\cot\phi_1 - 8)\sin^2\omega_o t - 2\pi\sec\phi_1\sin(\omega_o t+\phi_1) + (\pi - 2\tan\phi_1)\sin 2\omega_o t - 6\pi\tan\phi_1\big] \tag{3.6}$$

The RF output power is given by:

$$P_{out} = \frac{V_{DD}^2}{R}\frac{8\sin^2\phi_1}{\pi^2} \tag{3.7}$$

The power utilization factor, U, is plotted versus ϕ_1 in Fig. 3.2. Solutions achieved with $\phi_1 \in [43^o, 78^o]$ give U values comparable to that of the conventional class-E ($U = 0.0981$). This proves that the output power achieved with the continuous class-E modes can be maintained high over a wide range of solutions.

Using (3.2)-(3.4), the continuous class-E modes switch impedances $Z_n^S(\phi_1)$, see Fig. 3.1, are found as:

$$Z_1^S(\phi_1) = R\frac{(1+jx_1)\pi}{\pi + j2(1+jx_1)\cos^2\phi_1} \tag{3.8}$$

$$Z_2^S(\phi_1) = R\frac{j\pi x_2}{\pi - 4x_2\cos^2\phi_1} \tag{3.9}$$

$$Z_n^S(\phi_1) = -jR\frac{\pi}{2\cos^2\phi_1} \qquad n > 2 \tag{3.10}$$

In Fig. 3.3, Z_1^S and Z_2^S are plotted for $\phi_1 \in [43^o, 78^o]$ and a fixed output power level. As seen from the figure, the continuous class-E modes theory

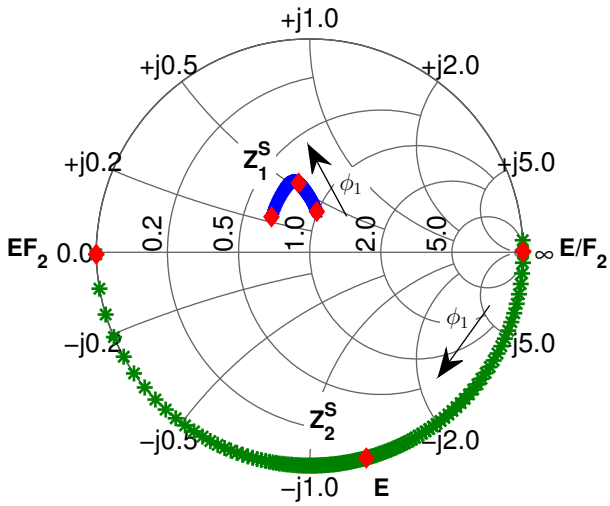


Figure 3.3: Fundamental tone and second harmonic switch impedances, Z_1^S and Z_2^S respectively, versus ϕ_1. The graphs are generated by assuming that $\Re\{Z_1^S|_{\phi_1=43^o}\} = 50\ \Omega$, i.e. the reference impedance of the Smith diagram. The output power is kept constant over the solution range used, $\phi_1 \in [43^o, 78^o]$. Red diamond markers ($\diamond$) represent the switch impedances for class-E/F_2, E, EF_2 modes.

significantly extends the impedance design space of ZVS/ZVDS SMPAs. The extended design space provides important possibilities for further efficiency improvement of SMPAs and wide-band SMPA design. These two distinct applications of the continuous class-E modes theory are discussed next.

3.2 RF Waveform Engineering

For a given device technology, the switch waveforms determine the SMPA efficiency. In Fig. 3.4, continuous class-E modes switch waveforms are shown for different ϕ_1 values. As seen from the figure, by changing ϕ_1 the switch waveforms can be shaped differently for performance optimization in specific applications.

In SMPAs, current through R_{on} during the on-state of the switch is a major loss source as mentioned previously. Although R_{on} is not accounted for in the analysis made in [Paper A], its losses can be calculated approximately by using the ideal waveform expressions given by (3.5)-(3.6) [41]. The expression of normalized losses in R_{on} then follows as:

$$\bar{P}_{loss} = \frac{i_{Srms}^2 R_{on}}{P_{out}} = \frac{i_{S-rms}^2 \max(v_C)}{P_{out} \max(i_S)} \frac{I_{max} R_{on}}{V_{BR}} \tag{3.11}$$

where I_{max} is the maximum current capability of the device and V_{BR} is the breakdown voltage. Note that, the first term in the expression on the right hand side depends purely on ϕ_1 while the second terms depends on the device

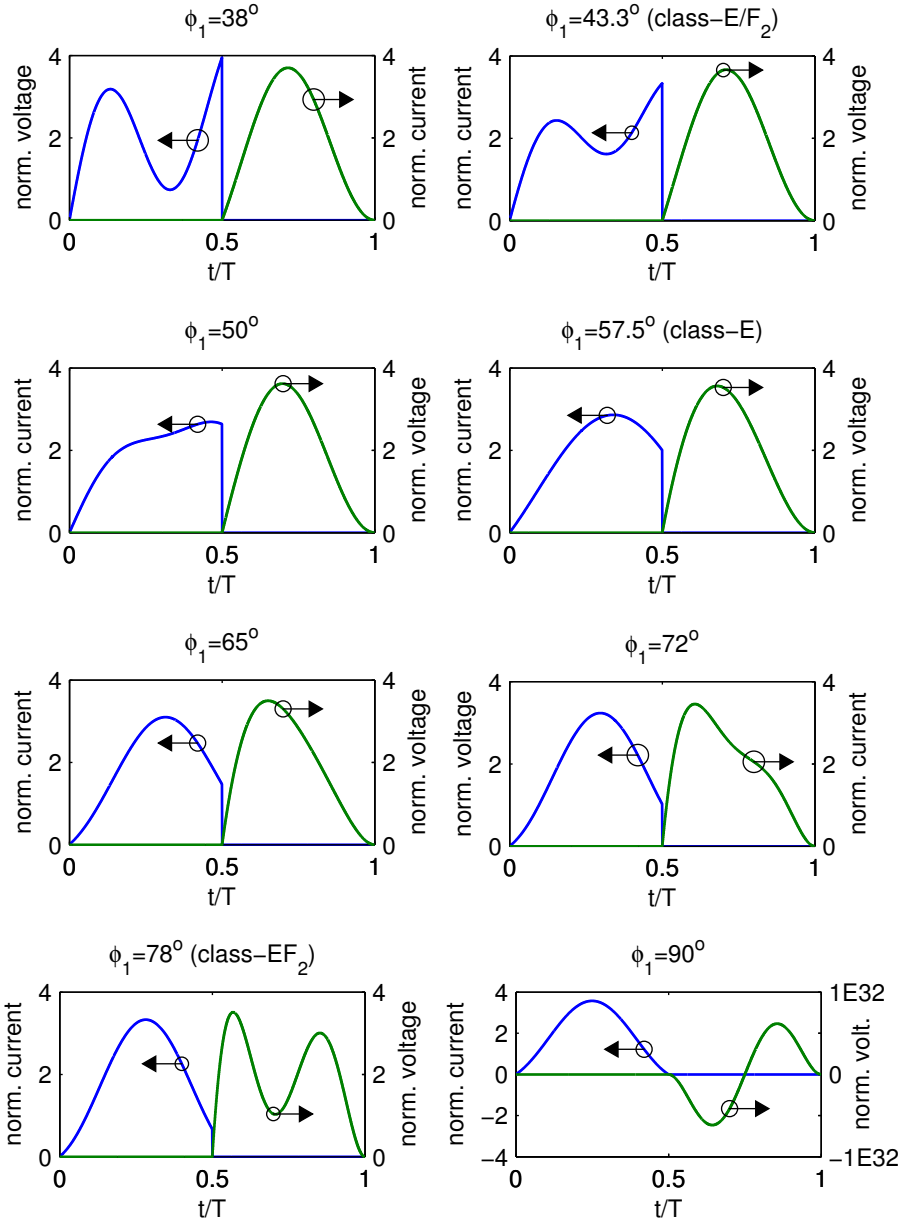


Figure 3.4: DC normalized switch current, i_S/I_o, and voltage, v_C/V_{DD}, waveforms for different ϕ_1 values. Time is normalized with the period (T).

technology. Variation of $\bar{P}_{loss}$ versus ϕ_1 is also shown in Fig. 3.2. As seen from the figure, there is a compromise between the output power and the normalized ohmic-losses.

For the conventional class-E case, the switch current makes a large jump at on-to-off switching instances, see the waveforms for $\phi_1 = 57.5^o$. This large current jump, especially if a slow switching transistor is used, may cause a high voltage-current overlap during switching transitions. Telegdy *et. al* proposed the class-E_M PA concept to address this issue [42]. In that case, using an auxiliary PA, a second harmonic current is actively injected to the class-E PA. In that way, the current waveform is shaped for zero current switching (ZCS) at the turn off moments of the switch. However, the use of an auxiliary PA costs extra DC power and increases circuit complexity dramatically. For the presented continuum, by proper selection of ϕ_1, the current waveform can actually be optimized for a relatively lower switch current at the turn off moments, see the waveforms for $\phi_1 = 72^o$, better tolerating a slow switching speed.

Observe that the solution given with $\phi = 90^o$ satisfies ZCS at the turn off moment of the switch. However, the peak value of the resulting voltage waveform tends to infinity for that solution yielding zero output power. In fact, this property for SMPAs was proven theoretically by Kazimierczuk in [43]. It was shown that ZVS, ZVDS and ZCS can not be simultaneously satisfied at a finite output power level with a passive load network.

Another application of the continuous class-E modes theory is wide-band SMPA design, which is discussed next.

3.3 Wide-band SMPA Design

In an SMPA design, to achieve a good efficiency-bandwidth performance, at least the necessary fundamental tone and the second harmonic load impedances has to be provided versus frequency. For instance, in class-F^{-1} SMPA designs, a purely resistive fundamental tone impedance and an open circuit second harmonic impedance has to be provided at the switch reference plane across the band. Similarly, for a wide-band class-E design a complex fundamental tone and a fixed capacitive second harmonic load impedances have to be provided versus frequency.

In wide-band SMPA designs, the fundamental tone impedance may be kept fixed over wide bandwidths by incorporating multi-section low pass filters in the load networks [44], [45]. However, the input impedance of these kinds of filters vary very sharply outside of their pass bands, making it very difficult to provide a fixed second harmonic impedance [44]. This, therefore, limits the achievable bandwidth.

The continuous class-E modes theory provides a new degree of freedom for wide-band SMPA designs. In Fig. 3.3, Z_1^S and Z_2^S were plotted for $\phi_1 \in [43^o, 78^o]$ and a fixed output power level. As seen from the figure, the extended design space allows some variation for both the fundamental tone and second harmonic switch impedances. The high efficiency and output power of the class-E PA may then be preserved over a wide bandwidth by mapping the unavoidable frequency dependence of the load network impedances to the

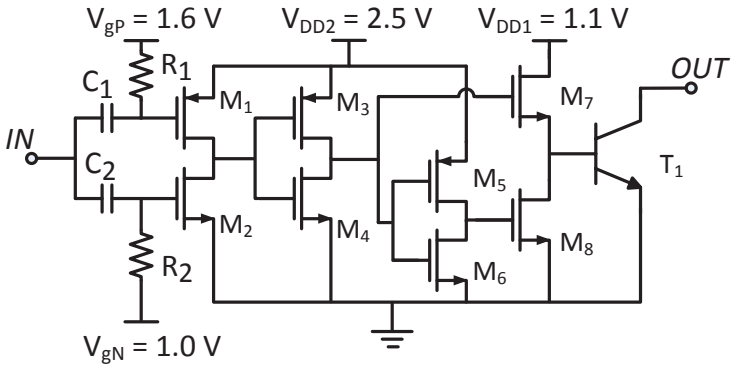


Figure 3.5: Schematic of the active power switch. On-chip decoupling capacitors are not shown for the sake of simplicity. The gate widths are: $W_{M1} = 0.48$ mm, $W_{M2} = 0.16$ mm, $W_{M3} = 0.96$ mm, $W_{M4} = 0.4$ mm, $W_{M5} = 0.8$ mm, $W_{M6} = 0.325$ mm, $W_{M7} = 2.8$ mm, $W_{M8} = 2$ mm. $R_{1,2} = 2$ kΩ, $C_{1,2} = 9.6$ pF.

$\{Z_1^S, Z_2^S\}$ trajectories. This was used as a basis for realization of a wide-band class-E PA demonstrator.

3.4 Wide-band Bi-CMOS Continuous Class-E Modes PA Prototype

In [Paper B], a watt-level 1.3-2.2 GHz continuous class-E modes SiGe BiCMOS SMPA is designed for experimental verification of the large bandwidth possibilities offered by the class E continuum. It is worth mentioning that, Gao *et al.* also utilized the derivations in [Paper A] for a wide-band CMOS SMPA design [46], further supporting the claim that the continuum enables high efficiency operation over wide bandwidth.

The active switching device for the class-E PA is realized in NXP's QUBIC4X SiGe BiCMOS process. The load network is realized off-chip on a teflon substrate. Next, the design of these two parts are briefly summarized. More details about the designs can be found in [Paper B].

3.4.1 Active Switch Design

In Fig. 3.5 the schematic of the BiCMOS chip comprising the HBT switch and CMOS driver circuit is shown. The output power switch for the class-E is implemented using a SiGe HBT with 13 V collector-base breakdown voltage (BV_{CBo}). The total emitter length of the HBT device is 4.96 mm, where the emitter width is 0.4 μm. The power bar has a total output capacitance (C_{out}) of 4.5 pF, which is considered as part of the continuum class-E load network. Three stages of inverters are implemented as drivers using 0.25 μm 2.5 V CMOS transistors. Due to slow speed/high power consumption of PMOS transistors, the last inverter stage is implemented using two NMOS devices and a conventional inverter. The last NMOS-only stage is operated at a drain-

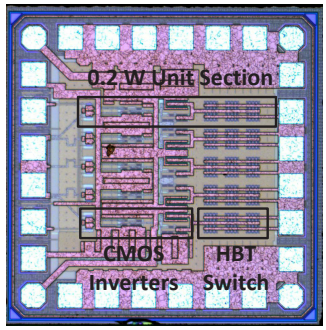


Figure 3.6: Chip photo, the dimensions are 1040x1040 μm.

source bias of 1.1 V, which is sufficient to turn the HBT switch on and off and hence no extra power is wasted for switching. The preceding inverter stages are biased with nominal 2.5 V bias. A photo of the fabricated chip is shown in Fig. 3.6.

3.4.2 Load Network Design

For the off-chip load network design, first the $\{Z_1^S, Z_2^S\}$ impedance trajectories are calculated from (3.8) and (3.9) assuming a constant 1 W output power. Different $\{Z_1^S, Z_2^S\}$ combinations may then be provided by the load network at each frequency. The following error function is thus defined for optimization of the load network parameters:

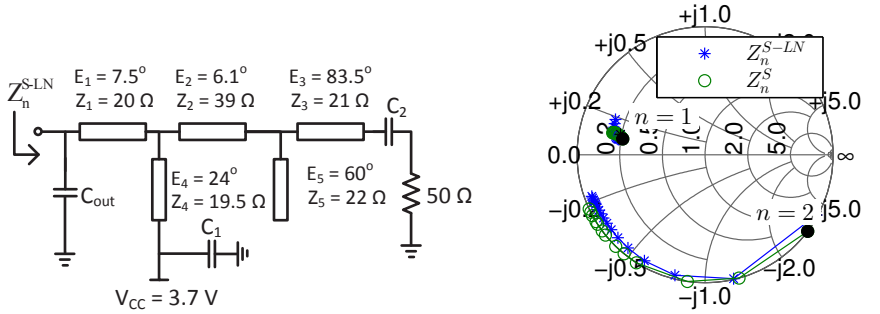
$$err = \sum_{n=1}^{2} \frac{1}{\max|Z_n^S(\phi_{1i})|} \sum_{i=1}^{N} |Z_n^{S-LN}(f_i) - Z_n^S(\phi_{1i})| \tag{3.12}$$

where ϕ_{1i} are also considered as optimization variables since Z_n^S are frequency independent. Term Z_n^{S-LN} denotes the frequency dependent load impedance provided by the load network. The number frequency points used for the optimization is $N = 17$.

The next step is to find a proper load network topology that yields a low err value, meaning that the network presents fundamental and second harmonic impedances that correspond to continuum class-E operation over the desired frequency band. For doing that, our strategy was to start with a highly complex topology and reduce the number of elements until a good complexity-performance trade off is achieved. A network consisting of several cascaded stages of transmission lines and shunt stubs is thus selected to start with. After a few number of trials, the load network topology shown in Fig. 3.7(a) is found, which yields a very good fit between the calculated and synthesized load impedance values, see Fig. 3.7(b).

3.4.3 Experimental Results

The load network shown Fig. 3.7(a) is implemented off-chip on a 5 mil thick teflon substrate with a dielectric constant of $\epsilon_r = 2.33$. A photo of the final constructed PA is shown in Fig. 3.8.



(a) (b)

Figure 3.7: (a) Schematic of continuum Class-E load network, where C_{out} represents the output capacitance of the HBT. (b) Calculated and synthesized switch impedances, $Z_n^S(\phi)$ $Z_n^{S-LN}(f)$ respectively, where subscript n denotes the harmonic index. The black markers denotes the impedance points at the lowest ϕ_1 and f, where $\phi_1 \in [44^o, 66^o]$ and $f \in [1.4, 2.2]$ GHz.

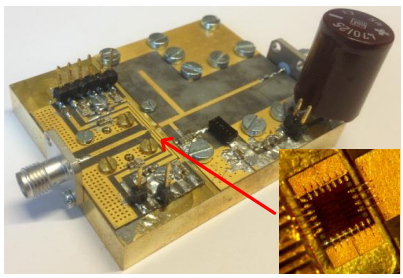


Figure 3.8: Fabricated continuous class-E modes PA prototype.

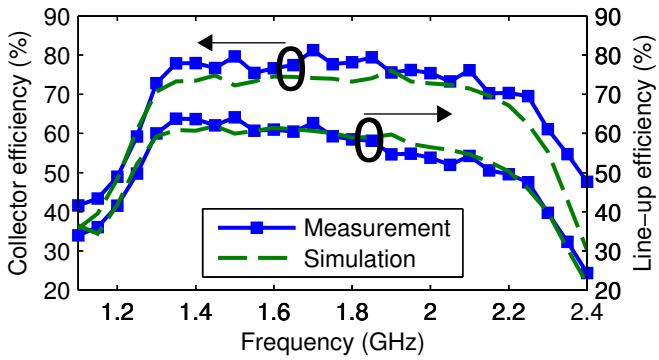


Figure 3.9: Collector and line-up efficiencies versus frequency.

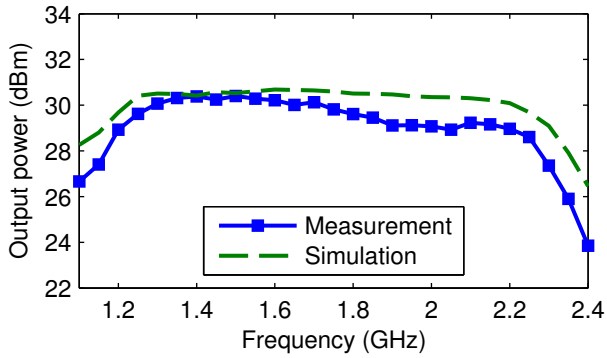


Figure 3.10: Output power versus frequency.

Table 3.2: Comparison with state-of-the-art CMOS/BiCMOS class-E PAs

	Tech.	Load Netw.	f (GHz)	Gain (dB)	P_{out} (dBm)	η (%)	η_{tot} (%)
2005, [47]	130 nm CMOS	On-chip	1.4-2	n/a	> 23	> 62	> 59
2006, [48]	IBM 0.25 μm BiCMOS	On-chip	0.5-1.2	> 7.2	> 17	n/a	> 50
2012, [49]	65 nm CMOS	Off-chip	0.55-1.05	> 16	> 30	> 67	> 52
This work	NXP 0.25 μm BiCMOS	Off-chip	1.3-2.2	> 23	> 29	> 70	> 50

In Fig. 3.9, the efficiency simulation and measurement results are shown. As seen from the figure, the prototype provides a virtually flat collector efficiency across $1.3 - 2.2$ GHz band, as expected from the theory. Measured collector efficiency is higher than 70% and the line-up efficiency, which also includes the power consumed by CMOS drivers, is higher than 50%. Output power results are shown in Fig. 3.10, where the measured output power is higher than 29 dBm across $1.3 - 2.2$ GHz. The output power variation is less than 1.5 dB across the same band. These results clearly prove that the continuum can enable high efficiency and high output power over wide bandwidth in SMPAs.

In Table 3.2, the measurement results are summarized and compared with state-of-the-art CMOS/BiCMOS based wide-band class-E PAs. As seen from the table, even considering that the center frequency is the highest for the prototype, the efficiency-bandwidth performance stands out. This indicates that the proposed design technique may provide a very useful toolbox for practical realization of wide-band highly efficient class-E PAs in diverse applications.

3.5 Summary and Discussion

A continuum of novel class-E solutions has been derived. The continuum enables comprehensive RF waveform engineering possibilities for performance improvement in specific applications. For instance, the switch waveforms can be shaped for lower ohmic losses or lower switching losses. Another important application of the new theory is wide-band SMPA design. In contrast to conventional SMPA modes, the continuous class-E modes allow some variation for the switch impedances. The high efficiency can then be maintained over a wide range of frequencies by mapping the inherent variation of the load impedances to calculated optimal impedance trajectories.

The extended design space revealed by the continuous class-E modes theory is expected to find many applications where high efficiency and high bandwidth are demanded.

Chapter 4

Wide-band Outphasing Modulation of Class-E Power Amplifiers

In the previous chapter, the problem of maintaining proper SMPA operation versus frequency has been addressed, but only a fixed output power level was considered. However, in modern communication standards, high crest factor envelope varying signals are used to achieve a good spectral efficiency. In this chapter we will move towards energy efficient amplitude modulation of SMPAs over large RF bandwidths.

Switch-mode transistor operation requires fixed high amplitude drive signals at the input. Therefore, the output amplitude of SMPAs can not be modulated in the conventional way by controlling the input amplitude. There are, however, a number of sophisticated techniques for amplitude modulation of SMPAs as previously discussed in the introductory chapter. The best known examples are base-band pulse width modulation (BB-PWM), RF pulse width modulation (RF-PWM), $\Delta\Sigma$ modulation, envelope elimination and restoration (EER) and outphasing architecture [10]. This chapter focuses on the outphasing transmitter architecture.

The outphasing architecture is proven for energy efficient amplification of amplitude modulated signals, e.g. in [16]. However, maintaining high average efficiency over large RF bandwidths in outphasing transmitters is an open issue, which is the research problem addressed in this chapter.

The outline of the chapter is as follows: First a brief overview of the outphasing architecture is given. Next, the outphasing combiner types are reviewed and their bandwidth limitations are discussed. Thereafter a novel wide-band outphasing combiner design technique is presented that is developed in [Paper C]. Then, design and characterization results of a 700-1000 MHz CMOS-GaN HEMT outphasing transmitter prototype is presented. As a sidetrack, it is further shown in [Paper D] that the theoretical approach developed in [Paper C] can also be used for design of Doherty PA combiner networks. Finally, the characterization results of a 3.5 GHz GaN HEMT Doherty PA demonstrator based on this approach is presented.

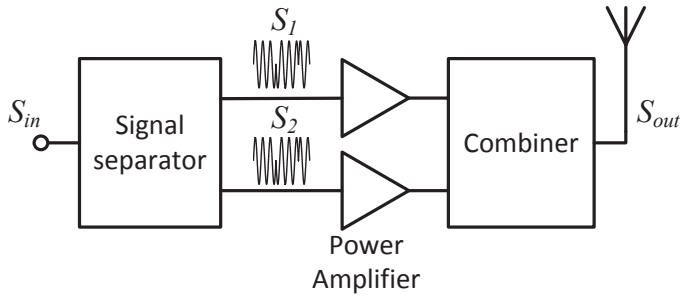


Figure 4.1: A block diagram of an outphasing transmitter architecture.

4.1 Outphasing Transmitter Architecture

The outphasing transmitter concept was first introduced by Chireix in 1935 [50]. In an outphasing transmitter, the amplitude modulated input signal is decomposed in two constant envelope signals with a phase offset between them (outphasing angle) as illustrated in Fig. 4.1. The outphasing angle is determined by the instantaneous amplitude of the input signal in a way we will describe later. The constant envelope signals can be amplified with highly efficient saturated PAs or SMPAs. After power amplification, the signals are summed using a passive combiner network and an amplified replica of the input signal is generated at the antenna. The outphasing method ideally enables the high efficiency of nonlinear saturated PAs or SMPAs to be exploited without disrupting signal integrity.

In addition to its potential for high efficiency, the outphasing architecture also provides interesting opportunities for integration. The constant envelope nature of the outphasing signals enables realization of the signal generation unit using digital-only building blocks. Heidari *et al.* have implement an outphasing modulator in 90 nm CMOS using two all-digital phase-locked-loop (AD-PLL) circuits [15]. Ravi *et al.* realized a 40 MHz channel bandwidth outphasing modulator in 32 nm CMOS using two digital delay-based phase modulators [17]. If the power levels are also low enough, realization of single-chip outphasing transmitters in digital CMOS technology is therefore possible. The outphasing architecture is thus considered as one of the strong candidates for realization of future fully digital energy efficient radio transmitter front-ends [51].

Research on outphasing transmitters, in general, has focused on two areas: 1) Outphasing signal generation and calibration algorithms 2) Outphasing combiner design. A comprehensive overview of the first research field can be found in [52]. The combiner design is subject of the next section.

4.1.1 Outphasing Combiners

In outphasing transmitters, the realization of the combiner determines how the PAs in the two transmitter branches interact. The combiner therefore plays a crucial role on the transmitter efficiency, linearity, and bandwidth.

In Fig. 4.2(a) a basic outphasing configuration is shown. A floating load

is directly connected between the drain terminals of two transistors. Analysis of this basic configuration may help understanding how transistors interact in outphasing transmitters. Fig. 4.2(b) shows a typically assumed equivalent circuit for analysis of this circuit in outphasing operation, both by Chireix [50] and others [53, 54]. The idealizing assumption made there is that the devices operate in deep saturation and can be modeled by RF voltage sources.

The output voltage V_o is the difference between the transistor outputs:

$$V_o = Ve^{j\psi} - Ve^{-j\psi} = j2V \sin\psi \tag{4.1}$$

Observe that the output voltage can be varied by changing the outphasing angle ψ. The current through the load resistor is:

$$I = \frac{V_o}{R_L} = \frac{j2V \sin\psi}{R_L} \tag{4.2}$$

The load impedances seen by the transistors then follow as:

$$Z_A = \frac{Ve^{j\psi}}{I} = \frac{R_L}{2}(1 - j\cot\psi) \tag{4.3}$$

$$Z_B = \frac{Ve^{-j\psi}}{-I} = \frac{R_L}{2}(1 + j\cot\psi) \tag{4.4}$$

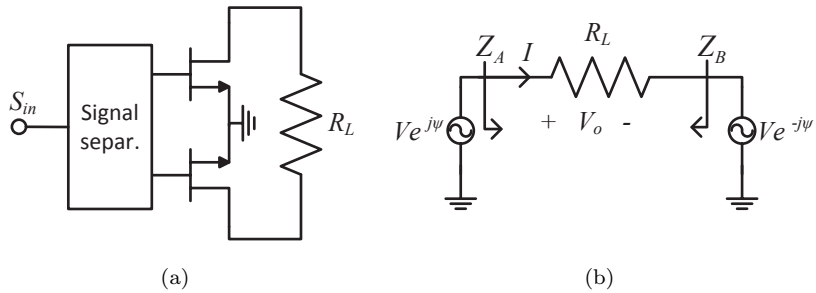
As seen from above, the reactive part of the load impedances depends on the outphasing angle. The devices will therefore observe highly reactive impedances for a wide-range of output power levels. For instance, at 3 dB output power back-off level, the reactive part of the impedance will already be equal to the resistive part. Reactive load modulation has at least two important consequences: First, the efficiency will degrade rapidly versus output power due to non-optimal transistor loading. Second, realistic transistors do not behave as ideal voltage sources under variable loading conditions. The relation between the outphasing angle and the output amplitude will therefore be a more complex function than a simple inverse-sine function.

In practical outphasing transmitters, combiner networks are used to achieve a better linearity-efficiency trade-off than what simple outphasing configuration such as that shown in Fig. 4.2(a) offers. In general, outphasing combiners can be grouped into isolated lossy combiners and non-isolated lossless combiners. First, isolated combiners will be treated.

Isolated Lossy Combiners

In outphasing transmitters, using an isolated lossy combiner, like a Wilkinson or a hybrid, ensures that the output of the PAs are isolated and do not interact. Isolated combiners therefore provide an ideal outphasing operation as the complications of signal dependent loading of the PAs are avoided [52]. These kinds of combiners thus provide perfect linearity [55, 56]. Furthermore, recent research has shown that it is also possible to design and realize very wide-band isolated combiners [57, 58]. Such components enable maintaining good linearity and high output power in outphasing transmitters over wide bandwidths.

With isolated combiners, the instantaneous transmitter efficiency, however, degrades rapidly as the outphasing angle increases. This is due to increasing



(a) (b)

Figure 4.2: (a) A basic outphasing configuration. (b) Model assumed for the circuit analysis.

power waste in the isolating resistance/port of the combiner. The system-efficiency characteristic is in fact the same as that of an ordinary linear class-A PA system, i.e. the efficiency is linearly proportional to the output power-level. Note that, in both systems the DC power is constant versus the output amplitude.

Different techniques have been proposed in the literature to improve the efficiency of outphasing systems with isolated combiners. Zhang *et al.* proposed recycling the RF power delivered to the isolation port using an RF to DC converter circuit [59]. However, at present such converter circuits typically provide very low efficiencies at microwave frequencies, severely limiting the achievable improvement [60–62].

In [63] discrete supply modulation is combined with outphasing operation. In such a configuration, the output voltage is coarsely controlled with discrete supply modulation and the fine control is done with outphasing modulation. This way the outphasing angle can be kept low, reducing the power waste in the isolating resistance. The abrupt change of the supply voltage will however create a significant amount of switching noise at the output, degrading the linearity [64].

Non-isolated Lossless Outphasing Combiners

In outphasing transmitters when using a lossless combiner the PAs will interact and load-pull each other. The simple outphasing configuration shown in Fig. 4.2(a) is an example where the PAs see highly reactive impedances for a large range of output power levels. By proper combiner network design, it can however be ensured that the load modulation occurs in a such way that the PAs experience optimal loading conditions at maximum power as well as at a pre-defined power back-off level. This way high average efficiency can be achieved also with amplitude modulated signals.

The best known lossless outphasing combiner type is the Chireix combiner. A Chireix combiner consists of quarter wave transmission lines and shunt reactive elements, see Fig. 4.3. The PA load admittances for a Chireix system,

assuming saturated class-B operation for the PAs, are derived in [53]:

$$Y_A = G_1 + jB_1 \tag{4.5}$$

$$Y_B = G_1 - jB_1 \tag{4.6}$$

Conductance G_1 and susceptance B_1 are

$$G_1 = \frac{2R_L}{Z_o^2}\sin^2\psi \tag{4.7}$$

$$B_1 = \frac{2R_L}{Z_o}\left(\frac{\sin 2\psi}{2} - \overline{B}_s\right) \tag{4.8}$$

where the normalized shunt susceptance $\overline{B}_s$ is:

$$\overline{B}_s = \frac{Z_o}{2R_L}B_s \tag{4.9}$$

As seen above, by proper selection of the shunt element B_s, the susceptance B_1 can be made zero for one output voltage level, see also Fig. 4.4. This way high efficiency can be achieved at a desired back-off output power level. The efficiency of class-B Chireix system as a function of output voltage is also derived in [53]:

$$\eta = \frac{\pi}{4}\frac{\sin\psi}{\sqrt{\sin^4\psi + (\frac{\sin 2\psi}{2} - \overline{B}_S)^2}} \tag{4.10}$$

The efficiency is plotted versus output amplitude for different $\overline{B}_S$ values in Fig. 4.5. As seen from the figure, the efficiency peak can be moved by varying value of shunt element B_S.

Chireix outphasing transmitters have shown great potential for energy efficient amplification of amplitude modulated realistic communication signals [65–67]. However, the efficiency of Chireix transmitters degrade rather steeply when the operating frequency is changed from the designed center frequency. This mainly due to fact that the transfer characteristics of quarter-wave transmission lines vary very rapidly versus frequency. In addition, the reactive compensation elements in the combiner network are also frequency dependent, overall creating a very sharp combiner frequency response [18].

Recently, there have been studies on wide-band transformer-type lossless outphasing combiners [16,18]. Although significant improvements are achieved with these new topologies, the performance still does not meet the bandwidth requirements of emerging and future communication standards.

4.2 Novel Wide-band Outphasing Combiner Design Approach

In [Paper C], a novel wide-band outphasing combiner design approach has been developed. In contrast to conventional design approaches, no fixed topology is assumed for the combiner. Instead, the design procedure starts with calculation of the combiner network parameters from the boundary conditions

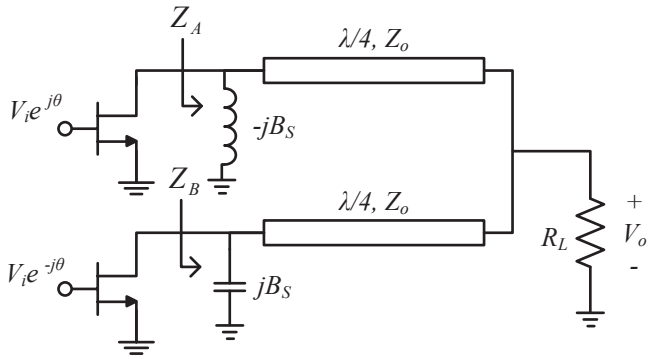


Figure 4.3: A block diagram of the Chireix outphasing transmitter architecture.

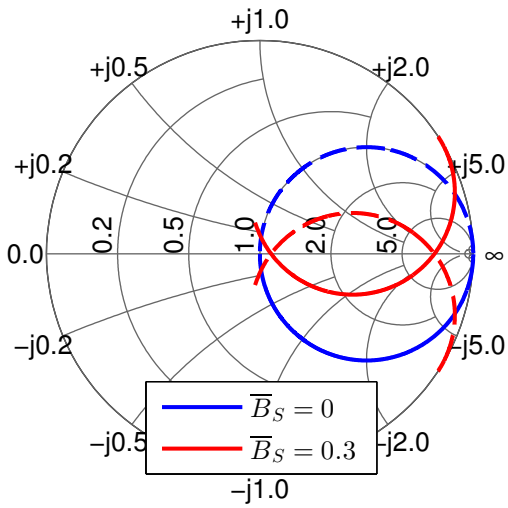


Figure 4.4: Transistor load trajectories in Chireix outphasing transmitters for two different normalized shunt reactance ($\overline{B}_S$) values.

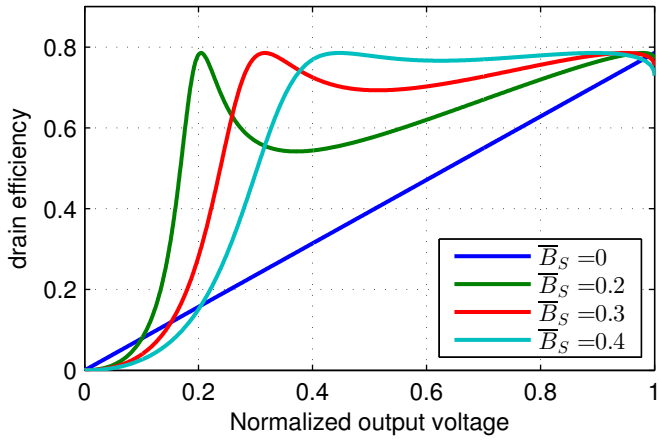


Figure 4.5: Drain efficiency versus output voltage for class-B Chireix outphasing transmitters for different normalized shunt reactance ($\overline{B}_S$) values.

required for proper class-E operation of the PAs in each branch. Utilizing the continuous class-E modes theory presented in Chapter 3, an additional degree of freedom is enabled for calculation of the combiner network parameters, providing an important possibility for wide-band realization. The combiner is finally synthesized to realize the calculated network parameters across the desired frequency band.

It will be assumed that the combiner is lossless and therefore it is important to understand load modulation properties of class-E PAs before starting the derivation of network parameters.

4.2.1 Load Modulation Properties of Class-E PAs

The switch impedances required to satisfy the class-E switching conditions are calculated in Chapter 2:

$$Z_n^S = \begin{cases} (1.52 + j1.11)R, & n = 1 \\ -j5.45R/n, & n > 1 \end{cases} \tag{4.11}$$

where n represents the harmonic index. As discussed previously, Z_1^S and Z_2^S have the highest impact on the efficiency and output power [26]. The factor R depends on the output power level, where

$$R = 0.58\frac{V_{DD}^2}{P_{out}} \tag{4.12}$$

Expression for R and (4.11) indicate that Z_n^S inversely scales with P_{out}. Ideally, the impedances at all harmonics of the carrier frequency should therefore be modulated to vary the output power without violating class-E operation. Even so, in practice, modulating only the fundamental tone impedance, impedance,while keeping the second harmonic impedance fixed, also yields a nearly flat efficiency versus output power profile, as it will be shown briefly with

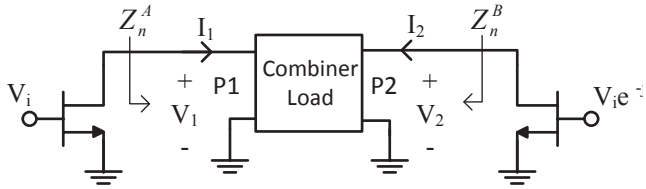


Figure 4.6: Schematic used for the derivation of the two-port combiner network parameters. $Z_n^{A,B}$ denotes impedances experienced by the switches, where n is the harmonic index. $\{V_1, V_2\}$ and $\{I_1, I_2\}$ denotes the fundamental tone component of the drain voltage and current waveforms.

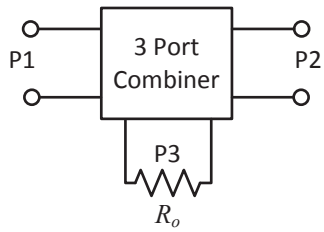


Figure 4.7: Realization of the combiner in Fig. 4.6 with a three-port lossless reciprocal network terminated with a resistive load.

simulations in this section. Therefore, only the fundamental tone impedance load modulation will be considered for the combiner design.

4.2.2 Derivation of Combiner Network Parameters

The derivation of the combiner network parameters is based on the schematics shown in Fig. 4.6-4.7. In the schematic shown in Fig. 4.6, Z_n^A and Z_n^B denotes the impedances experienced by the left and right transistors, respectively. First, the two-port combiner network parameters will be calculated assuming that the two-port is reciprocal and lossy, i.e. the load is included inside, see Fig. 4.6. It is then proven that it is possible to realize the combiner network parameters with a three-port lossless reciprocal network terminated with a purely resistive load, see Fig. 4.7. The combiner is then synthesized to realize the calculated parameters across the band.

The outphasing angle between the fundamental tone of the drive signals is represented by θ, see Fig. 4.6. In the previous examples, the phase of both branch signals were changed. As seen from Fig. 4.6, here we assume that only one of the branch signals is phase-shifted θ degrees while the phase of the other branch signal is kept fixed. This is merely to make the derivations somewhat easier. The same drain bias is assumed for the both cells. The following boundary conditions are further assumed for the derivation:

1. **Optimal impedance at peak power:**

   Both switch transistors see the optimal class-E fundamental tone impedance at the peak power level (P_{peak}) which occurs at $\theta = \theta_1$:

$$R(\theta_1) = 0.58\frac{V_{DD}^2}{P_{peak}} \tag{4.13}$$

$$Z_1^A(\theta_1) = Z_1^B(\theta_1) = (1.52 + j1.11)R(\theta_1) \tag{4.14}$$

2. **Optimal impedance at back-off:**

   Both transistors see the optimal fundamental tone impedance when the output power is backed-off by factor of γ at $\theta = \theta_2$:

$$R(\theta_2) = \gamma 0.58\frac{V_{DD}^2}{P_{peak}} \tag{4.15}$$

$$Z_1^A(\theta_2) = Z_1^B(\theta_2) = (1.52 + j1.11)R(\theta_2) \tag{4.16}$$

It will be shown briefly below that the outphasing angle at the peak output power level, θ_1, is fixed by the selected γ.

Note that, with the conventional Chireix combiner, the transistors experience the optimal load (for class-B) at a pre-defined back-off level and at a level near to the peak output power level, see also Fig. 4.4. The boundary conditions above, however, ensure that the optimal load impedances will be perfectly provided at a pre-defined back-off level and at the peak output power level.

The fundamental tone voltages and currents shown in Fig. 4.6 are related by the composite combiner/load Z parameter matrix:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{4.17}$$

where $Z_{12} = Z_{21}$ due to the reciprocity assumption so that there remains three unknown network parameters. Applying the boundary conditions given in (4.14) and (4.16) to (4.17), results in four distinct equations. Considering the parameter θ_2 also as an unknown, the solution set is found as:

$$Z_{11} = \frac{Z_1^A(\theta_2) - Z_1^A(\theta_1)}{1 + e^{j2\theta_1}} + Z_1^A(\theta_1) \tag{4.18}$$

$$Z_{12} = \frac{1}{2}\left(Z_1^A(\theta_1) - Z_1^A(\theta_2)\right)\sec\theta_1 \tag{4.19}$$

$$Z_{22} = \frac{Z_1^A(\theta_1) - Z_1^A(\theta_2)}{1 + e^{j2\theta_1}} + Z_1^A(\theta_2) \tag{4.20}$$

$$\theta_2 = \pi - \theta_1 \tag{4.21}$$

The two-port combiner network parameters are now derived in terms of P_{peak}, V_{DD} and γ, and assuming class-E operation for the PA cells.

It is worth mentioning that, the optimal peak power and back-off impedances $\{Z_1^A(\theta_1), Z_1^A(\theta_2)\}$ in (4.18)-(4.20) can also be found from load-pull simulations or measurements. In that case the parasitics and device nonlinearities

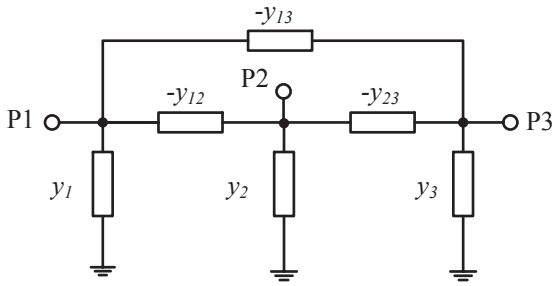


Figure 4.8: A schematic for realization of the three-port lossless network shown in Fig. 4.7 using reactive lumped-element components. The load, R_o, is connected to the third port, P3.

can be perfectly accounted for in calculation of the network parameters. At high frequencies, the device parasites significantly influence the impedance levels. A load-pull based combiner design approach may, therefore, be very suitable for high frequency, e.g. millimeter wave, implementations.

It should also be verified that the calculated two-port network parameters can be realized with a three-port lossless reciprocal network terminated with a purely resistive load, R_o, see Fig. 4.7. In [Paper C, Appendix], using the conditions for being a lossless reciprocal three-port network, it is shown that the following condition is necessary as well as sufficient for such a realization:

$$\Re\{Z_{12}\} = \sqrt{\Re\{Z_{11}\}\Re\{Z_{22}\}} \tag{4.22}$$

The condition given above is satisfied for four different θ_1 values. Each solution provides the same efficiency versus back-off profile but yields different network parameters. The solution set for θ_1 has the form of $\{\pm\theta_{1x}, \pm(\pi - \theta_{1x})\}$ and the value of θ_{1x} depends on the γ value. It is a difficult task to derive an analytical expression for θ_{1x} in terms of γ. However, for a known γ, the value of θ_{1x} is easily found numerically using (4.18)-(4.20) and (4.22).

In [Paper C, Appendix], Z-parameters of the three-port lossless network[1] seen in Fig. 4.7 is derived in terms of the calculated two-port network parameters and R_o:

$$z_{13} = j\sqrt{\Re\{Z_{11}\}/C_1} \tag{4.23}$$

$$z_{23} = j\sqrt{\Re\{Z_{22}\}/C_1} \tag{4.24}$$

$$z_{11} = Z_{11} + \frac{z_{13}^2}{z_{33} + R_o} \tag{4.25}$$

$$z_{12} = Z_{12} + \frac{z_{13}z_{32}}{z_{33} + R_o} \tag{4.26}$$

$$z_{22} = Z_{22} + \frac{z_{23}^2}{z_{33} + R_o} \tag{4.27}$$

[1] Z parameters of the the three-port lossless network are denoted with lower case letters, z_{ij}, to distinguish them from the Z parameters of the two-port network, which are denoted with capital letters Z_{ij}..

where $z_{21} = z_{12}$, $z_{31} = z_{13}$, $z_{32} = z_{23}$ and

$$C_1 = \frac{R_o}{R_o^2 + |z_{33}|^2} \tag{4.28}$$

The parameter z_{33} is here arbitrary, see [Paper C, Appendix].

Now we know the network parameters of the three-port lossless combiner network. In Fig. 4.8 a generic lumped element schematic of the three-port network is given [68]. The following formula may be used to calculate the component values in the schematic:

$$y_i = \sum_{j=1}^{n} y_{ij} \tag{4.29}$$

where y_{ij} are found using (4.23)-(4.27) and the well known Z to Y parameter conversion formulas [69].

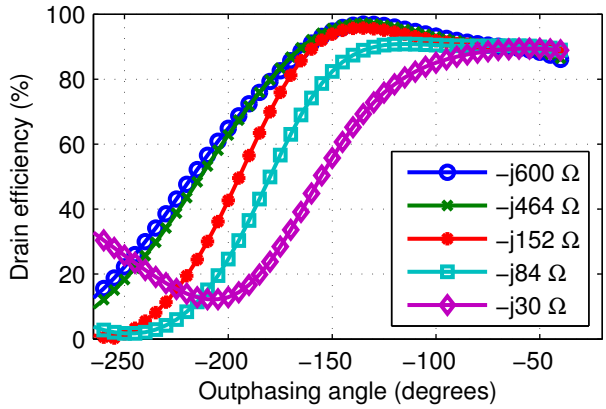
4.2.3 Design Example

To illustrate the design approach described above, a 900 MHz outphasing combiner will be designed in this section. It is assumed that $P_{out} = 15$ W, $V_{DD} = 28$ V and $\gamma = 7.5$ dB that yields θ_{1x} of 42^o. Assuming a reference impedance of 50 Ω, the two-port network parameters in S-parameter format follow as:

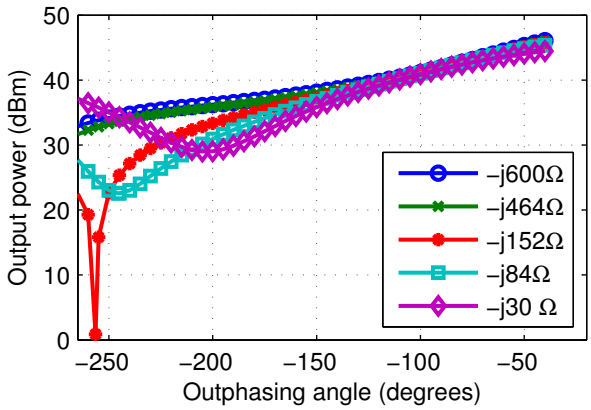
$$S = \begin{bmatrix} 0.69e^{j1.03} & 0.51e^{j2.96} \\ 0.51e^{j2.96} & 0.25e^{-j0.34} \end{bmatrix} \tag{4.30}$$

In Fig. 4.9, the efficiency and output power simulation results are presented using a symbolically defined combiner and an idealized switch model for the transistor. In simulations, we swept the second harmonic switch impedances, $Z_2^{A,B}$, from $-j30$ Ω to $-j600$ Ω. The optimal second harmonic impedances at peak power level and at 7.5 dB back-off are $-j84$ Ω and $-j464$ Ω, respectively. The results indicate that $Z_2^{A,B}$ play an important role for the efficiency and the dynamic range, see Fig. 4.9. The efficiency is rather flat versus output power for $Z_2^{A,B} > -84$ Ω and the best dynamic range is achieved for $Z_2^{A,B} = -152$ Ω. The effect of $Z_2^{A,B}$ on the dynamic range can be better understood by studying the example $\{Z_1^A, Z_1^B\}$ trajectories shown in Fig. 4.10. For $Z_2^{A,B} = -j152$ Ω, both devices see almost purely imaginary load impedances at $\theta = -250.25^o$, delivering very low output powers, see also Fig. 4.9(b). However, for $Z_2^{A,B} = -j84$ Ω, $\{Z_1^A, Z_1^B\}$ never become purely imaginary simultaneously and the resulting dynamic range is therefore much lower. As seen from Fig. 4.10, even negative resistances are presented to one of the transistors with $Z_2^{A,B} = -j84$ Ω. It is relevant to mention that negative load resistances with outphasing transmitters were also observed in [70] during measurements.

Using the schematic shown in Fig. 4.8 a lumped element combiner network can directly be realized. The component values are calculated using (4.23)-(4.27) and the two-port network parameters given in (4.30). However, at microwave frequencies, distributed transmission-line networks are preferred as already discussed in Chapter 2. We have not developed a direct recipe for



(a)



(b)

Figure 4.9: Drain efficiency and output power simulation results for different second harmonic load impedances ($Z_2^{A,B}$).

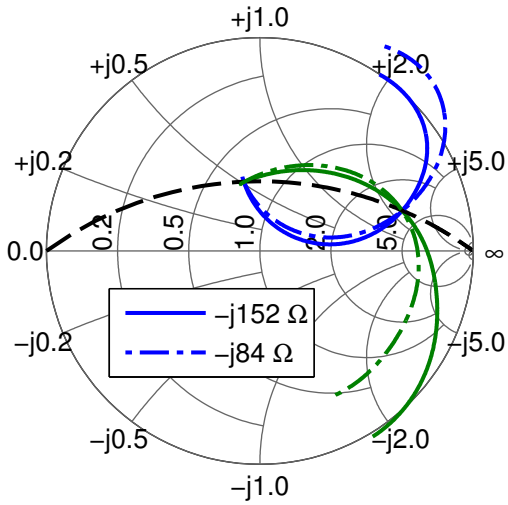


Figure 4.10: Fundamental tone load impedance trajectories for two different second harmonic load impedances ($Z_2^{A,B}$). The dashed black line represents the optimal fundamental tone class-E load trajectory for different output power levels.

realization of the combiner network using transmission lines. However, our experience is that, even using very simple combiner topologies, e.g. networks that consist of cascade connection of transmission lines and stubs, the calculated network parameters are typically easy to realize. Note also that, for empirical realization of the combiner, it is not required to calculate the three-port network parameters. Once θ_{1x} is determined, the circuit design boils down to realization of the calculated two-port network parameters.

In this example, the combiner topology shown in Fig. 4.11 is used for realization of the calculated network parameters at the design frequency, f_o = 900 MHz. In the combiner network, $\{TL_2, TL_7\}$ act as second harmonic traps where $\{TL_1, TL_9\}$ are optimized to have $Z_2^{A,B} = -j152\ \Omega$. Electrical lengths

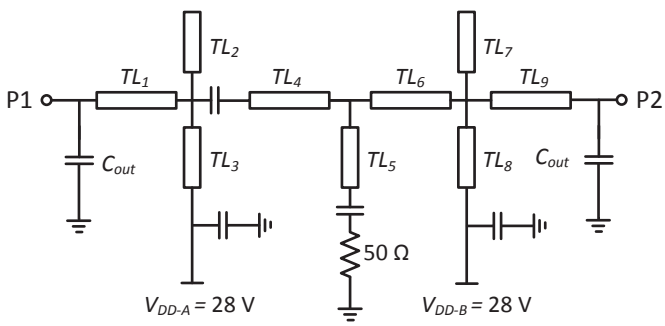


Figure 4.11: Outphasing combiner topology to realize the calculated network parameters.

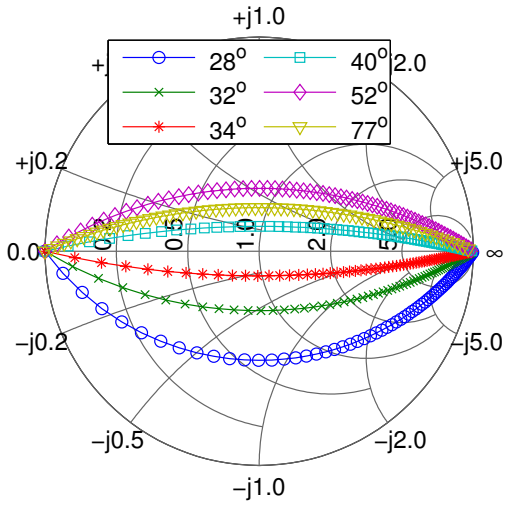


Figure 4.12: Optimal fundamental tone load impedances ($Z_1^S(\phi_1)$) versus output power for different ϕ_1 values.

and the characteristic impedances of the remaining transmission lines are optimized to have good fit to two-port network parameters given in (4.30). The efficiency and dynamic range simulation results achieved with the realistic combiner shown in Fig. 4.11 are identical to the results presented in Fig. 4.9 for the relevant $Z_2^{A,B} = -j152\ \Omega$, and therefore not repeated again.

Realization of calculated network parameters at a single frequency is a straight forward task as demonstrated with the design example above. However, it is not easy to maintain the network parameters over a wide frequency range. In particular, providing a fixed phase angle for S_{12} versus frequency is almost impossible due to the inevitable frequency dependent phase shift introduced by the reactive components in the combiner network.

4.2.4 Utilization of the Continuous Class-E Modes Theory

As demonstrated above, the conventional class-E theory yields a single set of combiner network parameters which does not provide much possibility for a wide-band realization. On the other hand, we will now describe how the continuous class-E modes theory enables an extra degree of freedom (ϕ_1, see Chapter 3) for calculation of the network parameters. This allow some variation in the network parameters, thus providing an important possibility for wide-band combiner realization.

Continuous class-E mode fundamental switch impedances, $Z_1^S(\phi_1)$, were already presented in Chapter 3, see (3.8). It is presented again here for the sake of completeness:

$$Z_1^S(\phi_1) = R\frac{(1+jx_1)\pi}{\pi + j2(1+jx_1)\cos^2\phi_1} \tag{4.31}$$

where x_1 only depends on ϕ_1, see (3.2), and

$$R = \frac{8\sin^2\phi_1}{\pi^2}\frac{V_{DD}^2}{P_{out}} \tag{4.32}$$

The impedances $Z_1^S(\phi_1)$ are plotted versus output power level in Fig. 4.12. Note that, an infinite number of high-efficiency impedance trajectories exist, where each will yield a different set of combiner network parameters.

Using $Z_1^S(\phi_1)$, the boundary conditions for calculation of the outphasing combiner network parameters are now generalized as:

1. **Optimal impedance at peak power:**

   Both switch transistors see an optimal fundamental tone impedance at the peak power level which occurs at $\theta = \theta_1$:

$$R(\theta_1, \phi_1^p) = \frac{8\sin^2\phi_1^p}{\pi^2}\frac{V_{DD}^2}{P_{peak}} \tag{4.33}$$

$$Z_1^A(\theta_1) = Z_1^B(\theta_1) = Z_1^S(\phi_1^p) \tag{4.34}$$

2. **Optimal impedance at back-off power:**

   Both transistors see an optimal fundamental tone impedance when the output power is backed-off by a factor of γ at $\theta = \theta_2$:

$$R(\theta_2, \phi_1^{bo}) = \gamma\frac{8\sin^2\phi_1^{bo}}{\pi^2}\frac{V_{DD}^2}{P_{peak}} \tag{4.35}$$

$$Z_1^A(\theta_2) = Z_1^B(\theta_2) = Z_1^S(\phi_1^{bo}) \tag{4.36}$$

Observe that, the boundary conditions assume different ϕ_1 values at peak power level ($\phi_1 = \phi_1^p$) and γ dB back-off ($\phi_1 = \phi_1^{bo}$). In other words, we allow the impedances seen by the switches (transistors) at the peak power level and at the back-off level to be on different trajectories in Fig. 4.12. This way even two new degrees of freedom are enabled for calculation of the network parameters. Each combination of $\{\phi_{1p}, \phi_{1bo}\}$ yields a different set of network parameters in (4.18)-(4.20). This reveals a very large combiner design space, providing important possibilities for wide-band realization as experimentally demonstrated in the next section.

4.3 Wide-band Outphasing Transmitter Demonstrator

In [Paper C], a 700-1000 MHz CMOS-GaN wide-band out-phasing transmitter prototype is designed to demonstrate the use of the extended combiner design space enabled via continuous class-E modes theory. In this section the design and measurement results are summarized.

In Fig. 4.13, a schematic of the transmitter demonstrator is shown. First the realization of the active switches is treated.

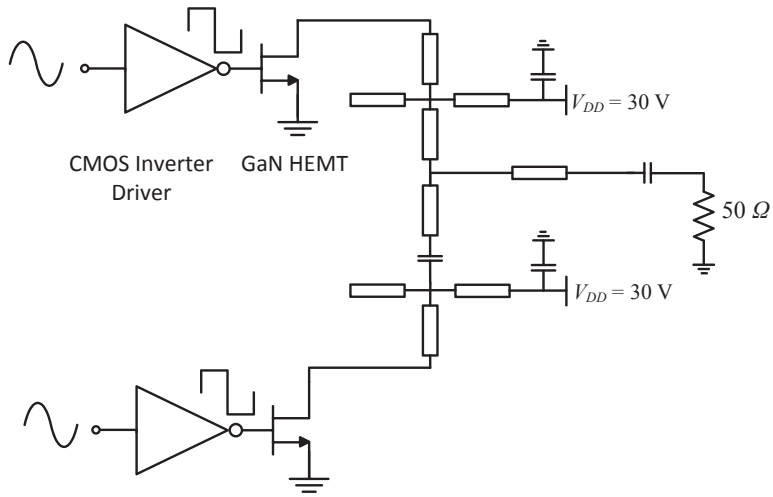


Figure 4.13: Schematic of a CMOS-GaN wide-band outphasing transmitter demonstrator.

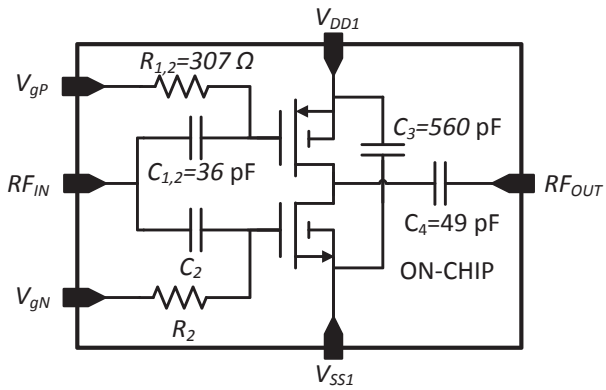


Figure 4.14: CMOS inverter circuit for generation of square shaped drive signals.

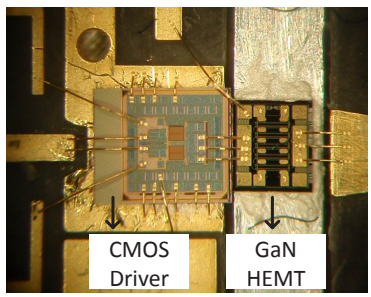


Figure 4.15: CMOS-GaN line up as a high power switch.

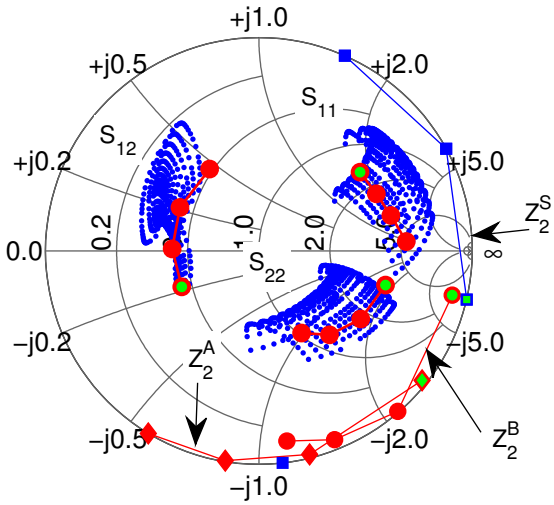


Figure 4.16: Calculated optimal combiner S-parameters (blue) and synthesized combiner S-parameters for frequency range of 700-1000 MHz (red). The green-filled markers denotes the lowest frequency points. The synthesized and optimal second harmonic impedances, $Z_2^{A,B}$ and Z_2^S respectively, are also presented.

4.3.1 Active Switch Realization

Commercial GaN HEMTs (Cree CGH60015DE) are used as the output switching devices for the class-E cells. A single stage inverter circuit implemented in a commercial 65 nm CMOS process is used as the driver for the GaN HEMT [71]. The schematic of the driver is shown in Fig. 4.14. The inverter driver ensures that the GaN HEMT is switched on and off with short transition times. A photo of the realized CMOS-GaN line-up is shown in Fig. 4.15.

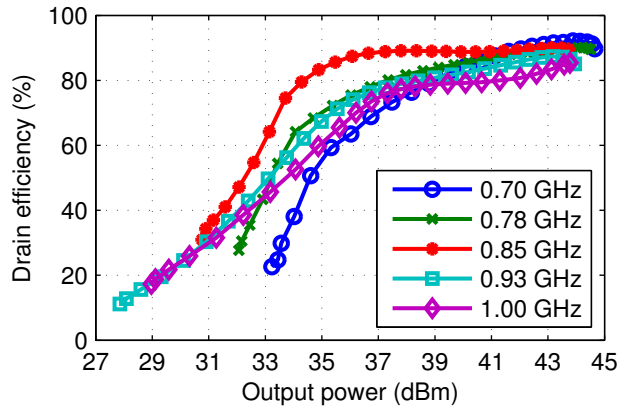
4.3.2 Combiner Design and Realization

For the combiner design, the first step is to calculate its network parameters using (4.18)-(4.20) and (4.33)-(4.36). It is assumed that $P_{out} = 15$ W, $V_{DD} = 28$ V and $\gamma = 7.5$ dB. The resulting network parameters, $\{S_{ij}\}$, are plotted in Fig. 4.16. Each point in the graph corresponds to a different combination of $\{\phi_1^p, \phi_1^{bo}\}$. As seen from the figure, a very large combiner design space is now enabled, allowing variation over frequency, while maintaining high efficiency.

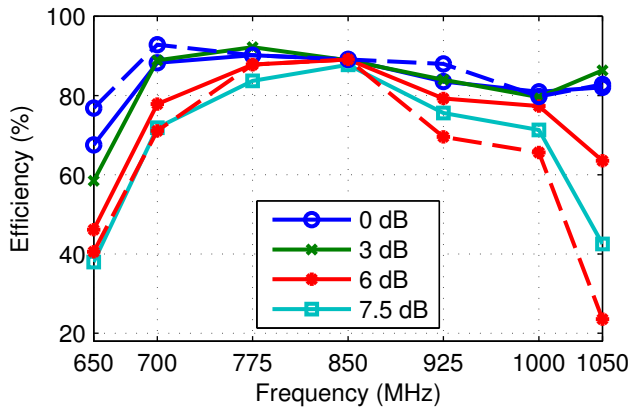
At each frequency point in the range between 700 and 1000 MHz we allow a different set of $\{S_{ij}\}$. The following error function is thus defined for optimization of the component values in the combiner network:

$$err = \sum_{i=1}^{2}\sum_{j=1}^{2} \frac{1}{\max|S_{ij}|} \sum_{n=1}^{N} |S_{ij}^c(f_n) - S_{ij}(\phi_{1n}^p, \phi_{1n}^{bo})| \tag{4.37}$$

where $\{\phi_{1n}^p, \phi_{1n}^{bo}\}$ values are also considered as optimization variables since we can freely select an S_{ij} from the design space at each frequency point. The



(a)



(b)

Figure 4.17: Cut-ready simulation results. The duty cycle range used in simulations is $d \in [0.35, 0.6]$, where d decreases monotonically versus frequency. (a) Drain efficiency versus back-off at different frequencies. (b) Drain efficiency versus frequency for different back-off levels. Efficiency results at peak output power level and 6 dB back-off with fixed 50% duty cycle (dashed-lines) are also included for comparison.

symbol S_{ij}^{c} denotes the frequency dependent S-parameters provided by the combiner network. The number frequency points used for the optimization is $N = 4$.

Ideally, the combiner should also provide the optimal second harmonic impedances versus frequency. However, including this also as an optimization goal causes a very poor fit for the fundamental tone S-parameters. On the other hand, without significantly increasing err, it can at least be ensured that $Z_2^{A,B}$ will be almost purely imaginary by also setting the following constraints for the optimization:

$$\{|S_{11}^{c}(2f)|, |S_{22}^{c}(2f)|\} > 0.95 \tag{4.38}$$

The constraint above ensures that almost no real power will be generated in the load at the second harmonic.

Using the combiner topology shown Fig. 4.11, a very good fit is achieved between the synthesized and calculated fundamental tone S-parameters, see Fig. 4.16. Also, almost purely imaginary second harmonic impedances are presented to the both switching transistors across the band.

Non-optimal second harmonic impedance phase angle cause efficiency degradation especially at back-off power levels. It is found that this can be compensated by fine tuning of the switch duty cycle around 50%. This is attributed to fact that the optimal combination of the fundamental tone and the second harmonic switch impedances strongly depends on the duty cycle for SMPAs [21], [25]. It is also important to add that optimization of switch duty cycle versus frequency for outphasing transmitters was first proposed in [72].

In the circuit, the duty cycle of the inverter driver is adjusted by varying the PMOS and NMOS transistor gate bias voltages, V_{gP} and V_{gN} respectively [73]. This property has been demonstrated via load-pull measurements in [Paper E], where the achieved duty-cycle range was approximately $d \in [0.35, 65]$.

Final cut-ready simulation results using an in house model for the GaN HEMT are shown in Fig. 4.17. As seen from the figure, a flat efficiency profile versus back-off is achieved for the 700-1000 MHz band. The drain efficiency is higher than 71% at 7.5 dB back-off across the band. These simulation results show that high average efficiency can be achieved over a wide frequency range in outphasing transmitters using the proposed outphasing combiner design technique.

The overall transmitter efficiency simulation results are not included here since no model was available for the CMOS driver circuit. The measured overall transmitter efficiency results are, however, presented in the following section.

4.3.3 Experimental Results

The combiner network shown in Fig. 4.11 is implemented on 15 mil thick teflon substrate with a dielectric constant of ϵ_r= 2.33. The fabricated load network, GaN HEMTs and driver boards are mounted on a brass fixture which also provides overall grounding. A photo of the manufactured outphasing transmitter demonstrator is shown in Fig. 4.18. The drain and line-up efficiencies, η and

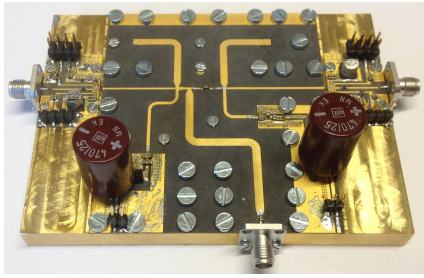


Figure 4.18: A photo of the constructed wide-band outphasing transmitter prototype.

η_{tot} respectively, were both measured. The efficiency definitions follow as [10]:

$$\eta = \frac{P_{out}}{P_{DC1}} \tag{4.39}$$

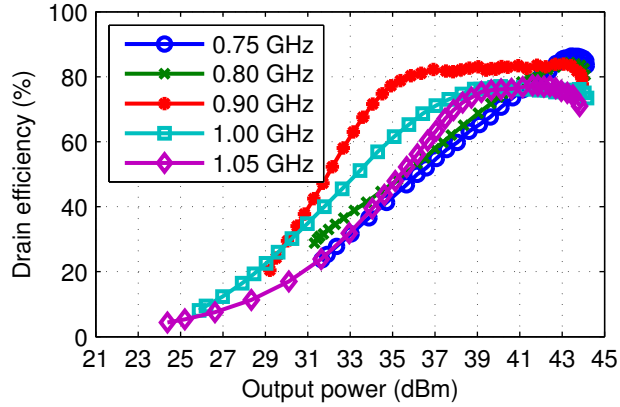
$$\eta_{tot} = \frac{P_{out}}{P_{DC1} + P_{DC2} + P_{av-tot}} \tag{4.40}$$

where P_{DC1} and P_{DC2} are the DC powers drawn by the GaN HEMT devices and the drivers, respectively. P_{av-tot} is the total available RF power applied to the CMOS drivers.

The drain and line-up efficiency measurement results are shown in Fig. 4.19. The measured drain and line-up efficiencies at 7.5 dB back-off are above 52% and 45% respectively across 750-1050 MHz, see Fig. 4.19b-c. The measured back-off efficiency for the frequency range of 700-800 MHz is lower than the simulation results, which might be attributed to the model inaccuracies and the fabrication tolerances. It is also observed that the center frequency is shifted from 850 MHz to 900 MHz. Despite the discrepancies, the prototype provides a very large RF bandwidth performance for outphasing transmitters. In Table 4.1 the results are compared with the state-of-the-art outphasing transmitter results. As seen from the table, the prototype provides the best back-off efficiency-bandwidth performance among all results.

Dynamic characterization and linearization study of the transmitter is left as a future work. One problem related to linearity is, however, the low dynamic range achieved with pure outphasing operation. The simulation results presented in Fig. 4.9 show that the dynamic range is sensitive to combination of the fundamental tone combiner network parameters and the second harmonic terminations. Although it is possible to achieve the optimal combination for dynamic range at a single operating frequency, it is difficult to provide specific fundamental tone network parameters and second harmonic reactive terminations over a wide range of frequencies. Therefore, more robust alternative approaches should be considered for achieving large dynamic ranges and thus good linearity versus frequency.

Switching to linear mode of operation, i.e. controlling the output amplitude by varying the input amplitude rather than varying the outphasing angle, is one approach for improving the dynamic range. The feasibility of hybrid linear-outphasing operation was experimentally demonstrated in [66] for a class-B



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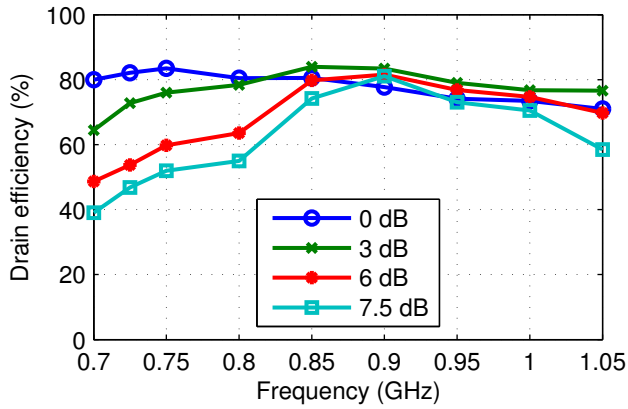

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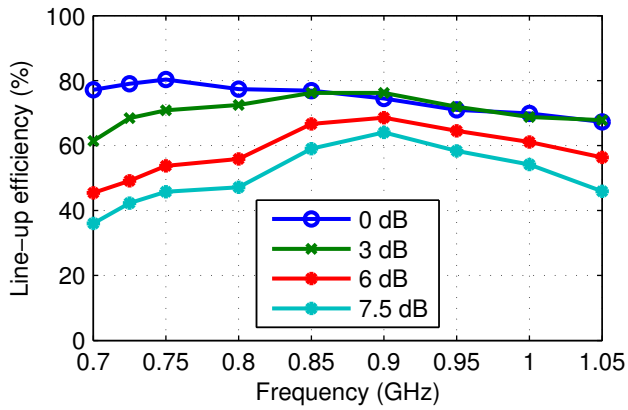


(c)

Figure 4.19: Measurement results using $V_{DD} = 30$ V, $V_g = -2.5$ V, $V_{DD1} = 6$ V, $V_{gN} \in [0.6, 1.4]$ V and $V_{gP} \in [4.8, 5.4]$ V. (a) Drain efficiency versus back-off at different frequencies. (b) Drain efficiency versus frequency for different back-off levels. (c) Line-up efficiency versus frequency for different back-off levels.

Table 4.1: Comparison with state-of-the art wide-band outphasing PAs

	Tech.	f_o (GHz)	BW (%)	P_{peak} (W)	ΔP (dB)	η @ P_{peak} (%)	η @ 6 dB OPBO[1] (%)
[18]	65 nm CMOS	0.7	29	> 1	3.9	> 48	> 46
[66]	GaN	2.14	7	> 63	1.5	> 60	58[2] (@ 2.14 GHz)
[16]	65 nm CMOS-GaN	1.92	18	> 19	0.7	> 68	> 55
This work	65 nm CMOS-GaN	0.9	33	> 24	0.35	> 71	> 60

[1]Output power back-off.
[2]Graphically estimated.

system. However, going to linear mode for switch mode PAs causes severe gain expansion, which may limit the linearity [Paper F].

Hybrid base-band pulse width modulation (BB-PWM)-outphasing operation is another alternative for dynamic range improvement. This hybrid approach was first proposed in [74]. In BB-PWM operation, the PA is driven with a constant envelope signal consisting of bursts of a phase-modulated carrier. The output amplitude is then encoded in the duration of the carrier bursts. In such hybrid operation, the amplitudes lower than the minimum signal level provided by outphasing operation are then generated by driving the PAs with bursted-carrier signals. In contrast to hybrid linear-outphasing approach, the drive signals remain binary which enables further digitalization and integration.

Finally, note that the driver power consumption remains constant versus output power for outphasing operation. The approaches mentioned above therefore also help reducing the driver power consumption. In fact both approaches were originally proposed as line-up efficiency improvement techniques, but they are also improving the dynamic range.

4.4 Doherty Demonstrator Results

As demonstrated experimentally, the novel combiner design approach enables design and realization of very wide-band outphasing transmitters. As a sidetrack it is further shown in [Paper D] that the same theoretical approach can also be used for design of Doherty PA combiner networks. Here only the key results of this study will be presented, where background on Doherty PAs and the design details can be found in [Paper D].

In [Paper D] Doherty combiner network parameters are derived in terms of the device fundamental tone voltage-current waveforms using operating boundary conditions very similar to what was presented in Section 4.2.2, but adopted to the Doherty operating principles. The formulation also allows using the

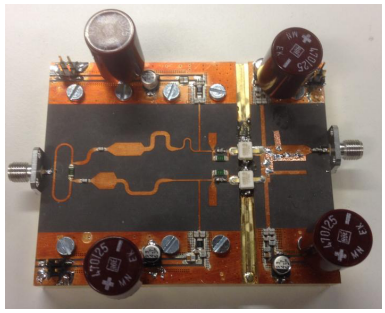


Figure 4.20: Photo of the fabricated Doherty PA using the novel combiner synthesis approach.

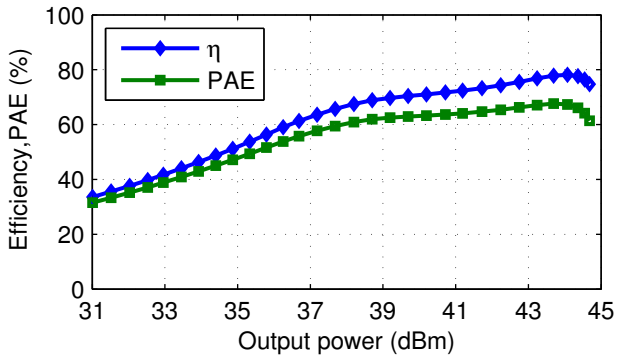


Figure 4.21: Static efficiency measurement results of Doherty PA at 3.5 GHz, $V_{DD} = 28$ V.

waveform data found from load-pull simulations or measurements. The device nonlinearities and parasitics can thus be perfectly accounted for in the combiner design. The design approach therefore enables ultimate efficiency performance to be obtained from the devices in Doherty configuration. This is experimentally verified in a 3.5 GHz Doherty PA demonstrator, showing state-of-the-art efficiency results for linearized modulated communication system signals. A photo of the Doherty PA demonstrator is shown in Fig. 4.20.

In Fig. 4.21 measured static continuous wave (CW) efficiency results are presented. Drain efficiency of 77% and power added efficiency (PAE) of 65% are measured at the peak power level, 28 W. High efficiency is also maintained for a large range of output power levels. At 8 dB back-off, the drain efficiency and PAE are measured to be 60% and 55%, respectively. These efficiency results are significantly higher than what has been previously achieved with single input Doherty PAs for similar frequency ranges [Paper D]. It is also worth mentioning that, these record-high efficiency results are cross-verified by external measurements at NXP Semiconductors, Nijmegen, The Netherlands, where the discrepancy between the two measurement results was less than 0.8 percentage units.

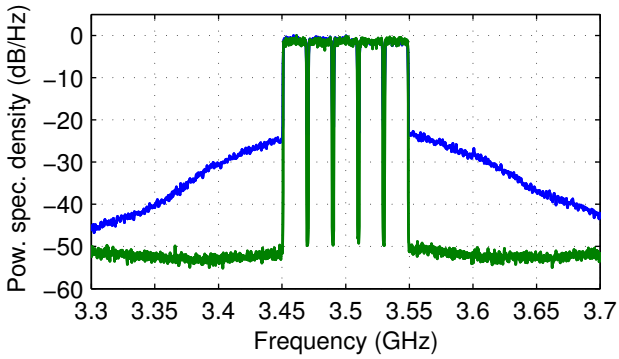


Figure 4.22: Modulated measurement results of Doherty PA without (blue) and with (green) DPD with 100 MHz (5×20) carrier aggregated OFDM signals.

The PA was also tested with realistic communications signals. An average PAE of 52% is measured with 9 dB PAPR 20 MHz LTE signals. The related measured adjacent-channel-leakage-ratio (ACLR) is -52 dB using a low complexity digital pre-distortion (DPD) linearization algorithm [75]. The PA maintains an ACLR of -50 dBc even when driven by a carrier aggregated 100 MHz (5×20 MHz) OFDM signal, see Fig. 4.22. This excellent performance provided by the prototype proves the advantages of the novel Doherty combiner design technique developed in [Paper D].

4.5 Summary and Discussion

In this chapter, a novel outphasing combiner design technique is presented. The design technique is based on calculation of the combiner network parameters from boundary conditions required for highly efficient switch-mode operation of the transistors. The combiner can be synthesized using transmission lines or lumped element networks. Continuous class-E modes theory creates an extra degree of design freedom. This allows some variation of the network parameters over frequency, enabling wide-band combiner realization.

The presented outphasing transmitter prototype provides a high average efficiency over a 33% RF bandwidth around 900 MHz. The bandwidth is mainly limited by the fact that simultaneously providing the optimal second harmonic impedances and the fundamental tone combiner network parameters is difficult for very large bandwidths. In this context, it is worth investigating push-pull topologies, like class-D^{-1}, for realization of the PA cells in outphasing transmitters. This may simplify the constraints on the combiner design and thus even better bandwidth performance may be achieved.

For calculation of the network parameters, one can also use optimal impedances found from load-pull simulations or measurements. The device nonlinearities and parasitics can then be perfectly accounted for in the combiner design. At millimeter wave frequencies, the device parasitics significantly influence the impedance levels. Load-pull based design approach may thus be very suitable for millimeter wave outphasing and Doherty PA designs.

The generic combiner design approach presented in this chapter provides a very useful toolbox for practical realization of outphasing and Doherty transmitters. The results presented in this chapter are the very first outcomes of the novel combiner design approach. It is expected that the approach will find many other applications where high average efficiency and large RF bandwidth are demanded.

Chapter 5

High Efficiency RF Pulse Width Modulation of Class-E PAs

This chapter will describe the RF-PWM technique, which is another method for amplitude modulation of SMPAs. In contrast to the outphasing transmitters presented in the previous chapter, in RF-PWM transmitters only one PA is utilized. The output power is instead controlled by modulation of the duty cycle/pulse width of the input signal driving the SMPA.

The outline of this chapter as follows: In the first section, RF-PWM principle is explained. Loss mechanisms in SMPAs associated with RF-PWM operation are studied. In the second section, a novel class-E topology is presented which is particularly suitable for energy efficient amplification of RF-PWM signals. In the last section, characterization results of a prototype RF-PWM transmitter is presented to prove the feasibility of the technique.

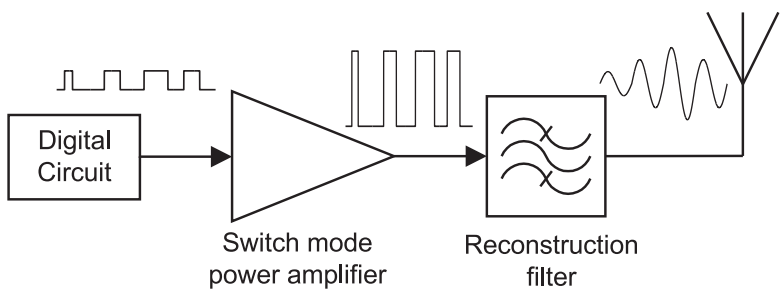


Figure 5.1: A block diagram of RF pulse width modulation based transmitter architectures.

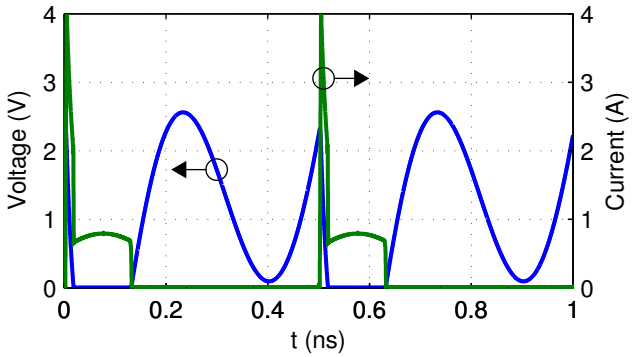


Figure 5.2: Simulated switch waveforms of class-E PA with a non-optimal duty cycle at the input.

5.1 RF Pulse Width Modulation Transmitters

The RF-PWM concept was first proposed by Besslich in [76] for linear amplification with highly efficient SMPAs. A block diagram of RF-PWM architectures is shown in Fig. 5.1. In RF-PWM, the pulse width (duty cycle) of an RF pulse train is varied according to the signal envelope. The phase information is conveyed by the timing of the pulses. The resulting pulse train is amplified with an SMPA and a reconstruction filter is used after the PA to remove the spurious products. The spurious products caused by the switched operation occur in the vicinity of the harmonics of the carrier and can therefore easily be removed with a low loss filter [77–79].

The main challenge associated with the RF-PWM architecture is that conventional SMPAs work with high efficiency only for a fixed duty cycle. Variable duty cycles at the input create severe switching losses decreasing the efficiency [80–82]. Therefore, in spite of its high potential, no competitive efficiency results have been published with RF-PWM architectures so far.

In Fig. 5.2, simulated switch waveforms of a class-E PA with a non-optimal duty cycle at the input is shown to illustrate the loss mechanisms. The PA is designed to operate at 50% duty cycle, whereas 25% duty cycle is used at the input. As seen from the figure, there is a high voltage and current overlap at the switching instances due to non-ZVS.

In [Paper E], a class-E based novel PA topology is developed that is particularly suitable for energy efficient amplification of RF-PWM signals. It is analytically derived that a class-E PA with varying imaginary part of the load impedance can provide ZVS operation over a wide range of duty cycles. RF-PWM of such a PA will therefore not suffer from any severe switching losses and consequently provide high average efficiency with realistic, modulated signals. The operation principle of the proposed PA topology is explained in detail in the next section.

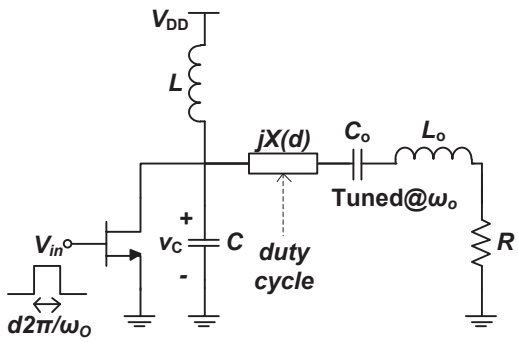


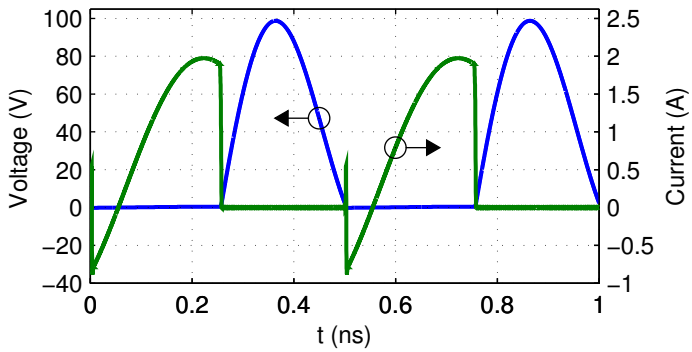
Figure 5.3: Class-E power amplifier with tunable X for high efficiency RF pulse width modulation.

5.2 Efficient RF Pulse Width Modulated SMPA

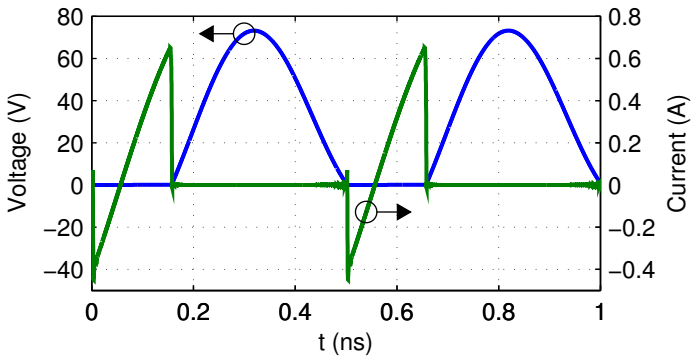
The components of a class-E PA are optimized for a fixed duty cycle, see Chapter 2. If the duty cycle is varied from its nominal value, the switching conditions are violated and the losses increase dramatically. A possible way to preserve the switching conditions is therefore to have electronically tunable components in the load network. Singhal *et al.* [83] analytically proved that ZVS and ZVDS switching conditions can be preserved if the $\{C, R\}$ components of a parallel circuit Class-E PA are modulated along with the duty cycle. For Class-E PAs with finite feed inductance, both switching conditions can actually be preserved if two of the reactive components of the Class-E, $\{C, X\}$ or $\{L, X\}$, are re-optimized as the duty cycle is varied. This property can easily be seen by studying the design equations (2.14)-(2.16). However, it is highly desirable to have only one tunable component in the load network from a complexity point of view. Tunable inductors are not practical which excludes L, while the tuning range of C will be limited by the output capacitor of the device. The series reactive element X is therefore selected as the tunable element, see Fig. 5.3.

Tuning only one element allows only one of the switching conditions to be preserved. The literature shows that ZVS is more important for high efficiency than ZVDS [21], [84]. It is therefore preferred to preserve ZVS, which corresponds to sub-optimal (or variable voltage slope) class-E mode. Corresponding design equations for this mode are required to calculate the X value versus the duty cycle.

Raab derived design equations for suboptimal class-E PAs with RF-choke at the supply at arbitrary duty cycle in [21]. However, as discussed in Chapter 2, class-E PAs with finite feed inductance gives much higher design flexibility. In [Paper E], design equations for suboptimal class-E PAs with finite feed inductance are therefore derived for arbitrary duty cycle. The derivation is



(a)



(b)

Figure 5.4: Simulated switch waveforms: (a) The duty cycle is 50% and $X = 34\ \Omega$ (b) The duty cycle is 30% and $X = 101\ \Omega$.

based on the following off-to-on switching conditions:

$$v_C(t)\Big|_{t=\frac{2\pi}{\omega_0}} = 0, \tag{5.1}$$

$$\frac{dv_C(t)}{dt}\Big|_{t=\frac{2\pi}{\omega_0}} = k\omega_o V_{DD} \tag{5.2}$$

where k is a real number used to parameterize the voltage slope at off-to-on switching moments. The resulting design equations have the following forms:

$$C = \frac{1}{\omega_o R} K_C(d, q, k) \tag{5.3}$$

$$X = R K_X(d, q, k) \tag{5.4}$$

$$R = \frac{V_{DD}^2}{P_{out}} K_P(d, q, k) \tag{5.5}$$

where the functions $\{K_C, K_X, K_L\}$ are found in [Paper E]. Also note that this formulation is similar to the expressions in (2.14)-(2.16), but with k as an added degree of freedom.

In (5.3), C should be fixed. Therefore k has a relation to the duty cycle d, i.e. $k = k(d)$. The optimal X trajectory versus d is then given by $X = RK_X(d, q, k(d))$. Examples of class-E switch waveforms for variable duty cycle and X values are shown in Fig. 5.4. As seen from the figure, there is no voltage and current overlap at the switching instances yielding near 100% efficiency, assuming that the transistor technology supports negative current.

A systematic class-E RF-PWM design procedure is also developed in [Paper E]. The procedure allows practical realization of the proposed topology from circuit and component specifications.

5.3 RF-PWM Transmitter Prototype

Following the design procedure and using in-house (Chalmers University) SiC varactor diodes [85] to implement the tunable imaginary load impedance, a 2 GHz 10 W peak output power GaN HEMT (Cree CGH60015DE) circuit demonstrator is realized. A block diagram of the demonstrator is shown in Fig. 5.5.

RF-PWM input signals for characterization of the prototype PA is generated using the same inverter driver circuit that was used for the outphasing prototype in the previous chapter [71].

5.3.1 Static Characterization

For operation of the transmitter, the optimal combination of varactor control signal V_c and the duty-cycle that maximizes the efficiency at every output power has to be identified. This is performed by continuous wave static measurements where V_c is stepped and the duty cycle at each step is optimized for the best line-up efficiency. Ideally, the gate bias voltages of both NMOS and PMOS transistors in an inverter should be varied to control the duty cycle. However, experiments have shown that keeping the NMOS bias voltage

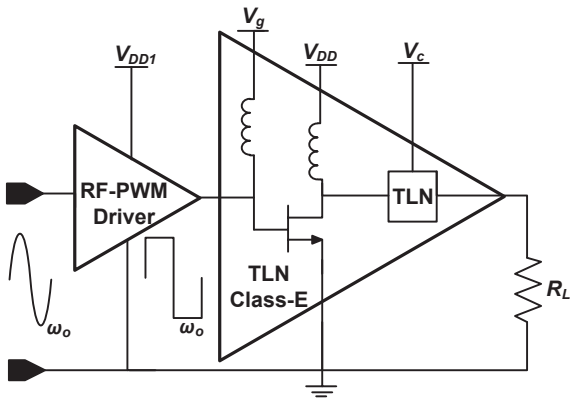


Figure 5.5: Block diagram of the RF pulse width modulated tunable load network (TLN) class-E transmitter.

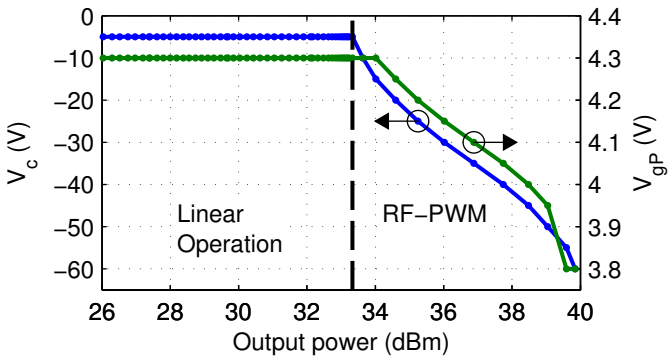


Figure 5.6: The optimal varactor and duty cycle control voltages, V_c and V_{gP}, respectively, versus the output power, P_{out}, at 2 GHz carrier frequency.

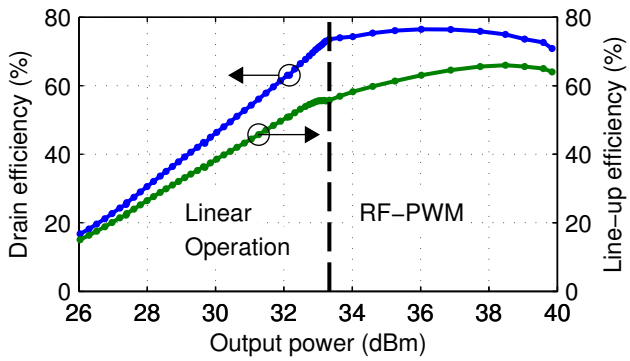


Figure 5.7: The measured drain efficiency of the Class-E stage η and the line-up efficiency η_{tot}, which also includes the driver power consumption, versus the output power at 2 GHz carrier frequency.

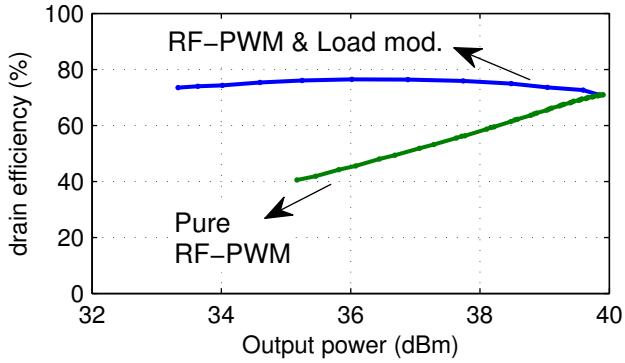


Figure 5.8: The efficiency results when the load impedance tuning disabled, $V_C = -60$ V, (green). The previously presented results that are achieved with optimized varactor control voltages are also included to facilitate comparison (blue).

fixed does not degrade the performance significantly in terms of efficiency and output power dynamic range [Paper E]. The duty cycle is therefore controlled by only varying the gate bias voltage of the PMOS transistor, V_{gP}. The resulting efficiency optimized control functions are shown in Fig. 5.6 and the corresponding efficiency performance is shown in Fig. 5.7. Observe that the efficiency of the class-E stage remains fairly constant versus output power for the RF-PWM region as expected from the theory.

The efficiency is also measured with constant V_c to observe the performance when the load impedance tuning is disabled. This represents traditional RF-PWM of the Class E PA with the results presented in Fig. 5.8. For that case, the drain efficiency drops to <41% at less than 5 dB back-off thus proving that very significant efficiency improvement is achieved with the proposed PA topology.

The output power dynamic range achieved with RF-PWM operation is around 6.5 dB as seen from Fig. 5.6. This dynamic range is clearly not enough for linear amplification of modern communication signals, e.g. W-CDMA or LTE. This limitation may be circumvented by operating the transmitter in linear mode in further back-off. Linear mode means that the output power is directly controlled by the RF input power rather than by the duty cycle and varactor voltage. The resulting input-output power relation is shown in Fig. 5.9.

5.3.2 Dynamic Characterization and Linearization

Characterization of the transmitter with modulated realistic signals requires that the baseband signals are generated dynamically. A two channel arbitrary waveform generator (AWG, Tabor Electronics WW2572A) is used to generate the baseband signals. A high speed op-amp (MS Kennedy 600r) based feedback amplifier is used to amplify the varactor control signal to the required level, see Fig. 5.6. The duty cycle control signal V_{gP} can directly be generated with one of the AWG channels. The RF input signal is generated using

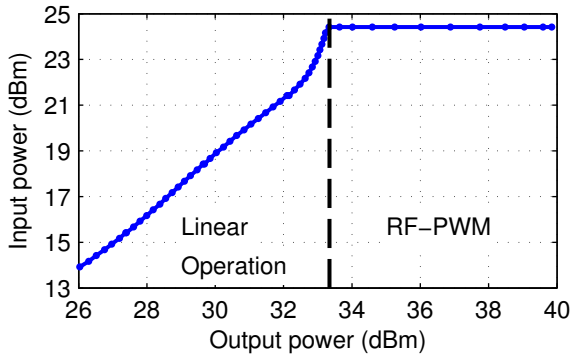


Figure 5.9: The available input power from the RF synthesizer versus the output power. The carrier frequency is 2 GHz.

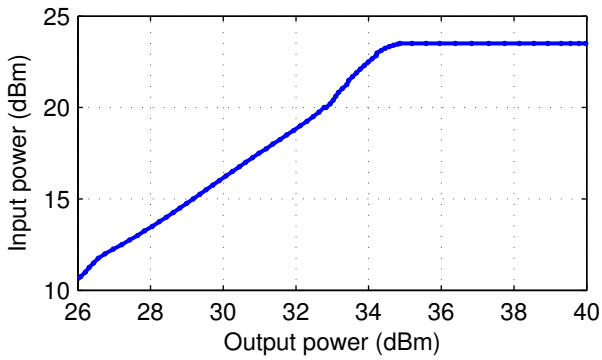


Figure 5.10: The available input power from the RF synthesizer versus the output power with optimized varactor control signal for a smooth transition between linear and RF-PWM modes. The carrier frequency is 2 GHz.

an evaluation board from Texas Instruments (TSW3100), consisting of two digital to analog converters (DAC) for the I and Q branches and an IQ modulator. An Agilent 54845A oscilloscope is used as the measurement receiver. A more comprehensive description of the dynamic measurement procedure used is given in [Paper F]

As switch mode operation requires CMOS and GaN HEMT devices to be deeply saturated, severe gain expansion is unavoidable in the transition to the linear operation region. This causes large discontinuity in the input-output power relationship as seen from Fig. 5.9. The varactor signal can, however, be re-optimized to obtain a smooth transition between linear and switch modes [Paper F]. The resulting input-output power relation with optimized varactor signal for a smooth transition is shown in Fig. 5.10. A smoother and linearization friendly transition region has a price in terms of slightly reduced efficiency but significantly improves the linearity [Paper F].

A digital pre-distortion (DPD) linearization scheme is incorporated to enhance the linearity of the transmitter, see Fig. 5.11. The transmitter is consid-

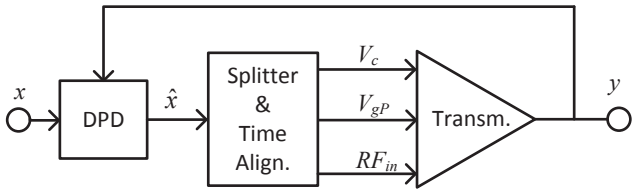


Figure 5.11: Digital pre-distortion linearization scheme.

Table 5.1: Summary of the linearization results

	NMSE (dB)	ACPR (dBc)	$P_{out-avg}$ (Watt)	η_{avg}	$\eta_{tot-avg}$
Before DPD	-13	-23	2.23	67.5%	55.5%
After DPD	-35	-45	2.18	67%	55%

ered as a single-input single-output system. Efficiency optimized input signals are derived from the predistorted input signal ($\hat{x}$) using a digital splitter constructed from the static CW measurement data, i.e. $\{V_c(\hat{x}), V_{gP}(\hat{x}), RF_{in}(\hat{x})\}$, as depicted in Fig. 5.11. The DPD model parameters are identified by comparing the measured output samples (y) and the input samples (x). A vector switched generalized memory polynomial (VS-GMP) model is used as the behavioral model for DPD operation [75]. The VS-GMP quantize the signal according to the signal amplitude into a number of regions and model each region separately. This makes the model very suitable for behavioral modeling of this type of transmitter which has two distinct operating regions: linear and RF-PWM, see Fig. 5.10.

A single carrier 3.84 MHz 6.7 dB PAPR W-CDMA signal is used for dynamic characterization and the results are summarized in Table 5.1. As seen from the table, without sacrificing efficiency the normalized mean square error

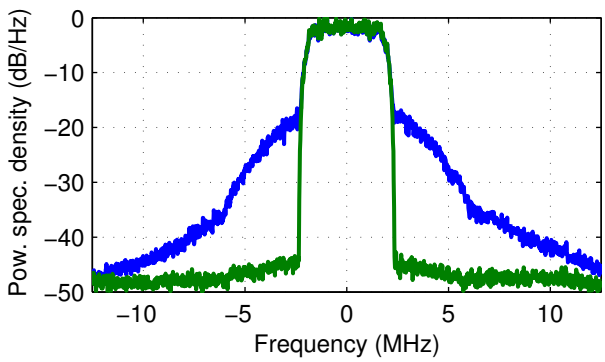


Figure 5.12: Normalized output power spectrum before (blue) and after (green) digital predistortion linearization.

(NMSE) is improved 22 dB when the proposed DPD linearization scheme is applied. Output spectra before and after linearization are shown in Fig. 5.12. The nonlinear transfer function of the transmitter causes severe spectral re-growth. The adjacent channel leakage ratio (ACLR) can however be suppressed down to -45 dBc by using the presented DPD.

5.4 Summary and Discussion

The results presented in this chapter show that the RF-PWM technique can be a very attractive solution for energy efficient amplification of envelope varying signals. However, a generic problem for the RF-PWM technique is low output power dynamic range of the practical modulator circuits [79, 81]. We have proposed a hybrid linear-RF-PWM operating scheme to circumvent this issue. The ACLR achieved with this approach was however at the limit of the specification. It is expected that further CMOS scaling in the future should enable realization of modulator circuits with higher dynamic ranges.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The demand for reduced deployment and operational cost and higher capacity in future mobile communication systems put new requirements on the base station transmitters used. As described in the introduction chapter, these are increased energy efficiency, frequency agility, and further integration.

Realization of highly integrated low cost wireless RF-front ends is alleviated with transmitters architectures that allows implementation of RF functionalities using digital only building blocks. In such transmitters, the overall energy efficiency and the RF bandwidth is determined by the design and realization of the SMPA unit. This thesis has contributed to the theory, design and practical realization of SMPAs that are compatible with digital transmitter architectures.

SMPAs provide a great theoretical potential for obtaining high energy efficiency. Utilization of this high potential in a transmitter architecture with realistic communication signals requires that a proper operation for dynamically varying output amplitude is maintained. We have carefully analyzed two different amplitude modulation techniques in this thesis, outphasing and RF-PWM. Upon understanding the loss mechanisms associated with these amplitude modulation techniques, we have addressed them by introducing new SMPA topologies and by developing new design techniques. This has enabled us to achieve average efficiency numbers very close to the peak efficiency of the SMPAs in both cases, thus truly utilizing their theoretical potential.

SMPAs were known to be inherently narrow band due to stringent harmonic termination requirements of the conventional PA modes. This has prevented them for use in wide-band, frequency agile applications. Through derivation of a continuum of novel high efficiency class-E PA modes we have theoretically proven that the SMPAs can indeed be made very wide band. Experimental results also confirms that the high efficiency of SMPAs can be maintained over a large range of frequencies and output power levels.

In summary, new power amplifier modes, novel power amplifier concepts

and new transmitter design techniques have been introduced. These contributions are there expected to play an important role on realization of new types of frequency agile, energy efficient, and highly integrated/digitalized radio transmitters for future wireless communication systems.

6.2 Future Work

There are several lines of research arising from work presented in this thesis which should be pursued.

In Chapter 3, a watt level highly efficient wide-band SiGe BiCMOS PA has been presented. Considering the power levels achieved, such a solution can be an interesting candidate for pico-femto cell base station transmitter applications. The BiCMOS technology allows complex designs to be made. Therefore, for amplitude modulation of such a PA, multi-bit RF-DAC topologies are interesting to investigate. In RF-DAC approaches, the output amplitude is controlled by regulating the number of active transistors, and therefore very high dynamic ranges can be achieved. In conventional RF-DAC circuits, however, the transistors cells load-pull each other in an undesired way, causing severe efficiency degradation at back-off. By combining the output of two RF-DACs with a combiner network, that may be derived using the same theoretical approach as was used for outphasing/Doherty combiner designs in this thesis, proper load modulation may be enabled.

Wireless industry is now showing a growing interest of using millimeter bands to augment the currently saturated 700 MHz-3.5 GHz radio spectrum bands. The demand for millimeter wave high efficiency radio transmitters will therefore rapidly increase in the near-future. However, at millimeter wave frequencies, the device parasitics significantly influence the impedance levels. The load-pull based outphasing/Doherty PA design technique presented in Chapter 4 is therefore very suitable for millimeter wave realizations. At millimeter frequencies, special attention has to be given to low-loss realization of the calculated combiner network parameters. The possible combiner network topologies and losses associated with them must therefore be investigated thoroughly.

At present, the common approach taken for wide RF bandwidth load modulation based transmitter design is to start with a narrow-band architecture, like Doherty or outphasing, and then try extending the bandwidth by modifying the conventional topology. It is, however, arguable if such an approach will be adequate for meeting the growing long-term demand for RF bandwidth in the long term. It is the author's view that it is also important to search for new load-modulation based transmitter concepts that are inherently wide-band. In other words, an architecture that does not require a tuned combiner network for achieving proper load modulation is what is ultimately needed. Some research activities has already started in this direction at Chalmers although the project is still at the concept development level.

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