

Superconducting 4-8 GHz Hybrid Assembly for 2SB Cryogenic THz Receivers

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Abstract—In the 2SB receivers, the rejection ratio is determined, among other factors, by the performance of the quadrature hybrids.

We present here the design and characterization of an intermediate frequency (IF) assembly comprising a compact 90° hybrid chip (coupled line coupler – Lange coupler– coupled line coupler), two bias-T circuits in order to bias the Superconductor-Insulator-Superconductor (SIS) mixers.

Specifically, the miniaturized 3-section hybrid chip made using thin-film technology utilizes superconducting Niobium (Nb) transmission lines and air bridges to connect the fingers of the Lange coupler (middle section). The assembly is complemented with two bias-T circuits with integrated MIM capacitors.

The assembly was designed to have the amplitude and phase imbalance better than 0.6 dB and $\pm 2.5^\circ$ respectively. Experimental verification of the assembly at 4 K shows good agreement between the measurements and simulations with amplitude imbalance of 0.5 dB and maximum phase imbalance of $\pm 2^\circ$.

Index Terms—Superconducting devices, Microwave components, Directional coupler, Thin-film circuits. 2SB receiver.

I. INTRODUCTION

MODERN cryogenic millimeter and sub millimeter receivers for radio-astronomy employ sideband separation (2SB) layouts since this technology provides ultimate sensitivity and observation possibilities for spectral line (spectroscopic) observations. At the Superconductor-Insulator-Superconductor (SIS) mixers' IF output, there exist both upper and lower sidebands, which are separated with an IF quadrature hybrid. In practice, there will always be some amplitude and phase imbalance in the performance of the RF and IF hybrids and the mixer conversion loss, which will prevent perfect cancellation of the unwanted sideband. Therefore, some of the upper sideband power (P_{USB}) will leak into lower sideband (P_{LSB}) and vice versa. The ratio of the wanted to unwanted sideband powers is called sideband rejection ratio.

There are commercially available hybrids with very good room-temperature performance. However, with 2SB receivers employing superconducting mixers and thus operating at cryogenic temperature (4 K), commercial hybrids' performance is severely degraded. Therefore, the work presented here concerns the design and development of an IF hybrid assembly comprised of a multi-section, superconducting, 90° hybrid, and bias-T circuit for the DC biasing of the SIS mixers. The specifications of the hybrid

assembly are: 4-8 GHz band, the amplitude and phase imbalances are better than 0.6 dB and 2.5° at cryogenic temperatures. The IF hybrid should be as compact as possible, utilize a planar layout so that thin-film technology can be adopted to ensure the repeatability. The aim with such assembly is not only to improve sideband rejection ratio considerably, but also to remove the need for external SIS bias circuit and interconnects/connectors associated with them therefore shrinking the total size of the 2SB receiver, which also could be a clear advantage for 2SB multi-pixel receiver architecture.

II. HYBRID DESIGN

A. Hybrid topology

Multi-section hybrids designs are commonly related to broad bandwidth since single-section hybrids cannot provide the required amplitude imbalance for bandwidths of greater than one octave at best [1] with no margins. However, instead of using a multi-section design for increasing the bandwidth substantially, we suggest, in this hybrid design, the use of multiple sections (i.e. three) to accomplish small amplitude and phase imbalance and at the same time increasing the bandwidth slightly in order to gain some margins at the edge of the IF band.

B. Substrate selection

The possibility to use a mineral substrate with reasonably high dielectric permittivity allows reaching compact design with minimum insertion loss; the latter depending on dielectric loss and conducting loss in the transmission lines. The miniature hybrid chip allows it to be integrated into virtually any sideband separating mixer operating at cryogenic temperatures and is furthermore especially advantageous for multi-pixel receivers or low noise balanced amplifier layouts.

The hybrid is operating at a cryogenic temperature of approximately 4K. In order to provide normal operation, the substrate used for the hybrid circuits needs to have adequate thermal conductivity to ensure proper cooling of the superconducting lines and high mechanical strength to withstand thermal contraction / mechanical stress while cooled to cryogenic temperatures. Furthermore, due to the multi-section design, it would be advantageous to use a substrate with high dielectric constant in order to minimize the overall chip dimensions. Silicon has a high dielectric constant and is furthermore, known to have both good thermal conductivity and good mechanical strength. Traditionally, Alumina substrates with dielectric constant 9.6 are used, as the Alumina substrate has excellent mechanical properties, low loss tangent, and good thermal conductivity. However, the disadvantage of using alumina

compared to single crystal silicon wafers is that the Alumina wafers often are micro porous and has noticeable surface roughness, which aggravates the wafer processing. Therefore, the fabrication of multi-layer components, e.g., the MIM-capacitors in the bias-T circuit is a difficult and unreliable task. For these reasons, we fabricated hybrid on a 675 μm thick high resistivity Silicon substrate.

C. Superconducting microstrip lines

At microwave frequencies, the microstrip line built using normal conducting materials should have a ground and a strip line thickness off at least three times the skin depth. As we consider applications operating at cryogenic temperatures around 4K, the temperature dependent conductivity should be accounted for operating at 4K. As a result, it is required that the microstrip conductor be at approximately 3 μm thick: three times the skin depth for lowest frequency in the IF band and accounting for an approximated value for thin-film gold conductivity at 4K. Our modeling shows that the required metallization thickness will have an influence on the hybrid performance due to the increased coupling capacitance of the microstrip edges. In order to achieve very precise and repeatable coupling, it is important that the microstrip line shape at its edges is as vertical as possible, since non-verticality of the edges affects the line capacitance such that the overall hybrid performance may differ noticeably from one batch to another. Obtaining vertical microstrip edges through electroplating process where the required thickness is 3 μm using gold is a challenging task [2]. Contrary to normal conductors, the skin depth for a superconductor at microwave frequency is zero whereas magnetic field does penetrate into superconductor with the characteristic London penetration depth λ_L [3]. Setting the superconductor thickness to $3\lambda_L$ ensures that the 95% of the B field is extinguished allowing use of a perfect electrical conductor (PEC) approximation for modeling of ScMSL. The London penetration depth for Niobium at microwave frequencies is approximately 85 nm [4], which means that the required thickness of the ScMSL and ground could be almost one order of magnitude less than the minimum thickness required for gold plated microstrip lines. As a result, the non-verticality of the ScMSL edges has negligible effect on the coupling capacitance. In addition, a clear advantage of using ScMSL is that it minimizes the number of fabrication process steps as compared to electroplated gold, especially for the bias-T circuit with integrated MIM capacitors. Therefore, using superconducting microstrip lines does not only provide ease of fabrication but also an important factor for reliable production of the IF assembly circuits. Commercial electromagnetic simulation tools could be used to simulate ScMSL with the superconducting material accounted for by assigning the surface impedance of the superconducting lines. From the equations in [5] it can be shown that the surface impedance of Nb superconductor with 300 nm thickness is of the $\text{m}\Omega$ order for the frequencies of interest, thus justifying the PEC approximation in the 3D simulations.

D. Three section hybrid and bias-T layout

The proposed design employs a symmetrical three-section coupler. The even mode characteristic impedance and for

each stage of the multi-section coupler can be found in tables for a given equi-ripple across the band [6]. The coupling coefficients of each section for a 3-section hybrid with an overall coupling of 3 ± 0.2 was calculated to be approximately -1.5 dB for the middle section and -14.6 dB for the adjacent sections. The first and the third sections consist of coupled line coupler structure whereas the middle section coupler consists of a Lange coupler. Through these choices of couplers, the final structure becomes planar and the hybrid dimensions are completely determined by photolithography process. A schematic of the three section hybrid is illustrated in Fig. 1. The initial dimensions for the multi-section coupler were calculated with Agilent ADS [7] LineCalc, using the coupling coefficients described above. The complete hybrid structure was optimized with Agilent EMPro [7]. The simulations yielded a layout with finger widths and finger separation for this Lange coupler of 28 μm and 12.5 μm respectively, precluding the use of bond wires for interconnecting the fingers. Instead, air bridges were employed as part of the hybrid fabrication using micro fabrication technology, also used in [1]. The dimension of the hybrid substrate is 18.3 mm and 4.3 mm wide.

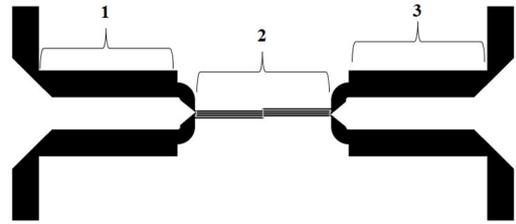


Fig. 1: The 3-section IF hybrid schematic, first and third sections are the coupled line couplers whereas the second section is the Lange coupler. The total length and width of the IF hybrid are 12, 3 mm (total substrate length 18,3 mm) and 4,3 mm respectively.

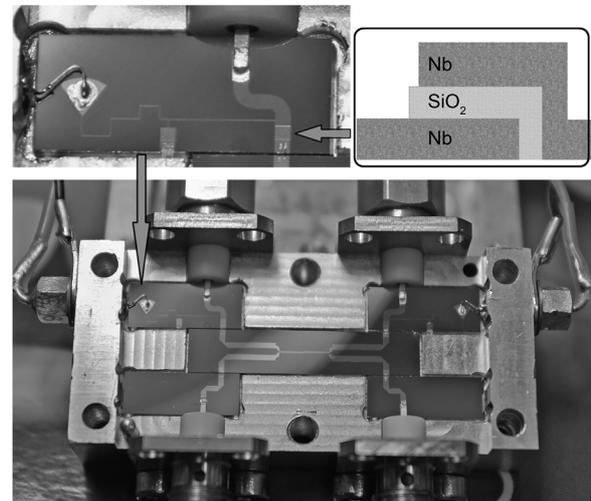


Fig. 2: The hybrid assembly with integrated bias-Ts, top left: layout of the bias-T circuit. Top right: schematic representation of integrated thin-film capacitor. The IF hybrid is placed in the center pocket. The outer dimensions of the assembly are 15 mm high, 43 mm long and 20 mm wide

Fig. 2 shows the IF hybrid assembly. In order to avoid substrate modes, which could compromise the hybrid performance, the IF hybrid is divided into five sections fabricated separately and inter-connected using bond wires. The hybrid chip is placed in the middle with two connecting lines with a bias-T at the input of the hybrid and two connecting lines at the output. The SMA (Radiall 3.5 mm) connectors and all five chips were glued into their respective pockets using cryogenic conducting epoxy. The box housing

of the hybrid assembly has metal walls between the five sections of the hybrid with corresponding metal posts from the top cover.

The bias-T consists of a capacitor that acts as an RF short, a $\lambda/4$ high impedance transmission line to transform this RF short to an open circuit and a DC block capacitor to prevent DC bias from leaking in to the hybrid chip. One side of the RF shorting capacitor is directly connected to the high impedance line and the other side of the capacitor is connected to ground using multiple bond wires (Fig. 2). This bias-T is designed following a MMIC-like approach, where capacitors are integrated on-chip and fabricated using thin-film technology. This approach enables us to fabricate the final product without the need to solder additional components. The integrated capacitors have a MIM structure where the top and bottom electrodes are made of sputtered Nb, whereas the insulator material is SiO₂. All chips entire circuitry, including the hybrid chip, the bias-T and the lines, which is are fabricated using in-house thin-film technology are sputtered on the backside with 0.3 μm Nb/Pd.

E. Measurement results

The measurement uncertainty was estimated using the VNA uncertainty calculator [8]. The amplitude and phase uncertainty is approximately ± 0.2 dB and $\pm 1.5^\circ$ respectively [8]. The measured performance of the hybrid assembly is depicted in Figs. 3-4. The measurement uncertainty in Fig. 3, which is ± 0.2 , is not shown in order to keep the figure as clear as possible.

Figure 3 shows the through and coupled ports, when the test signal is excited at port 1 and measured at port 3 (S_{31} , through port), port 2 (S_{21} , coupled port), port 4 (S_{41} , isolation port) and the reflected signal at port 1 i.e., S_{11} .

The discrepancy between the measurement results and the simulation is due to packaging effects, i.e., SMA connector-to-microstrip transitions, which were not included in the simulations. Furthermore, we cannot exclude the fact that a part of the performance deviation arises from calibration and mounting accuracy: e.g. a small difference of approximately 45 μm in positioning the SMA center-pin itself would result in 1° in phase imbalance [1].

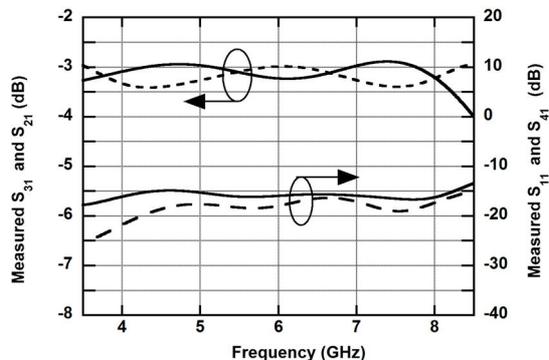


Fig. 3: Measured performance (through, coupled, return loss and isolation) of the hybrid assembly.

Similarly, a variation of approximately 200 μm in the lengths of the bond wires used to connect the bias-T and the transmission line circuit to the hybrid circuit as depicted in Fig. 2 is enough to cause 1° phase imbalance. However,

there is good agreement between the measured and simulated performance (Fig. 4).

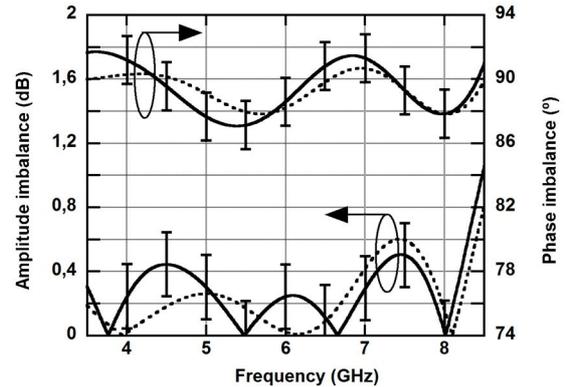


Fig. 4: Simulated and measured amplitude and phase imbalance of the 3-section hybrid, where the dotted curve corresponds to simulated performance and the solid curve represents the measured performance. The error bars indicate the uncorrelated VNA measurement uncertainty.

III. CONCLUSIONS

In this work, we report on the design and characterization of a 4-8 GHz IF assembly comprising a compact 90° hybrid chip, two bias-T circuits and two transmission line circuits. The compact size of the hybrid chip allows it to be integrated into virtually any sideband separating (2SB) mixer operating at cryogenic temperatures and is furthermore especially advantageous for multi-pixel 2SB receivers or low noise balanced amplifier layouts.

The hybrid was fabricated using in-house thin-film technology on Si-substrates and uses air bridges to interconnect the fingers of the coupler. The hybrid assembly that integrates the bias-T circuit using a MMIC-like approach, where capacitors are integrated on-chip and fabricated using thin-film technology. The four-port S-parameters measurement showed good agreement with the simulation results.

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