THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Charge transport in InAs nanowire devices

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Göteborg, Sweden 2013

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ISBN 978-91-7385-941-7

Doktorsavhandlingar vid Chalmers tekniska högskola
Ny serie nr 3622
ISSN 0346-718X

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ISSN 1652-0769
Technical Report MC2-266

Chalmers Reproservice
Göteborg, Sweden 2013

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Abstract

This thesis presents extensive experimental studies of the proximity effect in InAs nanowires connected to superconducting electrodes, radio-frequency single electron transistors based on nanowire heterostructures, and measurement of shot noise in nanowires coupled to superconducting electrodes.

We have investigated proximity induced superconductivity in a large number of InAs nanowire devices with a broad range of lengths at different temperatures and magnetic fields. The nanowires are either placed directly on the substrate or suspended above the substrate with local gates. We have measured the main features of the current-voltage characteristics: Josephson current, excess current, sub-gap current and sub-gap features, and compared them with theory.

In the shortest length device, $L = 30\,\text{nm}$, with very good contact-interface transparencies, we have achieved a record high value of Josephson critical current, 800 nA, an order of magnitude higher than what has been reported by others, and which comes close to the theoretical limit.

The sub-gap current exhibits a large number of structures, some of them are subharmonic gap structures that come from multiple Andreev reflections. The other structures, observed in both suspended and non-suspended devices, are independent of either superconducting energy-gap or length of the wire.

In gate-controlled suspended devices, the current-voltage characteristics manifest different properties depending on the resistance of the device. By applying gate voltage, in devices of relatively higher resistances, we have been able to tune the conductance from a completely insulating regime, via Coulomb-blockade regime, to a superconducting regime, combining different types of transport in a single device. In devices of intermediate resistances, we have been able to observe a cross over from a typical tunneling transport at large negative voltages, with suppressed sub-gap conductance, and negative excess current to a metallic behavior at positive gate voltages, with enhanced sub-gap conductance and positive excess-current.

In suspended devices of short lengths and good ohmic contact-interfaces, for negative gate voltages, the number of conducting channels is reduced gradually and we observe a stepwise decrease of both conductance and critical current before the conductance vanishes completely.

We have also demonstrated a radio-frequency single electron transistor based on suspended InAs/InP nanowire heterostructures. The single electron transistor is defined by introducing two barriers of InP in the middle of an InAs nanowire. The

stability diagram displays Coulomb blockade diamonds with sharp edges at negative gate voltages. We have measured a very high charge sensitivity of $2.5\ \mu e/\sqrt{\mathrm{Hz}}$, comparable to the best conventional Al-SETs. The low frequency noise shows approximately a $1/f$ behavior. The level of the noise is extrapolated to 300 $\mu \mathrm{e}_{rms}/\sqrt{\mathrm{Hz}}$ at 10 Hz.

Keywords: InAs nanowires, nanowire heterostructure, proximity effect, Andreev refelction, supercurrent, sub-gap current, excess current, conductance quantum, single electron transistor, and shot noise.

List of Publications

This thesis is based on the work contained in the following papers:

I: A radio frequency single-electron transistor based on an InAs/InP heterostructure nanowire.
H. Nilsson, T. Duty, S. Abay, C. M. Wilson, J. B. Wagner, C. Thelander, P. Delsing, and L. Samuelson
Nano Letters 8, 872 (2008).

II: High critical-current superconductor-InAs nanowire-superconductor junctions.
S. Abay, H. Nilsson, F. Wu, H. Q. Xu, C. M. Wilson, and P. Delsing
Nano Letters 12, 5622 (2012).

III: Quantized conductance and its correlation to the supercurrent in a nanowire connected to superconductors.
S. Abay, D. Persson, H. Nilsson, H. Q. Xu, M. Fogelström, V. Shumeiko, and P. Delsing
Nano Letters 13, 3614 (2013).

IV: Charge transport in InAs nanowire Josephson junctions.
S. Abay, D. Persson, H. Nilsson, Fan Wu, H. Q. Xu, M. Fogelström, V. Shumeiko, and P. Delsing
Submitted to Physical Review B (2013), arXiv:1311.1745

Contents

Chapter 1

Introduction

In the last 50 years, we have witnessed tremendous advancements in electronic devices. These developments are related to the key active component: *the transistor*. A transistor is a solid-state device that controls the amount of current flow through its two terminals by a means of a third terminal.[1, 2] The first transistor was invented by John Bardeen, Walter Brattain, and William Shockley in 1947, at AT&T's Bell Laboratories.[3] It is one of the greatest inventions of 20^{th} century. In recognition of their work, they were awarded the Nobel Prize in physics (1956). Since then, the transistor has revolutionized the field of electronics and the global society.

Modern Electronics are built on *integrated circuits* (ICs): integration of large numbers of solid state transistors into a small chip. The first working integrated circuit on a Germanium substrate was demonstrated in 1958 by Jack Kilby, who was awarded the Nobel Prize in physics in 2000. Half a year later, Robert Noyce came up with an idea to use Silicon for integrated circuits and it was produced at Fairchild Semiconductor. After that, the electronic industry have seen enormous advancements in producing low cost, less power consumption and high speed electronic devices. These capabilities are strongly linked to the increase in the number of transistors per chip which has been possible due to the continuous down-scaling of transistors. The trend of continuously increasing the density of transistors was stated in *Moore's law*[4, 5] in 1965: the number of transistors on integrated circuits doubles approximately every two years. His observation has been true for more than half a century and it has served as a guide for long-term planning of the semiconductor industry. This has been a result of new innovations[6, 7] and improvements in state of the art fabrication methods. For example, the minimum feature size in transistors shrank from 500 nanometer in 1990 to 22 nanometer in 2012. The trend is expected to continue for another decade (10 nm feature size) but not forever. The statistical nature of dopant atoms, lithography limitations, and quantum effects are expected to impose a limit on down scaling. However, other directions and new materials in research such as *nanowires*[8], a very tiny hair-like solid, are potential alternatives for future nanoscale transistors. In 2010, a first

junction-less Silicon-nanowire transistor, *i.e.* with out doping, was produced with minimum feature size of 10 nanometer.[9] Nanowire transistors have demonstrated performance that in some aspects exceed the limits of the conventional devices.[10]

However, as the minimum feature size gets smaller, quantum effects related to the charge carriers such as energy quantization, interference, spin effects, and tunneling will play a significant role in the current transport. Thus, the future may lie in designing and fabricating nano-scale devices that exploit the quantum effects. For example, the *single electron transistor*(SET)[11, 12] exploits the quantum tunneling effect to control sequential flow of electrons.[13, 14, 15, 16] The drawback of single electron transistor is that it needs to be even smaller than 10 nm to work at room temperature.

Semiconducting nanowires, such as InAs nanowires, provide a promising platform for studying "beautiful" physics at the nano-scale (mesoscopic physics) and could also be the building blocks of nano-scale devices.[15, 17, 18, 19, 20, 21] Nanowires can be made either by carving a bulk solid material to the intended size, a *top-down* approach, or self-assembling (growth) from chemical or physical deposition of growth species, a *bottom-up* approach.[**?**, 22] The nanowires presented in this thesis are grown at Lund University by the bottom-up approach that needs metallic particles to catalyze the growth process. The diameters of the nanowires are determined by the size of the catalysts which can be tuned to sub-100 nm and smaller. There have been intensive studies of electronic and optical properties of different types of nanowires by connecting them to metal electrodes.[15, 17, 18, 19, 20, 21] The contacts are mostly defined in a horizontal configuration: the nanowires are removed from the growth substrate and deposited horizontally on a second substrate.

Nanowires are one-dimensional systems, the electrons are confined in the radial direction and are free to propagate along the length of the wires reducing the degrees of freedom to one, like waveguides in electrodynamics. The confinement of electrons plays a significant role in the electronic properties of the nanowires. In particular, when the Fermi-wavelength of the conduction electrons is comparable to the diameter of the nanowire, the energy spacing between levels become bigger and significant. Semiconducting nanowires also provide the possibility to tune the wavelength by means of electrostatic gates. The number of conducting channels can also be controlled with gate voltages. As a result, at low temperatures, the energy quantization leads to conductance steps with gate voltages.[23] The step heights are given by constants of nature, $2e^2/h$, refereed as *conductance quantum*.

In the bottom-up method, the growth species for the nanowires are essentially unlimited, which gives the possibility to vary the nanowire materials in the the growth direction forming *nanowire heterostructures*. The difference in the electronic properties or the electronic bandstructures, along the nanowire allows to form tunnel-barriers. It is possible to localize the electrons between two tunnel-barriers, a property that can be used to form devices, for example, quantum-confined devices[24, 25] and single electron transistors.[15] The single electron transistor is an extremely charge-sensitive device. The intrinsic working frequency of single

electron transistors can exceed 10 GHz. However, the high resistance of the tunneling barriers and the capacitance of the measurement lines limit the dc-mode operation frequency to below 100 kHz. This operation frequency can be improved by working in the rf-mode: to measure the reflection coefficient of a radio frequency signal from a tank-circuit where the single electron transistor is embedded.[26, 27]

Another research interest has been in nanowires connected by superconductors (S).[28, 21] Superconductors are materials where a significant fraction of the free electrons occupy a macroscopic quantum state at temperatures below the superconducting transition temperature. In the superconducting state the electrons are paired into Cooper-pairs and their collective motion leads to a flow of charge without any dissipation. The superconducting condensate state is protected from other dissipative states by an energy gap Δ.

In S-nanowire-S hybrid devices, the nanowire serves as a weak link between the two superconducting electrodes. The nanowire gets superconducting properties by being in proximity to the superconductors, a property known as the *Proximity effect*. The proximity effect can extend over a large length scale (the coherence length) in the nanowire which is crucial for observing it in sub-micron devices, for example, a flow of supercurrent due to the phase difference between the two superconducting condensates.[21, 29, 30]

The maximum supercurrent that can flow through the weak link depends on the electrical properties of the nanowire and the contact-interface qualities. Among a variety of nanowires tested in experiments, nanowires of InAs play a central role.[21, 29] This is due to their material properties: high electron mobility, low effective mass, and pinning of the Fermi level in the conduction band that permits highly transparent galvanic S-nanowire contacts. The semiconducting nature of the nanowires also allows to tune the carrier density and hence, the coherence length by gate voltage. This tunes the maximum supercurrent with the gate voltage.[21, 29, 30] In a ballistic nanowire, *i.e* scattering free, the supercurrent is expected to change in steps correlated with the conductance quantum.

At non-zero voltages, $|V| \leq 2\Delta/e$, a dissipative current flows due to *Andreev reflections*[31], a mechanism that converts a dissipative current in the nanowire to a dissipation-less current in the S-electrodes. An electron that undergoes Andreev reflection at an ideal interface, transfers a Cooper-pair (two electrons) to the S-electrodes, at the same time a hole is reflected in the nanowire. This process enhances the sub-gap conductance by a factor of two compared the normal conductance. At $|V| < \Delta/e$, an electron can be n-times (multiple) Andreev reflected transferring (n+1) electrons to the superconductor. The onset of the n^{th} process happens at $|V| = 2\Delta/ne$. That is, the effective charge transfered per electron increases with decreasing the voltage. This effective charge can be finger-printed by measuring the shot-noise properties of the weak-links.

In this thesis there are seven chapters that contain the following:
Chapter 2: contains the basic theoretical background necessary for the thesis work. It includes electron transport in mesoscopic devices, Andreev reflections, Josephson current, sub-gap current, single electron transistor, radio-frequency single elec-

tron transistor and shot noise.
Chapter 3: covers experimental techniques: Growth and fabrication of nanowire devices, and measurement set-ups for both dc- and rf-read out.
Chapter 4: describes experimental and theoretical results of non-suspended InAs nanowires connected to superconducting electrode. It covers normal state properties, excess current, supercurrent, sub-gap current, and sub-gap features.
Chapter 5: summarizes the experimental results for the gate-controlled suspended devices.
Chapter 6: presents experimental results of the radio-frequency read-out on single electron transistors based on InAs/InP heterostructure nanowires.
Chapter 7: Conclusion and outlook.

Chapter 2

Theoretical background

2.1 Electron transport in semiconductor devices

The wave nature of the electron was predicted by L. de Broglie in 1924[32]: a moving electron has a wavelength inversely proportional to its momentum, $\lambda = h/p$, where h is the Plank constant. Davisson and Germer (1927) demonstrated [33] the wave-like nature of the electron by shooting a narrow beam of electrons at a surface of a crystal. The reflected beam displayed an interference pattern.

In mesoscopic devices, the phase of the electron wave can persist up to length-scales comparable to the device dimensions and plays an important role in the transport properties. The wave-like properties of electrons has been demonstrated in mesoscopic metal rings [34] where an electron wave-function splits into two paths. When the wave functions re-combine at the other end-point of the ring, the conductance displays interference effects as a function of the phase difference acquired between the two paths.

In perfect crystals, the atoms are arranged in a periodic lattice. The electrical properties of such crystals is described by the electronic band-structures, a powerful and simple model for electrons in solids. To get the band-structure, there are several models with slightly different assumptions and derivations. However, these band theories agree that electrons in the periodic crystals may possess energies within certain bands (allowed energies) but not outside them (energy gaps).

In equilibrium, the allowed energy states are filled with electrons, according to the Pauli exclusion principle and also taking into account spin degeneracy. The electrical properties depend on the number effective charge carriers, which in turn depends on if the highest occupied energy band is completely filled or not. Insulators are materials with completely full bands, there are no available free states to scatter into and electron transport is not allowed. Metals are materials with energy bands half-filled at the highest occupied level. Semiconductors are insulators but with smaller energy gaps in-between the highest-occupied and the lowest- empty band, and conductivity can be achieved by doping or elevated temperatures.

In semiconductors, electrical conduction happens either through electrons in

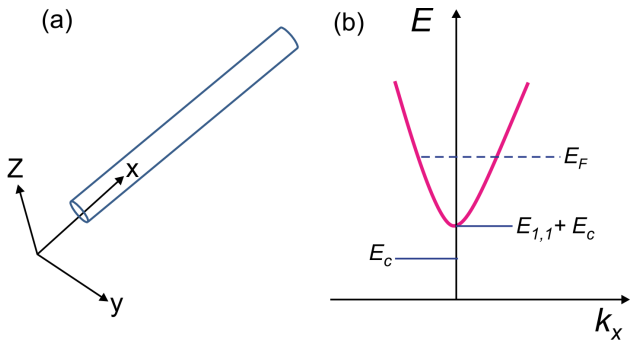

Figure 2.1: (a) A simple sketch of a nanowire. Electrons in the nanowire are free to propagate in the x-direction but are confined in the y-z direction giving transverse quantization. (b) Dispersion relation E-k in a semiconducting nanowire. The first-sub band is filled with electrons up to a Fermi-energy E_F.

the conduction band or holes in the valence band. The dynamics of the electrons in the conduction band can be expressed in a simplified description by the single-band effective mass equation,[35]:

$$\left[E_{CB} + \frac{(i\hbar\nabla)^2}{2m^*} + U(\vec{r})\right]\Psi(\vec{r}) = E\Psi(\vec{r}) \tag{2.1}$$

where E is the energy, $\hbar = h/2\pi$ and E_{CB} is the energy at the bottom of the conduction band, U(r) the potential energy due to impurity atoms, or an inhomogeneous lattice *etc.*, and m^* is the effective electron mass.

The effect of the periodic lattice potential on the wave-function is taken into account through the effective mass: the electrons in the semiconductor move like free electrons in vacuum but with a different effective mass m^*. The effective mass is related to the band curvature and its value is a measure of the coupling between the charged carriers and the lattice.

The solution of the wave-function calculated from eq. 2.1 depends on the boundary conditions and the dimensionality of the system. Dimensionality (0d, 1d, 2d, 3d) refers to the number of degrees of freedom in the electron momentum. For example, in a 2-dimensional electron gas (2DEG), the electrons are free to propagate in a plane but are confined by some potential in the direction perpendicular to the plane.

2.1.1 Nanowires

Nanowires are solid materials in the form of a wire with a diameter from a few nanometers to 100 nm, and lengths from a few nanometers up to a few of microns. A nanowire is a one dimensional system, the electrons are confined in two directions (y, z) and are free to propagate along the length of the wire (x) reducing the degrees of freedom to one, like waveguides in electrodynamics. A sketch of a nanowire is shown in Fig. 2.1a.

The electronic wavefunction in nanowires can be written as a product of the free-carrier solution in the x direction and the confined solution in the y-z directions:

$$\Psi(r) = \phi_{n,m}(y,z)\exp(ik_x x) \tag{2.2}$$

where k_x is the wavenumber in the x-direction. This results in the following dispersion (*E-k*) relation:

$$E = E_{CB} + E_{k_x} + E_{n_y,n_z} = E_{CB} + \frac{\hbar^2 k_x^2}{2m^*} + \frac{\hbar^2\pi^2}{2m^*}\left(\frac{n_y^2}{L_y^2} + \frac{n_z^2}{L_z^2}\right) \tag{2.3}$$

where L_x, L_y and L_z are the dimensions of the nanowire along the x-, y-, and z-directions, respectively.

The dispersion relation in eq. 2.3 shows a continuum of one-dimensional states associated with each pair of integers n_x, and n_y. The transverse quantum states n_x, and n_y are said to be the modes, the sub-band or the quantum channels. The confinement effect depends on both the nanowire dimensions (or diameter) and the effective mass. Therefore, the quantization effect in InAs nanowires is expected to be large as a result of its relatively low effective electron mass. In fact, in InAs nanowires with very small diameter, (below ~ 30 nm), the lowest energy sub-band is pushed well above the Fermi level. As a result, it is difficult to make ohmic contacts with metals and such nanowires hardly conduct at zero gate voltage.

Density of states

The nanowires are assumed to be of sufficiently long length L. A simple periodic boundary condition dictates that the allowed k_x values are such that $k_x = n_x 2\pi/L$. The number of available states per unit length of k-space is thus $L/2\pi$. Taking the $E-k$ dispersion in eq. 2.3 and the spin degeneracy ($\times 2$) into account, the density of energy states per unit length and per unit energy in the 1D case is given by:

$$D(E) = \frac{(2m^*)^{\frac{1}{2}}}{\pi\hbar}\frac{1}{\sqrt{E}} \tag{2.4}$$

The probability that a state is occupied by an electron is given by the Fermi-Dirac distribution function:

$$f(E) = \frac{1}{e^{(\epsilon - E_F)/k_B T} + 1} \tag{2.5}$$

At zero temperature, all the energy states below the Fermi energy E_F are filled and all states above the Fermi energy are empty. Therefore, the equilibrium electron density n_s, the total number of conduction electrons per unit length, can be estimated by counting how many of the available states D(E)dE are occupied above the conduction band:

$$n_s = \int_{E_c}^{E_F} D(E)f(E)dE = \frac{\sqrt{8m^*(E_F - E_{CB})}}{\pi\hbar} \tag{2.6}$$

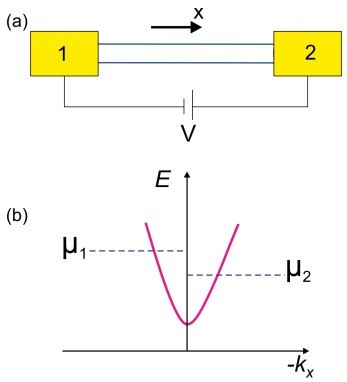

Figure 2.2: (a) A ballistic nanowire connected to two metal contacts. b) A single sub-band occupied according to the electro-chemical potentials (quasi-Fermi states) μ_1 and μ_2 of the contacts. The positive k-states are occupied by electrons coming from the left contact while the negative k-states are occupied by electrons coming from the right contact.

The low dimensionality changes the density of states and affects the filling of the energy states up to the Fermi level which is directly related to the effective number of charge carriers. The Fermi-wave number k_F can be expressed in terms of the charge density, $k_F = n_s\pi/2$. The corresponding Fermi velocity will be $v_F = \hbar k_F/m^*$.

2.1.2 Normal current transport

In a hybrid device consisting of a nanowire and metals, electrical conduction is established through the nanowire from/to the metals at the ends. The electrical conductance is determined by how far the charge carriers freely travel in the wire. The mean free path can be affected by the presence of scattering centers. These could cause elastic scattering or inelastic scattering. The elastic scattering is caused by static faults like atomic defects, impurities, and charge traps on the nanowire surface. The inelastic scattering comes from non-stationary or time varying scattering centers like temperature dependent electron-phonon interaction, and electron-electron interactions. This inelastic scattering randomizes the phase of electrons and could wash-out any interference effects for lengths longer than the phase coherence length l_ϕ.

The characteristic length scales: the geometrical length L, elastic l_e and inelastic scattering length l_i, and phase coherence length l_ϕ determines the carrier transport properties in the nanowire. For example, the relative size of the device L and the elastic scattering length determines whether the transport behavior is ballistic ($l_e > L$) or diffusive ($l_e < L$). Similarly, the phase coherence length indicates whether the transport will show quantum interference effects or not.

A sketch of a nanowire connected to metals is shown in Fig. 2.2a. The metals are filled with electrons up to maximum energy given by electrochemical potential (μ_1 and μ_2). To get a net current through the nanowire, the right going states are

only filled from the left reservoir and will be occupied up to μ_1. Similarly, the left going states are only filled from the right reservoir and will be occupied up to μ_2. The net current is determined by the difference in the right going current and the left going current, which in turn is determined by the electrochemical potential difference $\mu_1 - \mu_2 = eV$. Considering a ballistic nanowire with only a single sub-band, the current through a single mode m is given by the product of the (1D) density of electrons and the velocity, $I = env$:

$$I_m = 2e \int_{\mu_1}^{\mu_2} v(E)D(E)dE \tag{2.7}$$

The product of the density of states in the nanowire, $D(E) = (2\pi\partial E/\partial k)^{-1}$ and $v(E) = (\partial E/\partial k)/\hbar$ is $1/h$, a universal constant, independent of the energy dispersion $E(k)$ or the sub-band mode number m. The current for a single mode will then be:

$$I_m = 2e \int_{\mu_1}^{\mu_2} v(E)D(E)dE = \frac{2e}{h}(\mu_1 - \mu_2) = \frac{2e^2}{h}V \tag{2.8}$$

For N number of channels in-between μ_1 and μ_2 , the total current is the sum of the currents contributed by each mode:

$$I = \sum_{m=1}^{N} I_m = N\frac{2e^2}{h}V \tag{2.9}$$

The conductance can be drived from the current:

$$G = I/V = N\frac{2e^2}{h} \tag{2.10}$$

This is the celebrated universal conductance[36] for two terminal ballistic nanowire. The conductance is quantized in units of the conductance quantum, $2e^2/h$ and increases step wise with the number of channels N which depends on the the diameter of the nanowire.

The generalization of Eq. 2.10 is given by scattering theory of transport, the Landauer formalism,[36] for a conductor with arbitrary average transmission probability T':

$$G = I/V = N\frac{2e^2}{h}T' \tag{2.11}$$

In a ballistic point contact, realized for example in a two-dimensional gas (2DEG), the channel width and hence the number of conducting channels can be controlled by means of split gates. As a result, as the width is continuously reduced, the conductance decreases in steps with a step height of the conductance quantum $2e^2/h$.[37, 38] However, besides non-zero temperature, the backscattering of carriers from impurities situated nearby the constriction smears out the conductance steps. In particular, backscattering is critical in nanowires due to the

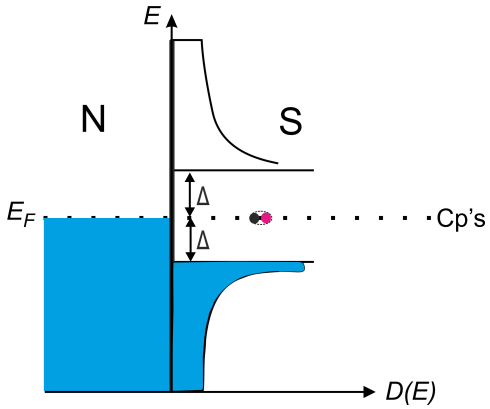

Figure 2.3: Density of states of a normal metal in contact with a superconductor. In the normal metal, there exist finite density of states at and around the Fermi level. The available empty states above the Fermi-level provides the phase-space to scatter and allow charge transport. A semiconductor representation of the density states for a superconductor at $T \ll T_c$. The macroscopic quantum state is occupied by a Cooper-pair condensate at the Fermi-energy. The Cooper-pairs are separated from the quasi-particle states by the superconducting gap Δ, *i.e*, there no free available quasi-particle states within the energy-gap.

small diameter which enhances the probability of electrons being reflected back from impurities or the confinement walls before they arrive in the reservoirs. For this reason, the quantization in nanowires has been difficult to observe and has only been reported recently in nanowires at high magnetic field, applied to suppress the backscattering.[23] In this thesis, we will demonstrate conductance quantization in gate-controlled semiconducting nanowires at zero magnetic field, see appended paper III.

2.2 Superconductor-normal (NS) transport

This section focuses on transport properties of electrons in nanowires connected by superconductors. The superconducting electrodes induce superconducting properties in the nanowire by being in proximity. This proximity effect is manifested in the electronic transport properties of the nanowire devices, such as the flow of a supercurrent. The proximity effect is microscopically understood in terms of Andreev reflection[39, 40, 41], a concept that I will discuss after a brief introduction to superconductivity.

Superconductivity

In 1908, Heike Kamerlingh Onnes liquefied helium for the first time and opened a new chapter in low temperature physics. Three years later, in 1911,[42] he discovered superconductivity. While investigating resistance of different metals in helium

liquid, he observed that the resistance in a sample of mercury dropped by several orders of magnitude below a transition temperature of $T_c \approx 4.15\,\mathrm{K}$. He wrote in his notebook: "The temperature measurement was successful. The resistivity of Mercury is practically zero".

Superconductivity is a macroscopic quantum effect, below a critical temperature T_c a finite fraction of the electrons are condensed into a single state described by a single wave function $\Psi(r) = |\Psi| \exp i\phi(r)$. The striking properties of superconductors such as the vanishing of the resistance, and the Meissner effect[43] (perfect dia-magnetism) that may make them levitate, are related to the energy spectrum.

There had been different phenomenological theories to explain superconductivity but in 1957, Bardeen, Cooper, and Schrieffer proposed the first microscopic theory of superconductivity, which is commonly named the BCS theory.[3] The underlying principle of the theory is based on a phonon mediated interaction between two electrons that allows them to pair up into Cooper-pairs.

A common picture to describe the mechanism of superconductivity is the following: a moving conduction electron interacts with lattice atoms via the Coulomb interaction and deforms the crystal lattice (or emits a phonon). A second electron moving through the same region feels an attractive electrostatic potential which is generated by the deformed lattice (or absorbs a phonon). Under certain conditions, when this phonon mediated attractive interaction becomes stronger than the direct repulsive electrostatic force, it results in a net attractive interaction.

In superconductors, below the critical temperature T_c, the net attractive interaction leads to the formation of Cooper pairs. Cooper-pairs are two coupled electrons with opposite momenta $\vec{k}$ and $-\vec{k}$ and opposite spins. The Cooper-pairs which are Bosons and therefore obey Boson-statistics, form condensate. The Cooper pairs are strongly correlated and they form coherent state with a well defined phase,ϕ.

The formation of the condensate opens an *superconducting energy-gap* 2Δ symmetric around the Fermi surface, in which there is no density of states for single electrons (or quasi-particle excitations). This energy-gap is responsible for the striking properties of the superconductors. That is, there is a minimum energy 2Δ needed to break Cooper-pairs, they are protected by the energy-gap and hence can carry a dissipation-less current.

The size of the gap depends on temperature and magnetic field. The gap increases with decreasing temperature below T_c and has a maximum value at zero temperature, $\Delta(0) \approx 1.76\, k_B T_c$, where k_B is the Boltzmann constant.

In normal metals or in InAs nanowires where the Fermi-level is pinned in the conduction band, there exists a certain density of states for electrons at the Fermi-level which ensures electron transport though them. The dynamics of the conduction electrons, or the holes is independently described by the Schrödinger equation. However, in superconductors, the electron-like and hole-like quasi-particles are coupled by the superconducting condensate and the quantum dynamics of the quasi-particles is described by the Bogoliubov-de Gennes (BdG) equation[44], which describes of two coupled Schrödinger equations.

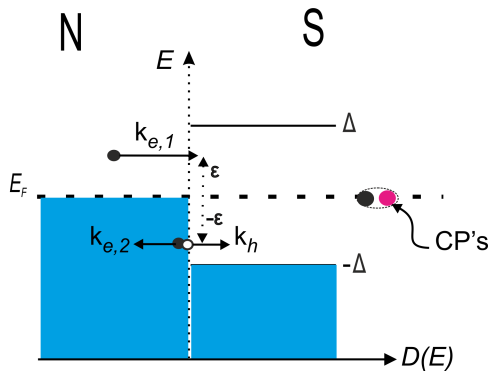

Figure 2.4: (a) Schematic picture of Andreev reflection at an NS interface. When an electron comes to the NS interface at energy $\epsilon < \Delta$ and momentum $k_{e,1}$, it sees no available quasi-particle states in S to scatter into. Rather, it gets reflected as a hole (or drags second electron from N with opposite momentum $k_{e,2}$ and spin) at an energy $-\epsilon$ thereby transferring a Cooper-pair to the superconductor S. The electron is retro-reflected as a hole which traces back the path of the incident electron. The phase of the reflected hole carries information of the phase of the incident electron and the macroscopic phase of the superconductor.

2.2.1 Superconductor-nanowire (NS)

As has been stated above, when a normal metal N is interfaced by a superconductor S, and if there is good electrical contact between the two, Cooper pairs can leak from S to N, a property known as the *proximity effect*. The coherence length or the superconducting correlation of the cooper-pairs can extend over a large length scale in the normal metal. This is crucial for observing superconducting properties induced in sub-micron normal devices, such as for nanowires.[21, 28, 29, 30, 45, 46] The microscopic understanding of the proximity effect is based on what happens at the interface, Andreev reflection, and on how long the electron-hole pairs can travel in the nanowire before the phase randomizes, the phase coherence length ξ. I consider the Fermi-level energy as the reference energy for the forthcoming discussion.

Andreev reflection

To establish current flow through the NS junctions, electrons have to cross from the normal metal to the superconductor through the N/S interface. Electrons coming from N at energy $\epsilon > \Delta$, can enter the unoccupied quasi-particle states in the superconductor. However, electrons incident at energies $\epsilon \leq \Delta$ on the other hand finds no available quasi-particle states to scatter into, charge transfer is forbidden and no current flows in terms of normal scattering. Normal reflection is also unlikely as there is no barrier at the interface to absorb the momentum difference.

However, charge transfer is possible if second order processes are allowed. That is, if the incident electron at energy ϵ and momentum $\vec{k}_{e,1}$ drags another

electron from N at energy $-\epsilon$ of opposite momentum $-\vec{k}_{e,2}$ and spin with it, to form a Cooper pair in the superconductor. In other words, if the incident electron is reflected as a hole, or vise versa. This mechanism of converting a dissipative electron current in the normal N to a dissipation-less Cooper-pair current in the superconductor is known as *Andreev reflection*. Andreev described this process in 1964 while studying heat transport at NS interfaces.[41] The Andreev reflection conserves momentum, energy (elastic) and charge at the interface.

The reflected hole possesses opposite momentum $\vec{k}_h$ to that of the second dragged electron $-\vec{k}_{e,2}$, but in the same direction as the incident electron $\vec{k}_{e,1}$. Owing to the negative effective mass, the group velocity of the hole is opposite to its momentum and the hole moves opposite to the incident electron. It traces back the path of the incident electron, this is called retro-reflection.

Dephasing

The tracing back of the original path of the electron is perfect when the incident electron comes at the Femi-energy or has the same momentum as the reflected hole. However, if the incident electron energy is different from the Fermi-energy, there will be a momentum difference δk with the reflected hole which can be estimated from their energy difference $\Delta E = 2\epsilon$ as:

$$\delta k \approx \Delta E \times (\frac{\partial E}{\partial k})^{-1} = \frac{2\epsilon}{\hbar v_F} \tag{2.12}$$

The wave-vector mismatch δk introduces a phase difference $\delta\phi = \delta k \cdot d$ in-between the incoming electron ($k_F + \epsilon/\hbar v_F$) and the reflected hole ($k_F - \epsilon/\hbar v_F$) after traveling a distance d in the nanowire. If this phase difference becomes larger than π, the initial in-phase condition is changed to out-of-phase. This happens after traveling distance $\pi/\delta k = \pi\hbar v_F/2\epsilon$. The phase coherence length ξ, the typical distance which an electron travels before the phase randomizes, in a ballistic nanowire is thus given by $\xi_0 \approx \hbar v_F/\Delta$.

To express the phase coherence in the diffusive case, we need to consider the dephasing time $\tau_D = \xi_0/v_F \approx \hbar/\Delta$ in the nanowire. The diffusive phase coherence length will have the form $\xi_D = \sqrt{D\tau_D} \approx \sqrt{\hbar D/\Delta}$, where $D \approx v_F l_e/3$ is the diffusion constant in the nanowire. This is the length scale over which an electron or hole diffuses during the time τ. In our InAs nanowire devices, we have estimated a phase coherence length of approximately 1.3 μm and 250 nm for the ballistic and the diffusive cases, respectively.

The most important property of Andreev reflection is that the reflected hole carries information of both the phase of the incident electron and the macroscopic phase ϕ_S of the superconductor. This energy dependent phase shift in the reflection follows from the matching of the BdG wave-functions at the interface:

$$\phi_h = \phi_{e,1} + \phi_S + \arccos(\frac{\epsilon}{\Delta}) \tag{2.13}$$

The effect of interferences

The above discussion considers ideal interfaces and that every incident electron is Andreev reflected as a hole, transferring a Cooper-pair with a charge of 2e and vice versa for an incident hole. Therefore, the sub-gap conductance G_{NS} at $eV \leq \Delta$ is twice as large as that of the normal conductance G_{NS} at $eV > \Delta$, which is the same as the conductance of the normal metal-nanowire (N-N) G_{NN}, at $T \geq T_c$. However, in real NS interfaces, there exists a potential barrier coming from different physical origins such as the Fermi-velocity mismatch, formation of Schottky barriers, oxides, and charge-space inhomogeneities. This results in normal scattering (e $\rightarrow$ e or h $\rightarrow$ h reflections) and suppresses the probability of Andreev reflection, which complicates the observation and analysis of the proximity effect.

In semiconducting nanowires, besides the presence of Schottky barriers, the impurities on the surface play an important role, and make it difficult to achieve high transparency interfaces. At low temperatures, this suppresses the proximity effect. However, the presence of charge accumulation at the surface of InAs nanowires helps to form Schottky barrier-free contact interfaces. To make transparent contact-interfaces, we also remove the native oxide and impurities on the surface prior to metal evaporation.[47]

To describe the quasi-particle transport, Blonder, Tinkahm, and Klapwijk (BTK) extended the Landauer formalism to the NS junctions.[31] They used the solutions, electron- or hole-like wave functions, of the BdG equation to calculate the probability of Andreev reflection at the NS interface. The normal scattering happens only at the interface, neither in N nor in S. The scattering at the interface is modeled by a delta-function potential, $V(x) = H\delta(x)$. The transmission probability through the barrier is given by $T_b = 1/(1 + Z^2)$, with the parameter $Z = H/\hbar v_F$.

In the BdG equations, the superconducting pair-potential is given by a complex $\Delta = |\Delta| \exp(i\phi_S)$, where $|\Delta|$ is the energy-gap and ϕ_S is the superconducting phase. In the NS systems the energy gap Δ is inhomogeneous with position. In the normal part, $\Delta = 0$.

Matching the wave-functions at the NS interface, BTK calculated the probabilities of Andreev reflection $A(\epsilon)$, normal reflection $B(\epsilon)$. The current through the NS interface is calculated from the probability currents in the nanowire region. This has been done by summing up the Andreev reflection contribution $A(\epsilon)$, and the normal reflection contribution $B(\epsilon)$ in a similar fashion as in the Landauer formalism:

$$I(V) = \frac{G_0}{e} \int_{-\infty}^{\infty} [f_0(\epsilon + eV) - f_0(\epsilon)][1 + A(\epsilon) - B(\epsilon)] d\epsilon \tag{2.14}$$

At low temperatures and small voltages, which has been the case in our measurements, the first factor is approximated by eV. The conductance G_{NS} is then given by the reflection probabilities:

$$G_{NS} = \frac{dI}{dV} = G_0[1 + A(\epsilon) - B(\epsilon)] \tag{2.15}$$

In the absence of elastic scattering $Z = 0$: $B(\epsilon) = 0$, and $A(\epsilon) = 1$, then $G_{NS} = 2G_{NN}$. This enhancement of conductance is manifested also at higher voltages as an excess current. The excess current is the current added to the normal current as a result of the Andreev reflection. It is defined as:

$$I_{exc} = I - \frac{V}{R_N} \tag{2.16}$$

at $V \gg 2\Delta$, where R_N is the normal resistance.

The BTK model describes incoherent carrier transport which excludes coherent transport such as the supercurrent. That is, there is only normal scattering at the NS interface but not in the nanowire, no backscattering or interference effects of quasi particles are considered. However, if the nanowires are phase coherent but diffusive, the incident electron will scatter from the impurities and reach back to the interface. At the interface it could be Andreev reflected as a hole or be partially reflected as an electron. The hole traces back the path of the electron. The partially reflected electron can also be scattered from the impurity to the superconductor and so forth. This coherent transport enhances the Andreev reflection probabilities and hence, enhances the conductance. This process is known as the *reflection-less tunneling*.[48] Taking such processes into account, Beenaker has generalized the expression of the sub-gap conductance in eq. 2.15 for any arbitrary transmission probabilities of the channels T'_n:

$$G_{NS} = \frac{2e^2}{h} \sum_{n=1}^{N} \frac{2T'^2_n}{(2 - T'_n)^2} \tag{2.17}$$

This implies that for any T'_n, $G_{NS} \leq 2G_{NN}$. For the special case of a ballistic nanowire $T'_n = 1$, we have $G_{NS} = 2G_{NN}$, which reproduces the ballistic case of the BTK. In the tunneling regime $T'_n \ll 1$, G_{NS} is proportional to T'^2_n and drops far below G_{NN}. This suppression of the sub-gap conductance could result in a negative excess current (deficit current).

In semiconducting nanowires, the transmission probabilities could be changed by a means of a gate voltage. This allows to cross over from the tunneling regime (NIS) with deficit current to the conducting regime (NS) with positive excess current. The cross over from NS to NIS has been demonstrated in adjustable atomic break junctions and in the appended paper IV.[49, 50]

2.2.2 Superconductor-nanowire-superconductor (SNS) junctions

When the nanowire forms a weak link between two superconductors, we get an SNS junction. In such devices, the phase difference between the superconductors plays a significant role in the coherent electronic transport such as the flow of a supercurrent, excess current and subharmonic gap structures.

The coupling strength of the weak link depends on the electrical properties of the nanowire and the interface qualities. Such junctions are often classified

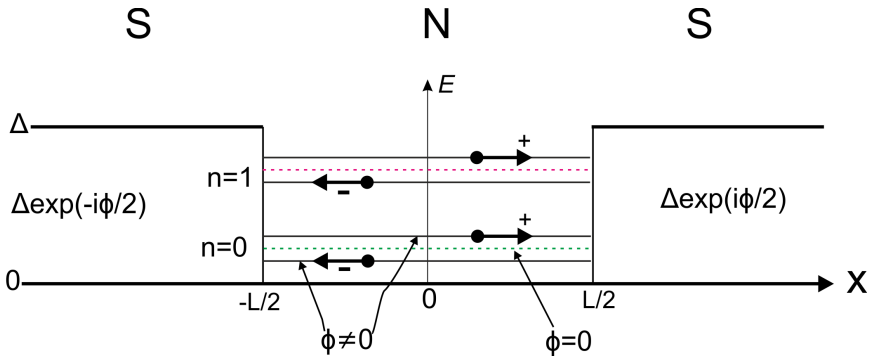

Figure 2.5: (a) Schematic representation of the Andreev bound states in the N region for only positive energies (electrons). The dashed lines show the degenerate states at zero phase difference $\phi = 0$. At non-zero phase difference $\phi \neq 0$, the right and left-going states are indicated with arrows.

based on the relation between the inter-electrode distance L and the characteristics lengths in the nanowire, such as the coherence length ξ and the mean free path l_e. The weak links with $L \ll \xi$ are called short junctions, and those with $L \gg \xi$ are called long junctions. The weak links are further classified to be in the dirty $l_e \ll \xi$ or clean limit $l_e \gg \xi$. Finally, if $l_e \ll L$ the device is classified as diffusive, and in the opposite case $l_e \gg L$ it is ballistic. Most of the devices that we have studied in this thesis are short, dirty and diffusive devices. However, in many cases, the length scales are comparable.

Supercurrent

In the Andreev reflection process, the reflected hole carries information of the phase of the first superconductor $\phi_{S,1}$. When it is retro-reflected, it passes through the nanowire and reaches at the other superconductor. The hole is then Andreev reflected as an electron which carries information of the phase of second superconductor $\phi_{S,2}$. The periodic process creates discreet Andreev bound states in the nanowire that carries supercurrent as a result of the phase difference between the two superconductors $\phi = \phi_{S1} - \phi_{S,2}$. The existence of a Josephson current through a normal metal was pointed out by de-Gennes in 1964.[51]

The early work of supercurrent based on the BdG equations has been done by Kulik[52] and Ishii[53], assuming the two NS interfaces are ideal, Z=0, giving perfect Andreev reflections $A(\epsilon) = 1$ at $\epsilon \leq \Delta$. Matching the values and the derivative of the wave-function at $x = \pm L/2$, the dispersion is given by:

$$\exp(2i\alpha(\epsilon))\exp[i(k^+ - k^-)L]\exp(\pm i\phi) = 1 \tag{2.18}$$

where, $k^+ = k_e$ and $k^- = k_h$ are the wave-vectors for electron and hole, respectively. The energy dependent phase factor $\alpha(\epsilon) = \arccos(\epsilon/\Delta)$. From Eq. 2.18, we see that the total phases acquired sum up to a multiple of 2π. That is, to have

a quantum state after performing one cycle e→ h→e, the electron returns to its initial position with the same phase plus $2\pi n$, where n is an integer number. Using eq. 2.12, the energy-dispersion of the *Andreev bound states* will be:

$$\epsilon_n^{\pm} = \frac{\hbar v_F}{2L}[2(\pi n + \arccos(\epsilon/\Delta)) \pm \phi] \tag{2.19}$$

where $n = 0, 1, 2, ...$ The $\epsilon_n^{\pm}$ indicates the energy spectrum for right (positive) and left (negative) going electrons.

The most important result of eq. 2.19 is that the discrete Andreev levels depend on the phase difference ϕ. That is, for a given state n, the momentum of the right going (k_e^+) differs from that of the left (k_e^-) moving electron by an amount that is linearly dependent on the phase difference ϕ. This means for a given temperature, the energy levels (right and left going) will be filled according to the Fermi-function. This further implies there will be a net current carried by the state n. For $\phi = 0$ the right going and the left going contribute equally and the net current is zero.

Recently, the first tunneling spectroscopy of individually resolved Andreev bound states has been reported in a nanotube-superconductor device.[54]

The supercurrent through the discrete levels is obtained from the energy-phase relation:

$$I = \frac{2e}{\hbar} \sum_n \frac{\partial \epsilon_n}{\partial \phi} \tag{2.20}$$

Short junctions

In short ($L \ll \xi$) and ballistic ($L \ll l_e$) junctions, with no barrier at the interface $T' = 1$, there will be only one state and the energy-phase relation in eq. 2.19 reduces to a simple expression:

$$\epsilon = \pm\Delta \cos(\phi/2) \tag{2.21}$$

This has been generalized to finite transmission value T_n' in the normal region by Beenaker.[48] The energy levels are expressed by:

$$\epsilon_n = \Delta[1 - T_n' \sin^2(\phi/2)]^{1/2} \tag{2.22}$$

In superconducting point contacts, ($L \ll \xi$) with $T_n' = 1$, the Andreev states are given by eq. 2.21. The supercurrent at zero temperature $T = 0$, will then be $I = N(e\Delta/\hbar)\sin(\phi/2)$. This corresponds to a critical current $I_c = N(e\Delta/\hbar)$ which is quantized in units of $e\Delta/\hbar$. Such quantization of the critical current have been reported in two dimensional electron gas systems defined in semiconductor heterostructure.[55, 56, 57] However, the critical currents are normally much smaller than predicted by theory.

In suspended nanowire with local gates stepwise increase of the critical current has been observed, see in appended paper III.[58] The formation of a point-contact-like constriction in the nanowire can be understood from the local-gate

configuration. The local-gate, some 15 nanometers below the nanowire, is effectively coupled to the conducting channels. When the gate voltage is stepped to low negative values, the electric field starts to gradually deplete the lower section of the nanowire of electrons. At more negative-gate voltage, the depletion depth increases and a point-contact like constriction is created on the top-side of the nanowire before it is completely depleted of carriers. When the width of this constriction is comparable to the Fermi-wavelength, the transverse momentum is quantized and the free motion of the carrier is restricted to one dimension. The wave nature of the carriers is observed in the conductance quantization. The number of conductance modes is determine by the constriction area.

Long junctions

The critical current in long ($L \gg \xi$), and ballistic ($L \ll l_e$) junctions, was calculated by Kulik [52]. Taking the expression for $\epsilon_n^{\pm}$ in eq. 2.19 into eq. 2.20 gives that each level carries a supercurrent with a maximum value, critical current, of ev_F/L. At $\epsilon \ll \Delta$, the lowest levels are evenly spaced with the number of levels approximately given by L/ξ. Resulting in a critical current of :

$$I_c = \frac{ev_F}{\xi} \tag{2.23}$$

I_cR_n Product

The *characteristic voltage* of the Josephson junction, the I_cR_n *product*, is a measure of the coupling strength of the nanowire or the quality of the device. It takes different values depending on the nature of the junction. For example, at $T = 0$, for short devices, the product depends on the superconducting gap Δ, *i.e*, $I_cR_n = c\Delta/e$, where c is some constant describing either ballistic $c = \pi$ or diffusive $c = 2.07$ devices.[59] For a tunnel junction $c = \pi/2$.

In SNS devices, the magnitudes of the critical currents that have been reported are relatively small, typically of the order of 50 nA or smaller. The small critical currents are at least partly due to the long channel lengths but also to non-ideal interface transparencies.[29, 28] Fabrication of short channel devices is limited by the resolution of electron beam resist, in particular, for electrodes as thick as the diameter of the nanowires. Using double lift-off nanofabrication process [30] enabled us to make very short length devices, as short as 30 nanometer, together with good ohmic contacts, see appended paper II. This increased the magnitude of the critical current by almost an order of magnitude compared to earlier reports.[29, 28] Subsequently, the I_cR_n product improved to a value comparable to Δ, with $c = 1.0$.

Temperature dependence of critical current

The discrete Andreev bound states carry the net supercurrent which is driven by the phase difference. As have been stated above, the net current is proportional to

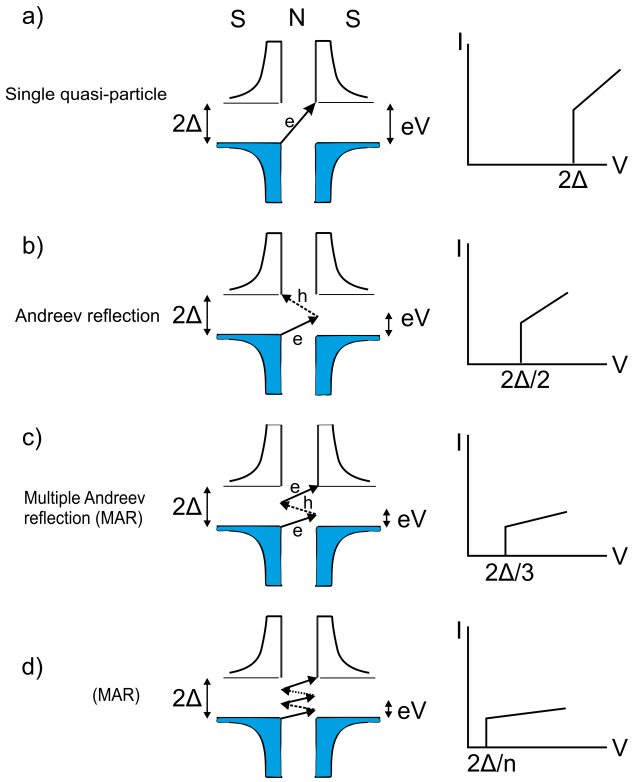

Figure 2.6: (a) Schematic representation of the multiple Andreev reflection in the tunnel limit. The right hand side shows the current contribution of each process.

the energy spacing induced by the phase difference. For a given state n, when the energy level spacing between the right going and left going is comparable to k_BT, the states will be mixed. This results in reduction of the supercurrent approximately as:

$$I_c(T) = I_c(0) \exp\left(\frac{-L}{\xi(T)}\right) \tag{2.24}$$

where, $\xi(T) = \hbar v_F / k_B T$ is the thermal coherence length.

Sub-gap current

In the sub-gap region the current is carried by quasi-particle transport at non-zero voltage, $|V| \leq 2\Delta$. If a constant voltage V is applied across the junction the phase develops with time, according to the ac-Josephson relation, $\phi = (2eV/\hbar)t$. It creates an ac Josephson current that oscillates with the Josephson frequency $2eV/h$. This however does not contribute to the dc-current.

To get a dissipative dc-current across the SNS junctions, the quasiparticles from the left superconductor has to travel through the nanowire to the quasi-particle states above the superconducting gap of the right superconductor. This process happens if the external voltage supplied is comparable or bigger than $|V| > 2\Delta/e$.

The process transfers only single charge e across the junction. This is the mechanism of current flow at $|V| > 2\Delta/e$, see Fig. 2.6

What if $\Delta < |V| < 2\Delta/e$? In this case, the electron from the left S has gained eV when it reaches the right NS interface. Assuming an ideal interface, the electron will be Andreev reflected and the reflected hole traces back the path of the electron to the left NS interface while accumulating eV on its way. The reflected hole has enough energy (total of $2eV$) and makes it to the empty quasiparticles state in the left S. In this process, the electron and the hole gain an energy eV each when they cross the nanowire region, and transfers Cooper-pairs to the right S electrode. This Andreev reflection contributes to the current at $\Delta < eV < 2\Delta$.

When the voltage is lower to $|V| = 2\Delta/3e$, a multiple Andreev reflection (MAR) starts to take place, the quasiparticles cross the N region three times. That is, the electron will be reflected as a hole thereby transferring Cooper-pair to the right S electrode. Since the retro-reflected hole does not have enough energy to make it to the empty quasiparticles state, it has to be reflected as an electron. This second electron will traces back the path of the hole and will have accumulated enough energy to get in to the quasi-particle state in the right S electrode. This process transfers a Cooper pair and a single electron charge from left to right. This process contributes to the current at $2\Delta/3e < |V| < \Delta$.

In general, the n^{th}-order MAR process involves transferring of n-quasi-particles (n-times crossing of the nanowire) from left to right, and vise versa. The onset of the n^{th} process happens when the voltage $|V| = 2\Delta/ne$. This gives the sub-harmonic gap structures in the SNS junctions. In non-ideal interfaces, the current contribution of the n^{th} order MAR depend on the normal state transmission probability $(T')^n$. The structures are more pronounced in the tunneling limit $T' \ll 1$ and are completely smeared at $T' = 1$.

The current-voltage characteristics of the SNS junctions show enhancement of the conductance in the sub-gap region. This is also reflected in the excess current at $|V| > 2\Delta/e$. In suspend nanowires, the transmission probabilities of the channels could be controlled by a means of the local-gate voltage and hence observe the cross over from the tunneling limit (SIS) behavior to SNS behavior, see appended paper IV.[58]

2.3 Single electron transistor

Single electron transistors (SETs) are three terminal devices that exploit the concept of quantum mechanical tunneling and the electrostatic Coulomb interactions.[11, 12] The SET device consists of two tunnel junctions in series and a capacitively coupled gate electrode to the central island. The gate tunes the electrostatic potential of the island thereby controls the sequential tunneling of a single electron from the source to the drain.[60, 61, 13, 62, 14] It is an extremely charge sensitive device.

In conventional single electron transistors, the tunneling barriers are defined by

very thin oxides in-between two metals. In nanowire SETs, the tunneling barriers are formed by engineering the band-structure of *heterostructure nanowires*.[15] When a thin and wide band-gap material is introduced in the middle of a narrow band-gap material, the band-gap offset forms a tunneling barrier. If two barriers such are introduced at proper positions, they can localize charge carriers. The nanowire part in-between the two tunnel barriers serves as the island of SET.

The working principle of SETs is based on the *Coulomb interaction* of electrons in a charged object. The charge residing on the object is linearly related to its potential relative to ground, $q = CV$. The proportionality factor is the capacitance which depends on the geometry and size of the object. For an isolated body with a certain capacitance C and charge q residing on it, the Coulomb interaction among the charge carriers gives rise to an electrostatic energy $U = q^2/2C$. This implies there is electrostatic energy associated with adding a single electron named as the *charging energy* $E_c = e^2/2C$. Reducing the size of the object leads to an increase of the charging energy.

To be able to observe the single electron charging effects in transport properties of small scale devices, there are two necessary conditions to be fulfilled. The first condition is that the thermal energy has to be much smaller than the charging energy so as to not smear out the effects of the charging energy $k_B T \ll e^2/2C$. This condition represents the greatest challenge to manufacture small-scale devices operating at room temperature. Room temperature $T = 300\,\mathrm{K}$ corresponds to a thermal energy of 25.8 meV, which corresponds to a very small capacitance 3 aF.

Second, to have a well defined charge, the electrons on the island has to be localized. The typical time $\tau = RC$ for the charge to leak away through any of the leads need to be sufficiently long. This requires the energy uncertainty associate with the leak out time to be smaller than the charging energy, $\delta\epsilon = \hbar/(RC) \ll E_c = e^2/2C$. This condition requires that the resistance of any junction in a single electron device must exceed $R \approx 25\,k\Omega$.

A circuit model of a SET device is shown in Fig. 2.7. The tunnel barriers are represented by leaky-capacitors C_1 and C_2 connected to the source and drain electrodes, respectively. The gate affects the energy of the system by inducing a polarization charge $Q_g = C_g V_g$, where C_g is the gate-capacitance and V_g is the applied gate voltage. The net charge on the island is given by $Q_1 + Q_2 + Q_g = -ne$. The Coulomb interaction in the island expressed by a single capacitance $C_\Sigma = C_1 + C_2 + C_g$. The electrostatic energy $U(n, V_g)$ due to the net charge on the island is given by:

$$U(n, V_g) = \frac{q^2}{2C_\Sigma} = \frac{(-ne + Q_g)^2}{2C_\Sigma} \tag{2.25}$$

In the Orthodox theory, tunneling happens if the system's free energy E is reduce after the tunneling event $i.e$, if $\triangle E < 0$. The free energy of the SET system is given by the sum of the work done by the voltage sources W_s, and the

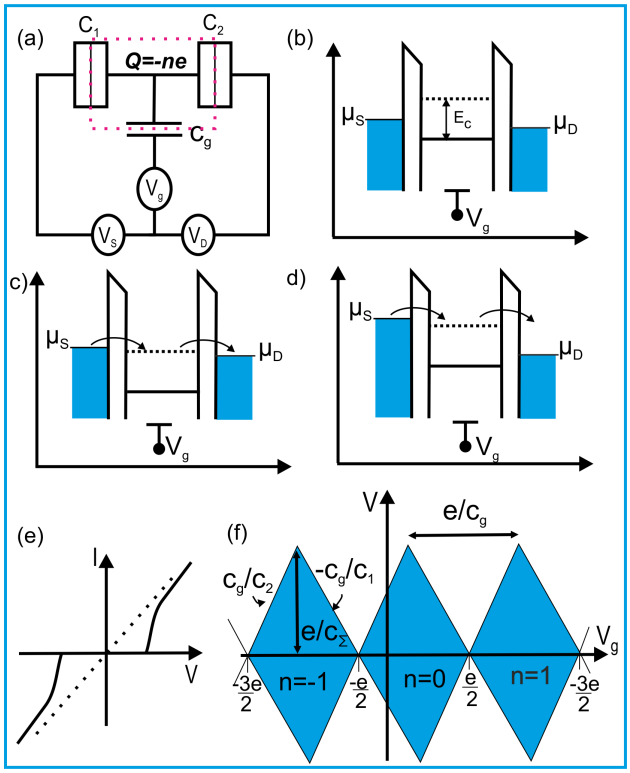

Figure 2.7: (a) An equivalent circuit model for single electron transistor. (b) Schematic representation of the energy-diagrams for the SET. There is no level in between μ_S and μ_D, the net charge is fixed on the island due to Coulomb blockade. (c) The Coulomb blockade is lifted by a gate voltage that aligns the electrochemical potential of the island in-between μ_S and μ_D. This results in single electron tunneling. The island can have either n or $n-1$ electrons. (c) The source-drain voltage is increased such that there is a level in between μ_S and μ_D. This results in a tunneling current which depends on the tunneling rate between the island and the reservoirs. (d) Current voltage characteristics for two gate voltages that corresponds to Coulomb blockade (solid line) and to degenerate state (dashed line). (d) The stability diagram of SET. At low voltages there are rhombic shaped regions with stable number of charges on the island, no tunneling current. The asymmetric junctions C_1 and C_2 gives different slopes of the threshold voltages, indicated by arrows. Along the gate-axis $V = 0$, there are periodic ($V = e/C_g$) degeneracy points, where it does not matter to have n or $n \pm 1$ on the island.

electrostatic energy U, $E = U - W_s$:

$$E(n_1, n_2) = E_c\Big[(n - n_g)^2 - V\Big(n_2(2C_1 + C_g) - n_1(C_2 + C_g)\Big)\Big] + constant \tag{2.26}$$

where, the charging energy of the island is $E_C = e^2/C_\Sigma$. The change in the free energy $\triangle E$ when an electron tunnels into the island via the drain junction C_2, *i.e* $n \to n + 1$, is given by:

$$\triangle E = E(n_2{+}1, n_1){-}E(n_1, n_1) = E_c\Big[(2n{+}1{-}2n_g){+}\frac{2V}{e}(C_1{+}C_g/2)\Big] \tag{2.27}$$

Similarly, three more energy difference can be obtained for single electron tunneling a) out of the island via C_2 ($n \to n - 1$), b) into the island via C_1 ($n \to n + 1$) and c) out of the island via C_1 ($n \to n - 1$). Each tunneling is energetically favorable if the corresponding energy differences is negative after the tunneling events. Thus, to get the critical conditions for the various tunneling events, we equate each energy difference to zero.

These thresholds conditions are represented graphically by four-lines in the (V, V_g)-plane. This is known as the *stability diagram*, see Fig. 2.7f. Along the gate V_g axis, symmetrically around $V = 0$, the stability diagram shows arrays of rhombic shaped regions. In these regions, the net charge on the island is stable, $n = ..., -1, 0, 1, ...$ and the system is in *Coulomb blockade*. The Coulomb blockade condition could be lifted either with a gate or source-drain voltage, see Fig. 2.7. At $V = 0$, there exist degeneracy points, where the energy is the same for being in n or $n + 1$, $U(n, V_g) = U(n + 1, V_g + \triangle V_g)$. The degeneracy points comes periodic with the gate voltage at $\triangle V = e/C_g$.

2.4 Radio frequency single electron transistor

The important property of the single electron transistor is that it is very sensitive to charge changes on the gate electrode. The theoretical sensitivity is limited by the intrinsic shot noise of the SET.[63, 64] However, in dc-mode experiments, the charge sensitivity is limited by amplifier and $1/f$ noise. The high impedance of the SET and the capacitance ($\sim$ 2 nF) due to external circuit limit the operation frequency below $1/(2\pi RC) \approx 20$ kHz. This problem can be overcome by operating the SET in the RF-mode (RF-SET).[26]

The underlying principle of the RF-SET is to measure the reflection coefficient of a radio frequency signal from a tank-circuit in which the single electron transistor is embedded. In the reflectrometry, a carrier signal at the resonance frequency of the tank circuit is launched towards the SET. The reflected signal is amplified by both cold and warm amplifiers before it is detected at room temperature. This increases the operating frequency and the bandwidth of the RF-SET which is limited by the bandwidth of the tank circuit, ~ 100 MHz. The RF-SET is

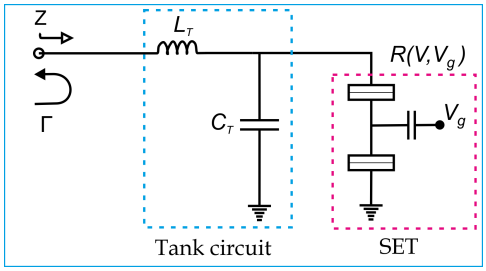

Figure 2.8: a) Equivalent circuit of an RF-SET. The SET is embedded in a tank circuit of external inductor L and C. The reflection coefficient Γ depends on the resistance of the SET $R(V, V_g)$.

an extremely charge sensitive device since it works at a frequency above the $1/f$ noise corner.[27]

The power of the reflected signal is modulated by the state of the SET, which in turn is a function of the bias and gate voltages. Th reflection coefficient Γ is defined in terms of the impedance mismatch:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{2.28}$$

Without the matching circuit, the large impedance mismatch between R and measurement line $Z_0 = 50\,\Omega$ reflects back almost all the signal, like light reflection from a smooth mirror, so we hardly see any modulation of the reflected power as the SET state changes. By implementing a matching circuit to transform the SET resistance R to the $50\,\Omega$ coaxial line we can get strong modulations of the reflected signal. This helps to get strong dependence of the reflected signal for a small change of resistance.

The tank circuit consists of a shunting capacitance C_T and an external inductance L_T in series with the SET. The shunting capacitance is provided by the bonding pad capacitance to ground. The inductance comes from an inductor mounted on the sample holder. One of its ends is wire bonded to the drain of the SET. The tank circuit is characterized by its resonance frequency $f_0 = 1/(2\pi L_T C_T)$ and its quality factor Q.

Resonance frequency

The *resonance frequency* is defined as the frequency at which the stored energy oscillates between the capacitive and inductive energy. The frequency resonance of the matching circuit terminated by the SET is determined by measuring the reflection coefficient with a network analyzer. This frequency corresponds to the minimum amplitude of the reflection coefficient.

The equivalent impedance Z of the matching circuit terminated by the SET is

given:

$$\begin{aligned} Z =& R \parallel (j\omega C)^{-1} + j\omega L_T = \frac{R}{1+(\omega/\omega_0)^2(R/Z_{L_TC_T})^2} \\ &+ j(\omega/\omega_0)\left(Z_{L_TC_T} - \frac{R^2/Z_{L_TC_T}}{1+(\omega/\omega_0)^2(R/Z_{L_TC_T})^2}\right), \end{aligned} \tag{2.29}$$

where, $\omega_0 = 2\pi f_0 = (\sqrt{L_TC_T})^{-1}$, $Z_{L_TC_T} = \sqrt{L_T/C_T}$, and R is the resistance of the SET.

The resonance frequency which can also be expressed as the frequency where the imaginary part of the reflection coefficient vanishes. Equating the imaginary part of eq. 2.29 to zero, gives the loaded resonance frequency ω_0':

$$\omega_0'^2 = \omega_0^2(1 - (Z_{L_TC_T}/R)^2) \tag{2.30}$$

This implies that the resonance frequency depends on the resistance R of the SET. This shift in frequency could be significant in small resistance devices such as in measuring the differential resistance of S-nanowire-S weak links.

The Quality factor

The *quality factor* Q is defined as the ratio of the energy stored in the resonator to the energy loss per cycle:

$$Q = 2\pi\frac{Energy\,stored}{Energy\,loss\,per\,cycle} = \omega_0\frac{Energy\,stored}{Power\,loss} \tag{2.31}$$

The energy loss could either be due to internal losses inside the resonator or due to coupling to the external environment. These losses contribute in parallel and can be characterized independently. These are referred to as the *internal* and the *external* factors, Q_i f and Q_e.

The internal quality factor Q_i for the tank-circuit, not coupled to the transmission line, is given by $Q_i = R/Z_{L_TC_T}$. In the reflectrometry, the device is coupled through the LC tank circuit to the $50\,\Omega$ coaxial line. This gives one way of loosing energy out of the resonator and subsequently lowers the quality factor. This external quality factor is defined as $Q_e = Z_{L_TC_T}/Z_0$. The total quality factor Q is:

$$\frac{1}{Q} = \frac{1}{Q_i} + \frac{1}{Q_e} = \frac{Z_{L_TC_T}}{R} + \frac{Z_0}{Z_{L_TC_T}} \tag{2.32}$$

At resonance, the amplitude of the reflection coefficient can be expressed in terms of the quality factors:

$$|\Gamma| = \frac{Q_e - Q_i}{Q_i + Q_e} \tag{2.33}$$

The power of the reflected signal P_r as a function of the SET resistance and the power in P_{in} on resonance will have the form:

$$P_r = |\Gamma|^2 P_{in} = P_{in}\left(1 - 4Q^2\frac{Z_0}{R}\right) \tag{2.34}$$

2.5 Electrical noise

Electronic noise is a random, stochastic process, that generates a set of continuous, randomly varying functions of time (for example voltage $v(t)$ or current $i(t)$). However, although noise is random and its value can not be predicted from instance to instance, it has certain uniform properties which it can be characterized by. For example, the power spectral density of a noise source is related to the noise statistics. This is important to minimize its effects and to model noise sources. Also, "the noise is the signal", was the saying of Rolf Landauer[65]. It can provide information beyond the measured current, for example, the shot noise gives the charge of the carriers.

For a continuous random variable x, the probability that $x(t)$ is within some range on any instantaneous observation, is specified in the probability density function, $f(x) = \partial F(x)/\partial x$, where $F(x)$ is the distribution function of the noise source which could be for example a Gaussian or a Poisson distribution. Assuming the noise process is ergodic: *i.e* the ensemble average (the statistical mean value) equals the temporal mean (time averaged) value expressed by

$$\overline{x} = \int_{-\infty}^{\infty} x f(x) dx = \lim_{x\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} x(t) dt \tag{2.35}$$

Noise can be generated by a number of different physical mechanisms, and could have different statistics. However, the noise at for example, different out-put ports of an electrical device may not be completely independent, since it may have its origin from the same source. This partial dependence is expressed as a correlation. An important property is the auto correlation function which is expressed as:

$$R_x(\tau) = \overline{x(t) \cdot x(t-\tau)} = \lim_{x\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} x(t) x(t-\tau) dt \tag{2.36}$$

Finally, the power spectral density of a signal $x(t)$, S(ω), is simply the Fourier transform of the auto-correlation function:

$$S_x(\omega) = \int_{-\infty}^{\infty} R_x(\tau) \exp(-i\omega\tau) d\tau \tag{2.37}$$

2.5.1 Thermal noise

Einstein predicted (1906), that the fluctuation of charges in lossy resistor in thermal equilibrium would result in a noise voltage (or current) at its terminals. These has been experimentally observed by J. B. Johnson (1928) and theoretically analyzed by H. Nyquist in the same year.[66, 67] The thermal noise is also known as the Johnson-Nyquist noise. Nyquist showed that the spectral density (or mean-squared value per bandwidth B) of the short circuited terminal noise current i_n is given by

$$S_i(f) = \overline{i_n{}^2} = 4kT/R = 4kTG \tag{2.38}$$

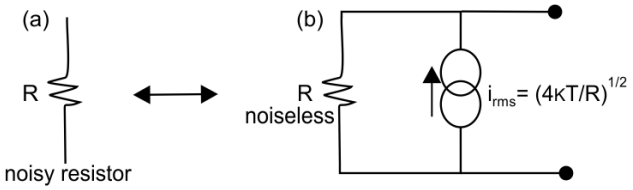

Figure 2.9: a) Circuit representation for a noisy resistor. b) Equivalent circuit of a noisy resistor.

The available noise power per unit bandwidth, $i.e.$ the noise power delivered per unit bandwidth to a matched load, which would be another resistor of the same value R is given by k_BT. The thermal noise does not provide us with additional information since it is independent of the conduction mechanism, or dimensions of the resistor. However, since the noise power spectral density depends only upon the value T, it is widely use to characterize any flat noise spectrum as a noise temperature.

The noisy resistor can be represented by a Norton equivalent in a bandwidth B, consisting of a noise current source of rms value, $i_{n,rms} = \sqrt{4kBT/R}$ and a noiseless resistor R, see Fig. 2.9.

2.5.2 Low frequency (1/f) noise

All solid state devices show a form of increased noise at low frequencies. The noise spectrum varies approximately as $1/f^{\alpha}$, where α is close to 1. There are different assumption to explain its location and origin, such as defects, charge traps close to interfaces. However, its physical mechanism is still unknown.

In conventional SETs, charge traps on the substrate has been suggested as the physical sources for the $1/f$ noise, but measurement results did not show any conclusive evidence so far. In nanowire SETs, the nanowires are suspended from the substrate, if there is any role from the substrate, the device would have less $1/f$ noise. However, the actual measurement show a typical $1/f$ behavior. See appended paper I.

2.5.3 Shot noise

The shot noise is a non-equilibrium noise associated with the discrete nature of charge flow and originates because the emission of charge carriers across a potential barrier is a random process. The shot noise in vacuum diodes was first described by Schottky in 1918.[68]

The power spectral density of the current fluctuations is given by the Schottky formula, $S_P = 2eI$, for a perfectly Piossonian random process. The shot noise has a white noise spectrum. It is proportional to the electronic charge e, and the mean value of the current I. The shot noise gives more information of the electron

transport as it is sensitive to any modification to the randomness, for example, due charge-transport correlations in superconducting contacts.

In the Landauer formalism, a coherent mesoscopic conductor is connected to the contact reservoirs by reflectionless leads. At zero temperature, the states in the reservoirs are filled, according to the Pauli principle, up to the electrochemical potential μ and there is no fluctuation in the occupation number of the states in the leads (the injected electrons are noiseless). However, the charge carriers (wave packets) experience scattering by the conductor before they reach the other contact, which results in fluctuations of the occupation number of the outgoing states and hence results in a random process, shot noise.

For a coherent mesoscopic conductor with N conducting modes, each with an arbitrary transmission probability T'_n, the spectral density at low frequency for a given voltage V and temperature $T = 0$ is

$$S_I(V) = 2e \sum_{n=1}^{N} I_n(1 - T'_n) \tag{2.39}$$

[69]. For a ballistic conductor $T' = 1$, $S_I = 0$ (there is no fluctuation in the occupation number and no shot noise). For weakly transmitting channels $T'_n \ll 1$, the Schottky formula $S_P = 2eI$ is recovered. The Fano-factor F is the ratio between the actual shot noise S_I and the Schottky value,

$$F = S_I/S_P = (1 - \sum_{n=1}^{N} T'^2_n / \sum_{n=1}^{N} T'_n) \tag{2.40}$$

This implies that measuring the shot noise gives more information about the quantum transport properties than just measuring the current. The reduction (sub-Poissonian) in the shot noise due to correlation in charge carriers has been experimentally observed in point contacts formed in a 2DEG systems and SETs.[70, 71, 72]

When the contacts in an SNS device are in the superconducting state the charge transport is correlated, and the conductance through the conductor depends on the voltage. The sub-gap current is due to the transfer of multiple charge quanta $(2e, 3e, ..., (n+1)e)$ carried through the multiple Andreev reflections $n = 2\Delta/eV$. Therefore, the effective charge $q^* = S_I/2I$ is expected to increase with decreasing the voltage. In the tunnel regime $T'_n \ll 1$, the effective charge has shown a step-like behavior in a single channel superconducting quantum point contact (SQPC).[73].

In nanowire-superconductor hybrid device, there has not been any shot-noise measurements to reveal the stepwise increase of the effective charge. This might have been mainly due to the $1/f$-noise that dominates and smear-out such effects at low frequency. Here, we exploited the RF-SET, working above $1/f$ frequency, to measure shot noise and hence the effective charge.

2.5.4 Measurement of shot noise

The shot noise in S-NW-S junctions has been measured with the RF-SET up, similar to what has been performed in aluminum SETs by S. Kafanov *et al.*[72] The device is embedded in a tank-circuit as shown in Fig. 2.8. The shot noise power spectral density, $S_i(f) = \overline{i_n{}^2} = 2eIF$ generated at different dc-currents through the device is amplified by a low noise HEMT amplifier. The output noise power is then feed-in to a spectrum analyzer. Here, we derive an expression to extract the actual shot noise of the device from the measured noise, which also includes the amplifier noise contribution. For more details of the measurements see section 3.4

The noisy resistor, as in Fig. 2.9, can be represented by a Norton equivalent, consisting of a noise current source of $i_s = i_{rms} = \sqrt{2eIF}$ value, and noiseless resistor R. The voltage noise v_s, at the input stage of the amplifier generated by the current noise can be expressed as:

$$v_s = \frac{Z_0}{j\frac{\omega}{\omega_0}\left[\frac{1}{Q}\right] + \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]} i_s \tag{2.41}$$

where, Q is the total quality factor of the tank circuit.

The noise power spectral density, considering $Z_0/R \ll 1$, at the amplifier output is given by

$$S_i = \frac{G}{2Z_0} v_s^2 = \frac{G}{2} \frac{Z_0}{\left(\frac{\omega}{\omega_0}\right)^2 \left[\frac{1}{Q}\right]^2 + \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]^2} i_s^2 \tag{2.42}$$

where, G represents the amplifier power gain. Eq. 2.42 implies that the output noise power spectral density has a Lorentzian shape, see Fig. 2.10b for a noise measured for a typical device at the normal state, $V \gg 2\Delta/e$.

At resonance, $\omega \approx \omega_{L_T C_T}$, the shot noise spectral density depends on the quality factor:

$$S_i = \frac{G}{2} Z_0 Q^2 i_s^2 \tag{2.43}$$

The quality factor can be written in terms of the reflection coefficient Γ and device resistance R, $Q = R(1- \mid \Gamma \mid^2)/4Z_0$. The noise spectral power density, taking into account $i_s^2 = 2eIF$, will then be:

$$S_i = \frac{G}{4}(1 - |\Gamma|^2)(RI)eF = \frac{G}{4}(1 - |\Gamma|^2)VeF \tag{2.44}$$

The total noise power spectral density at the output of the amplifier is the sum of the contribution from the shot noise and the amplifier noise $S_{amp} = Gk_BT_N$. The amplifier noise is considered to be independent of the reflection coefficient since it is isolated from the device by a circulator. The measured noise power spectrum S_m will then be:

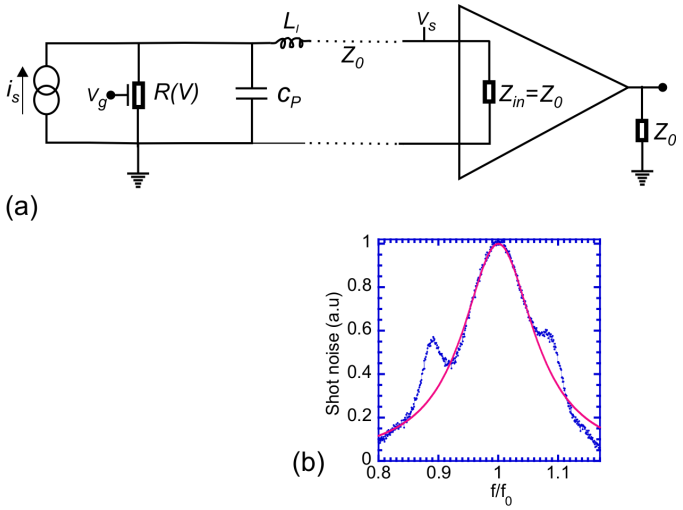

Figure 2.10: a) The shot noise generated in the device is represented by a Norton model, consisting of a noise current source i_s, and a noiseless resistor R. The noise current is filtered out by the tank circuit before it creates a voltage noise $_s$ at the input stage of the low noise HEMT amplifier. The voltage noise signal, besides the amplifier noise characterized by a noise temperature T_N, is then amplified and feed into a spectrum analyzer.

$$S_m = G\left[\frac{1}{4}(1-|\Gamma|^2)eFV + kT_N\right] \tag{2.45}$$

The measured noise power P_m as a function of bias can be found by integrating the noise close to the resonance frequency, within a bandwidth $\triangle f$, such that $\triangle f \ll f_0/Q$. The amplifier noise power can be extracted from the measured noise at zero voltage, $P_m(V=0) \approx P_{amp}$. The slope of $\partial P_m/\partial V$ can also be used to estimate the power gain G of the amplifier. The Fano-factor F as a function of bias, from eq. 2.46, is then given by:

$$F(V) = \frac{(P_m(V) - P_m(0))}{\partial P_m/\partial V}\,\frac{(1-|\Gamma(V \gg 2\Delta)|^2)}{(1-|\Gamma(V)|^2)} \tag{2.46}$$

Chapter 3

Experimental techniques

This chapter covers the nanofabrication process and the low-temperature experimental techniques to study carrier-transport in the superconductor-nanowire hybrid devices. It includes nanowire growth, contacting nanowires with metals, and both direct current and radio-frequency read-out techniques.

3.1 Sample preparation

One interesting property of InAs is the pinning of the Fermi energy into the conduction band due to surface states. It leads to a charge accumulation layer at the surface that helps to get highly transparent contact-interfaces with metals. The formation of high-quality interfaces is crucial to demonstrate proximity induced superconductivity in current transport through the nanowires. However, the small dimensions of the nanowires makes it difficult to effectively gate-control the current transport through such weak-links, especially using a weakly coupled back-gates. This has motivated us to fabricate suspended devices with local gates that are very close to the nanowire and therefore strongly coupled to the nanowires. This section deals with the fabrication process of such suspended and also non-suspended devices, *i.e.* nanowires placed directly on the substrate. The details of the recipes are presented in the appendix.

3.1.1 Nanowire growth

The epitaxial growth of nanowires has been performed at the division of solid state physics, Lund University. Here, only an overview of the growth process is presented, for more details, see Ref.[74].

In the epitaxial growth of nanowires, the method of growth could use either physical deposition or chemical reaction of growth materials. For our devices, the nanowires are grown by chemical beam epitaxy (CBE) in ultra high vacuum.[74] In the growth process, the semiconductor growth materials are injected into the reaction chamber as gas sources, precursors, directed at a heated substrate. On

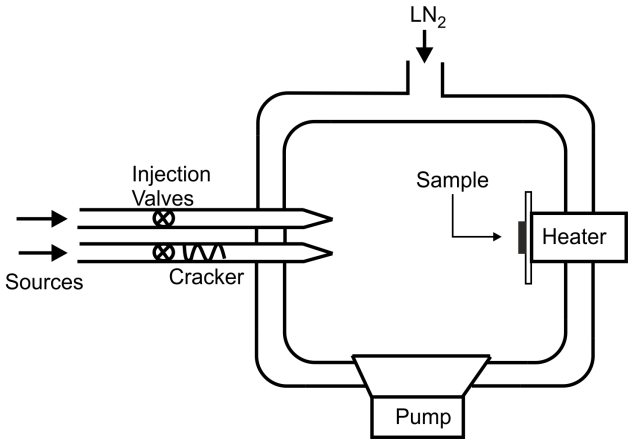

Figure 3.1: Schematic picture of chemical beam epitaxy. The precursors, containing the growth materials, are injected through the nozzles to the growth chamber. Owing to the high vacuum achieved by a turbo pump, the gas-sources are introduced to the reaction chmaber as a beam directed towards the heated substrate. A constant supply of liquid nitrogen on the surface helps to cryo pump and cold-trap residual chemicals on the chamber walls.

the substrate the precursors react and crystallization is locally catalyzed by gold particles pre-deposited on the surface of the substrate. As more materials are incorporated, the Au-catalysts are ”lifted-up” from the substrate forming vertically growing nanowires. The size of the Au-particles determine the diameter of the nanowires.

The CBE method offers the possibility not only to control the growth rate but also to switch materials during the growth process. Therefore, it allows to grow nanowires with different material layers or chemical compositions, *i.e* nanowire heterostructures.

A schematic picture for the CBE method is shown in Fig. 3.1. The growth chamber is pumped to high vacuum using a turbo pump. The substrate where the nanowires are formed is placed on a stage with a heater. The temperature of the sample is monitored with an infra-red remote surface temperature sensor. To start the growth process, metal-organic gaseous sources, containing the desired atoms, are thermally cracked to their components and the growth materials are injected to the growth chamber through nozzles. Due to the very low-pressure, the mean free path of the gas motion is large and the source precursors move in a beam trajectory towards the substrate. The on-going surface reconstruction is followed with the help of Reflective High Energy Electron Diffraction (RHEED) mounted in the chamber at a small grazing angle with the surface of the substrate. The diffraction pattern constructed by a reflected signal (electron) from the substrate gives information about the growing surface. During the growth process, a constant flow of liquid N_2 is supplied in the walls of the growth chamber. Keeping the walls cold not only provides additional cryo-pumping but also helps to cold-trap

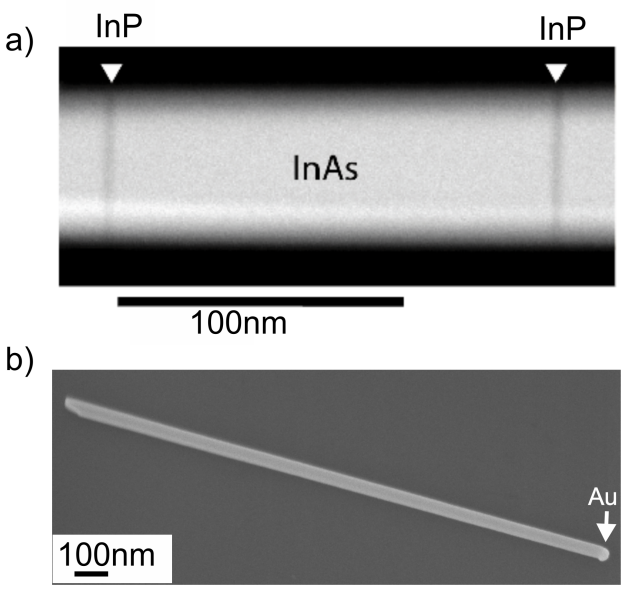

Figure 3.2: a) TEM image of InAs/InP double heterostructure nanowire. The contrast clearly shows the two InP barriers with a thickness of 2-3 nm introduced in the 50 nm-diameter InAs nanowire. b) SEM image of a pure 80 nm-diameter InAs nanowire. The Au-catalyst which also determines the diameter of the nanowire is indicated by an arrow.

any residual chemicals on the inner surface and inhibit them from moving to the sample surface and the growth process.

The CBE growth method for InAs/InP heterostructures is done by switching the injection of the growth species with time. Depending on the intended thickness of the materials the growth time for each species is controlled manually or with a computer. The amount of the growth material is controlled by controlling the pressure at which the gas sources are injected to the chamber. The metal-organic sources are trimethylindium (TMIn), tertiarybutylarsine (TBAs), and tertiarybutylphosphine (TBP) for In, As, and P, respectively. The As and P source-molecules are thermally cracked when entering the chamber.

To what extent the growth of two bulk materials on top of each other is epitaxial, depends on the lattice constants of the growing materials. The lattice mismatch between InP and InAs is 3.4%, as a result there will be a strain at the interface that can cause dislocations or defects. However, this does not happen in the nanowire growth of the two materials. The reason is that the small cross sectional area of the growing nanowires allows relaxation of the strain radially (the diameter changes) within a few monolayers.

In this thesis work, the nanowires are in general of two types: InAs/InP heterostructure nanowires where two thinner InP are grown in the middle of InAs nanowires (see Fig. 3.2a), and pure InAs nanowires (see Fig. 3.2b). The nanowires are approximately from 40 nm to 80 nm in diameter.

3.1.2 Device fabrication

After the growth process, the vertically grown nanowires are "harvested" from the growth substrate and are transfered to another substrate (device substrate) where they are transformed into devices by coupling them to metals. The transfer is carried out by gently wiping out a sharp-side of a piece of paper on the growth of substrate. Some of the nanowires that stick with it are then transferred by gently touching the device substrate by the sharp side of the piece of paper.

In general, the devices can be categorized in two types: a) nanowires placed directly on the substrate with either two or more superconducting contacts, (see Fig. 3.3). b) Suspended nanowires with local gates, (see Fig. 3.4). Both types of devices are made on standard Si-substrate capped by 400 nm thick thermally grown SiO_2. Fabrication of the devices requires standard-nanofabrication techniques such as lithography, metal deposition and lift-off processes.

Electron-beam lithography is made in two steps, one at small scale to define the smallest features, and one at large scale to define relatively bigger features. The small-scale is done to connect the nanowires with metal electrodes. Particularly in the suspended devices, it is necessary to accurately place the contacts on the nanowires with a very small misalignment and rotation. Often misplacement is limited to a few nanometers. This mainly depends on how good the e-beam lithography is, which in turn depends on the quality of the alignment marks. For this purpose, several high quality alignment marks per chip are defined by large-scale e-beam lithography rather than by photo-lithography. At the same time, the bonding pads are also made by a large-scale e-beam lithography, details of this process is explained in appendix B.

For the small-scale e-beam lithography, for interfacing the nanowires with metals, we used two e-beam resist layers, Copolymer and ZEP520. While the top layer, ZEP, provides a very high resolution and contrast, the bottom layer, Copolymer provides an undercut for better lift-off. The thickness of the bottom Copolymer layer has been different depending on the intended final thickness of the electrodes.

Non-suspended devices

To fabricate the non-suspended devices, InAs nanowires are first transferred to a device substrate and their relative positions with respect to predefined marks are located with the help of scanning electron microscope (SEM) images. The extracted locations are then used to pattern superconducting Ti/Al (5/150 nm thick) contacts on the nanowires (Fig. 3.3a). Multiple contacts have also been placed on a single nanowire separated by different lengths (Fig. 3.3b). This helps to study junction properties as function of length on a single nanowire with similar physical properties, such as nanowire diameter and impurity levels. Depending on the intended device length, which we define as the distance between source and drain electrodes, the superconducting electrodes are defined by either single-step electron beam lithography or a double lift-off method. The shorter devices ($L < 100\,\text{nm}$)

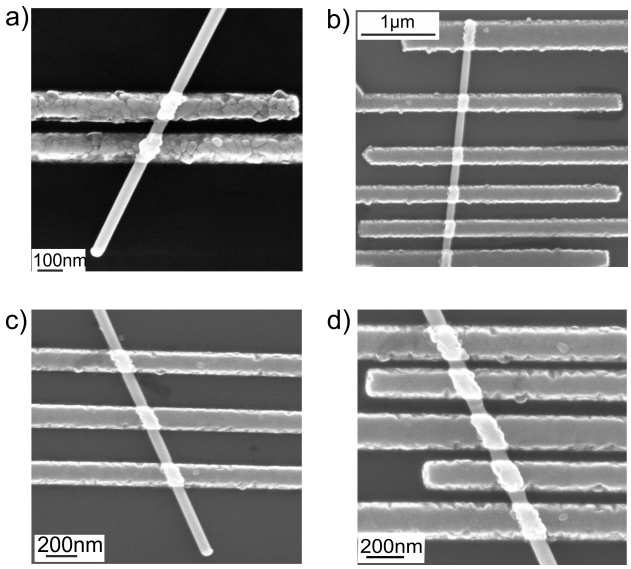

Figure 3.3: a) SEM image of a nanowire with two superconducting contacts defined by a single e-beam lithography. b) SEM image of a single nanowire with multiple superconducting contacts defined by a single e-beam lithography. This heps to compare junction properties as a function of length. c) SEM image of a nanowire connected by three superconducting contacts spaced intentionally at large distances. d) SEM image of the same nanowire after the second lift-off stage. Two more superconducting contacts are defined in between the already exist electrodes.

are defined by the double lift-off process whereas the somewhat longer devices ($L \geq 100$ nm) are defined by the single-step e-beam lithography.

The double lift-off process is a two-step process to fabricate very short length nanowire devices. In the first step, superconducting electrodes on the nanowire are defined by e-beam lithography spaced intentionally at somewhat larger distances. Fig. 3.3c shows a SEM image of the electrodes on the nanowires. In the second step, we defined more electrodes (of the same width) on the same nanowire in between the already deposited electrodes (Fig. 3.3d). Using this method we have fabricated nanowire devices with lengths down to 30 nm combined with highly transparent interfaces to Ti/Al contacts.

In the single-step process, the inter-electrode distance is limited, by the properties of the e-beam resist to 100 nm. In the two-step process, the minimum length of the devices was not limited by the e-beam resist, but rather by the alignment accuracy between successive lithography steps. The specified repeatability for our JEOL9300 e-beam writer is 25 nm. In practice, with carefully designed alignment marks, it can be made even smaller. Thus, we can with good reproducibility place source and drain electrodes at a distance of 30 nm from each other without getting short circuits between the electrodes. In addition, the large spacing of the electrodes in both steps means that it is possible to increase the development time of the e-beam resist. An increase in the resist development time enables us to get rid of residual resist which in turn helps to produce better metal-nanowire interfaces. The second lithography step is done within hours of the first step in order to avoid degradation of the interfaces between the nanowire and the already deposited electrodes.

Suspended Josephson devices

To fabricate the suspended devices, a standard Si substrate is first patterned with interdigitated metal stripes [75]. Pure InAs nanowires or InAs/InP heterostructure nanowires are then transferred to the already patterned Si substrate and some of the nanowires end up on top of the interdigitated metal stripes. The stripes are made in a two-step fabrication process in order to get a height difference of 15 nm between every two adjacent stripes. This allows the nanowire to rest on the thicker bias electrodes Ti/Au/Pd (5/55/5 nm thick) while being suspended above the substrate and the thinner gate electrodes Ti/Au/Pd (5/40/5 nm thick). With the help of SEM images, the positions of suitable nanowires are found and superconducting electrodes Ti/Al (5/150 nm thick) are defined on top of selected nanowires with e-beam lithography. A SEM image of typical metal stripes with a nanowire placed on top is shown in Fig. 3.4a.

The minimum device length is determined by the distance between every two adjacent thicker electrodes. This has been varied from a 100 nm to 300 nm, depending on the intended properties of the final device, particularly the gate width. A SEM image of a typical suspended device with superconducting electrodes and with a length of $L = 150$ nm is shown in Fig. 3.4b.

Suspended heterostructure nanowires

For suspending the nanowire heterostructures, a similar recipe as for the suspended Josephson nanowires has been implemented to fabricate the interdigitated metals. After the nanowires are transferred, only those suspended nanowires situated with their middle body-part centered around the local gate are selected with help of SEM images. This likely gives a better chance of finding the island defined by the two barriers symmetrically placed above the local gate.

Interface preparation

To get good transparency of the metal-nanowire interfaces, an ammonium polysulfide solution (NH_4S_x) cleaning process [47, 30] was used prior to evaporation of the superconducting contacts. The solution is prepared by adding extra pure sulfur to a commercially available ammonium sulfide solution. The solution removes the native oxide from the nanowires and also removes some other impurities on the surface of the nanowires thereby improving metal-nanowire interfaces. The solution is also believed to passivate the nanowire surface and therefore prevents a re-oxidation of the surface prior to metal deposition. Finally, the samples are characterized at room temperature and stored in vacuum before further measurements at low temperatures.

3.2 Cryogenics

We have used two different types of cryostat, a top-loading dilution cryostat and an Oxford Kelvinox-100 dilution cryostat.

The top-loading dilution-refrigerator is mainly used for dc-measurements and has a base temperature of 15 mK. It is kept in an electromagnetic shielded room. The dc-lines are pair-twisted wires equipped with low pass and powder filters to minimize noise coupling to the devices. The design of the refrigerator allows to measure several devices on one chip, with the additional advantage that the chip can be replaced within two hours with out warming up the cryostat. The other valuable merit of the fixed dc-setup, for the right design of contact pads, is that there is no need for wire bonding. Instead the sample is connected by spring-loaded pogo-pins. As a result, most of the devices survive repeated mounting and top-loading processes.

The second cryostat, an Oxford Kelvinox-100 dilution refrigerator with a base temperature of 20 mK, is mainly used for high frequency measurements. The cryostat is equipped with coaxial cables. To minimize noise coupling to the device, a series of filters and attenuators are mounted starting at room temperature down to the device. The choice of the filters depend on the nature of the line such as the frequency of interest and signal levels. Similar to the top-loading fridge, the dc-lines are filtered with low pass and powder filters.

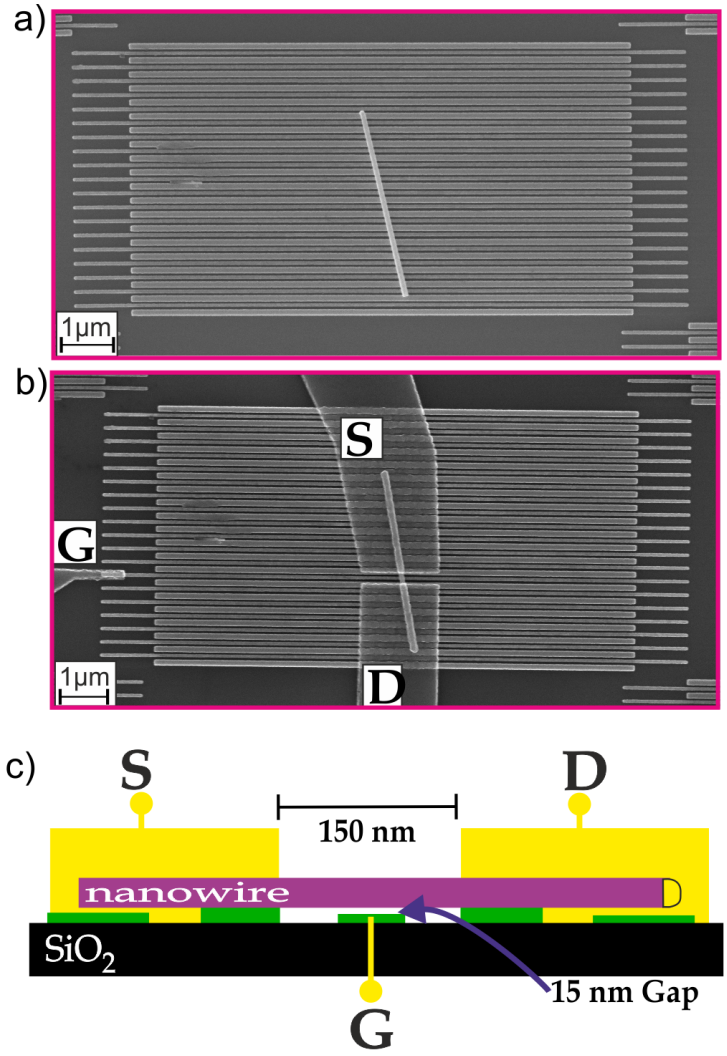

Figure 3.4: a) SEM image of a nanowire placed on interdigitated metal stripes. The thinner gate-stripes are 50 nm thick, 50 nm wide and 11 μm long. The thicker bias-stripes are 65 nm thick, 100 nm wide, and 9 μm long. The spacing between every two adjacent stripes is 50 nm. b) A SEM image of (a) after two superconducting contacts are defined on top of the nanowire. At the same time, only the gate stripe right in-between the source-drain electrodes is also connected to a bonding pad. The final device has a length $L = 150$ nm. c) A side-view sketch of the suspended device.

Both cryostat allow to measure transport properties as a function of temperature and magnetic field in a very precise and well controlled way. There is a possibility to vary the temperature by controlling the current through a resistor placed on the mixing chamber(MXC). The temperature is measured accurately with a calibrated ruthenium oxide, RuO_2 thermometer.

The dilution cryostat has a 3-Tesla magnet working in a persistent current mode. The persistent mode is achieved by a superconducting switch in parallel with the magnet. To set it to persistent mode, the magnet is short circuited by the superconducting shunt. To set the magnetic field to some other values, the persistent mode is interrupted by electrically heating the superconducting shunt. When measuring IVCs as a function of magnetic field, the heater is always on, and the current to the magnet was applied using a separate voltage to current converter.

3.3 DC measurement set-up

The current voltage characteristics (IVCs) have important information about the carrier transport through a junction. The current through the mesoscopic devices, such as the supercurrent, is very small and extremely sensitive to any sort of noise, such as thermal noise and electromagnetic interference. Therefore, it requires low-noise and accurate data-acquisition techniques not to smear-out any features in the transport characteristics.

To decrease noise coupling to the devices, every dc-lines going down to the lowest temperature is prepared with low-pass filters and powder filters to cut out any high frequency noise. Also, the lines are twisted into pairs to prevent any peak-up of radiation from external electromagnetic fields. Moreover, the filters are thermally anchored at different temperature stages of the refrigerator.

In order to measure the IVCs, we have employed either a current-bias or a voltage-bias configuration. In the current-bias scheme, a voltage is applied to two bias resistors R_b connected in series with the device. The bias resistors, which can be selected in the range $\mathrm{R}_b = 10^2 - 10^9\ \Omega$, are set to substantially larger resistance as compare to the device resistance. Hence, it determines the current through the device. As we increase the current, the voltage across the device and the bias resistors are simultaneously measured with instrumentation amplifiers. The symmetric current-bias scheme is shown in Fig. 3.5a.

In the voltage bias scheme, a voltage bias is directly applied across the device while the current is simultaneously measured using a trans-impedance amplifier. The setup utilizes the input stage of a low-noise trans-impedance preamplifier to set the voltage bias on the device. The current is inferred from the voltage output of the amplifier while the voltage drop across the sample is accurately measured with another voltage amplifier. The schematic picture of the setup is depicted in Fig. 3.5b.

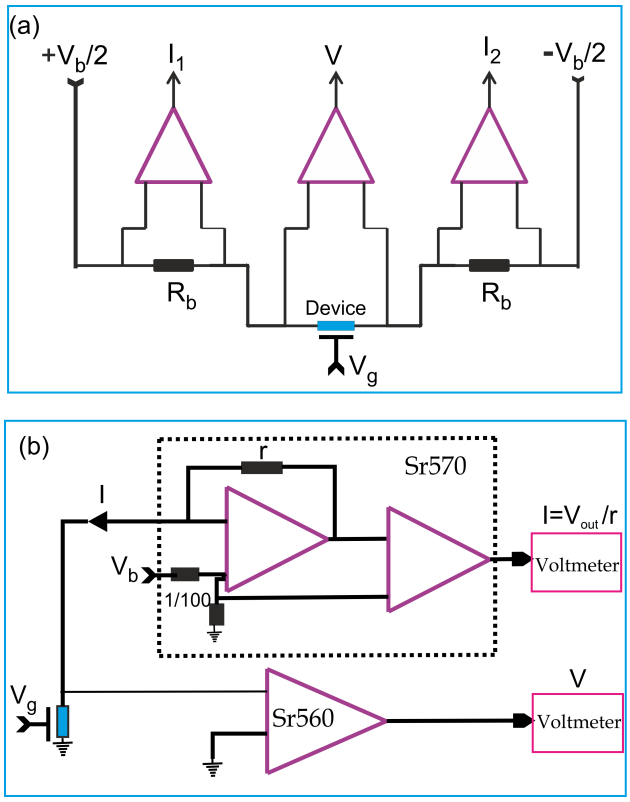

Figure 3.5: Two different set-ups were used for the dc-characterization of the nanowire devices. a) A schematic diagram for a symmetric current-bias configuration. The device is addressed through two variable bias resistors $R_b = 10^2 - 10^9\,\Omega$, which are selected to be substantially higher resistance compared to the device resistance, thereby controlling the current through the device. The source-drain voltage is measured with a differential amplifier. The gate is connected through a voltage divider at room temperature. b) A schematic diagram for voltage-bias scheme. A voltage bias is directly applied on the device through an input stage of a trans-impedance.

3.4 Radio-frequency measurment set-up

The current transport of some of the devices has also been investigated by a radio-frequency read-out technique.[26]. It has been implemented for studying electron transport properties in two types of devices. i) Single electron transistors defined in InAs /InP nanowire heterostructures. ii) Suspended InAs nanowires coupled to superconducting leads. The technique and the measurement setups are quiet similar for both devices except the cryostat used. The measurement for the SETs has been performed using a dipstick in a He^4 liquid bath. The He-bath is thermally shielded by vacuum and can be pumped to reach a temperature of 1.5 K. The measurement for the nanowire based Josephson junctions has been done in the Oxford Kelvinox-100 dilution refrigerator described above. Owing to the similarities of the setup, only the dilution-fridge system is discussed here.

As have been stated in section 2.4, the read-out mechanism is based on studying the dissipation of a radio-frequency signal. A signal is launched from a Z_0 =50 Ω source via a coaxial line towards the impedance matching circuit terminated by the nanowire device. The magnitude of the reflected signal contains information of the power dissipated in the nanowire. The signal level is set such that the IVC is approximately linear. This means that the system should supply weak enough signal to the device and also to amplify the reflected signal such that it is detectable above the background noise.

A schematic picture of the radio frequency read-out setup is shown in Fig. 3.6. For every line, the 4.2 K temperature stage is connected to room temperature through coaxial cables of stainless steel, UT85SS. The stainless steel are semi-rigid cables with low-thermal conductivity and characteristic impedance of $Z_0 = 50\,\Omega$. The cables from the 4.2 K stage down to the MXC are thin and flexible Ni-Cr. However, in the rf-out line, to prohibit any loss of the signal, is a superconducting Nb-Ti cable which connects the circulator and the HEMT amplifier. The cable is semi-rigid and dissipative in the normal state whereas in the superconducting state, $T \leq T_c \approx 10$ K, it has very low dissipation and negligible thermal conductivity. At the MXC, all the cables are Cu-wires with good thermal and electrical conductivity.

Similar to the dc-setup, a combination of Mini-circuits low-pass filters (1.9 or 15 MHz cut-off frequency) and powder filters are employed in the dc-lines. The powder filters provide effective filtering at low frequencies and also at high frequencies where the lumped element filters do not work. Before the dc-bias is feed into the device, it is combined with the input rf-signal using a bias-T placed at the mixing chamber next to the sample holder.

The rf-signal, in addition to a low-pass filter, 1 GHz cut-off frequency, passes through a series of attenuators mounted at room temperature and in the dilution unit. The total cold attenuation without considering the cables amounts to 36 dB (20 dB at 4.2 K, 10 dB at 1.5 K and 6 dB at the MXC). This helps to reduce the noise temperature seen by the device. The noise temperature at the device is the sum of thermal noises generated at each temperature stages divided by the total attenuation on the way down to the device.

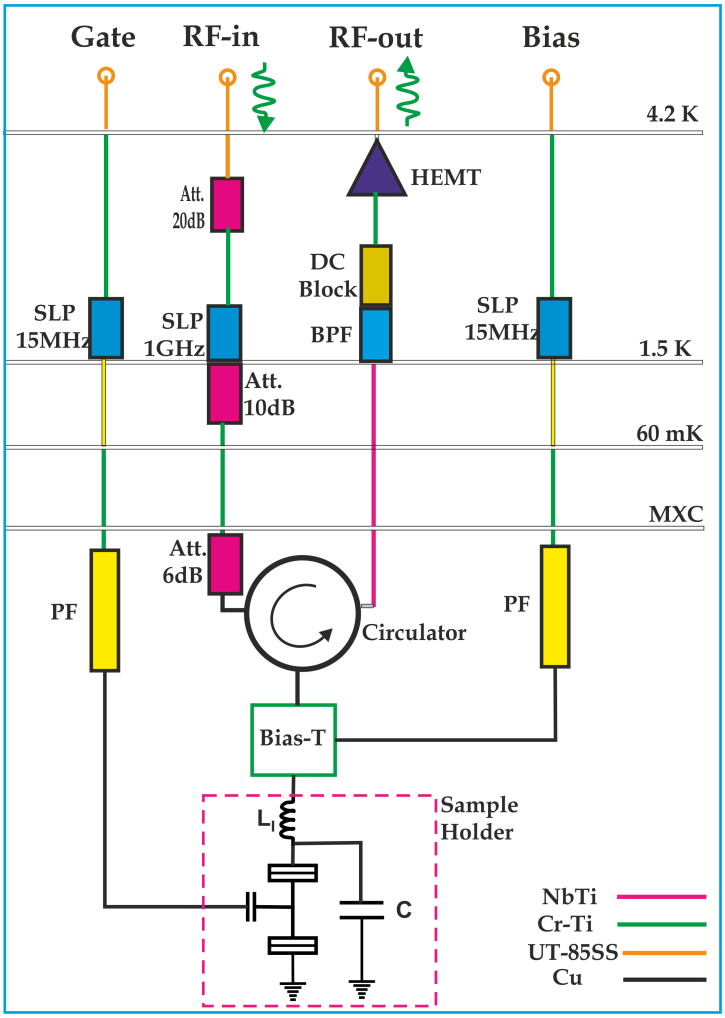

Figure 3.6: A sketch for the cryogenic radio-frequency setup. The carrier signal at a resonance frequency of a tank circuit is launched through cascades of attenuators and a low-pass filter to the device. The reflected signal is then directed to pass though a superconducting Nb-Ti cable before it is amplified by a low noise HEMT amplifier. In the bias and gate lines, low-pass filters and powder filters are employed to filter out any unwanted noise signals at low and high frequency, respectively.

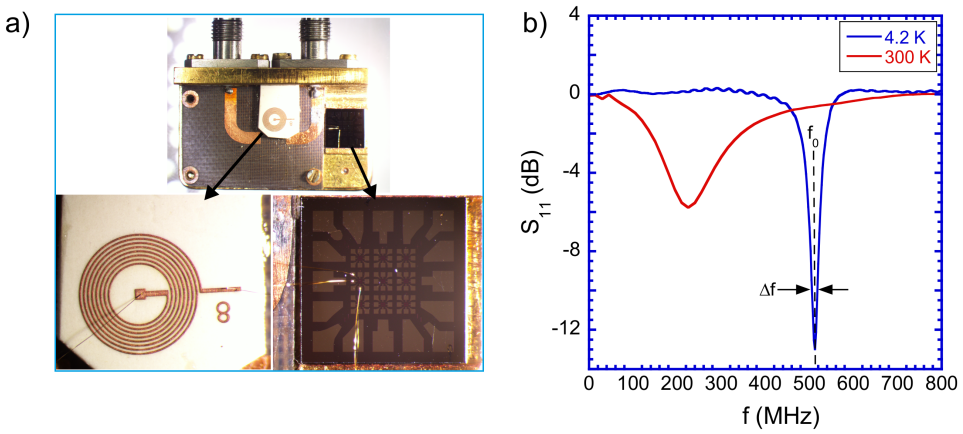

Figure 3.7: A sample holder with two fixed connectors. The sample holder is made of gold-plated highly conductive oxygen-free copper which provides good thermalization. One connector is wire bonded to the source of the nanowire via the inductor. The drain is wire-bonded to the ground plane. The second connector is wire-bonded to the gate line. The zoom-in picture display better view of the inductor and chip. The chip has bonding pads that can be customize for both type of refrigerators. b) Resonance frequency of a tank circuit at both room temperature and 4.2 K. The tank circuit is terminated by a 4 kΩ suspended nanowire. The resonance at room temperature shifts towards higher frequency and becomes narrower as the device was cooled down in a dipstick. The shift in resonance occurs due to the change in resistance of the Si substrate thereby decreasing the stray capacitance to ground. The decrease in width is due to lower losses in the inductor which leads to a higher Q value.

After the signal is reflected from the device, it is directed to a low-noise HEMT amplifier by a circulator. The circulator allows the signal to travel in only one direction. Its isolation is typically 20 dB. Therefore, the circulator isolates the device from the back-action of the amplifier.

Once the fixed setup is ready, the sample holder shown in Fig. 3.7a, containing both the tank-circuit and the device, is mounted on a finger like brass-rod attached to the mixing chamber. In order to provide good electrical grounding and thermalization, the sample holder is made from gold-plated highly conductive oxygen-free copper. There are two SMA connectors fixed on the sample holder. Their inner pins are soldered to 50 Ω coplanar lines on a printed circuit board, PCB. While one of the lines is wire bonded to one-end of an inductor placed on the PCB, the other line is left to be wire bonded to the gate.

The device substrate is mounted on a metallic-ground plane in the sample holder. After that, the free-end of the inductor is wire bonded to the drain of the device and the source is wire bonded to the metallic ground plane. Once the bonding process is completed, the device is immediately mounted onto the refrigerator. Meanwhile, in both bonding and mounting, due care has been taken to prohibit any electrostatic damage to the device. In particular, devices of low resistance has proven to be more easily damaged.

Resonance frequency measurement

The operating frequency is set by the HEMT amplifier, which has a bandwidth of approximately 100 MHz around 650 MHz. As a result, the resonance frequency, which is determine by the non-linear elements C_T and L_T, has to lie within its bandwidth. The stray capacitance C_T, which is difficult to control, is treated as a fixed value for a given area of the bonding pad, leaving the only option of selecting an appropriate inductor. After several test of different inductors, mounting and bonding an inductor to the bonding-pads without any device or open circuit, the inductor that gives a resonance at the frequency of interest, preferably at the center of the amplifier bandwidth, is selected for further use. The resonance frequency is identified when the network analyzer shows a dip in the amplitude of the reflection together with a $\pi/2$ shift in the phase. The total quality factor is extracted from the resonance frequency and the bandwidth, $Q = f_0/\Delta f$.

The test for an inductor has been performed at helium bath since the conductance of the standard Si substrate depends on temperature. At room temperature, the Si substrate is conducting since the carriers of the dopant atoms are thermally excited to the conduction band. However, once the temperature is below 50 K, the thermal energy is smaller than the energy-gap in between the dopant level and the conduction band, the Si substrate runs out of carriers and does not conduct at all. As a result, the stray capacitance decreases and the resonance shifts to higher frequency. A typical shift in resonance frequency is shown in Fig. 3.7b for a device of 4 kΩ. The resonance frequency at 4.2 K is typically a factor of two higher than that at room temperature.

The RF-SET stability diagram

In the RF-read out, a carrier signal at the angular resonance frequency w_c is launched to the matching circuit. The amplitude of the reflected signal depends on the resistance of the nanowire junction, which in turn depends on the gate and voltages. This resistance dependence, and the SET stability diagram in the case of the heterostructure nanowires, can be fully mapped by demodulating the reflected signal. The setup for this purpose is sketched in Fig. 3.8a.The gate voltage was applied with a function generator that combines a dc-offset with a low frequency ac ramp signal.

To record the stability diagram, the gate is stepped for each fixed source drain voltage while simultaneously the rf-source launches a signal at the resonance $V(t) = V_a \cos w_c t$ towards the matching circuit. The reflected signal is amplitude modulated by the change in resistance which can be expressed as $V_a \Gamma(t) \cos(w_c t)$.

After the reflected signal is amplified with a low noise HEMT, it is demodulated by standard synchronous detection (homodyne mixing), *i.e.* a local oscillator (LO) with the same frequency as the carrier signal is mixed with the reflected signal. However, the local oscillator signal, $\cos(w_c t + \theta)$ will have a phase difference θ with the reflected as a result of the long cabling in the cryostat. The output signal

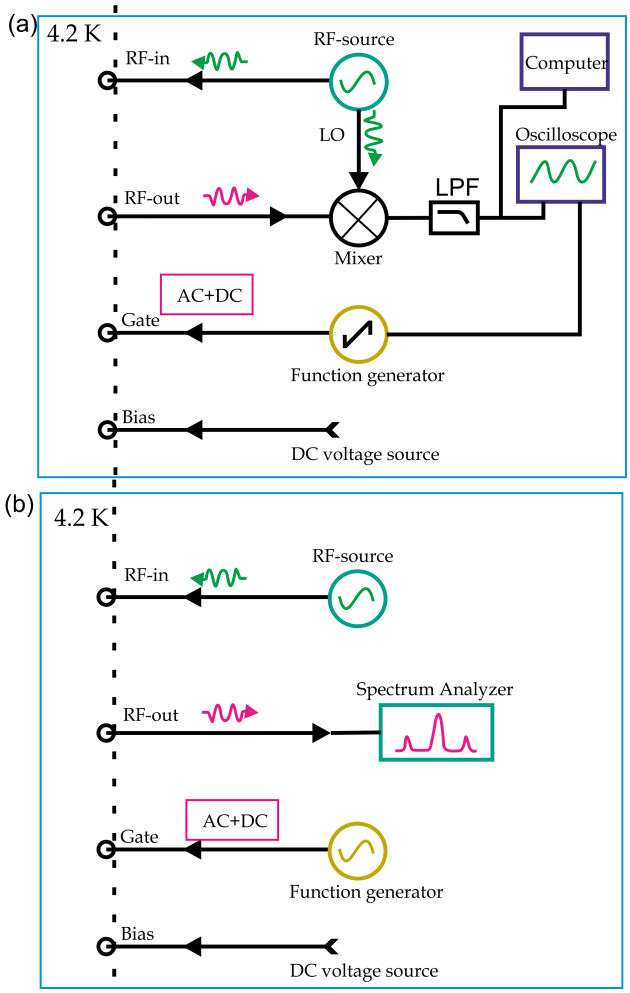

Figure 3.8: a) The stability diagram measurement with a radio-frequency read-out. A carrier signal is launched to a tank circuit in which the device is embedded. The reflected signal is amplitude modulated by the change in the device resistance which in turn is a function of both bias and gate voltages. After the reflected signal is amplified with a low noise HEMT amplifier, it is down converted with homodyne mixing. The resulting signal is low-pass filtered to the base band to be recorded by an oscilloscope or a computer. b) The charge sensitivity schematics. After the SET is set to the maximum charge sensitive condition, the carrier signal is amplitude modulated by a small charge signal of single-tone on the gate. The single-tone of frequency appear as the side bands on the reflected signal in a spectrum analyzer. The signal to noise ratio of the side bands indicates the charge sensitivity of the device.

of the mixer consists of signals at the baseband and at the sum of the carrier and LO-frequencies ($w_c + w_c = 2w_c$):

$$V_r \sim \Gamma(t)\cos(w_c t) \times cos(w_c t + \theta) = \\ 0.5[\Gamma(t) cos\theta(1 - cos(2w_c t) + \Gamma(t)\sin\theta\, sin(2w_c t)]. \quad (3.1)$$

The phase difference can be canceled out by carefully adjusting the phase of the local oscillator, phase-locking detection. This maximizes the low frequency signal. To get the modulation signal $\Gamma(t)$, the high frequency terms of the output signal are eliminated by a low pass filter (a cut-off frequency $\ll 2w_c$). After the filtering, the conductance signal $\Gamma(t)$ is left and is detected with an oscilloscope or a captured by a computer.

The Charge Sensitivity measurement

The RF-SET is extremely charge sensitivity device since it works at frequencies above the 1/f noise.[27] To measure the charge sensitivity, we have implemented the setup in Fig. 3.8b. This setup is similar to the stability diagram except the amplified reflected signal is directly feed into a spectrum analyzer.

In the charge sensitivity measurement, after the gate V_g and bias dc-voltages are set to the steep slopes of the Coulomb blockade oscillations, the carrier signal $V_a cos(w_c t)$ is amplitude modulated by a single-tone RF-signal $\Delta q_{rms}\sqrt{2}\cos(w_g t)$ on the gate. Due to the modulation of the reflection coefficient, the SET serves as a mixer with the output signal containing the gate frequency up-converted to two side bands close to the carrier frequency ($w_c - w_g$, w_c, $w_c + w_g$). Assuming both input-signals (the carrier and the ac gate signal) have low amplitudes the reflected signal, or the up-converting of the gate signal can be expressed as:

$$V_r = (\Gamma_0 + \Delta\Gamma\cos(w_g t))\cos(w_c t) = \\ V_a\Gamma_0 V_a\cos(w_c t) + 1/2 V_a \Delta\Gamma V_a[\cos((w_c - w_g)t) - \cos((w_c + w_g))t \quad (3.2)$$

The output voltage at the frequency of interest are directly detected with a spectrum analyzer. The resolution band width RBW of the spectrum is optimized to clearly resolve the sidebands and their signal to noise ratio is related with the charge sensitivity δq as:

$$\delta q = \frac{\Delta q_{rms}}{\sqrt{2RBW}\,10^{\frac{SNR}{20}}} \quad (3.3)$$

[27] where, Δq_{rms} is the induced charge on the gate. The number $\sqrt{2}$ in the denominator comes from the contribution of both side-bands

The low-frequency noise measurement

The amplitude modulation of the carrier frequency comes not only from the intentionally applied gate charge but also from uncontrolled random fluctuations, such

as two-level fluctuators placed on the surface of the nanowires or somewhere near the SET. These random fluctuations at low frequencies broadens the reflected signal in frequency. To measure the low-frequency noise components, the reflected signal is down-converted with homodyne mixing as shown in Fig. 3.9a. The resulting spectral power density is detected with a spectrum analyzer. This is similar to the stability diagram except that there is no low-pass filter prior to detection. In order to calibrate the noise power in charge units, a charge signal (a pilot signal) is applied on the gate. Knowing the rms amplitude of the pilot signal and the RBW of the spectrum analyzer, the whole spectrum can be calibrated in units of $e/\sqrt{\mathrm{Hz}}$

Shot-noise measurement

As have been discussed in section 2.5.3, the shot noise comes from the discrete nature of charge carriers. In hybrid devices of nanowires and superconductors, the effective charge and hence the shot noise depends on the source drain voltage. The changes happens at voltages corresponding to on the onsets of the n^{th} MAR. In the rf-read out, the shot noise is measured with the setup depicted in Fig. 3.9b. For a given current through the device, the shot-noise generated is filtered-out by the tank-circuit and results in a voltage noise at the input stage of the HEMT amplifier. The output noise power is then feed into a spectrum analyzer.

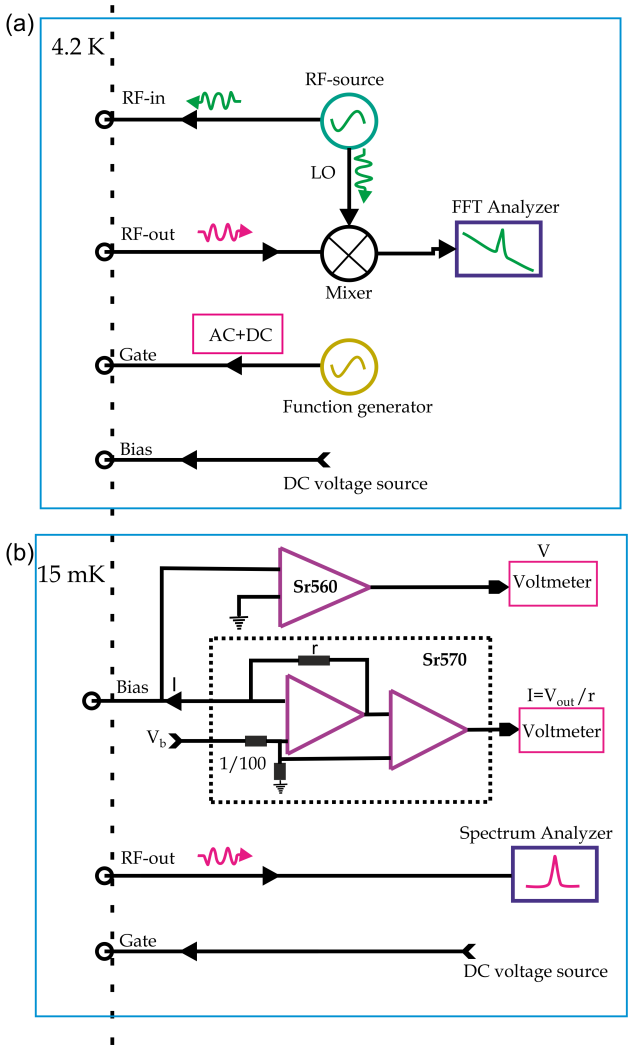

Figure 3.9: a) Low frequency noise measurement scheme. The scheme is the same as the stability diagram. The spectrum analyzer captures the spectral density of the low frequency noise. b) shot noise measurement scheme. The shot noise generated is modeled by a current noise on the sample. The current noise is a function of the current through the device and it is filtered by the tank circuit which results in voltage noise at the input stage of the low temperature HEMT amplifier. The amplified noise signal is then detected with a spectrum analyzer.

Chapter 4

Superconductor-nanowire-superconductor devices

This chapter covers experimental and theoretical results on superconductor-nanowire-superconductor (S-NW-S) hybrid devices. The chapter includes both the normal and the superconducting-state properties of non-suspended devices.

To establish an electrical current through the devices, quasiparticles from the occupied states of one electrode tunnels to energy levels in the nanowire and then tunnels from the nanowire to empty states in the other electrode. Therefore, the current flow depends on the electrical properties of the nanowire and also on the tunneling rate through the S-NW interfaces. While the nanowire electrical properties depend on the length scales such as the mean free path and the coherence length, the tunneling rate mainly depends on the quality of the S-NW interface as well as on the Fermi-wavelength mismatch of the materials. For good contact-interface transparency, Cooper-pairs and Andreev reflection transport are easily observed at low temperatures. For low-quality interfaces, and also in long devices, supercurrent and sub-gap current are suppressed.

A typical current-voltage characteristics is depicted in Fig. 4.1 for a device with good interface contacts and a length of $L \approx 150\,\text{nm}$. Above the critical temperature $T_c \approx 1.1\,\text{K}$, the superconducting electrodes are in the normal state and the IVC (in blue) exhibits ohmic behavior with a normal-state resistance of $R_n = 1.07\,\text{k}\Omega$. When the device is cooled down to temperatures well below T_c, the IVC (in red) shows three distinct conductance regimes. i) For voltages $|V| > 2\Delta/e$, the IVC shows a linear behavior with the same resistance as in the normal state. ii) For lower voltages $|V| \leq 2\Delta/e$, the resistance is of approximately $R_n/2$ and exhibits sub-gap features. iii) At zero voltage $V = 0$, the device switches to a zero-resistance state exhibiting a Josephson current. The voltage-dependence of the conductance originates from the different mechanisms of carrier transport once the superconducting-order parameter is turned on. The results in this chapter have

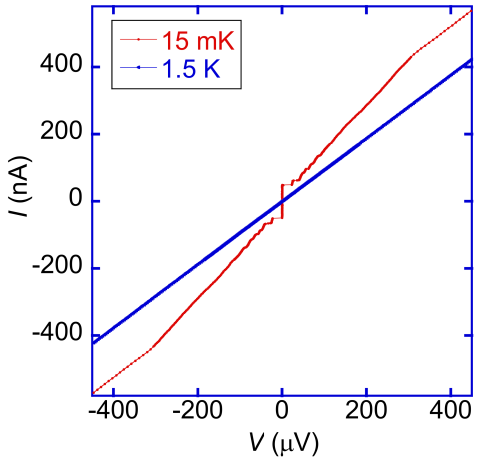

Figure 4.1: Current-voltage characteristics recorded at the normal state $T = 1.5\,\mathrm{K}$ (blue), and superconducting state $T = 15\,\mathrm{mK}$ (red) for a short device $L \approx 150\,\mathrm{nm}$ with $R_n = 1.07\,\mathrm{k\Omega}$. The superconducting state shows three clear regimes, the normal state $|V| > 2\Delta/e$, the sub-gap state $0 < |V| \leq 2\Delta/e$ and the supercurrent state $V = 0$.

been structured in such a way that first the normal state and then the superconducting properties of the devices are discussed.

4.1 Normal state properties

Here, the normal-state refers to the current-voltage characteristic (IVC) at $T > T_c$ or to the part of the IVC at the voltages $|V| \geq 2\Delta/e$. In order to characterize the normal state properties of the devices, such as the electron mean free path, Fermi-wavelength and the number of channels in the nanowires, dc measurements have been done on a large number of devices with a broad range of lengths and resistances. These results are presented in appended paper IV.

The IVCs of the normal state are measured in a two-, or four-point configuration. In the two-point, a bias current is sent through two leads on the nanowire and the voltage drop is measured between the same leads. In the four-point, a bias current is sent through two outer leads while the voltage drop is simultaneously measured across two other inner leads. The normal-state resistance is then extracted from the slope of the IVC. While the two-point measurement includes interface resistances in addition to the nanowire resistance, the four-point measurement gives only the nanowire resistance.

Measurement results of some devices are tabulated in Table 4.1. More information can be found in appended paper IV. In all devices, the nanowires are approximately 80 nm diameter taken from the same growth batch. The devices are categorized into two groups: A, and B. Type A devices are nanowires on a Si/SiO_2 substrate connected by two superconducting contacts. Type B devices are similar

Device		L(nm)	R_n(kΩ)	I_c(nA)	eI_cR_n/Δ	$eI_{exc}R_n/\Delta$
A	1	30	0.16	800	1.02	1.52
	2	90	0.55	95	0.40	0.87
	3	100	0.56	54	0.23	0.65
	4	220	1.04	30	0.24	0.76
B	5a	150	1.07	50	0.41	1.20
	5b	170	1.28	40	0.39	1.28
	5c	180	1.34	36	0.37	1.31
	5d	190	1.37	35	0.36	1.11
	6a	110	1.84	23	0.32	1.21
	6b	200	2.40	12	0.21	0.81
	6c	250	2.72	9	0.20	0.77
	6d	500	4.21	3	0.10	0.71
	6e	600	4.82	1	0.04	0.64

Table 4.1: Measurement properties for non-suspended devices of different length. Type A devices are nanowires with two superconducting contacts. Type B devices are defined on a single nanowire with multiple contacts.

to type A devices but taken from a single nanowire with multiple contacts separated by different lengths, therefore the devices share the same physical properties, such as nanowire diameter. In addition to length dependence, type B devices offer the possibility to take two-, and four-point resistance measurements of a single junction and therefore allow to separate the influence of contact resistances. Two such devices, B_5 and B_6, from two different chips are presented in Table 4.1.

The normal-state resistances as a function of length for both device B_5 and B_6 are plotted in Fig. 4.2. The resistances of each device linearly increases with length, approximately with the same resistance per unit length, $R/L \approx 6\,\Omega/\text{nm}$. Here, the resistance values are taken only from the two-point measurements that also include interface resistances. From the normal-state resistance *v.s.* length, it is possible to estimate the interface resistance by extrapolating to zero length. Assuming symmetric interfaces, for type B_6 device, each contact interface contributes approximately $0.6\,k\Omega$. For type B_5 device, we find that each contact interface contributes less than $90\,\Omega$. We also find that a resistance of two, three and four successive devices ($L = 320$, 500, 690 nm) agrees well with the linear fit of the individual junctions.

Number of channels

Assuming an idealized situation with reflection-less contacts so that electrons approaching one of the contacts have zero probability of being backscattered, we can use a multi-terminal device B_5 to extract the number of channels from a combination of two and four-point resistance measurements.

From the Büttiker-Landauer formalism[35], a two-point resistance can be writ-

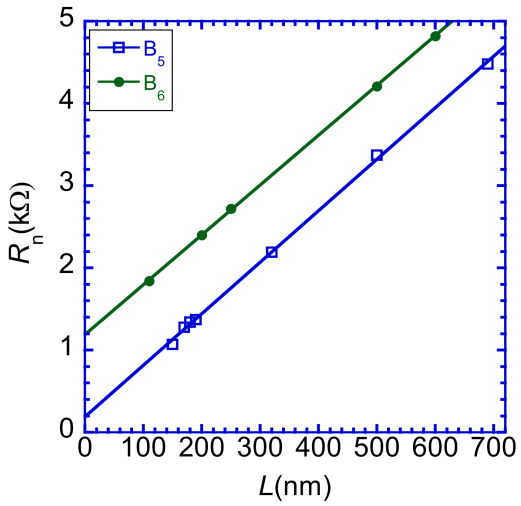

Figure 4.2: a) Normal state differential resistance as a function of length for both B_5 and B_6 devices. The two devices show approximately the same resistance per unit length 6 Ω/nm. The resistances are taken in two point configuration allowing to extract interface resistances by extrapolating to zero length. Each contact interface contributes less than 90 Ω for B_5 and 0.6 kΩ for B_6.

ten as:

$$R_{2p} = \frac{R_q}{NT'} = R_q \frac{1-T'}{NT'} + \frac{R_q}{N} \tag{4.1}$$

$$R_{4p} = R_q \frac{1-T'}{NT'} \tag{4.2}$$

where $R_q = h/2e^2$ is the quantum of resistance, N is the number of channels and T' is the average transparency of the channels. The two- and four-point resistance measurements for the same section, B_{5c}, are $R_{2p} = 1.34k\Omega$, and $R_{4p} = 1.18k\Omega$, respectively. Using these values, the number of channels $N \approx 80$ and the transmission probability $T' \approx 0.12$ are estimated.

Fermi-wavelength

Next there is the question about where these states are situated, near the surface or bulk. At least in bulk InAs, the Fermi-level is pinned in the conduction band as a result of the surface states. In InAs nanowires, there has not been a direct-experimental observation of the surface states other than achieving highly-transparent contact interfaces. The Schottky barrier-free contact interfaces and the n-type nature of InAs nanowires, which are not likely in other semiconducting nanowires, are believed to be the finger prints of the surfaces states (surface-charge accumulation). Considering the whole wire is conducting, we have to solve the Schrödinger equation on a circle to see how much the Fermi-wavelength should

be to fit all channels in the nanowire. The result gives a Fermi-wavelength of $\lambda_F \approx 22\,\text{nm}$.

Electron mean-free path

The elastic mean free path is the average distance which electrons travel in between two elastic scattering events. Assuming the charge-carriers travel at the Fermi-velocity v_F, the mean free path can be expressed in terms of the mean free time, the average time between two scattering events $l_e = v_F\tau$. The mean free time can be estimated from the Drude conductivity, $\sigma = ne^2\tau/m^*$, which gives a mean free path of:

$$l_e = v_F\tau = \frac{m^* v_F}{ne^2\rho} \tag{4.3}$$

The carrier density n, is related to the electro-chemical potential of the system μ, see eq. 2.6. Considering the Fermi-pinning in the conduction band due to the surface charge accumulation, it is reasonable to assume a parabolic energy dispersion in the conduction band. This allows to express the charge density in terms of the Fermi-vector, $n = k_F^3/3\pi^2$.

The mean free path can then be re-written as:

$$l_e = \frac{p_F}{ne^2\rho} = \frac{\hbar k_F}{ne^2\frac{R}{L}A} = \frac{3}{4\pi^2}\frac{h}{2e^2}\frac{\lambda_F^2}{\frac{R}{L}r_w^2} \tag{4.4}$$

Assuming that the wire is homogeneous and uniform we can use the resistance per unit length $R/L = 6\,\Omega/\text{nm}$ in Fig. 4.2. The nanowire radius is $r_w \approx 40\,\text{nm}$. These values give a mean free path of $l_e \approx 46\,\text{nm}$. The value agrees reasonably with what has been previously reported in similar devices. Similarly, the Fermi-velocity is determined to be $v_F = \hbar k_F/m^* \approx 1.3 \times 10^6\, m/s$. The effective electron mass m^* has been taken the same as the effective electron mass in a bulk InAs $m^* = 0.026 m_e$.

Electron mobility

A simple model gives an approximate relationship between the scattering time and the electron mobility. It is assumed that after each scattering event, the electron's motion is randomized, so it has zero average velocity. After that, it accelerates uniformly in the electric field, until it scatters again. The resulting average drift mobility is $\mu = em^*/\tau \approx 3000\,\text{cm}^2/(\text{V}\cdot\text{s})$.

Diffusion length, D

From the Fermi-velocity and the mean free path, electrons move in three dimension with a diffusion constant of D=$v_F l_e/3 \approx 200\,\text{cm}^2/\text{s}$

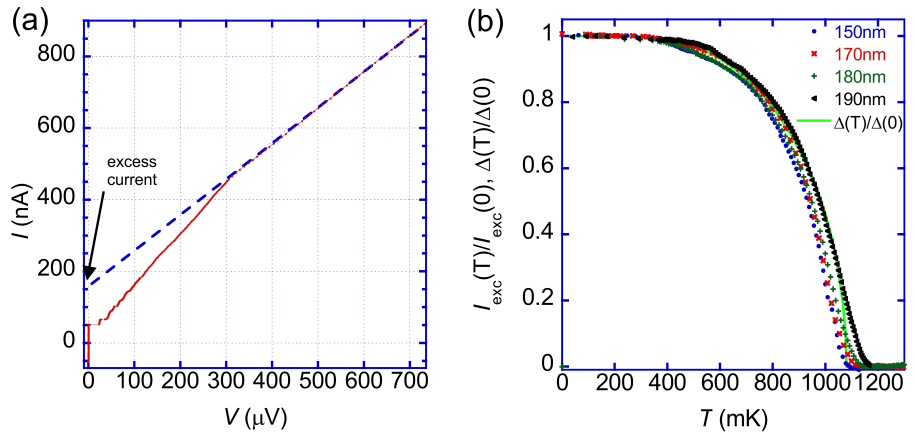

Figure 4.3: a) Current-voltage characteristic of B_{5a} device with length $L = 150\,\text{nm}$ and normal state resistance $R_n = 1.07\,\text{k}\Omega$. The current-voltage characteristic shows a slope change at $V \approx 2\Delta/\text{e}$. This is visible in the excess current shown by a blue dashed line extrapolated to the zero voltage. b) Excess currents as a function of temperature are shown for device B_5 ($L = 150\,\text{nm}$, 170 nm, 180 nm, and 190 nm). The excess currents follow the superconducting energy-gap $\Delta(T)$ (light green).

Coherence length, ξ

The normal state properties can be used to estimate some superconducting parameters, such as the coherent length in the nanowires. For a ballistic case the clean coherence length is $\xi_0 = \hbar v_F/\Delta \approx 1300\,\text{nm}$. For diffusive case, $\xi_D = \sqrt{l_e \xi_0} \approx 250\,\text{nm}$. Most of our devices are in the diffusive $L > l_e$, short $\xi_D > L$, and dirty $\xi_D > l_e$ limit.

4.2 Excess current

Next, we discuss the dissipative branch of the IVCs once the leads switch to a superconducting state. The IVC at $|V| > 2\Delta/e$ is offset by an additional current, the excess current, coming from the Andreev transport.[31, 41] The excess current is defined as:

$$I_{exc} = I - \frac{V}{R_n} \tag{4.5}$$

at $|V| > 2\Delta$/e.

To illustrate the excess current, the IVC for device B_{5a} is shown in Fig. 4.3a. A linear fit at the normal conductance is shown with a blue dashed line and is extrapolated to the zero voltage, giving $I_{exc} = 150\,\text{nA}$ and $I_{exc}R_n/\Delta = 1.20$. To verify the correlation of the excess current with the superconducting gap, the excess current I_{exc} for $|V| > 2\Delta$/e, as a function of temperature is plotted in Fig. 4.3b for device B_5 ($L = 150\,\text{nm}$, 170 nm, 180 nm, and 190 nm). As the temperature is increased, the excess currents do not change significantly up to 300 mK. How-

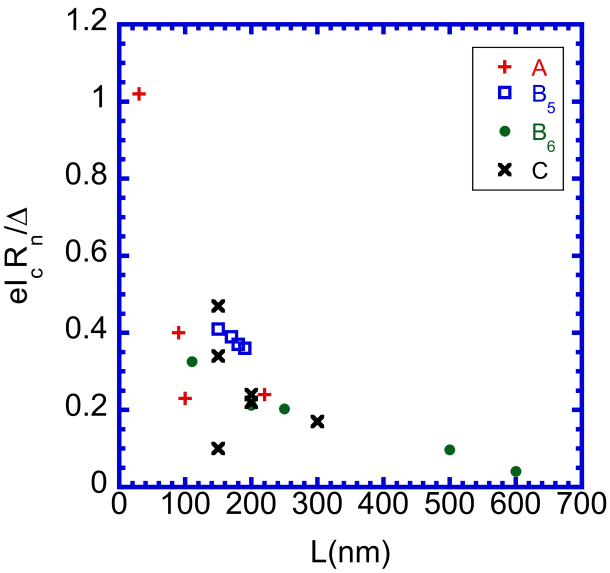

Figure 4.4: (a) The I_cR_n product as a function of length for both A, and B types devices. In the same figure is shown a type C devices, suspended nanowires discusses in chapter 5.

ever, above 300 mK, the excess currents decreased smoothly and are completely suppressed at $T_c \approx 1.1$ K consistent with the suppression of the superconducting energy-gap $\Delta(T)$ shown by the light green line. The excess current is discussed in detail in appended paper IV.

4.3 Supercurrent

For devices with a short length compared to the coherence length and with transparent contact interfaces, a supercurrent can flow through the nanowires as a result of the proximity effect. The supercurrent is driven by the phase difference across the superconducting contacts and its amplitude depends on the magnitudes of the pair potentials in the superconducting electrodes, the interface transparencies and the normal-state resistance of the weak link.

The critical currents for some devices, extracted from the IVCs at the base temperature of 15 mK, are shown in Table 4.1. The critical current I_c exhibits a range of values depending on the resistance and length of the devices, from a few nA to 800 nA. Similarly, the characteristic voltage, *i.e.* I_cR_n product also exhibits a range of values, from 20 μV to 130 μV, depending on the interface transparency and length of the devices. In this section, we present the properties of the supercurrent branch as a function of length, temperature, and magnetic field.

Length dependence

First let us compare the length scales that play an important role in the transport characteristics of the devices. In most of our devices, the separation of the superconducting electrodes is comparable to the coherence length ($L \approx \xi_D$), falling in between the long and short-limit. The wires are mostly diffusive, and in the dirty limit ($l_e \ll \xi_D$). It is also obvious from Fig. 4.2 that the overall resistance increases linearly with the inter-electrode separation L. Since the I_cR_n is a measure of the superconducting coupling strength, it is expected to reduce if the inter-electrode separation L is increased.

To study length dependence of the supercurrent, we have measured several devices with a broad range of lengths, from $L = 30$ nm to 600 nm. The I_cR_n product as a function of length is plotted in Fig. 4.4. According to the theoretical fits shown in the appended paper IV, for the non-suspended devices in Table 4.1, the critical currents are reduced (approximately by a factor of 4) compared to the theoretical values. Reduction of Josephson current is commonly observed in nanowires, and it is also common in 2DEG InAs Josephson junctions[57].

However, in a device of very short length $L = 30$ nm, together with good contact-interface transparencies, the critical current shows a record high value of 800 nA, an order of magnitude higher compared to earlier reports in similar devices. This high value of I_c is attributed to the short channel length and the highly transparent interfaces.

Comparing the elastic scattering length l_e and the coherence length in the nanowire, the device falls in the short ($L << \xi_0$) and dirty ($l_e << \xi$) limit. The measured $I_cR_n = 128\,\mu$eV product is comparable to $\Delta \sim 130\,\mu$eV. The very large I_cR_n product can also be attributed to the small distance between the Al-electrodes. However, even though this I_cR_n product is higher than what has been reported in similar devices, it is still approximately a factor of two less than the expected value for short and dirty devices.[59] Nevertheless, the maximum I_c, even for ideal short devices, is reduced due to an intrinsic Fermi-velocity mismatch at the NW-S interfaces which in turn lowers the I_cR_n product [76]. The comparison to theory is discussed in more detail in appended paper IV.

Temperature dependence

The theoretical description of supercurrents in mesoscopic Josephson devices is based on supercurrent carrying Andreev bound states. The right and the left-going states are separated by energy gaps that are proportional to the phase difference between the two superconductors. At low temperatures only the Andreev levels below the chemical potential are occupied, so that the critical current remains constant. As the temperature is increased, the thermal energy starts to mix the left and right going Andreev levels and the critical current starts to decrease.

To investigated the temperature dependence of the supercurrent in our devices, we have measured IVCs as a function of temperature for a large number of devices.

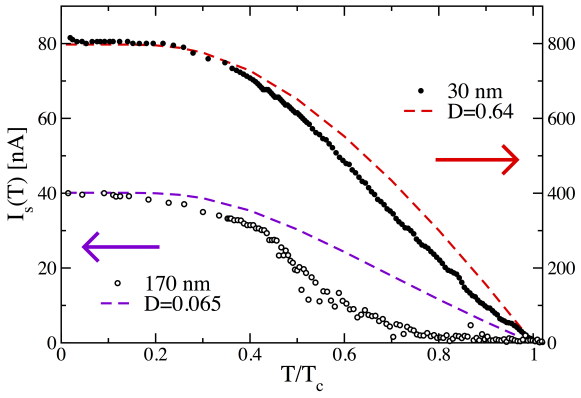

Figure 4.5: Critical currents as a function of temperature for two devices of length $L = 30\,\text{nm}$ and $L = 170\,\text{nm}$. The critical currents at the base temperature of 15 mK are $I_c = 800\,\text{nA}$ and $I_c = 40\,\text{nA}$, respectively. Theoretical fits are also shown for both devices. The theoretical fit for the shortest device works well but deviates from the longer device at high temperature.

Critical currents as a function of temperature for two devices are plotted along with the theoretcial fits in Fig. 4.5. The devices have lengths $L \approx 30\,\text{nm}$ and $170\,\text{nm}$ (sample A_1 and B_{5b}), and the normal state resistances are $R_n = 0.16\,\text{k}\Omega$ and $1.15\,\text{k}\Omega$, respectively. At the base temperature $T = 15\,\text{mK}$, the devices have critical currents of $I_c = 800\,\text{nA}$ and $40\,\text{nA}$, respectively.

There are two obvious observations in the critical current as a function of temperature. First, at low temperatures the critical currents tend to saturate. Second, both device show a monotonous decrease of critical current at higher temperatures. The critical currents are suppressed completely above $T \geq T_c \approx 1.1\,\text{K}$.

The critical current for the shortest device agrees well with the theory in a broad range of temperatures. However, the longer device shows a concave shaped decay at higher temperatures and deviates from the theoretical fit. Such suppression of the critical current might result from premature switching of the device to the dissipative branch due to thermal fluctuations or other noise sources.

At base temperature, we have also obtained IVCs as a function of magnetic field, see appended paper. The magnetic field was applied perpendicular to the superconducting leads and the nanowire. As a function of magnetic field, the critical currents of the devices decreased and are totally suppressed at a critical magnetic field of B_c. The critical magnetic B_c has varied in a range from 20 to 100 mT. No Fraunhofer oscillations are observed in any of the devices consistent with a suppression of superconducting energy-gap in the leads. This is also supported by the decrease of the sub-gap conductance to the normal-state conductance just beyond the critical magnetic field.

Hysteretic behavior was not observed in any of the IVCs due to the lateral con-

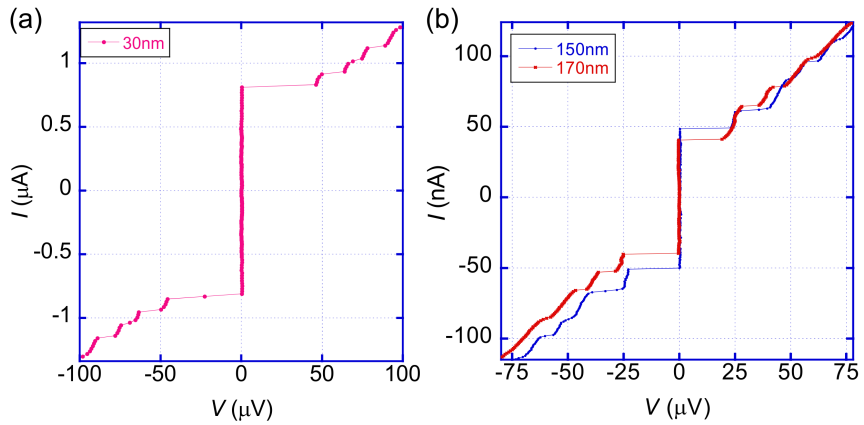

Figure 4.6: Current voltage characteristics at low voltages for device A_1 (length $L = 30\,\text{nm}$ and normal state resistance $R_n = 0.16\,\text{k}\Omega$). The device shows successive voltage jumps with the resistance continuously increasing just after each voltage jump. b) Similarly, the current-voltage characteristics for somewhat longer devices B_{5a} and B_{5b} ($L = 150$, and 170 nm), show similar voltage steps at low voltages.

figuration of the devices with a significant distance between the superconducting electrodes, resulting in a small device-capacitance. The devices dynamics can be explained by the resistively and capacitively shunted device (RCSJ) model.[77, 78] From the geometry of our device, we estimate a capacitance of the order of 1 fF, which results in a Stewart-McCumber parameter of $\beta = 2eI_cR_n^2C/\hbar \approx 0.1 \ll 1$, from which we expect a nonhysteretic IVC consistent with what we observe.

4.4 Sub-gap current

The sub-gap region corresponds to voltages below the superconducting energy gap $|V| < 2\Delta/e$. In most of our devices, in addition to the overall increase of the conductance, the sub-gap conductance has shown two kinds of conductance peaks: i) Conductance peaks that come from the multiple Andreev reflections, where their voltage positions depend on the magnitude of superconducting energy-gap and ii) conductance peaks, mostly near zero voltage, where their voltage positions do not depend on the superconducting energy-gap. These gap independent conductance peaks are observed in all of our devices. In this section, we report the investigation of the sub-gap state as a function of device length, temperature and magnetic field.

A typical IVC, close to zero voltage, is shown in Fig. 4.6a for device A_1 with length $L = 30\,\text{nm}$. Once the device switches to the dissipative state, we can clearly observe successive voltage steps (jumps) in the IVC. We also note that the resistance increases continuously just after every voltage step. Similar to the very short device, the IVCs for device type B_5 also show a series of voltage steps at low voltages. IVCs for two sections, B_{5a} of length $L = 150\,\text{nm}$ and B_{5b} of length $L = 170\,\text{nm}$), are shown in the Fig. 4.6b.

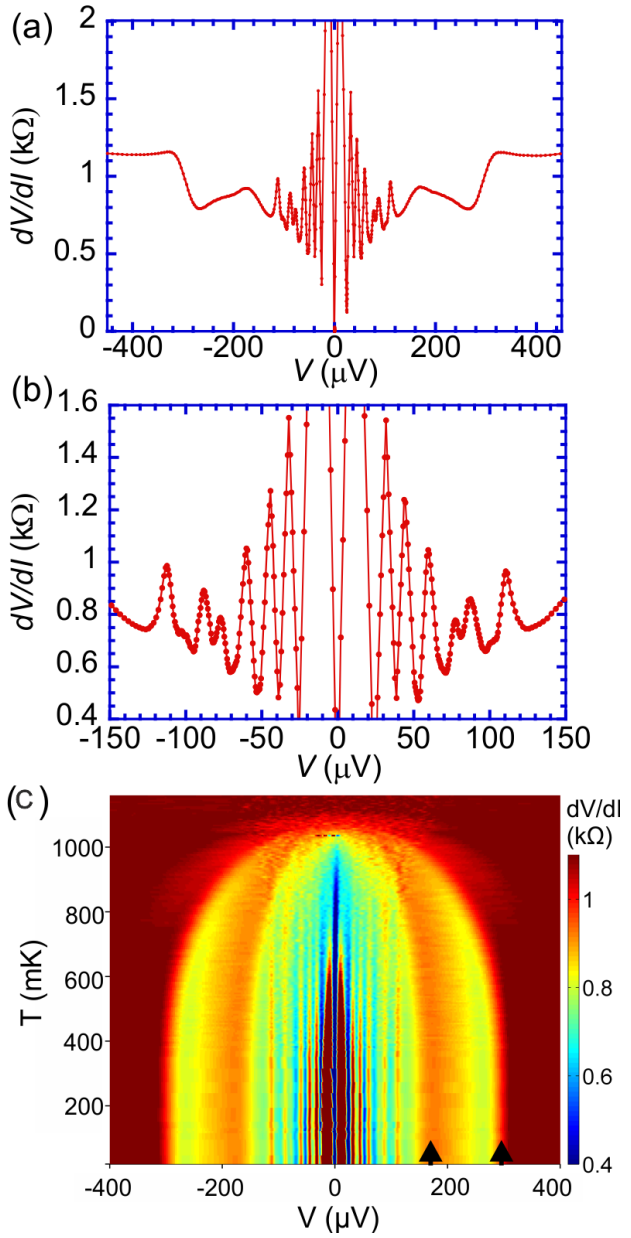

Figure 4.7: (a) The differential resistance dV/dI as a function of voltage for device B_{5b} ($L = 170\,\text{nm}$ and $R_n = 1.15\,\text{k}\Omega$). The resistance substantially decreased at $|V| \approx 2\Delta/e$ and exhibits symmetric resistance peaks/dips. (b) A zoom in of the differential resistance to clearly display the anomalous peaks at low voltages. (c) An image plot of differential resistance dV/dI as a function of voltage and temperature. As the temperature is increased, the first two peaks, marked by two arrows, smoothly move towards lower voltages consistent with the decrease of the superconducting energy-gap $\Delta(T)$. The voltage positions of the other sharper peaks are independent of temperature.

To clearly display details of the sub-gap conductance, the differential resistance dV/dI as a function of voltage is plotted in Fig. 4.7a for device B_{5b}. First, one can observe that the differential resistance substantially decreases from a normal state resistance $R_n = 1.15\,\mathrm{k}\Omega$ at $|V| > 2\Delta/e$ to a sub-gap resistance $R_{SG} \approx 0.7\,\mathrm{k}\Omega$ at $|V| < 2\Delta/e$. Second, we clearly see symmetric sub-gap features (the peaks/dips) in the zoomed-in plot of the differential resistance in Fig. 4.7b.

In order to verify the microscopic origin of these sub-gap features, if they are from multiple Andreev reflection(MAR) or not, we have measured IVCs as a function of temperature and magnetic field. An image plot of the differential resistance dV/dI as a function of voltage and temperature is shown in Fig. 4.7c. As the temperature is increased from 15 mK, the first two peaks/dips (marked by arrows) are smoothly shifted towards lower voltages, in agreement with the decrease of superconducting energy-gap $\Delta(T)$. This indicates that these features have a microscopic origin in multiple Andreev reflections. Using $\Delta \sim 130\,\mu$eV, the features correspond to voltages of $2\Delta(T)/$n, where n=1, and 2. However, the voltage positions of the other sharper peaks are independent of temperature, which indicates that their microscopic origin is actually different from MAR. Nevertheless, their origin has to do with the superconducting nature of the junctions as their amplitudes decay with temperature and are completely suppressed above the critical temperature $T_c \approx 1.1\,\mathrm{K}$.

The differential resistance dV/dI is also characterized as a function of magnetic field at the base temperature. The differential resistance dV/dI for device A_4 at a magnetic field $B = 0$ is depicted in Fig. 4.8a. The device has a length of 220 nm and $R_n = 1.04\,\mathrm{k}\Omega$. The resistance substantially decreases to $R_{SG} \approx 0.7\,\mathrm{k}\Omega$ at $|V| < 2\Delta/e$. There also appear clear sub-gap structures in the sub-gap current region. The extracted resistance as a function of magnetic field is plotted in Fig. 4.8b. While some of the sub-gap structures moves smoothly towards lower voltages following the magnetic-dependent gap Δ(B) some of them stay at constant voltages irrespective of the magnetic field. This magnetic-field dependence of the sub-current complements to the temperature dependence. In fact, it seems that the magnetic field independent features die immediately together with the critical current at $B = 20\,\mathrm{mT}$ while the B-dependent MAR features persist to somewhat higher fields.

To investigate the length dependence of the temperature and magnetic field independent peaks, we have measured IVCs of several devices with a broad range of lengths. The voltage positions corresponding to the peaks in the differential conductance dI/dV are plotted in Fig. 11 for some devices of type A, B and C. C-type are suspended devices that will be discussed in the next chapter. Assuming the peaks are harmonics of a fundamental frequency, we have plotted solid lines corresponding to integer multiples of $V = 24\,\mu$V. This value is obtained by averaging the voltage positions of the lowest peaks. Here, the lowest peak corresponds to the first current step just after the device switches to the dissipative state (see Fig. 4.6b). As can be seen in Fig. 4.9, the anomalous peaks occur at voltages that are almost harmonics of the fundamental peak position and are independent of the

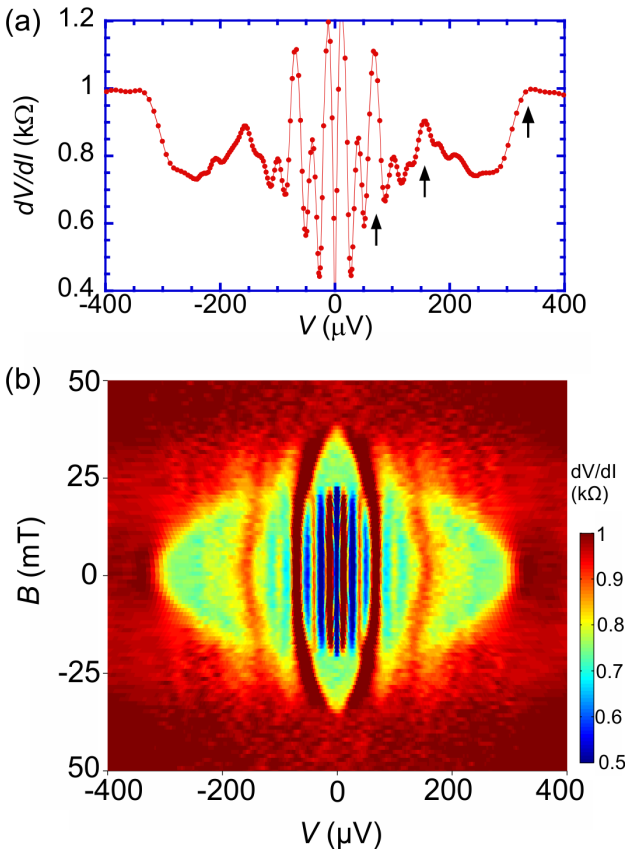

Figure 4.8: (a) The differential resistance dV/dI as a function of voltage for device A_4 ($L = 220\,\text{nm}$ and $R_n = 1.04\,\text{k}\Omega$). The resistance substantially decreased at $|V| \approx 2\Delta/e$ and exhibits symmetric resistance peaks/dips. (b) An image plot of differential resistance dV/dI as a function of voltage and magnetic field. As the magnetic field is increased, some of the resistance peaks smoothly move towards lower voltages consistent with the decrease of the superconducting energy-gap. However, the voltage positions of the other sharper peaks are independent of magnetic field.

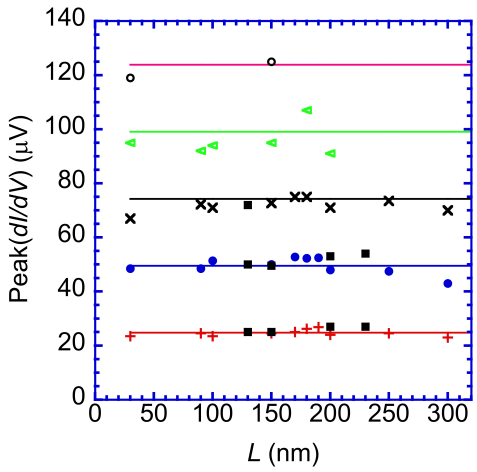

Figure 4.9: Voltage positions corresponding to the temperature independent differential conductance dI/dV peaks for some devices of type A, B and C. Integer multiples of the mean value obtained by averaging the voltage positions for the lowest peaks are shown with solid lines. Compared to the solid lines, the voltage positions of the peaks are almost not only integer multiples of the lowest peaks but also independent of length.

junction length.

The origin of these structures is not clear. The fact that the positions of the temperature- and magnetic-independent structures are the same in different junctions makes it unlikely that they are related to external electromagnetic resonances, but rather result from some general intrinsic mechanism.

Recently, similar conductance peaks have been observed by Kretinin *et al.*[79] in a suspended nanowire and their microscopic origin has been attribute to the coupling of ac Josephson oscillations to longitudinal acoustic waves of the suspended nanowire. However, our experimental observation disagrees with this conclusion on two important points. i) The premises in Ref. [79] is that the anomalous peaks are observed as a result of the suspended nature of the nanowire. However, we observe these anomalous peaks not only in suspended devices but also in non-suspended devices just lying on the Si/SiO_2 substrate. ii) We also find that the fundamental frequency is independent of the device length which is contrary to the claimed $1/L$ length dependence.

Chapter 5

Gate-controlled suspended nanowire devices

The semiconducting nanowire as a weak link offers the possibility to tune the coupling strength with a gate voltage.[21] The gate voltage changes the carrier concentration in the nanowire thereby changing the resistance and the coherence length in the nanowire. This gate-controlled carrier transport and the small-scale size of the nanowires creates promising platform for studying fundamental phenomena such as quantum interferences effects[45, 57] and quantization of the critical currents.[56, 58] This chapter covers the results on gate-controlled charge transport in suspended devices.

The nanowires are suspended 15 nm above local gates as shown in Fig. 5.1. The local gate ensures strong capacitive coupling to the nanowires allowing to tune the conductance from an insulating to metallic state with gate voltages less than ± 10 V. In addition, the local-gate is placed in between the source and drain electrodes, that makes it easier to effectively address only the conductance channel in the nanowire. This allows to individually control different nanowires on a single chip necessary for building integrated circuits.

For electrical transport in these hybrid devices, quasiparticles or Cooper-pairs from one of the superconducting electrodes have to tunnel to the nanowire and then from the nanowire to the other electrode. This charge-transfer process depends on the coupling strength γ which essentially gives the tunneling rate $\gamma/\hbar$ from the nanowire to the electrodes. In this process, if a state in the nanowire is already occupied by a quasi-particle, another electron coming to the nanowire feels electrostatic repulsion force characterized by electrostatic interaction energy U. The electrostatic energy has a substantial effect in a weakly coupled devices $\gamma \ll U$. In a strongly coupled devices, $\gamma \gg U$ the influence of the electrostatic energy is negligible and the quasiparticles or the Cooper-pairs easily flow through the nanowires.

In general, depending on the magnitude of the coupling strength γ, the superconducting energy-gap Δ, and the electrostatic potential U, the devices exhibits

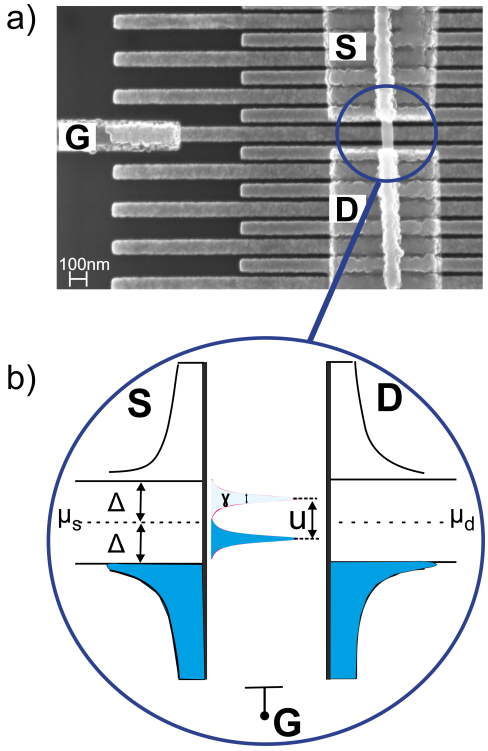

Figure 5.1: a) SEM image of a typical suspended nanowire with a nearby local gate. The device has a 100 nm wide gate-metal stripe and a source-drain length of $L = 200$ nm. b) A schematic energy-digram of the device. The Fremi-levels μ_s and μ_d are for the source and drain electrodes, respectively. The energy levels, each broadened by a width of γ, are separated by a level spacing U.

different charge transport regimes. However, the gate eventually serves as a means to select the transport regime, for example, by changing the coherence length in the nanowire, it can determine if a Cooper pair from either side can tunnel through the device before it dephases in the weak link.

5.1 Strongly-coupled devices

In these devices, the two superconducting leads are strongly coupled $\gamma \gg U$, owing to good contact-interfaces and the presence of conducting channels in the nanowires. As a result, coherent transport through such devices are observed. The effective device length also plays an important role in determining the conductance properties of the devices.

Device		L(nm)	R_n(kΩ)	I_c(nA)	eI_cR_n/Δ	$eI_{exc}R_n/\Delta$
C	1	200	2.23	15	0.24	1.30
	2	150	3.3	13	0.34	1.17
	3	130	2.19	28	0.47	1.02
	4	300	3.80	6	0.17	1.23
	5	150	5.01	2.6	0.10	0.78
	6	200	3.6	7.5	0.21	1.11
	7	150	6.7	2	0.1	1.20
	8	200	13	-	-	-
	9	300	40	-	-	-

Table 5.1: Measurement properties for suspended-devices of type C. For devices C_8 and C_8, the critical currents are suppressed at $V_g = 0$

Current-voltage characteristics

The current-voltage characteristics have been recorded in a similar way as the non-suspended devices except that many IVCs have been take at different gate voltages. The gate, locally creates a potential barrier in the nanowires, controls the transmission probability through each conducting channel, thereby changing the coupling strength of the junction. The possibility of controlling the transmission probabilities $T'(V_g)$ allows to observe cross over from a distinct S-normal metal-S (SNS) type behavior to tunneling S-inslulator-S (SIS) type behavior.

To display the gate-dependence, an image plot of the differential conductance dI/dV as a function of gate and voltage is shown in Fig. 5.2a for device C_1 in Table 5.1. The device has a length $L = 200\,\text{nm}$ and $R_n = 2.23\,\text{k}\Omega$. From the image plot, one can make two simple observations. First, the overall conductance at $V \gg 2\Delta/e \approx 260\,\mu\text{V}$ increases with the gate voltage. In addition, along the gate axis, the normal conductance increases in steps at $V_g = -3$ and -1.3 V. Second, the conductance increases in the sub-gap region, at $|V| \leq 2\Delta/e \approx 260\,\mu\text{V}$ and also with the gate voltage. IVCs for three different gate voltages $V_g = -3, 0, 2.5\,\text{V}$ are plotted in Fig. 5.2b. The IVCs show similar behavior as the non-suspended devices except the magnitude depends on the gate voltages.

Gate-tunable Josephson current

The concept behind the tunable critical current is nothing but changing the coherence length ξ in the nanowire weak links. The coherence length ξ in the nanowire increases with the carrier concentration which in turn is tunable with the gate voltage. To display the gate-dependence of the Josephson current, an image plot of the differential resistance dV/dI as a function of source-drain current and gate voltage is shown in Fig. 5.3a for device C_1. The plot clearly displays the supercurrent-branch as the deep blue area. The overall area increases as the gate is stepped from negative to more positive values consistent with the overall decrease in resistance.

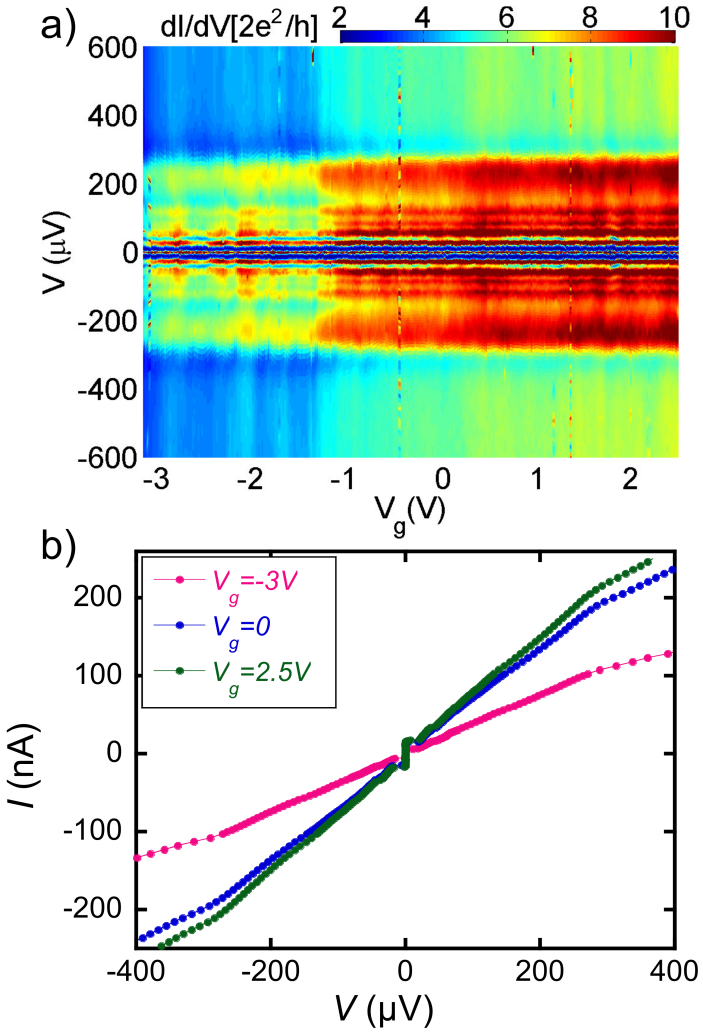

Figure 5.2: a) The differential conductance dI/dV as a function source-drain voltage and gate for sample C_1. In addition to the over all increase in conductance with the gate voltage, sharp-conductance changes are observed in both axises. Along the gate-axis, steps in the conductance are observed at -3 and -1.3 V. Along the source-drain axis, the conductance increases at voltages $V \leq 2\Delta/e \approx 260\,\mu$V as the transport mechanism changes from the single-particle to the multi-particle Andreev reflections. b) IVCs for three different gate voltages $V_g = -3, 0, 2.5$ V.

The critical current and the normal state differential resistance as a function gate voltage are presented in Fig. 5.3b. The differential resistance is taken at source-drain voltage of $V = 2\,\mathrm{mV} \geq 2\Delta/e$. The resistance decreases in steps while the critical current increases in a similar fashion. Also, on top of the over all increase in the critical current, the switching current fluctuates with gate voltage which is directly correlated with the fluctuation of the normal-state conductance. The conductance fluctuations are due to interference effects of charge carriers mediated by the scattering centers in systems when the electron-mean free path is less than the device length $l_e \ll L$. These mesoscopic conductance fluctuations depend on the carrier concentration and are therefore observed as a function of the gate voltage.

The correlation between the measured normal state conductance and the critical current can be verified by the I_cR_n product. The I_cR_n product depends only on the superconducting energy-gap of the contacts, therefore, when the resistance of the device changes the critical current has to change so that the I_cR_n product remains constant. The I_cR_n product as a function of the gate voltage is plotted in Fig. 5.3c. We observe on average a constant $I_cR_n \approx 30\,\mu\mathrm{V}$ over a wide range of gate voltage. The constant value of the I_cR_n product confirms that the critical current is related to the normal state conductance.

Quantized-conductance and its correlation to the supercurrent

For short and ballistic one-dimensional weak links $l_e \ll L$, such as atomic-point contacts, the conductance at low temperature is expected to increase in quantized steps as a function of gate voltage.[36] In line with the conductance quantization, the critical current through short and ballistic weak-links is also predicted to be quantized with a step height of $\delta I_c = e\Delta/\hbar$ [80], see section 2.2.2. For our sample δI_c should be $\sim 30\,\mathrm{nA}$.

In nanowire weak links such properties have been difficult to observe, mainly due to less transparent interfaces and the scattering of electrons in the conduction paths: reflections of electrons due to scattering centers such as crystal defects, impurities, Schottky barriers, surface states. Backscattering by such inhomogeneities smear out the conductance steps.

To realize quantization in both the conductance and the critical current, suspended devices that are short length and strongly coupled to superconducting electrodes has been prepared. In these devices, the number of conducting channels is reduced gradually with negative gate voltages, and we observe a stepwise decrease of both conductance and critical current before the conductance vanishes completely. This is shown in Fig 5.4 for device C_7 and described in more detail in the append paper III.

Sub-gap conductance

Similar to the non-suspended devices, we have also investigated the sub-gap region, $V \leq 2\Delta/e$, properties of the suspended devices. The differential resistance

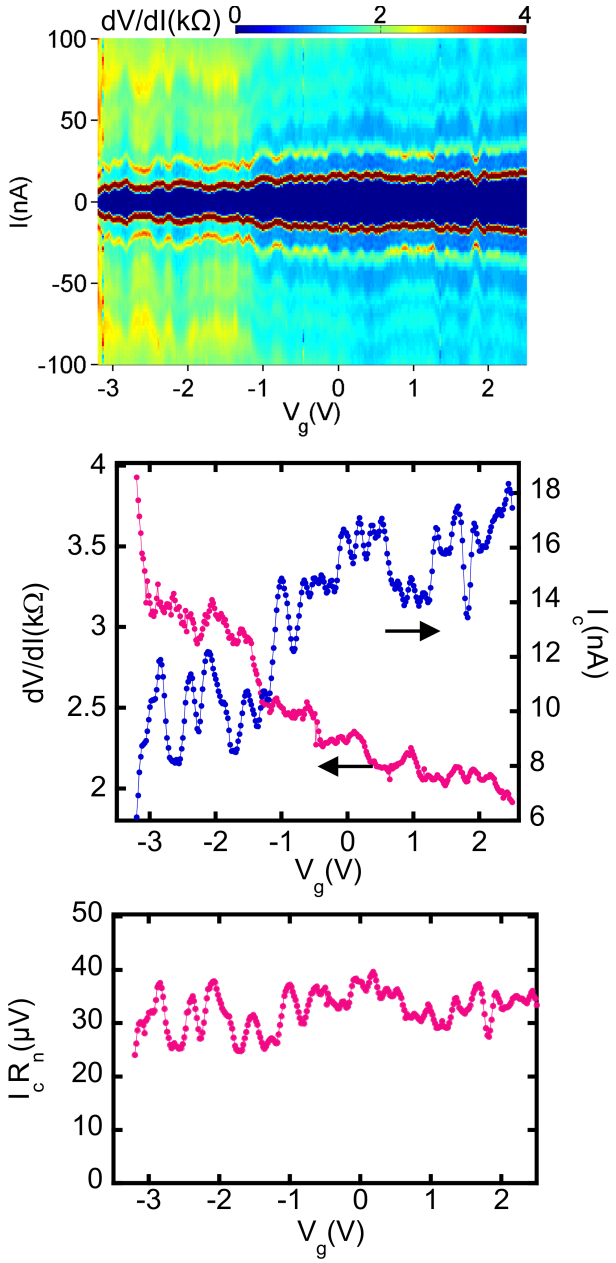

Figure 5.3: a) An image plot of the differential resistance as a function current and gate voltage. The boundary of the supercurrent area varies with the gate voltage. b) The critical current I_c and normal state resistance dV/dI as a function of the gate voltage. The conductance and critical current increases roughly linearly with the gate voltage. c) The I_cR_n product as a function of gate voltage. The I_cR_n product roughly shows a constant value of $30\,\mu$V. The constant value confirms that the critical current is correlated with the normal state conductance.

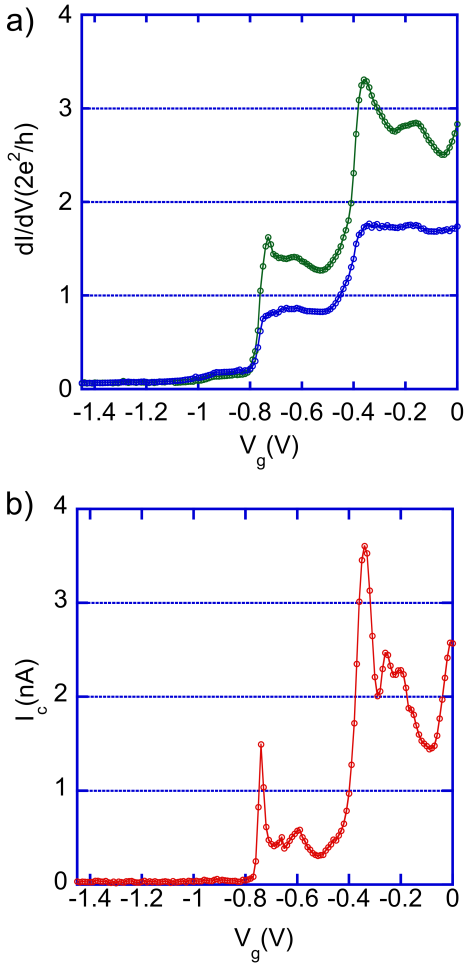

Figure 5.4: a) Normal state conductance (blue) and a sub-gap conductance (green) as a function of gate voltage. The normal state conductance, extracted at $V = 1\,\mathrm{mV}$, clearly displays a step wise increase of the conductance as a function of the gate voltage. The sub-gap conductance, taken at $V = 125\,\mu\mathrm{V} \sim \Delta/e$, also increases in steps but with step height larger than the normal state conductance. b) The critical current as a function of the gate voltage. The critical current also increases in steps directly correlated with the normal state conductance.

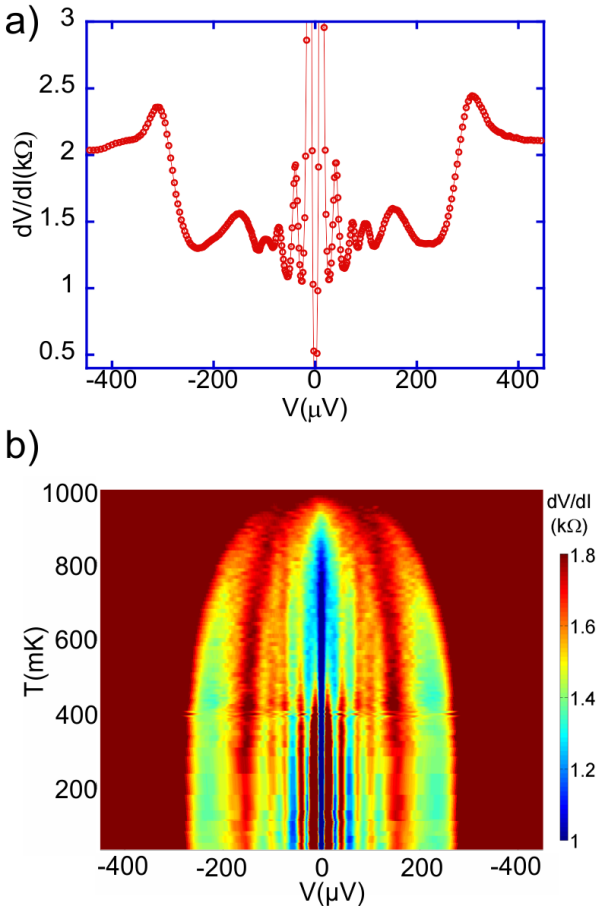

Figure 5.5: a) The differential resistance dV/dI as function of source-drain voltage for a device of length $L = 200\,\text{nm}$ and normal state resistance $R_n = 2.2\,\text{k}\Omega$. The resistance substantially decreased at $V \approx 2\Delta/e$ and exhibits symmetric resistance peaks/dips. b) An image plot of differential resistance dV/dI as a function of source-drain voltage for different temperatures. As the temperature is increased, the first two peaks smoothly move towards lower source-drain voltages consistent with the decrease of the superconducting energy gap $\Delta(T)$. However, the voltage positions of the other anomalous peaks are independent of temperature.

dV/dI as a function of source-drain voltage at $V_g = 0\,\mathrm{V}$ is shown in Fig. 5.5a for device C_1. The obvious observation is that the differential resistance substantially decreases from the normal-state resistance $R_n = 2.2\,\mathrm{k}\Omega$ to the sub-gap resistance $R_{SG} \approx 1.2\,\mathrm{k}\Omega$. The ratio $R_n/R_{SG} \approx 1.8$ indicates that the interfaces are highly transparent, close to ideal.

The sub-gap region also displays resistance dips/peaks similar to those seen in the non-suspended devices. The differential resistance dV/dI as a function of source-drain voltage and temperature is shown in Fig. 5.5b. As the temperature is increased from 15 mK, the first two peaks/dips are smoothly shifted towards lower voltages, in agreement with the decrease of the superconducting energy-gap $\Delta(T)$. This implies that these two features have a microscopic origin in multiple Andreev reflections (MAR). Using $\Delta \sim 130\,\mu\mathrm{eV}$, the features correspond to voltages of $2\Delta(T)/n$, where $n = 1$, and 2. However, the voltage positions of the other peaks are independent of temperature which indicates that their microscopic origin is actually different from MAR. These results are described in detail in the appended paper IV.

5.2 Weakly coupled devices

Fabry-Perót like interference

The superconductor-nanowire interfaces are not always ideal. If the interface transparency is low and the coherence length in the nanowires is long compare to the device length, $\xi \gg L$, the device can serve as a resonator similar to the Fabry-Perot resonator in optics. The formation of resonant states in the nanowire leads to oscillations in the conductance and the critical current. These interference effects are dependent on the carrier concentration, and therefore are observed as a function of gate voltage or magnetic field. In this section, we will discuss such gate-dependent conductance and critical current oscillations.

In equilibrium, at zero source-drain and gate voltage, the resonant states are above the Fermi-level and the supercurrent is suppressed. The states could be accessible for charge transport by either gate-controlling the Fermi-level in the nanowire or by applying source-drain voltages, a bias spectroscopy. To observe these states, the level spacing has to be greater than the thermal energy k_BT to prevent smearing out of the levels. The level spacing, assuming particle in a box states, is proportional to the Fermi-velocity and is expected to be well defined in InAs nanowires owing to the low effective mass $m^* = 0.026m_e$. In addition, the nanowires for this purpose has been chosen to have smaller diameters, on the average of 40 nm to 60 nm.

An image plot of the differential conductance dI/dV as a function of gate and source drain voltage for device C_8 of length $L = 200\,\mathrm{nm}$ and a relatively high normal state resistance, $R_n = 13\,\mathrm{k}\Omega$ at $V_g = 0$ is shown in Fig. 5.6a. In the image plot, we observe a chess-board-like conductance modulation at low bias, Fabry-perot interferences. The pattern is symmetric with respect to the source-drain axis.

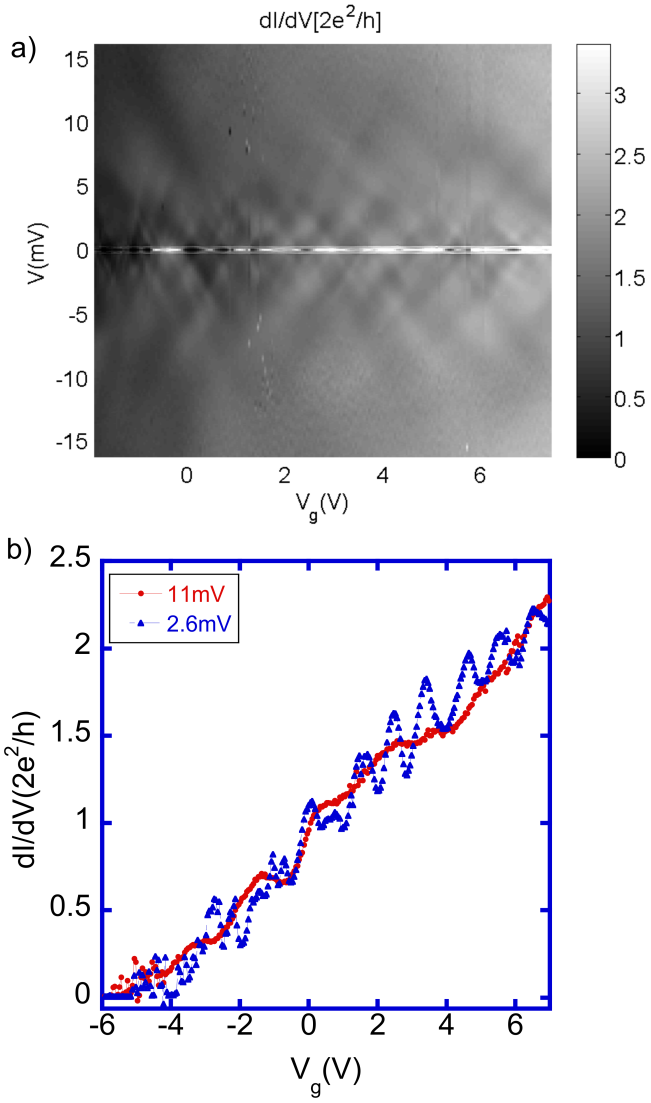

Figure 5.6: (a) An image plot of differential conductance dI/dV as a function of gate and source-drain voltages for device C_8 of length $L = 200$ nm. The conductance shows a Fabry-Perot like interference effect due to the longitudinal quantization. (b) Line cuts of the image plot in (a) for two source-drain voltages. They are taken at voltage of 2.6 mV (in blue) and 11 mV (in red). The conductance oscillations are clearly visible at the low bias voltage 2 mV but are smeared out at the higher bias voltage 11 mV.

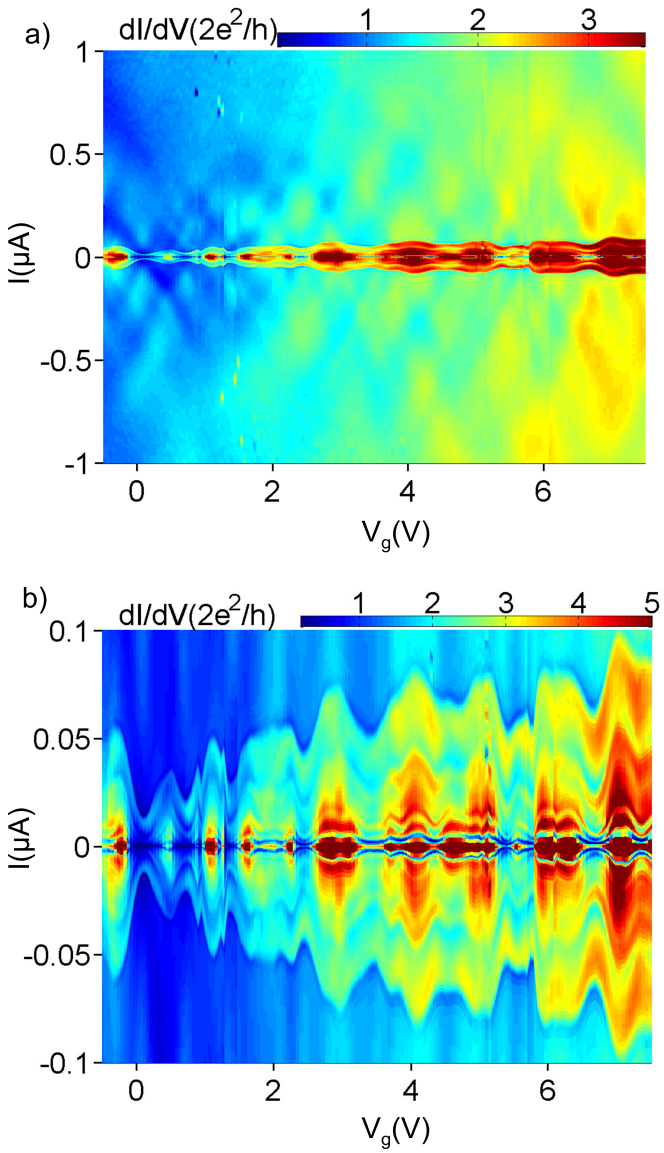

Figure 5.7: a) An image plot of differential conductance dI/dV as a function of current and gate voltage. The normal state conductance shows a Fabry-Perot like interference effect due to longitudinal quantization. Similarly, in addition to the overall increase in conductance, the sub-gap conductance also shows a quasi-periodic modulation with the gate voltage. b) The same differential conductance image in (a) zoomed-in near zero-current. The critical current varies with the gate voltage and has high/low values corresponding to the on/off resonance states.

The Fabry-Perot conductances are clearly visible at low bias, for $V > 5\,\mathrm{mV}$ the features are smeared at high bias. These can be explained in terms of potential-barriers present at both interfaces. At low bias voltages, the barriers are well defined and the bound energy states are well discretized to reveal the longitudinal quantizations. At high bias voltage, the potential barriers are shallow and more transparent to energetic single-particles, or the wave-function of the quasi-particles leaks more into the source-drain electrodes, giving rise to broader energy levels that are not well defined compared to the thermal energy. This results in a smeared conductance.

Two line cuts of the differential conductance are shown in Fig. 5.6b to clearly display the bias dependence. At high-bias voltage $V = 11\,\mathrm{mV}$, the overall conductance increases with the gate voltage, from a completely depleted (insulating) to a conducting regime revealing no clear conductance oscillations. However, the conductance increases in steps with step heights smaller than the conductance quantum $2e^2/h$. At low-bias voltages $V = 2.6\,\mathrm{mV}$, the conductance increases in similar fashion as the high-bias voltages except with conductance oscillations, Fabry-Perot like interferences. These conductance oscillations are clearly visible in the conducting regime, once the gate opens a few channels. These quasi-periodic conductance modulations are unlikely to be Coulomb blockade oscillations since they are observed at total conductance $G_n \approx 1.5(2e^2/h)$ much higher than the necessary condition for Coulomb blockade $G_n \leq 0.5(2e^2/h)$.

The way to verify that these conductance oscillations are Fabry-Perot like interferences is to compare the wavelength corresponding to the energy-level spacing $\triangle E$ with the effective channel length. The average level spacing $\Delta E \approx 5\,\mathrm{mV}$ is extracted from the conductance oscillations along the source-drain voltage. The device length can be estimated from the wavelength, $L_{eff} = \hbar v_F \pi/(\triangle E) \approx 50\,\mathrm{nm}$. This effective length is less than the actual length of the device $L = 200\,\mathrm{nm}$. The smaller effective length might be explained by the non-uniform electric field of the gate on the nanowire. The electric field is more effective in the middle of the nanowire and has a weak effect near the interfaces owing to the screening by the metals, creating a potential difference along the conduction paths implying a shorter channel length.

To relate the critical current to the Fabry-Perot conductance oscillations, the same image plot of the differential conductance dI/dV is shown in Fig. 5.7a, but now, the current is shown in the y-axis. In addition to the Fabry-Perot interferences, in the sub-gap region, we clearly see an enhanced sub-gap conductance (red) traversing the whole gate range while its magnitude is modulated by the gate voltage. The higher conductance regions happen right at positions where the Fabry-Perot resonances intersect the zero current. Similarly, the lower conductances happen at positions in between these resonance states. The critical current (deep red) is directly correlated with the sub-gap conductance and shows a maximum value at gate voltages corresponding to the resonances crossing at the zero current and shows lower values otherwise. The scenario is clearly visible in the zoomed in picture of the same plot in Fig. 5.7b.

5.2.1 Crossover from Coulomb blockade to supercurrent

Next we discuss devices where the nanowires are weakly coupled by tunnel barriers to two superconducting reservoirs, forming a quantum dot. The tunnel barriers are defined by the non-ideal S/NW interfaces. If the barriers are strong enough to localize charge carriers for long time, Coulomb interaction of charge carriers leads to observation of Coulomb blockade. When the Fermi level lies right on resonance states, a supercurrent can flow through the device proportional to the superconducting energy-gap Δ but scales as $(e/\hbar)\gamma\Delta/(\Delta+\gamma)$.[81] This section covers a widely gate-tunable suspended device C_9, from a completely insulating to superconducting state combining different transport regimes. These results are described in append paper II.

The device had a 100 nm wide gate stripe, a length of $L = 300$ nm, and a normal state resistance of $R_n = 40\,\mathrm{k}\Omega$ at $V_g = 0$ V was measured at a temperature of 15 mK. As a result of the high resistance compared to the quantum resistance, the carrier transport is due to tunneling and the supercurrent is highly suppressed. The data shows a low conductance at low-bias voltages except at source-drain voltages corresponding to $V = 2\Delta$, where we observed enhanced conductance. The increase in conductance indicates an increase in the tunneling probability which is attributed to the large density of states in the superconducting reservoirs at $V \approx 2\Delta$. The conductance at this voltage is clearly visible by two bright lines in the differential conductance Fig. 5.8b, indicated by arrows.

At high negative voltage $V_g < -1.1$ V, the conducting channels are pushed all the way beyond the Fermi-level and the nanowire is completely depleted of charge carriers. At $V_g = -3$ V, the device showed no electrical conductivity for source-drain voltages $V \leq 0.5$ V (not shown here). However, once the gate voltage is increased close to the pinch-off, $V_g \approx -1.1$ V to -0.5 V, and near to $V = 0$ V, few electrons starts to conduct showing Coulomb-blockade diamonds, see Fig. 5.8a.

At positive but small gate voltages, narrow resonance states in the nanowire comes to mediate quasiparticle transport across the device. Depending on the gate voltage, the normal state conductance varies between weakly conducting state on resonance and tunneling behavior off-resonance. The narrow states also indicate weak coupling to the leads which is consistent with the very limited coherent transport of Cooper pairs on resonance. The behavior is depicted in Fig. 5.8b.

When the gate is increased to more positive values, wider resonance states which are better coupled to the leads comes to play an important role in the transport. When the Fermi-level is aligned right on the resonance levels, supercurrent flows through the nanowire consistent with the on-resonance normal state conductance. The supercurrent is the deep red color in the image plot Fig. 5.8c. However, when the Fermi-level is aligned in the middle of the level spacing, no supercurrent flows through the device, shown in a deep blue in the Fig. 5.8c. At high positive gate-voltages, more conducting channels are brought below the Fermi-level resulting in an increase of the carrier concentration thereby increasing the coherence length. This improves the coupling to the superconducting reservoirs. As a

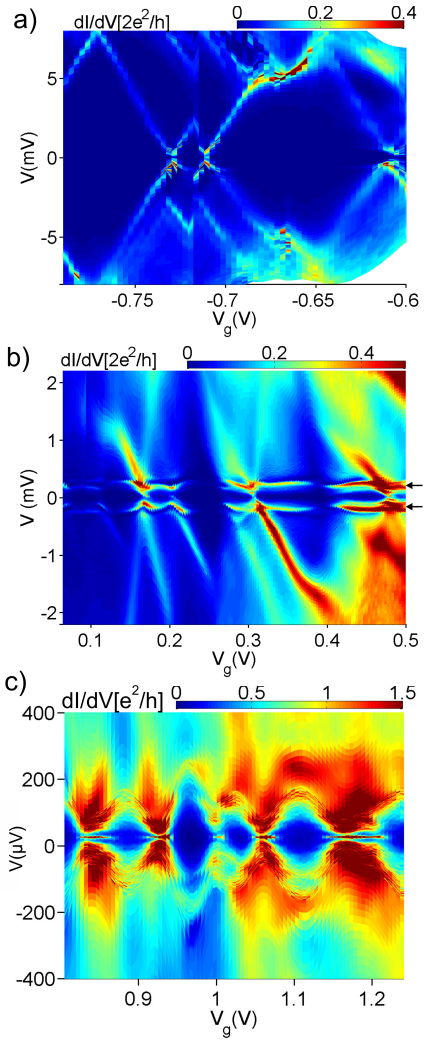

Figure 5.8: An image plot of differential conductance dI/dV as a function of gate and source-drain voltages for a device of length of $L = 300\,\text{nm}$. a) At high negative gate voltage just before the device is depleted of carriers. The image plot clearly shows Coulomb blockade diamonds with superconducting energy gap in the middle. b) At positive and low gate voltages. The conductance with the gate voltage shows sharp resonances crossing at the zero source drain voltage. The conductance increase is also visible at $V \approx 2\Delta \approx 260\mu$V. c) The interplay of Coulomb blockade and supercurrent depending on the gate voltage.

result, a supercurrent flows through the device with its magnitude monotonically increasing with the gate voltage.

Chapter 6

Radio-frequency read-out of nanowire based devices

The chapter covers experimental results acquired based on the radio-frequency read-out technique. The read-out is conducted on two types of suspended devices: i) InAs nanowires coupled to Al-based superconductors and ii) single-electron transistors SETs realized by heterostructure-nanowires of InAs/InP. The chapter is then roughly divided into two parts depending on the nature of the devices. The first part deals with the hybrid devices and the second part deals with the nanowire heterostructures.

6.1 Radio-frequency read-out on InAs nanowires coupled to superconductors

The current-voltage characteristics of superconductor-nanowire-superconductor junctions (SNS) have been presented in chapter 4. In general, the transport characteristics in the superconducting state shows three conductance regimes depending on the voltage. i) The normal-state conductance, above the superconducting energy-gap $|V| > 2\Delta$, b) the sub-gap conductance, below $|V| \leq 2\Delta$ and c) the supercurrent, at the zero-bias voltage. The current in the normal state is carried by single-particles with a charge size of $q = e$. The sub-gap current is carried through Andreev reflections. Each Andreev reflection transfers effective charge size of $q^* = 2e$. Depending on the incoming energy of the electrons, multiple Andreev reflections also contribute to the sub-gap current. The n-times Andreev reflections transfer effective charge size of $q^* = (n+1)e$. Thus, the shot noise power spectral density $S(f) = 2q^*IF$, proportional to the effective charge size q^* (the shot size), is expected to vary in line with these different transport mechanisms. In particular, the Fano factor is expected to increase in steps with decreasing the voltage, due to the openings of channels for higher order MARs.

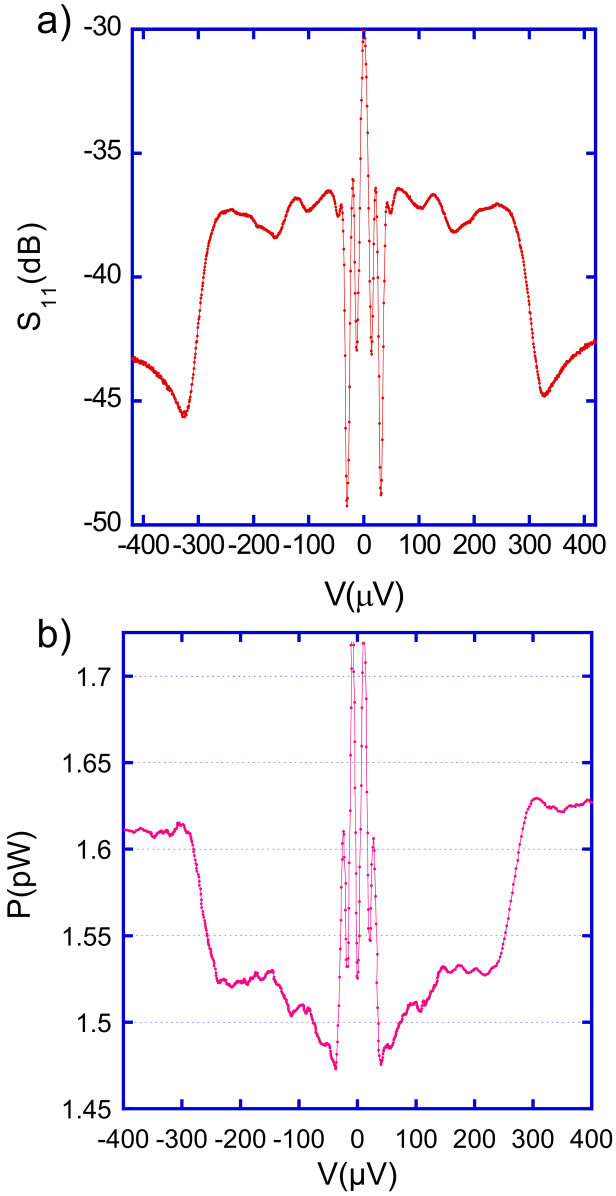

Figure 6.1: (a) A reflection coefficient as a function of bias. The reflection coefficient shows a substantial decrease in magnitude at $|V| \leq 2\Delta \approx 260\,\mu$V. It also manifests pronounced sub-gap structures. b) The noise power measured as a function of voltage. The noise power is integrated in frequency range within the bandwidth of the tank-circuit, $\delta f = 7\,\text{MHz} \ll \Delta f$.

6.1.1 Shot noise

Here, a radio-frequency set-up is implemented to study the shot noise in suspended nanowire junctions. The set-up is shown in Fig. 3.9b. To measure the shot noise as a function of bias current, no radio-frequency signal is sent to the device, rather the signal output of the amplifier is directly feed into a spectrum analyzer. The shot noise in the device, modeled as a current source, see section 2.5.3, in parallel with the resistance of the device, is filtered by the tank circuit and creates a voltage noise in the input stage of the cold amplifier. The voltage signal is then amplified with both cold and room temperature amplifiers before it is feed into the spectrum analyzer.

First, we measured the reflection coefficient as a function of voltage. The reflection coefficient at the resonance frequency 620 MHz is shown in Fig. 6.1a for a device of length $L = 150\,\text{nm}$ and $R_n = 3\,\text{k}\Omega$. The reflection coefficient exhibits a similar behavior as the conductance of the dc-measurement. The reflection manifests a substantial decrease in amplitude at voltages $|V| \leq 2\Delta$ which correspond to the change in resistance of the device. It also exhibits pronounced sub-gap structures that are well resolved due to the the measurement scheme.

In Fig. 6.1b, the noise power is plotted as a function of voltage. The noise power is integrated at the resonance frequency with a frequency range of $\delta f = 7\,\text{MHz}$. The frequency range is taken within the bandwidth Δf of the tank-circuit, *i.e.* $\delta f \ll \Delta f$. The behavior of the measured noise power corresponds well to the reflection coefficient. decreases in steps as the voltage decreases which is directly correlated with the reflection structures in Fig. 6.1a. The analysis of the Fana-factor F as a function of voltage is at its early stage and is not included in this thesis.

6.2 RF-SET based on InAs/InP nanowire heterostructure

In a conventional SETs, two tunneling barriers define the island of the SET.[13, 14, 62] In the nanowire heterostructure, the island is defined by growing two InP barriers in the middle of an InAs nanowire. The tunnel barrier arises from the difference in the electronic-band structure of the two materials, carriers have different Fermi-velocity and effective mass. The barrier height depends on the electron affinity difference between the two materials.

The sequential tunneling of electrons, SET behavior in DC, has been realized in nanowire devices.[15] Here, we demonstrate RF-SET operation for two devices based on nanowire heterostructures of InAs/InP. The devices are prepared from two sets of nanowire heterostructures. While the higher resistance, 600 kΩ, has 4-5 nm thick InP barriers at a spacing of 150 nm, the second lower resistance 55 kΩ has 2-3 nm thick InP barriers at a spacing of 50 nm introduced in the middle of the InAs nanowires (2-3 μm long). A schematic diagram for the SET devices is shown in Fig.6.2a.

6.2.1 Stability diagram

The first step in the radio-frequency read-out is to identify the resonance frequency of the tank circuit. In measuring the two sets of devices we have used two HEMT amplifiers, center frequencies at 450 MHz and 350 MHz for the high and low resistance devices, respectively. The resonance frequency 499 MHz and 367.5 MHz are determined for both devices, respectively, by selecting suitable inductors as described in section 3.4. Here, the stability diagram for only the higher resistance is presented.

The stability diagram is recored using the setup in Fig. 3.8a. To acquire the stability diagram, for each fixed source-drain voltage, the gate voltage is swept while a weak radio frequency signal at 499 MHz is launched towards the tank circuit. The gate voltage is applied by a function generator that combines a dc-offset voltage and an ac-ramp signal at a frequency of 47.9 Hz. The reflected signal is amplitude modulated by the SET resistance. The resulting stability diagram at a temperature of 1.5 K is shown in Fig. 6.2. At negative gate voltages, the device displays Coulomb-blockade diamonds with sharp edges. At positive gate voltages, the barrier strength decreases due to n-type nature of the InAs nanowires giving rise to rounded edges of the Coulomb-blockade diamonds. The period along the gate voltage $\Delta V_g \approx 15\,\mathrm{mV}$ corresponds to e/C_g, giving a gate capacitance $C_g \approx 11\,\mathrm{aF}$. The charging energy $E_c \approx 1.2\,\mathrm{meV}$ corresponds to a total capacitance of $\mathrm{C}_\Sigma \approx 70\,\mathrm{aF}$.

6.2.2 Charge sensitivity

In the RF measurements, we have already seen that the reflected signal is amplitude modulated with the gate charge on the SET. This amplitude modulation of the reflected signal has steep slopes for certain values of the gate charge. A very small gate charge variation at the steep slopes of the Coulomb oscillations, gives high modulation in the power of the reflected signal. The measurement of the charge sensitivity is conducted with the setup in shown Fig. 3.8b. Although, this has been done for the two devices, here we report for the low resistance device taken at a temperature of 1.5 K.

To measure the charge sensitivity, the source-drain bias and the dc-gate voltage are first set to maximize slope of the Coulomb oscillations. The carrier signal $f_c = 367.5\,\mathrm{MHz}$ is then amplitude modulated by a weak pilot signal applied to the gate. The gate signal has a frequency of $f_g = 200\,\mathrm{kHz}$ and induces a charge amplitude of $\Delta q_{rms} = 2.9\,\mathrm{m}e$. The power of the carrier signal is $-72.7\,\mathrm{dBm}$ at the tank circuit. The reflected rf-signal is amplified and directly feed into a spectrum analyzer. The resulting power spectrum is shown in Fig. 6.3a. The carrier signal f_c appears with two side bands at frequencies corresponding to the sum $f_c + f_g = 367.7\,\mathrm{MHz}$ and the difference $f_c - f_g = 367.3\,\mathrm{MHz}$. The amount of power (signal to noise ratio, SNR) in these side bands determines the charge sensitivity of the SET. The charge

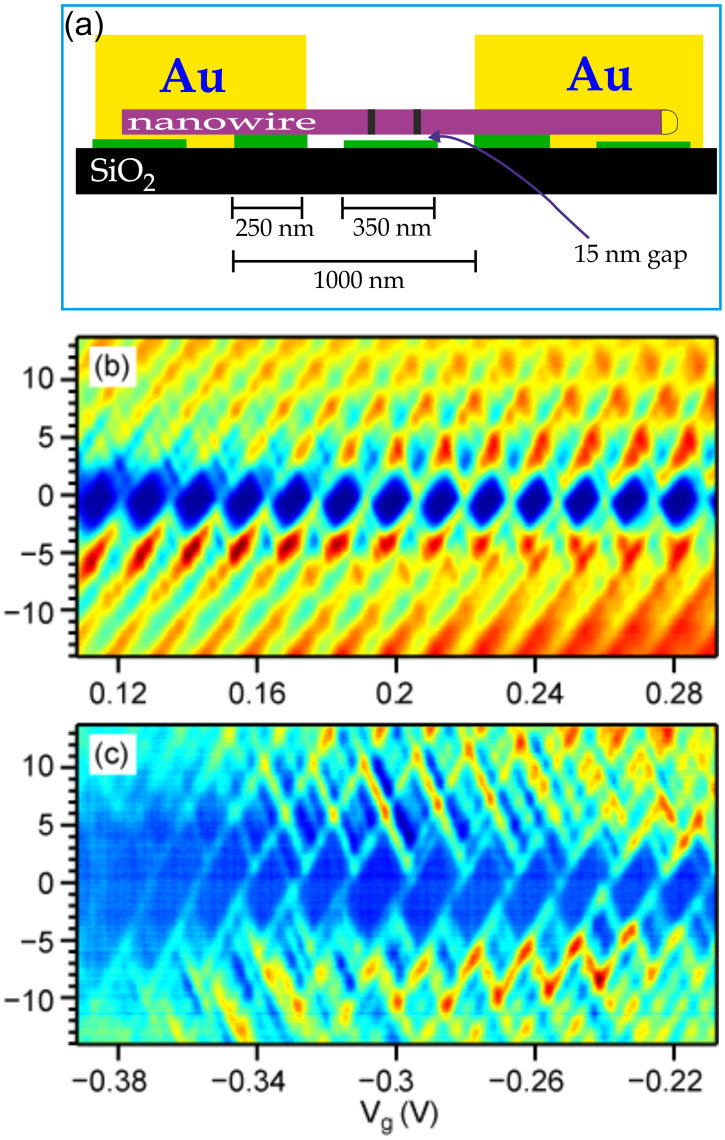

Figure 6.2: (a) A schematic diagram for a suspended nanowire heterostructure device with a nearby local gate. (b) The stability diagram for the high-resistance nanowire at a temperature of 1.5 K. A carrier signal, at the resonance frequency $f_c = 499$ MHz, is launched to a tank circuit terminated by the nanowire heterostructure. The reflected signal is amplitude modulated by the resistance state of the SET, which in turn is a function of gate and source drain voltage. The reflected signal is demodulated by a homodyne mixing and the amplitude of the signal at the base band displays Coulomb-blockade diamonds. c) The stability diagram at negative voltages. The Coulomb-blockade diamonds have sharp edges consistent with the n-type nature of the nanowires.

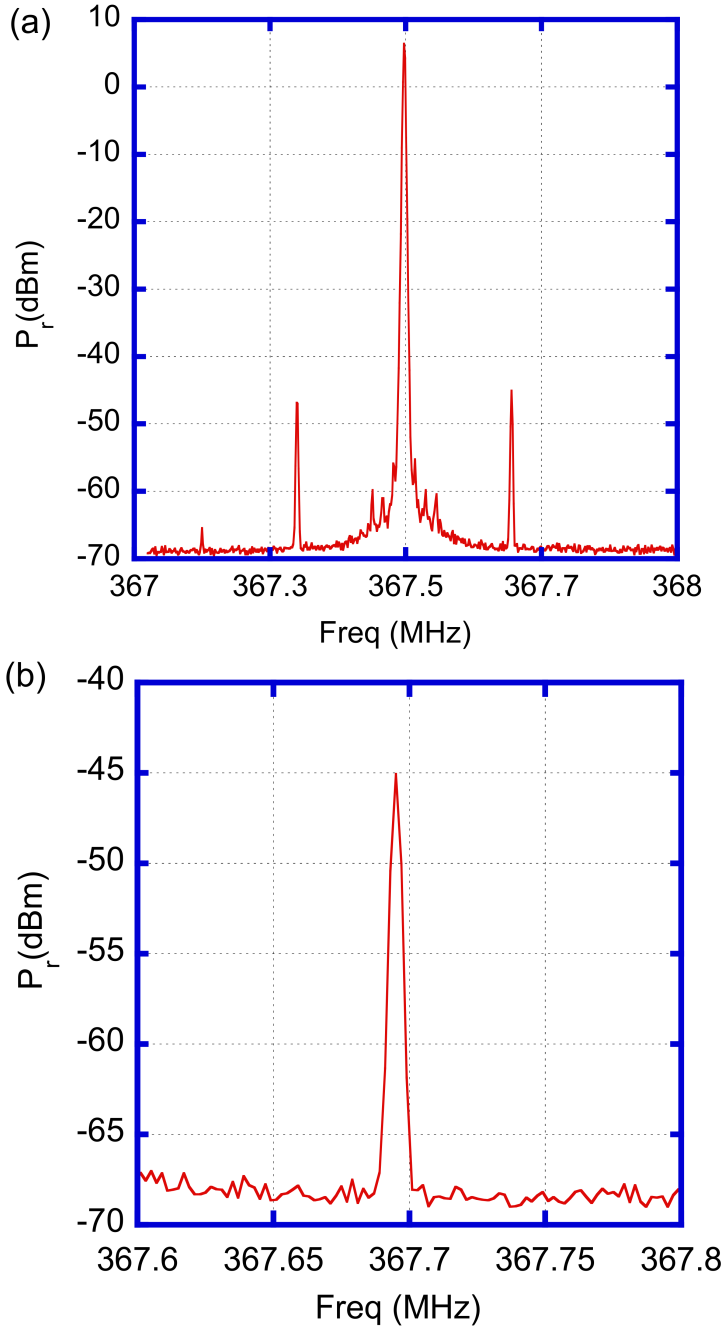

Figure 6.3: (a) The power spectrum of the reflected signal. The carrier frequency, 367.5 MHz is amplitude modulated by a small charge signal applied on the gate voltage. The signal has a charge amplitude $\Delta q_{rms} = 2.9\,\text{me}$ at a frequency of $f_g = 200\,\text{kHz}$. The amplitude modulated reflected signal appears with two side bands in a spectrum analyzer. (b) The side band at a frequency $f_c + f_g = 367.7\,\text{MHz}$. The power in the side band compared to the noise floor, or the signal to noise ratio SNR$= 23.4\,\text{dB}$.

sensitivity δq can be estimated from the expression in eq. 3.3:

$$\delta q = \frac{\Delta q_{rms}}{\sqrt{2\mathrm{RBW}}10^{\frac{SNR}{20}}} = 2.5\,\mu e/\sqrt{\mathrm{Hz}} \tag{6.1}$$

A resolution bandwidth of RBW=3 kHz has been used during the detection with the spectrum analyzer. The signal to noise ratio SNR$= 23.4$ dB is taken from the upper side band peak shown in the Fig. 6.3b. The measured charge-sensitivity is close to the best values reported in conventional Aluminum based SET.[27]

6.2.3 Low frequency noise properties

Theoretically, the charge sensitivity of the Al-based SET is fundamentally limited by the shot noise arising from the sequential tunneling of the electrons. Practically, it is limited by 1/f noise at low frequencies and by the amplifier noise at high frequency. We used the highly sensitive RF-SET to investigate the low frequency noise properties of the nanowire SETs. One would naively think that if the noise sources are in the substrate, the suspended nanowires would have a lower noise than other SETs. The measurement is acquired with the setup sketched in Fig. 3.9.

As can be seen in Fig. 6.3, the reflected carrier signal is not a sharp peak (or a delta function) but is broadened by the random fluctuations at low-frequencies (noise). Therefore, the technique to measure the low-frequency noise properties of the SETs is to down-convert the reflected signal with homodyne mixing at a fixed frequency. The resulting charge-noise spectral density is displayed in Fig. 6.4. The two spectra are taken at two different gate voltages corresponding to low and high charge sensitivity of the device. This serves to separate the noise contribution from the amplifier and the SET. The pronounced peak in the middle of the spectral density is a pilot signal applied on the gate. It has a charge amplitude of $5.9\,\mathrm{m}e_{rms}$ and a frequency of 2.94 kHz. The signal is used to calibrate the measured noise in terms of charge noise.

When the SET is biased in the stable Coulomb blockade state, a random fluctuation of small charge has no considerable effect on the differential conductance of the SET. Therefore, at this low charge sensitive state of the SET, the spectral noise (shown in red/circle) is dominated by the amplifier noise and the phase noise of the rf-source. However, when the SET is biased at the steep slope of the transfer function, the SET is sensitive to small charge fluctuations. Hence, the spectral noise includes both contributions from charge noise in the SET and the amplifier/rf-source noise. This highly sensitive state is shown in blue (rectangles) in Fig. 6.4. Therefore, the contribution of the SET to total charge noise can be extracted by subtracting the amplifier-noise from the charge-noise in the high sensitive regime. The result is presented in green (cross) color. Here we have neglected the small variation of the amplifier noise with SET resistance.

The SET amplitude noise shows approximately a $1/\sqrt{f}$ noise (in units of $e/\sqrt{\mathrm{Hz}}$) dependence at low frequencies as it is compared with the reference $1/\sqrt{f}$ noise(dashed) line. However the SET noise deviates from the $1/\sqrt{f}$ noise at higher

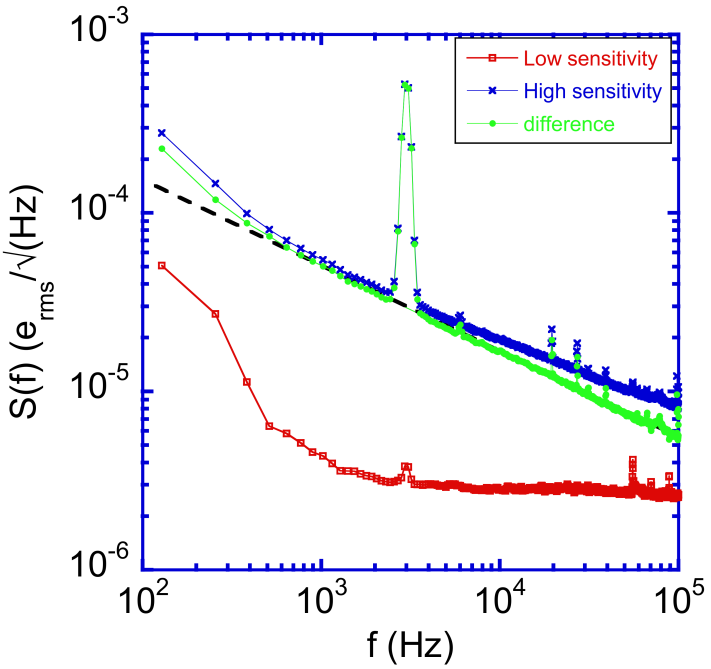

Figure 6.4: a) The charge-noise power spectral density of the reflected signal at 1.5 K. The low frequency noise components of the reflected signal are measured by down converting the reflected signal with the homodyne mixing. These measurements are performed at low (red) and high (blue) charge sensitivity states of the nanowire SET. The noise at the low-charge sensitivity is dominated by the amplifier noise whereas the noise at the high-charge sensitivity comes from both the SET and the amplifier. The difference of the two states (green) gives the charge-noise power spectral density of the SET. The noise spectral density of the SET displays a $1/f^{1/2}$ behavior, indicated by the dashed power fit line(black). A pilot charge signal is applied on the gate to calibrate the noise in charge units. It has a charge amplitude of $5.9\,\mathrm{me}_{rms}$ at a frequency of 2.94 kHz.

frequencies. The level of the low frequency noise is extrapolated to 300 $\mu e_{rms} Hz^{-1/2}$ at 10 Hz. The suspended configuration of the SET, physically separated from the substrate, was hoped to have lower $1/f$ noise. However, the measurement shows this was not the case.

Chapter 7

Conclusion and outlook

In this thesis, we have investigated charge transport and noise properties of InAs nanowires connected by superconducting electrodes using both dc- and rf-readout techniques.

We fabricated a large number of non-suspended and suspended devices with different lengths, ranging from long to short and from diffusive to quasi-ballistic. We systematically investigated proximity effect induced in the nanowires at different temperatures and magnetic fields. We measured relevant features of the current-voltage characteristics: Josephson critical current, excess current, and sub-gap current, and compared them with theory. In the shortest length device, which had very good contact-interfaces, we have observed a record high value of Josephson critical current, 800 nA, which is close to the theoretical limit and an order of magnitude higher than what has been reported elsewhere.

In gate-controlled suspended devices of short length and with very good interface quality, we observed stepwise decrease of both conductance and critical current before the conductance vanishes completely. In somewhat longer devices, we observed cross over from a distinct S-normal metal-S (SNS) type behavior with large positive excess-current and enhanced sub-gap conductance to tunneling S-insulator-S (SIS) type with negative excess current and suppressed sub-gap conductance.

We demonstrated also a radio-frequency single electron transistor based on InAs/InP nanowire heterostructures. Operating in the rf-mode at 350 MHz, we achieved a very high charge sensitivity of $2.5\,\mu e/\sqrt{\mathrm{Hz}}$, comparable to the best conventional Al-SETs. The low-frequency noise was also characterized. It showed approximately a $1/f$ behavior and was of the same magnitude as in Al-SETs.

Recently, we measured shot noise in suspended devices. The preliminary data shows a noise spectral density in the sub-gap region which depends on the voltage. The data also shows steps correlated with the conductance steps as a function of the voltage. However, more analysis of this is needed.

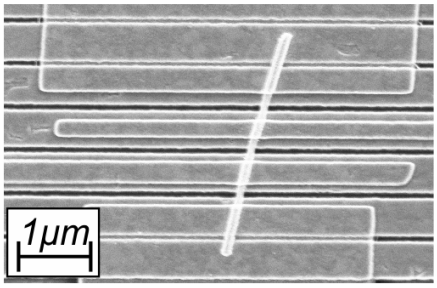

Figure 7.1: (a) SEM image of a nanowire connected by YBCO nano-stripes.

Future work

There is a variety of interesting phenomena that can be studied in the nanowire superconducting hybrid devices given the reproducible fabrication processes and advanced measurement techniques.

i) Recently, the nanowire hybrid devices have attracted new attention following the prediction of Majorana bound states, in condensed matter.[82, 83, 84] A Majorana fermions, is a fermion that is its own antiparticle. It has been suggested that devices that support Majorana bound states could be fundamental building blocks for a future quantum computer because the Majorana particles are stable against external influences. The on-going experimental studies are at the early stages and the reported findings are based on dc-measurements. I see that there is great advantage in using the rf-mode to detect and understand Majorana bound states. The rf-mode will have a better signal to noise ratio (better sensitivity) since it works at higher frequency which is well above the 1/f noise corner.

ii) By implementing the wet-etching recipe described in section 3.1.2 for a longer time, after the suspended samples are ready, it is possible to form a quantum point-contact like constriction just above the gate. This has another the advantage that one can start with a thicker nanowire, which gives better contacts, and one can still study very narrow wires. I had prepared a few samples, if possible, they will be measured.

iii) Another possible future work is to couple nanowires with YBCO-nanowire stripes. This will be to investigate proximity induced superconductivity in nanowires. The fabrication is challenging, but it may give information about the High T_c superconductors. A SEM image of a nanowire connected by YBCO is shown in Fig. 7.1

Appendix A

A.1 Symbols and abbreviations

Natural constants	
e	Electron charge
h, $\hbar$	Plank constant, Reduced Plank constant ($h/2\pi$)
k_B	Boltzmann constant
G_0	Conductance quantum
R_q	Resistance quantum
Symbols	
Transport:	
T	Temperature
m, m^*	Free electron mass, Effective electron mass
N, T'	Number of channels, Transmission probability
E, P, k	Energy, Momentum, Momentum number
$f(E)$	Fermi-distribution function
λ_F, v_F, k_F	Fermi-wavelength, Fermi-velocity, Fermi-wavevector
μ, E_F	Electrochemical potential, Fermi-energy
Ψ	Wave-function
Δ	Superconducting energy-gap
E_{CB}	Conduction band
$D, D(E)$	Diffusion constant, Density of states
n_s	Equilibrium charge density
τ_D	Depahsing time
ϕ	Phase difference
l_e	Elastic scattering length
ξ	Coherence length
ξ_0	Coherence length in ballistic nanowire
ξ_D	Coherence length in diffusive nanowire
L	Length
l_i, l_ϕ	Inelastic scattering length , Phase coherence length
A	Andreev reflection probability
B	Normal reflection probability

I, R, G	Current, Resistance, Conductance
G_{NN}, G_{SG}	Normal conductance, Sub-gap conductance
I_c,	Critical current, Normal resistance
I_{exc}	Excess current
V, V_g	Source-drain voltage, Gate voltage
R_b	Bias resistor
γ	Coupling strength

Single electron transistor:

f	Frequency
ω	Angular frequency
f_0, Ω_0	Resonance frequency, Resonance angular frequency
ω_c, ω_g	Angular frequency of carrier signal , Angular frequency of gate signal
C, C_g, C_Σ	Capacitance, Gate capacitance, Total capacitance
E_c	Charging energy
L_T	Inductance of tank circuit
C_T	Capacitance of tank circuit
Z	Impedance
Z_{LC}	Impedance of an LC-tank circuit at f_0
Q_T, Q_i, Q_e	Quality factor, Internal quality factor, External quality factor
Z_0	Characteristics impedance of $50\,\Omega$ line
Γ	Amplitude reflection coefficient
P_r, P_{in}	Reflected Power, Power in
Δf	Bandwidth
q, q^*	Charge, Effective charge
δq	Charge sensitivity
Δq_{rms}	Small charge signal
S	Noise spectral density
F	Fano factor
Al, Au	Aluminum, Gold
InAs, InP	Indium Arsenide, Indium Phosphide
E-beam	Electron beam

Abbreviations

CP	Cooper pairs
S, N/NW	Superconductor, Normal/Nanowire
SNS	Superconductor-nanowire/normal-superconductor
SIS	Superconductor-insulator-superconductor
MAR	Multiple Andreev reflection
IVC	Current-voltage characteristics
1D, 2D, 3D	One, Two, Three dimensional
HEMT	High electron mobility transistor
CBE	Chemical beam epitaxy
dc	Direct current
ac	Alternating current
rf	Radio frequency
LO	Local oscillator
SLP, BPF, PF	Low pass filter, Band pass filter, powder filter
att.	Attenuator
SEM	Scanning electron microscope
TEM	Transmission electron microscope
RHEED	Reflective high energy electron diffraction
SET	Single electron transistor
SNR	Signal to Noise ratio
RF-SET	Radio frequency single electron transistor
MXC	Mixing chamber

Appendix B

B.2 Fabrication Recipe

Here, I present in detail fabrication steps for both types of devices. The first sub-section is defining relatively large-scale structures, the contact pads and position marks, by large-scale electron beam lithography. The second and third subsections will be on connecting nanowires with superconducting contacts for non-suspended and suspended devices, respectively.

B.2.1 Contact pads and cross markers

In fabrication of the nanowire devices, a vertically grown nanowires are removed from the growth substrate and transfered to another substrate. After that, the wires are connected with superconducting contacts preferably separated by a very short length. In addition, the suspended devices are fabricated in several e-beam layers each with no tolerance for rotation. This requires high resolution of e-beam lithography which requires perfect chip marks with very small mis-alignments. The following is the fabrication recipe for detection marks and bonding pads.

1. 2" inch standard Si-wafer was capped by 400 nm thick thermally grown SiO_2. Clean the wafer with hot acetone, hot Shipley remover (611), rinse in IPA and dry it by N_2 gas. Strip in oxygen plasma for 1 min at 100 W.
2. Spin-coat e-beam resist: Spin-coat HDMS premier for sticking purpose, 3000rpm for 20 s. Spin-coat LOR 3A at 3000rpm for 1 min. Bake at 175°C for 5 min. Spin-coat UV5 0.8 at 3000rpm for 1 min. Bake at 130°C for 2 min.
3. Expose with EBX 9300, dose 25μC/cm^2, 100 kV, 70 nA current and aperture 8. There is no need for proximity correction.
4. Post exposure bake at 130°C for 1.5 min. Develop in MF24A for 1.5 min to transfer the pattern to the resist. Ashing in oxygen plasma, 50 W for 30 s, to remove any residual resist.
5. Deposit metals Ti/Au/Pd (5/90/5 nm thick) in vacuum. Evaporation is done by e-beam heating the source targets.
6. Lift-off either in an aceton overnight or in hot Shipley remover(611), 75°C for 12 min. Clean in Ultrasonic bath, IPA, water, brief ashing in oxygen plasma. Spin-coat the wafer with a protection resist. This kinds of wafer are further processed for both non-suspended and suspended device.

B.2.2 Non-suspended devices

These type of devices are nanowires just lying on top of the Si-SiO_2 substrate connected by two or more superconducting contacts. The contact electrodes are defined either by a single-step e-beam lithography or a double lift-off process. On both ways, we used two e-beam resist layers, Copolymer and ZEP. While the top layer, ZEP, provides a very high resolution and contrast, the bottom layer, copolymer provides an undercut for better lift-off. The thickness of each e-beam layer varies depending on the intended final thickness of the electrodes on the nanowires. Here follows a recipe for a typical non-suspended device.

1. Dice the already pattern wafer into 7×7 cm chips. Remove the protection resist cover in hot aceton. Clean thoroughly the selected chips for fabricating the non-suspended devices.
2. Mechanically transfer InAs nanowires from the growth substrate to an already patterned chips. This is done by gently wiping a sharp piece of paper locally on the growth substrate followed by gently dropping them on the chips. Blow dry N_2 gas to clean dirty materials deposited unintentionally along the nanowire transferring process.
3. Scanning electron microscope images are taken to locate the relative positions of possibly good nanowires with respect to the pre-defined marks (coordinates). The SEM images are used to draw Auto CAD files to be patterned on selected nanowires by e-beam lithography.
4. Spin-coat a bottom layer, Copolymer EL6 (6 % solid in Ethyl Lactate solvent) at 2000rpm for 1 min. Bake 170°C for 3.5 min. Spin-coat a top layer, ZEP520 in 1:1 Anisole (0.8 % solid in Anisole solvent) at 6000rpm for 1 min. Bake 170°C for 2 min.
5. Expose with EBX 9300, dose 360 μC/cm^2, 100 kV, 2 nA current and aperture 6. For a double lift-process, there should be extra effort in getting the lowest possible rotation in the optical alignment.
6. Develop the top layer ZEP520 in O-Xylene for 1 min. Rinse in IPA and blow dry N_2 gas. Develop the bottom Copolymer resist in MIBK:IPA (1:1) for 2 min. Rinse in IPA and blow dry N_2 gas. Ash for residual resist in oxygen plasma, at 50 W for 10 s.
7. Etching the native oxide and cleaning impurities on the surface of the nanowires with an ammonium ploysulfide solution. The stock solution is prepared by mixing a commercially available ammonium sulfide with a pure sulfur. The stock solution is diluted 10 times in water prior to etching the nanowires at 40°C for 2.5 mints.
8. Immediately after the brief etching of the nanowires, run to the evaporator, load the sample and pump it to vacuum. Deposit superconducting Ti/Al (5/150 nm thick) contacts in vacuum. This is done by e-beam heating of the source targets.
9. Lift-off in hot Shipley remover at 75°C for 12 min. Rinse in IPA and blow dry N_2 gas.
10. The ready sample is store in vacuum to prevent degradation of the interface transparency and also to de-sorb some impurities on the surface of the nanowires. Sometimes, I dare to briefly look at the final devices with SEM.

B.2.3 Suspended devices

These types of devices are nanowires suspended just above a local gate electrode. The nanowires rest on interdigitated metal stripes with 15 nm thickness difference between every two adjacent stripes. These interdigitated metals are defined in a two step e-beam lithography. First, arrays of thinner-gate electrodes are defined intentionally at large distances so that the thicker-bias electrodes get rooms to be placed in between them. Since the nanowires rest on the thicker electrodes, the distance between the thicker-bias electrodes determines the minimum device length, which has been varied from 100 nm to 300 nm. Similar to the non-suspended devices, e-beam lithography has been done using two e-beam resist layers, Copolymer and ZEP520. Here follows the common recipes for a typical suspended device:

Gate-stripes

The thinner-gate electrodes are 50 nm thick and 11μm long. The gate-width varies from 30 to 100 nm depending on the intended device.

1. Remove the protective resist on a patterned wafer (with bonding pads and cross marks) in hot aceton. Clean thoroughly the wafer in DI water, and IPA. Brief ash in oxygen plasma.
2. Spin-coat a bottom layer, Copolymer EL6 (6 % solid in Ethyl Lactate solvent) at 6000rpm for 1 min. Bake 170°C for 3.5 min. Spin-coat a top layer, ZEP520 in 1:1 Anisole (0.8 % solid in Anisole solvent) at 6000rpm for 1 min. Bake 170°C for 2 min.
3. Expose with EBX 9300, dose 360 μC/cm^2, at 100 kV, 2 nA current and aperture 6. There is no tolerance for small rotation and misplacements.
4. Develop the top layer ZEP520 in O-Xylene for 1 min. Rinse in IPA and blow dry N_2 gas. Develop the bottom Copolymer resist in MIBK:IPA (1:1) for 1 min. Rinse in IPA and blow dry N_2 gas. Get ride-off any residual resist by ashing in Oxygen plasma, at 50 W for 10 s.
5. Deposit metals Ti/Au/Pd (5/40/5 nm thick) in vacuum.
6. Lift-off in hot Shipley remover at 75°C for 12 min. If there is time, It is recommended to do the Lift-off in acetone over long time (up to three days) gives very clean structures with no any left-overs in between the stripes. Clean thoroughly in hot aceton, water, IPA, briefly ash in Oxygen plasma.
7. Look at the fine structures with SEM images before further process.

Bias-stripes

The thicker-bias electrodes are 65 nm thick and 9μm long, leaving the gate electrodes thinner by 15 nm but longer by a μm on each side. The bias-width varies between 100 to 150 nm depending on the intended device.

1. The bias-metal stripes are fabricated in between the already made gate-stripes following the same recipe as the gate stripes except their thicker thickness, Ti/Au/Pd (5/55/5 nm thick).

2. Spin-coat a protective resist and dice the wafer into 7×7 cm chips. These chips are ready for further process, placing nanowires on top of the interdigitated stripes and connecting them with electrodes.

Contacting the nanowires

At this step, nanowires are transfered onto the interdigitated stripes possibly rested on the thicker electrodes and suspended above the thinner-gate stripes. The well placed nanowires are interfaced by superconducting electrodes. At the same time, the gate-electrode underneath the nanowire is also connected to one of the bonding pads. Here is presented fabrication recipes for connecting the nanowires by electrodes.

1. Remove the protective resist and thoroughly clean the already patterned chips in aceton, DI water, IPA.
2. Transfer InAs nanowires from the growth substrate to the already patterned Si-SiO_2 chips. Blow dry N_2 gas to clean any paper pieces and dirty materials deposited unintentionally along the nanowire transferring process.
3. Scanning electron microscope images are taken to locate the relative positions of nanowires on the interdigitated metal stripes. The SEM images are also used to select well placed nanowires. The extracted positions are used to prepare e-beam (Auto CAD) files for e-beam lithography.
4. Spin-coat a bottom layer, copolymer EL6 (6 % solid in Ethyl Lactate solvent) at 2000rpm for 1 min. Bake 170°C for 3 min. Spin-coat a top layer, ZEP520 in 1:1 Anisole (0.8 % solid in Anisole solvent) at 6000rpm for 1 min. Bake 170°C for 2.5 min.
5. Expose with EBX 9300, dose 360 μC/cm^2, 100 kV, 2 nA current and aperture 6. Good optical alignment is crucial.
6. Develop the top layer ZEP520 in O-Xylene for 1 min. Rinse in IPA and blow dry N_2 gas. Develop the bottom Copolymer resist in MIBK:IPA (1:1) for 1 min. Rinse in IPA and blow dry N_2 gas. Ash for residual resist in oxygen plasma, at 50 W for 10 s.
7. Etch the native oxide with an ammonium ploysulfide solution at 40°C for 2.5 mints. The sulfur also passivates the dangling bonds on the surface the nanowires.
8. Immediately after the brief etching, run to the evaporator, load the sample and pump it to vacuum. This often takes less than a minute, from the time of etching process to reaching a low vacuum (5e-7).
9. Deposit superconducting Ti/Al (5/150 nm thick) contacts in vacuum. This is done by e-beam heating of the source targets.
10. Lift-off in hot Shipley remover at 75°C for 12 min. Rinse in IPA and blow dry N_2 gas.
11. Before low temperature measurements, the ready sample is store in vacuum to prevent degradation of the interface transparency. The vacuum also help to de-sorb some impurities on the surface of the nanowires thereby decreases the resistance of the devices .

Acknowledgements

Foremost, I would like to express my deepest gratitude to my supervisor Per Delsing, for his continuous guidance, advice and genuine care. It has been privilege working with you and I appreciate all your contributions, wisdom, and constructive discussions. Thank you for patiently reading my thesis and our papers.

Many thanks to my assistant supervisor Vitaly Shumeiko for his commitment, passion and advice. My appreciation goes to Henrik Nilsson for sharing his impressive scientific skills and experience in nanowires. I benefited a lot from closely working with Fan Wu and Jonas Bylander. Daniel Persson and Mikael Fogelström, thank you for theoretical contributions and hard work on our papers. Thanks to Chris Wilson, Hongqi Xu, and Lars Samuelson for your time and contributions. The thesis will not have exist without the nanowires grown at Lund University, and for this, I would like to thank again Hongqi Xu and Lars Samuelson. I express my appreciation to Thilo Bauch, Floriana Lombardi, and Reza Baghdadi for positive discussions and collaboration.

Thanks to Sergay Kafanov for getting me started in the clean room. I have enjoyed working with Arsalan Pourkabirian in Mr. Freeze.

I am grateful to my previous and current colleagues: Tauno Palomaki, Martin Sandberg, Arseniy Lartsev, Marco Arzeo, Martin Gustafsson, Io Chun Hoi, Philip Krantz, Kyle Sundqvist, Saroj Prasad Dash, Venkata Kamalakar, Sophie Charpentier, André Dankert, Sumedh Mahashabde, Michaël Simoen, Sebastian de Graaf, Seckin Kintas, Gunta Kunakova, Omid Habibpour, Matthias Staudt, Ida-Maria Svensson, Thomas Yager, Thomas Aref, Astghik Adamyan, Maria Ekström and all the others in the group.
Thanks to Jan Jacobsson, Stafan Pehrson, Lars Jönsson, Ann-Marie Frykestig, Marie Fredriksson, Susannah Carlsson, and to all staff members of the nanofabrication laboratory, especially Henrik Frederiksen, Bengt Nilsson and Kaija Matikainen.

I would like to thank Tsadkan, Simon and Lucas, for being family. Thanks to my childhood friend Haileselassie Medhin, his wife Elisabeth and little Zema. My sincere thanks go to my best friends Meweal and Mikeal, Yeshi's, Elias's, and Roman's family. I would like to appreciate Sanna Henningsson, Bea Granberg, Raneesh Sadanandan, and Girmay Gebrekidan for being so nice and caring.

Massive credit goes to my mama Letebrihan Beyene, for endless care and love. Thanks to my family at home and abroad for all care and support.

Above all, special thanks to my dearest wife Elsa Kassa. "Nehatey", your tolerance and smile have been magnificent. I am blessed to have you in my life. My lovely son Jacob, I am so proud of you.

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