Feasibility Issues of using Three-Phase Multilevel Converter based Cell Balancer in Battery Management System for xEVs

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Abstract:
The use of a three-phase (3-ϕ) multilevel converter (MLC) as an integrated cell balancer and motor driver is investigated for 3-ϕ AC applications in EVs/HEVs/PHEVs. The paper analyzed an issue of additional battery losses caused by the flow of reactive and/or harmonic power from each power cell of the 3-ϕ MLC battery system. The paper also investigates the size of shunt capacitor required for compensation of the losses to acceptable level. This study concludes that the size of the required capacitor is too big for the vehicle application unless some other active compensation is used as well. Another practical way to employ the MLC as a cell balancer is to use it in a cascaded connection with the conventional 3-ϕ two-level voltage source inverter however it may not be a cost-effective solution either due to high component count.

Keywords: Hybrid electric vehicles, Batteries, Cell balancing, Three-phase multi-level converter, Reactive power and dc-link current ripple issues, DC-link capacitor sizing.

1. INTRODUCTION

The battery pack in Hybrids (HEVs) and Electric Vehicles (EVs) is built from a large number of small cells connected in series and parallel to meet both the traction power demand and electric range requirement. The Depth-of-Discharge, see Kuhn et al. (2005), and the cell temperature, see Park and Jaura (2003), are the two most important factors that determine the degradation of the battery cells. Hotter cells degrade more quickly than colder cells. Therefore, even a few overheated cells may result in shortening the lifetime of the whole battery pack. Hence, the battery management system should ideally be able to both balance the state-of-charge (SoC) of the cells and keep the temperature differences between the cells less than 5°C with a maximum temperature below 40°C, see Park and Jaura (2003). With the purpose of transfering charge from cells having higher SoC to cells having lower SoC, there are several active and passive cell balancing schemes based on various topologies of switched capacitive and resistive circuits, see for example Lee et al. (2011), and Krein (2007).

In recent years cascaded MLCs, see Rodriguez et al. (2009), have been discussed for the drive of the electric motor in HEVs, see Tolbert et al. (1999) and Josefsson et al. (2010). The MLC consists of n cascaded H-bridges (HBs) with an isolated battery cell for each HB. The combination of an HB and a battery cell is here called a Power Cell (PC). The MLC, other than reducing the total harmonic distortion in the generated waveform for the electric machine, also offers an additional advantage of extra degree-of-freedom (DoF) to generate the load voltages. In most of these motor drive applications of the MLCs, the usual strategy is to use a phase shifted pulse width modulation technique to achieve the uniform use of cascaded cells, see Rodriguez et al. (2009).

In Altaf et al. (2012) the MLC is proposed as both a cell balancer and a drive for EV/HEV/PHEVs (xEVs) equipped with DC electric motors. The extra DoF of the MLC is used to achieve simultaneous thermal and SoC balancing among the battery cells. However, in almost all xEVs, a 3-ϕ AC machine is used to power the wheels. Therefore, in Wilkie et al. (2008) it is proposed to use the MLC as a cell balancer for the 3-ϕ application. In the proposed configuration, the single-phase MLC is used as a dedicated cell balancer in the battery pack and is integrated with 3-ϕ TLI (Two-Level (voltage source) Inverter) in a way such that the dc-link of 3-ϕ TLI is supplied by the cascaded MLC. This configuration works very well as a cell balancer but the component cost is likely too high. This would partly be alleviated by using the 3-ϕ MLC to directly drive the 3-ϕ AC machine as proposed by Josefsson et al. (2010).

This paper investigates the configuration proposed in Josefsson et al. (2010), studying the practical consequences for the battery cells when using the 3-ϕ MLC to directly drive the 3-ϕ AC machine. The paper investigates in detail the reactive/harmonic power flow which leads to a high level dc-link ripple current causing significant additional ohmic losses in batteries. The extra losses increase the operating temperature which accelerates the capacity fading of batteries, see I. Bloom et al. (2001).

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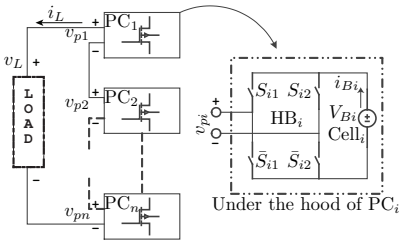


Fig. 1. Block diagram of a single phase cascaded HB MLC.

The main contributions of the current article are as follows: Issues of using 3-ϕ MLC as an integrated cell balancer and motor drive are thoroughly studied and analyzed; in order to characterize the losses and the size of compensating capacitor, the dc-link current is accurately computed using double Fourier series approach, see McGrath and Holmes (2009),Holmes and Lipo (2003), and Black (1953); the additional battery losses due to dc-link current ripple are computed and analyzed and the size of shunt-capacitor needed for the passive compensation is evaluated under normal operating conditions; and the results are compared to the case of 3-ϕ TLI.

The paper is organized as follows. Section 2 gives an overview of the basic function of single-phase MLC for DC loads. The problem description and the underlying assumptions for the analysis are given in section 3. The dc-link current is computed based on double Fourier series approach in section 4. The capacitor sizing based on computed dc-link ripple current is done in section 5 and then the additional battery losses due to dc-link ripple current are computed in section 6. Finally the conclusions are drawn in Section 7.

2. MULTI-LEVEL CONVERTERS

In this section, the single-phase MLC for a DC load is reviewed. In contrast to two-level converters, consisting of a single large battery pack connected with a single HB, the MLC consists of many series connected PCs where each PC contains an HB and the independent battery cell as shown in Figure 1. The HB is a switch mode dc-dc power converter, see Mohan et al. (2003), that produces a four-quadrant controllable dc output using four switches S_{i1} , S_{i2} , $\bar{S}_{i1}$, $\bar{S}_{i2}$ as shown in Figure 1. Therefore, depending on which switch pair is turned-on, three modes of operation can be defined for each PC$_i$. In *Mode–1* $v_{pi} > 0$, in *Mode–2* $v_{pi} < 0$ and in *Mode–3* $v_{pi} = 0$. To model these three modes of operation, let's define $s_{ij}(t) = 1$ for ON-State and $s_{ij}(t) = 0$ for OFF-State of switch S_{ij} where 'i' corresponds to PC$_i$ and $j \in \{1, 2\}$. Now the switching function $s_i(t)$ for a PC$_i$ (or Cell$_i$) can be defined by $s_i(t) = (s_{i1}(t) - s_{i2}(t)) \in \{1, -1, 0\}$ corresponding to *Mode–1*, *Mode–2* and *Mode–3* respectively. Thus all three modes of HB can be defined in terms of $s_i(t)$. The switching vector $s(t) = [s_1(t)\ s_2(t)\ \cdots\ s_n(t)]^T$ contains switching functions for all n PCs inside the MLC. Assuming the ideal switch behavior, the ohmic and switching losses can be ignored and, therefore, the input and output of HB, as shown in Figure 1, are related through the switching function $s_i(t)$. Thus, the current through Cell$_i$ is given by:

$$i_{Bi}(t) = s_i(t) i_L(t) \tag{1}$$

where $i_L(t)$ is the load current. Note that due to the series connection, the same current i_L passes through each PC. However, the direction of current passing through the battery Cell$_i$ depends both on the selection of switches and the direction of load current i_L. Similarly the voltage output from each PC$_i$ is defined by $v_{pi}(t) = V_{Bi}(t) s_i(t)$ and hence the total voltage output from the MLC is given by $v_L = \sum_{i=1}^{n} v_{pi} = \sum_{i=1}^{n} V_{Bi}(t)\, s_i(t)$ with the MLC being able to generate $L = 2\,n + 1$ different voltage levels (v_L).

The MLC allows to independently switch ON/OFF each battery cell in a battery pack . This extra DoF opens up many intriguing control research problems which can be studied for various applications. In Altaf et al. (2012), the potential benefit of cell balancing using extra extra DoF of single-phase MLC has been evaluated for DC loads by formulating it as a constrained convex optimization problem. The results show that the optimal control policy, exploiting the full DoF of MLC, gives significant benefit in terms of reduction in temperature and SoC deviations, especially under parameter variations, compared to uniformly using all the cells.

Table 1. Nomenclature and List of Symbols

Symbols	Definition
n, PC$_i$	Number of Power Cells, Power Cell i
F_p, ESR	Power Factor, Effective Series Resistance
$s_i(t)$	Switching function of PC$_i$
$v_x(t)$	Instant. voltage of phase x where $x = a, b,$ or c
$i_x(t)$	Instant. current in phase $x = a, b,$ or c
θ	Phase angle between $v_x(t)$ and $i_x(t)$ in phase x
ω_o	Fundamental frequency of output AC variables
ω_m	Mechanical (angular) speed of AC machine
n_p	Number of pole pairs in AC machine: $n_p = \omega_o/\omega_m$
ω_s/ω_c	Switching/Carrier frequency where $\omega_s = \omega_c$
V_r	Amplitude of reference modulating signal in PWM
V_c	Amplitude of carrier signal in PWM
M_o	Modulation Index in PWM: $M_o = V_r/V_c$

3. PROBLEM DESCRIPTION

The 3-ϕ MLC driving 3-ϕ balanced load is shown in Figure 2 for case of $n = 2$. It has been noted that, for the case of 3-ϕ AC machine, which acts as inductive load with lagging power factor, the 3-ϕ MLC has to supply the bidirectional fluctuating power from each PC. Though one of the major components of this fluctuating power from each PC is the reactive power whose magnitude largely depends on the power factor angle θ however there is a large contributions due to switching harmonics as well. In particular, the flow of reactive power and the switching action generates a large dc-link (i.e. DC input side of the HB) ripple current at 2nd order baseband harmonic frequency. Ideally, to minimize losses, a constant dc current should flow through the battery cell. However, the battery cells in the MLC are cascaded in series and connected across dc-link in each phase. Thus, in the absence of compensation, the battery cells at each dc-link get exposed to this very high ripple current which incurs significant additional losses on the battery cells and thus increases the battery temperature. The battery operation at elevated temperature has detrimental effect on the battery lifetime and therefore the large ripple current needs to be compensated by using a dc-link capacitor

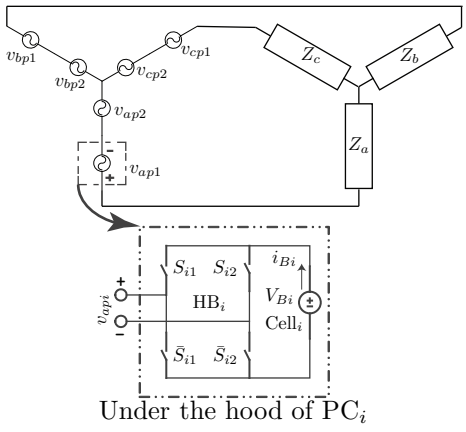


Fig. 2. 3-ϕ MLC for $n = 2$.

in parallel with battery. In contrast to 3-ϕ MLC, the balanced 3-ϕ TLI provides almost constant power under ideal conditions, see Rashid (2010), Mohan et al. (2003). Though the reactive power also flows in 3-ϕ TLI, the batteries do not see this reactive power by virtue of the topology and the symmetrical fast switching in three legs. Under ideal conditions almost all the reactive power instantaneously shuffles between three phases and hence never flows back to the battery pack. Thus, compared to 3-ϕ TLI, the 3-ϕ MLC, as an integrated cell balancer and motor driver, faces some serious issues which need to be carefully analyzed to check its feasibility for xEVs.

3.1 Assumptions:

The following assumptions are outlined here which will be employed later to calculate the dc-link current harmonics:

Assumption 1. Distortion is present only in voltage whereas the output load current in all phases is assumed perfectly sinusoidal with frequency ω_o and power factor angle θ i.e.

$$i_a(t) = \sqrt{2} I_a \cos(\omega_o t + \theta) \tag{2}$$

Assumption 2. Three-phase source (3-ϕ MLC or 3-ϕ TLI) is balanced i.e. all three phases have same rms voltage V and frequency ω_o. Moreover three phases are symmetrical i.e. they are shifted exactly by 120° w.r.t. each other and 3-ϕ source has counterclockwise rotating positive-sequence of phases a, b, and c, see Glover et al. (2008).

Assumption 3. Inverters are driving 3-ϕ balanced inductive load i.e. all three loads connected in Y or Δ configuration have same impedance. It implies that there is no asymmetrical current flowing in the 3-ϕ circuit and thus all phase currents are equal i.e. $I_a = I_b = I_c$.

Assumption 4. The switching (or carrier) frequency f_s is infinite. Under this assumption, all the carrier harmonics and their sidebands can be easily filtered, using a very small capacitor, and thus can be neglected. See section 5.

Assumption 5. We assume Thevenin model for the battery Cell$_i$ with internal resistance $R_{si} = 6.3\,m\Omega$.

Assumption 6. It is assumed that naturally sampled sine-triangle PWM (SPWM) is used as a modulation strategy for switches. The SPWM uses a sinusoid, having amplitude V_r, as a reference modulating signal and a high frequency triangular waveform, having amplitude V_c, as a carrier signal. These two signals are compared to generate the PWM, see Holmes and Lipo (2003) for details.

Assumption 7. The permanent magnet synchronous machine (PMSM) with two pole pairs is assumed in this study i.e. $n_p = 2$. Thus the mechanical speed of the machine and the fed electrical frequency are related by $\omega_o = 2\omega_m$. In this study, the nominal operating speed of $\omega_m = 6$krpm is assumed for PMSM, see Rabiei et al. (2012).

Assumption 8. The dc-link capacitor is assumed to be non-ideal i.e. it has effective series resistance (ESR) R_{ci}. This assumption is made to stay close to reality in terms of compensation potential of dc-link capacitor.

4. DC-LINK CURRENT CALCULATION USING DOUBLE FOURIER SERIES APPROACH

The dc-link ripple current is the cause for additional battery losses. Though, the harmonic content of dc-link current can also be determined using Fast Fourier Transform analysis of time-varying switched waveforms of the *simulated* circuit but it is computationally very expensive especially for PWM systems with a high switching frequency. Thus, in this section, to exactly characterize the losses the dc-link current is *analytically* computed for both 3-ϕ MLC and 3-ϕ TLI using double Fourier series approach, see Black (1953), and Holmes and Lipo (2003) for details. In high frequency PWM power converters, the dc-link current is normally a product of a switching function and the load current as shown, for example, in (1) for MLC. It is generally quite tedious to precisely determine analytically the complex waveform of this dc-link current. The determination of current waveform can be done more easily in frequency domain. If frequency spectrums of $s_{i1}(t)$, $s_{i2}(t)$, and $i_a(t)$ are known then convolution can be performed in frequency domain and then inverse fourier transform is taken to recover the time-waveform of $i_{dci}(t)$.

The spectral analysis of PWM processes is extensively researched in recent years, see Holmes and Lipo (2003), McGrath and Holmes (2009), and the frequency spectrum of commonly used switching functions is now well known from PWM theory. The switching waveform generated by PWM process is not generally periodic and is normally a function of two other periodic time-waveforms so the machinery of double Fourier series, see Black (1953), is used to analyze the harmonic content of this complex waveform. The general solution for any switching function $s_{ij}(t)$ of any switched phase-leg[1] 'j' is given by, see McGrath and Holmes (2009)

$$\begin{aligned} s_{ij}(t) = \frac{A_{00}}{2} &+ \sum_{l=1}^{\infty}\Big[A_{0l}\cos(ly) + B_{0l}\sin(ly)\Big] \\ &+ \sum_{k=1}^{\infty}\Big[A_{k0}\cos(kx) + B_{k0}\sin(kx)\Big] \\ &+ \sum_{k=1}^{\infty}\sum_{\substack{l=-\infty \\ l\neq 0}}^{\infty}\Big[A_{kl}\cos(kx+ly) + B_{kl}\sin(kx+ly)\Big] \end{aligned} \tag{3}$$

where A_{kl} and B_{kl} are Fourier coefficients given by

[1] It refers to a leg with a switch-pair inside 3-ϕ MLC or 3-ϕ TLI. It should not be confused with the phase of 3-ϕ AC system.

$$A_{kl} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} s_{ij}(t)\cos(kx+ly)\mathrm{d}x\mathrm{d}y \tag{4a}$$

$$B_{kl} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} s_{ij}(t)\sin(kx+ly)\mathrm{d}x\mathrm{d}y \tag{4b}$$

and $x = \omega_c t + \theta_{ci}$, $y = \omega_o t + \theta_{oj}$ where ω_c is the carrier frequency, ω_o is the output fundamental frequency, θ_{ci} is the carrier phase angle for PC$_i$ and θ_{oj} is the phase angle of the fundamental sinusoidal waveform used as a reference in PWM generation for each phase-leg 'j'.

4.1 Double Fourier Series of SPWM

In this study we use SPWM (cf. assumption-6) for switching the switches. The double Fourier series representation of SPWM is now well known and is given by, see Holmes and Lipo (2003), McGrath and Holmes (2009)

$$\begin{aligned} s_{ij}(t) &= \frac{1}{2} + \frac{M_o}{2}\cos(y) \\ &+ \frac{2}{\pi}\sum_{k=1}^{\infty}\left[\frac{1}{k}J_0\left(k\frac{\pi}{2}M_o\right)\sin\left(k\frac{\pi}{2}\right)\cos\left(kx\right)\right] \\ &+ \frac{2}{\pi}\sum_{k=1}^{\infty}\sum_{\substack{l=-\infty\\ l\neq 0}}^{\infty}\left[\frac{1}{k}J_l\left(k\frac{\pi}{2}M_o\right)\sin\left([k+l]\frac{\pi}{2}\right)\cos\left(kx+ly\right)\right] \end{aligned} \tag{5}$$

where $J_l(\xi)$ denotes a Bessel function of the first kind with order l and argument ξ. The angle

$$\theta_{ci} = \frac{2\pi(i-1)}{(n-1)}, \quad \forall i \in \{1, 2, \cdots, n-1\} \tag{6}$$

is the carrier phase angle, θ_{oj} is the phase angle of the fundamental sinusoidal waveform used as reference in PWM generation for each phase-leg, and M_o is its modulation index. The frequency of this waveform is equal to that of desired fundamental output and the value of phase-angle θ_{oj} normally depends on the number of phase-legs in the PC. Now comparing (5) with (3) we get the following Fourier coefficients for SPWM:

$$\begin{aligned} &A_{00} = 1,\ A_{01} = \frac{M_o}{2} \text{ and } \ A_{0l} = 0,\ \forall l > 1, \\ &A_{kl} = \left[\frac{2}{k\pi}J_l\left(k\frac{\pi}{2}M_o\right)\sin\left([k+l]\frac{\pi}{2}\right)\right], \forall k \in \mathbb{N}^+,\ \forall l \in \mathbb{Z}, \\ &B_{kl} = 0,\ \forall k \in \mathbb{N},\ \forall l \in \mathbb{Z} \end{aligned} \tag{7}$$

4.2 3-ϕ MLC: DC-Link Current in a Power Cell

In this subsection, the dc-link current in three-level PC$_i$ of 3-ϕ MLC is calculated. Only phase-a of 3-ϕ MLC is considered. Due to stated assumptions, the result will be same for other phases. Let us now consider the dc-link current, in PC$_i$ of phase-a, given by

$$i_{dci}(t) = s_i(t)i_a(t) = \left[s_{i1}(t) - s_{i2}(t)\right] i_a(t) \tag{8}$$

where $s_{i1}(t)$ and $s_{i2}(t)$ are SPWM switching function for phase-leg-1 and phase-leg-2 and $i_a(t)$ is the sinusoidal load current, as defined in (2), for phase-a of 3-ϕ MLC. The phase switching functions are given by (5) with angles θ_{oj} defined by

$$\theta_{oj} = \begin{cases} 0 & \text{if } j = 1 \\ -\pi & \text{if } j = 2 \end{cases} \tag{9}$$

Recall that in context of MLC, $s_i(t)$ is considered as a switching function for whole PC$_i$. In the following, the expression for $s_i(t)$ will be derived. For notational convenience here we assume $\theta_{ci} = 0$ but it will not change the form of final result.

Phase-leg 1: In this case $\theta_{o1} = 0$. Now plugging in the values of x and y in (5) and doing some simple manipulations, (5) can be rewritten as follows

$$\begin{aligned} s_{i1}(t) &= \frac{1}{2} + \frac{M_o}{2}\cos(\omega_o t) + \frac{2}{\pi}\sum_{k=1}^{\infty}\left[\frac{1}{k}J_0\left(k\frac{\pi}{2}M_o\right)\sin\left(k\frac{\pi}{2}\right)\right. \\ &\left.\times\cos\left(kw_c t\right)\right] + \frac{2}{\pi}\sum_{k=1}^{\infty}\sum_{\substack{l=-\infty\\ l\neq 0\\ l=even}}^{\infty}\left[\frac{1}{k}J_l\left(k\frac{\pi}{2}M_o\right)\sin\left([k+l]\frac{\pi}{2}\right)\right. \\ &\left.\times\cos\left(k\omega_c t + l\omega_0 t\right)\right] + \frac{2}{\pi}\sum_{k=1}^{\infty}\sum_{\substack{l=-\infty\\ l\neq 0\\ l=odd}}^{\infty}\left[\frac{1}{k}J_l\left(k\frac{\pi}{2}M_o\right)\right. \\ &\left.\times\sin\left([k+l]\frac{\pi}{2}\right)\cos\left(k\omega_c t + l\omega_0 t\right)\right] \end{aligned} \tag{10}$$

Phase-leg 2: In this case $\theta_{o1} = -\pi$ is used in (5) and then using the fact that $\cos(\alpha - l\pi) = \cos(\alpha)$, if l is even and $\cos(\alpha - l\pi) = -\cos(\alpha)$, if l is odd, we get the following double Fourier series representation of SPWM for phase-leg 2

$$\begin{aligned} s_{i2}(t) &= \frac{1}{2} - \frac{M_o}{2}\cos(\omega_o t) + \frac{2}{\pi}\sum_{k=1}^{\infty}\left[\frac{1}{k}J_0\left(k\frac{\pi}{2}M_o\right)\sin\left(k\frac{\pi}{2}\right)\right. \\ &\left.\times\cos\left(kw_c t\right)\right] + \frac{2}{\pi}\sum_{k=1}^{\infty}\sum_{\substack{l=-\infty\\ l\neq 0\\ l=even}}^{\infty}\left[\frac{1}{k}J_l\left(k\frac{\pi}{2}M_o\right)\sin\left([k+l]\frac{\pi}{2}\right)\right. \\ &\left.\times\cos\left(k\omega_c t + l\omega_0 t\right)\right] - \frac{2}{\pi}\sum_{k=1}^{\infty}\sum_{\substack{l=-\infty\\ l\neq 0\\ l=odd}}^{\infty}\left[\frac{1}{k}J_l\left(k\frac{\pi}{2}M_o\right)\right. \\ &\left.\times\sin\left([k+l]\frac{\pi}{2}\right)\cos\left(k\omega_c t + l\omega_0 t\right)\right] \end{aligned} \tag{11}$$

Now using (10) and (11), the overall switching function s_i of PC$_i$ is given by

$$\begin{aligned} &s_i(t) = s_{i1}(t) - s_{i2}(t) = \\ &M_o\cos(\omega_o t) + \frac{4}{\pi}\sum_{k=1}^{\infty}\sum_{\substack{l=-\infty\\ l\neq 0\\ l=odd}}^{\infty}\left[\frac{1}{k}J_l\left(k\frac{\pi}{2}M_o\right)\sin\left([k+l]\frac{\pi}{2}\right)\right. \\ &\left.\times\cos\left(k\omega_c t + l\omega_0 t\right)\right] \end{aligned} \tag{12}$$

Finally the dc-link current in PC$_i$ can be computed by direct multiplication of (2) and (12) which gives

$$\begin{aligned} i_{dci}(t) &= \frac{M_o I_a}{\sqrt{2}}\cos(\theta) + \frac{M_o I_a}{\sqrt{2}}\cos(2\omega_o t + \theta) \\ &+ \left[\frac{4}{\pi}\sum_{k=1}^{\infty}\sum_{\substack{l=-\infty\\ l\neq 0\\ l=odd}}^{\infty}\left[\frac{1}{k}J_l\left(k\frac{\pi}{2}M_o\right)\sin\left([k+l]\frac{\pi}{2}\right)\right.\right. \\ &\left.\left.\times\cos\left(k\omega_c t + l\omega_0 t\right)\right]\right]\sqrt{2}I_a\cos(\omega_o t + \theta) \end{aligned} \tag{13}$$

Thus, it is obvious from (13) that dc-link current in any PC_i of 3-ϕ MLC consists of a dc component, large 2nd baseband harmonic, and all odd carrier sidebands including triplen sideband harmonics.

4.3 3-ϕ TLI: DC-Link Current Harmonics

The 3-ϕ TLI consists of only one PC with six switches arranged in three phase-legs. Since there is only one PC so subscript 'i' will be dropped in the following mathematical development. The total dc-link current in any 3-ϕ TLI is given by adding dc-link current contributions from all three phase-legs as follows

$$i_{dc} = i_{dc1}(t) + i_{dc2}(t) + i_{dc3}(t) \tag{14}$$

According to McGrath and Holmes (2009), the dc-link current contribution from any phase-leg 'j' for 3-ϕ TLI is given by

$$\begin{aligned} i_{dcj}(t) = \frac{\hat{A}_{00}}{2} + \sum_{l=1}^{\infty}\Big[\hat{A}_{0l}\cos(l\omega_0 t + l\theta_{oj}) \\ + \hat{B}_{0l}\sin(l\omega_o t + l\theta_{oj})\Big] + \sum_{k=1}^{\infty}\Big[\hat{A}_{k0}\cos(k\omega_c t) \\ + \hat{B}_{k0}\sin(k\omega_c t)\Big] + \sum_{k=1}^{\infty}\sum_{\substack{l=-\infty \\ l\neq 0}}^{\infty}\Big[\hat{A}_{kl}\cos\left((k\omega_c t + l\omega_0 t) + l\theta_{oj}\right) \\ + \hat{B}_{kl}\sin\left((k\omega_c t + l\omega_0 t) + l\theta_{oj}\right)\Big] \end{aligned} \tag{15}$$

where $\theta_{oj} = 0$ for $j = 1$ (phase-a), $\theta_{oj} = -\frac{2\pi}{3}$ for $j = 2$ (phase-b), $\theta_{oj} = \frac{2\pi}{3}$ for $j = 3$ (phase-c), and the Fourier coefficients for all three phases are given by:

$$\hat{A}_{00} = \frac{M_o I_j}{4}\cos(\theta), \quad \hat{A}_{0l} = \hat{B}_{0l} = 0, \forall l > 2, \tag{16a}$$

$$\hat{A}_{01} = \frac{1}{2}I_j\cos(\theta), \quad \hat{B}_{01} = -\frac{1}{2}I_j\sin(\theta), \tag{16b}$$

$$\hat{A}_{02} = \frac{M_o}{4}I_j\cos(\theta), \quad \hat{B}_{02} = -\frac{M_o}{4}I_j\sin(\theta), \tag{16c}$$

$$\hat{A}_{kl} = \frac{I_j}{k\pi}\cos\left([k+l]\frac{\pi}{2}\right)\cos(\theta)\left[J_{l+1}(\cdot) - J_{l-1}(\cdot)\right], \quad \forall k \in \mathbb{N}^+, \forall l \in \mathbb{Z}, \tag{16d}$$

$$\hat{B}_{kl} = \frac{I_j}{k\pi}\cos\left([k+l]\frac{\pi}{2}\right)\sin(\theta)\left[J_{l+1}(\cdot) + J_{l-1}(\cdot)\right], \quad \forall k \in \mathbb{N}^+, \forall l \in \mathbb{Z} \tag{16e}$$

Now using above coefficients, the expression (15) for the jth phase-leg switched current gets simplified to

$$\begin{aligned} i_{dcj}(t) = \frac{M_o I_j}{8}\cos(\theta) + \frac{I_j}{2}\cos(\theta)\cos(\omega_0 t + \theta_{oj}) \\ - \frac{I_j}{2}\sin(\theta)\sin(\omega_o t + \theta_{oj}) + \frac{M_o I_j}{4}\cos(\theta)\cos(2\omega_0 t + 2\theta_{oj}) \\ - \frac{M_o I_j}{4}\sin(\theta)\sin(2\omega_o t + 2\theta_{oj}) + \sum_{k=1}^{\infty}\Big[\hat{A}_{k0}\cos(k\omega_c t) \\ + \hat{B}_{k0}\sin(k\omega_c t)\Big] + \sum_{k=1}^{\infty}\sum_{\substack{l=-\infty \\ l\neq 0}}^{\infty}\Big[\hat{A}_{kl}\cos\left((k\omega_c t + l\omega_0 t) + l\theta_{oj}\right) \\ + \hat{B}_{kl}\sin\left((k\omega_c t + l\omega_0 t) + l\theta_{oj}\right)\Big] \end{aligned} \tag{17}$$

Using (17) for $j = 1, 2, 3$ in (14) gives a messy expression but it can be simplified by first using assumption-3 and then identifying the following two trigonometric identities.

$$\begin{aligned} \Big[\cos(x) + \cos(x - l\frac{2\pi}{3}) + \cos(x + l\frac{2\pi}{3})\Big] = 0, \\ \Big[\sin(x) + \sin(x - l\frac{2\pi}{3}) + \sin(x + l\frac{2\pi}{3})\Big] = 0, \\ \forall x, \quad \forall l = \{\pm 1, \pm 2, \pm 4, \pm 5, \pm 7, \cdots\} \end{aligned} \tag{18}$$

Note that the above two identities are true for any angle x where $x \in \{\omega_o t,\ 2\omega_o t,\ (k\omega_c + l\omega_o)t\}$ here. Applying these two identities, the expression for total dc-link current is simplified to (19)

$$\begin{aligned} i_{dc} = \frac{3M_o I_a}{8}\cos(\theta) + 3\sum_{k=1}^{\infty}\Big[\hat{A}_{k0}\cos(k\omega_c t) + \hat{B}_{k0}\sin(k\omega_c t)\Big] \\ + 3\sum_{k=1}^{\infty}\sum_{l\in\mathcal{L}}\Big[\hat{A}_{kl}\cos(k\omega_c t + l\omega_o t) + \hat{B}_{kl}\sin(k\omega_c t + l\omega_o t)\Big] \end{aligned} \tag{19}$$

where $\mathcal{L} = \{-\infty, \cdots, -6, -3, 3, 6, \cdots, \infty\}$. From the expression (19) it is quite obvious that the dc-link current in 3-ϕ TLI consists of dc-component, carrier harmonics and triplen sidebands. Thus in 3-ϕ TLI, the fundamental , baseband harmonics including second, and the non-triplen harmonics are all cancelled. Thus compared to MLC the harmonic content on the dc-side of 3-ϕ TLI is much less which means the current ripple is very low in 3-ϕ TLI compared to that in each PC_i of 3-ϕ MLC.

5. DC-LINK RIPPLE CURRENT COMPENSATION: SHUNT CAPACITOR SIZING

The objective is to reduce extra losses in the battery cell due to flow of ripple current. Thus, in order to achieve this objective, a shunt-capacitor with appropriate value need to be connected across $Cell_i$ in the dc-link. The capacitor acts as a compensator/filter for dc-link ripple current. In this section, the size of capacitor is determined for both 3-ϕ TLI and for each PC_i in 3-ϕ MLC.

5.1 DC-Link Capacitor Size for each PC_i in 3-ϕ MLC

The size of the dc-link capacitor depends either on the amount of ripple current that is shunted by the capacitor or on the amount of energy it has to store over one cycle of fundamental frequency. With infinite capacitance value, the whole oscillating power (including the reactive power) will be supplied by the capacitor C_i and the battery will only supply the active power. Since infinite capacitance is practically infeasible, some tolerable level of current/voltage ripple is allowed to determine the finite capacitance value. The ripple in the dc-link voltage appears due to the oscillating dc-link current and the battery internal resistance. The amplitude of voltage ripple depends on the amplitude of the oscillating component of the dc-link current $i_{Bi}(t)$ and the value of series resistance R_{si}. To determine these ripple variables, the dc-link ac equivalent circuit is drawn as shown in Figure 3. In the model, the capacitor is assumed to be non-ideal i.e. it has effective series resistance (ESR). Now using phasor analysis and applying Kirchhoff's current law at node-A, the ac ripple current in the battery is obtained as

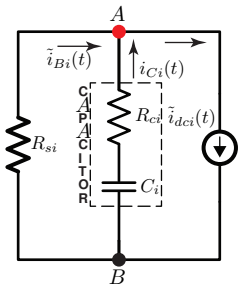


Fig. 3. DC-Link ac equivalent circuit.

$$\tilde{I}_{Bi}(\omega) = \left(\frac{1 + sR_{ci}C_i}{1 + sR_{ci}C_i + sR_{si}C_i}\right)\tilde{I}_{dci}(\omega) \qquad (20)$$

where $s = j\omega$ and $\tilde{I}_{dci}(\omega)$ is the pure ac-component of the dc-link current given by (13). Under the assumption of infinite switching frequency, all the carrier and sideband harmonics can be easily filtered, using a very small capacitor, and thus can be neglected. Therefore, the equation (13) is simplified to

$$i_{dci}(t) \cong \underbrace{\frac{M_o I_a}{\sqrt{2}}\cos(\theta)}_{I_{dci}} + \underbrace{\frac{M_o I_a}{\sqrt{2}}\cos(2\omega_o t + \theta)}_{\tilde{i}_{dci}(t)} \qquad (21)$$

where $w_o = 2\omega_m$ is the electrical angular frequency being fed to electrical machine. From (21) it is quite evident that the dc-link current at the PC_i input consists of two components: the pure dc-component I_{dci} and the pure ac-component $\tilde{i}_{dci}(t)$ at second baseband harmonic frequency. Note that the amplitude of this ac-component is equal to dc-component. Using this approximation, the expression (20) can be easily evaluated for peak magnitude of the battery ripple current as given below

$$\tilde{I}_{Bim}(\omega) = \left(\sqrt{\frac{1 + \omega^2 R_{ci}^2 C_i^2}{1 + \omega^2 (R_{ci}C_i + R_{si}C_i)^2}}\right)\frac{\sqrt{2}M_o I_a}{2} \qquad (22)$$

where $\omega = 2\omega_o = 4\omega_m$ is the dc-link ripple frequency. Note that in the absence of dc-link capacitor, $i_{Bi}(t) = i_{\text{dci}}(t)$. Only the dc-component transfers the real power whereas the ac-component in the absence of capacitor incurs extra losses in the internal resistance of the battery. It is well known that this ac ripple current degrades the battery life-time, see Wen et al. (2012). Thus it is quite important to take this thing into consideration while designing the dc-link side of each PC_i. Ideally battery should provide only the dc-component and the ac ripple should be taken by capacitor. However, the battery manufacturer normally allows certain maximum tolerable level of ripple current above which battery's life-time is significantly degraded. It is normally recommended to limit the ripple current below 10% of the rated current capacity of a battery cell, see Wen et al. (2012). Thus, for a graphical illustration it is more useful to show *battery ripple current peak magnitude per unit dc current component* as given below

$$\delta\tilde{I}_{Bim}(\omega) = \frac{\tilde{I}_{Bim}(\omega)}{\bar{I}_{Bi}} = \left(\sqrt{\frac{1 + \omega^2 R_{ci}^2 C_i^2}{1 + \omega^2 (R_{ci}C_i + R_{si}C_i)^2}}\right)\frac{1}{\cos(\theta)} \qquad (23)$$

where $\bar{I}_{Bi} = I_{dci} = \frac{M_o I_a}{\sqrt{2}}\cos(\theta)$ is the dc component of dc-link current provided by the battery. The above relation

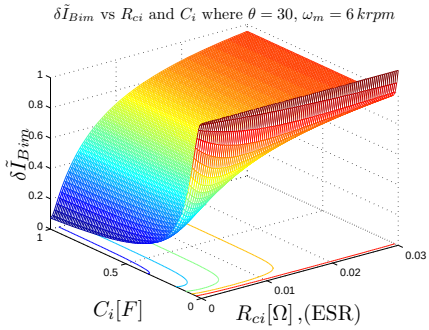


Fig. 4. *Peak magnitude of battery ripple current per unit dc current* versus C_i and R_{ci}.

clearly shows that the battery ripple current depends not only on capacitor size, capacitor effective series resistance (ESR) but also on the frequency ω of the ripple current component under consideration. For sake of completeness, other ripple variables are also determined as given below. The ripple current through the capacitor is given by

$$I_{Ci}(s) = \left(\frac{-sR_{si}C_i}{1 + s(R_{ci}C_i + R_{si}C_i)}\right)\tilde{I}_{dci}(s) \qquad (24)$$

Similarly, the ripple voltage across capacitor is given by

$$V_{Ci}(s) = \left(\frac{R_{si}}{1 + s(R_{ci}C_i + R_{si}C_i)}\right)\tilde{I}_{dci}(s) \qquad (25)$$

and the ac ripple in the dc-link voltage is given by

$$\tilde{V}_{dci}(s) = \left(\frac{1 + sR_{ci}C_i}{1 + s(R_{ci}C_i + R_{si}C_i)}\right)\tilde{I}_{dci}(s)R_{si} \qquad (26)$$

where $\tilde{V}_{dci}(s) = \tilde{V}_{AB}(s)$. Note that all the ripple signals involved here have frequency $\omega = 2 \cdot \omega_o$. Figure 4 shows the plot of $\delta\tilde{I}_{Bim}$ versus C_i and R_{ci} for nominal machine operation @$f_m = 100\,\text{Hz}(\omega_m = 6\,\text{krpm})$ which implies that the ripple frequency $f = 4f_m = 400\,\text{Hz}$. All other parameters are assumed as fixed i.e. $\theta = 30°$, $M_o = 0.9$, and $R_{si} = 6.3\,m\Omega$. This plot clearly shows that to achieve $\delta\tilde{I}_{Bim} < 0.1$, very large value ($> 1F$) of capacitor with significantly low ESR value will be needed. The idea of the required capacitor size can be perceived by the size $90 \times 150\,[mm]$ $(D \times L)$ of a typical $10\,mF, 350\,V$ aluminium capacitor.

5.2 Capacitor Size for 3-ϕ TLI

Under ideal conditions, i.e. infinite switching frequency, balanced linear load with harmonic free ac voltages and currents, (cf. assumptions), all the carrier and sideband harmonics can be neglected and the dc-link current given by equation (19) can then be approximated by

$$i_{dc}(t) \cong \frac{3M_o I_a}{8}\cos(\theta) \qquad (27)$$

The above equation shows that the dc-link current has only pure dc component and there is no time-varying component of power output exactly like in the case of ideal 3-ϕ ac systems. Thus, for ideal 3-ϕ TLI no dc-link compensation capacitor is needed.

Remark 1. Note that under non-ideal conditions i.e. when harmonics are present and/or switching frequency is finite then the dc-link current will contain harmonics and thus there will be a time-varying power component. However,

the dc-link current harmonics in this case will be present around switching frequency f_s which is much higher than the fundamental ac frequency f_o. In this case, the reactive power will shuffle from one phase to another phase $@f_s$. Thus even under non-ideal conditions, the capacitor has to deliver time varying power for a very short time interval compared to the case of dc-link capacitor in PC_i of MLC. Thus the capacitor has to store very small amount of energy and consequently the size will be very small comparatively. This is the main advantage of 3-ϕ TLI.

6. ADDITIONAL BATTERY LOSSES IN 3-ϕ MLC

In this section, the additional power loss at the battery due to ripple current is calculated as

$$P_{lBqi} = \tilde{I}_{Bir}^2 R_{si} \tag{28}$$

where $\tilde{I}_{Bir}$ is the rms value of the battery ripple current given by

$$\tilde{I}_{Bir} = \left(\sqrt{\frac{1+\omega^2 R_{ci}^2 C_i^2}{1+\omega^2 (R_{ci}C_i + R_{si}C_i)^2}} \right) \frac{M_o I_a}{2} \tag{29}$$

Thus the power loss at the battery $Cell_i$, caused by the flow of ripple current $\tilde{i}_{Bi}(t)$, is given by

$$P_{lBqi} = \left(\frac{1+\omega^2 R_{ci}^2 C_i^2}{1+\omega^2 (R_{ci}C_i + R_{si}C_i)^2} \right) \frac{R_{si} M_o^2 I_a^2}{4} \tag{30}$$

Similarly, the power loss at the battery $Cell_i$ due to the flow of dc current component $\bar{I}_{Bi}$ corresponding to real power is given by

$$P_{lBai} = \bar{I}_{Bi}^2 R_{si} = \left(\frac{R_{si} M_o^2 I_a^2}{2} \right) \cos^2(\theta) \tag{31}$$

Now for graphical illustration, the *ripple power loss per unit real power loss* is computed

$$\delta P_{lBqi} = \frac{P_{lBqi}}{P_{lBai}} = \left(\frac{1+\omega^2 R_{ci}^2 C_i^2}{1+\omega^2 (R_{ci}C_i + R_{si}C_i)^2} \right) \frac{1}{2\cos^2(\theta)} \tag{32}$$

Note that the above relation is only valid for $R_{si} \neq 0$. The expression (32) shows that in the absence of dc-link compensation capacitor ($C_i = 0$), the additional power loss in the battery cell explicitly depends on the power factor $F_p = \cos(\theta)$ i.e.

$$\delta P_{lBqi}^{uc} = \frac{1}{2\cos^2(\theta)} = \frac{1}{2F_p^2} \tag{33}$$

The last relation (33) shows that for the uncompensated case as

$$F_p \to 0 \Rightarrow \delta P_{lBqi}^{uc} \to \infty \tag{34}$$

It is now quite obvious that for low power factor operation, battery cells will see very high additional losses in the absence of a dc-link compensation capacitor. Thus, for sake of saving batteries from additional losses, the dc-link compensation capacitor is unavoidable. In the following, we will use equation (32) and graphically illustrate the effect of various factors on the losses.

6.1 Effect of C_i and R_{ci} (ESR)

In figure 5(a), the per unit ripple power loss δP_{lBqi} is plotted versus C_i and R_{ci} for fixed power factor angle $\theta = 30°$. It is assumed that electric machine is operating at the fixed nominal speed of $\omega_m = 6krpm$. Under these conditions, for $C_i = 0$, the battery cell will see almost 66% additional losses. The figure shows that for any fixed value of capacitor, increasing ESR will significantly increase the losses. The figure also shows that just choosing a bigger capacitor without taking ESR into consideration may not help to reduce the losses. Both capacitance and ESR value are equally important and thus capacitor must be selected properly considering both parameters. For example, to compensate for the additional losses under stated conditions, we have to use here at least $0.5\,F$ capacitor with very low ESR value ($R_{ci} \leq 1\,m\Omega$).

6.2 Effect of C_i and Power Factor (F_p) Angle θ

The figures 5(b) and 5(c) show variation in δP_{lBqi} as a function of C_i and power factor angle θ where it is assumed that $R_{ci} = 10\,m\Omega$ and the electric machine is operating at the fixed nominal speed of $\omega_m = 6krpm$. The figure 5(b) shows that for $F_p = 0.5$ and $C_i = 10\,mF$, the battery will see almost 182% additional losses. Similarly figure 5(c) shows that for $F_p = 0.2$ and $C_i = 10\,mF$, the battery will see 11 times more losses. These figures show that for low power factor operation ($F_p < 0.7, \quad (\theta > 45°)$), the additional battery losses due to ripple current will be significantly high even when using compensation capacitor with $C_i = 10\,mF$ and $R_{ci} = 10\,m\Omega$. These figures also show that even for unity power factor, battery cells will see 50% more losses despite using $10\,mF$ capacitor with $10\,m\Omega$ ESR.

Thus, the large dc-link ripple current in each PC_i of 3-ϕ MLC causes significant additional heating that results in rise of operating temperature of cells which is well known to have a detrimental impact on a battery lifetime.

6.3 Capacitor Size Example

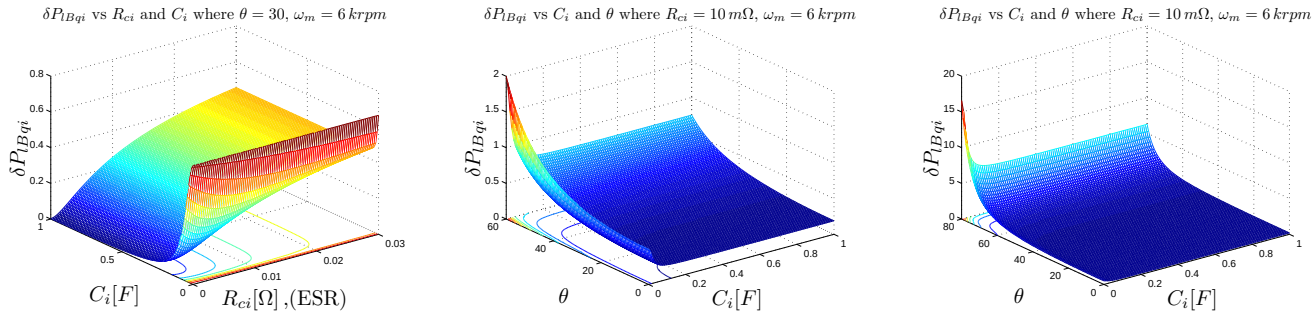
Let us assume that electric machine is operating at $\omega_m = 6krpm$ with power factor $F_p = 0.9$ and $R_{si} = 6.3\,m\Omega$. The objective is to reduce additional losses δP_{lBqi} below 10%. Now using equation (32), it is easy to verify that the compensation capacitor with following specifications will be needed inside each PC_i of 3-ϕ MLC to achieve the objective:

$$C_i = 132\,mF, \quad R_{ci} = 1\,m\Omega \tag{35}$$

Thus, all the figures and the above capacitor size example shows that a very big capacitor with very low ESR is required inside each PC_i of 3-ϕ MLC to save battery cells from significant additional losses and the accelerated capacity fading not only for low power factor but also for high power factor operation.

7. CONCLUSIONS

In this study we have theoretically established that the ripple current on the dc-link inside each PC_i of 3-ϕ MLC is significantly high. Consequently, a large dc-link capacitor is required to filter the ripple. It does not seem practical to put such a big capacitor inside each PC_i of MLC. We have also shown that in the absence of this capacitor, the battery will have to provide significant extra power per unit real power which would result in much higher additional ohmic losses and accelerated capacity fading



(a) *Ripple power loss* δP_{lBqi} versus C_i and R_{ci} for constant power factor angle $\theta = 30°$.

(b) *Per unit ripple power loss* δP_{lBqi} versus C_i and power factor angle $\theta \in \{0, 60°\}$. Here it is assumed that $R_{ci} = 10\,m\Omega$.

(c) *Per unit ripple power loss* δP_{lBqi} versus C_i and power factor angle $\theta \in \{0, 80°\}$. Here it is assumed that $R_{ci} = 10\,m\Omega$.

Fig. 5. Per unit power loss due to ripple current and effects of various factors on the losses.

compared to the case of 3-ϕ TLI especially for low power factor operation. Thus it is concluded that it is not feasible to use 3-ϕ MLC as an integrated cell balancer and a motor driver for 3-ϕ AC applications in xEVs unless, in addition to the dc-link capacitor, some other active filtering/compensation technique is used in order to reduce the size of the capacitor and/or the battery temperature. The alternative is to use single-phase MLC as a dedicated cell balancer inside a battery pack with 3-ϕ TLI at front as a dedicated 3-ϕ AC motor driver but such a solution does not seem cost-effective due to high component count.

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