

THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Novel Terahertz Emitters and Detectors:
InGaAs Slot Diodes and InAs Self-Switching Diodes

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Abstract

Two novel types of diodes for emission and detection of THz radiation have been investigated. The diodes are based on high electron mobility III-V heterostructures. Both diodes are aimed for room-temperature operation, for which there is a demand for new THz technology.

For emission, slot diodes based on an InGaAs heterostructure were studied. Slot diodes have been proposed as a potential power source at terahertz frequencies. However, slot diodes have never been demonstrated experimentally, only in Monte Carlo (MC) simulations. In this thesis, design, fabrication and I-V characterization of slot diodes are covered, as well as emission experiments. Despite the fact that MC simulations predicted an output power of $50 \mu\text{W}$ at 0.8 THz or higher, no emission was detected for the fabricated slot diodes experimentally up to 1 THz with a noise floor of 10 nW.

For detection, InAs self-switching diodes (SSDs) for zero-bias operation were investigated. Fabrication, design and characterization of InAs SSDs are presented. Responsivity was measured on-wafer in the range 2-315 GHz, for which no roll-off was observed. At 50 GHz, the InAs SSD showed a responsivity of 17 V/W and noise-equivalent power (NEP) of $150 \text{ pW}/\text{Hz}^{1/2}$ when driven by a 50Ω source. With a conjugately matched source a responsivity of 34 V/W and NEP of $65 \text{ pW}/\text{Hz}^{1/2}$ are expected, based on s-parameters and responsivity as measured with a 50Ω source. An InAs SSD designed with a substrate antenna demonstrated detection in a free-space experiment at 600 GHz.

For comparison, InGaAs SSDs which are a more established type of SSDs were evaluated. For InGaAs SSDs, a lowest NEP of $65 \text{ pW}/\text{Hz}^{1/2}$ with a 50Ω source was achieved, measured at 50 GHz. The measured responsivity was 280 V/W.

It was observed that DC measurements can be used to successfully predict responsivity and NEP of SSDs. Also, the first systematic experimental study of how the design influences the SSD detection performance was carried out.

Keywords: slot diode, self-switching diode, InAs, InGaAs, zero-bias diode, terahertz, detection, emission

List of Publications

Appended Publications

This thesis is based on the work contained in the following papers:

- [A] A. Westlund, P. Sangaré, G. Ducournau, P-Å. Nilsson, C. Gaquière, L. Desplanque, X. Wallart, J. Grahn "Terahertz Detection in InAs/Al_{0.8}Ga_{0.2}Sb Self-Switching Diodes at Room Temperature and Zero Bias", Manuscript
- [B] A. Westlund, G. Moschetti, H. Zhao, P-Å. Nilsson, J. Grahn, "Fabrication and DC characterization of InAs/AlSb Self-Switching Diodes", in *24th International Conference on Indium Phosphide & Related Materials*, IPRM, pp. 65-68, Aug 2012.
- [C] A. Westlund, P-Å. Nilsson, J. Grahn, "Fabrication and Characterization of InGaAs/InAlAs Slot diodes", in *37th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe*, WOCSDICE, May 2011.
- [D] A. Westlund, G. Moschetti, P-Å. Nilsson, J. Grahn, L. Desplanque, X. Wallart, "Cryogenic DC Characterization of InAs/Al_{0.8}Ga_{0.2}Sb Self-Switching Diodes", in *25th International Conference on Indium Phosphide & Related Materials*, IPRM, May 2013.

Other Publications

The following papers and publications are not appended to the thesis, either due to contents overlapping that of appended papers, or due to contents not related to the thesis.

- [a] J. Mateos J.F. Millithaler, I. Íñiguez-de-la-Torre, A. Íñiguez-de-la-Torre, B.G. Vasallo, S. Pérez, T. González, Y. Alimi, L. Zhang, A. Rezazadeh, A.M. Song, P. Sangaré, G. Ducournau, C. Gaquiére, A. Westlund, J. Grahn, "Room temperature THz detection and emission with semiconductor nanodevices", in *Spanish Conference on Electron Devices, CDE*, p 215-18, 2013.
- [b] J. Mateos J.F. Millithaler, I. Íñiguez-de-la-Torre, A. Íñiguez-de-la-Torre, B.G. Vasallo, S. Pérez, T. González, Y. Alimi, L. Zhang, A. Rezazadeh, A.M. Song, P. Sangaré, G. Ducournau, C. Gaquiére, A. Westlund, J. Grahn, "", in *36th International Conference on Infrared, Millimeter, and Terahertz Waves, IRMMW-THz 2011*, p 1-2, 2011.

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Chapter 1

Introduction

The terahertz (0.3 THz-3 THz) regime has been of importance to astronomy and spectroscopy physics for decades. While space science has historically been the main driving force [1], there is now an increasing interest from other fields such as public security [2] and data communication [3]. As a result, existing but also new components operating at THz frequencies are constantly being developed for larger bandwidth, higher output power and lower noise.

In this work, two novel types of diodes for room temperature generation and zero-bias detection of THz radiation are investigated. As operation frequency climbs up towards THz, device output power as well as noise properties quickly degrade. It is therefore of general interest to explore new electronic device concepts for generation and detection above 100 GHz.

For THz generation, the InGaAs slot diodes has been experimentally investigated in this work. It is a diode based on a high mobility III-V heterostructure with an InGaAs channel. The slot diode has never been demonstrated experimentally, only in Monte Carlo (MC) simulations [4]. These MC simulations have predicted that the slot diode may operate as a fundamental oscillator at frequencies exceeding 1 THz. The underlying phenomenon is similar to that of Gunn diodes. In the slot diodes the oscillations are expected to occur at a higher frequency than in Gunn diodes, due to ballistic electron transport. In this licentiate thesis, the fabrication and characterization of slot diodes based on the MC simulations are described, including performed emission experiments.

For THz detection, zero-bias direct detectors offer an attractive low-complexity solution. Zero-bias detectors also offer reduced power consumption and $1/f$ noise compared to biased detectors. Room-temperature THz zero-bias detection is today typically achieved with Schottky diodes [5]. The underlying phenomenon in Schottky diodes, thermionic emission, is unfortunately associated with strong temperature dependence [6]. However, Schottky diodes have been demonstrated as detectors up to 2 THz [7]. A noise equivalent power (NEP) of $1.5 \text{ pW/Hz}^{1/2}$ has been reported at 150 GHz, rising to around $20 \text{ pW/Hz}^{1/2}$ at 800 GHz [5]. An alternative to Schottky diodes is Sb-heterostructure backward diodes based on interband tunneling. Sb-heterostructure backward diode detectors at 110 GHz have been demonstrated, with models predicting a cut-off frequency of 805 GHz [8]. Improved temperature stability over Schottky diodes have been reported [9].

In this work, a novel room temperature zero-bias THz detector has been investigated, the self-switching diode (SSD) [10]. The SSD is a field effect device, in which the conductivity of thin semiconductor channels is modulated by the applied voltage. First demonstrated in InGaAs 2003 [10], SSDs have been demonstrated in several III-V heterostructures. Detection has been demonstrated in cryogenically cooled InGaAs SSDs at 2.5 THz [11], and in room temperature GaAs SSDs at 1.5 THz [12]. Room-temperature GaN SSDs have recently been reported, operating at 300 GHz [13]. SSDs also have been fabricated in a range of other materials, such as ZnO [14], Indium tin oxide [15] and polymer films [16].

The lowest published NEP in SSDs is $65 \text{ pW/Hz}^{1/2}$ for 0-110 GHz, reported for InGaAs SSDs [17]. While this NEP is modest compared to existing technologies at a few hundred GHz, the performance of SSDs is not expected to decrease until far into the THz range [18]. Since InAs exhibits a mobility superior to all other materials mentioned above, a higher operation frequency may be expected from InAs SSDs. Indeed, MC simulations of InAs SSDs suggest a constant responsivity from DC to up to 2 THz [18].

In this work, InAs SSDs are presented for the first time. The fabrication is described and design aspects analyzed. On-wafer measurements up to 315 GHz are presented, followed by detection at 600 GHz in a free-space set-up. Finally, an imaging experiment with InAs SSDs is presented.

Chapter 2

InGaAs slot diodes

The slot diode is a proposed novel device for producing THz radiation [4,19,20]. So far, the slot diode has only been proven to generate THz radiation in MC simulations. These have demonstrated fundamental oscillations in the range 0.4-2. THz [19]. By adjusting the bias voltage, the oscillation frequency can be tuned 50%. However, THz emission from slot diodes has never been demonstrated experimentally.

This chapter starts out describing the operation of the slot diode. Then follows the fabrication and I-V measurements. Finally, a summary of performed emission experiments is presented.

2.1 Device principle

In MC simulations, oscillations in slot diodes occur in a way similar to that in Gunn diodes, but at higher frequencies. The frequency of oscillation is predicted to be tunable over a large bandwidth [21]. The slot diode bears a strong physical resemblance to a gate-less high-electron mobility transistor (HEMT) and is fabricated in a similar heterostructure. Similar to HEMTs, the operation of the slot diode relies on the presence of a high-mobility two-dimensional electron gas (2DEG).

A schematic view of the slot diode is shown in Fig. 2.1. Similar to a HEMT, the slot diode is composed of a buffer, channel (containing the 2DEG), barrier and cap layer. In the band structure of the InGaAs channel, electrons are transported in both the central Γ -valley and the satellite L -valley. In the L -

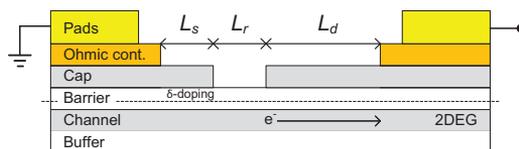


Figure 2.1: Schematic cross-section of the active area of a slot diode. Electrons are accelerated beneath the recess before drifting across the recess-drain region.

valley, the electron mass is higher, and the electrons move slower than in the Γ valley. The band separation is 0.6 eV.

When the slot diode is forward biased, the current in the 2DEG oscillates. Two-dimensional MC simulations of electron velocity, valley occupation and electron distribution at different times of the oscillation cycle (0.2, 0.3, 0.5, 0.7 ps) is shown in Fig. 2.2 [19]. Since the recessed region is more resistive than the regions with cap the voltage drop across the terminals is concentrated to a small part of the channel under the recess. The strong electric field beneath the recess enables ballistic acceleration of the Γ -valley electrons, reaching a speed of about 10×10^5 m/s at the edge of the recess (Fig. 2.2(a), 0.7 ps). When the voltage across the recess reaches the energy separation of the Γ - and L -valleys, electrons leaving the recess region are to a large extent scattered into the L -valley (Fig. 2.2(b), 0.2-0.5 ps). A domain of slower L -valley electrons forms and traverse the recess-drain region at a speed of $2 - 4 \times 10^5$ m/s (Fig. 2.2(a-b), 0.2 ps). In the meantime, the fast Γ -valley electrons that left the recess before (and after) the accumulation of slow L -valley electrons still travel at 10×10^5 m/s. This causes an area of low total electron concentration to form where the L -valley concentration is high (Fig. 2.2(b), 0.2 ps). As this area of low total electron concentration grows, the voltage drop across it will increase at the expense of the voltage drop across the recess. After some time, the voltage drop across the recess is not enough to allow electrons to scatter into the L -valley. The region of low electron concentration travels across the recess-drain region (Fig. 2.2(a-c), 0.3-0.5 ps) until it has completely left the device (Fig. 2.2(a-c), 0.7 ps). The process starts over.

In a Gunn diode, the field propagates at the saturation velocity for high fields, for InGaAs around 1×10^5 m/s [6, 22]. In the slot diode, the field propagates at the speed of ballistic electrons, around 10×10^5 m/s [19]. For this reason, higher oscillation frequencies are expected from the slot diode.

The three dimensions L_s , L_r and L_d of slot diode defined in Fig. 2.1 are expected to affect the oscillation frequency and magnitude [20]. The source-recess region L_s is considered a parasitic series resistance and should be kept small. By decreasing the length of the recessed region L_r , the electrons are accelerated over a shorter distance, leading to a higher oscillation frequency. The recess-drain region L_d corresponds to the drift region in Gunn diodes. By reduction of L_d , the electrons reach the drain faster. Hence, the oscillations frequency is increased. For larger L_r and L_d , the oscillation frequency becomes low, as well as its magnitude. In fact, simulations suggest that oscillations below <800 GHz are increasingly difficult to achieve [23]. Also, it is not expected from simulations that the presence of oscillations will affect I-V characteristics. Thus indications of slot diode oscillation are expected to be found only from direct measurements of emission in the THz range.

2.2 Device fabrication

InGaAs slot diodes were fabricated with different combinations of L_s , L_r and L_d varying one parameter at a time, based on a $L_s = 200$ nm, $L_r = 200$ nm and $L_d = 550$ nm design. The InGaAs heterostructure was similar to that of a traditional InP HEMT [24], see Fig. 2.3. The heterostructure was grown on

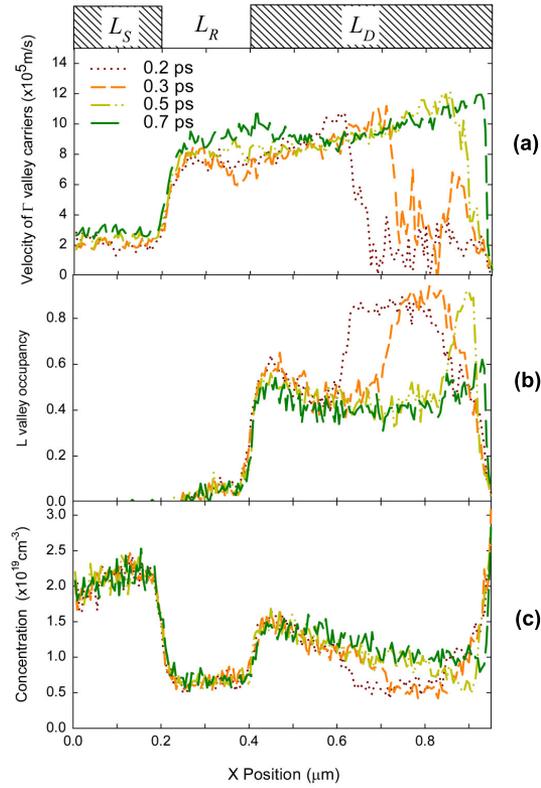


Figure 2.2: MC simulations describing how electron accumulation and depletion regions form and traverse the recess-drain region. [19]

Upper Cap Layer	In ₅₃ Ga ₄₇ As	Si 5x10 ¹⁹ cm ⁻³	100 Å
Lower Cap Layer	In ₅₃ Ga ₄₇ As	Si 6x10 ¹⁸ cm ⁻³	100 Å
Barrier	In ₅₂ Al ₄₈ As	δ -doping	120 Å
Spacer	In ₅₂ Al ₄₈ As	Si 6x10 ¹² cm ⁻³	30 Å
Channel	In ₇₀ Ga ₃₀ As		150 Å
Buffer	In ₅₂ Al ₄₈ As		5000 Å
Substrate	2" S.I InP (001)		

Figure 2.3: Epitaxial structure used for fabrication of the InGaAs slot diode.

an InP wafer using molecular beam epitaxy (MBE). 500 nm In₅₂Al₄₈As buffer was grown on top of the substrate, followed by a 15 nm In₇₀Ga₃₀As channel. Together with the subsequent In₅₂Al₄₈As spacer layer, an InGaAs/InAlAs quantum well was formed, creating a two-dimensional electron gas (2DEG). A $6 \times 10^{18} \text{cm}^{-2}$ planar Si δ -doping deposited on top of the spacer provided electrons for the 2DEG.

To concentrate the electric field to the recess region, the cap must be highly conductive. However, according to MC simulations, a too conductive cap risks to short-circuit any oscillations [23]. In MC simulations, a maximum 10 nm thick cap layer with a doping concentration of $6 \times 10^{18} \text{cm}^{-3}$ was found suitable [4]. However, such a doping level means a relatively high contact resistance. A high doping concentration of $5 \times 10^{19} \text{cm}^{-3}$ was known to produce a low contact resistance ($< 0.3 \Omega \text{mm}$) [25]. These conflicting demands on doping level were traded off by dividing the cap in two separate adjacent layers, one upper cap layer with high doping and one lower cap layer with low doping. Ohmic contacts were formed in the upper, high-doped layer.

The fabrication process is shown in Fig. 2.4. First, the mesa was etched, in a hydrogen peroxide/phosphoric acid-based solution. The second step was ohmic contacts deposited through evaporation, see Fig. 2.4(a). A three-metal Ni/Ge/Au (100/520/820 Å) stack was used. After deposition followed a rapid thermal anneal (RTP) at 275 °C. The contact resistance was $< 0.15 \Omega \text{mm}$. Next, metal pads were evaporated, using a Ti/Au/Ti (200/3000/200 Å) stack.

After the fabrication of the metal layers, the thinning of the cap was implemented, see Fig. 2.4. Using the metal layers as an etch mask, the cap was thinned by wet etching with citric acid/hydrogen peroxide solution. Several samples were etched different times to achieve different cap thicknesses.

Fig. 2.4(c) shows the recess formation. The recess was defined by e-beam lithography. An opening in the resist of width $L_r - 100 \text{ nm}$ was formed. The etch was done with a selective succinic acid/hydrogen peroxide solution, known to etch the InGaAs cap layer at around 70 times higher rate than the InAlAs barrier [26]. By overetching, the recess was extended laterally to reach the width L_r . Oxides were removed before and after etch, with an hydrochloric acid solution.

The sample was passivated by growing 80 nm silicon nitride (SiN_x) (d). The growth was done in a plasma enhanced chemical vapor deposition (PECVD) process at 270 °C. Finally, openings in the SiN_x for probing was done by a

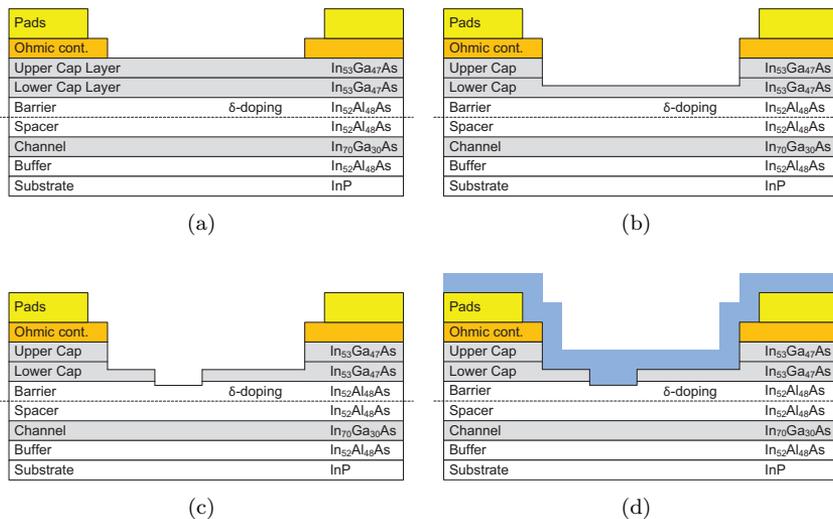


Figure 2.4: Process flow, InGaAs slot diode fabrication. Etching of mesas was followed by (a) ohmic contact and metal pad formation, (b) thinning of cap (c) etching of recess, and (d) device passivation.

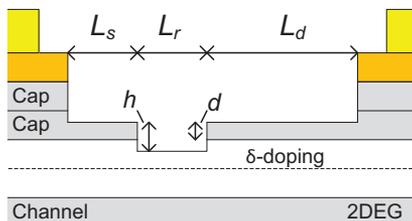


Figure 2.5: Schematic cross-section of the fabricated InGaAs slot diode.

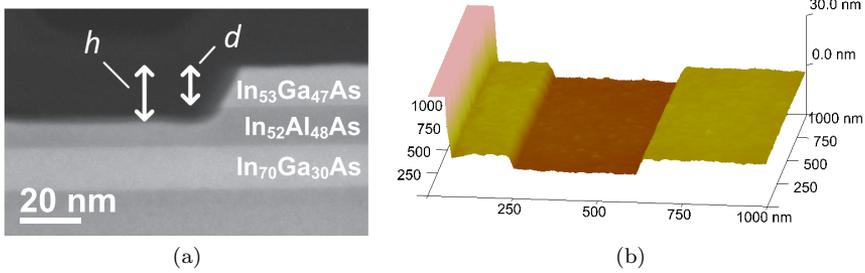
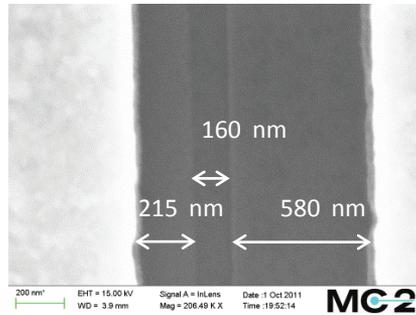
reactive ion etch (RIE) process with NF_3 .

A schematic cross-section of the fabricated device is shown in Fig. 2.5. The recess depth h can be measured with atomic force microscopy (AFM). The cap thickness d can be found by knowing $(h - d)$, that is, how far the recess etch reaches into the barrier. In Fig. 2.6(a), a cross-sectional transmission electron microscopy (XTEM) is shown. This sample was recessed with the same recipe as the slot diodes, and the epitaxial structure was similar. The distance $(h - d)$ was determined to 3 ± 1 nm. Since the etchant is very selective [26], the depth in the InAlAs is not sensitive to etch time. The h parameter was measured to 7 nm with AFM, see Fig. 2.6(b). Hence, by combining the AFM and XTEM measurement, d could be calculated to 4 ± 1 nm.

Hall measurements were performed for recessed regions and regions with 3 nm cap layer, see Table 2.1. For the recessed regions, similar values have been reported earlier [27]. The sheet resistance for regions with thinned down cap was through MC simulations found suitable for achieving the expected oscillations [28]. Hence, thinning down the cap produced the desired combination of suitable sheet resistance and low contact resistance. Finally the lateral

Table 2.1: Hall data for regions with recess or 4 nm cap layer.

Region	R_{sh} [Ω/sq]	n_s [10^{12} cm^{-2}]	μ [cm^2/Vs]
Recess	294	1.64	12900
4 nm cap	112	4.81	11600

Figure 2.6: (a) XTEM of a recessed region. (b) AFM image of the recess in the fabricated slot diode. Measured $h = 7 \text{ nm}$.Figure 2.7: SEM image of a fabricated slot diode. $L_s = 215 \text{ nm}$, $L_r = 160 \text{ nm}$, $L_d = 580 \text{ nm}$.

dimensions of the slot diode were measured by scanning electron microscopy (SEM), see Fig. 2.7. It was found that $L_r = 160 \text{ nm}$, 40 nm less than the nominal design, likely due to the lateral etch rate being lower than expected when the cap was only 4 nm thick. Consequently, L_s and L_d was marginally larger than designed.

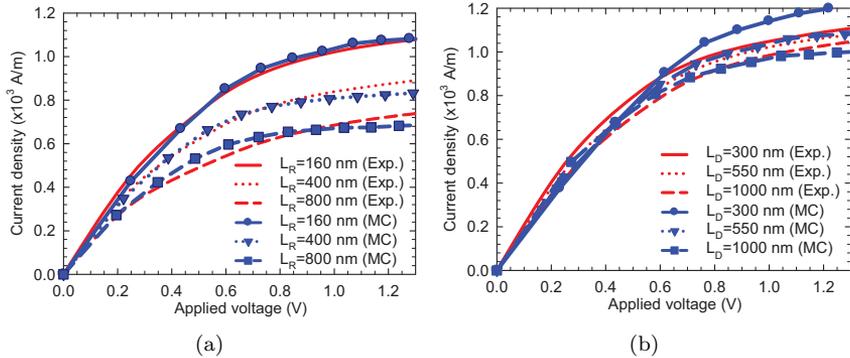


Figure 2.8: In red, I-V measurements of slot diodes with varying (a) L_r ($L_s = 200$ nm, $L_d = 550$ nm) and (b) L_d ($L_s = 200$ nm $L_r = 160$ nm). Corresponding MC simulations in blue. [23]

2.3 Characterization

2.3.1 DC measurements

I-V measurements were performed on slot diodes with different combinations of L_s , L_r and L_d . A typical design with $L_s = 200$ nm, $L_r = 200$ nm $L_d = 550$ nm was used, then varying one parameter at a time. The measured current density for varying L_r and L_d is shown in Fig. 2.8, together with MC simulations of the same design [23]. The current level for $L_r=160$ nm is similar to the maximum current that is observed in InP HEMTs on similar material and recess lengths [25].

The MC simulations in Fig. 2.8 were performed by adjusting the surface charge [28] of regions with recess and 4 nm cap until the I-V measurements was reproduced. As shown in Fig. 2.8, the I-V relation obtained in MC simulations reproduces the I-V measurements fairly well, as well as the effect of changing L_r and L_d . In the same simulations that reproduced the I-V measurements, THz oscillations were observed [23]. Thus, the MC simulations predicted that the fabricated slot diodes would oscillate at THz frequencies.

2.3.2 Cryogenic DC measurements

A comparison of I-V measurements at room temperature and cryogenic conditions, i.e. 300 K and 6 K, respectively, was performed on InGaAs slot diodes. [Paper C]. The MBE-grown epitaxial structure is shown in Fig. 2.9, and was identical to structures used for InP HEMTs [25]. The fabrication was identical to the one described in section 2.2, except for that the cap was not thinned down. Hall measurements at 300 K with the cap layer etched away showed a channel electron mobility of more than 13000 cm²/Vs and a sheet carrier concentration of 9.8×10^{11} cm⁻².

A weak kink was noticed in I-V measurements at 300 K around 0.5 V drain voltage, see Fig. 2.10(a). To further investigate the kink, cryogenic I-V measurements were performed at 6 K and are presented in Fig. 2.10. Compared

Cap Layer	In ₅₃ Ga ₄₇ As	Si 5x10 ¹⁹ cm ⁻³	200 Å
Barrier	In ₅₂ Al ₄₈ As	δ-doping	110 Å
Spacer	In ₅₂ Al ₄₈ As	Si 5x10 ¹² cm ⁻²	30 Å
Channel	In ₆₅ Ga ₃₅ As		150 Å
Buffer	In ₅₂ Al ₄₈ As		5000 Å
Substrate	2" S.I InP (001)		

Figure 2.9: Epitaxial structure used for fabrication of slot diodes for cryogenic measurements.

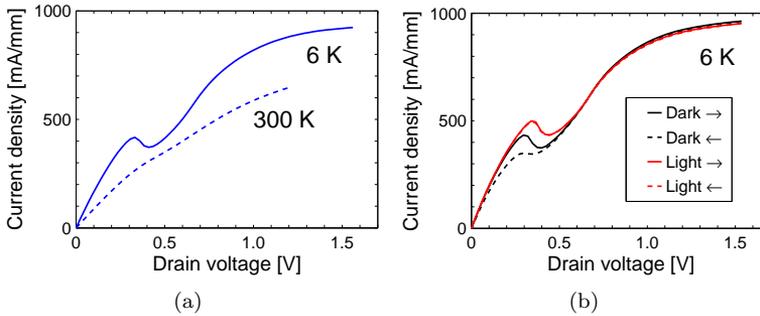


Figure 2.10: Probed I-V measurements of a slot diode at (a) 300 K and 6 K, (b) sweep direction and illumination dependence at 6 K.

to 300 K, the kink behavior was enhanced and the current increased. Similar observations have been reported for InP HEMTs based on identical epitaxial heterostructure [25]. In Fig. 2.10(a), a negative I-V slope is observed at 6 K. However, a negative differential resistance is not expected in I-V measurements of slot diodes. In Fig. 2.10(b), the voltage was swept in the right and left direction at 6 K, in both dark and illuminated conditions. In darkness, the kink was stronger when swept towards the right than when swept towards the left. The negative slope was present in both sweep directions. Illumination reduced the hysteresis. Also, the kink was shifted to a slightly higher voltage.

Later findings in InP HEMT research has shown that a kink very similar to the one observed in the slot diode I-V in Fig. 2.10 can be strongly reduced with Al₂O₃ passivation [29]. Here, the slot diodes were passivated with SiN_x grown in as PECVD process. Further, when MC simulations were tuned to replicate the 300 K I-V measurements in Fig. 2.10(a), no THz oscillations were observed in the simulations (MC could only be performed at 300 K). [23]. This suggests that the kink is a phenomenon related to traps at the heterostructure interfaces rather than an indication of ongoing oscillations.

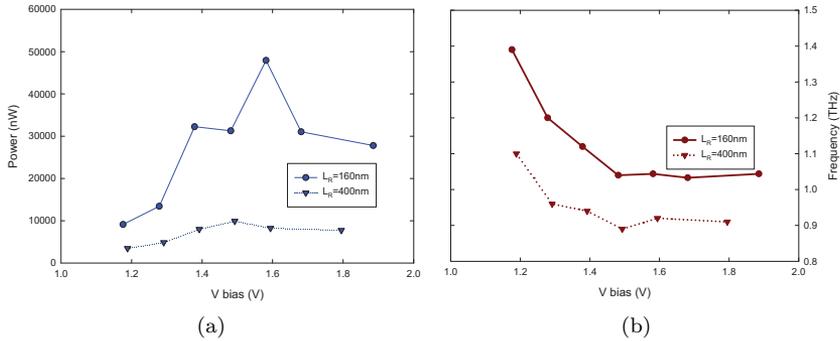


Figure 2.11: MC simulations of (a) output power and (b) oscillation frequency of fabricated slot diodes. [23]

2.3.3 Emission measurements

In Fig. 2.8, MC simulations reproduced I-V measurements of the fabricated slot diodes and predicted that THz oscillation would occur. The MC simulations also provided an estimation of the expected output power and oscillation frequency as a function of applied bias for different L_r , shown in Fig. 2.11. In the MC simulations, the slot diode was short-circuited RF-wise. The design was $L_s = 200\text{ nm}$ and $L_d = 550\text{ nm}$ with a mesa width of $7\text{ }\mu\text{m}$. When biased, an oscillating current was observed in the simulations. The power shown in Fig. 2.11(a) was found as the power this current would dissipate when passed through a $75\text{ }\Omega$ load. It was found that a device with $L_r = 160\text{ nm}$ can be expected to produce higher output power than $L_r = 400\text{ nm}$, and at higher frequencies. A maximum output power of $50\text{ }\mu\text{W}$ was predicted at 1.05 THz and 1.6 V bias. The lowest oscillation frequency was around 0.9 THz.

The expected efficiency can be estimated. For 1.6 V bias, experimental I-V measurements are not available but judging from Fig. 2.8(b) the current should not exceed $1.2 \times 10^3\text{ A/m}$. The DC power consumption for a $7\text{ }\mu\text{m}$ wide slot diode is thus $\approx 13\text{ mW}$. If $50\text{ }\mu\text{W}$ RF would indeed be delivered to the load, the efficiency would be 0.4 %.

It should be noted that this way of estimating the output power is based on the assumption that the oscillating slot diode can be regarded as a constant current source. In reality, the load will cause a feedback that may enhance or reduce oscillations. There may also be an impedance mismatch between the diode and the antenna.

For emission experiments, slot diodes were fabricated with $7\text{ }\mu\text{m}$ wide mesas contained in antennas. Both double-slot antennas and spiral antennas were fabricated, see Fig. 2.12. EM simulations of the self-complementary spiral antenna (in the software ADS Momentum) showed a real input impedance of $50 - 110\text{ }\Omega$ in the range 200-2000 GHz. The real impedance of the double slot antenna is $50\text{ }\Omega$ at 1 THz and is more narrowband than the spiral antenna.

An emission test using a Schottky detector was performed at IEMN in Lille, France [28, 30]. The setup is shown in Fig. 2.13. The samples were glued to a circuit board. To the right in Fig. 2.13, the circuit board mounted sample is seen with a silicon lens placed firmly against the backside of the substrate with

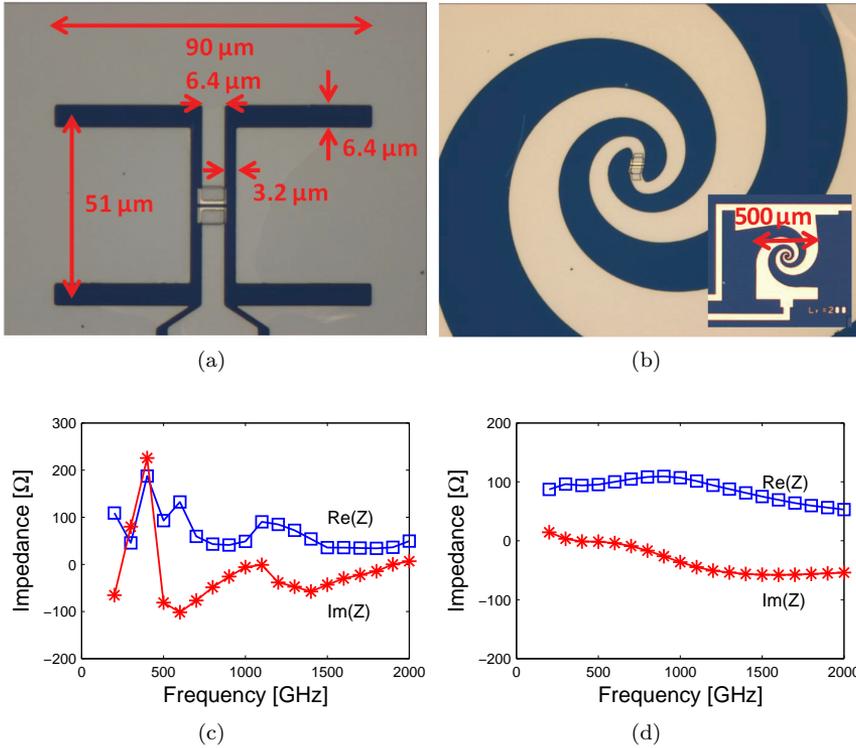


Figure 2.12: Slot diodes with (a) double-slot antenna and (b) spiral antenna. (c) Simulated impedances for double-slot antenna in and (d) spiral antenna. The double slot antenna is resonating at approx 0.9 THz. The spiral antenna is wide-band, with a real impedance in the range 50-110 Ω for 0.2-2 THz.

the samples. Any output was focused with a lens onto the linearly polarized Schottky detector. The detector worked up to 900 GHz. An optical chopper modulated the beam. No output power was detected. Several devices with both $L_r = 160$ nm and $L_r = 400$ nm were tested at different bias in the range 1-1.5 V. The noise floor as referenced to emitted power was estimated to 50 nW at 900 GHz, and lower for lower frequencies.

A second experiment was set up by the University of Manchester, UK [31]. The setup is shown in Fig. 2.14. The detector was an InSb bolometer with a window transparent for 0.1-1 THz radiation. With a black-body source, the responsivity of the bolometer was measured to 800 V/W. The noise floor as referenced to emitted power was estimated to 10 nW. Slot diodes with both $L_r = 160$ nm and $L_r = 400$ nm were tested. No emission was detected.

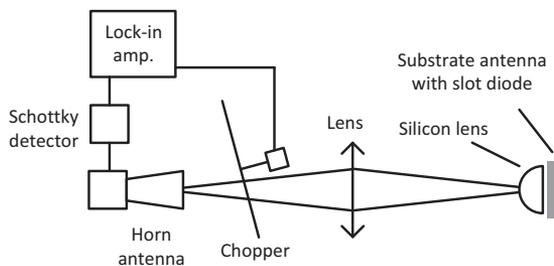


Figure 2.13: Set-up for slot diode emission experiments with a Schottky detector. The sample under test was positioned with the backside firmly against the silicon lens.

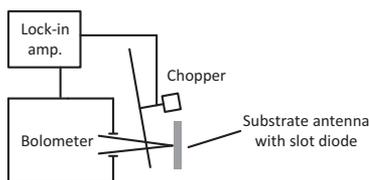


Figure 2.14: Bolometer-based measurement system used for detecting emission from slot diodes.

2.3.4 Characterization summary

Slot diodes proposed to operate as THz emitters as predicted by MC simulations have been designed and fabricated. I-V measurements of the fabricated diodes were closely reproduced by MC simulations. The same simulations predicted that the fabricated slot diodes would oscillate. The predicted frequency of oscillation was 0.8 THz or higher. However, no evidence of slot diode emission was detected neither with a Schottky detector up to 900 GHz nor with a bolometer detector up to 1 THz.

A possible reason for the absence of detected emission is that the frequency of oscillations was higher than 1000 GHz. Other reasons could be that in the MC simulations, the slot diode was simulated as short-circuited RF-wise, while the load is about 100Ω in the emission experiments. Finally, the three-dimensional nature of components, material imperfections and heat effects are not taken into account in the MC simulations. All this may partly explain the absence of detected output power for InGaAs slot diodes in the THz range as predicted from the MC simulations.

Chapter 3

InAs self-switching diodes

Self-switching diodes (SSDs) were first demonstrated in InGaAs [10] and has since then been fabricated in a wide range of materials. The highest operation frequencies of SSDs as RF detectors have been demonstrated in III-V compound semiconductor heterostructures. Room temperature SSD detectors have been demonstrated at 110 GHz in InGaAs [17], at 300 GHz in GaN [13], and at 1.4 THz in GaAs. In cryogenic conditions, detection has been demonstrated at 2.5 THz in InGaAs SSDs [11].

InAs has the second smallest band gap (0.36 eV) of all III-V semiconductors, surpassed only by InSb. InAs offers a very high electron mobility ($30000 \text{ cm}^2/\text{Vs}$) and saturation velocity ($4 \times 10^7 \text{ cm/s}$) [32], making it interesting for high frequency applications. MC simulations of intrinsic SSDs have shown that for the same design, InAs SSD detectors will work for higher frequencies than the more established InGaAs SSDs [18]. While I-V measurements of InAs SSDs have been reported previously [33, 34], InAs SSDs have not been characterized as detectors until recently [Paper A].

This chapter starts by explaining the principle of the SSD. Responsivity and NEP are explained, and how they relate to I-V measurements. Then follows the fabrication of the InAs SSDs. The large lattice constant of InAs requires an AlSb buffer. However, AlSb is chemically unstable [35] and poses a challenge in fabrication. For this reason, SSDs were also fabricated in an InGaAs, which is chemically more stable. DC and RF characterization is presented. RF characterization was performed on-wafer for 2-315 GHz and in a free-space experiment at 200 and 600 GHz. Finally, imaging experiments using an InAs SSD detector are presented.

3.1 Device principle

SSDs are defined by a two-dimensional geometry in a semiconductor. In this work, the SSD was defined in an heterostructure containing a 2DEG. The design is shown in Fig. 3.1. The SSD can be understood as a transistor where one or several channels (marked A in Fig. 3.1) of width W connect the source to drain. Channels are separated by flanges (marked B in Fig. 3.1) acting as gates connected to the drain [36].

The SSD diode behavior is illustrated in Fig. 3.2. In Fig. 3.2(a), the SSD is in equilibrium. Surface charge on the trench sidewalls causes a lateral depletion in the 2DEG of width W_d . The effective channel width is $W_{eff} = W - 2W_d$. In reverse bias (Fig. 3.2(b)), the flanges will be negatively biased, and thus reduce W_{eff} . Fig. 3.2(c) shows the diode in forward bias, where the flanges will be positively biased, and thus increase W_{eff} . As a result, the channel resistance will depend on the bias voltage applied to the SSD. For smaller W , the difference in resistance between forward and reverse bias is increased [37].

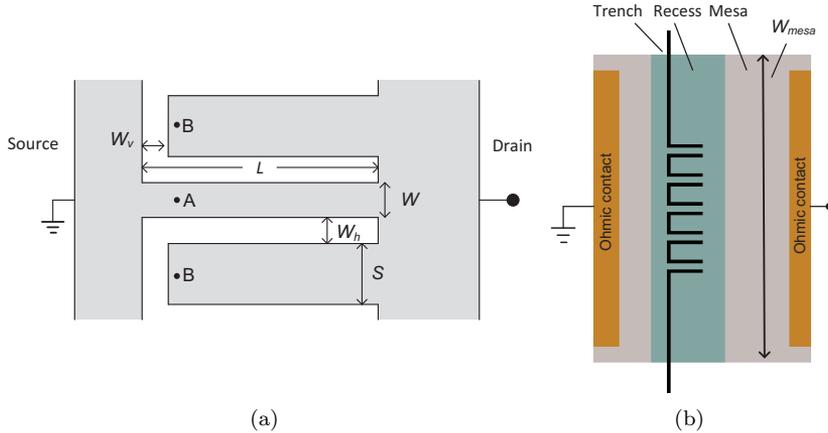


Figure 3.1: Schematic view of the geometry of (a) a single SSD channel and (b) a multi-channel SSD. Design parameters are channel width (W), channel length (L), number of channels (N), trench widths (W_h, W_v), separation (S) and mesa width W_{mesa} .

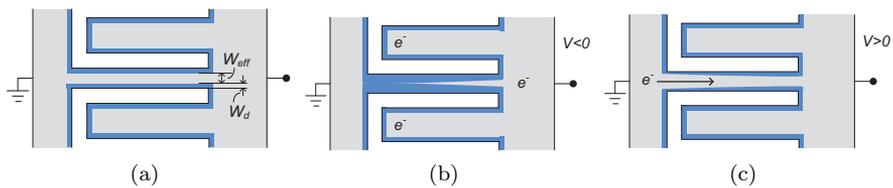


Figure 3.2: Schematic view of depletion of the SSD channel in (a) zero bias, (b) reverse bias and (c) forward bias.

3.2 Voltage responsivity and NEP

When an RF power P_a is absorbed by a nonlinear diode, a voltage V_{det} arises across the terminals. The highest output voltage for a certain incident power P_i is achieved when the RF source is perfectly matched to the diode ($P_i = P_a$) and all incident power is also absorbed. With the optimum small-signal voltage

responsivity defined as the ratio $\beta_{opt} = V_{det}/P_a$, it can be shown [38] that

$$\beta_{opt} = \frac{1}{2}R_0\gamma, \quad (3.1)$$

where $R_0 = 1/(dI/dV)|_{V=0}$ is the zero-bias resistance and γ is the curvature, defined as

$$\gamma = \frac{\partial^2 I}{\partial V^2} / \frac{\partial I}{\partial V}. \quad (3.2)$$

For all zero-bias detectors, the dominating noise process at low incident power is Johnson noise, which has also been shown for SSDs specifically [17]. Johnson noise gives rise to a Gaussian-distributed rms noise voltage $V_n = \sqrt{4kTR_0}$ across the terminals, where k is Boltzmann's constant and T the physical temperature. An important figure of merit for a detector is the NEP, which represents the input power for which the output voltage equals the noise floor ($= V_n$). Thus, the NEP is found as

$$\text{NEP}_{opt} = \sqrt{4kTR_0} / \beta_{opt} \quad (3.3)$$

It is seen from (3.1) and (3.3) that increasing R_0 will increase β_{opt} and decrease NEP_{opt} . However, if R_0 is large, the RF mismatch may become significant. With a large mismatch, only a small amount of the incident power is actually absorbed by the diode. For sufficiently low frequencies the diode's zero-bias impedance Z_0 can be approximated by R_0 and the reflection coefficient Γ is

$$\Gamma = \frac{Z_0 - Z_s}{Z_0 + Z_s} \approx \frac{R_0 - Z_s}{R_0 + Z_s}. \quad (3.4)$$

where the absorbed power is $P_a = P_i(1 - |\Gamma|^2)$. Defining the unmatched voltage responsivity as $\beta_v = V_{det}/P_i$:

$$\beta_v = \beta_{opt}(1 - |\Gamma|^2) \quad (3.5)$$

In the same way, the NEP taking the mismatch into consideration is

$$\text{NEP}_v = \text{NEP}_{opt}/(1 - |\Gamma|^2) \quad (3.6)$$

From (3.4)-(3.6), it is clear that also the RF match needs to be considered when optimizing the design of the diode.

N-dependence in SSDs

An SSD can be designed with any number of channels in parallel. Assuming the I-V relations for the separate channels are identical and independent of the number of channels, conclusions can be drawn regarding the design of the SSD. If the current for one channel is $I_{N=1}(V)$, the current for N channels in parallel is $I_N(V) = NI_{N=1}(V)$. The zero-bias resistance is then $R_0(N) = R_{0,N=1}/N$. From (3.1), β_{opt} is then found as

$$\beta_{opt}(N) = \frac{1}{N}\beta_{opt,N=1} \quad (3.7)$$

since γ is independent of N . In the same way, $\text{NEP}_{opt}(N)$ is found from (3.3) as

$$\text{NEP}_{opt}(N) = \sqrt{N} \text{NEP}_{opt,N=1} \quad (3.8)$$

and the reflection coefficient Γ_N as

$$\Gamma_N = \frac{R_{0,N=1}/N - Z_s}{R_{0,N=1}/N + Z_s}. \quad (3.9)$$

Using Γ_N and (3.5)-(3.6), expressions for $\beta_v(N)$ and $\text{NEP}_{opt}(N)$ can be derived. The responsivity and NEP as a function of N , both matched and unmatched is plotted in Fig. 3.3 along with the absorbed power ratio $(1 - \Gamma_N^2)$. The $\beta_{opt,N=1}$, $\text{NEP}_{opt,N=1}$, $R_{0,N=1}$ and Z_s used for these plots were chosen arbitrarily. It is seen from β_{opt} and NEP_{opt} that for a matched SSD, $N = 1$ is clearly favorable. However, $N = 1$ causes a large R_0 and severe mismatch, only a few percent of incident power is absorbed. In the matched case, β_v decreases with increased N . However, NEP_{opt} decreases until reaching a minimum at a certain N . The minimum occurs for a lower N than for which $R_0 = 50 \Omega$.

This analysis shows that the design for optimal responsivity and NEP differs between the matched and unmatched case. It also shows that a minimum NEP_v can be expected for an optimum N .

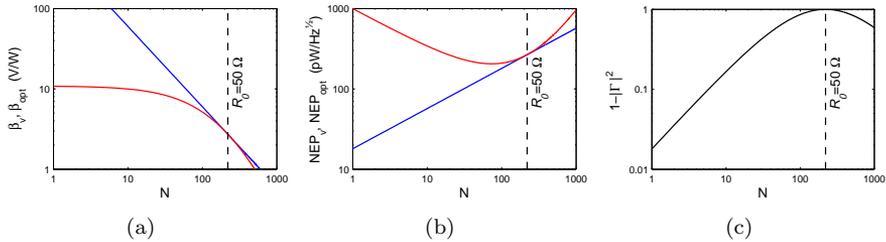


Figure 3.3: (a) β_v (blue) and β_{opt} (red) and (b) NEP_v (blue) NEP_{opt} (red) versus number of channels N . (c) Absorbed power ratio versus N . For a certain N , $R_0 = 50 \Omega$, indicated by the dashed vertical line.

3.3 Device fabrication

3.3.1 InAs SSDs

The design of the epitaxial structure, particularly the buffer, was crucial for successful fabrication of InAs SSDs. Examples of investigated designs are given in Fig. 3.4, together with SEM cross-sections of etched and passivated SSD trenches. The cross-section was made by fabricating long trenches and then breaking the substrate perpendicularly to the trenches.

Essentially, the buffer design is a trade-off between chemical stability and isolation. AlSb is known to be prone to oxidation [35] but offers good isolation whereas $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ is more stable but also more conductive [39]. In a pre-study of InAs SSD fabrication [Paper B], the buffer design illustrated

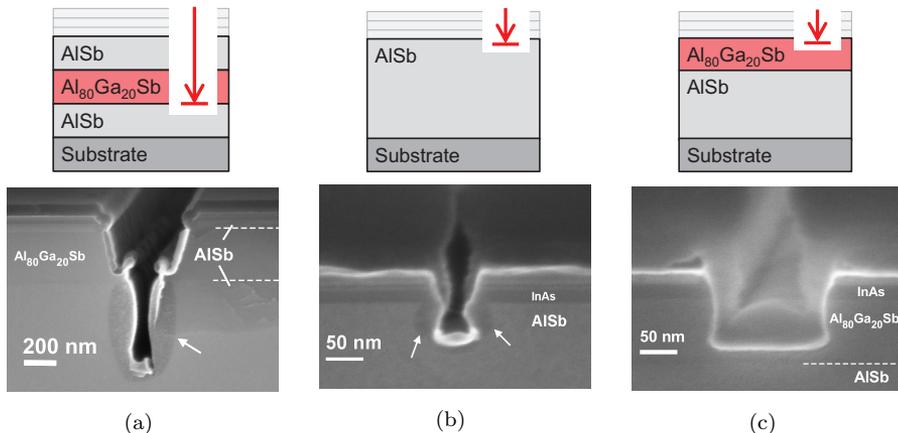


Figure 3.4: Three buffer designs explored in the development of the InAs SSD process: (a) AISb/AlGaSb/AISb buffer [Paper B], (b) pure AISb and, (c) AlGaSb/AISb buffer which was used in the final fabrication.

in Fig. 3.4(a) was used. The same buffer design has been successfully implemented in InAs/AISb HEMT fabrication [40]. In this design, a 250 nm $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ layer was sandwiched between AISb layers. In the pre-study, InAs SSDs were successfully fabricated by etching through the entire $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ layer. As shown in Fig. 3.4(a), there was a considerable growth of oxide in the AISb. For this reason, the etch is stopped inside the $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ layer in HEMT fabrication [40]. However, tests showed that if the etch was stopped in the $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ layer, the leakage through the residual $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ would make the resistivity of etched trenches $120 \text{ k}\Omega/\text{sq}$. Meanwhile, R_0 for the fabricated SSD was $1.6 \text{ M}\Omega$. To maintain a buffer resistance higher than R_0 , a sheet resistance of trenches $> 120 \text{ M}\Omega/\text{sq}$ was needed. The $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ would short-circuit an SSD. Therefore, the $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ layer was abandoned and the pure AISb buffer design in Fig. 3.4(b) investigated.

With a pure AISb buffer, as in Fig. 3.4(b), tests showed that the sheet resistance of trenches would be $75 \text{ M}\Omega$, and still cause a significant leakage in comparison to R_0 of the SSD. By designing the SSD with many channels and thus decreasing R_0 , the leakage current could be made less significant. However, the oxidation could not be overcome. The cross section SEM shown in Fig. 3.4(b) was made only minutes after the trench etch. Despite the sample being passivated with SiN_x , the oxidation was clearly visible. To avoid oxidation, an $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ layer was necessary in the SSD buffer design.

In the final buffer design, shown in Fig. 3.4(c), a 100 nm $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ -layer was re-introduced in the top part of the buffer. The trenches were etched just through the InAs channel and stopped in the $\text{Al}_{80}\text{Ga}_{20}\text{Sb}$ layer. As seen in Fig. 3.4(c), the stability was largely improved. The sheet resistance of trenches was $> 700 \text{ M}\Omega$. Hence, the isolation was more than enough for not degrading the device performance. Since the heterostructure in Fig. 3.4(c) was grown by a different vendor, the reason why the isolation was better than in the pure AISb buffer was likely different growth conditions. The epitaxial structure is

Cap layer	InAs:Te	50 Å
Protection Layer	InAlAs	40 Å
Barrier	Al ₈₀ Ga ₂₀ Sb	130 Å
Channel	InAs	150 Å
Metamorphic buffer	Al ₈₀ Ga ₂₀ Sb	1000 Å
Metamorphic buffer	AlSb	10000 Å
Buffer	GaAs	3000 Å
Smoothing layer	InAlAs	100 Å
Substrate	2' S.I GaAs (001)	

Figure 3.5: The developed epitaxial structure used for fabrication of the InAs SSDs. In the top part of the buffer as well as for the barrier, AlSb is exchanged for Al₈₀Ga₂₀Sb.

Table 3.1: Hall data of InAs and InGaAs SSD wafers. Measured in passivated regions where the cap layer had been etched away, similar to the active regions of the SSDs.

Sample	R_{sh} [Ω/sq]	n_s [10^{12} cm^{-2}]	μ [cm^2/Vs]
InAs	167	1.5	26000
InGaAs	480	0.9	15000

shown in detail in Fig. 3.5. Hall data for this structure is shown in Table. 3.1. Similar carrier concentration and mobility have previously been observed in similar non-intentionally doped InAs quantum wells [41].

The fabrication of the InAs SSDs was started by the evaporation of Pd/Pt/Au (200/200/600 Å) contacts and a subsequent anneal at 275°C. After that, metal pads were formed by evaporation of Ti/Au/Ti (200/3000/100 Å). Next, the cap layer was recessed in the active area of the device by first removing oxides with a hydrogen chloride/water solution. The recess etch itself was done with citric acid/hydrogen peroxide solution. After the recess followed the crucial trench formation, illustrated in Fig. 3.6. Trenches were patterned in ZEP520A resist by e-beam lithography. The trench was etched with a Cl:Ar inductively-coupled plasma reactive ion-etch process and stopped in the Al₈₀Ga₂₀Sb buffer just below the channel. Traditional resist removal techniques such as wet solvent processes or oxygen plasma were both inapplicable due to the risk of initiating oxidation. Instead, an NF₃ plasma was used to remove the resist *in situ*. Then, approximately 25 nm of silicon nitride (SiN_x) was deposited in a room temperature plasma-enhanced chemical vapor deposition process (PECVD). The SiN_x was grown *in situ*, without first exposing the sample to air, in order to temporarily passivate and encapsulate the trenches for the rest of the fabrication. The top-view SEM-picture in Fig. 3.7 shows an InAs in this state of the fabrication. After the trench formation, mesas were etched in a similar way as the trenches, but with the etch extended down to the substrate for maximum stability and isolation. The trenches were completely covered by an *in situ*-grown 180 nm thick SiN_x passivation layer deposited using PECVD at room-temperature. A cross-section of etched trenches is shown in 3.7. The etch was stopped just below the InAs channel. As a final step, openings in the

passivation for metal pads were defined.

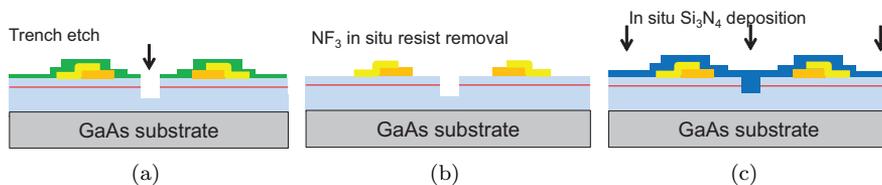


Figure 3.6: InAs SSD trench formation: (a) trench etch, (b) *in situ* resist removal, (c) *in situ* growth of SiN_x passivation. The red line represents the InAs channel.

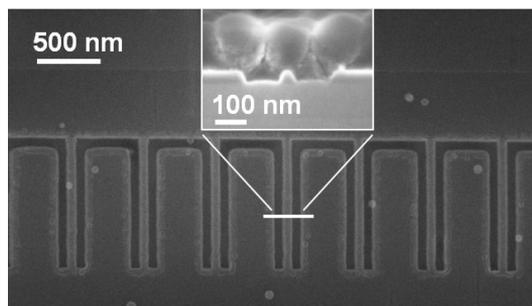


Figure 3.7: Top view SEM image of an InAs SSD after trench fabrication. The inset shows a SEM cross-section of a finalized SSD channel covered with 180 nm SiN_x passivation.

3.3.2 InGaAs SSDs

In contrast to InAs SSDs, the fabrication of InGaAs SSDs on an InAlAs buffer was not complicated by oxidation issues. The epitaxial structure was identical to the one used for InGaAs slot diodes; see Fig. 2.9. The same structure have been used for low-noise InP HEMTs [25]. First, mesas, ohmic contacts and metals pads were processed in the same way as for slot diodes, described in 2.2. The cap layer was etched away in the active area of the SSDs with a succinic acid/hydrogen peroxide solution. Trenches were pattern by e-beam lithography in ZEP520A resist. The trenches were etched with a Cl:Ar inductively-coupled plasma reactive ion-etch process just like the InAs SSDs. The resist was removed in a conventional way with wet solvents and ashing. 25 nm SiN_x passivation was grown in a room temperature plasma-enhanced chemical vapor deposition process. Finally, openings in the passivation were made for metal pads. Hall data from structures processed on the same sample as the InGaAs SSDs is shown in Table. 3.1. Similar values have been reported for the same epitaxial structure in [27]. As expected, both the carrier concentration and electron mobility were lower for InGaAs than for InAs.

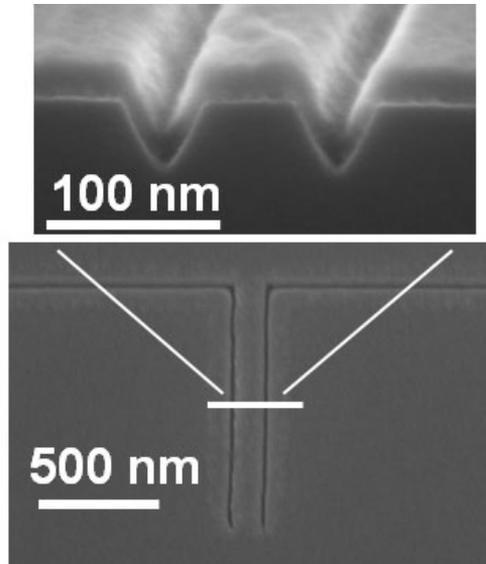


Figure 3.8: Top view and cross-section SEM image of a finalized InGaAs SSD

3.4 Characterization

3.4.1 DC measurements

I-V measurements of an InAs SSD and an InGaAs SSD are presented in Fig. 3.9 and Fig. 3.10, respectively. The presented I-V measurements were performed on the SSD which in RF measurements showed the lowest NEP_v of all measured devices in respective technology. For the InAs SSD, $N = 43$ and for the InGaAs SSD $N = 5$. Also shown in Fig. 3.9 is the asymmetric current I_{asym} for the corresponding devices, defined as $I_{asym} = I(|V|) + I(-|V|)$. In other words, I_{asym} represents how much higher the current is in forward bias compared to reverse bias.

The I-V characteristics of the InAs SSD is shown in Fig. 3.9(a). For this device, the current is only slightly higher in forward bias than in reverse bias. As shown in Fig. 3.9(b), I_{asym} is $\approx 60\mu\text{A}$ for $+0.5\text{ V}$. The total current is $\approx 1\text{ mA}$. While I_{asym} of the improved SSD is of the same order of magnitude as for other non-linear detectors such as Sb-based backward diodes [42], it constitutes only $\approx 6\%$ of the total current in the InAs SSD. This large parallel current is due to that the channel does not completely pinch in reverse bias. However, it is this small asymmetry that makes the InAs SSD a detector.

The I-V characteristics of the InGaAs SSDs is shown in Fig. 3.10(a). The I-V for InGaAs SSD is in many aspects different from the InAs I-V. First, the current in the InGaAs SSD starts to saturate for $\approx 0.1\text{ V}$. This saturation occurs also in $I_d - V_d$ measurements for $V_g = 0\text{ V}$ of InP HEMTs fabricated in the same heterostructure [29]. Second, the current level is more than a factor 100 higher in the InAs SSDs. Per channel, it is 15 times higher. However, asymmetry is stronger in the InGaAs device: Below saturation, I_{asym} in the

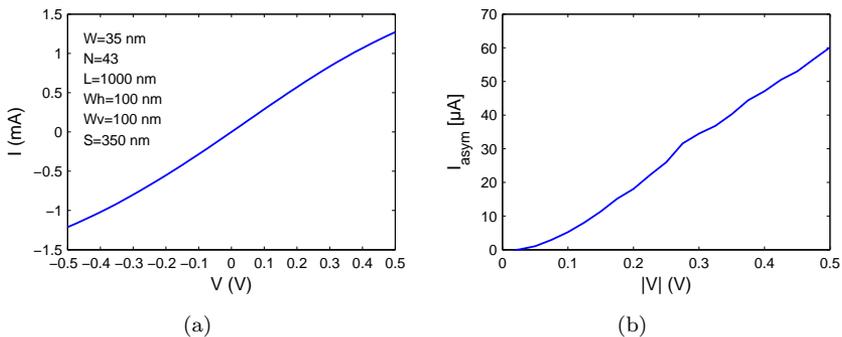


Figure 3.9: (a) I-V characterization of an InAs SSD and (b) the asymmetric current I_{asym} .

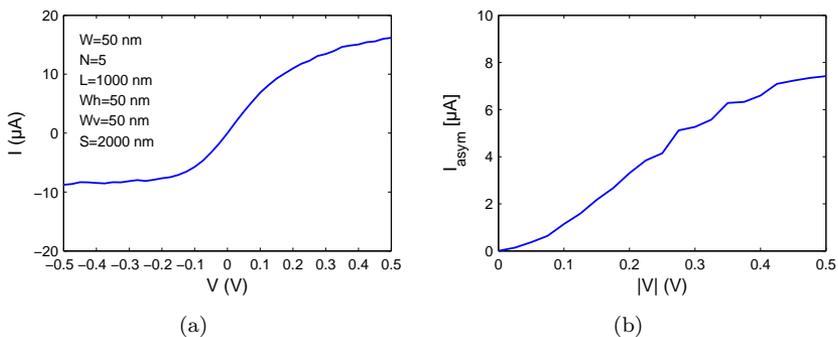


Figure 3.10: (a) I-V characterization of an InGaAs SSD and (b) the asymmetric current I_{asym} .

InGaAs SSD comprises $\approx 15\%$ of the total forward current.

Responsivity and NEP can be derived from measured I-V according to (3.1)-(3.3). The values in Table 3.2 have been derived from the I-V measurements presented in Fig. 3.9 and Fig. 3.10. In comparison to the InGaAs SSD, the InAs SSD has higher NEP_{opt} and much lower β_{opt} . However, the significantly lower R_0 makes the power transfer from a $50\ \Omega$ system easier with the InAs SSD than for the InGaAs SSD.

DC-measurements of R_0 and γ at zero bias as a function of W is shown in Fig. 3.11. For InGaAs devices, R_0 is many $k\Omega$ for small W , making matching difficult. Smaller W leads to higher γ in both InAs SSDs and InGaAs SSDs, reaching maximally $0.2\ \text{V}^{-1}$ and $2.5\ \text{V}^{-1}$, respectively. For comparison, zero-bias Schottky diodes and Sb-heterostructure diodes have γ of 26 and $47\ \text{V}^{-1}$ respectively, leading to the high responsivities observed with those diodes [7, 43].

Table 3.2: Detector characteristics of InAs and InGaAs SSDs derived from I-V measurements. Derived from the I-V characteristics shown in Fig. 3.9 and Fig. 3.10

	R_0 (Ω)	β_{opt} (V/W)	NEP_{opt} (pW/Hz $^{1/2}$)	β_v (V/W)	NEP_v (pW/Hz $^{1/2}$)
InAs SSD	350	18	200	11	210
InGaAs SSD	1800	14000	1.2	150	115

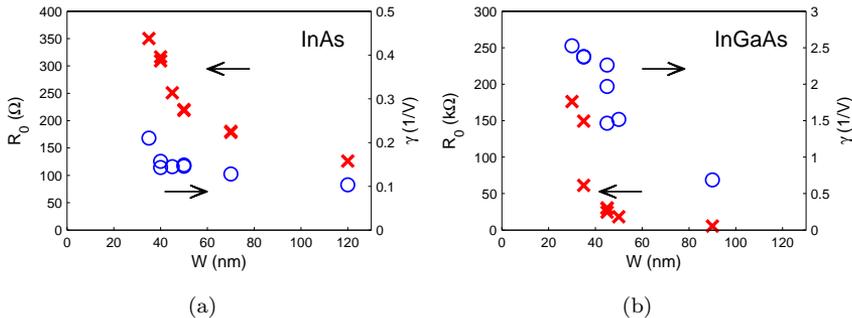


Figure 3.11: R_0 (crosses) and zero-bias γ (circles) versus W in (a) InAs SSDs and (b) InGaAs SSDs. Other design parameters according to Fig. 3.9 and Fig. 3.10.

3.4.2 Cryogenic DC measurements

I-V measurements were carried out on an InAs SSD at 6 K and compared to room temperature measurement [Paper D]. The InAs SSDs were fabricated as described in section 3.3.1, with the difference that the cap layer was not removed in this particular diode.

Hall measurements were performed on a sample processed like the SSD, but with the cap layer etched away. By etching away the cap, the transport properties in the 2DEG only were investigated. Table 3.3 shows how the sheet resistance R_{sh} is virtually unaffected upon cooling from 300 K to 77 K whereas the sheet carrier concentration n_s is halved and mobility μ doubled. The transport properties are not expected to differ significantly between 6 K and 77 K [41].

In Fig. 3.12(a), the diode current I versus applied voltage V is plotted at 300 K and 6 K. The resistance for small V increases upon cooling, from 2.8 k Ω to 6.9 k Ω . From the Hall measurements on the 2DEG showed in Table 3.3, the resistance is expected to stay about the same. A possible reason for the discrepancy is the geometry. At 6 K, charges on the trench sidewalls may deplete the channel further, thus narrowing the effective channel width. For larger V , current increases rapidly. This may be due to impact ionization.

β_{opt} versus V was calculated according to (3.1)-(3.3). At 300 K and 6 K, β_{opt} were 490 and 4400 V/W, respectively. Corresponding NEP_{opt} was 14 and 0.34 pW/Hz $^{1/2}$. Thus, the performance of the InAs SSD can be expected to improve upon cooling. This has been verified with RF measurements in InGaAs SSDs [11], but not so far in InAs SSDs.

Table 3.3: Hall measurements for InAs SSDs at 300 K and 77 K. The Hall sample was prepared like the InAs SSDs, except for the cap layer which was etched away to reveal the properties of the 2DEG.

	R_{sh} (Ω/sq)	n_s (cm^{-2})	μ (cm^2/Vs)
300 K	181	1.3×10^{12}	26000
77 K	175	6.3×10^{11}	57000

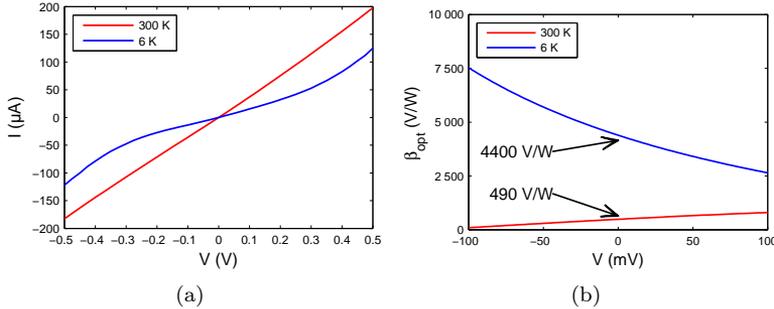


Figure 3.12: (a) I-V measurements and (b) derived β_{opt} for an InAs SSD at 300 K and 6 K.

3.4.3 On-wafer RF measurements

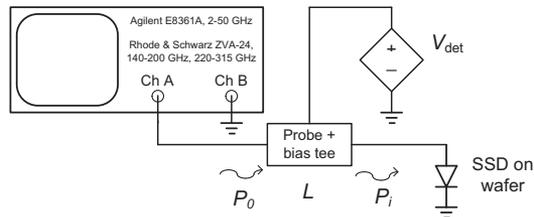


Figure 3.13: Schematic view of the setup for on-wafer characterization of InAs and InGaAs SSDs.

On-wafer measurements were performed using a vector network analyzer as the signal source. The setup is shown in 3.13. Different equipment was used for each of the three different bands (2-50, 140-220 and 240-315 GHz), all following the same principle: The power from the source was measured with a calorimetric power meter for each frequency setting. By subtracting the loss of the RF probes, the available power at the probe tip was found. The power incident to the device was $1.7 - 8.5 \mu\text{W}$, delivered by a 50Ω source. Resulting DC detection voltage was measured through a bias-tee with a high-resistance load. The unmatched responsivity β_v was found as the ratio $\beta_v = V_{det}/P_i$.

The influence of design parameters W on responsivity and NEP was studied at 50 GHz. Typical designs for InAs and InGaAs SSDs are shown in

Table 3.4: Typical SSD designs fabricated in InAs SSDs and InGaAs.

Material	W (nm)	N	L (nm)	W_h (nm)	W_v (nm)	W_{mesa} (μm)
InAs	45	43	1100	100	100	30
InGaAs	45	5	1100	50	50	15

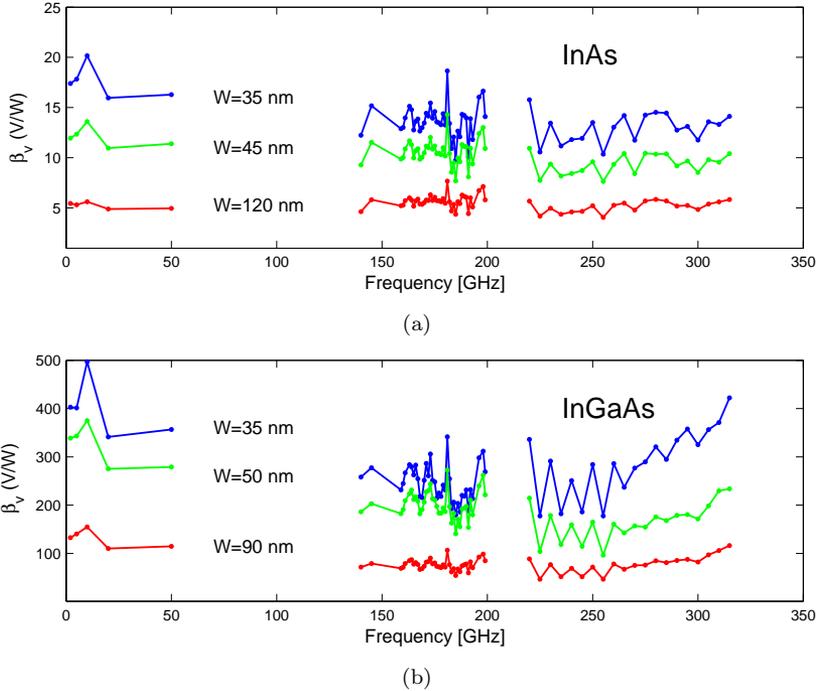
Figure 3.14: β_v derived from on-wafer RF measurements for (a) InAs SSDs and (b) InGaAs SSDs.

Table 3.4. Based on these designs, W -dependence was tested by measuring on different SSDs, varying only W . For InAs SSDs, also N - and L - dependence was investigated.

Fig. 3.14(a) shows β_v as a function of frequency for InAs SSDs, with three different W . The ripple in the data is attributed to the fact that when P_0 was measured with the power meter, the source saw a different load than when the SSDs were measured. Notably, no strong roll-off is observed in the measured band up to 315 GHz, in particular for $W = 45$ nm and $W = 120$ nm. The highest β_v is achieved for $W = 35$ nm, for which $\beta_v > 10$ V/W in the measured band. For larger W , β_v is lower, but shows very similar frequency dependence. Fig. 3.14(b) shows the corresponding data for InGaAs SSDs. Generally, β_v in the InGaAs SSDs is higher than in the InAs SSDs. The difference in β_v between the two materials is consistent with the observation in section 3.4.1 that InGaAs SSDs have a more nonlinear I-V relation than InAs SSDs.

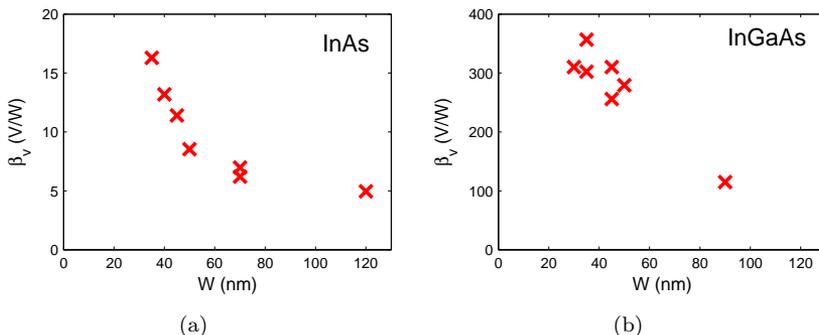


Figure 3.15: β_v at 50 GHz. For (a) InAs SSDs, (b) InGaAs SSDs.

Design dependence

W -dependence

The channel width W is an important design parameter in the SSD. A detailed study of how β_v depends on W is shown in Fig. 3.15 for InAs and InGaAs SSDs. The measurement was performed at 50 GHz with an incident power of $3.2 \mu\text{W}$. Clearly, β_v was higher for small W . The exact dependence on W is more easily understood by studying β_{opt} , which is done in Fig. 3.16. For InAs SSDs, β_{opt} was found as $\beta_{opt} = \beta_v / (1 - |\Gamma|^2)$, where Γ was the measured reflection coefficient. For InGaAs SSDs, $R_0 \gg 1 \text{ k}\Omega$, thus Γ was close to 1 and hard to measure. Instead Γ for InGaAs SSDs was found from DC-measurements according to (3.4). For both materials the highest β_{opt} , 34 V/W and 270 kV/W for InAs and InGaAs respectively, was achieved for the smallest W investigated.

Shown in 3.16(a) is also β_{opt} as derived from I-V characterizations. These derivations were done according to (3.1)-(3.3) by fitting a 5th-order polynomial to measured I-V characteristics for $V \in [0.2, 0.2] \text{ V}$. The β_{opt} derived in this way matched the measured β_{opt} closely, both in a relative and absolute sense. This opens for further understanding of the effect of scaling W by studying different contributions to β_{opt} , based on (3.1). For InAs SSDs, from $W = 120$ to 35 nm, β_{opt} increased from 6.5 to 34 V/W, corresponding to a 420% increase. In Fig. 3.11, DC analysis showed that the increase in R_0 was 180 % (from 126 to 350 Ω) and in γ , 100 % (from 0.1 to 0.2 V^{-1}). The increase in γ is important since it shows that the increase in β_{opt} was not merely due to an increased R_0 , but also an increased non-linearity of the current in each channel. As explained in section 3.2, an increased R_0 increases β_{opt} , but will also increase the mismatch. For InGaAs SSDs, from $W = 90$ to 20 nm, β_{opt} increased from 3.2 to 270 kV/W, and γ 260 %.

NEP_v and NEP_{opt} versus W were calculated according to (3.3) and (3.6) and are plotted in Fig. 3.17. For InAs SSDs, the lowest NEP_v and NEP_{opt} were 150 and 70 $\text{pW}/\text{Hz}^{1/2}$, respectively. For InGaAs SSDs, corresponding values were 60 and 0.3 $\text{pW}/\text{Hz}^{1/2}$. $\text{NEP}_v = 64 \text{ pW}/\text{Hz}^{1/2}$ has been reported for InGaAs SSDs elsewhere, for a design with $N=2000$ [17]. Here, similar NEP_v is achieved with $N=5$.

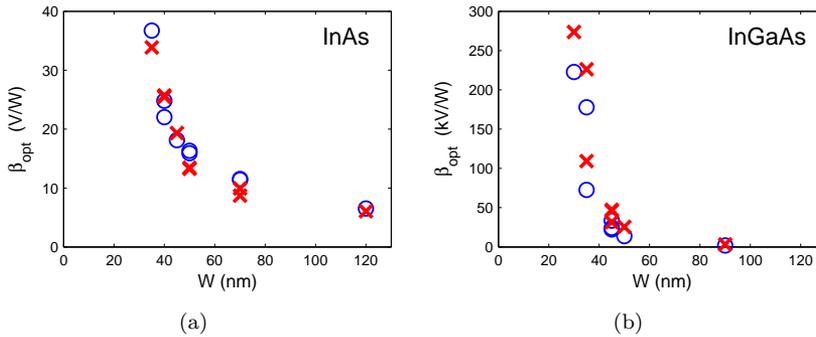


Figure 3.16: β_{opt} versus W , as measured (crosses) and calculated from I-V measurements (circles). For (a) InAs SSDs, (b) and InGaAs SSDs.

In InAs SSDs, the lowest NEP_v and NEP_{opt} are achieved for the lowest W . Scaling of W may thus further improve the device. In this study, both the minimum NEP_v and NEP_{opt} were considerably lower in InGaAs SSDs than in InAs SSDs. For InGaAs SSDs, $W = 50$ nm optimal in terms of NEP_v . For smaller W , the large increase of R_0 caused the noise to increase.

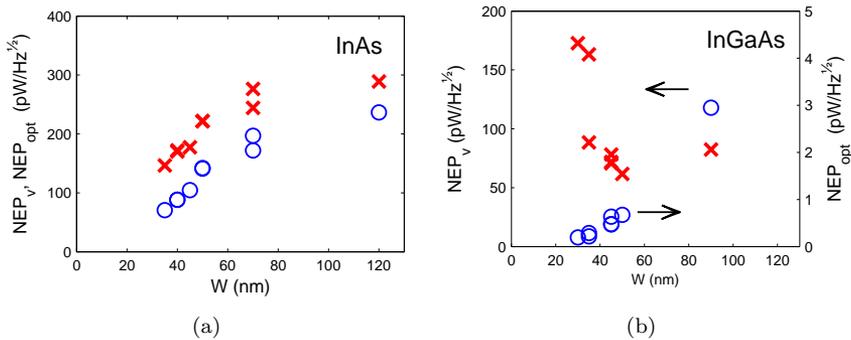


Figure 3.17: NEP_v (red crosses) and NEP_{opt} (circles) versus W measured at

N -dependence

In InAs SSDs, also the N dependence was studied, with results shown in Fig. 3.18. From the $N=43$ device, $R_{0,N=1}$ and $\beta_{opt,N=1}$ was extracted. Using (3.7)-(3.9), $\beta_v(N)$ and $\beta_{opt}(N)$, as well as $NEP_v(N)$ and $NEP_{opt}(N)$ could be plotted in Fig. 3.18 and compared to measurements. The agreement is good, with some discrepancy for small N . It is shown that as NEP_{opt} increased for higher N , NEP_v decreased. This is explained by the decreased R_0 for large N , resulting in reduced mismatch. Fig. 3.18(b) further suggests that increasing N beyond 40 has little effect on NEP_v even if the expected minimum occurs for $N = 70$.

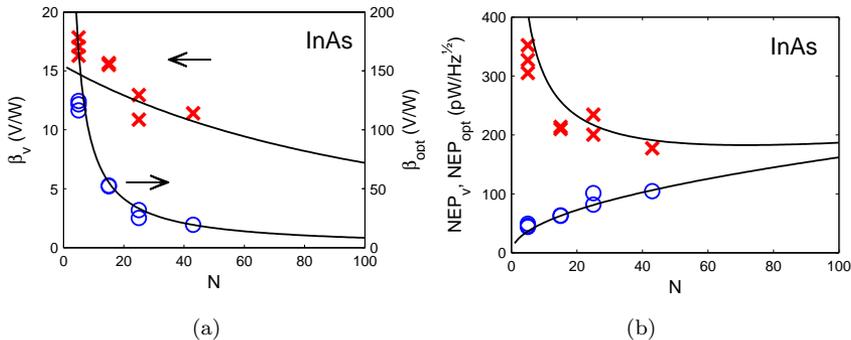


Figure 3.18: β_{opt} and NEP_{opt} (circles), and β_v and NEP_v (crosses) versus N , measured at 50 GHz. The theoretical relation (black lines) was derived from the value of $\beta_{opt,N=43}$ and $R_{0,N=43}$.

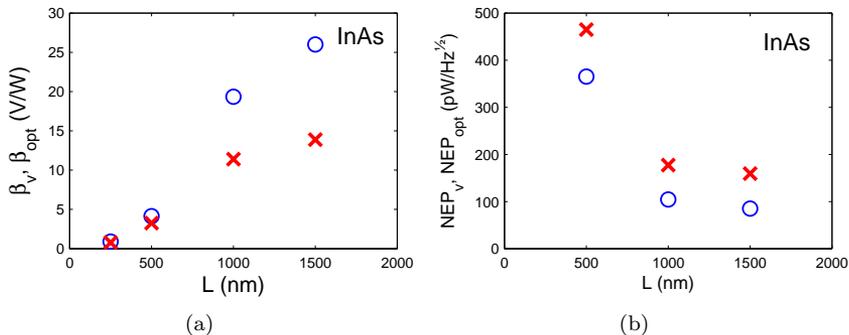


Figure 3.19: β_{opt} and NEP_{opt} (circles), and β_v and NEP_v (crosses) versus L . Measured at 50 GHz.

L -dependence

The last design parameter investigated was the L -dependence, shown in Fig. 3.19. Increased L increases β_{opt} and decreases NEP_{opt} . Also β_v and NEP_v are improved, but to a lesser extent due to increased R_0 and thus increased mismatch.

3.4.4 Free-space RF measurements

To investigate if the SSDs could function as a detector at 600 GHz, a free-space setup was used, shown in Fig. 3.20. A measurement at 200 GHz was conducted in a similar way, for comparison with the on-wafer results. A detector was built from an InAs SSD contained within a circularly polarized spiral substrate antenna [44], for which the simulated impedance was plotted in Fig. 2.12. The SSD design was $N = 11$, $W = 65$ nm, otherwise according to Table 3.4. From I-V characterization, $\beta_{opt} = 53$ V/W is expected. A silicon lens was placed firmly against the backside of the substrate with the SSDs. The output voltage was measured with a lock-in amplifier, thus presenting a high DC-load.

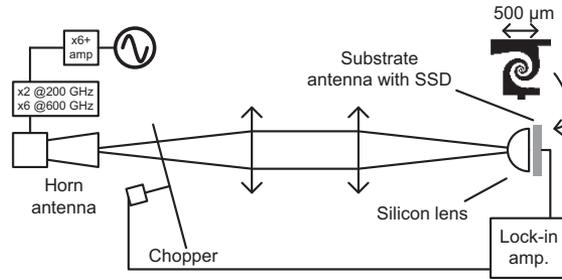


Figure 3.20: The setup used for free-space measurements at 200 and 600 GHz.

On the transmitter side, the vertically polarized beam was radiated through a conical horn antenna. By replacing the receiver with an Erickson PM4 power meter with a horn antenna, the incident power was measured. At 200 GHz and 600 GHz the power in pulses was 1.15 mW and 7 μ W, respectively. The responsivity of the system at 200 GHz and 600 GHz was 2.1 V/W and 0.70 V/W, respectively. Compensating for polarization mismatch (50%) and the mismatch between R_0 and the antenna radiation resistance ($\approx 50\%$), β_{opt} is calculated to 8.4 V/W and 2.8 V/W at 200 and 600 GHz, respectively.

In the on-wafer RF measurements, measured β_{opt} matches the one calculated from I-V measurements, see Fig. 3.16. The discrepancy between the β_{opt} measured in the free-space setup at 200 GHz and the β_{opt} calculated from I-V measurements may be due to other losses than what was compensated for. For example, reactive contributions was not considered when calculating the antenna mismatch, nor the fact that not all incident power is coupled into the antenna. However, it was confirmed that InAs SSDs can function as detectors at 600 GHz, with a responsivity of the same order of magnitude as for 200 GHz. This find motivates further investigation of InAs SSD detection at 600 GHz and higher frequencies.

3.4.5 InAs SSD imaging

With the same SSD used for free-space detection ($N = 11$, $W = 65$ nm), the imaging setup in Fig. 3.21 was used to image an RFID card. The imaging was performed at 200 GHz with an output power of 1.15 mW. The beam was focused on the RFID card shown in Fig. 3.22. The card was moved in a grid pattern and the output voltage V_{det} in the SSD was recorded for every point. Plotting the signal strength versus position resulted in the image shown in Fig. 3.22. The plastics of the card is transparent to the radiation and thus imaged bright, while the metal antenna and microchip are reflective and imaged dark.

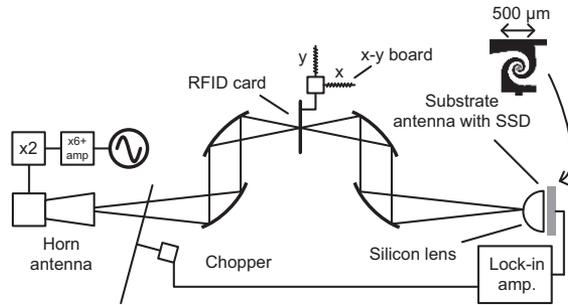


Figure 3.21: Setup used for imaging at 200 GHz with an InAs SSD. Spherical mirrors were used to focus the beam.

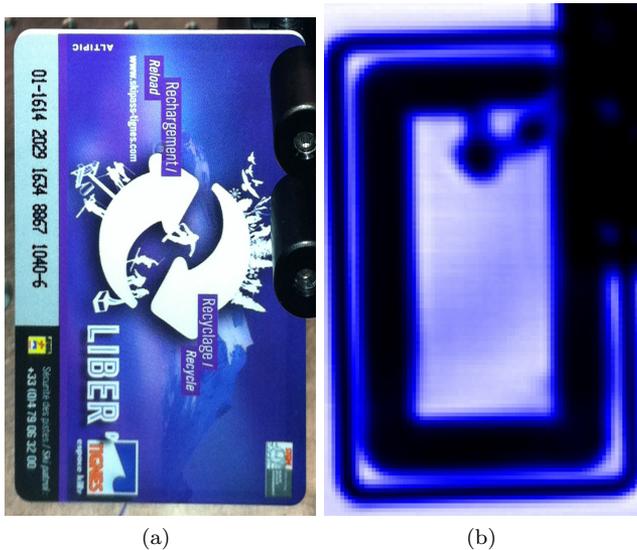


Figure 3.22: (a) An RFID card and (b) its image when irradiated by 200 GHz waves and detected by the InAs SSD.

3.4.6 Characterization summary

DC-characterization of InAs SSDs were performed in which a relatively small nonlinearity was observed. Upon cooling to 6 K, this nonlinearity increased compared to at 300 K, increasing β_{opt} tenfold.

InAs and InGaAs SSDs were characterized as room-temperature detectors on-wafer in the range 2-315 GHz, in which no strong roll-off of responsivity was observed. A comparison of different designs were made at 50 GHz. It was shown that for the range of designs tested, NEP_v benefits from larger L and smaller W . For InAs SSDs, larger N will not reduce NEP_v significantly. For InGaAs, larger N may lower NEP_v .

For InAs SSDs, measured at 50 GHz, the highest β_v and lowest NEP_v observed were 17 V/W and 150 pW/Hz^{1/2}, respectively. For the same device, the R_0 was 350 Ω , making the mismatch fairly low. With a conjugate match,

34 V/W and 70 pW/Hz^{1/2} is expected.

InGaAs SSDs were studied in parallel. Compared to InAs SSDs, InGaAs SSDs are more resistive and suffer from a larger mismatch, but also have a larger γ . The lowest NEP_v observed at 50 GHz when measured a 50 Ω source was 60 pW/Hz^{1/2}, for a device with $N =$. Corresponding β_v was 280 V/W. Similar NEP_v has been observed in InGaAs previously, then with $N = 2000$ [17].

A free-space detector was designed and fabricated from an InAs SSDs. The responsivity of the detector was 2.1 V/W and 0.70 V/W at 200 GHz and 600 GHz, respectively. Several losses not compensated for may explain why the responsivity from free-space characterization was lower than than in corresponding DC and on-wafer RF measurements. Furthermore, the free-space experiment showed that the InAs SSD operated up to 600 GHz.

Finally, an imaging experiment was performed. An RFID card was imaged at 200 GHz using InAs SSDs.

Chapter 4

Conclusions and future work

This thesis describes the fabrication and characterization of InGaAs slot diodes for THz emission, and InAs SSDs for THz detection, both at room-temperature conditions. Also, the more established InGaAs SSDs were studied thus allowing to benchmark with the InAs SSDs.

InGaAs slot diodes were designed in an epitaxial InGaAs heterostructure with a lateral design according to MC simulation results [21]. I-V measurements of fabricated slot diodes at 300 K were well reproduced by MC simulations which predicted emission around 1 THz. Trap-related phenomena were observed in I-V measurements on slot diodes at 6 K. Despite the fact that MC simulations predicted an output power of 50 μ W at 0.8 THz or higher, no THz emission was detected from slot diodes in measurements up to 1 THz with a noise floor of 10 nW.

In future investigations of THz emission in InGaAs slot diodes, emission at higher frequencies should be investigated. Since electron mobility increases upon cooling, cryogenic emission experiments may be rewarding.

InAs self-switching diodes have been fabricated and characterized as detectors for the first time. The responsivity of InAs SSDs was measured on-wafer in the range 2-315 GHz, in which no roll-off of responsivity was observed. The highest responsivity and lowest NEP observed were 17 V/W and 150 pW/Hz^{1/2}, respectively, measured at 50 GHz with a 50 Ω source and no matching network. With a conjugately matched source a responsivity of 34 V/W and NEP of 65 pW/Hz^{1/2} are expected, based on S-parameters and responsivity as measured with a 50 Ω source. In a free-space detection experiment, an InAs SSD detector with a substrate antenna was demonstrated at 600 GHz. For InGaAs SSDs, the lowest noise equivalent power when measured at 50 GHz with a 50 Ω source was 60 pW/Hz^{1/2} and the responsivity 280 V/W. Up to at least 315 GHz, the maximum frequency in the on-wafer measurements, the InGaAs SSDs outperform the InAs SSDs in terms of responsivity and NEP. However, in the THz range, InAs SSDs may challenge both InGaAs SSDs and other detector technologies.

An experimental study of how the design influences the SSD detection performance was reported for the first time. Also, it was successfully shown

that DC measurements can be used to predict the responsivity of SSDs.

This thesis has demonstrated the feasibility of InAs SSDs for THz detection. Compared to other detectors, there is still much improvement to be done in order to enhance responsivity and reduce NEP. However, the potential for detection above 1 THz is there, and with improved technology, optimized design (including antenna) and adequate measurements, InAs SSD technology may become a viable detector for THz applications. Since SSDs can be fabricated in the same heterostructure as HEMTs, MMIC integration may be explored.

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Paper A

Terahertz Detection in InAs/Al_{0.8}Ga_{0.2}Sb Self-Switching Diodes at Room Temperature and Zero Bias

A. Westlund, P. Sangaré, G. Ducournau, P-Å. Nilsson, C. Gaquière, L. Desplanque, X. Wallart, J. Grahn

Manuscript, May 2013.

Paper B

Fabrication and DC characterization of InAs/AlSb Self-Switching Diodes

A. Westlund, G. Moschetti, H. Zhao, P-Å. Nilsson, J. Grahn

IEEE 24th International Conference on Indium Phosphide & Related Materials, IPRM, pp. 65-68, Aug 2012

Paper C

Fabrication and Characterization of InGaAs/InAlAs Slot diodes

A. Westlund, P-Å. Nilsson, J. Grahn

37th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe, WOCSDICE, May 2011

Paper D

Cryogenic DC Characterization of InAs/Al_{0.8}Ga_{0.2}Sb Self-Switching Diodes

A. Westlund, G. Moschetti, P-Å. Nilsson, J. Grahn, L. Desplanque, X. Wallart

IEEE 25th International Conference on Indium Phosphide & Related Materials, IPRM, May 2013