A SiGe 8-Channel Comparator for Application in a Synthetic Aperture Radiometer

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***Abstract*— We present a high-speed low-power 8-channel comparator tailored for the application of sampling antenna signals in a cross-correlator system for space-borne synthetic aperture radiometer instruments. Features like clock return path, per-channel offset calibration and bias current tuning make the comparator adaptable and gives the possibility to adjust the comparator for low power consumption, while keeping performance within the requirements of the cross-correlator system. The comparator has been implemented and fabricated in a 130-nm SiGe BiCMOS process. Measurements show that the comparator can perform sampling at a rate of 4.5 GS/s with a power consumption of 48 mW/channel or 1 GS/s with a power consumption of 17 mW/channel.**

I. Introduction

Earth observation in the microwave region can be used for studies of moisture and temperature distributions in the atmosphere. The cloud penetrating properties at microwave wavelengths, not achievable in visible or infrared spectrum, enable a way to study phenomena occurring within cloud formations. Two instruments of this kind have previously been proposed; the Geostationary Atmospheric Sounder (GAS) [1] and the Geostationary Synthetic Thinned Aperture Radiometer (GeoSTAR) [2]. Both of these instruments are supposed to operate from geostationary earth orbit (GEO), which gives advantages like continuous and almost full hemisphere coverage. The distance to earth from GEO and the relatively large wavelengths require large aperture to retain any kind of useful spatial resolution. This is a drawback, since sending very large parabolic dish antennas into space can be very challenging, if not impossible. The solution proposed for these instruments is using an aperture synthesis approach. An array of small antennas mounted on foldable booms are used for emulation of a larger aperture. This way the same resolution can be retained without the need for large single-dish antennas. Additionally a synthetic aperture approach captures an entire image in one go, obviating the need for scanning. A drawback of the aperture synthesis approach is that it requires more signal processing. Signals from the antennas have to be pair-wise cross-correlated before sent back to earth, in order to reduce the otherwise immense data bandwidth required of the downlink.

A cross-correlation system is currently under development. A digital 64-channel 1-bit cross-correlator ASIC has previously been designed and implemented as a concept demonstrator [3]. A new 1-bit cross-correlator ASIC with 128 differential input channels is currently being developed. Sampling of the analog signals in these correlator systems is to be performed using the comparator presented in this work. Sec. II will present the implementation of the comparator, while Sec. III will present simulation and measurement results. Finally, conclusions are presented in Sec. IV.

II. Comparator Implementation

The decision to go for a custom design for the comparators on the correlator system was based on several factors. First, power consumption was very important. For a correlator system with hundreds of input channels, especially considering the extra difficulty involved in power delivery and cooling on satellites, power efficiency is a key parameter. A custom design can be tailored to the specific requirements of the cross-correlator application within a strict power budget. Extra features such as input offset calibration, supply current tuning and clock return path can be added. Finally, going for a custom design gives the possibility to make an 8-channel design, which limits power consumption overhead and reduces board design complexity compared to a single-channel alternative. Also, the 8-channel design with one clock path matches the input bank pattern used for the previously constructed digital cross-correlator ASIC, which has one clock input for every eight data inputs. The same input bank system is also to be used for the new digital cross-correlator ASIC that is under development. The clock signal will be generated from a common clock source and split up to all comparators. The clock output of the comparator will then be routed alongside the data outputs to the digital cross-correlator input pins.

The comparator has been implemented in a high-speed 130-nm SiGe BiCMOS process, with a maximum cutoff frequency, f_T, of 230 GHz. The choice of a BiCMOS process was due to the good device matching, giving an easier implementation of a high-precision low-power comparator without a need for automatic offset cancelation techniques [4]. The entire design is realized using bipolar/HBT NPN transistors. The SiGe HBT process has an advantage over Si BJT when it comes to space applications in that it is more robust against current gain degradation due to neutron radiation [5]. Furthermore, similar to Si BJTs, SiGe HBTs show only minor degradations from ionizing radiation [6]. A Gilbert cell based mixer has previously been demonstrated to have lower power consumption and better noise figure in a bipolar SiGe process compared to a CMOS process with almost identical designs in both cases [7].

A block diagram of the comparator is shown in Fig. 1. A 100-Ω LVDS-style termination is used for each differential

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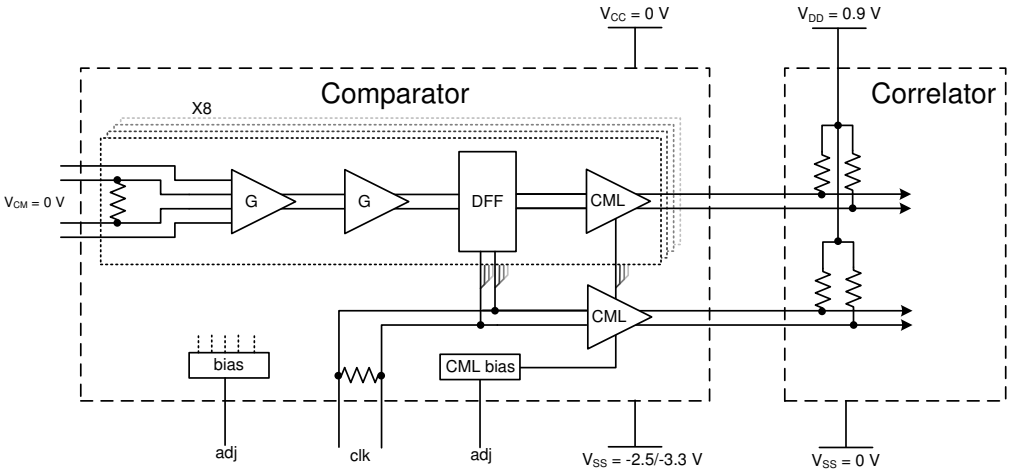


Fig. 1. Comparator schematic with intended connectivity to a digital cross-correlator ASIC.

input pair. These are followed by two amplification steps, a D-flip-flop and a CML output driver. Two pins for current mirror bias control are included. The first pin controls amplifiers and latches. The second pin controls the current for the CML output stage. This way performance and power consumption of the comparator can be tuned separately from the drive strength and, hence, the output swing of the CML stage. Additionally, the performance and power consumption can be adjusted by changing supply voltage. The comparator is designed to operate between -3.3 and -2.5 V. The negative supply voltage in combination with the CML-type output means that the comparator and the digital cross-correlator ASIC share a common ground and can be connected without any additional level-translation circuitry. A CML termination to V_{DD} of the digital correlator is all that is required, making for a simpler connection.

The two input amplification stages are depicted in Fig. 2. The first stage consists of a Gilbert gain cell [8] (within the dashed marker), an extra set of inputs connected in parallel with the ordinary inputs and emitter followers on all four inputs. Gilbert gain cells were used because of their flat frequency response. The extra inputs are to be used for offset calibration. A voltage applied across these inputs, inverse to the input offset, will cancel out the offset voltage seen at the latching stages. The emitter followers move the input range above ground level so that ground can be used as default common-mode level. An input swing of around 100 mV for the cross-correlator system can be expected. The second amplification stage consists of only the Gilbert gain cell without extra inputs and emitter followers. The Gilbert gain cell operates as a current amplifier. The current amplification (Eq. 1) is set by the ratio between bias currents in the inner and outer transistor pairs, I_E and I_B. The bandwidth (Eq. 2) of the amplification stage is determined by the transistor cutoff frequency and the current amplification, A_I.

$$A_I = (1 + \frac{I_E}{I_B}) \tag{1}$$

$$f_{3dB} = \frac{f_T}{A_I} \tag{2}$$

Careful considerations have to be made when trading amplification for available bandwidth. For the comparator presented in this work, the inner and outer bias currents are the same, making for a current gain of 2. The cutoff frequency of the transistors is also dependent on bias current. Additionally, the voltage gain (Eq. 3) of the amplifier is dependent on the current gain, the load resistors, R_L, and the emitter degeneration

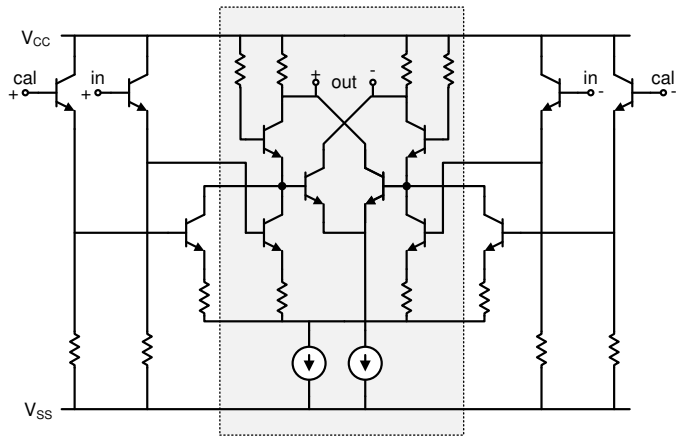


Fig. 2. Gilbert gain cell with emitter followers and calibration pins.

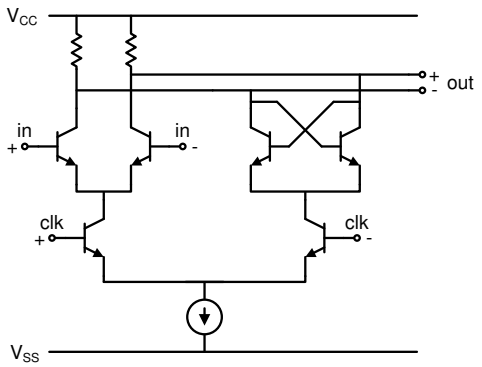


Fig. 3. Latch.

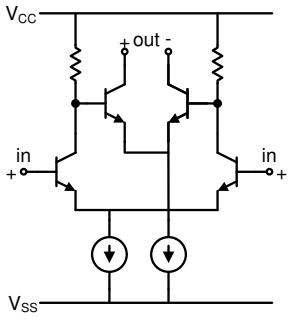


Fig. 4. CML output stage with preamplifier.

resistors, R_E. A design with two amplification steps was selected to multiply amplification.

$$A_v = \frac{R_L}{R_E}(1 + \frac{I_E}{I_B}) \tag{3}$$

Two latches (Fig. 3) form the D-flip-flop. When the positive clock input is in a high state, the latch is transparent and the differential gain stage on the input is driving the output. When the clock is low, the cross-coupled transistor pair pulls the outputs to logical one or zero depending on the voltage differential previously driven by the input stage. The reason for including a complete flip-flop stage instead of only latching functionality for the comparator is the relatively high speed combined with the fact that several inputs arriving from a number of comparators have to be phase matched for the final application. The flip-flop approach will hold data signals stable for an entire clock period, making it easier to correctly match the timing of the inputs.

The CML output stage is shown in Fig. 4. A differential gain stage works as preamplifier for the output driving transistor pair. The bias current for both stages is controlled by the CML bias control pin, although the output transistor pair has a considerably higher current.

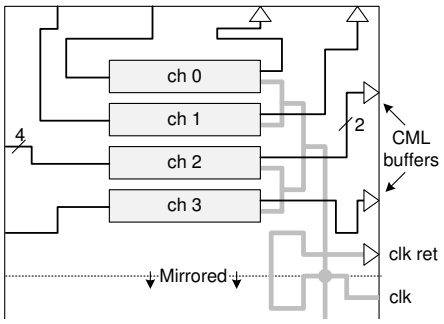


Fig. 5. Signal and clock path layout.

Common centroid design practices were used for all differential signal paths to reduce offsets. Resistances are implemented as polysilicon sheet resistors. Length matching between signal paths for the eight different channels and for clock paths were used for reduction of timing skews, as shown in Fig. 5. Termination resistors are placed adjacent to the input pads and CML buffers are placed close to the output pads.

The die in Fig. 6 has an area of 1.3 x 1.5 mm^2. Offset calibration pins are placed on either side of the signal input pins and one V_{CC}/V_{SS} pin is also placed between each input channel in order to increase channel crosstalk isolation.

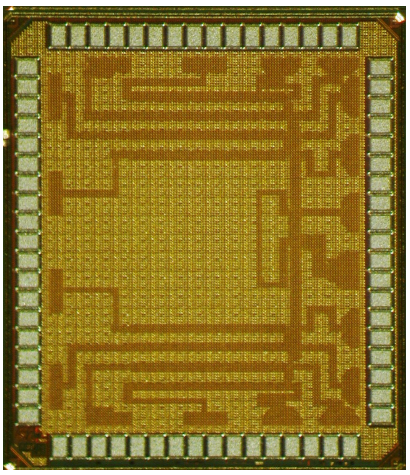


Fig. 6. Die photo of comparator.

III. Results

A. Simulation results

Simulations have been performed on RC-extracted netlists. The frequency response suggests bandwidths of 3.3 and 2.1 GHz and gains of 42 and 33 dB for supply voltages of -3.3 and -2.5 V, respectively, in a typical corner case.

Monte Carlo simulations at 1 GS/s using a -3.3-V supply were performed to find the input offset variation. Results suggest that input offsets of up to 10 $\mathrm{mV_{p-p}}$ are to be expected when no offset calibration is performed. This demonstrates why the extra offset calibration pins are important; in the cross-correlator system the accuracy might have to be calibrated down to around 1 mV.

B. Measurement results

Tests have been performed on a naked die bonded to a carrier board (Fig. 7). All tests were performed at a controlled temperature of 25°C. Calibration of the test setup was performed prior to testing, ensuring consistent input power to the carrier over the measured frequency ranges. Both data and clock inputs are driven as sine waves by frequency synthesizers. The power consumption and timing test results are listed together with other device parameters in Table I.

Two modes of operation have been used during testing; one low-power (LP) mode where the minimum requirement was a 1-GHz sampling frequency, and one high-performance (HP) mode where maximum sampling frequency within reasonable component stress was the objective. The LP mode uses -2.5 V supply, while the HP mode uses -3.3 V. Both modes have the output drivers tuned, using the CML bias, for a 200-mV swing over 100-Ω terminations. Due to constraints in the test setup—only 50-Ω terminations could be used—all tests are performed with a corresponding 100-mV output swing.

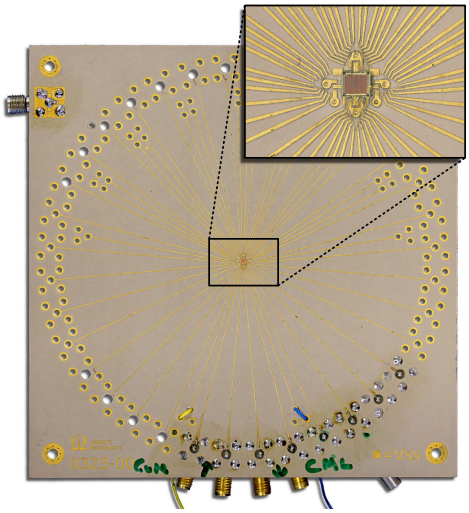
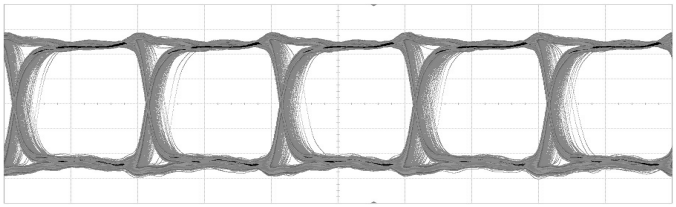
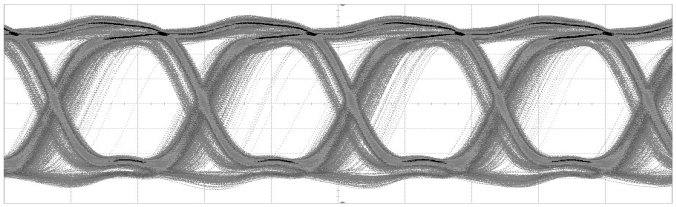


Fig. 7. Comparator test substrate.



(a) LP mode at 1-GHz sampling frequency.



(b) HP mode at 4.5-GHz sampling frequency.

Fig. 8. Eye diagrams of data output.

Rise and fall times, between 10% and 90% of peak, for both clock and data outputs were measured using a 1-GHz clock and a 300-MHz input signal. Rise and fall times for the clock return are somewhat larger than those of data outputs. Halving the clock frequency severely impacts rise and fall times, suggesting that much of this difference is due to the slope of the clock input's sine wave. The time skew between the clock return path and data output was also measured; this skew must be considered when matching the lengths of the return paths in the correlator implementation.

Data output eye diagrams for two operating cases are shown in Fig. 8. In Fig. 8(a), where the LP mode is used, a clock signal of 1 GHz is used for sampling an 80-$\mathrm{mV_{p-p}}$ single-ended input (other terminal tied to gnd) sine wave of 325 MHz. In Fig. 8(b), where the comparator, in HP mode, is clocked at 4.5-GHz, a 1.5-GHz input signal is used. Some of the samples take extra time to be triggered due to sampling close to zero crossing of the input sine, and can be seen as delayed transitions occurring within the eye opening. At higher clock frequencies, these transitions will increase in number.

TABLE I

DEVICE SUMMARY

Process	130-nm SiGe BiCMOS
Supply voltage	-2.5 to -3.3 V
Size	1.9 mm^2
Number of channels	8
Data output rise/fall time	99/95 ps @ HP, 176/168 ps @ LP
Clk return rise/fall time	171/165 ps @ HP, 189/182 ps @ LP
Data/clk output timing skew	90 ps @ HP, 103 ps @ LP
Power consumption	48 mW/channel @ HP, 17 mW/channel @ LP

In the HP mode, the comparator core draws 93 mA of current from the ground line. The nine CML outputs, which are terminated to a 0.9-V supply with a 200-mV signal swing over a 100-Ω termination, would consume an additional 18 mA. In total, this amounts to a power consumption of 382 mW, which is close to 48 mW/channel. In the LP mode, the core consumes only 31.2 mA, which for the same output drive strength means a total of 140 mW, or 17 mW/channel. For a correlator system with 256 input channels and 32 comparators, the total power consumption for signal sampling in LP mode would be 4.3 W, which is well within the range manageable for space applications.

IV. CONCLUSION

A high-speed low-power 8-channel comparator to be integrated in space-borne cross-correlator systems has been presented. Measurement results confirm that the comparator will be a good candidate for the task of sampling input signals. Bias control, supply voltage scaling and offset calibration make it possible to tune the comparator to within required specifications for such systems. Extra features such as clock return path and CML output also make the comparator suitable for integration within the system.

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