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Multilevel Inverter Topology Survey

Master of Science Thesis in Electric Power Engineering

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Göteborg, Sweden, 2011

THESIS FOR THE DEGREE OF MASTER OF SCIENCE

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Göteborg, Sweden, 2011

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Abstract

Multilevel inverters have become more popular over the years in electric high power application with the promise of less disturbances and the possibility to function at lower switching frequencies than ordinary two-level inverters. This report presents information about several multilevel inverter topologies, such as the Neutral-Point Clamped Inverter and the Cascaded Multicell Inverter. These multilevel inverters will also be compared with two-level inverters in simulations to investigate the advantages of using multilevel inverters. Modulation strategies, component comparison and solutions to the multilevel voltage source balancing problem will also be presented in this work.

It is shown that multilevel inverters only produce 22% and 32% voltage THD while the two-level inverter for the same 1kHz test produces 115% voltage THD. For another simulation, while using lower switching frequency, it is shown that when the two-level inverter generates 25.1W switching losses, the tested multilevel inverters only produce 2.1W and 2.2W switching losses.

Index Terms: Multilevel inverter, topologies, modulation, voltage balance, comparison

Acknowledgments

This master thesis project has been carried out at the Department of Energy and Environment at Chalmers, Sweden. It has been a great opportunity to work with this project and gain knowledge about this area of Power Electronics. I would like to thank the staff of this department for the this opportunity with special thanks to my examiner and advisor Stefan Lundberg.

I would also like to thank Oskar Josefsson for his help and positive "Are you done yet?" attitude.

Andreas Nordvall
Göteborg, Sweden, 2011

Contents

Nomenclature

I_a: Load current, RMS

$P_{cond,tot}$: Total conduction power losses

$P_{sw,tot}$: Total switching power losses

V_a: Load voltage, RMS

V_{CMC}: Cascaded Multicell Inverter module voltage

V_{dc}: DC side input voltage

V_{M2I}: Modular Multilevel Inverter submodule voltage

V_{P2}: P2-cell voltage

CCMLI: Capacitor Clamped Multilevel Inverter

CMCI: Cascaded Multicell Inverter

CSI: Current Source Inverter

EMI: Electromagnetic Interference

EV: Electric Vehicle

FACTS: Flexible AC Transmission System

GMCSI: Generalized Multilevel Current Source Inverter

GMLI: Generalized Multilevel Inverter

HEV: Hybrid Electric Vehicle

HVDC: High Voltage DC

M2I: Modular Multilevel Inverter

m: Number of levels in MLI

MLI: Multilevel Inverter

NPC: Neutral-Point Clamped

NPCMLI: Neutral-Point Clamped Multilevel Inverter

PDPWM: Phase Distortion Pulse Width Modulation

PSCPWM: Phase Shift Carrier Pulse Width Modulation

PWM: Pulse Width Modulation

RMS: Root Mean Square

RVMLI: Reversing Voltage Multilevel Inverter

SHE: Selective Harmonic Elimination

SVC: Space Vector Control

SVM: Space Vector Modulation

THD: Total Harmonic Distortion

VSI: Voltage Source Inverter

1 Introduction to Multilevel Inverters

1.1 The Concept of Multilevel Inverters

Conventional two-level inverters, seen in Figure 1.1, are mostly used today to generate an AC voltage from an DC voltage. The two-level inverter can only create two different output voltages for the load, $\frac{V_{dc}}{2}$ or $-\frac{V_{dc}}{2}$ (when the inverter is fed with V_{dc}). To build up an AC output voltage these two voltages are usually switched with PWM, see Figure 1.2. Though this method is effective it creates harmonic distortions in the output voltage, EMI and high $\frac{dv}{dt}$ (compared to multilevel inverters) [2]. This may not always be a problem but for some applications there may be a need for low distortion in the output voltage.

The concept of MultiLevel Inverters (MLI) do not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform, see Figure 1.3, with lower $\frac{dv}{dt}$ and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed.

To better understand multilevel inverters the more conventional three-level inverter, shown in Figure 1.4, can be investigated. It is called a three-level inverter since every phase-leg can create the three voltages $\frac{V_{dc}}{2}$, 0, $-\frac{V_{dc}}{2}$, as can be seen in the first part of Figure 1.3. A three-level inverter design is similar to that of an conventional two-level inverter but there are twice as many valves in each phase-leg. In between the upper and lower two valves there are diodes, called clamping diodes [1], connected to the a neutral

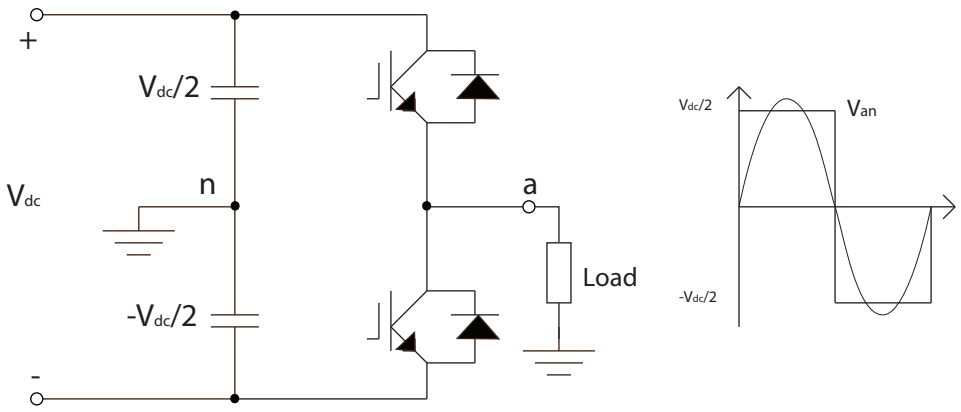

Figure 1.1: One phase leg of a two-level inverter and a two-level waveform without PWM

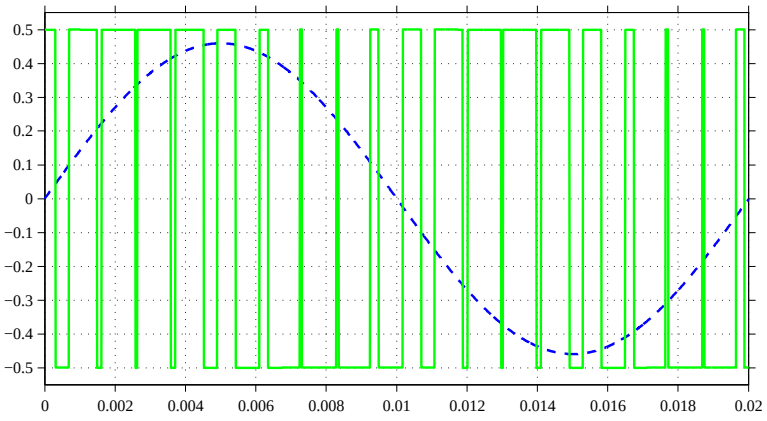

Figure 1.2: PWM voltage output, reference wave in dashed blue

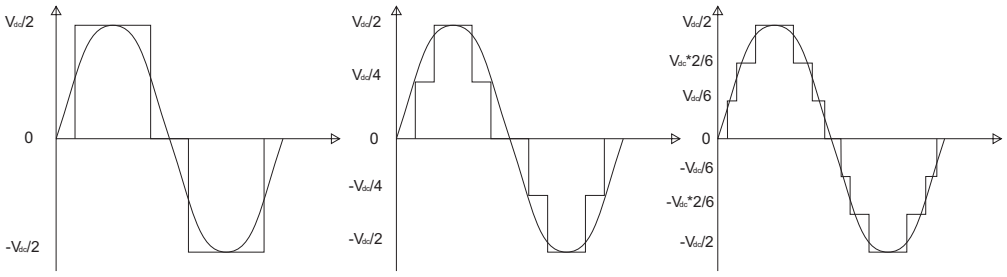

Figure 1.3: A three-level waveform, a five-level waveform and a seven-level multilevel waveform, switched at fundamental frequency

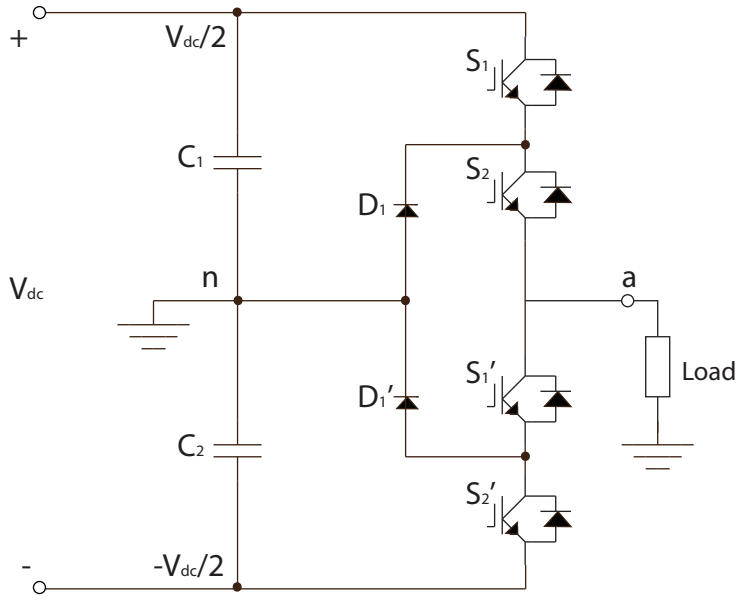

Figure 1.4: One phase leg of a three-level inverter

midpoint in between two capacitors, marked n in the figure. These capacitor build up the DC-bus, each capacitor is charged with the voltage $\frac{V_{dc}}{2}$. Together with another phase-leg an output line-to-line voltage with even more levels can be obtained. To create the zero voltage the two switches closest to the midpoint are switched on and the clamping diodes hold the voltage to zero with the neutral point. Now, if more valve pairs, clamping diodes and capacitors are added the inverter can generate even more voltage levels, see Figure 1.3, the result is a multilevel inverter with clamping diode topology.

Some of the most attractive features in general for multilevel inverters are that they can generate output voltages with very low distortion and $\frac{dv}{dt}$, generate smaller common-mode voltage and operate with lower switching frequency [2] compared to the more conventional two-level inverters. With a lower switching frequency the switching losses can be reduced and the lower $\frac{dv}{dt}$ comes from that the voltage steps are smaller, as can be seen in Figure 1.3 as the number of levels increase. There are also different kinds of topologies of multilevel inverters that can generate a stepped voltage waveform and that are suitable for different applications. By designing multilevel circuits in different ways, topologies with different properties have been developed, some of which will be looked upon in this report. The Multilevel inverter topologies that are investigated in this work are: Neutral-Point Clamped Multilevel Inverter (NPCMLI), Capacitor Clamped Multilevel Inverter (CCMLI), Cascaded Multicell Inverter (CMCI), Generalized Multilevel Inverter (GMLI), Reversing Voltage Multilevel Inverter (RVMLI), Modular Multilevel Inverter (M2I) and Generalized Multilevel Current Source Inverter (GMCSI).

The most dominant multilevel inverters use one or more voltage sources [3], as the three-level inverter, and most topologies presented in this report will have voltage sources,

so called Voltage Source Inverters (VSI). There are however also multilevel inverters with current sources, Current Source Inverters (CSI), for example the GMCSI in the list above.

1.2 Purpose of this work

This thesis report purpose is to gather information about multilevel inverter topologies and to investigate the properties of these topologies. Especially the voltage balancing problem that are common with multilevel inverter will be investigated and also the advantages and disadvantages of the multilevel inverters will be compared to two-level inverters.

1.3 Objectives of this work

The thesis work objectives can be divided into three parts: A literal study where several multilevel topologies are presented, an evaluation and comparison of the different topologies and a simulation presentation where two MLI topologies have been tested in simulation to investigate voltage balancing solutions and to compare with a two-level inverter. The comparisons include generated THD:s, harmonic components and losses.

2 Multilevel Inverter Topologies

2.1 Multilevel Diode Clamped/Neutral Point Inverter, NPCMLI

According to patents the first multilevel inverter (MLI) was designed in 1975 and it was a cascade inverter (cascaded inverters will be presented in a later chapter) with diodes blocking the source. This inverter was later derived into the Diode Clamped Multilevel Inverter, also called Neutral-Point Clamped Inverter (NPC) [2], see Figure 2.1. This topology is, as can be seen from the figure, based of the same principal as the before mentioned three-level inverter in Figure 1.4.

In the NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by a even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line, see the left part of Figure 2.1. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an $m-1$ number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate).

In Figure 2.1 one phase-leg of a five-level NPC inverter is displayed. By adding two identical circuits the three phase-legs can together generate a three-phase signal where sharing of the DC-bus is possible. Take note that the required number of clamping diodes are quite high and for higher number of voltage levels the NPC topology will be impractical due to this fact [2]. The reason for the inverter to have clamping diodes connected in series is so that all diodes can be of the same voltage rating and be able to block the right number of voltage levels. For example, in Figure 2.1 all diodes are rated for $\frac{V_{dc}}{4}$ ($\frac{V_{dc}}{m-1}$ in general) and the $D_1{}'$ diodes need to block $3\frac{V_{dc}}{4}$ and therefore there are three diodes in series. However, for low voltage application there is no need to connect components in series to withstand the voltage, since components with sufficient high voltage ratings are easy to find. With this configuration five levels of voltage can be generated between point a and the neutral point n; $\frac{V_{dc}}{2}$, $\frac{V_{dc}}{4}$, 0,$-\frac{V_{dc}}{4}$ and $-\frac{V_{dc}}{2}$, depending on which switches that are switched on. A waveform from one phase-leg of the inverter can also be seen in Figure 2.1 in which the steps are clearly visible. For NPCMLI:s with a higher number of voltage levels the steppes will be smaller and the waveform more similar to a sinusoidal signal. Of course, with a higher number of voltage levels the complexity of the inverter increase and also, as earlier mentioned, the number of components needed.

To achieve the different voltage levels in the output a setup of switching state combinations are used. In Table 2.1 the different states for the five-level NPC inverter are shown. Note that there is the possibility to only turn on (and off) every switch once per cycle, meaning that the inverter can generate a stepped sinusoidal waveform with a

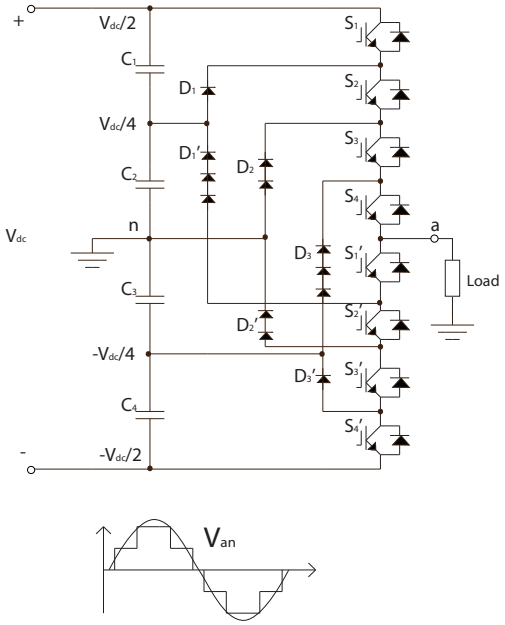

Figure 2.1: One phase-leg for a five-level NPC Inverter

fundamental switching frequency. From Table 2.1 it can be seen that for the voltage $\frac{V_{dc}}{2}$ all the upper switches are turned on, connecting point a to the $\frac{V_{dc}}{2}$ potential, see Figure 2.2. For the output voltage $\frac{V_{dc}}{4}$ switches S_2, S_3,S_4 and S_1' are turned on and the voltage is held by the help of the surrounding clamping diodes D_1 and D_1'. For voltage levels $-\frac{V_{dc}}{4}$ or $-\frac{V_{dc}}{2}$ clamping diodes D_2 and D_2' or D_3 and D_3' hold the voltage, respectively. For the voltages $\pm\frac{V_{dc}}{2}$ the current, when both voltage and current are positive (positive current goes out from the inverter), goes through the four top or bottom switches. For the other states positive current, while voltage is positive, goes through the D_x diodes and negative current through the D_x'diodes and also through the switches in between the clamping diodes and the load. For example, for state $\frac{V_{dc}}{4}$ positive current goes through diode D_1 and switches S_2, S_3 and S_4. In Figure 2.2 the turned on switches for every state are shown, switches in parallel to the thick dashed lines are on. In the figure the current paths are also shown, thin dashed lines, for every state and for both positive and negative current. For example for the $\frac{V_{dc}}{2}$ state the switches (positive current) or the diodes (negative current) are conducting and for the $\frac{V_{dc}}{4}$ state the current goes either through D_1 and three switches (positive current) or D_1' and through one switch (negative current). If there is a DC-source charging the DC-bus there is also currents flowing through the DC-bus to keep the DC-bus voltage constant. Table 2.1 also shows that some switches are on more frequently than others, mainly $S_4$and S_1', as long as a sinusoidal output wave that requires the use of all voltage levels is created. When the inverter is transferring active power this leads to unbalanced capacitors voltages since the capacitors are charged and discharged unequally, partly due to different workloads

Table 2.1: Switching states of one five-level phase leg. A "1" means turned on and "0" means turned off.

Output Voltage	S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

and that current is drawn from nodes between capacitors. The total DC-bus voltage will be the same but the capacitors voltage will deviate from each other. While transferring real power current is drawn from, for example, capacitor C1 and C2 during different amount of time, as can be seen in the left part of Figure 2.3. The time intervals in the figure represent the discharge time and as can be seen C2 is discharged more, leading to unequal capacitor voltages. Also, during for example the $\frac{V_{dc}}{2}$ state current discharges both C1 and C2 but in the $\frac{V_{dc}}{4}$ state current is drawn from the point between C1 and C2, discharging C2 but charging C1. This makes the voltages over the capacitors to deviate in a special way. When only transferring reactive power however the NPCMLI does not have this voltage unbalancing problem [3], see right part of Figure 2.3. This is because of that time intervals during which the capacitors charged and discharged are equal during reactive power transfer, as the figure suggests. To solve the voltage balancing problem an additional balancing circuit can be added or more complex control methods can be implemented. Due to the complications of the capacitor voltage balance, the NPCMLI at higher number of voltage levels is unusual.

When it comes to component quantities, such as number of needed components and their ratings, some things have to be considered that have been partially mentioned in the text above. As mentioned the inner switches are on more frequently than the outer switches since they are used in several of the switching states. Because of this a different amount of RMS current will flow through the switches depending on their position, with higher current rating needed for the inner switches [3]. The position of the clamping diodes are also important to their ratings since they need to block different levels of reverse voltage depending on where they are connected. If equal ratings are assumed for every individual diode, for every extra level of voltage that needs to be blocked and extra diode is required. This in turn explains why the NPC topology is unpractical with higher amounts of voltage levels since, because of the extra blocking diodes, the number of diodes grows quadratically with the level m following the equation $(m-1)*(m-2)$ [3]. This is however not valid for low voltage inverters, but since this report focuses on high and medium voltage application this is still the case. As for the other components $m-1$ DC-capacitors, $2(m-1)$ main diodes and $2(m-1)$ switches are needed for the NPCMLI topology. For thee-phase inverter of the NPC type the DC-bus can be shared and only the mentioned $m-1$ DC-capacitors are needed but the requirements for all other components are multiplied by three.

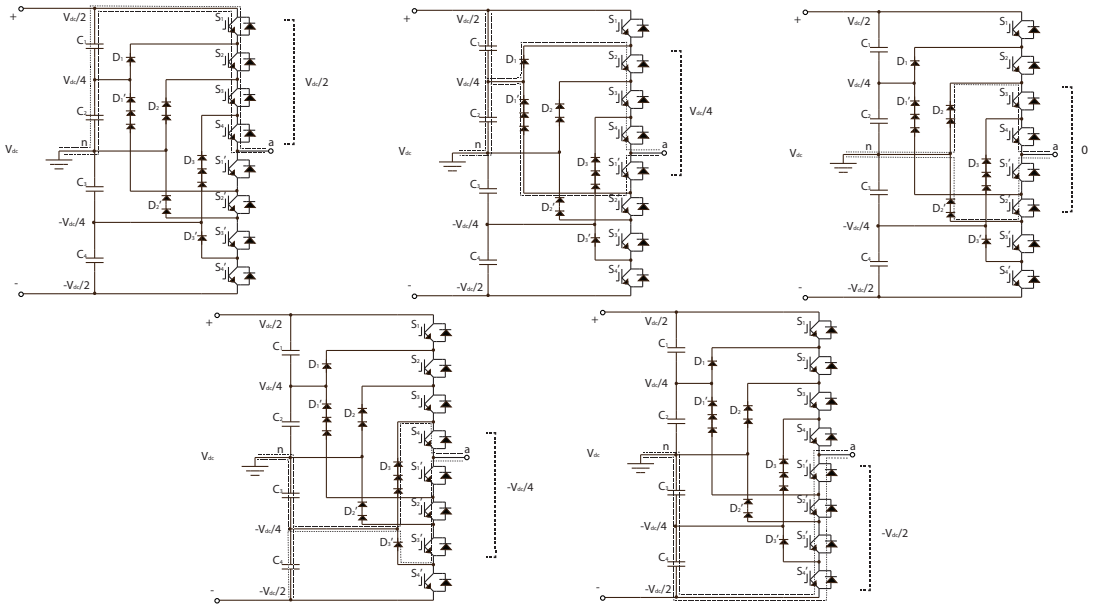

Figure 2.2: The thick dashed bar shows which switches that are on for every state. When both current and voltage is positive the current goes through these switches, otherwise through the diodes in parallel (depending on angle). Thin dashed line represent current path.

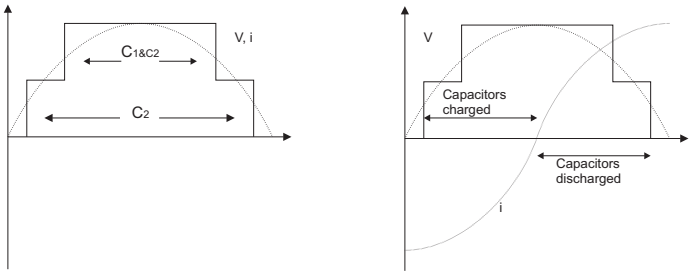

Figure 2.3: When voltage and current are in phase, to the left, capacitors are discharged unequally, but when the voltage and the current are 90 degrees out of phase, to the right, the charges is balanced.

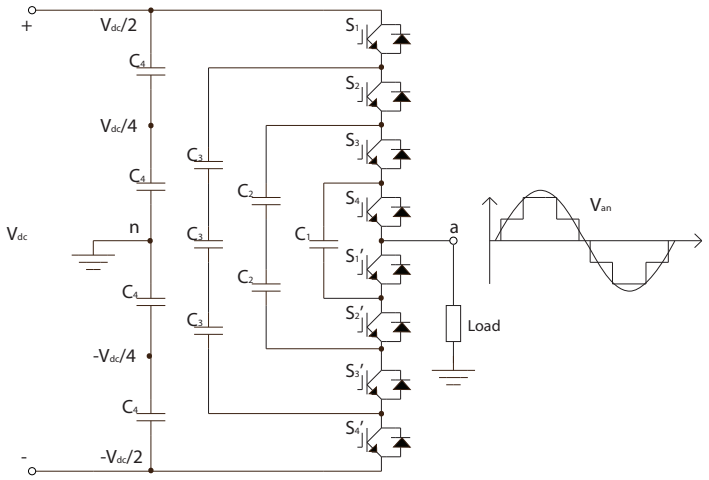

Figure 2.4: A Capacitor Clamped Multilevel Inverter with five voltage levels

2.2 Multilevel Capacitor Clamped/Flying Capacitor Inverter, CCMLI

A similar topology to the NPCMLI topology is the Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology, which can be seen in Figure 2.4. Instead of using clamping diodes it uses capacitors to hold the voltages to the desired values. As for the NPCMLI, $m-1$ number of capacitors on a shared DC-bus, where m is the level number of the inverter, and $2(m-1)$ switch-diode valve pairs are used. However, for the CCMLI, instead of clamping diodes, one or more (depending on position and level of the inverter) capacitors are used to create the output voltages. They are connected to the midpoints of two valve pairs on the same position on each side of the a midpoint between the valves [3], see capacitors C1, C2 and C3 in Figure 2.4.

As can be noticed in Figure 2.4 the same number of main switches, main diodes and DC-bus capacitors as in the NPCMLI are used for the CCMLI. The big difference is the use of clamping capacitors instead of clamping diodes, and since capacitors do not block reverse voltages the number of switching combinations increase [3]. Several switching states will be able to generate the same voltage level, giving the topology redundant switching states. The sum of a certain output voltage is generated by the DC-bus voltage $\pm\frac{V_{dc}}{2}$ and one or more of the clamping capacitors voltages added together. Since every capacitor is rated for the voltage $\frac{V_{dc}}{4}$ (in this five-level case, $\frac{V_{dc}}{m-1}$ in general), DC-capacitor and clamping capacitor alike, the output voltage, for this example $\frac{V_{dc}}{4}$, is generated by the DC-bus positive top value ($\frac{V_{dc}}{2}$) and the reverse voltage of clamping capacitor C_1. The other voltage states work in similar ways but with the help of other clamping capacitors.

Table 2.2 shows some switching states for a five-level CCMLI and Figure 2.5 shows an alternative to the state giving zero voltage in the table. In the figure the dashed

Table 2.2: Switching states for a five level Capacitor Clamped Inverter. A "1" means turned on and "0" means turned off.

Output Voltage	S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-\frac{V_{dc}}{4}$	1	0	0	0	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

line represent the path the current flows from the neutral point to the load. It flows through two C4 capacitors, giving $\frac{V_{dc}}{2}$ potential, then through switch S1 and down the C3 capacitors. Since every capacitor is charged with the voltage $\frac{V_{dc}}{4}$ the potential is now lowered with $3\frac{V_{dc}}{4}$. The current the flows up through the diodes in parallel with the switches S3´and S2´ and through capacitor C1 and then out to the load through switch S4 with the resulting potential 0 Volt.

As before with the NPCMLI only one switch need to be opened and one to be closed to change one state to another. This leads to that the inverter can be modulated at low (fundamental) switching frequency since a stepped sinusoidal waveform can be created when every switch is turned on and off only once per output frequency cycle. Also, as mentioned, the states shown in Table 2.2 are not the only states that put out these voltages, there are several switching states for all of the voltage levels, except the $\pm\frac{V_{dc}}{2}$ states. Depending on what state is chosen the capacitors can charge or discharge each other, making it possible to balance the charge in the capacitors with control methods [2]. Since the same current flows through all the active capacitors in a state, energy can be transferred from more charged to less charged capacitors, balancing the capacitors voltages between the capacitors that are conducting. If a method of using redundant switching states for voltage balancing is not applied there will be a capacitor voltage balance problem when transferring active power. However, if such a method is used the switching frequency may need to be raised for the balancing to be achieved properly [3]. The reason the capacitors voltages to get unbalanced while transferring active power some states are on during a longer time and the active capacitors gets discharged or charged more than others, much like in Figure 2.3. The unequal workload cause voltage unbalance but by using the redundant switching states the unbalances can be controlled. For pure reactive power transfer the CCMLI does not have any voltage balancing problem, which is also explained with Figure 2.3. Capacitors are charged and discharged equally during one cycle while transferring reactive power, like with the NPCMLI.

The amount of components for the CCMLI topology is as stated very similar to the NPCMLI, $m-1$ number of capacitors on a shared DC-bus and $2(m-1)$ switch-diode valve pairs, but with the difference that CC topology uses clamping capacitors instead of diodes. These capacitors do, as the diodes did, grow in numbers quadratically with the voltage level m, following the equation $\frac{(m-1)*(m-2)}{2}$ [2], not counting the main capacitors on the DC-bus. Again the need for several components of the same sort and rating in

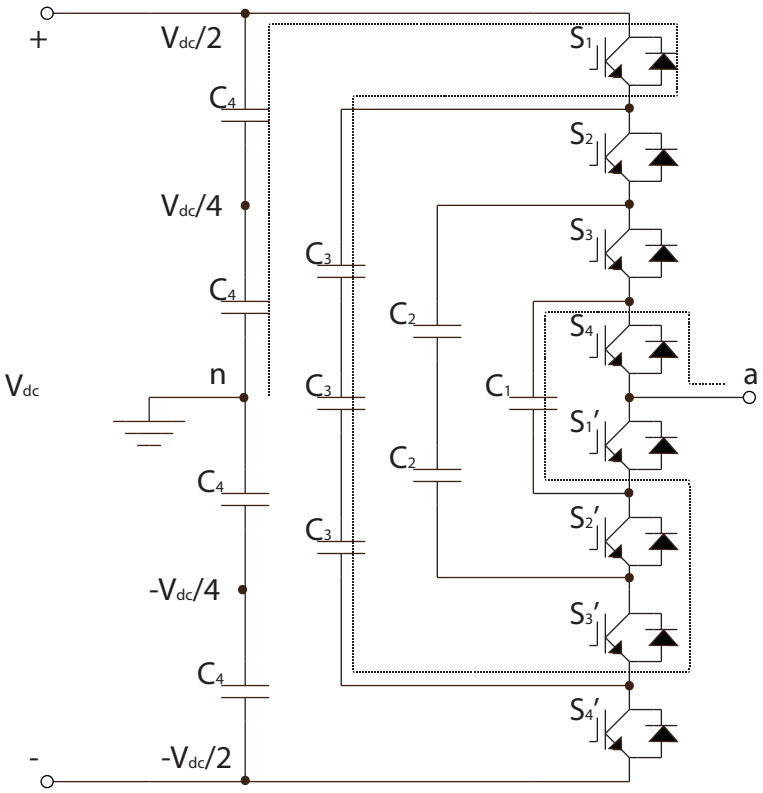

Figure 2.5: One example of a alternative switching state for the voltage 0. The dashed line represent how the current flows through the capacitors and switches out to the load.

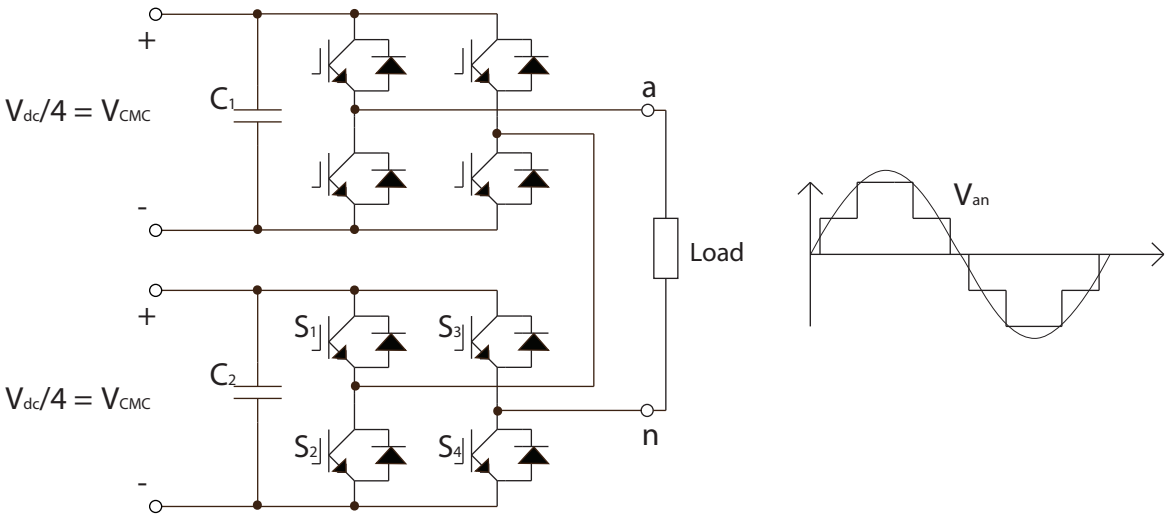

Figure 2.6: A five-level Cascaded Multicell Inverter

series is needed because of the high voltage ratings, as for the clamping diodes in the NPCMLI. When the CCMLI is used in a three-phase setup it can, as the NPCMLI, share the DC-bus and only multiply all the other remaining components by three.

2.3 Cascaded Multicell Inverter, CMCI

A Cascaded Multicell Inverter (CMCI) differs in several ways from NPCMLI and CCMLI in how to achieve the multilevel voltage waveform. It uses cascaded full-bridge inverters with separate DC-sources, in a modular setup, to create the stepped waveform. In Figure 2.6 one phase-leg of a five-level Cascaded Multicell Inverter is shown. Each full-bridge can be seen as a module and it is only these modules that build up the CMCI topology. One full-bridge module is in itself a three-level CMCI, and every module added in cascade to that extends the inverter with two voltage levels. In Figure 2.6 there are two full-bridge modules creating the five different voltage levels available. Applications suitable for the CMCI are for example where photovoltaic cells, battery cells or fuel cells are used [3]. Such an example could be an Electric Vehicle there several power cells exists.

The total output voltage is the sum of the outputs of all the full-bridge modules in the inverter and every full-bridge can create the three voltages V_{CMC}, 0 and $-V_{CMC}$. To change one level of voltage in the phase output the CMCI turns one switches on (and one off) in one full-bridge module. For a full-bridge module to add the voltage V_{CMC} the switches $S_1$and S_4 are turned on, for $-V_{CMC}$ the switches S_2 and S_3 are turned on. When there is current flowing through the full-bridge the 0 voltage is achieved by turning on the two switches on the upper halves of the full-bridge (S_1 and S_3) or the two switches on the lower part (S_2 and S_4). Together with several full-bridges a stepped waveform can be generated. The maximum output voltage is $\frac{m-1}{2}V_{CMC} = sV_{CMC} = \frac{V_{dc}}{2}$ (and minimum voltage $\frac{m-1}{2}(-V_{CMC}) = s(-V_{CMC}) = -\frac{V_{dc}}{2}$), where m is the number of

levels and s the number of full-bridge modules[2]. It should be noted that the CMCI is capable of putting out the total voltage source magnitude in both positive and negative direction while many other topologies can only put out half the total DC-bus voltage source magnitude. This is why the total sum of the DC-side voltages in Figure 2.6 is $\frac{V_{dc}}{2}$ and not V_{dc}, since it is still able to put out $\frac{V_{dc}}{2}$ to the output (like the other topologies). All full-bridge inverters that are connected can contribute with the same voltage, in a way making the topology very scalable. There is also the possibility to charge every modules with different voltages.

The sources in each full-bridge need to be isolated if the inverter is going to be implemented in a active power transfer application, for voltage balance reasons since there is no common DC-bus to recharge the sources energy content. However, since the CMCI uses separate energy sources it is well suitable for renewable energy or energy/fuel cell applications there every separate voltage source could be isolated [3]. A drawback for the energy/fuel cell applications is however that the sources must be charged individually or through the inverter. Still, the charge balance in the voltage sources needs to be controlled, for example in electric vehicle batteries, so that there is no voltage unbalance, but this can be done with balancing modulation methods. Balancing modulation methods will be investigated further in chapter 4. When adapted to pure reactive power applications the CMCI is self balanced, just as the NPCMLI and CCMLI, since the charge change over one cycle is zero [3] (right part of Figure 2.3). Since there is no common DC-bus to recharge the sources in the CMCI topology, balancing modulation strategies include prioritizing higher charged modules in modulation (see chapter 4) or activating two modules not needed for the output voltage level and let them balance each other (transferring energy from higher charged module to lower charged module). Two modules for balancing purposes are only available when the output voltage level is two levels lower than maximum (zero voltage level for the five-level MLI) or more. When two modules are available in this way one of the can be activated with positive voltage and the other with negative voltage. The resulting output voltage of these two modules is then zero but energy is transferred from the positive module to the negative module when current goes out from the inverter (and the other way around when current goes into the inverter). In this way two modules can balance each other when they are not needed for generating the output voltage.

Compared to the NPCMLI and CCMLI the CMCI requires fewer components, every voltage level requires the same amount of components. However, the number of sources are higher, for the phase-leg to be able to create a number of m voltage level $s = \frac{m-1}{2}$ sources are required [4]. The number of sources s is also equal to the number of full-bridge modules. In turn, every full-bridge module has four diodes and four switches in turn giving the CMCI $4\frac{m-1}{2} = 2(m-1) = 4s$ diodes and switches. When making a three-phase inverter with the CMCI topology the number if needed components needs to be multiplied by three for all components since there is no common DC-bus to share.

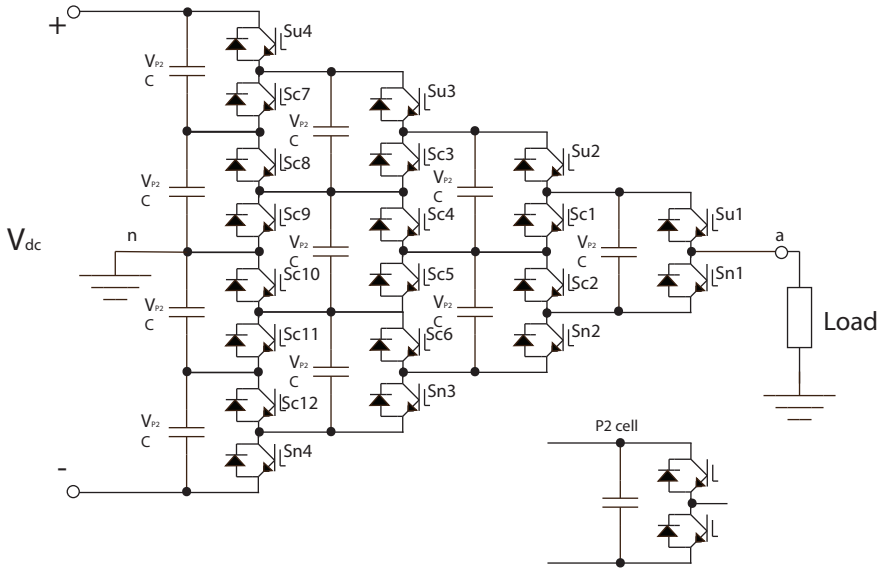

Figure 2.7: A five-level Generalized Multilevel Inverter

2.4 Generalized P2-cell Multilevel Inverter, GMLI

This far all the presented MLI:s all have a problem with voltage balancing when transferring active power. The Generalized Multilevel Inverter (GMLI), seen in Figure 2.7, does however not have the voltage balance problem since it is able to self balance its own capacitors without the need for extra circuits [5]. The NPCMLI, CCMLI and CMCI, among others, can also be derived from this generalized MLI topology [6]. The topology is based upon the use of simple two-level voltage cells, called P2 cells, which are connected in a triangular shape. Each P2 cell has two switch-diode pairs and one DC-capacitor that is charged with the value of $V_{P2} = \frac{V_{dc}}{m-1}$ (there m is the voltage level number). When one P2 cell is not used to achieve a certain voltage level it has one switch turned on to automatically balance the capacitor voltages[5], which one is decided depending on what switch in bordering P2 cell that is on. Figure 2.7 shows one phase leg for the generalized MLI, for three-phase two more of these circuits are needed in parallel. It is possible to share the DC-bus between phase-legs.

The two simplest voltage states for the GMLI, in this case a five-level GMLI, are the voltages $2V_{P2} = \frac{V_{dc}}{2}$ and $-2V_{P2} = -\frac{V_{dc}}{2}$. When all the upper switches (Su4, Su3, Su2, Su1) are on, the output voltage is $2V_{P2}$, and when all the lower switches (Sn4, Sn3, Sn2, Sn1) are on the voltage is $-2V_{P2}$. For all voltage states, except $\pm\frac{V_{dc}}{2}$, there are several combinations to choose from. The GMLI follow a couple of specific rules to decide which switches that should be on and off, including which switches that should be on for the purpose of voltage balancing, in addition to that only one switch in a P2 cell is open at a time. The rules are as follows [5].

1. Each switch pole/P2 cell is independent

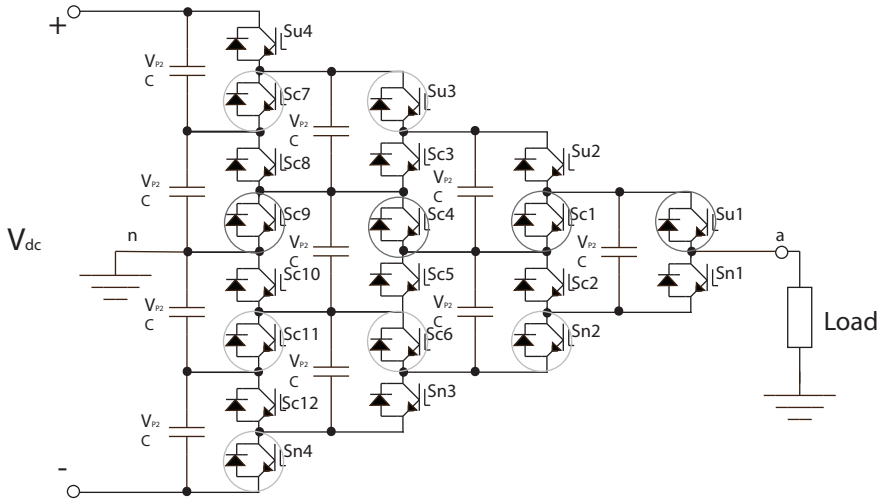

Figure 2.8: Generalized MLI in a switching state, switches in circles are turned on. In this case the output voltage is 0 since Sc9, Sc4, Sc1 and Su1 are turned on, represented with dark circles. The switches with lighter colored circles are on for balancing.

2. If one switch in a cell is on, the other is off
3. If a switch state is chosen, the other switches state can be determined by the two first rules

A switch pole is the two switches that exists in a P2 cell. These rules should be applied to the inverter after that switches for an output voltage state has been chosen. Figure 2.8 shows an example of a switching state there some switches are on for achieving the output voltage level and the rest of the switches that are on are balancing the capacitors voltages. To understand the automatic balancing for the GMLI topology note that, for instance, the switch Sc7 is switched on in Figure 2.8 for automatic balancing in the circuit and surrounding switches are turned off. This makes the DC-bus capacitor charge the cell capacitor close to Sc7 with the DC-bus capacitor voltage, $\frac{V_{dc}}{4}$, which is the voltage that all capacitors are charged with in this five-level case. During different voltage states other sets of capacitors can balance each other so that all capacitors are equally charged. The DC-bus capacitor, that can be assumed to be balanced, should be used properly in the balancing as well, as in the example above.

Even though the precise rules to control the inverter switches, holding the complexity back, it is clear from the figures that with increasing number of voltage levels the number of components required increase even more. To extend a m level GMLI inverter with one level, m P2 cells are needed. For two voltage levels, $m + (m + 1) = 2m + 1$ P2 cells will be added, and so on. The number of P2 cells can be expressed with the sum

$$\sum_{n=1}^{m-1} n = \frac{m(m+1)}{2} - m$$

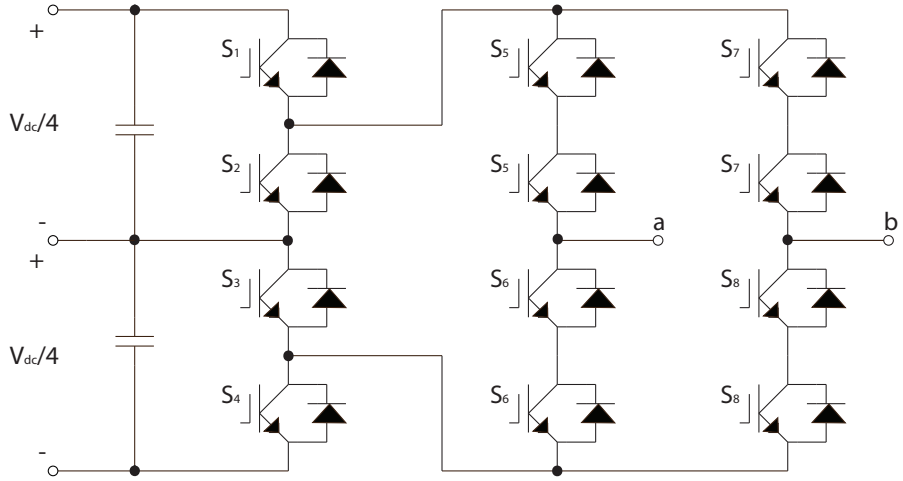

Figure 2.9: One phase-leg for a five-level Reversing Voltage Multilevel Inverter

and as we can see in the figures, for every cell there is one capacitor, two diodes and two switches.

2.5 Reversing Voltage Multilevel Inverter, RVMLI

Compared with the four earlier chapters, which have presented popular and well documented multilevel topologies, the topology in this chapter, the Reversing Voltage topology, has not yet, as it seems, gained any great recognition. The Reversing Voltage (RV) MLI topology, displayed in Figure 2.9, was proposed during late 2008 [7] as a new topology to challenge the existing popular topologies, such as the NPCMLI. A great proposed advantage over the more popular MLI topologies, the NPCMLI and CCMLI, is the need for fewer components, but since components with equal ratings are used in this report (in favor of comparison with other topologies) the number of components is not very low, as compared with if valves with different ratings would be used.

The basic method that the RVMLI uses in operation is to create a multilevel stepped voltage half-wave, only positive values, with a simple inverter with a low number of DC-sources. The full-bridge connected to the first inverter can then reverse these positive half-wave voltages every half cycle to generate a complete sinusoidal voltage over the load. In this way, the components are used effectively, but if the circuits is going to withstand the voltages, under the assumptions that all devices of the same sort has the same ratings, additional valves are needed compared to requirements proposed in [7]. The full-bridge can also be controlled with low frequency since it is only supposed to reverse the voltage every half cycle, so the switch pairs in the full-bridge can be operated at the fundamental output voltage frequency [8]. The inner inverter could however be modulation at fundamental or high frequency independent of the full-bridge inverter modulation.

By operating the switches S_1 to S_4 a stepped positive voltage waveform is created

Table 2.3: Switching states for the five-level Reversing Voltage Inverter. A "1" means turned on and a "0" means turned off.

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$-\frac{V_{dc}}{2}$	1	0	0	1	0	1	1	0
$-\frac{V_{dc}}{4}$	0	1	0	1	0	1	1	0
0	0	1	1	0	1	0	0	1
$\frac{V_{dc}}{4}$	0	1	0	1	1	0	0	1
$\frac{V_{dc}}{2}$	1	0	0	1	1	0	0	1

and by opening either the switches S_5 and S_8 or S_6 and S_7 in the full-bridge a positive or negative voltage waveform is generated. Table 2.3 shows the different states for the multilevel positive half-wave inverter of the topology.

Two advantages with the RVMLI are simpler controlling, since the modulation is divided in two parts (positive half-wave and reversing) and that it does not have a voltage unbalance problem if separate sources are used, as proposed in [7]. It is however true for several topologies that separate sources can solve the voltage unbalance problem. If separate sources are not used, balancing will have to be achieved by balancing the workload between the sources, since there is also one more state to create the $\frac{V_{dc}}{4}$ voltage (switches S1 and S3 on instead of S2 and S4). If workload is modulated properly it can be chosen from which source energy is to be transferred to or from during the $\pm\frac{V_{dc}}{4}$ voltage states and in that way the sources can be held balanced. As for the CMCI the RVMLI is capable of putting out the full range of its DC-side voltage, dividing the need for the DC-side voltage by two for the same output voltage compared to other topologies, such as the NPCMLI.

For a number of voltage levels m the topology needs $(m-1)+2(m-1) = 3(m-1)$ main switches and diodes per phase and also $\frac{m-1}{2}$ isolated supplies [7] and/or DC capacitors. The reason for the high number of components in the full-bridge is that every phase leg in the full-bridge must be able to withstand the voltages from the multilevel inverter phase-leg. No clamping diodes or flying capacitors are needed. However, even though the number of components are low, a transformer is required for isolation on the load side for each phase if the low number of sources is going to be valid [8], see Figure 2.10. This could however also be applied to other topologies. The importance of the use of transformers is also dependent on the application.

2.6 Modular Multilevel Inverter, M2I

The Modular Multilevel Inverter (M2I), seen in Figure 2.11, is a newer topology first introduced in 2002 [17]. It uses a modularized setup of submodules, essentially half-bridges, which are connected or bypassed to generate a certain output voltage level. Every phase-leg is composed of two arms where each arm has a number of n submodules. In turn, in every submodule there is a DC-capacitor charged with the voltage $V_{M2I} = \frac{V_{dc}}{m-1}$. Each arm can then generate the maximum voltage of $\pm n * V_{M2I} = \pm V_{dc}$, where the

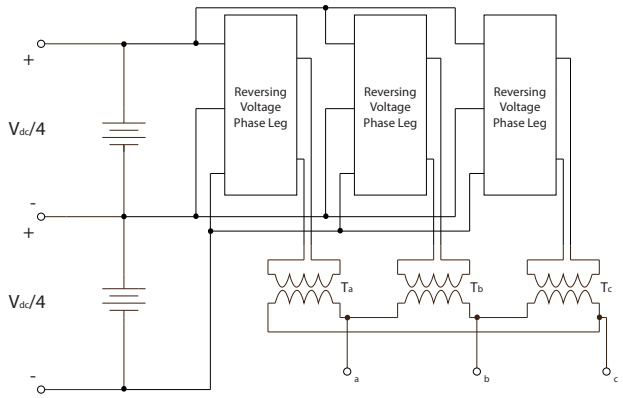

Figure 2.10: A three phase setup with five-level RVMLI phase-legs and transformers on each phase

modules in both arms are connected or bypassed to create a AC output voltage. So for a number of voltage levels m the inverter needs $m-1=n$ number of submodules per arm, so $2(m-1)=2n$ submodules per phase-leg. Compared to the somewhat similar CMCI topology the modules in this M2I topology can only put out two voltages, V_{M2I} or 0. This explains the need for two arms in every phase-leg. The M2I topology does not need shared DC-capacitors in a DC-bus, but does however require a DC-bus for circulating currents. These currents can however also circulate through other phase-legs. The two inductors, one in each arm in a phase-leg, are there to take up the voltage difference when modules are switched in and out.

To activate a certain submodule in an phase-leg arm to make its voltage source contribute to the output voltage the switch S1 is switched on and S2 is switched off. To bypass a submodule the switches S1 is turned off and S2 is turned on in that certain submodule. The arm in which a submodule is to be connected is determined by if the wanted voltage is positive or negative and which submodule in the arm is determined by the balancing modulation. The balancing modulation is the program that chooses which modules that are to be activated for each state to achieve voltage balance in all modules. To keep the sources in the submodules balanced the order in which they are connected can be changed. If, for instance, one submodule has more charge stored in its capacitor it can be prioritized to be activated first or last, depending on current direction, to balance the submodule voltages. The M2I topology hence has a redundant setup of switching states. Some switching state examples for achieving the voltage levels in this five-level M2I can be seen in Table 2.4. Note that during any moment, half the modules are connected and half the modules are bypassed. This is necessary since the sum of all connected modules in a phase-leg must be V_{dc}.

Component requirements for the M2I topology is mostly dependent on the number of submodules, and hence the number of voltage levels, since there is only the inductors in the topology setup that is independent of the number of levels. Every submodule is composes of a half-bridge and a DC-capacitor, so for every submodule there is two

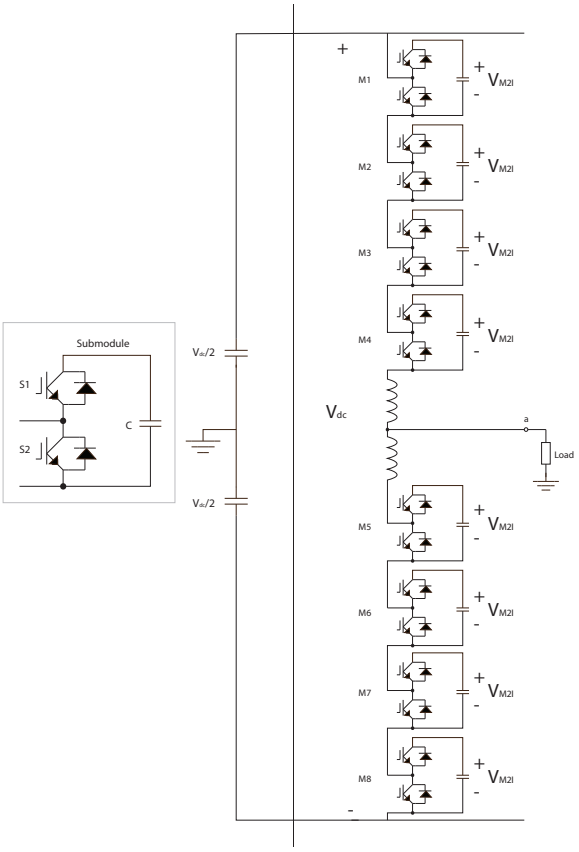

Figure 2.11: One phase-leg of a five-level Modular Multilevel Inverter

Table 2.4: M2I switching states examples. A "1" means that a submodule is inserted (switch S1 on) and a "0" means that it is bypassed (switch S2 on).

V_{load}	M1	M2	M3	M4	M5	M6	M7	M8
$\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1
$\frac{V_{dc}}{4}$	1	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1	1
$-\frac{V_{dc}}{4}$	1	1	1	0	0	0	0	1
$-\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0

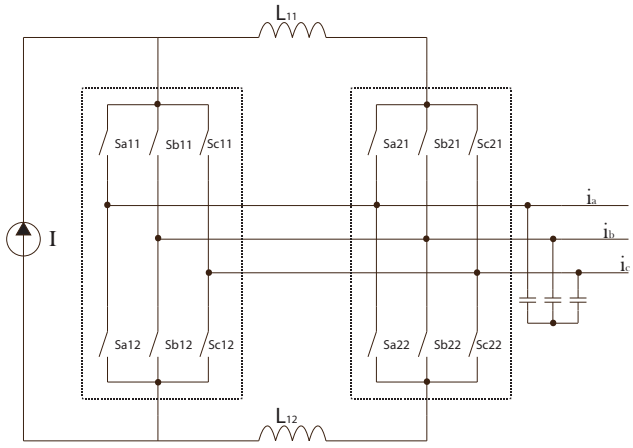

Figure 2.12: A three-phase five-level Generalized Current Source Inverter

switches, two diodes and one capacitor. Additionally, for every phase-leg there is two inductors for the phase-leg arms. The inductors, seen close to the midpoint in the phase-leg in Figure 2.11, are there to take up the voltage difference between states. Also, each switch in the M2I submodules must be able to withstand at least the submodule capacitor voltage, V_{M2I}. Since the voltage spanning over both arms is V_{dc} and the number of submodules in the arms, as a function of number of voltage levels, is $m-1$ the voltage that a switch must be able to withstand described with the total DC voltage is $\frac{V_{dc}}{m-1}$.

2.7 Generalized Multilevel Current Source Inverter, GMCSI

The topologies presented so far have all been inverters with voltage sources, so called Voltage Source Inverters (VSI). Even though Multilevel VSI:s are the most popular topologies [3] there do exist multilevel Current Source Inverters (CSI). The concept of a multilevel CSI is to use one or more current sources instead of voltage sources and with the help of power electronics inject levels of current to a load. In this report the Generalized Multilevel Currents Source Inverter (GMCSI) from [9] will be presented, displayed in Figure 2.12.

The GMCSI is a three-phase topology that consist of a number of "current source six-valve modules", see the valves within dashed lines in Figure 2.12. In addition there are also $m-3$ positions with inductors to smooth the DC-side current and to divide its source into different current ratings [9]. Only one current source is needed. As with many of the other MLI topologies, one of the advantages with the GMCSI topology is that it can eliminate the use of transformers in some high power applications. Also the modularized configuration is advantageous and the topology is not as component heavy as some other topologies [9].

One problem with the GMCSI, comparable with the voltage unbalance problem in some of the VSI:s, is that there can be a current unbalance in the smoothing inductors. This problem can however be solved with the use of redundant switching states [9]. The

Table 2.5: Examples for some GMCSI switching states

i_a	i_b	i_c	Switches on
0	I	$-I$	Sb12, Sb22, Sc11, Sc21
$\frac{I}{2}$	$-I$	$\frac{I}{2}$	Sa11, Sb12, Sb22, Sc21
I	$-I$	0	Sa11, Sa21, Sb12, Sb22
I	$-\frac{I}{2}$	$-\frac{I}{2}$	Sa11, Sa21, Sc12, Sc22

number of switching states for a GMCSI can also be calculated by the number of modules n ($n = \frac{m-1}{2}$ as mentioned above) with the equation

$$N_c = 3^{2n} \tag{2.1}$$

where N_c is the number of switching states. For the five-level GMCSI, $N_c = 3^{2*2} = 81$, meaning 81 switching states on five levels for three phases. Some of these states is shown in Table 2.5. The reason for the inductor current unbalance is the voltage across the inductors. Depending on if the voltage is positive or negative the current through the inductors will ramp up or down from its supposed value. By changing states in a proper way the inductor currents can be held on a balanced level.

The inductors also have different amounts of current flowing through them and the amount of current is dependent of the inductors position. For every valve module that is passed the current amplitude drops $\frac{I}{n}$ since the amount of current that goes through every closed switch (in every module) is $\frac{I}{n}$. Also, only one switch in the upper half of a valve module and one switch in the lower half of a valve module can be switched on at any moment [9]. This also means that the current rating of a valve should be at least $\frac{I}{n} = \frac{2I}{m-1}$. Since different amounts of current flow through the inductors depending on their position it is necessary to add inductors in parallel closer to the source if components with the same current rating are to be used. For an GMCSI with m number of current levels the inverter is composed of $\frac{m-1}{2}$ valve modules (within the dashed line in Figure 2.12), which all contain six switches. There are also $m-3$ positions where inductors should be placed. With inductors with equal current rating the number of inductors is $\frac{m-1}{2}(\frac{m-3}{2}-1)$. For the seven-level GMCSI this would mean two inductors in parallel closest to the source (on each side, top and bottom) and one inductor at the second inductor position. For a nine-level GMCSI three inductors in parallel would be in the first position followed by two and one inductor.

3 Modulation

When it comes to multilevel inverter modulation there are basically two groups of methods: modulation with fundamental switching frequency or high switching frequency PWM [2]. For both cases a stepped output waveform is achieved, but with the high switching frequency methods the steppes are modulated with some sort of PWM. Independent of switching frequency choice there are, however, also space vector methods to choose from.

3.1 PWM for two-level inverters

Ordinary PWM modulation for two-level inverters is accomplished through comparison between a reference wave and a triangular carrier wave. The reference wave have the frequency and amplitude wanted for the output voltage signal and the triangular carrier wave has the amplitude of half the DC input voltage, in an simple ordinary case, and its frequency is dependent on application but must be higher than the reference wave frequency. In electric power application the carrier wave frequency is often in the range of kHz. The reference wave frequency decides how often the switches in the inverter changes state, every time the triangular carrier wave crosses the reference wave the switches turn on or off. A plot of the ordinary two-level PWM reference, carrier wave and output voltage can be seen in Figure 3.1. If the carrier wave crosses the reference so it becomes higher than the reference the top switch turns off and bottom switch turns on in the two-level inverter (see Figure 1.1) so that $\frac{V_{dc}}{2}$ becomes the output. When the carrier wave crosses the reference again, now getting lower than the reference, the switches change state and the output becomes $-\frac{V_{dc}}{2}$. When the reference is positive the output voltage signal will be $\frac{V_{dc}}{2}$ for the majority of the time resulting in a positive output AC signal following the reference. An straightforward example is if the reference wave is constant at zero voltage, the carrier wave would then cross it upwards and downwards with the same time between every crossing, making $\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$ being the output for equal time, each cycle. This leads to that the average output voltage over one carrier wave period becomes zero.

3.2 PWM for multilevel inverters

Multilevel PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave, much like in the two-level PWM case. To reduce harmonic distortions in the output signal phase-shifting techniques are used [2]. There are several methods that change disposition of or shift multiple triangular

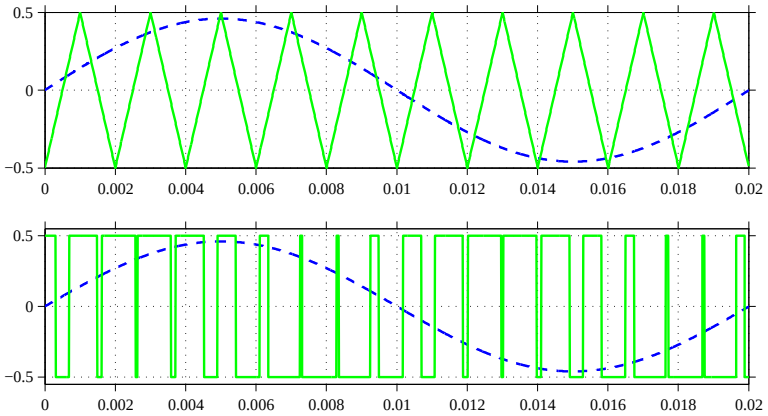

Figure 3.1: PWM reference (blue dashed) and triangular carrier (green solid) wave in upper plot and output voltage (green solid) eave in lower plot

carrier waves. The number of carrier waves used is dependent to the number of switches to be controlled in the inverter.

In addition to the two sinusoidal carrier wave modulation methods presented further down there are also two more well known alternative methods that will not be discussed in this report: Alternative Position Opposition Disposition (APOD) and Phase Opposition Disposition (POD) [10].

3.2.1 Phase Shifted Carrier PWM

The Phase Shifted Carrier PWM (PSCPWM), Figure 3.2, is a multicarrier modulation strategy that has all carrier waves phase shifted from each other. It is the standard modulation strategy for the CMCI topology [10] but is not exclusively for that topology.

For a CMCI with n number of full-bridge modules in each phase-leg there are also n number of triangular carrier waves. There is one triangular carrier wave for each full-bridge module, phase shifted with $\frac{180^\circ}{n}$ in between them, with amplitudes the magnitude of the total DC voltage. The magnitudes for the carrier waves are modulated by the actual voltage level in the appropriate module. For the five-level CMCI with two modules there are two triangular carrier waves, one for each module, see Figure 3.2. The modules create the two voltages in Figure 3.3 with PSCPWM modulation. There are also two reference waveforms for the two legs in each inverter modules that are phase shifted 180° from each other, as can be seen in Figure 3.2. Both reference waves are compared with both carrier waves, one reference wave is for modulation of the left full-bridge module leg switches (dashed reference wave) and the other reference wave to modulate the right full-bridge module leg switches (solid reference wave). The first triangular wave in Figure 3.2 is compared with the upper output voltage plot in Figure 3.3 (and the second triangular with the lower voltage plot). Close to 2ms in the plots it can be seen that the first triangular wave crosses one reference wave downwards, controlling the right leg switches

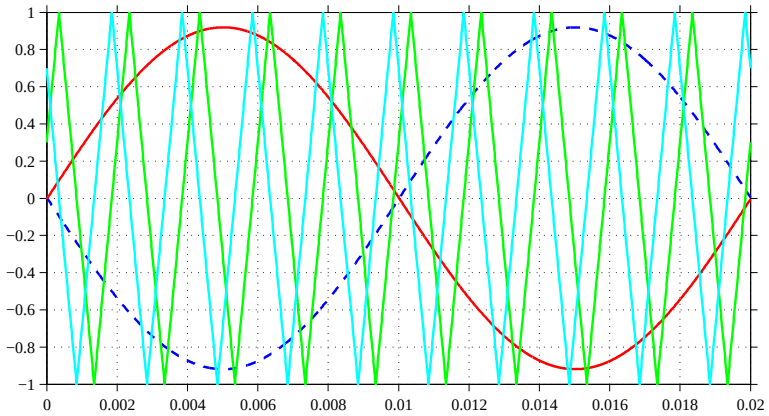

Figure 3.2: The carrier and reference waves for a five-level CMCI with PSCPWM, two reference waves and two triangular waves (one for each module)

of the modules, turning that modules output voltage from 0 kV to −0.5 kV. Closely after the second carrier wave crosses the same reference wave (the one that controls the right leg switches in the modules) upwards turning the output voltage from −0.5 kV to 0 kV. Comparisons with the other reference wave works in the same wave, but then controlling switches in the modules left legs. As the plots suggests the two modules share the workload for all levels, no module is strictly connected to one voltage level in the output. For the CMCI this strategy cancels all carrier and sideband associated harmonics up to the 2nth carrier group [11].

3.2.2 Phase Distortion PWM

In Phase Distortion PWM (PDPWM), Figure 3.4, all carrier waves are in phase. A great acknowledgment for this technique is that it is generally accepted as the method that creates the lowest harmonic distortion in line-to-line voltage [12].

When used for an NPCMLI with m number of voltage levels, $m-1$ number of triangular carrier waves are used. These carrier waves have the same frequency and are arranged on top of each other, with no phase shift, so that they together span from maximum output voltage to minimum output voltage [11]. The carrier waves amplitudes should be modulated with aspect of the current voltage magnitude for each respective voltage level, each carrier wave is connected to a specific output voltage level. If the carrier waves are not modulated in this way the correct output voltage will not be achieved if the sources voltage levels change from their supposed value (get unbalanced). If the sources voltage amplitudes change without that the carrier waves are modulated with that change the correct output voltage will not be generated during the during the correct time spans. When one carrier wave is crossed by the reference the output wave steps one level up or down with a switch transaction. One carrier wave hence modulates the use of one voltage state. Only one level is modulated at any time, as can be seen in the in Figure 3.4, since

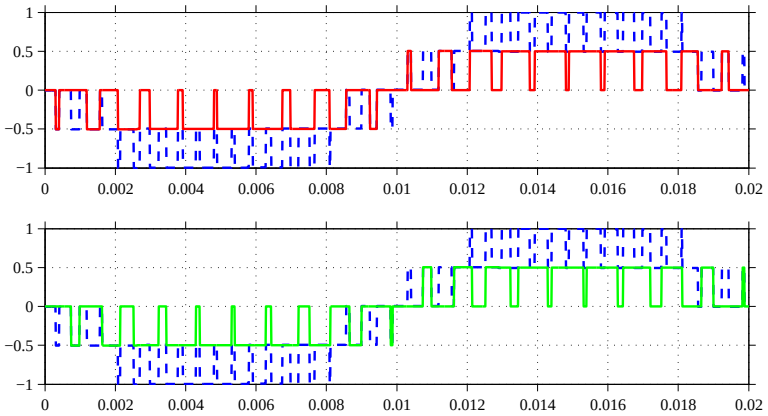

Figure 3.3: The two module voltages, one in each plot, together with the achieved total output voltage (blue dashed line in both plots)

the reference only crosses one carrier at any level. The output voltage from the PDPWM modulation with a five-level NPCMLI is shown in Figure 3.5. The carrier waves should be modulated with aspect of the current voltage magnitude for each respective voltage level.

Phase Distortion PWM is also the proposed control method for the RVMLI [8] but can be used with other topologies as well. For the CMCI the PDPWM modulation is built up of $m-1$ carrier waves, two for each full-bridge module, one below zero and one above zero for every module. Each module then modulates one voltage level. Which level one full-bridge module modulates can be changed for balancing purposes. For the five-level CMCI this could mean that the module with highest charge within its source is modulated by the carrier waves two and three in Figure 3.4, if counting the carrier waves from top to bottom. The other module, with lower charge, would then be controlled by carrier waves one and four. Since waves two and three are closest to zero the first module, with higher charge, will be connected to the load first every half cycle, for both positive and negative output voltages. This will lead to a higher workload for this module. If which module contains the most charge change, the modules can change which carrier waves that modulate them with each other. More generally, the two triangular waves closes to zero (one wave with positive voltage and one with negative voltage) can control the module with the highest charge if active power is to be transferred. The positive carrier then modulated the full-bridge modules left leg for positive output voltages and the negative carrier the right leg for negative output voltages. Other modules should be controlled by two carrier waves further away from zero, one from each side of zero voltage at the same position (second wave above and second wave below zero, for example). The carrier waves amplitudes should be modulated by the voltage level in the full-bridge module it controls, much like with the carrier wave modulation for PSCPWM, so that correct output voltages are generated during the correct time spans.

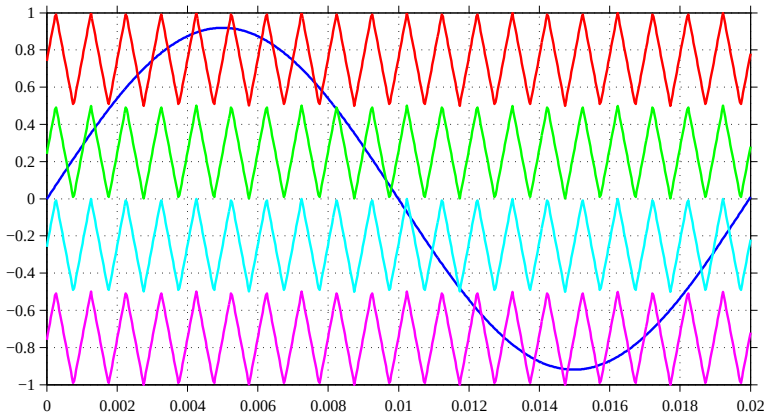

Figure 3.4: The reference (cosine) and carrier waves (triangular) for a five-level NPCMLI or CMCI with PDPWM.

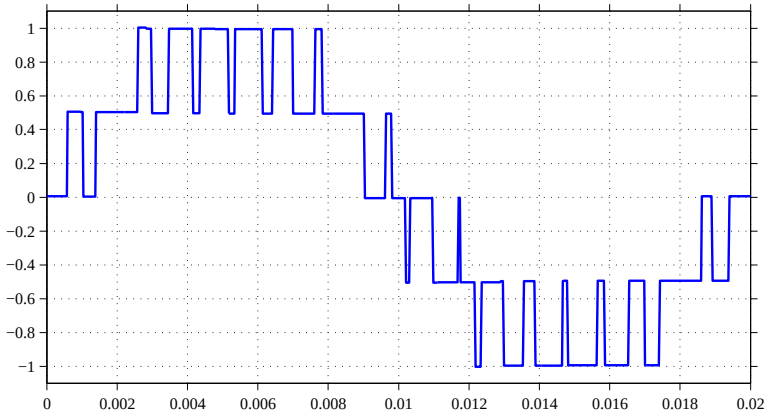

Figure 3.5: The output voltage for a five-level NPCMLI with PDPWM

3.3 Space Vector Modulation and Space Vector Control

Space Vector Modulation (SVM) is a high frequency modulation alternative to PWM, where one big difference is that SVM must be used with a three-phase system. In SVM, the three reference phases are transformed into one reference vector which is placed inside a Space Vector Diagram, see Figure 3.6. Depending on the three phases amplitudes the vector in the diagram will end up somewhere in one of the diagrams triangles. Every corner of the diagram represents a state for the three-phase inverter, where the state number represent the wanted level for each phase-leg. The states for the three corners in the triangle that the vector is inside are modulated, each state on for a specific time, so that the vector is recreated by the inverter in the form of a mean value of the three used vectors in the diagram. The left part of Figure 3.6 shows the Space Vector Diagram for a thee-phase two-level inverter. In this case the voltage reference vector is inside the upper right triangle of the diagram. This means that the inverter will use the vectors 110, 100, and 111 or 000 to create output voltage like that the reference represents. Every number in a state nnn (for example 110) is connected to a phase-leg and represent the level wanted, 1 for positive voltage and 0 for negative voltage. The same applies for a multilevel Space Vector Diagram but the states includes more level, a state could for instance be 302 which would mean that one phase leg should put out voltage level 3, one leg voltage level 0, and one leg voltage level 2 for a calculated amount of time. A five-level Space Vector Diagram is shown to the right in Figure 3.6. The three vectors that would be used to recreate the reference in the multilevel Space Vector Diagram in the figure (if lowest level is 0 and highest 4) are 210, 220 and 320. Space Vector Modulation can be used with any multilevel inverter since its vector diagram are universal and has relative easy hardware implementation by a Digital Signal Processor [2]. However, with higher number of voltage levels the complexity of choosing switching states increases since the redundancy of switching states increases as well.

Space Vector Control (SVC), a low (fundamental) frequency space vector modulation method, does not, contrary to SVM, generate the desired mean load voltage value in every switching interval but for inverters with a higher number voltage levels the errors will be small in comparison to the reference vector [2]. SVC may therefore be adequate for inverter with higher number of voltage levels.

3.4 Selective Harmonic Elimination

Selective Harmonic Elimination (SHE) is a low switching frequency strategy that uses calculated switching angles to eliminate certain harmonics in the output voltage. With the help of Fourier Series analysis the amplitude of any odd harmonic in the output signal can be calculated. Usually the switcning angles are chosen so that the fundamental is set to the wanted output amplitude and the other harmonics to zero, see Figure 3.7. The switching angles must however be lower than $\frac{\pi}{2}$ degrees and for a number of switching angles a harmonic components can be affected, where $a-1$ number of harmonics can be eliminated[2] (one angle to set the fundamental). If angles were to be larger than $\frac{\pi}{2}$ an

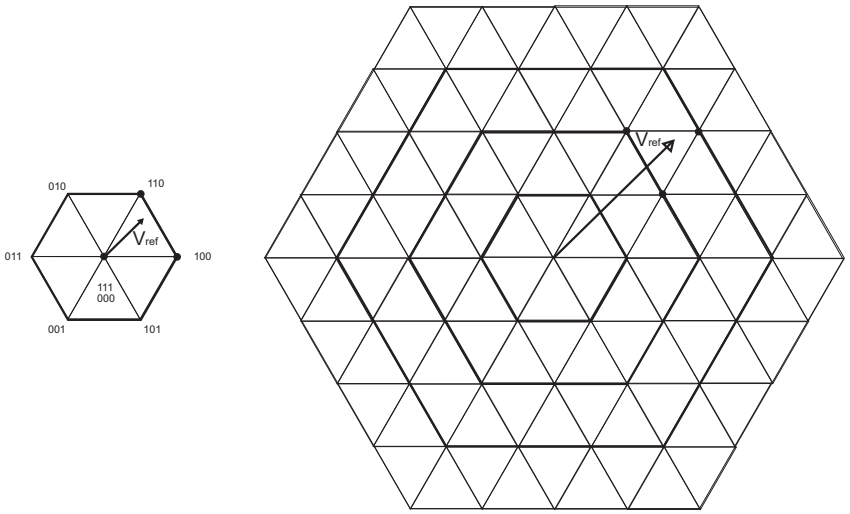

Figure 3.6: A two-level Space Vector Diagram, to the left, and a five-level Space Vector Diagram, to the right

correct output signal would not be achievable. For an inverter with m levels $a = \frac{m-1}{2}$. Higher harmonics can be filtered out with additional filters added between the inverter and the load if needed. For a five-level inverter $a = 2$, so there are two switching angles available and $a - 1 = 1$ angles can be used for harmonic component elimination.

In Figure 3.7 the first angle, $\alpha 1$, is set to modulate the fundamental signal amplitude the second angle, $\alpha 2$, is set to eliminate a chosen harmonic distortion. The Fourier Series equations for these signals are the following.

$$\frac{m_i * V_{max} * \pi}{4} = \frac{V_{max}}{2} cos(\alpha 1) + \frac{V_{max}}{2} cos(\alpha 2) \tag{3.1}$$

$$0 = cos(n * \alpha 1) + cos(n * \alpha 2) \tag{3.2}$$

$$m_i = \frac{V_{ref}}{\sqrt{2} V_{max}} \tag{3.3}$$

The variable n is in these equations is the number (multiple of the fundamental frequency) of the harmonic that is to be eliminated. For every switch angle available one cosine term i added to each equations and there are also as many equations as there are switching angles. So for a situation with a number of switching angles there are a number of equations with a number of cosine terms. As for this five-level inverter case there are two firing angles, two equations and two cosine terms in every equation. For a seven-level inverter the equation setup would instead be as the following. Variables n_1 and n_2 are the numbers of the two harmonics to be eliminated.

$$\frac{m_i * V_{max} * \pi}{4} = \frac{V_{max}}{3} cos(\alpha 1) + \frac{V_{max}}{3} cos(\alpha 2) + \frac{V_{max}}{3} cos(\alpha 3) \tag{3.4}$$

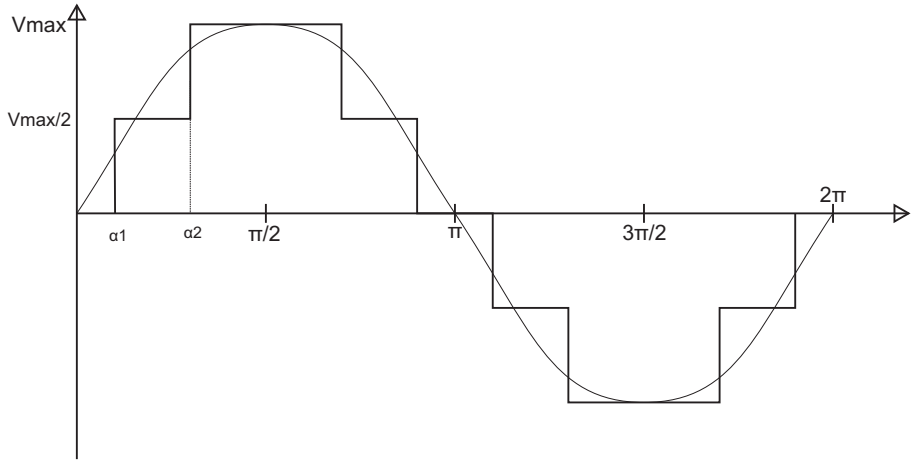

Figure 3.7: Switching with angles determined by Selective Harmonic Elimination for a five-level inverter

$$0 = cos(n_1 * \alpha 1) + cos(n_1 * \alpha 2) + cos(n_1 * \alpha 3) \tag{3.5}$$

$$0 = cos(n_2 * \alpha 1) + cos(n_2 * \alpha 2) + cos(n_2 * \alpha 3) \tag{3.6}$$

3.5 Power losses

Losses is an important aspect of power electronics since lower losses gives higher efficiency. Since the two-level and multilevel inverters can operate at different switching frequencies and with different balancing control schemes they will not have the same amount of power losses. To be able to investigate the switching losses in an inverter a model for losses is needed. The switching power loss P_{sw} during one second in a switch is defined by the formula

$$P_{sw} = \sum \frac{1}{2} V_d I_0 t \tag{3.7}$$

there V_d is the voltage over the switch when off, I_0 is the current through the switch after turned on or before turned off and t is either the turn on time t_{on}or the switch off time t_{off} [18]. The sum of all the switching loss event energies during one second for one switch results in that switch's switching power loss. The switching loss energies can be divided into the turn on and turn off loss energies as

$$E_{sw,on} = \frac{1}{2} V_d I_0 t_{on} \tag{3.8}$$

$$E_{sw,off} = \frac{1}{2} V_d I_0 t_{off} \tag{3.9}$$

During one second $E_{sw,on}$ and $E_{sw,off}$ are lost a number of f_{sw} times, where f_{sw} is the switching frequency of the switch, so the sum of the switching energy losses equals the switching power losses. Also the number of switches in a circuit has to be included.

$$P_{sw} = \sum(E_{sw,on} + E_{sw,off}) = \sum E_{sw,tot} \tag{3.10}$$

$$P_{sw,tot} = N_{sw} \sum(E_{sw,on} + E_{sw,off}) = N_{sw} \sum E_{sw,tot} \tag{3.11}$$

where $N_{sw}$is the number of switches in the inverter. For these equations it is assumed that the same voltage lies over all switches and also that the same current flows through them. Both voltage and current used for with these equations are values measured every sampling instance during simulations. Since voltages and currents does not change between sampling instances during simulations the current $I_0$and voltage V_d can be assumed to be constant for every term in the sum calculations. Diodes, like clamping diodes or those in parallel with switches, also have turn off losses that needs to be included. Also, when the current is negative (positive current down through switch) the current goes through the diode in parallel to the switch and the switch has no losses. The diode turn off energy loss is similar to that of the switch.

There are also conduction losses in the semiconductor devices. These are not dependent on the inverter switching frequency but on the voltage over and current through the device. The on-state resistance in the devices is also important for conduction loss calculations. For a time t_{cond} that a semiconductor is on and conduction the conduction energy losses can be calculated with

$$E_{cond} = t_{cond}(V_t I_0 + R_{on} I_0^2) \tag{3.12}$$

where R_{on} is the on-state resistance and V_t the voltage over the device during on-state (threshold voltage). Also here the voltages and currents are measured at every sampling instance during a simulation and hence the currents and voltages can be assumed to be constant for each term in the sum calculation. To get the total conduction power losses for all devices during one second the conduction energies for all switches has to be summed up.

$$P_{cond,tot} = N_{sw} \sum E_{cond} \tag{3.13}$$

4 Balancing

4.1 Prioritizing

For the topologies where there are redundant switching states, such as the CMCI and M2I topologies, the voltage unbalance problem can be solved with the modulation by choosing a switch state that corrects the unbalance. This can also be called prioritizing. By prioritizing in which order that voltage sources are to be used the workload can be divided between the sources so that they are held balanced. The prioritizing order is dependent on the current direction and if voltage amplitude is negative or positive. If, for example, a capacitor in a full-bridge module for the CMCI has a higher charge (and therefore higher potential) that certain module can be given the heaviest workload during a period where the capacitor is going to be discharged (positive voltage and current flowing to the load), lowering the voltage closer to the wanted value. The strategy can also work the other way around, to charge capacitors with lower potential by connecting them to the load, with positive potential forward, when current is flowing from the load, or vice versa. However, this strategy is most effective when transferring active power. When transferring only reactive power the sources does not get unbalanced and this balancing strategy is not necessary.

4.2 Additional circuits

If voltage balancing by modulation is not achievable, available or for other reasons not implemented, additional circuits can be used to balance the capacitor voltages. These balancing circuits aim to charge or discharge the capacitors so that they keep the same voltage.

One example of a balancing circuit for the NPCMLI is that found in [16], see Figure 4.1. This balancing circuit is to be implemented in parallel over two DC-capacitors, so for the five-level NPC inverter two of these circuits are needed. It aims to exchange energy between capacitors C1 and C2 through the inductor. The circuit has three states, one connecting to C1, one freewheeling state and one connecting to C2. When connected to one of the capacitors energy is flowing out or in from the capacitor through the inductor. Later when connected to the other capacitor the energy from the inductor either charges or discharged that capacitor, equalizing the voltage between the capacitor pair. The freewheeling state serves as a transition from one capacitor to the other so that the two switches that are on in the inverter shares the voltage equally.

The control for this circuit is built up by two PI controllers, one outer to control the voltage difference between the capacitors and one inner to control the inductor current.

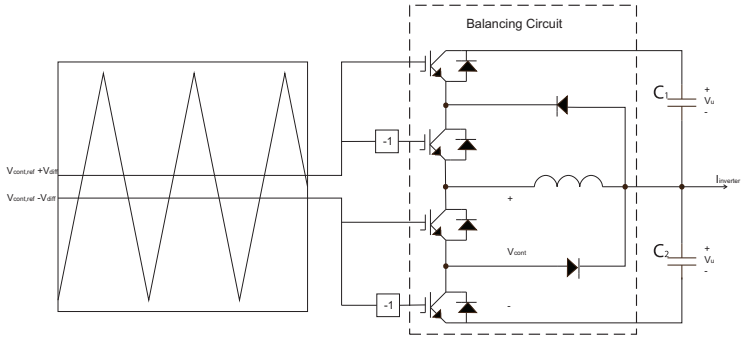

Figure 4.1: The NPC Inverter balancing circuit and the modulation for the switches. C1 and C2 are the DC-bus capacitors in the inverter, see Figure 2.1

The output of the two controllers modulates the time the balancer is connected to each circuit. The size of the inductor, and its resistance, and the wanted bandwidth of the system decides the values for the PI controller constants. The controller constants should also be transformed to state space form and discretisized. The balancing circuit does not need any specific modulation method for the NPC inverter. A model for the balancer circuit system and the regulators can be seen in 4.2. The modulation for changing switch states in the balancer is made with a triangular carrier wave in comparison with a reference that is modulated by the voltage difference from a capacitor pair. If the capacitors are balanced the reference is in the middle of carrier waves top and bottom value. To use the freewheeling states the reference should be made in to to references with a small space between, one reference to control the first and third switch and one reference to control the second and fourth switch, counting from the top in Figure 4.1. The state of the third switch is inverted compared to the state of switch one and also the state of the fourth switch is inverted compared to the state of the second switch.

To design the regulators the system withing them can be seen as a first order system and with chosen bandwidths the regulators constants can be calculated. The bandwidth for the inner current controller should be four to ten times larger than that of the outer voltage controller. Also the balancing circuit carrier wave frequency should be four to ten times higher than that of the current controller. The variable C in the equations below is the value for the source capacitors (in this case the capacitors C1 and C2 in Figure 4.1).

$$F_{current}(s) = \frac{\alpha_c}{s}(sL + R) = \alpha_c L + \frac{\alpha_c R}{s} = K_{pi} + \frac{K_{ii}}{s} \tag{4.1}$$

$$F_{voltage}(s) = \frac{\alpha_v}{s} Cs = \alpha_v C + \frac{0}{s} = K_{pv} + \frac{K_{iv}}{s} \tag{4.2}$$

$$\alpha_c > \alpha_v \tag{4.3}$$

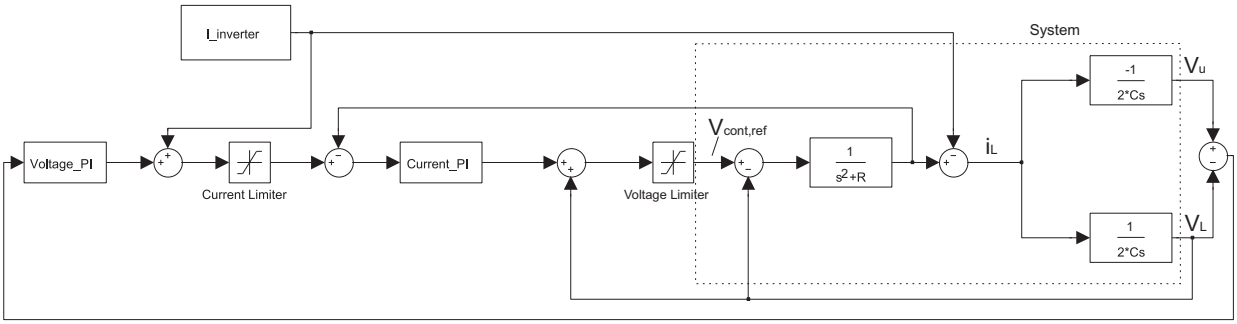

Figure 4.2: Model for the voltage Balancer circuit and the regulators

4.3 Balancing with three-phase

With a three-phase setup it is possible to modulate balancing for the NPCMLI through the choice of zero-sequence component [15]. Since the states for the NPCMLI tends to eject and inject current from certain DC-capacitors, by raising or lowering the same number of voltage levels in all the three phases which capacitors that will be charged or discharged can be chosen without that the three-phase output changes for the load. This will for instance mean that if all phase-legs in a inverter raise their states to one voltage level higher at the same time, as long as the load is not grounded, it will still see the same three-phase output as before. The currents will however flow differently in the inverter during this state than the one before the inverter raised a level in all its legs. By knowing how currents flow during different states this can be used for balancing.

However, when using this method there must be margins in the available output voltage [16]. To be able to change to an alternative state there must be a higher or lower voltage level for each phase to choose from, making this method less flexible. For the same range of output voltage this method requires an inverter with higher input voltage range. This is one reason to that this method not will be discussed or used further in this report.

5 Topology Evaluation

5.1 Component Rating Comparison

One of the advantages with multilevel inverters against ordinary two-level inverters is that the voltage is divided over more components, decreasing the requirements of every individual component. In this way cheaper components can be used for the inverter instead of fewer expensive higher rating components. Still, the question of a topologys component rating requirements is important and for the different topologies the specifications differ. Since all components in the VSI topologies needs to withstand the same amount of voltage this comparison is not only valid for switches. All the inverter topologies have the same maximum output voltage in their descriptions, $\sqrt{2}V_a$, and the same output current, I_a, for valid comparison. Since all inverters are not equal in design all inverters will not have the same input voltage or ratings for their components. In this way the input and rating requirements for the inverters can be compared while having common outputs. Table 5.1 show the rating requirements for each topology valve and in Figure 5.1 two plots to describe the ratings as a function of level m are displayed. Plot a) shows the voltage rating requirements for the inverters in two groups, VSI:s and CSI (voltage source and current source inverters). Plot b) shows the current rating requirements for all components divided into the two groups VSI:s and CSI. As can be seen, the voltage rating for the VSI:s decreases for each level m but stays constant for the CSI. For current rating the case is the opposite, the ratings for the CSI decreases for every level m while the current ratings stays constant for the VSI:s. The "Minimum DC voltage" in Table 5.1 means the required DC side input voltage in terms of RMS output voltage V_a.

For the GMCSI topology it is assumed that the peak phase output voltage is also V_a as it is with the the other VSI topologies. The voltage over two valves between two modules will then be the line-to-line voltage $\sqrt{6}V_a$, or $V_{dc}\frac{\sqrt{3}}{2}$. Depending on switching state these two switches can be both on, both off or one on and one off. In the case where one is on and one is off the maximum voltage over the switch that is turned off is the peak line to line voltage, see Figure 2.12. Hence, this is the voltage each switch must withstand.

Table 5.1: The topologies rating requirements per level m, if maximum output voltage is V_a (RMS) and load current is I_a (RMS).

Topology	Two-level	NPCMLI	CCMLI	CMCI	GMLI	RVMLI	M2I	GMCSI
Component voltage rating	V_{dc}	$\frac{V_{dc}}{m-1}$	$\frac{V_{dc}}{m-1}$	$\frac{V_{dc}}{m-1}$	$\frac{V_{dc}}{m-1}$	$\frac{V_{dc}}{m-1}$	$\frac{V_{dc}}{m-1}$	$\sqrt{6}V_a$
Minimum DC voltage, $V_{dc} =$	$2\sqrt{2}V_a$	$2\sqrt{2}V_a$	$2\sqrt{2}V_a$	$\sqrt{2}V_a$	$2\sqrt{2}V_a$	$\sqrt{2}V_a$	$2\sqrt{2}V_a$	-
Active component current	I_a	I_a	I_a	I_a	I_a	I_a	I_a	$\frac{2I_a}{m-1}$

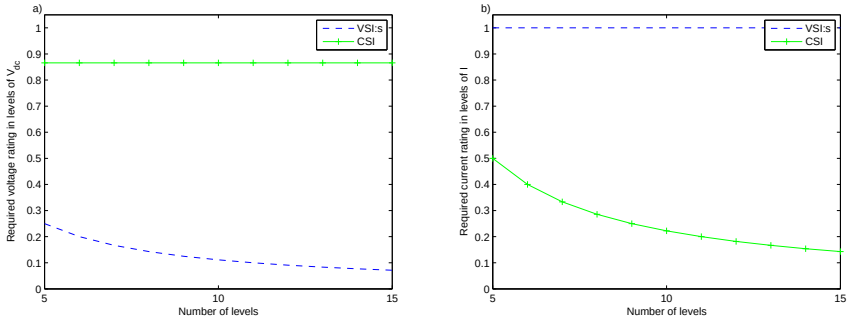

Figure 5.1: The voltage and current rating requirements for the components as a function of voltage level m. Component voltage rating in a) and component current rating to in b)

5.2 Component Quantity Requirement Analysis

The topologies presented in the earlier chapter all have similar function but differs in their constructions. In this section of the report the component quantity requirements for the topologies will be compared and analyzed.

5.2.1 Individual rating comparison

In Table 5.2 the numbers of components needed per level are displayed. All equations are for a three-phase setup for every topology without the DC-bus capacitors being shared for any setup. All the values in the table are for individual cases, only the number of components that are needed for each topology and rating requirements suitable for its own setup. In Figure 5.2 the component requirements as stated in Table 5.2 is shown, without rating comparison between the inverters taking into account. Only the lowest voltage and current rating for each individual inverter for itself is considered. The ratings for each inverter are those stated in Table 5.1. Most similarities can be seen in the need for main switches and diodes, most of the topologies have similar needs for those components, except for the GMCSI that here uses GTO switches instead of IGBT switches with diode in parallel. However, IGBT with series diodes can be used for the GMCSI as well [9]. For the other topologies choice of switches, the switching frequency, which is depending on modulation method, is somewhat determining the choice of switching components. Here IGBT:s with parallel diodes are used.

5.2.2 Lowest common rating comparison

To make the comparison more fair it would be good to take into account the rating requirements discussed in the chapter before so that component with the same ratings are added together. The lowest common ratings would be the lowest ratings in any of the inverters in Table 5.1. The voltage ratings for the inverters where either $\frac{\sqrt{2}V_a}{m-1}$,

Table 5.2: Component Requirements for the Topologies for a three-phase setup. The voltage/current level is represented by m. DC-buses are not shared between the phases.

Topology	NPCMLI	CCMLI	CMCI	GMLI	RVMLI	GMCSI	M2I
DC-bus cap./ Isolated sources	$3(m-1)$	$3(m-1)$	$3\frac{m-1}{2}$	$3(\frac{m(m+1)}{2}-m)$	$3(\frac{m-1}{2})$	1	$6(m-1)$
Main diodes	$6(m-1)$	$6(m-1)$	$6(m-1)$	$6(\frac{m(m+1)}{2}-m)$	$3(3(m-1))$	0* $6(\frac{m-1}{2})$**	$12(m-1)$
Main switches	$6(m-1)$	$6(m-1)$	$6(m-1)$	$6(\frac{m(m+1)}{2}-m)$	$3(3(m-1))$	$6(\frac{m-1}{2})$* $6(\frac{m-1}{2})$**	$12(m-1)$
Clamping diodes	$3(m-1)(m-2)$	0	0	0	0	0	0
Clamping cap.	0	$\frac{3(m-1)(m-2)}{2}$	0	0	0	0	0
Smoothing ind.	0	0	0	0	0	$\frac{m-3}{2}(\frac{m-3}{2}+1)$	6
Transformers	0	0	0	0	3***	0	0

*GMCSI with GTO switches
**GMCSI with IGBT switches and parallel diode (not used in plots and comparisons)
***Three transformers as in one transformers for each phase in a three-phase setup

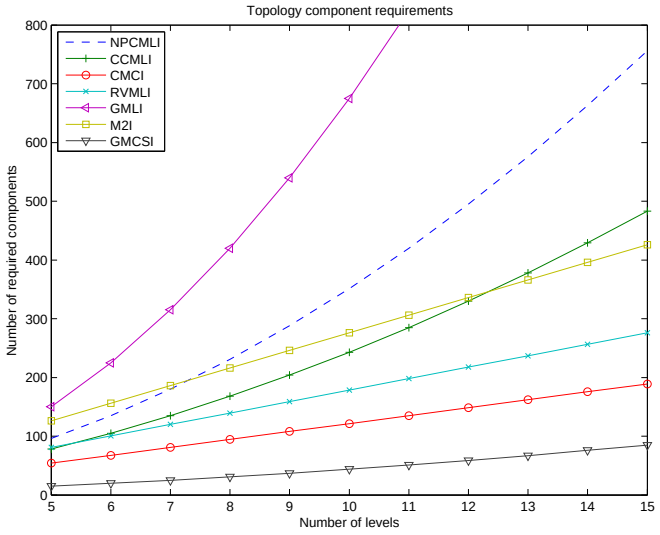

Figure 5.2: Components needed for the topologies as a function av voltage/current level without rating comparison between inverters taken into account

$\frac{2\sqrt{2}V_a}{m-1}$ or $\sqrt{6}V_a$ (for the CSI). For any level m, $\frac{\sqrt{2}V_a}{m-1}$ is the lowest voltage rating so the GMCSI would then have $\sqrt{3}(m-1)$ more components than stated in Table 5.2 in series to withstand the voltage. This number would also have to be rounded up so that a whole number of components are added. Also other voltage source inverters, such as the NPCMLI, which have twice the ratings than the CMCI, M2I and RVMLI, will need twice as many components in series to withstand the voltages. The current rating of the components is decided by the GMCSI, since the lowest amount of current rating only changes with level m for this topology. For the VSI:s to be able to withstand the current with the available lowest current rating components the number of components in Table 5.2 must be multiplied with $\frac{m-1}{2}$, where the added components are to be connected in parallel to divide the current between them. The component multiplication factors for each topology, both for withstanding voltage and current, can be seen in Table 5.3.

Figure 5.3 shows the total component requirements as a function of voltage or current level presented in Table 5.2 with added components with aspects to ratings, as discussed. As can be seen, and earlier mentioned, the NPCMLI greatly outnumbers the other topologies with higher levels and also the CCMLI shows its quadratic component requirement. This is because of the clamping diodes and capacitors. Only the GMLI shows a higher number of components which is caused by the rate of needed P2-cells for each level. The topology with the lowest component requirements is the CMCI followed by RVMLI and also the GMCSI. Visible is also that, because of the added components to withstand voltages (a multiplication by four for a five-level case), the GMCSI also requires a higher number of components compared to the individual rating comparison (where the GMCSI needed the lowest number of components).

For low numbers of levels the GMCSI and the CMCI need about the same amount of components. For higher levels the NPCMLI, CCMLI and GMLI strongly shows their quadratic component requirements. Also at 13 levels the GMCSI has a small amount less components than the RVMLI, but after that level the GMCSI needs more components than the RVMLI. In general, however, the CMCI, GMCSI and RVMLI are the inverters with the lowest amount of needed components, in that order. As can be seen there are some differences, especially for the GMCSI and M2I topologies, between this lowest common component rating case and the individual topology rating case in Table 5.2 and Figure 5.2. The M2I inverters components require lower voltage ratings than the NPCMLI, CCMLI and GMLI so it has here lower component requirements compared to them. The GMCSI additional components to withstand voltages, as high as seven times more components as early as for $m = 5$, makes so that this inverter topology no longer has the lowest amount of components. Since the CMCI already used the lowest rating voltage components and the setup is truly modular, with no extra components outside the modules (as with the M2I inverter), it benefits the most from the lowest common component rating comparison, with the least number of needed components.

Table 5.3: Component multiplication factors for the inverter topologies to withstand voltages and current when using a lowest common component rating, as a function of level m

Topology	NPCMLI	CCMLI	CMCI	GMLI	RVMLI	M2I	GMCSI
Multiplication to withstand voltage	2	2	1	2	1	1	$\sqrt{3}(m-1)$
Multiplication to withstand current	$\frac{m-1}{2}$	$\frac{m-1}{2}$	$\frac{m-1}{2}$	$\frac{m-1}{2}$	$\frac{m-1}{2}$	$\frac{m-1}{2}$	1

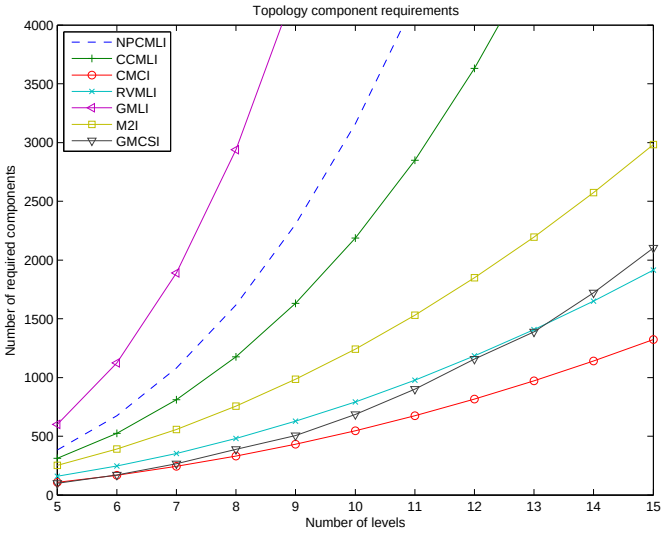

Figure 5.3: Components needed for the topologies as a function of the voltage/current level with added component because of rating requirements

5.3 Strengths and weaknesses of the topologies

Because of the topologies different designs they also have separate properties that distinguish their suitability for different applications and situations. Their design and basic principle has been presented earlier in this work but for further evaluation a short and simple view on the topologies positive and negative properties could be helpful. The advantages and disadvantages are listed for every topology below.

Neutral-Point-Clamped Multilevel Inverter (NPCMLI)

+	High efficiency since fundamental switching frequency can be used for all devices
+	Controllable reactive power flow
+	Simple control method for back-to-back power transfer system
-	High number of clamping diodes with high number of voltage levels
-	Difficulties with active power flow [3]
-	Capacitor Voltage Balance problem that need complex modulation

Capacitor Clamped Multilevel Inverter (CCMLI)

+	Capacitors can function as power storage during outage [3]
+	Voltage balancing with redundant switching states
+	Can control both active and reactive power transfer
-	Requires many capacitors
-	Complicated control, leading to high switching frequency and losses, when transferring real power

Cascaded Multicell Inverter (CMCI)

+	Requires a low number of components per level
+	Modularized structure without clamping components
+	Possibility to implement soft-switching
+	Simple voltage balancing modulation
-	Needs separate isolated DC sources for real power transfer
-	No common DC-bus

Generalized Multilevel Inverter (GMLI)

+	True multilevel structure with auto voltage balancing
+	Able to eliminate need of transformer
+	Suitable for DC/DC applications [5]
-	Number of components required is not linear

Reversing	**Voltage Multilevel Inverter (RVMLI)**
+	Few components required, essentially with higher number of voltage levels
+	Low switching frequency implementable
+	No need for voltage balancing for certain applications
-	Uses isolated sources
-	Need for one transformer per phase
Modular	**Multilevel inverter (M2I)**
+	Modular design
+	Low number of components
+	Simple voltage balancing
-	Many DC-capacitors
Generalized	**Multilevel Current Source Inverter (GMCSI)**
+	Very few components required
+	Modularized design
+	Inductor current balancing capabilities
-	Needs additional logic together with SPWM [9]

5.4 Application Examples

In this report the focus is on high and medium power applications and a electric vehicle propulsion converter and a converter for the electric power grid system are used here as application examples.

5.4.1 Hybrid Electric Vehicle Application

Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV) are becoming more and more popular and they are more than likely to be a part of a more sustainable society. Depending on EV/HEV configuration, the power train need one or more converters/inverters to feed power for propulsion. The electric system of a EV/HEV uses series and parallel connected battery cells as power source. The voltage level of these batteries needs to be controlled with extra circuitry so they are equally charged. High efficiency, to achieve long driving range, is important but compact design and light weight of the power electronics, and other devices, are also essential. There are also EMI regulations. A simple example of a EV electric power train setup can be seen in Figure 5.4.

An MLI topology suitable for implementation in a HEV should, with the aspects above in mind, be able to deliver an alternating voltage with low losses and take advantage of

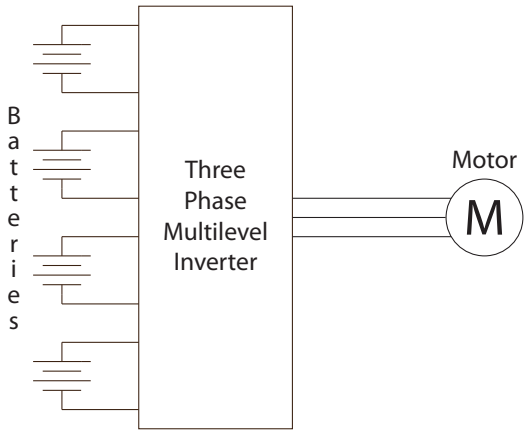

Figure 5.4: Hybrid Electric Vehicle/Electric Vehicle power train

the multiple battery cells setup used in EV:s/HEV:s with weight and efficiency prioritized. Real power transfer is important for this case so the chosen topology should have no problems with or effective solutions for voltage unbalances. If the inverter in itself could control the voltage levels of the sources that would be an advantage. In line with efficiency and light weight there is also need for low EMI, preferably without filters, so low distortions is an important quality for the MLI topology.

With aspect to these design requirements for an application with several battery cells as power source, the CMCI topology has been chosen for the EV/HEV application simulation in this work. Dividing the batteries into several isolated DC sources, as shown in Figure 5.4, real power can be transferred without voltage unbalance problems when correct modulation is applied. This makes the CMCI suitable for this application. Charge balance in the batteries must however be controlled but since the CMCI topology can control the sources workload with the modulation, there is no need for extra balancing circuits. This leads to lower weight and higher efficiency. Another advantage with the topology is that low amounts of components are needed (leading to lower weight), compared with other multilevel topologies, see Figures 5.2 and 5.3. The topology setup can also be combined with the battery cell setup where the cells in series can be for build up one phase-leg, taking advantage of the topologys modular setup, and cells in parallel can build up several phases. With enough voltage levels the CMCI should also be able to produce an output voltage with low distortions. The ability to switch at fundamental frequency also leads to high efficiency, extending the driving range for the vehicle (this is however, as stated, not a special feature for the CMCI).

Another topology that could have been used for these simulations is the M2I topology. The M2I topology could also make good use of its modular design and balancing methods. However, even though the M2I uses a low number of components the CMCI needs even fewer (see Component Comparisons in Section 5.2) and the M2I also needs more sources than the CMCI (see Section 5.3). Because of this the CMCI was chosen over the M2I.

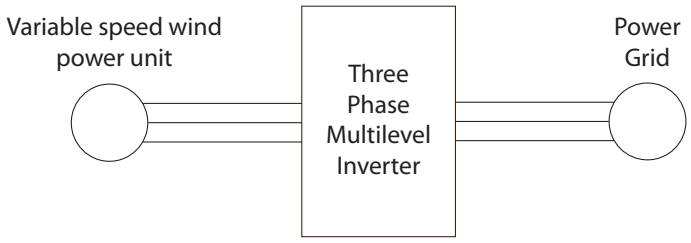

Figure 5.5: Power Grid Application example

5.4.2 Electric Power Grid Systems

In line with more decentralized power generation and smarter power grids with more renewable power sources new requirements follows. DC/DC, AC/DC and AC/DC conversion is required for several applications such as HVDC-transmission application and back-to-back configurations for asynchronous grid connection [3], for example for connecting wind farms with the power grid, see Figure 5.5. There is also need for reactive power compensation and power outage/voltage dip compensation. Low EMI and high efficiency are also among the requirements. For power grid applications a common DC-bus is necessary when power is to be transferred.

An MLI topology suitable for Electric Power Grid applications should be able to be used in compensations applications and FACTS but also have rectifying capability so that it may be used for HVDC-transmission and similar applications. It would also be preferred if the use for high power transformers could be minimized or eliminated. For some applications there is however no need for transformer elimination, for example HVDC where transformers exists anyway. For some of the applications there is active power transfer and chosen application need a solution to the voltage unbalance problem for these cases. The MLI topology should also have high efficiency and be able to produce low EMI and other distortions to avoid large filters. Chosen available topology should also be able to transfer both active and reactive power, however not necessarily at the same time, and must also have a common DC-bus to be suitable for power grid system applications.

For the Power Grid case several of the presented topologies are suitable for one or more of the interesting applications, for example reactive power compensation [3]. The three biggest topologies, the NPCMLI, CCMLI and CMCI, can all be used in reactive power compensation without voltage unbalance problem but only the NPCMLI and CCMLI have a common DC-bus and are possible in back-to-back configurations. The GMLI can auto-balance the capacitor voltage but uses the most components. The RVMLI uses the least amount of components and was proposed to be used in HVDC [7] but it require isolated sources and transformers for balanced operation.

With aspect to industrial popularity [13], design simplicity, suitability for back-to-back and reactive power compensation the NPCMLI have been chosen for simulation for the Electric Grid System case in this work. With the proposed vector control method in [14] and [15] the capacitor voltage unbalance can be controlled which makes the NPCMLI a

attractive choice. The NPCMLI can transfer both reactive and active power, as mentioned, have a common DC-bus and the topology itself have no need for transformers. Several balancing methods are known for the NPCMLI and the ability to function with low switching frequency leads to high efficiency. Also, the multilevel setup creates low distortions, lowering need for big filters.

6 Simulation Results and Loss Calculations

6.1 Simulation scope

The two selected MLI topologies, the NPCMLI and CMCI, are compared with each other and with a conventional two-level PWM inverter to investigate the differences between multilevel technology and ordinary two-level technology. For the comparison quality issues such as harmonic components and THD are used together will calculated switching and conduction losses. The capacitor voltage balance problem have been investigated for both MLI topologies.

Simulations for the NPCMLI have concerned one pure reactive power case to examine its capability for VAR compensation and one case with mixed active and reactive power transfer to investigate the topologys suitability for applications such as HVDC transmission. The CMCI topology will be tested with the same sets of simulations, pure reactive and mixed active and reactive power transfer, with concern on equal discharge of the voltage sources. For performing the simulations PSCAD v.4.2.1 is used and the simulation result are presented with the tools in MatLab.

6.2 Simulations models and component values

The three simulations models used are the two-level inverter, the five-level Cascaded Multicell Inverter (CMCI) and the five-level Neutral-Point Clamped Inverter (NPC). These models can be seen in Figures 6.1, 6.2 and 6.3. The values for the two load cases, reactive power transfer and mixed power transfer, can be seen in Table 6.1. The small amount of resistance in the reactive load represents some active losses and it removes the DC-component in the output current. This DC-component will appear in the beginning of the simulations due to that the simulations are performed without a current controller. The values for the capacitors are for the two-level inverter 2000uF, for the CMCI 10000uF and for the NPC 4000uF. The inductance in the NPC balancing circuit is 0.01 H with a resistance of 0.1 Ohm. These values where taken from the report [16] in which the balancing circuit was found since that also used the same value for the DC-capacitors. The switching frequency for the balancing circuit is 500 Hz. The current PI controller bandwidth was chosen to $\alpha_i = 2\pi 100$ rad/s and the voltage PI controller bandwidth was chosen to $\alpha_v = 2\pi 20$ rad/s.

Table 6.1: Simulation values for the two different simulation cases

	R [Ohm]	L [H]	V_a(RMS) [kV]	$I_{a,ideal}$ (RMS) [kA]	P_a [kW]	Q_a [kVAR]
Reactive Load	0.05	0.1	0.65	0.020	0.021	13
Mixed/Active Load	25.05	0.1	0.65	0.016	6.6	8.2

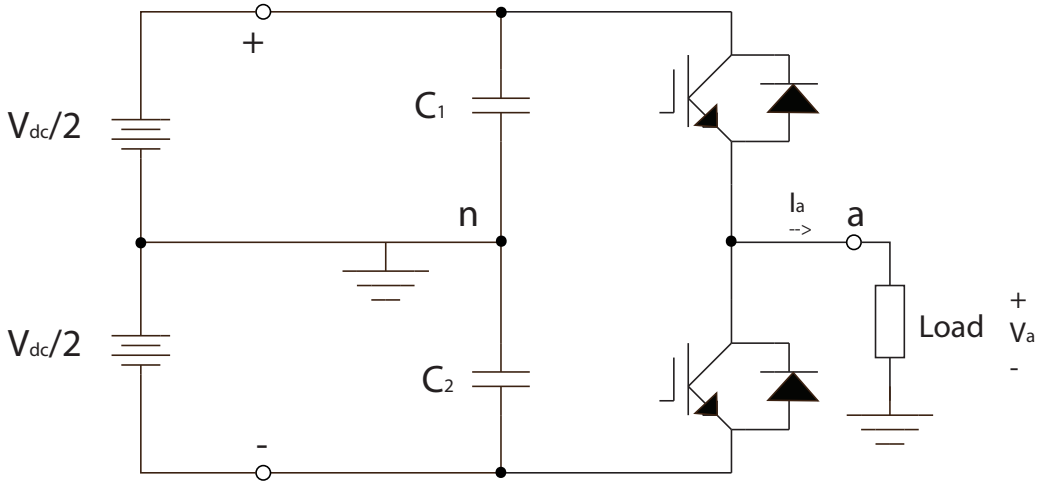

Figure 6.1: Two-level simulation model

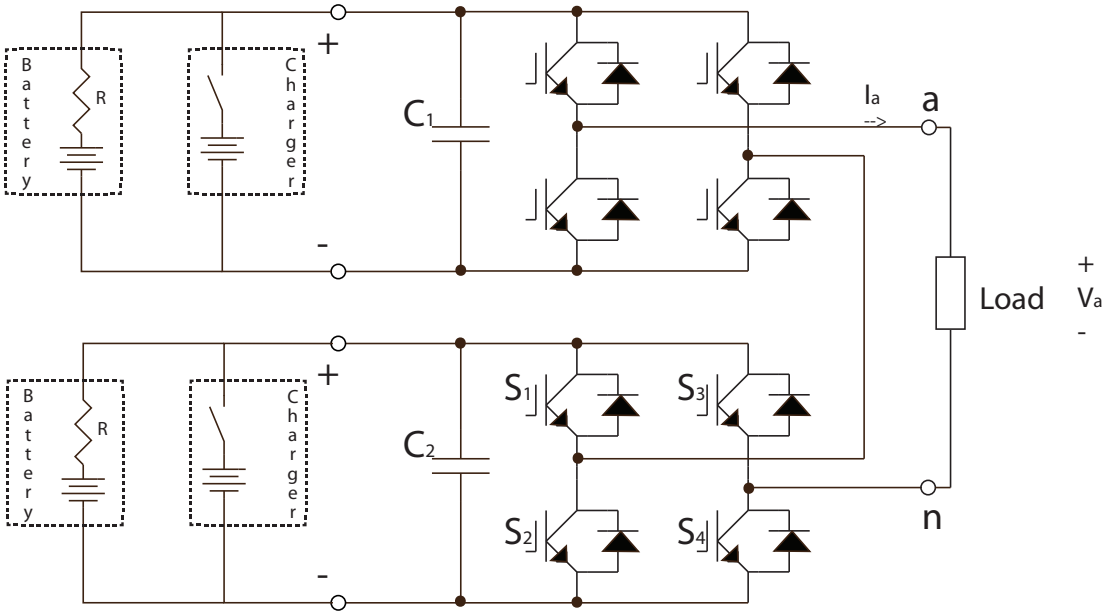

Figure 6.2: Five-level Cascaded Multicell simulation model

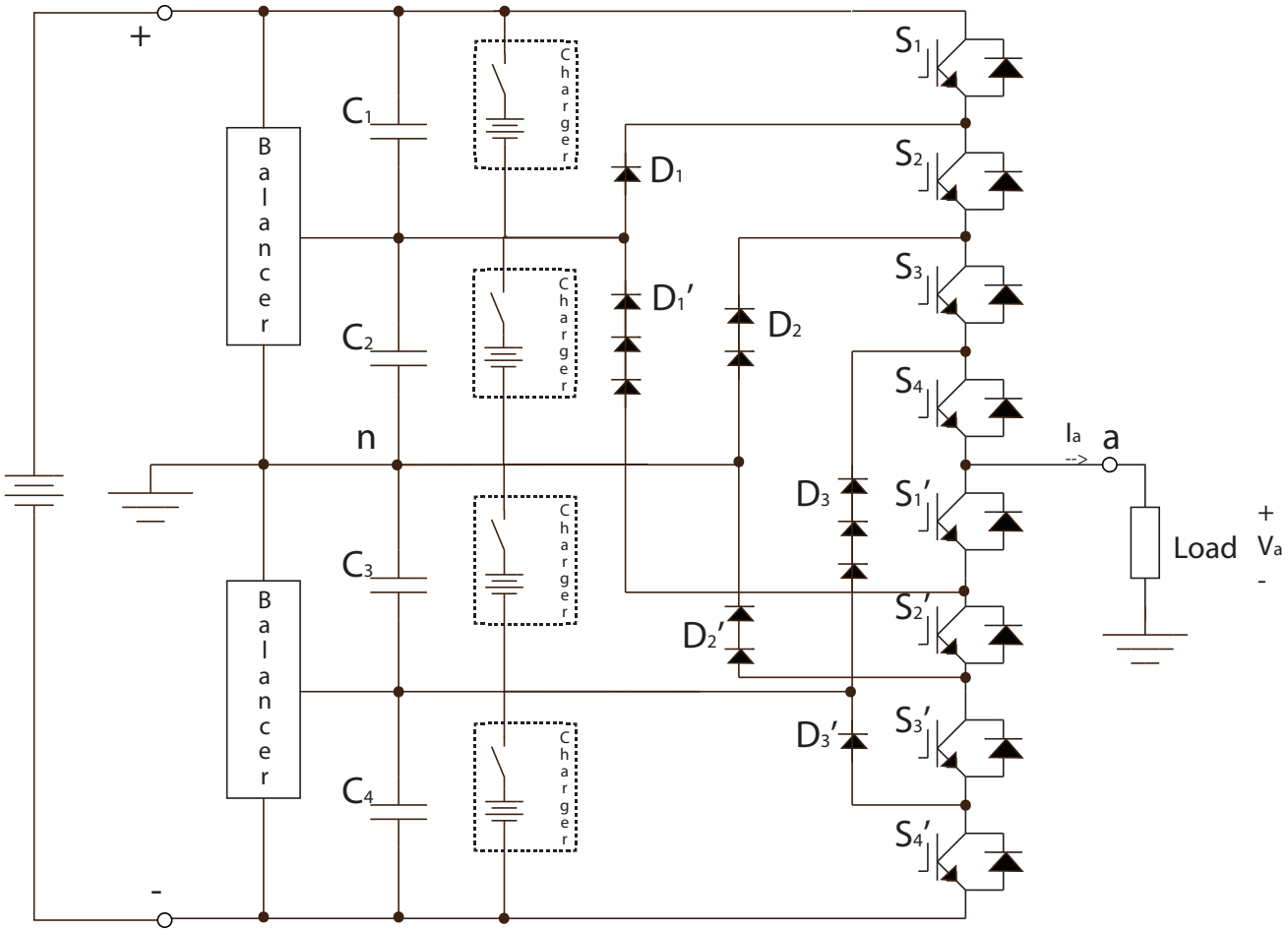

Figure 6.3: Five-level Neutral-Point Clamped simulation model

6.3 Voltage balance for the selected MLI:s

6.3.1 Voltage balance for the Cascade Multicell Inverter (CMCI)

The Cascaded Multicell Inverter (CMCI) with its use of several voltage sources is suitable in Electric Vehicles (EV) since battery cells is the power source. The battery cells may not always be equal and depending on the output demand the cells may be discharged unequally. It is therefore important to investigate the voltage source unbalance problem in the CMCI.

In Figure 6.4 the results of the five-level CMCI connected to an active/mixed power load and a pure reactive power load can be seen. Each capacitor where charged to 500V during the beginning of the simulation with the charging voltage source, see Charger in Figure 6.2. The charging voltage source where disconnected after the circuit reached steady-state operation. It should be noted that there are battery models connected to each module capacitor, recharging them over time so that they do not run out of stored energy. The battery models are rated to 500V with a resistance of 10 Ohm (see battery in Figure 6.2). The reason for the big battery resistance is that the sources should not be recharged to fast, so that the discharging and unbalance characteristics can be seen clearly.The modulation in the simulation was PSCPWM at 1050Hz switching frequency and the output voltage frequency was 50Hz. An odd multiple of the output voltage frequency is used for switching to eliminate output current offset, mainly for the pure reactive simulations.

As can be seen in Figure 6.4 the voltages of the two capacitors C1 and C2 in the CMCI are balanced at steady normal operation. This is because that the PSCPWM discharges the sources equally, but it needs high switching frequency to do so. However, when the capacitors are charged with different magnitudes of voltage the voltages does not re-balance for any of the cases. In this work the voltage unbalance for the CMCI has been solved by adding the principle of voltage source prioritization, discussed earlier in Chapter 4. The modulation method uses $m-1=4$ carrier waves, two for positive voltage levels and two for negative voltage levels, like the PDPWM modulation in Subsection 3.2.2. Depending on what voltage source has the most charge the modulation compares the most prioritized inverter modules to the carriers closest to zero and those will hence be on during the longest time letting the less charged voltage sources catch up. This also means that there is no injection of current for balancing the sources, which makes the method slow, specially for pure reactive power transfers. The results from active and reactive power transfers can be seen in Figure 6.5 for the five-level CMCI.

Plot a) in Figure 6.5 shows the capacitors voltage after some time of operation for the pure reactive power transfer case. At this point the voltages are balanced but the duty priorities does not change. Due to the fact that the capacitors charge, while transferring only reactive power, does not change over one fundamental cycle. At the beginning of the simulation the capacitors where charged with different voltages, meaning that the higher charged module had the heaviest workload until a balanced state where reached. The beginning of the simulation is not seen in plot a) in Figure 6.5, see plot a) in Figure 6.6 where the capacitors are first unbalanced. The b) plot in Figure 6.5 is for active power

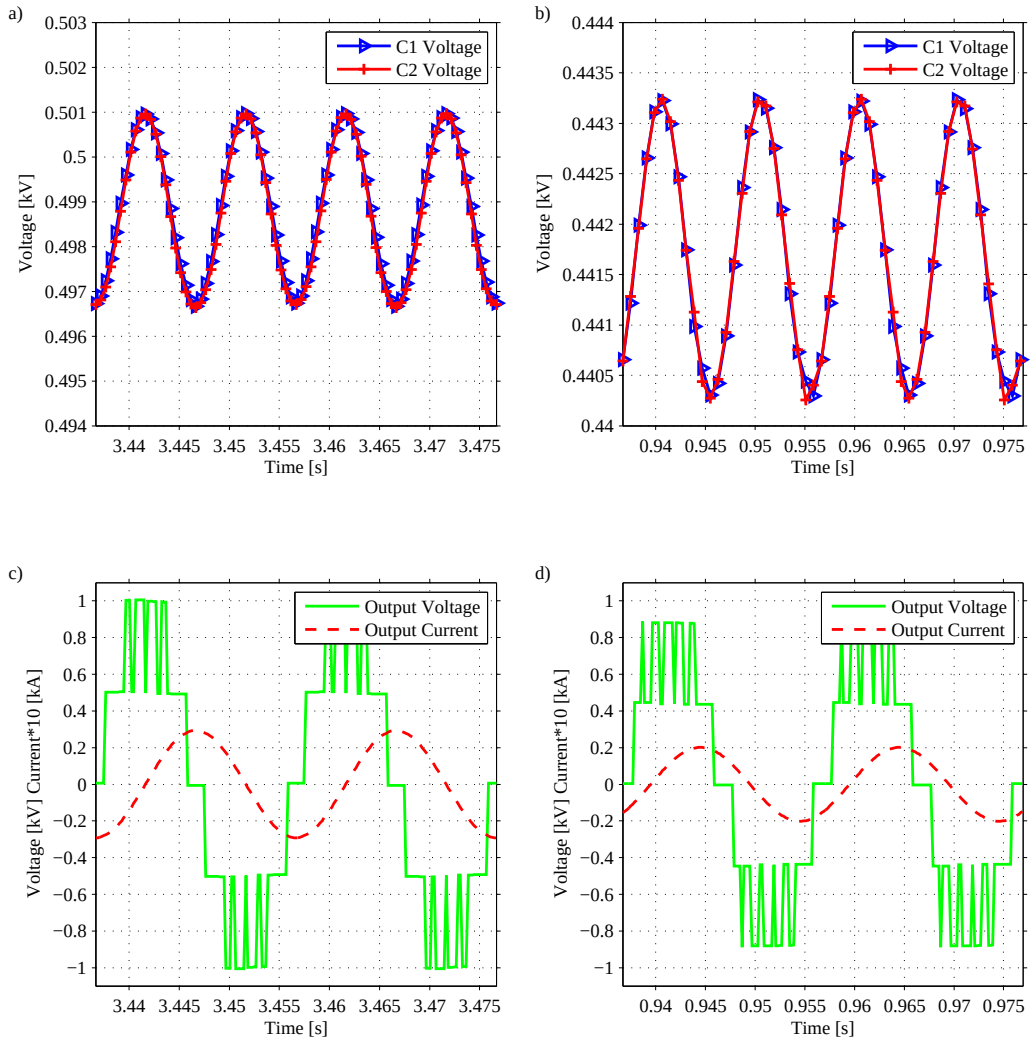

Figure 6.4: Unbalanced Simulation for the CMCI. a) Reactive power transfer capacitor voltages. b) Active/mixed power transfer capacitor voltages. c) Reactive power transfer load voltage and current. d) Active power transfer load voltage and current.

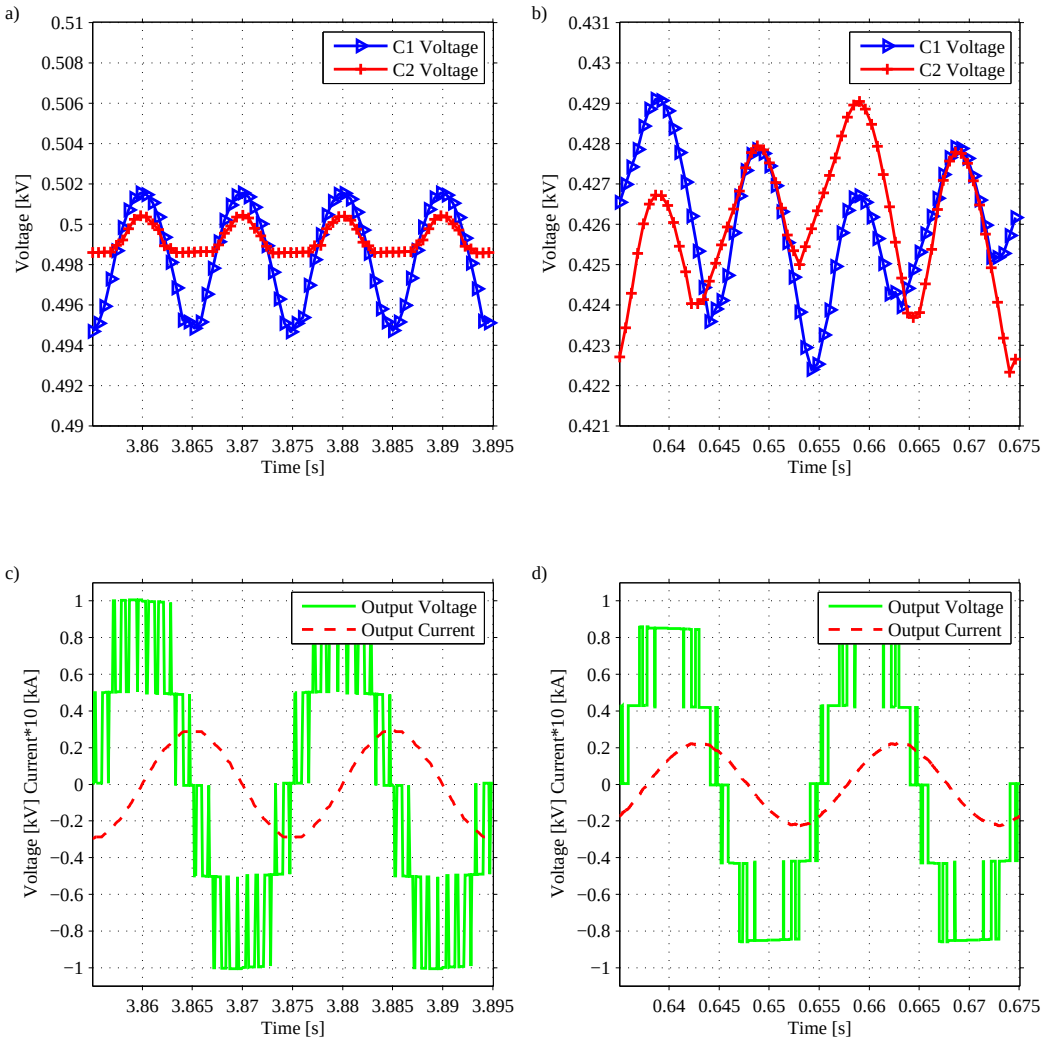

Figure 6.5: Balanced Simulation for the CMCI. a) Reactive power transfer capacitor voltages. b) Active/mixed power transfer capacitor voltages. c) Reactive power transfer load voltage and current. d) Active power transfer load voltage and current.

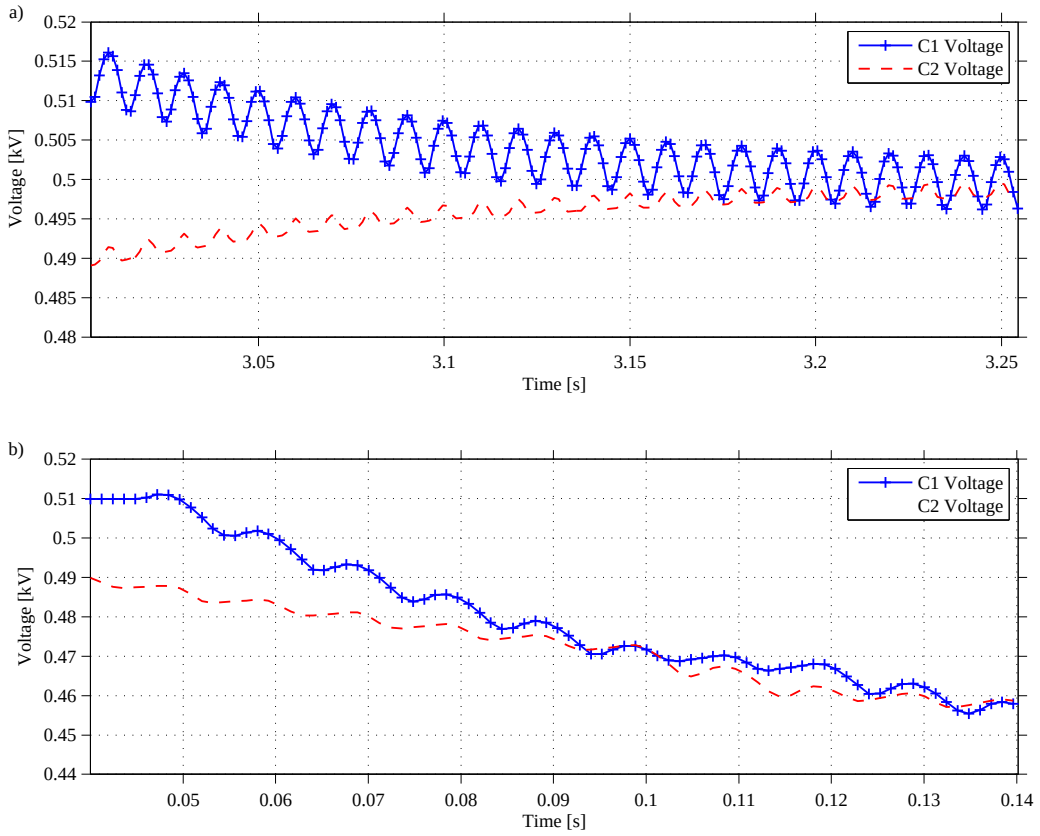

Figure 6.6: Capacitor Balancing Voltage Responses for a) reactive power transfer b) active/mixed power transfer for the CMCI

transfer (active/mixed) where source capacitors where initially differently charged and it can be seen that the duty priorities change. It can be seen that the priorities change since in the plot at about 0.64s and 0.66s the two capacitors have change workload with each other. The balancing prioritizing method effectiveness for both cases is clearly visible in Figure 6.6, where plot a) shows the balancing response for the capacitors for the reactive power transfer case and plot b) shows the voltage balancing response for active/mixed power transfer case. In plot a) it can be seen that for 0.25s the capacitor C1 is prioritized and is discharged more than capacitor C2, then the two capacitors are balanced to about the same voltage. Also in plot b) capacitor C1 is prioritized with heavier duty but only until about 0.1s. In between 0.1s and and 0.12s it can be seen in plot b) that it is now capacitor C2 that has the heaviest duty since it is now discharged more than capacitor C1. Between 0.12s and 0.14s the prioritization changes back again. For the reactive case some of the balancing is because of that the battery is charging the capacitors.

6.3.2 Voltage balance for the Neutral Point Clamped Inverter (NPC)

As stated earlier NPCMLI has problem with balancing the capacitor voltage when transferring active power but it does not have this problem while only transferring reactive power. To show this, simulations with an active and a reactive load for the five-level NPC Inverter has been performed. During these simulations the DC-link capacitors where first charged to 500V with charging voltage sources to balance the capacitors voltages, see chargers in Figure 6.3. When the circuit reached steady-state the chargers where disconnected. Both cases were simulated using the PDPWM modulation method at 1050Hz switching frequency, see Subsection 3.2.2, and the fundamental output frequency was 50Hz. The reason for using an odd multiple of the output voltage frequency for switching was the same as for the CMCI simulation. The carrier waves where modulated with aspect of the current voltage magnitude for each respective voltage level.

In Figure 6.7 it can be seen how the voltages over the DC-link capacitors change for the two cases, active and reactive power transfer, for the five-level NPCMLI. The voltages in the plot a) is for the reactive power transfer case. As can be seen the voltages are not fixed, they vary periodically around 500V. Depending on what the current direction is when the charging voltage sources are disconnected it will differ if a capacitor is charged or discharged first. In this case current is at lowest almost maximum negative magnitude when the charging voltage sources are disconnected. This leads to that C2 is initially charged, as can be seen in plot a). The range in which the voltages deviate depends on how large the capacitors are. Figure 6.7, plot b), shows the capacitor voltages for when the five-level NPCMLI transfers active power. As can be seen the voltages oscillates in this case as well but the voltages unbalance is increasing with time. The reason for this lies in the charging of one capacitor and discharging of the other capacitor in the $\pm\frac{V_{dc}}{4}$ voltage level, as discussed in section 2.1. In Figure 6.7 plot c) and d) the output voltages and current for the two cases can be seen. For the pure reactive case the capacitor voltages unbalance were also increasing over time since there were a small resistance in the load.

To correct these voltage unbalances in the DC-capacitors additional balancing control

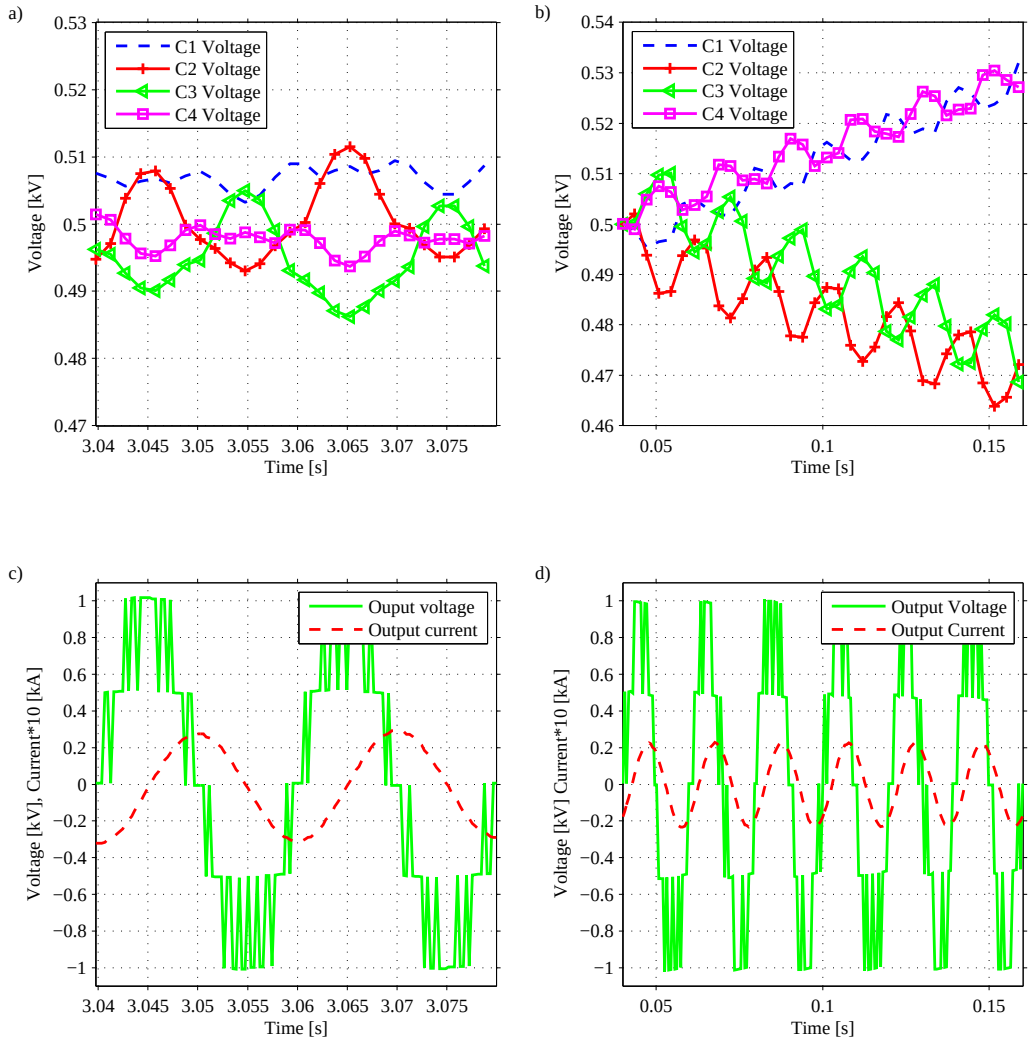

Figure 6.7: Unbalanced Simulation for the NPCMLI. a) Reactive power transfer capacitor voltages. b) Active/mixed power transfer capacitor voltages. c) Reactive power transfer load voltage and current. d) Active power transfer load voltage and current.

is needed, either in the form of additional balancing modulation or additional balancing circuits. A balancing circuit found in [16], discussed in the chapter 4, was used in this work to simulate the balancing for the five-level NPC Inverter. By transferring energy between the capacitor pairs in the NPC five-level inverter the voltages could be held from deviating from each other.

In Figure 6.8 the DC-bus capacitors voltages for pure reactive power transfer, plot a), and active power transfer, plot b), can be seen. In plot a) the capacitor voltages do vary around 500V but get more balanced over time, as can be seen in Figure 6.9 a), and hence vary with lower magnitude. The voltages varies since the capacitors are still charged and discharged by the reactive power transferred. Plot b) show the results from the active power simulation and compared to the unbalanced case the capacitor voltages does no longer get unbalanced over time but are held balanced by the balancing circuit, even though there are some oscillations. The oscillations comes from that the circuit transfers both active and reactive power, so there is some charging involved in the process. Also, another reason for the oscillations, or rather why the balancing circuit can not control these variations as well, is that the voltage controller is to slow for these oscillations. As stated, the voltage controller bandwidth is 20Hz and the oscillations have a frequency of 50Hz, making the controller unable to remove these oscillations. The balancing circuit is also implementable on NPC inverters switched with fundamental switching frequency with similar results. The voltage balancing response for the active power transfer simulation can be seen in Figure 6.9 b). The output voltages and currents for the reactive and active power simulations can be seen in Figure 6.8 c) and d).

6.4 Comparison between the two-level inverter and the selected MLI:s

To investigate the performance of multilevel inverters, compared to conventional two-level inverters performance, there are several parameters that can be analyzed for comparison, for example the output voltage and current THD:s, the switching frequency used for the inverters, the Fourier Transform Analysis of output voltages and the losses in the semiconductors. In this work comparison of the THD:s and the Fourier Transform Analysis of the two-level, Cascaded and Neutral-Point-Clamped inverters are compared in two cases. The first case compares results from the inverters when all of the are operated with 1kHz switching frequency and the second case compares results between the multilevel inverters and the two-level inverters when creating the same level of current THD with as low switching frequency as possible. Switching losses and conduction losses for the inverters will also be compared for both cases. In all comparison cases the output voltage magnitude and load is the same. The load is the mixed active/reactive load from earlier simulation cases (25.05Ohm, 0.1H) for all further comparison simulations. Finally a simulation there the MLI:s are compared when using SemiPWM, a mix of normal PWM mode and fundamental switching mode, is presented. All THD:s are calculated with harmonics up to the 255th in PSCAD. The fundamental output voltage frequency is 50Hz in all simulations.

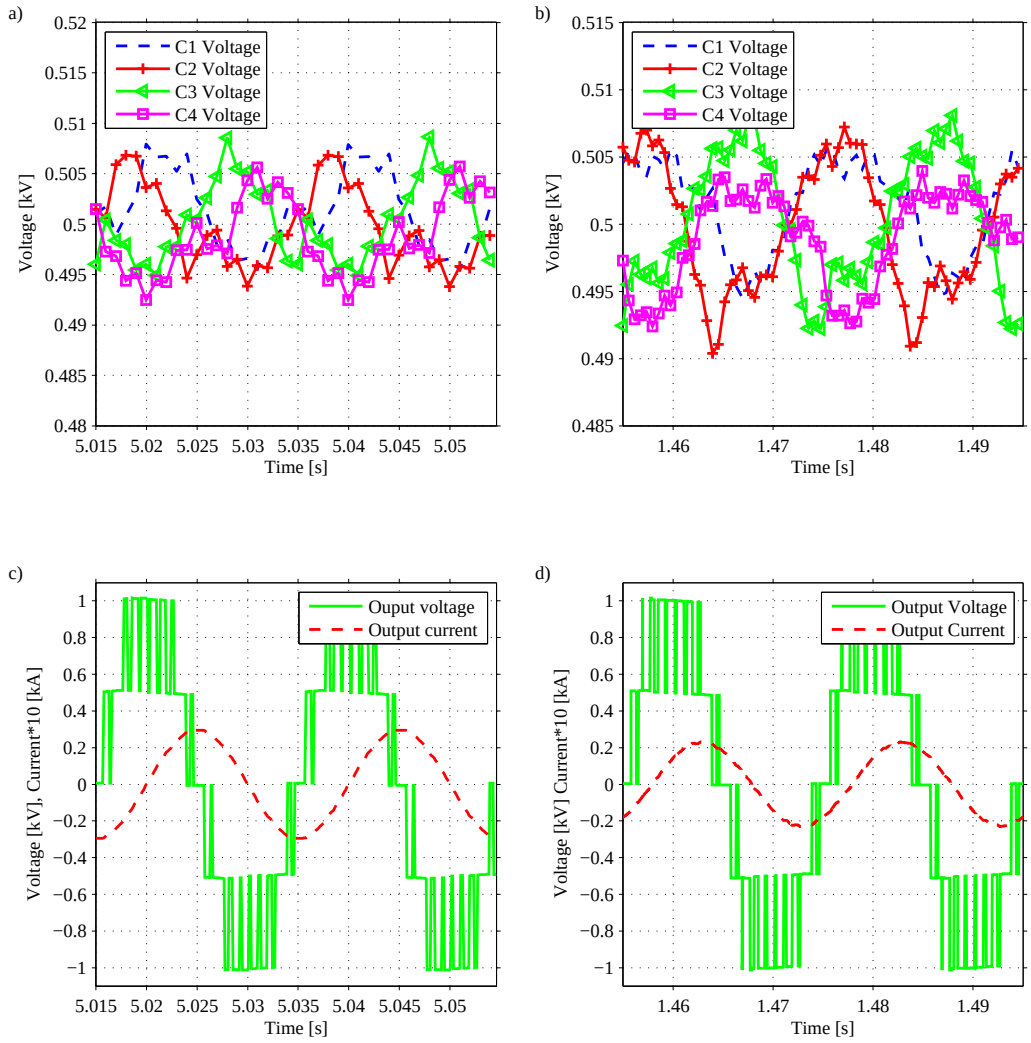

Figure 6.8: Balanced Simulation for the NPCMLI. a) Reactive power transfer capacitor voltages. b) Active/mixed power transfer capacitor voltages. c) Reactive power transfer load voltage and current. d) Active power transfer load voltage and current.

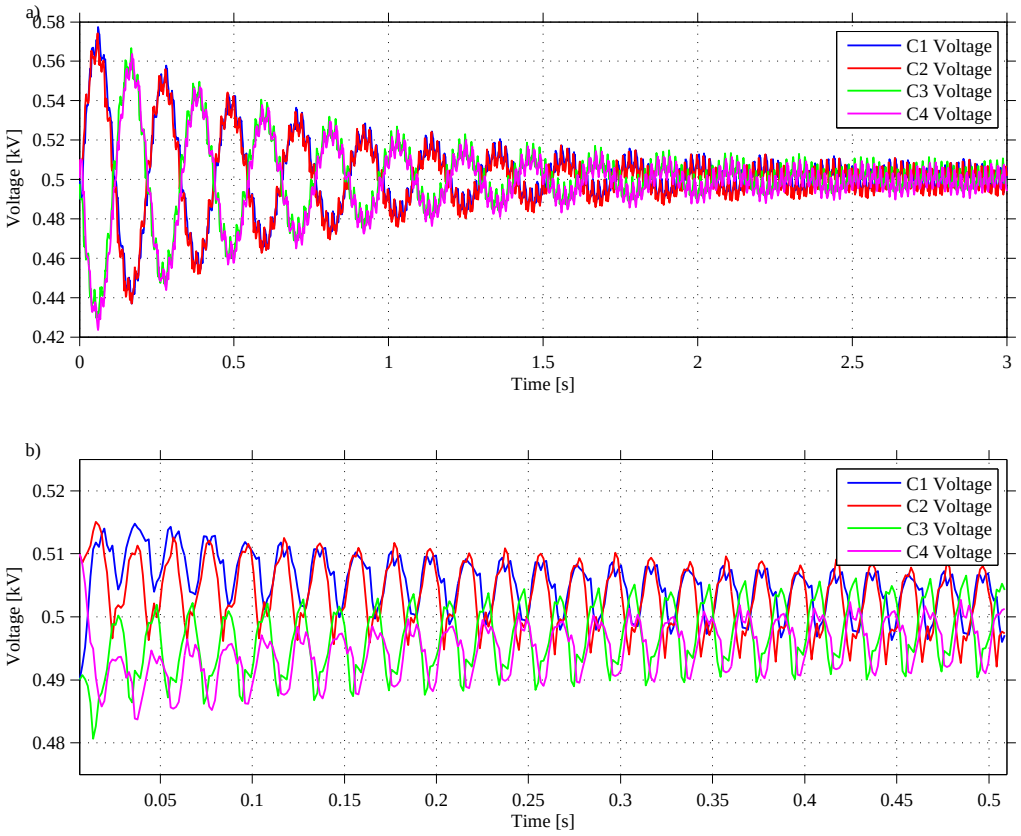

Figure 6.9: Capacitor Balancing Voltage Responses for a) reactive power transfer b) active/mixed power transfer for the NPCMLI

Table 6.2: Perfect case THD comparison, 1kHz

Topology	Two-level	Cascade five-level	Neutral-Point Clamped five-level
Voltage THD%	114.95	29.65	31.57
Current THD%	5.82	0.43	1.87

6.4.1 Equal switching frequency comparison (PWM)

In Table 6.2 and Table 6.3 the voltage and current THD:s can be seen for the two-level, Cascaded Multicell, and Neutral-Point-Clamped inverters when all operated with 1000 Hz switching frequency PWM. In both tables the same inverter modulations are used for the two-level inverter, ordinary two-level PWM and for the NPCMLI PDPWM is used for bot cases, but for the CMCI the modulations differs between the perfect balanced case and the implemented balanced method case. For the perfect case the modulation for the CMCI is PSCPWM and for the implemented balanced case it is PDPWM.

In Table 6.2 all inverters are using stable voltage sources instead of capacitors to represent perfect balancing. The CMCI presents the best result in this simulated comparison and the two-level inverter the worst. The two-level inverter produces the most THD in both voltage and current since in every switching the output voltage goes between 1kV and -1kV, a step of 2kV every switch transaction, a much larger step than for multilevel inverters. The voltage steps for the MLI:s is only 500V each, one fourth of that of the two-level inverter, and hence the two-level inverters harmonic components are larger in amplitude and therefore are also the THD:s higher. The reason for most of the THD:s for the NPCMLI is high disturbances from the $20th$ harmonic (caused by the switchings) and above. If these disturbances would be filtered out the THD:s would be significantly lower. It should also be noted that for the CMCI, when it is modulated with PSCPWM in this perfect balanced case, there are distortions created around the $80th$ harmonic (because of the high number of switching events for PSCPWM modulation with CMCI inverter). Since the harmonic components lies higher for the CMCI than for the NPCMLI more of the CMCI:s THD:s (both for voltage and current) are filter out by the load, and therefore there are some differences between the two MLI:s THD:s. The modulation methods for the multilevel inverters are here, in the perfect balanced case, PSCPWM for the CMCI and PDPWM for the NPCMLI.

In Table 6.3 the simulations are the same but this time with earlier presented balancing methods, additional balancing circuit for the NPCMLI and prioritized voltage source balancing for the CMCI, to balance the DC-bus and voltage source capacitors, but there a no longer any sources holding the individual voltages for the multilevel inverters (except that the CMCI:s capacitors have battery models in parallel, as shown in Figure 6.2). The two-level inverter is assumed to have perfect balancing for its voltage sources. The NPCMLI inverter modulation is PDPWM and modulation for the CMCI is also PDPWM (with prioritized voltage balancing). The results are similar to the perfectly balanced case but with higher current THD for the CMCI inverter (compared to perfect case). The THD:s for the NPCMLI have not changed since the same modulation as before is used, only balancing differs.. Again the high voltage THD:s for the NPCMLI is due to high

Table 6.3: Implemented balance case comparison, 1kHz

Topology	Two-level	Cascade five-level	Neutral-Point Clamped five-level
Voltage THD%	114.95	22.19	31.57
Current THD%	5.82	1.88	1.86

$20th$ harmonic and above, as can be seen in the Fourier Transform analysis in Figure 6.10. Since most of the harmonics are high (in frequency) for all inverters, a low pass filters could improve the THD:s for all three inverters. THD is lower for the multilevel inverters since the overall magnitude of the FFT components are lower, as can be seen in the figure. For the implemented balanced case for the CMCI it should be noted that the PDPWM modulation does not create the higher harmonics, as with PSCPWM, and hence Figure 6.10 does not show components as high as the $80th$. However, even though the load does not filter out more distortions for the CMCI output, as with PSCPWM modulation, the voltage THD for the CMCI is lower in Table 6.3 than that of the NPCMLI, even though both MLI:s are using PDPWM to generate the same output voltage. The lower voltage THD for the CMCI is because of, since active power is transferred, the sources voltage amplitude are at a lower level. The voltage sources does not get recharged to supposed value since batteries with high resistance are used. The CMCI is then trying to generate the same output as before but with voltage levels with lower amplitude. Since carrier waves are modulated by the actual source voltage amplitude this leads to shorter pulse-widths that create higher lower THD. If the voltage levels and pulse-widths would have been the same for the NPCMLI and CMCI the voltage THD:s would have been close to each other. Also, the higher CMCI current THD, in proportion to the voltage THD, is about the same as the NPCMLI current THD. Since pulse-widths are modulated for the CMCI the inverter still generates the same output current as the NPCMLI and hence the current THD should be the same. The CMCI current THD is also much higher for the implemented balance case than for the perfect case. Since PDPWM is used for the implemented balance case instead for PSCPWM, that created higher order harmonics, there is no longer as much distortions filtered out by the load.

6.4.2 Similar Current THD comparison

The result in Table 6.4 comes from simulations where as low switching frequency as possible is used for similar amount of output current THD for the three inverters. Lowest switching frequency possible for the multilevel inverters is fundamental frequency, in this case 50 Hz, see waveforms in Figure 6.11. For the two-level inverter to create similar current THD as the multilevel inverters, around 3-6%, a switching frequency of 900Hz is used. The modulation for the multilevel inverters is Selective Harmonic Elimination, discussed in section 3.4, where the third harmonic is eliminated by the switching pattern (two available switching angles, one angle to create fundamental waveform and one angle to eliminate harmonic component). Not only did the multilevel inverters have lower voltage THD, but also lower switching losses (as will soon be discussed more in detail).

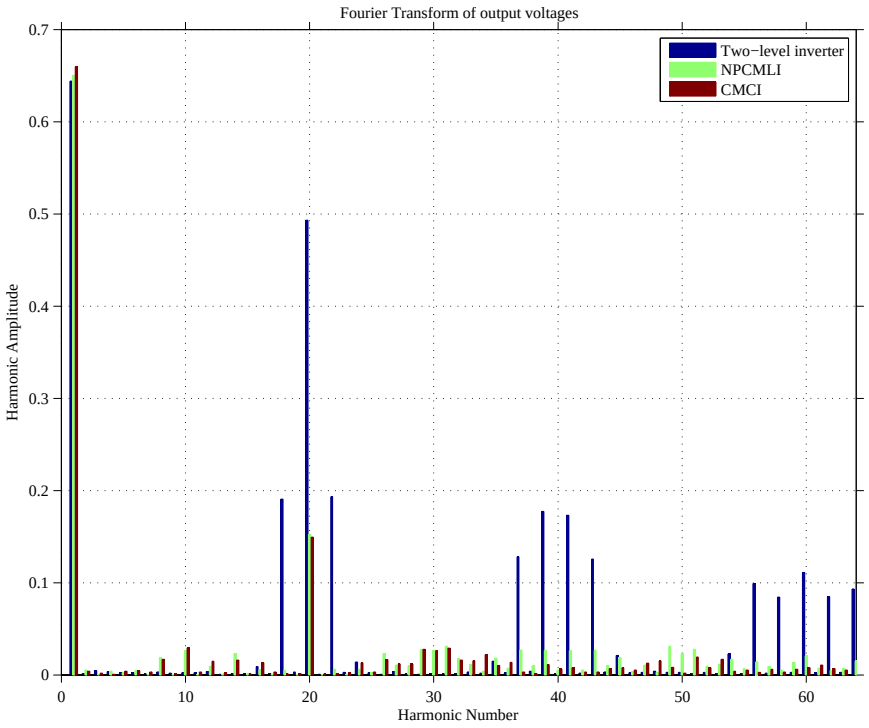

Figure 6.10: Fourier Transform of the output voltages for the 1kHz PWM case with discussed balancing methods for the MLI:s

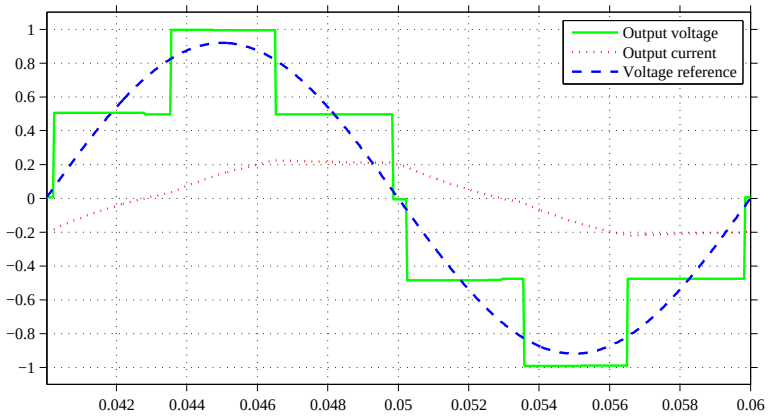

Figure 6.11: Fundamental switching frequency waveforms for five-level multilevel inverters. Reference in dashed blue.

Table 6.4: Implemented balance case, THD comparison, similar current THD

Topology	Two-level	Cascade five-level	Neutral-Point-Clamped five-level
Voltage THD%	113.33	22.50	29.69
Current THD%	6.47	3.83	6.35
Switching Frequency	900Hz	50Hz	50Hz (+500Hz)*

*The extra 500Hz is for the switchings in the balancing circuits

The drawback for the multilevel inverters against the two-level inverter is however the low order harmonics that are harder to filter out than the two-level inverters higher order harmonics, as can be seen in the Fourier Transform in Figure 6.12. Comparing voltage THD:s for the MLI:s in Table 6.4, it can be seen that once again the CMCI voltage THD is lower than that of the NPCMLI. As for the PWM case before, with implemented balance, this is due to that the CMCI voltage levels are lower by active power transfer that lower the sources voltages. The modulation tries modulate for the voltage changes, and hence lower voltage THD similar to the implemented balance PWM case. However, to properly generate the correct output the firing angles would have to be recalculated, which they are not for this case. The CMCI and NPCMLI uses the same firing angles. Therefore not the exact same output is generated, which leads to that the CMCI current THD is different from that of the NPCMLI in Table 6.4. If the CMCI would have had their voltage sources recharged to supposed value, the THD:s for the CMCI and NPCMLI would have been similar.

In this example five-level multilevel inverters are used in comparison with the two-level inverter. When using five levels the THD:s at fundamental switching frequency are quite low, but with a higher number of voltage levels in the multilevel inverters the THD:s could be even lower. If the same test is performed with a Cascaded Multicell seven-level inverter using fundamental switching frequency together with Selective Harmonic

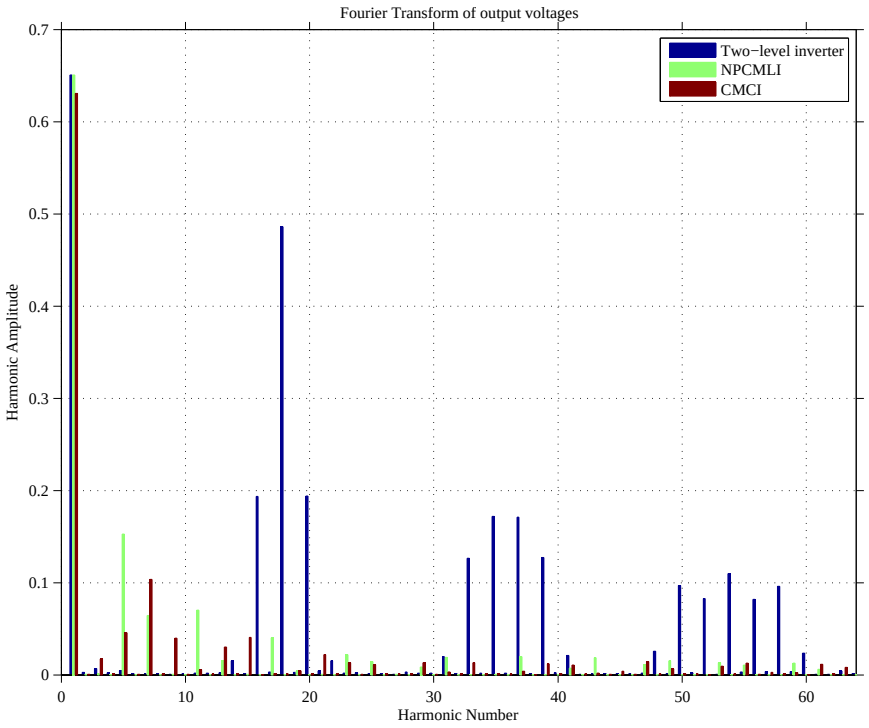

Figure 6.12: Fourier Transform of the output voltage for the similar current THD simulation case

Elimination modulation, where the third and eleventh harmonic are eliminated (switching angle calculations did not converge for third and fifth harmonic with chosen algorithm), the voltage THD is significantly lower than the one in Table 6.4, about 16.2%, and the current THD is also lower, about 2.5%. This indicates that the use of higher numbers of voltage level in a multilevel inverter can be advantageous for the generated THD.

6.4.3 Power loss comparison

In the section 3.5 the switching and conduction power losses for semiconductor switches were discussed. If the equation P_{sw} and P_{cond} for each and every switch in the three simulated inverters are calculated, their respective losses are found. Depending on current direction there will in some cases be a diode turn-off loss instead of switch turn-on and turn-off loss since the diode will conduct the current instead of the switch. For the NPCMLI there will also be diode turn-off losses for each voltage level because of the clamping diodes. Values used for losses calculations are data from the semiconductor "SKiiP 25AC126V1" data sheet, modulated with appropriate current for each event. Losses for both diodes and switches, both for switching and conduction, will be the same since, according to the data sheet, for the currents in this reports simulation the losses are very similar. In Table 6.5 the calculated switching and conduction losses for the three Similar Current THD case inverter simulations in Table 6.4 can be seen. The table shows that the multilevel inverters has lower switching losses for the same load in this simulation. The two-level inverter has eight switches instead of two so that every switch is rated for the same voltage as for the multilevel inverters. Due to this fact all switches have the same losses for equal voltage, current and switching frequency. Because of this the two-level inverter uses as many switches as the the five-level MLI inverters. As a result, as can be seen, the conduction losses for the two-level inverter is about the same for as the conduction losses for the multilevel inverters. Also, the conduction losses for the CMCI are slightly smaller than that of the NPCMLI. This is because of that in the instant the measurements where taken the voltage for the CMCI sources where lower due to active power transfer. This is true since, even though same references are used to generate the same output voltage, the firing angles for the CMCI is not as optimal for the CMCI as for the NPCMLI and hence creates slightly lower current. When it comes to switching losses the CMCI has the lowest, followed by the NPCMLI total switching losses. Because of the two-level inverters higher switching frequency the inverters switching losses are higher than for the multilevel inverters. For the NPCMLI there are also losses for the balancing circuit, they are however not included in any power loss calculations.

In Table 6.6 the same kind of calculations have been made for the 1kHz switching frequency case. As can be seen the multilevel inverter switching losses are still low compared to two-level inverter switching losses, and low even for 1kHz switching frequency compared to the 50Hz case. The reason for that the switching losses is not entirely proportional to the switching frequency is that for the 50Hz case the energy losses for every switching instance are high since the current is high for these instances, in this case. For the 1kHz case most of the switching instances occur when the current is low and hence

Table 6.5: Switching Power loss comparison for the three inverters for the similar voltage THD case

Topology	Two-level	Cascade five-level	Neutral-Point-Clamped five-level
Switching power loss	25.1W	2.1W	0.8W + 1.4W*
Switching Frequency	900Hz	50Hz	50Hz
Conduction power loss	99.1W	95.6W	99.1W
Number of switches	8	8	8
Total Losses	1.9%	1.49%	1.55%

*Clamping Diode turn-off losses

the energy losses are lo. Therefore the switching losses does not become proportional to the frequency. This is however not true in general, but it happens to be the case here. Do however also note the difference in switching power loss for the CMCI with balancing modulation (based on PDPWM) and PSCPWM modulation. Since both modules are always switching independent of the output voltage level for the PSCPWM modulation the switching losses are high. The conduction losses are the same as in the case before.

In Table 6.5 and 6.6 the total power efficiency for all three inverter and for both cases can also be seen. With both switching and conduction losses added together the two-level inverter is the least power efficient inverter for both cases. This is because of the equally high conduction losses, since equal numbers of switches are used, and the two-level inverters higher switching losses. However, the two-level inverter is not very far behind the multilevel inverters, with the CMCI as the most efficient of the two. In these total loss calculations the losses for filters are not included, since output signals has not been filtered from distortions, and as already stated the multilevel inverters produces much less distortions which would lead to lower filter losses. Also, if the two-level inverter had not used as many switches as the multilevel inverters in the comparison, its losses would have been smaller. However, if equal numbers of switches would not have been used their ratings would had differed.

6.4.4 Comparison between fundamental switching, PWM and SemiPWM switching

When using multilevel inverters there is the choice to modulate the inverters levels differently. All but the last level could for instance be modulated at fundamental switching frequency and the last with high frequency PWM (SemiPWM). This would lower the switching frequency for the inverter but create a smoother waveform than if an inverter where only modulated at fundamental switching frequency. However, THD:s and har-

Table 6.6: Switching Power loss comparison for the three inverters for the 1kHz switching frequency case

Topology	Two-level	Cascade five-level	Neutral-Point-Clamped five-level
Switching power loss	27.1W	4.1W* 24.9W**	3.8W + 4.0W***
Switching Frequency	1000Hz	1000Hz	1000Hz
Conduction power loss	99.1W	95.6W	99.1W
Number of switches	8	8	8
Total Losses	1.94%	1.53%	1.63%

*CMCI with balancing modulation based on PDPWM
**CMCI with PSCPWM modulation
***Clamping Diode turn-off losses

monics will also be affected. For the five-level multilevel inverters in this work this SemiPWM modulation would modulate one level at fundamental frequency and modulate one level with high frequency PWM every half cycle, see output voltage waveform in Figure 6.13 plot a). In Table 6.7 the THD results from the SemiPWM simulations can be seen. Compared with ordinary fundamental switching in Table 6.4 it can be seen that the THD:s for the Neutral-Point Clamped and the Cascaded Multicell inverters are lower with this modulation. In Figure 6.14 the Fourier Transform analysis for the SemiPWM simulations can be seen. Low order harmonics are more common than for the other cases but are instead lower in amplitude. Also the higher order harmonic components tend to be higher in amplitude for the SemiPWM in the Fourier Transform Analysis. That the distortions are lower for low frequencies and higher for higher frequencies can be an explanation for the lower SemiPWM THD:s, since more of the distortions are filtered out by the load than for the other two modulation methods.

The SemiPWM modulation is composed of a switching angle, chosen with the help from trial and error testing, for the fundamentally switched level and a 1kHz triangular carrier waves, compared to a voltage reference wave, for the PWM modulated level. Together the two modulation methods spanned from maximum positive output voltage to maximum negative output voltage, with the PWM carrier waves at top and bottom. See Figure 6.13 plot b).

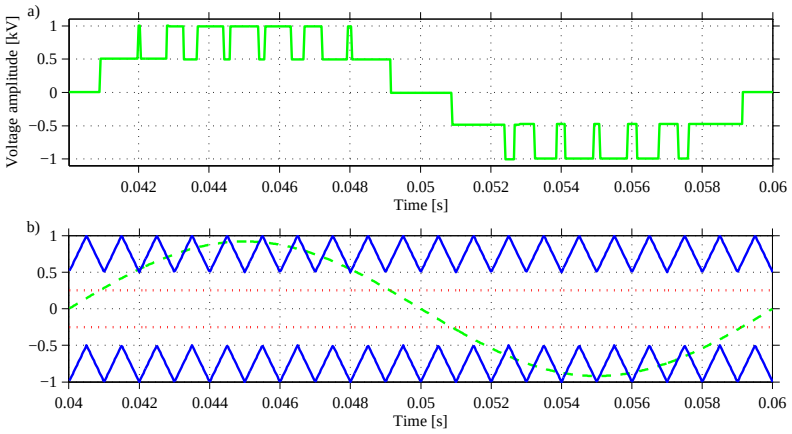

Figure 6.13: SemiPWM Voltage Waveform. a) Output voltage waveform. b) Reference (dashed green), PWM carrier waves (solid blue) and switching angle reference (dotted red)

Table 6.7: SemiPWM switching THD:s

Topology	Cascade five-level	Neutral-Point Clamped
Voltage THD%	20.11	28.71
Current THD%	1.99	2.07

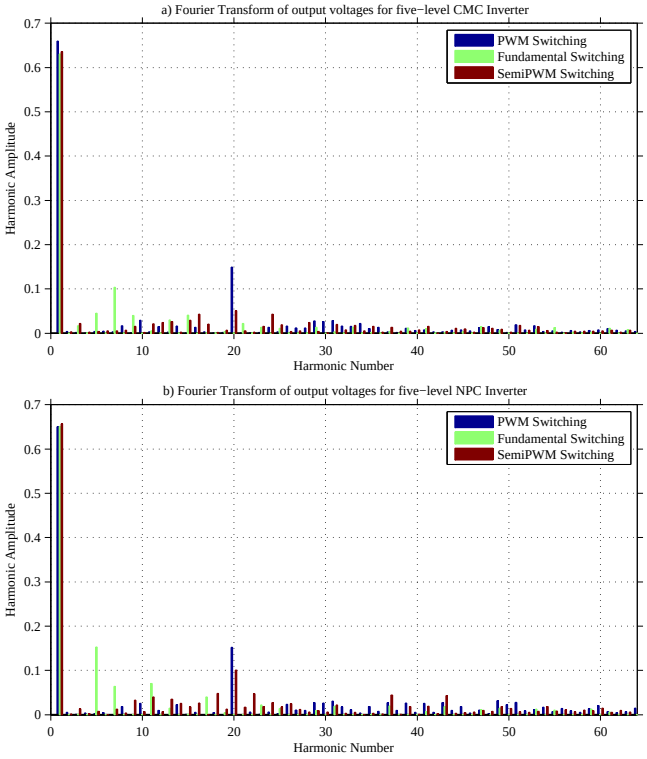

Figure 6.14: Fourier Transform for the Cascaded Multicell Inverter in a) and the Neutral-Point Clamped Inverter in b) when comparing with SemiPWM

7 Conclusion

7.1 Result

This work has presented several topologies for multilevel inverters (MLI), some of them well known with applications on the market. Every topology have been described in detail. Several modulation techniques have also been presented which are to be used with the presented topologies.

Topology comparisons, such as number if components and their ratings, have been presented and shows that multilevel inverters compete with two-level inverters in the area of voltage ratings for their components (diodes, switches and such), even though the number of components needed for multilevel inverters, as shown, can be very high. For a five-level MLI case the voltage rating requirements is only one fourth of that of the two level inverter, but four times more switches are needed (for components with different ratings).

The simulation chapters in this report have presented results concerning both the discussed voltage balancing problem and comparison with a two-level inverter for the Cascade Multicell inverter (CMCI) and the Neutral-Point Clamped (NPC) inverter. For the balancing problem it is shown with simulation results that the voltage levels, with different strategies, can be balanced for both the CMCI and the NPC inverter. For the NPC inverter an additional balancing circuit was used that with both active and reactive power load could balance the voltages in the DC-bus capacitors, with a variation off about $\pm 1\%$ in both cases. For the CMCI a modulation strategy that prioritized modules depending on stored charge, showed that the voltage levels in this inverter could be discharged equally. Especially for the active power load where a voltage difference of 20V, while transferring 6.6 kW, where balanced in 0.1 seconds. Since balancing solutions where presented for both simulated topologies in this work, the possibility has been shown to use multilevel inverter with potential methods of treating the problem of voltage unbalance.

The multilevel topologies have also been tested in several simulations and compared with the two-level inverter. It is shown that the two-level inverter has competition in generation of THD, switching power loss and conduction power losses, as long as equal numbers of the same components are used in the comparisons. In all simulations the two-level inverter have created higher voltage THD, and in most cases also higher current THD, than both the Cascade Multilevel inverter and the Neutral-Point Clamped inverter. For the 1kHz simulation case the two-level inverter produced about 115% voltage THD while the CMCI and NPCMLI only produced about 22% and 32% voltage THD. It is also shown that the multilevel inverter can produce less voltage THD and switching power loss compared to the two-level when the multilevel inverters are modulated at fundamental

switching frequency. Additionally, it is shown that high numbers of voltage levels in the MLI:s are not needed for the lower THD:s to be noticeable. Together with low switching frequencies multilevel inverters can be used in applications to lower both THD:s and switching losses. The difference in switching losses between the MLI:s and the two-level inverter where, at its highest difference, about twelve times higher, 25.1W against 2.1W and 2.2W for the CMCI and NPCMLI. However, the conduction losses for the multilevel inverters are about the same as for the two-level inverter, but the total efficiency is still lower for multilevel inverters for all calculated cases. The test with largest differences in efficiency where the Similar Current THD test where the two-level inverter had a total losses of 1.94% while the CMCI and NPCMLI had efficiencies off 1.53% and 1.63%.

To summarize the results from this report it has been shown with simulations that multilevel inverters can be used instead of two-level inverters to get lower THD in both output voltage and current and also to lower the switching power losses. However, a higher number of components must be used but these can be of a kind with lower voltage ratings, depending on the number of voltage levels used in the multilevel inverter. It has also been shown that the CMCI, in general, is the best choice of MLI when it comes to component requirements, since it was the voltage source MLI with the lowest number of needed components for both component comparisons in this report. The CMCI is also among the MLI:s that require the lowest voltage ratings.

7.2 Discussion

The results that this report has presented are in line with other results from other reports and articles. The lower amount of disturbances is one of the more frequently mentioned advantages for multilevel inverters, which has also been proven in this report. It seems that the biggest reason for using multilevel inverters is to lower the THD so that less filters needs to be used. The possibility to lower the switching frequency for higher efficiency is advantageous, even though the amount of disturbances that are generated gets harder to filter out. Also, another disadvantage is the more complex control, especially for voltage balancing. The high conduction losses are also a disadvantage, lowering the total efficiency. However, by trading off and choosing switches with higher switching losses but lower conduction losses, the efficiency can be optimized.

The advantages with multilevel inverters over two-level inverters are clear. If low disturbances or low switching power loss is wanted, multilevel inverters are certainly a solution.

7.3 Future Work

- Actual laborations on the topologies for simulation verification.
- Simulations on the Neutral-Point Clamped inverter with a voltage balancing modulation, such as those that where mentioned, instead additional balancing circuit.
- Multilevel and two-level inverter filter loss comparison

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