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A Harmonic-Oscillator Design Methodology Based on Describing Functions

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A Harmonic-Oscillator Design Methodology Based on Describing Functions

by

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Front cover: Pendulum clock. Photograph by Erik Boman.

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Abstract

Oscillators are present in most electronic equipment where they provide timing information, for example as sampling clocks in analog-to-digital converters or as radio carriers in wireless communications. To design an oscillator, we must have knowledge of the properties and the operation of oscillators. Since oscillators are inherently nonlinear and are subject to noise, we have a system that is difficult to analyze since the large wanted signal and the small unwanted signal interact. It is shown in this thesis that describing functions can be used to calculate not only the large-signal behavior, but also the small-signal behavior using the method of impulse sensitivity functions. Based on theoretical results from this method, a design methodology for harmonic oscillators is derived and analyzed. The design methodology aims at the design of harmonic oscillators fulfilling phase-noise requirements with minimized power consumption subject to constraints from the other requirements set by the specification and the technology used to implement the oscillator. The design methodology has been used to design oscillators meeting quite different specifications, both discrete and integrated implementations and with either inductors and capacitors or crystals as frequency-determining elements.

Keywords: oscillator, design methodology, describing function, impulse sensitivity function, frequency tuning, amplitude control, phase noise, oscillator design efficiency

Contents

Acknowledgements

After finishing my undergraduate studies in electrical engineering, I wanted to learn more about analog electronics. The path I chose was to stay a few more years in academia. My PhD studies provided the time needed to delve deeper into the vast subject of analog electronics; I spent a lot of time studying old text books on various subjects related to electronics – a chance I would probably not have had if I had been working in the industry. I would like to thank my supervisor Lena Peterson for providing this opportunity and giving me the freedom to pursue the subjects I found interesting.

A special thank goes to Roger Malmberg, my fellow PhD student at the circuit design group, for many fruitful discussions, of which at least some were related to electronics. I would also like to thank all my former and present colleagues at the department of Signals and Systems for their pleasant company and for providing the needed distractions from work, such as coffee breaks and other social events.

However, analog electronics is so much more than theoretical knowledge. The missing piece of the puzzle – practical knowledge – I came in contact with during my sabbatical year at Ericsson Technology Licensing AB, and I therefore want to thank all my colleagues during that rewarding year.

Finally, I would like to thank my family and friends for all their support.

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Abbreviations and Acronyms

AAC	Automatic Amplitude Control
AC	Alternating Current
AM	Amplitude Modulation
BJT	Bipolar Junction Transistor
CCO	Current Controlled Oscillator
CB	Common Base
CC	Common Collector
CD	Common Drain
CE	Common Emitter
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor (FET)
CS	Common Source
DC	Direct Current
DF	Describing Function
FET	Field-Effect Transistor
IDF	Incremental Describing Function
ISF	Impulse Sensitivity Function
JFET	Junction Field-Effect Transistor
MEMS	Micro-Electro-Mechanical Systems
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor (FET)
ODE	Oscillator Design Efficiency

PLL	Phase-Locked Loop
PM	Phase Modulation
PMOS	P-channel Metal Oxide Semiconductor (FET)
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
SOI	Silicon On Insulator
VCO	Voltage Controlled Oscillator

Notation

The symbols for currents and voltages at the terminals of active devices have subscripts which indicate the pertinent terminal for currents or terminal pair for voltages. In addition, uppercase and lowercase symbols and subscripts are used to distinguish between quiescent values, total values, and incremental values.

I_D, V_{GS}, V_{DS}	=	DC value
i_D, v_{GS}, v_{DS}	=	total instantaneous value
i_d, v_{gs}, v_{ds}	=	AC value
$I_{d,2}$, $V_{gs,1}$, $V_{ds,0}$	=	amplitude of sinusoidal component, the number indicates harmonic number
I_{SS}, V_{GG}, V_{DD}	=	supply voltage or current

Uppercase letters with tilde denote (possibly complex) describing functions.

$\widetilde{F}$	=	describing function

The operators given below are used in conjunction with the symbols given above.

x^*	=	complex conjugate
$\Re[x]$	=	real part
$\Im[x]$	=	imaginary part
$\overline{x}$	=	time average
$\mathrm{E}[x]$	=	expectation
$\mathcal{F}[x]$	=	Fourier transformation

α Phase shift of feedback part

β	Current amplification of bipolar transistor
γ	Noise factor of field-effect transistor
Γ_n	Complex amplitude of the n:th harmonic of the ISF.
δ	Noise factor of field-effect transistor
ζ	Phase shift of active part
η	Power efficiency
θ	Phase
μ_0	Magnetic constant ($4\pi \times 10^{-7}$ [N/A^2])
Υ	Oscillator design efficiency
ω	Angular frequency
f	Function of active part
f	Frequency
F	Noise factor
g_m	Transconductance of transistor
G_m	Transconductance of differential pair
h	Function of feedback part
I_n	Modified Bessel function of the first kind
j	Imaginary unit ($j^2 = -1$)
k_B	Boltzmann constant (1.3807×10^{-23} [J/K])
$\mathcal{L}$	Single-sided phase noise
T	Absolute temperature [K]
V_T	Thermal voltage [V]
q	Charge of electron (1.60219×10^{-19} [As])
Q	Q-value, quality factor
X_n	Complex amplitude of the n:th harmonic of signal x.

Chapter 1

Introduction

This thesis is definitely not the first one dealing with the design of electronic oscillators; many have been written during the years that electronics has been a research subject. So how is this thesis different from others written on this subject? It is my aspiration that this introductory chapter should provide you with the answer to this question and other related ones that you may have. The design methods used today for oscillators are discussed and conclusions drawn from this discussion are the motivation for the research on design methodology described in this dissertation. I have chosen to concentrate on harmonic oscillators, which I take to mean an oscillator having a nearly sinusoidal waveform somewhere within the oscillator. This type of oscillator has the potential to have very low phase noise and is often used in radio communication circuits as a means to generate a clean receive or transmit carrier.

1.1 Background

The background given in this section covers the analysis and design of oscillators. General background about oscillators is given in Chapter 2. Since this thesis targets only electronic oscillators, we use the word 'oscillators' to mean electronic oscillators throughout the thesis.

Today, oscillators are used in most electronic circuitry, both digital and analog, for example as carrier generators for radio systems and as clock generators for digital circuitry. The number of oscillators per system has grown over time since more and more systems are implemented as systems on chip where the component count is much less important than for discrete implementations.

At the same time as the number of oscillators per system and the requirements on oscillators are increasing, we also want to decrease the design time to get the product out on the market as quickly as possible [Kundert, 2000]. Companies that manage to reduce their design time have an advantage against its competitors. In addition to the reduced cost for the design phase, the company also gets the product out on the market before its competitors.

The reader who is not familiar with oscillators may want to read Chapter 2, which contains an introduction to oscillators, before proceeding with the remainder of the introduction.

1.1.1 Why do we need a Systematic Design Methodology?

The main benefit of designing in a systematic way is that the design time is fairly short and the chance of success is higher than for most other design methodologies. Another benefit of systematic design is the possibility to determine if the specification is possible to reach early in the design process. Other ways of designing, such as tweaking an existing circuit, may be quicker in many cases, but do not guarantee that the result fulfills the specification. Repeating this procedure for many different existing circuits will probably yield a circuit fulfilling the specification sooner or later, but the solution may be far from optimal and the design time may be prolonged.

The choices made during the design of oscillators are generally not done in a systematic way today; consequently one usually ends up with a suboptimal solution – if a solution is found at all. To design in a systematic way, one must be able to analytically calculate the specifications in terms of topology and circuit parameters. Such analytical expressions make it possible to see which requirements are orthogonal and consequently can be considered separately. Today, different methods are used to calculate for example signal waveform, frequency tuning range and phase noise. A consequence of using different methods is that one easily misses the interconnections between the specifications. It also takes more time when each aspect has to be calculated separately and calculation methods for some aspects are still missing.

In addition to being systematic a design process should, if possible, be *orthogonal*. If it is orthogonal, each property of the oscillator can be optimized independent of the others, which simplifies the design procedure and guarantees that a near-optimal solution is found. The orthogonality is necessary to achieve a top-down design process without iterations. Using an orthogonal design process for a problem which is not completely orthogonal, one may reject solutions that are optimal; however, near optimal ones are found in a

systematic way.

Plenty of research effort has been spent on the development of a design methodology for negative-feedback amplifiers [Verhoeven et al., 2003]. However, not nearly as much effort has been spent on the development of systematic design methodologies for oscillators [Westra et al., 1999, van Staveren et al., 2001, van der Tang et al., 2003].

1.1.2 Analysis of Oscillators

To design an oscillator in a systematic way, one needs to understand the operation of oscillators. Consequently, to develop a design methodology, much effort must be spent on the analysis of oscillators. Therefore, most research is focused on the function of oscillators.

Much early oscillator research sought to explain the general behavior of oscillators [van der Pol, 1934]. The research was targeting the large-signal behavior, such as the output signal waveform and frequency. Since oscillators are nonlinear circuits by nature, linear theory did not suffice and approximate solutions to the resulting nonlinear equation systems were sought.

Once the large-signal behavior was explained, research focus shifted toward small-signal behavior, such as phase noise [Leeson, 1966]. Even though the noise is small enough for linear theory to be valid, the equation systems are time-varying with the large oscillation signal. Since the large-signal and the small-signal behavior interact, the resulting time-varying system will not be exactly periodical which makes the analysis complicated.

1.1.3 Design of Oscillators

Several books on the design of oscillators are available, but few of the books written so far has included all the design specifications that are important today. Some older books, such as the one by Parzen [Parzen, 1983], provides cookbook recipes for designing different types of oscillators, but neglect the phase noise. Older books usually focus on bipolar transistors or vacuum tubes and have no information whether the information provided is applicable to oscillators based on field-effect transistors.

Many books targeting oscillator design methodology assume that the components of the oscillator are linear in operation [Westra et al., 1999, van Staveren et al., 2001]. Hence, the design methodologies are not suitable when oscillators with high power efficiency or oscillators having frequency tuning are designed.

Today, there are books available that deal with most of the important requirements on oscillators [Hegazi et al., 2005, van der Tang et al., 2003].

However, they assume the circuit topology to be given and do not deal with all requirements in a systematic way.

1.2 Contributions

The main contribution of this thesis is the design methodology described in Chapter 3. This design methodology, which is based on analytical expressions, speeds up the design of high-performance harmonic oscillators compared to most methods used today. In addition to this main contribution, other matters of interest were found during the development of the design methodology and these contributions are pointed out below.

In Chapter 8, I show how it is possible to obtain approximate expressions for the Impulse Sensitivity Functions (ISFs) using the method of Describing Functions (DFs). This new method has less limitations than previous methods for deriving analytical expressions for the ISFs of oscillators. The ISFs derived in this thesis may be used to gain understanding in existing oscillators and help during improvement of these oscillators.

The derived expressions for the ISFs are used in Chapter 5 through 7 to obtain closed-form approximate phase-noise expressions for general oscillators, including the effect of amplitude control and frequency tuning. The expressions derived in this thesis show how different circuit topologies affect the phase noise of the oscillators. Especially the impact of different frequency tuning schemes and the impact of amplitude control on the AM-to-PM conversion are investigated.

I show how to use ISFs to calculate the frequency shift due to harmonic frequency content in the oscillator in Section 9.1. This frequency shift is usually not of importance in LC oscillators, but may be important when designing for example stable timing references where an error in frequency of only two parts per million corresponds to an error of one minute per year.

I also show how large the series base resistance of a bipolar transistor in an oscillator implementation may be before its noise contribution to the total phase noise becomes significant in Section 3.2.3.

Furthermore, it is shown in Section 9.3 that it is possible to estimate the phase-noise performance of existing oscillators within a few dB, only by knowing the topology, power consumption, supply voltage, Q-value and oscillation frequency, assuming the oscillator was designed for minimum phase noise.

1.3 Thesis Outline

This thesis has a top-down outline: First I describe the design methodology; then we dig into the gory details of deriving the equations on which the methodology is based.

Before proceeding with the methodology, I briefly discuss the operation of oscillators in Chapter 2. I also discuss implementation aspects and how to specify an oscillator. Without a specification, we cannot know what we should design or if we have accomplished what we sought. The reader already familiar with oscillators and the design of oscillators may skip this chapter.

In Chapter 3 I introduce the design methodology, which in combination with the information on oscillator topologies provided in Chapter 4 constitute the complete design methodology.

The four following chapters contain derivations of different aspects of the operation of oscillators. In Chapter 5 I discuss amplitude control and in Chapter 6 I discuss frequency tuning. In Chapter 7, the phase noise of oscillators is derived using Impulse Sensitivity Functions (ISFs). These ISFs are derived in Chapter 8 using Describing Functions (DFs).

The derived expressions used in the development of the design methodology are verified in Chapter 9. Mostly simulations are used for the verification, but also measurements from many papers are used. Finally, in Chapter 10 I discuss conclusions drawn from the research presented in this thesis and possible future extensions to it.

Chapter 2

Oscillator Basics

In this chapter I provide the basic explanation of how oscillators work. In addition to the simple electrical LC oscillator used in examples, I use the pendulum clock as a mechanical analogy for the reader who is a novice in the area of electronics. After discussing how oscillators should work, I discuss limitations arising when they are physically implemented and how to specify the requirements on these limitations. Finally, I briefly discuss how to achieve an oscillator realization that fulfills these requirements.

2.1 Introduction

Oscillators are systems producing timing information without *any* external information. An example of a simple mechanical oscillator is the pendulum clock of Figure 2.1. The pendulum swings back and forth with a well-predicted period, for example one second. By counting the number of periods we know the time that has elapsed since we started counting.

The energy in the pendulum changes from kinetic energy when the pendulum is at its lowest point to potential energy when the pendulum reaches the highest points on its trajectory. If there were no losses, the pendulum would swing forever. However, there are losses which will make the pendulum stop swinging after some time. These losses may for example be the air resistance and the friction in the connection point. To make the pendulum swing for a long time, we must replenish the energy lost in each period. The weight to the right in the figure has potential energy which is used to restore the energy of the pendulum lost in each cycle. The energy is transferred via the cog-wheels and the escapement gear to the pendulum in small discrete energy pulses, one pulse each period, via the anchor. At the same time as

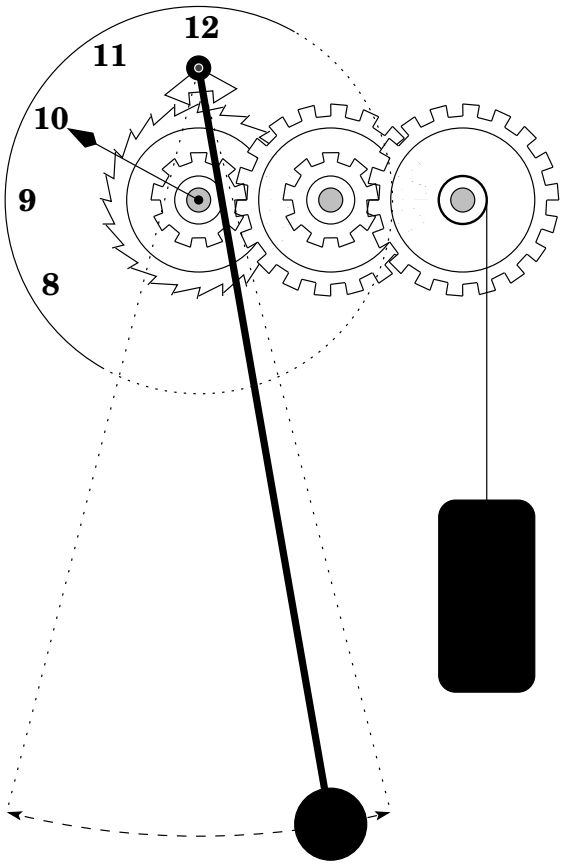


Figure 2.1: Pendulum clock.

the energy is transferred, the escapement gear below the connection point rotates a cog and the hand of the clock moves.

Other types of mechanical clocks use springs to store the energy instead of a weight and some clocks use a balance-wheel instead of the pendulum to determine the oscillation period, but the principle is the same.

A simple electrical oscillator is shown in Figure 2.2. In the electrical oscillator the energy is transferred between the capacitor and the inductor with a certain oscillation period. The output of the oscillator could for example be the voltage over the capacitor, v.

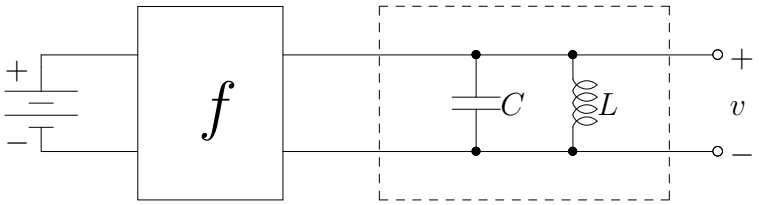


Figure 2.2: LC oscillator.

As in the pendulum clock, we have losses. The losses might for example be resistive losses in the capacitor and the inductor, which will make the oscillator stop after a while. As in the clock, we must replenish the lost energy. The active block, f, to the left in the figure transfers energy from the battery to the parallel LC circuit, replacing the lost energy each period. The battery stores energy and performs the same role as the weight in the clock.

2.1.1 Feedback Model of an Oscillator

To predict the operation of an oscillator, we need a mathematical model of it. We have chosen to model the oscillator as a feedback system with an active part, f, and a passive feedback part, h, according to Figure 2.3. The division into two parts does not imply that a particular physical component is placed entirely in either one of these parts; a transistor may for example be present both in the active part as a transconductance and in the passive feedback part as a gate–source capacitance. The division is performed such that the input to the active part, $x(t)$, is quasi-sinusoidal.

The active part, f, supplies the energy necessary to keep the oscillations going and also determines the amplitude of the oscillation. The passive feedback part, h, determines the oscillation frequency. This feedback model of the oscillator is used throughout this thesis.

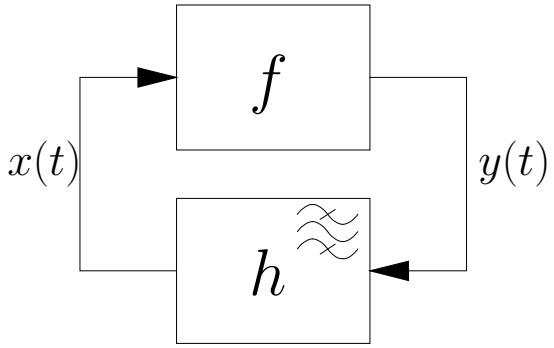


Figure 2.3: Feedback model of an oscillator. There is an active part f and a feedback part h.

The pendulum clock could be modeled such that x equals the pendulum angle, the pendulum makes up the feedback part, h, and y equals the force supplied from the active part, f, via the cog-wheels. The electrical oscillator could be modeled such that x equals the voltage v across the passive LC circuit, h, and y equals the current supplied from the active part, f.

2.2 Large-Signal Properties

The large-signal properties of the oscillator relate to the output signal of the oscillator when no disturbances, such as noise, are present. Since the output signal is the reason for constructing an oscillator in the first place, these properties are among the most important. For example, the output signal of a sinusoidal oscillator is shown in Figure 2.4.

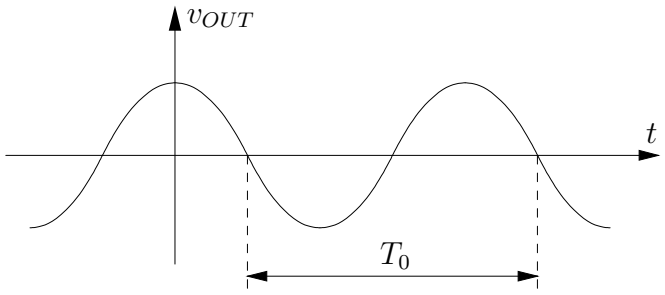


Figure 2.4: Output signal of sinusoidal oscillator.

2.2.1 Signal Waveform

The waveform of the output signal is one of the most basic characteristics of an oscillator. The requirements on the waveform differ depending on what the oscillator will be used for, and the output waveform could for example be a sinusoid, a squarewave, or a sawtooth waveform. Any divergence from the desired waveform is called distortion and the maximum allowed distortion is often one of the design parameters.

2.2.2 Frequency

In addition to the exact waveform, we want the oscillator to have a stable output frequency regardless of manufacturing spread, temperature variations, and aging of components. The frequency is defined as the inverse of the period time T_0, see Figure 2.4.

How stable the frequency must be and what absolute accuracy is needed depend on the application wherein the oscillator will be used. Oscillators with high frequency stability often use a piezoelectric crystal as their frequency-determining component.

Frequency Tuning

In many oscillators, the frequency should be adjustable in operation over a specified frequency range, especially in radio circuits where the radio is used to transmit or receive signals at different frequencies. There are also requirements on the speed with which the oscillation frequency can be adjusted.

For a Voltage Controlled Oscillator (VCO), an applied control voltage V_{ctrl} will change the oscillation frequency by an amount $\omega_\Delta = K_{VCO}V_{ctrl}$, where K_{VCO} is the frequency tuning constant. The output voltage of an oscillator with frequency tuning producing a sinusoidal signal can be modeled as

$$v_{OUT}(t) = V_{out,1}\cos\left(\omega_c t + K_{VCO}\int_{-\infty}^{t} V_{ctrl}dt\right), \tag{2.1}$$

where $V_{out,1}$ is the output-voltage amplitude and ω_c is the center frequency.

In reality, the frequency tuning is not a linear function of the tuning voltage. Depending on the use of the oscillator, we might have requirements on the linearity, for example when the oscillator is used in a Phase-Locked Loop (PLL).

2.3 Small-Signal Properties

An ideal oscillator should have output power only at the oscillation frequency and its harmonics. Due to noise, however, the power spectrum is widened and a noise floor is introduced as indicated by the dashed line in the power spectrum of Figure 2.5.

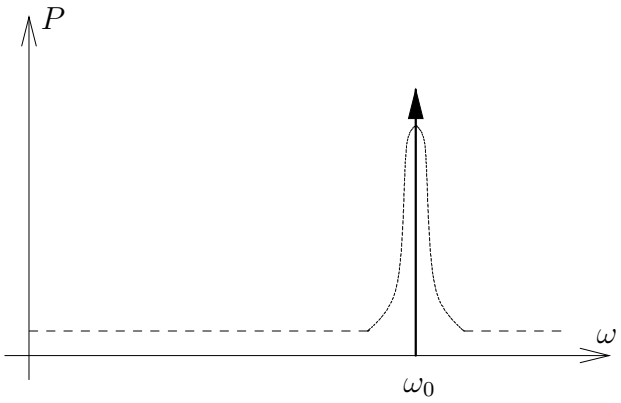


Figure 2.5: Spectrum of sinusoidal oscillator with noise.

The source of any widening of the spectrum may be deterministic or stochastic in nature. Deterministic sources include noise on the supply voltage from other circuitry; stochastic sources include thermal noise in resistors. Sometimes it is more convenient to model the deterministic sources as stochastic sources as well, depending on their properties.

The requirements on the output noise are given in the time domain or frequency domain, depending on which one is most suitable for the case in question. Sampling systems usually have requirements only on the crossing events, given as timing jitter. Radio-carrier oscillators on the other hand usually have requirements on the spectrum given as phase noise, but there may also be requirements on the amplitude noise. Timing jitter and phase noise basically describe the same phenomena.

An oscillator has a stable limit cycle as shown in Figure 2.6. A noise impulse will move the trajectory from the limit cycle. Due to the amplitude-controlling function of the oscillator, the trajectory will approach the stable limit cycle with time. However, once it is back on the limit cycle, it may have moved to a different point compared to if no noise impulse would have been injected, with a difference in phase θ. Noise can be modeled as a series of impulses with different levels. Consequently, the phase error θ is a function of time.

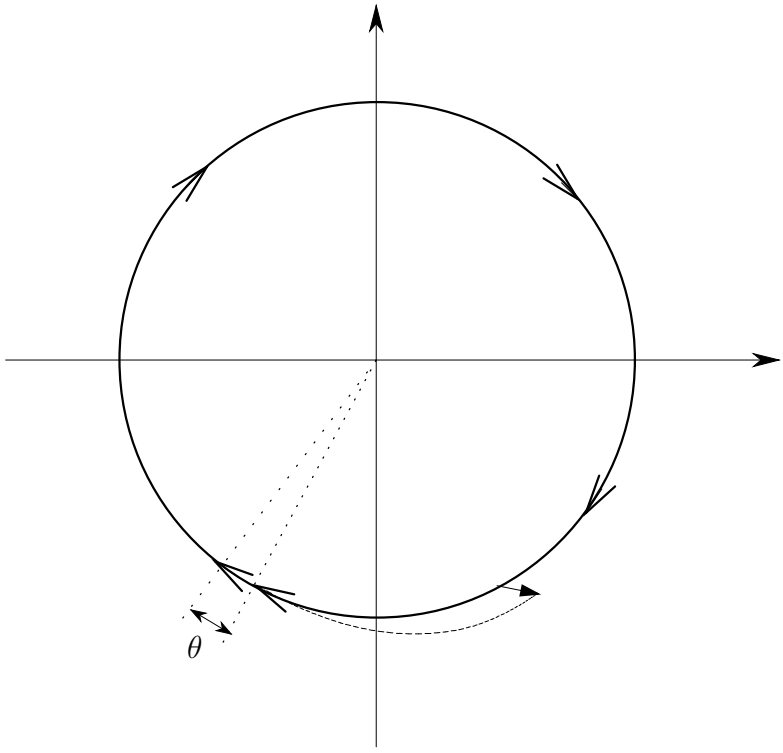


Figure 2.6: Stable limit cycle with noise impulse. The units on the axes could for example be the voltage over the capacitor and the current through the inductor.

2.3.1 Amplitude Noise

When a noise impulse causes the amplitude to change, the amplitude-controlling mechanism of the oscillator will correct for this error with time as explained above.

The amplitude noise is often less important than phase noise because many circuits, such as switching mixers, are less susceptible to amplitude noise than phase noise. However, in some cases we may have requirements on the amplitude noise as well.

2.3.2 Phase Noise

Oscillators are autonomous systems, *i.e.* self-timed systems, and cannot correct a timing error within the oscillator once it has occurred since there is no possibility to compare to a true timing value. Hence, any timing or phase errors will accumulate with time and since oscillators are nonlinear and time-variant systems, these timing errors are not easy to calculate.

The phase noise $\mathcal{L}$ is defined as follows: the phase perturbation power in 1 Hz bandwidth at offset ω_m from center frequency ω_0, normalized to the power of the fundamental component.

A typical phase-noise spectrum of a free-running oscillator is shown in Figure 2.7. Beginning to the right we have a phase-noise floor. To the left of this region, we have phase noise which is inversely proportional to the square of the offset frequency ω_m. The cause of this noise is the white noise in the oscillator components. Further to the left, phase noise is inversely proportional to the cube of the offset frequency. The cause of this noise is the 1/f noise in the components that is upconverted to the oscillation frequency. The corner frequency between the $1/\omega_m^2$ region and the $1/\omega_m^3$ region is termed $\omega_{m,1/f}$. At low offset frequencies the phase-noise spectrum levels out.

The phase noise affects Radio Frequency (RF) circuits in several ways; it affects the transmitted spectrum, the signal constellation, and the Signal-to-Noise Ratio (SNR) after downconversion [Mehrotra and Sangiovanni-Vincentelli, 1999]. The timing jitter affects sampling circuits since there is now an uncertainty in the sampling instants, see Figure 2.8. If the sampling occurs at different time instants than what one expects, there is an error in the sampled value compared to the true value at the wanted sampling instant if the sampled signal has changed between the wanted and the actual sampling instants.

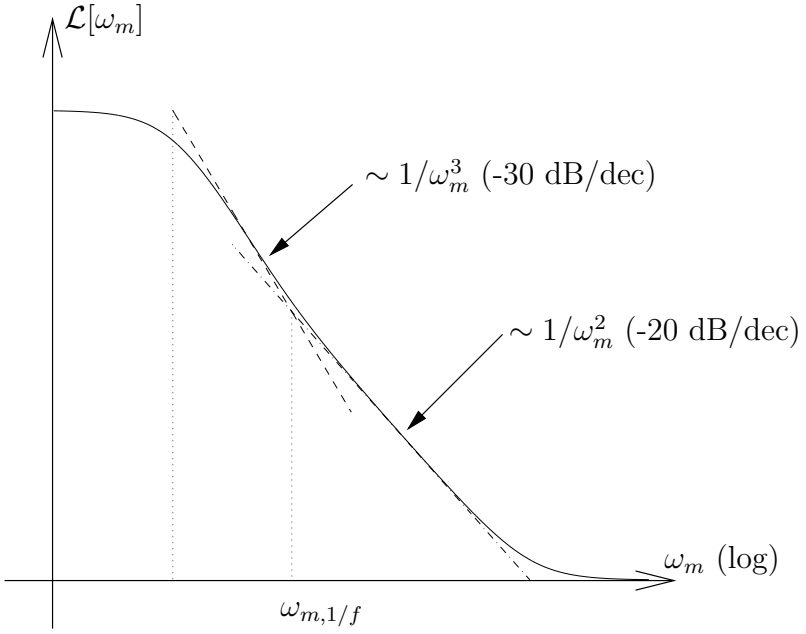


Figure 2.7: Phase noise of sinusoidal oscillator as a function of offset frequency.

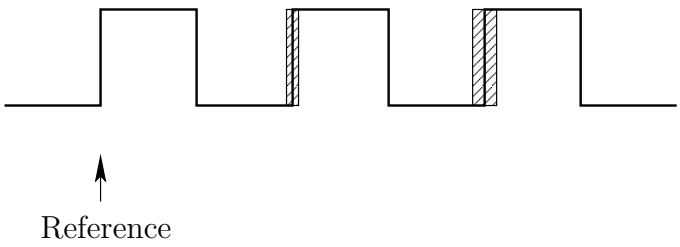


Figure 2.8: Timing jitter in oscillator with squarewave output.

AM-to-PM Conversion

Even if the amplitude noise *per se* is unimportant in many applications, it may be converted into phase noise through a process called AM-to-PM conversion. This conversion occurs, for example, when a nonlinear capacitor is used for frequency tuning. When the voltage amplitude increases, the capacitance is affected and the frequency changes. Frequency error and phase error are coupled since the instantaneous frequency is the time-derivative of the phase.

2.3.3 Injection Locking

Injection locking may occur in oscillators when an input signal of sufficient magnitude is injected and the oscillation frequency changes from the free-running frequency to that of the injected signal [Adler, 1946, Kurokawa, 1973]. The injected signal must be close enough to one of the multiples of the fundamental free-running frequency for an injection lock to occur.

In some cases the injection locking is desired, as in some radio receivers, but in other cases it might be a problem, as when the oscillator locks to a disturbance from nearby circuitry.

2.4 Specifying an Oscillator

Before an oscillator can be designed, we must know what the requirements on this particular oscillator are. Foremost, we have the functional specification: the oscillator should produce a certain waveform at a given frequency. In addition there are requirements on design properties which specifies how much the function may deviate from the desired one, for example expressed as phase noise spectrum. There are usually additional design constraints due to the application in which the oscillator is to be used. One typical such constraint is the supply voltage. Finally, we usually have a cost function, for example minimization of power consumption.

A list of requirements could be as follows:

- Center frequency and frequency stability
- Frequency tuning range
- Phase noise / Timing jitter
- Immunity to disturbances (supply, load variations, substrate)

- Power consumption
- Supply voltage
- Output waveform
- Start-up time
- Cost (price/size/design time)
- ...

All these requirements should generally be fulfilled over fabrication variations, component aging and temperature variations.

2.5 Designing an Oscillator

So: how do we now design an oscillator to the given requirements, or formulated differently: how do we implement the oscillator in electronic building blocks such as transistors, resistors, capacitors and inductors? We must from the specification determine

- Circuit topology
- Method for amplitude control
- Frequency tuning implementation
- Component values
- ...

Not only do we want to create an oscillator that fulfills the specification, we also want to do it in as short design time as possible while still guaranteeing proper function. This task is far from easy, but it is not unique for the design of oscillators; the same question arises in all electronic design. If we manage to achieve orthogonality between the design properties, we can design for each of these properties individually and hence simplify the design process considerably since we only have to look at one property at a time. In addition, we should do this in a systematic way not to forget any requirements. If complete orthogonalization is achieved we may design the oscillator in a top-down fashion without any iterations, guaranteeing very short design time indeed.

Chapter 3

Oscillator Design Methodology

The proposed oscillator design methodology is described in this chapter. Together with Chapter 4, which contains the derivations, it provides all the information necessary to design an oscillator in a systematic way.

Following the description of the design methodology, three design examples with different specifications are presented. Using the proposed design methodology, I design each oscillator according to specification in great detail to show how each step in the design methodology is carried out. Finally, I discuss whether it is possible to show if the design methodology will work in all cases or not.

3.1 Introduction

An oscillator design methodology should facilitate the design of a functioning oscillator which fulfills the specification over manufacturing variations, temperature variations and aging of components; and it should preferably minimize the design time and effort. It should also indicate, as early as possible in the design process, whether a design specification is attainable or not. Finally, it should preferably be based on analytical expressions simple enough to be understood and hand calculated in order to give the designer the insights needed.

The design methodology described in this chapter fulfills these requirements for many types of oscillators encountered today. It is useful both for the design of LC oscillators, with or without frequency tuning, and for the design of crystal oscillators. The design methodology also provides a macro model for the phase noise as a function of the power consumption and im-

plementation process to be used during the overall system design.

When developing a design methodology, one usually strives to attain orthogonality between the different requirements. If orthogonality is achieved, each of the requirements can be designed for separately and one can concentrate on one goal at the time, according to the principle of divide and conquer. This division speeds up the design process considerably.

However, the orthogonality should not come at the expense of too much performance. It is often reasonable to lose some performance if we get a design that still fulfills the specification, especially if the design time is shortened. However, if the design requirements are tough to fulfill, the performance loss may not be acceptable. The design methodology presented in this chapter strives to achieve orthogonality whenever the performance is affected to a lesser extent, but in the cases where substantial performance must be sacrificed some requirements are considered simultaneously.

The design methodology targets harmonic oscillators where the requirements on output waveform and absolute frequency accuracy are modest and the primary cost function is the power consumption. High requirements on output waveform and absolute frequency accuracy preclude the use of transistors operating in a nonlinear fashion with high voltage amplitudes and high power efficiency, but most oscillator designs do not have these requirements.

3.2 Methodology

We now introduce the design methodology, which is based on the following steps:

1. Specification Attainable?
2. Topology Selection
3. Initial Component Sizing
4. Simulation and Optimization
5. Implementation and Verification

The work in this thesis is aimed at the first three steps, after which we have attained an oscillator topology with an initial sizing of all components. The last two steps are not part of the work in this thesis and are described elsewhere in the literature.

In the first step, we choose the implementation process and check if the specification is possible to fulfill. If the specification appears to be impossible

or close to impossible to achieve, we must reassess the considerations we used when we came up with the specification for the oscillator.

In the second step, we derive which topology to use, that is, which types of components to use and how to connect them together.

In the third step, we choose values for all the components that make up the oscillator. In case of a discrete implementation, we choose which resistors, capacitors, inductors, transistors, *etc*, to use, and in the case of an integrated implementation, we size all components.

3.2.1 First Step: Specification Attainable?

Before we start our design effort we need to know if the specification is possible to fulfill using the chosen implementation process, or which implementation process to choose if there is a choice among several available implementation processes.

The minimum achievable phase noise due to the white noise in the oscillator itself, $\mathcal{L}_{min}$, is given by

$$\mathcal{L}_{min}[\omega_m] = \frac{k_B T}{2 P_{DC} Q^2} \frac{\omega_0^2}{\omega_m^2}, \tag{3.1}$$

where ω_m is the frequency offset, ω_0 is the oscillation frequency, P_{DC} is the power consumption, Q is the oscillator Q-value, k_B is the Boltzmann constant, and T is the operating temperature. This expression is further discussed at the end of this section.

We use the concept of Oscillator Design Efficiency (ODE) [van der Tang and Kasperkovitz, 2000] and define the oscillator design efficiency, Υ, according to

$$\Upsilon = \frac{\mathcal{L}_{min}[\omega_m]}{\mathcal{L}[\omega_m]}, \tag{3.2}$$

where $\mathcal{L}$ is the actual phase noise of the oscillator and where the ODE, Υ, is less than unity (negative when expressed in dB), see discussion at the end of this section. For most good oscillator designs, the ODE ends up in the order of 1% to 10% (-20 dB to -10 dB). How large the ODE is depends on the requirements: a small tuning range and low component spread tend to increase it, but a higher oscillator design efficiency than -10 dB is hard to achieve in all cases. On the other hand, it should be possible to have an oscillator design efficiency of at least -20 dB for most specifications.

Usually in an LC oscillator, the Q-values of the inductors dominate the total Q-value of the oscillator and the Q-value of the inductors may be taken as a preliminary value for the Q-value of the oscillator. In a crystal oscillator,

the Q-value should be set by the crystal, and as a preliminary value the Q-value of the crystal operating with the intended capacitive load may be used.

Using the requirements on phase noise, power consumption and the estimated Q-value, we can now determine if it is possible to design an oscillator with these requirements by calculating the oscillator design efficiency, and we can also get an estimation of how hard it will be to design. The toughest requirement for the oscillator phase noise should be used when several requirements are given, and since the Q-value of components often changes with temperature, the minimum Q-value should be used. However, just because the specification passes this test does not necessarily means that it is possible to build the oscillator since there are usually more requirements involved.

If the oscillation frequency should be adjustable during operation, we must make sure that there are varactors that fulfill the requirements on Q-value and capacitance ratio needed for the tuning range. Sometimes it may be wise to split the tuning range into several smaller tuning ranges as described later. When splitting the frequency tuning range, the requirements on the varactors usually are relaxed.

If the specification seems possible to fulfill, we proceed to the next step in the design process. First, we discuss a few more matters regarding the Oscillator Design Efficiency (ODE), which will come in handy later during the design process.

The phase noise due to white noise is calculated in Chapter 5 to be

$$\mathcal{L}[\omega_m] \approx \frac{k_B T F}{2 P_1 Q^2} \frac{\omega_0^2}{\omega_m^2}, \tag{3.3}$$

where P_1 is the power at the oscillation frequency dissipated in the feedback network and F is the noise factor. Using (3.3), we see that the oscillator design efficiency is given by

$$\Upsilon = \frac{\eta}{F}, \tag{3.4}$$

where F is the noise factor and η is the power efficiency defined as

$$\eta = \frac{P_1}{P_{DC}}. \tag{3.5}$$

Optimizing an oscillator from the white noise point of view is seen to be the process of maximizing the fraction η/F, which is always less than unity (0 dB) because $F \geq 1$ and $\eta \leq 1$. Hence, $\mathcal{L}_{min}$ gives a lower bound for the phase noise.

3.2.2 Second Step: Topology Selection

We shall now select a topology that fulfills our requirements on the oscillator using the chosen technology/components. The choice of *a differential or a single-ended topology* is made based on information on surrounding circuits and supply/ground/substrate disturbances. In general, integrated oscillators are implemented as differential circuits since the environment is noisy and the oscillator shares the substrate with other circuitry. Discrete oscillators are usually implemented as single-ended circuitry to keep the component count low and hence the price and size down.

Once we have chosen the type of transistors to use and whether we are going for a single-ended or differential topology, it is time to design the *feedback network* and bias the active part. These two tasks are done simultaneously since the feedback network is an integral part of the biasing network; the inductors and capacitors of the feedback network may act as coupling and decoupling components in the biasing arrangement. The feedback network is usually chosen as simple as possible since more complicated networks add poles and zeros to the loop transfer function and make the amplitude stability of the oscillator harder to guarantee.

The *ground datum* is chosen based on information about parasitic elements, such as stray capacitances and inductances, and the tuning circuitry. For example, in an integrated oscillator many components share the same substrate which is usually connected to the supply ground. We must also take into consideration whether the voltages are allowed to swing above the supply voltage or not. External noise sources, such as supply noise, also affect the choice of grounding strategy. The inherent minimum phase noise of the oscillator is also affected by this choice, as seen in Section 4.4, but in many cases the other aspects mentioned above are more important.

We next focus on the *frequency tuning*. As mentioned above, the components used to perform the frequency tuning, usually voltage-dependent capacitors such as MOS structures or reverse-biased diodes, play a part in determining the feedback network to use and the grounding strategy. The reason for this restriction is that the varactors often need to have one terminal signal-grounded and that the varactors are sensitive to *any* voltage changes over them, including those of unwanted disturbances on for example supply lines transferred to the varactor.

We also need to calculate the *tuning range* needed to cover the frequency band of interest, taking into account aging, temperature variations and process variations. If the frequency tuning range turns out to be wide compared to the center frequency, it may be wise to split the tuning range into several smaller tuning ranges by implementing part of the tuning capacitance as

fixed capacitors in series with transistors operating as switches. The choice of splitting may also make the tuning characteristic more linear, which is often an advantage when using a Voltage Controlled Oscillator (VCO) in a Phase-Locked Loop (PLL). A final advantage of splitting the tuning range into several smaller tuning ranges is that the phase noise decreases since part of the phase noise is an increasing function with $\frac{f_{tune}}{f_0}Q$, where f_{tune} is the tuning range and f_0 is the center frequency. This matter is further discussed in Chapter 6.

The last step in the topology selection is to design an *amplitude-determining network* to make the oscillation amplitude independent of component variations during manufacturing. This network may also help to reduce the phase noise, especially the phase noise due to 1/f noise. The simplest amplitude controls use nonlinearities in the transistors or explicit diodes as voltage limiters. These types of amplitude controls make the Q-value of the oscillator independent of temperature, aging and process variations, unless the bias current of the oscillator is changed with for example temperature. When the Q-value is made constant using this type of amplitude limiting, it is reduced to its lowest possible value. Using this type of amplitude control increases the phase noise due to the reduction in Q-value, but the design effort is quite low.

An Automatic Amplitude Control (AAC) does not lower the Q-value of the oscillator considerably, but requires much more design effort. Circuitry that measures the oscillation amplitude as well as circuitry that controls the bias voltages or currents of the oscillator must be designed, and the control loop must be stable and have enough bandwidth while not contributing too much noise or consuming too much power. Consequently, this type of amplitude control is usually used only when simpler methods do not fulfill the requirements such as for a crystal oscillator with requirement on short start-up time.

3.2.3 Third Step: Initial Component Sizing

Once we have designed the topology, it is time to size all the components of the oscillator. This task is carried out in several smaller steps. First we determine the voltage gain of the feedback network, Z_{21}/Z_{11}, by maximizing the Oscillator Design Efficiency (ODE), Υ, which is the task as maximizing the fraction η/F, where η is the power efficiency and F is the noise factor. In addition to the voltage gain, we also determine all bias voltages and currents and the oscillation amplitudes at the input and output of the active network. Some useful expressions for different topologies are available in Section 4.4.

One important source of noise not covered above is the noise of series base

and gate resistances. As shown in Section 7.2.3, the phase noise due to the series base and gate resistances depends on the levels of harmonics generated in the active device. Since the FET has significantly weaker nonlinearity than the BJT, this source of noise is mostly a problem of oscillators based on BJTs. From (7.23) we have that

$$\frac{R_I}{\Re[Z_{11}]}\frac{\Re[Z_{11}]^2}{Z_{21}^2}\sum_{n=1}^{\infty}\frac{n^2|\widetilde{F}_n|^2}{|\widetilde{F}_1|^2} \ll 1 \tag{3.6}$$

in order for this additional phase noise to be negligible, where R_I is the series base or gate resistance and $\widetilde{F}_n$ is the describing function for the active part.

For an oscillator based on a single BJT stage, we use (C.24) to get

$$\frac{R_I}{\Re[Z_{11}]}\frac{\Re[Z_{11}]^2}{Z_{21}^2}\frac{4}{9}\left(\frac{V_{in,1}}{V_T}\right)^{\frac{3}{2}} \ll 1 \tag{3.7}$$

and for a BJT differential stage, we use (C.46) to get

$$\frac{R_I}{\Re[Z_{11}]}\frac{\Re[Z_{11}]^2}{Z_{21}^2}\frac{1}{4}\frac{V_{in,1}}{V_T} \ll 1, \tag{3.8}$$

where in both expressions $V_{in,1}$ is the input-voltage amplitude to the active network. If these inequalities are not fulfilled, the choice of the voltage gain $\frac{Z_{21}}{Z_{11}}$ must be reassessed, this time taking also the series base resistance into account.

Once the phase noise due to white noise sources has been designed for, we focus on the phase noise due to 1/f noise. The noise corner between phase noise due to white noise and phase noise due to 1/f noise is given by (7.96) as

$$\omega_{m,1/f} = \frac{2\pi(K_{1/f,f}+K_{1/f,b})I_{DC}P_1}{4k_BTF}\left(K_{AM-PM}\frac{1}{B}\frac{\partial B}{\partial I_{DC}}+\frac{\partial\zeta}{\partial I_{DC}}\right)^2, \tag{3.9}$$

where $K_{1/f,f}$ is the 1/f noise constant of the active network, $K_{1/f,b}$ is the 1/f noise constant of the bias network, I_{DC} is the bias current, P_1 is the fundamental power delivered to the feedback network, K_{AM-PM} is the AM-to-PM conversion, B is the amplitude gain of the active network and ζ is the phase shift of the active network.

We choose to size the transistors to maximize their transit frequency, f_T, and in the cases where there is a current density that gives a peak f_T, size the transistors to get that current density. This choice makes $\frac{\partial\zeta}{\partial I_{DC}}$ small

and minimizes the phase noise contribution from induced gate noise. Also assuming that $\frac{\partial B}{\partial I_{DC}} \approx \frac{B}{I_{DC}}$, we get the noise corner as

$$\omega_{m,1/f} \approx \frac{2\pi(K_{1/f,f} + K_{1/f,b})P_1}{4k_BTFI_{DC}}K_{AM-PM}^2, \tag{3.10}$$

which can be rewritten as

$$\omega_{m,1/f} \approx \frac{2\pi(K_{1/f,f} + K_{1/f,b})\Upsilon V_{DC}}{4k_BT}K_{AM-PM}^2, \tag{3.11}$$

where Υ is the Oscillation Design Efficiency (ODE) and V_{DC} is the supply voltage. We see that there is two principal methods to reduce the phase noise due to 1/f noise: choose components with low inherent 1/f noise to get low $K_{1/f}$, and reduce the AM-to-PM conversion, $|K_{AM-PM}|$. We assume that Υ is set by requirements on phase noise due to white noise. Since we already have requirements on the speed of the transistor, we cannot make them larger to reduce the inherent 1/f noise, but we could for example choose PMOS transistors if they have much lower 1/f noise than NMOS transistors. What remains is the AM-to-PM conversion coefficient which is minimized by the use of a strong amplitude control as explained in Chapter 5.

3.2.4 Fourth Step: Simulation and Optimization

Once we have an initial sizing of all components, we may commence simulation of the oscillator to determine if it is working as intended. We may now also tweak the component values to optimize the performance. Since the simulator usually includes more details in its component models, the results will probably differ somewhat from the hand-calculated ones, but the error should not be large since most essential component characteristics are included in the design methodology. The hand calculations used during the design process are never better than the models used during these calculations. The same conclusion is also true for simulators; the simulation results are never better than the accuracy of the component models.

3.2.5 Fifth Step: Implementation and Verification

The last step in the design process is to actually build the circuit and measure it to verify the actual performance. This verification phase can be quite time consuming, especially if a high confidence that the design meets the specification over temperature and process spread in mass production is needed.

3.3 Design Examples

The design methodology outlined above is applied to three design examples in this section. Design examples with different specifications are carried out to highlight different aspects of the design methodology. Before studying these design examples in detail, it is recommended to read through Chapter 4.

3.3.1 Crystal Oscillator

The first design example is a crystal oscillator. The oscillator may be used as a stable frequency reference with low phase noise.

Specification

Design a crystal oscillator using the crystal with specifications given below. The phase noise and power consumption should be minimized. The supply voltage is 5.0 V and the temperature operating range is -25°C to 80°C.

The crystal has the following specifications: $f_0 = 6.144$ MHz, $C_L = 16$ pF, $R_1 = 30 \sim 50\ \Omega$, $C_0 \approx 4$ pF, $C_1 \approx 14$ fF, $P_{max} = 100\ \mu$W.

First Step: Specification Attainable?

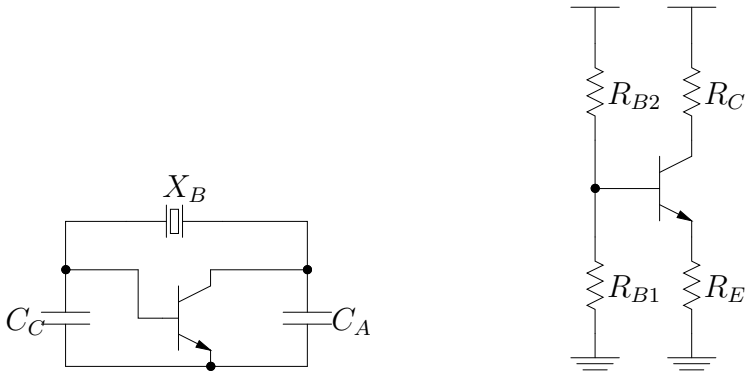
As the first step in the design process, we calculate what performance we expect to verify that the design specification makes sense.

The maximum drive level for the crystal was given as $P_{max} = 100\ \mu$W. Since we will minimize power consumption and we have an ideal power supply, we will probably end up with a power efficiency, η, in excess of 10%. Hence, the power consumption, P_{DC}, will probably not exceed 1 mW. Consequently, the currents will be low and impedances high, which might pose a problem later on in the design process.

We conclude that the specification seems attainable and proceed with the topology selection. Before proceeding with the design, we estimate the resulting phase-noise performance, which is limited by the crystal.

To calculate what phase-noise performance we might expect to get, we need to estimate the Q-value. From (4.7) we get the minimum series Q-value, Q_S, as 37000 when R_1 is 50 Ω. From (4.47) we get the minimum Q-value for the oscillator as 23700. In reality, we may have an even lower Q-value due to additional losses and parasitic capacitances parallel to C_0. However, we use the calculated value for now to estimate the phase noise of the oscillator.

Using (3.3) we get the minimum achievable phase noise at room temperature (25°C) as -138.6 dBc at 10 Hz offset by assuming that the noise



(a) AC schematic. (b) DC schematic.

Figure 3.1: AC and DC schematics for crystal oscillator.

factor, F, is unity, the Q-value, Q, is that given above and that P_1 is P_{max} equal to 100 μW. Due to the reduction in Q-value mentioned in the previous paragraph and the noise factor, F, we expect the phase-noise performance to be worse by approximately 3 dB to 10 dB, depending on the quality of the other components.

Second Step: Topology Selection

Since we are building a discrete circuit, we go with a single-ended solution based on a BJT. As described in Section 4.1.7, a crystal network can be designed by replacing one of the inductors in an LC network by a crystal. From Section 4.1.6 we have that LCL and CLC networks are the only two networks with the right sign for the transfer impedance when we go for a single-ended circuit. We prefer the CLC network over the LCL network since it is easier to bias and has fewer inductors. The chosen AC topology is shown in Figure 3.1(a).

The next step is to bias the bipolar transistor. A general biasing scheme for a one-transistor topology using resistors is shown in Figure 3.1(b). The emitter current is determined by the emitter resistor, R_E, and the voltage potential at the base, which in turn is set by the two resistors R_{B1} and R_{B2}. The collector voltage potential is set by the emitter current and the collector resistor, R_C.

We now need to determine which node should be the ground datum. The crystal does not need to have any lead grounded and we may hence chose to signal-ground the emitter node. This choice gives a higher Q-value since the parasitic capacitances C_{P1} and C_{P2} in the crystal, see Section 4.1.4, do not end up parallel with C_0. By signal-grounding the emitter, we place these

parasitic capacitances in parallel with to C_A and C_C. The full schematic is shown in Figure 3.2 where we have added the capacitor C_E to signal-ground the emitter.

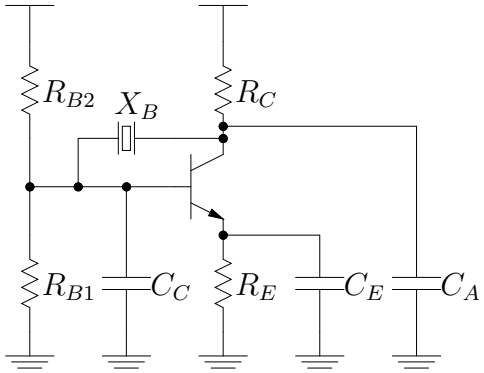


Figure 3.2: Complete schematic for crystal oscillator.

We might want to replace the resistor R_C with an inductor or add an inductor in the base biasing network to provide a higher AC impedance. It is also possible that we need to add a capacitor in series with the crystal if the series capacitance of C_A and C_C is higher than the prescribed load capacitance C_L. We will know if these modifications are needed once we have calculated the component values in the next step of the design methodology.

The remaining topology decision is the means for amplitude control. Since the power consumption is very low and we do not have any requirement on the start-up time, we do not gain much by using an explicit amplitude control. Consequently, we choose diode limiting amplitude control using the base–collector diode, because this way we avoid adding another component.

Third Step: Initial Component Sizing

We first need to decide which transistor to use. We want a transistor with low series base resistance and low parasitic capacitances. A transistor fulfilling these requirements is the NPN transistor 2N2369 with the following data: $C_{BE} \approx 3$ pF, $C_{BC} \approx 3$ pF, $r_{bb} \approx 10\ \Omega$ and $\beta \approx 40$.

The capacitance C_{BC} is parallel to C_0 of the crystal and needs to be subtracted from C_L. Introducing C_L' as the remaining capacitance, we have

$$C_L = C_{BC} + C_L' \tag{3.12}$$

with $C_L' = 13$ pF in our case. From (4.47), we get the Q-value of the oscillator as

$$Q \approx Q_S \left(\frac{C_L'}{C_0 + C_{BC} + C_L'} \right)^2 \approx 15600. \tag{3.13}$$

From (4.49) and (4.45), we have that the Q-value of the capacitors must fulfill

$$Q_C \gg \frac{C_1}{2(C_0 + C_L)} Q \approx 5.5 \tag{3.14}$$

in order not to degrade the Q-value, which should not pose any difficulties. We will for now assume that this inequality is fulfilled and check it later.

The next step in the choice of components is to calculate the Z-parameters of the feedback network in order to calculate the capacitances. The fundamental power delivered to the feedback network is given by

$$P_1 = \frac{V_{out,1}^2}{2Z_{11}}. \tag{3.15}$$

The fundamental power, P_1, was given to be less than 100 μW in the specification so we need to choose $V_{out,1}$ to get a value for Z_{11}. We can already now see that it is not practical to replace R_C with an inductor. The impedance of this inductor would need to be very high since the impedance levels are very high due to the low power consumption. Consequently the output voltage cannot swing above the supply voltage. From (4.56) we have

$$|V_{out,1}| \approx V_{c,0} - V_{e,0} - V_{CE,min}, \tag{3.16}$$

where $V_{CE,min}$ is approximately 0.2 V. We choose $V_{e,0} = 1.8$ V for good bias stability and small shift in bias current during start-up. A higher value would give better stability but lower power efficiency and higher power consumption. We also choose

$$V_{c,0} = V_{DC} - |V_{out,1}| \tag{3.17}$$

to maximize the output amplitude and thereby the efficiency. Combining these two last equations we get

$$|V_{out,1}| = \frac{V_{DC} - V_{e,0} - V_{CE,min}}{2} = 1.5 \text{ V}. \tag{3.18}$$

We can now calculate Z_{11} as

$$Z_{11} = \frac{V_{out,1}^2}{2P_1} \approx 11.3 \text{ k}\Omega. \tag{3.19}$$

From (4.19) we have

$$Z_{11} \approx \frac{X_A^2}{R_S}, \tag{3.20}$$

where

$$R_S \approx R_1 \left(\frac{C_0 + C_{BC} + C_L'}{C_L'} \right)^2 \leq 118 \ \Omega \tag{3.21}$$

from (4.48). Hence, we get $X_A = -1.15$ kΩ and

$$C_A = -\frac{1}{\omega_0 X_A} \approx 22 \text{ pF}. \tag{3.22}$$

We now need to determine the fraction $\frac{Z_{11}}{|Z_{21}|}$ in order to calculate C_C. A high fraction gives us higher Q_C and lower bias variations during start-up but higher phase noise, see Figure 4.19(c). As a compromise, we choose a value of 3 which gives only a slight degradation of the phase-noise performance. From (4.23) we have

$$\frac{Z_{21}}{Z_{11}} \approx -\frac{X_C}{X_A} = -\frac{C_A}{C_C}, \tag{3.23}$$

giving us $X_C \approx -384$ Ω and $C_C \approx 67$ pF.

Calculating the series connection of C_A and C_C, we get a load capacitance for the crystal of 17 pF which is higher than the wanted value C_L'=13 pF. Since the value is only slightly higher than the wanted, we choose to modify C_A and C_C instead of adding a capacitor in series with the crystal. This choice gives us slightly lower power P_1, but one component less. The new values are $C_A = 18$ pF and $C_C = C_{BE} + 47$ pF, where we have chosen capacitors from the E12 series. The new reactances are $X_A = -1.44$ kΩ and $X_C = -520$ Ω and the new input impedance to the feedback network is $Z_{11} = 17.5$ kΩ.

Assuming that $|V_{out,1}| \approx 1.5$ V, we get $|I_{out,1}| = 86$ μA and from (4.147) we have $I_{c,0} = 43$ μA. We also have

$$R_C = \frac{V_{DC} - V_{c,0}}{I_{c,0}} = \frac{|V_{out,1}|}{I_{c,0}} \approx 35 \text{ kΩ} \tag{3.24}$$

and choose $R_C = 36$ kΩ from the E24 series. The Q-value for Z_A then becomes 25, which fulfills the requirement on Q_C. We also have

$$R_E = \frac{V_{e,0}}{I_{e,0}} \approx \frac{V_{e,0}}{I_{c,0}} \approx 41.9 \text{ kΩ} \tag{3.25}$$

and choose $R_E = 39$ kΩ from the E24 series.

We proceed with the bias resistors R_{B1} and R_{B2}. The DC voltage at the base terminal is given by (4.55) as

$$V_{b,0} = V_{e,0} - |V_{in,1}| + V_{BE,max} \approx 1.9 \text{ V}, \tag{3.26}$$

where we have assumed that $V_{BE,max} = 0.6$ V. During start-up we will have $|V_{in,1}| = 0$ which gives $V_{e,0} \approx 1.3$ V and $I_{e,0} \approx 33$ μA. This start current corresponds to a small-signal loop gain of 7.5 at room temperature. The

current through R_{B1} should be at least ten times higher than the base current for good bias stability, which corresponds to a current of at least 11 μA. Higher current gives lower resistances, which in turn gives a lower Q-value for C_C. We choose $R_{B1} = 160$ kΩ and $R_{B2} = 240$ kΩ. The parallel connection of R_{B1} and R_{B2} is 96 kΩ which gives a Q-value of 185 for C_C – well above the required minimum Q-value.

The last component to size is the capacitor C_E. The reactance from this component must be much less than X_A and X_C at the oscillation frequency. A capacitance of 10 nF gives a reactance of -2.6 Ω.

The current consumption may be found by adding the emitter DC current and the current flowing through R_{B1}, 46 μA and 12 μA, giving a total current consumption $I_{DC} = 58$ μA. The power efficiency is given by

$$\eta = \frac{I_{e,0}}{I_{DC}} \frac{V_{out,1}}{V_{DC}} \approx 24\%. \tag{3.27}$$

The total power consumption is 290 μW and the power delivered to the crystal is 67 μW. We also calculate the peak current from (C.23) to be approximately 500 μA which should not cause any problems.

We check if the base resistance is low enough to give negligible contribution to the phase noise. Using (3.7), we have

$$\frac{r_{bb}}{Z_{11}} \frac{Z_{11}^2}{Z_{21}^2} \frac{4}{9} \left(\frac{V_{in,1}}{V_T} \right)^{\frac{3}{2}} \approx 0.2, \tag{3.28}$$

which gives negligible contribution to the phase noise. The noise factor for the oscillator is given by (4.173) as

$$F \approx 1 + \frac{1}{2} \frac{Z_{11}}{|Z_{21}|} \approx 2.5, \tag{3.29}$$

and if we add the contribution from the base series resistance, we get a noise factor of 2.7. The Oscillator Design Efficiency (ODE) can now be calculated from (3.4) to be -10.7 dB, which is very good considering that the design is done without inductors. We calculate the minimum achievable phase noise, $\mathcal{L}_{min}$, from (3.1) to be -139.6 dBc/Hz at 10 Hz offset for the calculated power consumption. The phase noise can now be calculated using (3.2) to be -128.9 dBc/Hz at 10 Hz offset.

If we had the requirement that the oscillation amplitude must be very stable, we could increase the current consumption to make the amplitude limiting stronger at the expense of higher power consumption.

Fourth Step: Simulation and Optimization

We simulate the oscillator, including measurement buffers, to verify the functionality. We get an output-voltage amplitude, $V_{out,1}$, of 1.102 V and an input-voltage amplitude, $V_{in,1}$, of 0.402 V. The simulated current consumption is 56.5 μA and the simulated phase noise is -132.1 dBc at 10 Hz offset.

We deem the simulated performance to be satisfactory and proceed with the implementation of the oscillator.

Fifth Step: Implementation and Verification

The oscillator was built and measured. The measured current consumption was 54 μA at 5.0 V supply and the oscillation frequency was 6.146 MHz. The phase noise could not be measured due to lack of instruments capable of measuring such low phase noise.

Summary

The performance of the crystal oscillator in room temperature is summarized in Table 3.1. The calculated, simulated and measured values agree quite well. It was, unfortunately, not possible to measure the phase noise of the implemented oscillator.

Table 3.1: Performance of crystal oscillator.

	spec.	calc.	sim.	meas.	unit
I_{DC}	min.[a]	58	57	54	μA
$\mathcal{L}$ @ 10 Hz	min.[b]	-128.9	-132.1	?[c]	dBc/Hz

[a]The current consumption should be minimized once the phase noise has been minimized.

[b]The phase noise should be minimized subject to constraint on maximum power dissipated in the crystal.

[c]Could not be measured with the measurement equipment available.

3.3.2 VCO using JFET

The next design example is a Voltage-Controlled Oscillator (VCO) to be used in an FM system. The primary function of the VCO is to frequency-modulate the signal.

Specification

The VCO is part of a loop controlling the average output frequency to 100 MHz. The function of the loop is to relate the output carrier frequency to that of a stable frequency reference, for example a crystal oscillator. The loop bandwidth is much lower than the lowest frequency component of the input information signal and does not interfere with the frequency modulation.

The requirements on the modulation is as follows: full modulation of 75 kHz, input modulation bandwidth from 30 Hz to 15 kHz, and incidental frequency modulation of at least 100 dB below full modulation. We also want to minimize the power consumed by the VCO, which is supplied from a voltage source of 6.0 V.

We first calculate the requirement on phase noise from the requirement on incidental frequency modulation, β_f. From this requirement we have $\beta_f \leq 0.75$ Hz. The maximum allowed phase noise can be calculated from

$$\beta_f = \sqrt{2 \int_{f_l}^{f_h} f_m^2 \mathcal{L}[f_m] df_m} \tag{3.30}$$

to be -127.26 dBc at 10 kHz offset, where we have used $f_l = 30$ Hz and $f_h = 15$ kHz from the specification and assumed that the phase noise origins from white noise alone.

First Step: Specification Attainable?

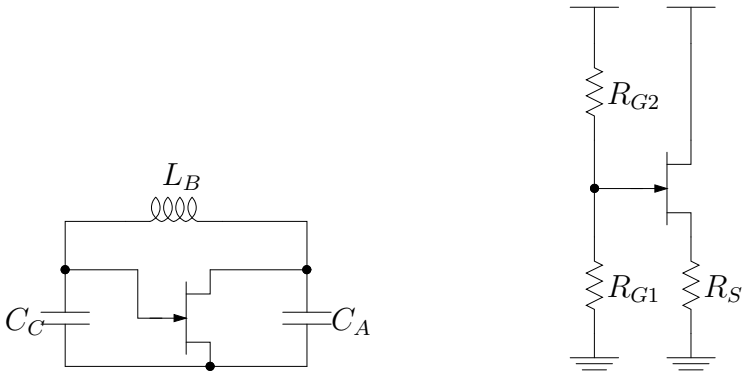
Since the phase-noise performance is specified, we can calculate what power consumption will be necessary to fulfill this requirement to see if the specification makes sense. From (3.1) we have

$$P_{DC,min} = \frac{k_B T}{2\mathcal{L}[\omega_m] Q^2} \frac{\omega_0^2}{\omega_m^2}, \tag{3.31}$$

which gives us a lower limit of 0.44 mW, assuming that the Q-value of a discrete inductor is at least 50. Since the ODE probably will be worse than -10 dB, we expect the power consumption, P_{DC}, to be somewhat above 5 mW. This power consumption should not pose any problems and we may proceed to the next step in the design methodology.

Second Step: Topology Selection

We choose to base our design on a JFET, since JFETs are known to have low 1/f noise and designs based on FETs are less sensitive to series base/gate



(a) AC schematic. (b) DC schematic.

Figure 3.3: AC and DC schematics for JFET oscillator.

resistance than designs based on BJTs. The base series resistance would probably impact the design if a BJT is chosen, since the power consumption is much higher and therefore the impedance levels are much lower in this oscillator than the previous design example. Discrete bipolar transistors with low parasitic capacitances and low series base resistance are not common.

The only simple feedback networks with the correct sign are CLC and LCL networks, as discussed in Section 4.1.6. We choose the CLC network because it is easier to bias and has fewer inductors, which are less ideal than capacitors. The resulting AC schematic is shown in Figure 3.3(a).

The transistor must also be biased to get its desired amplifying operation. We use the common bias scheme of Figure 3.3(b). The bias current is set by R_S in combination with the gate potential set by V_{DC}, R_{G1} and R_{G2}.

The next step is to determine the ground datum. From Section 4.4.1 we have that common-gate and common-source configurations have better phase-noise performance than does the common-drain configuration. We choose to signal-ground the gate in this oscillator and the resulting schematic is shown in Figure 3.4.

We proceed with the means for amplitude control. Since we design a discreet implementation, we choose to implement the amplitude control using the nonlinearity in the transistor to keep the component count down. In this case, the nonlinearity reduces the output-current amplitude from the transistor when it enters the linear region.

The last decision to make for the topology is the means for frequency modulation. We may choose to use a varactor to change one of the reactances X_A, X_B or X_C. According to Chapter 6, it is preferred if the voltage amplitude across the varactor is low because the AM-to-PM conversion will

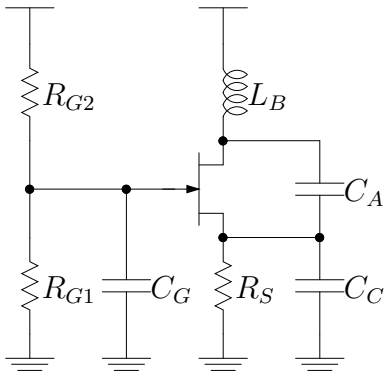


Figure 3.4: Complete schematic for JFET oscillator.

be lower. Since the frequency tuning range is quite moderate, (we only have to modulate 75 kHz and track slow frequency changes due to temperature and aging), we choose to control the reactance X_C. The new schematic is shown in Figure 3.5, where the capacitance C_C now is replaced with a fixed capacitor C'_C in parallel with a reverse-biased diode acting as a varactor. The capacitance C_D provides a low impedance at the fundamental frequency and R_D is inserted to filter out noise on the control voltage V_C.

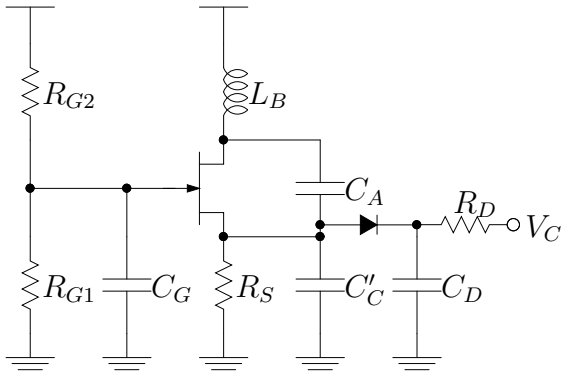


Figure 3.5: Complete schematic for JFET VCO.

Third Step: Initial Component Sizing

Our first choice regards the transistor. Since the operation frequency is quite high, we need a transistor with low parasitic capacitances. We also want the transistor to have small gate–source voltage compared to the supply voltage at the operation current, which we expect to be in the vicinity of 1 mA from the first design step. We choose the BF245A n-channel JFET. It has the

following typical parameters: $K = 1$ mA/V^2, $V_T = -2$ V, $C_{GS} = 2.2$ pF and $C_{GD} = 2.2$ pF.

The spread in threshold voltage, V_T, for this transistor type is estimated to be about ± 0.5 V from the data sheet. Hence, we choose the source terminal DC voltage, $V_{s,0}$, to be 2 V to give a stable bias current over component variations. From the first step, we estimated the DC current to be about 1 mA which gives an overdrive voltage of about 1 V, and consequently the minimum drain–source voltage will be approximately 1 V. We can now calculate the output amplitude from (4.56) to be

$$|V_{out,1}| \approx V_{d,0} - V_{s,0} - V_{DS,min} \approx 3.0 \text{ V}. \tag{3.32}$$

We proceed with the determination of the fraction $\frac{Z_{11}}{|Z_{21}|}$. We want the input amplitude to be at least 1 V to guarantee start-up, which requires that $V_{in,1} > K_{FET} V_{GT0}$, see Section 4.2.3. At the same time, we do not want the input amplitude to be large enough to forward-bias the gate–source diode. Since the input-voltage amplitude is across the diode we get better tuning range when the fraction is low, but we also get higher AM-to-PM conversion. We choose $\frac{Z_{11}}{|Z_{21}|} = 3$ to get $|V_{in,1}| = 1.0$ V.

To calculate the noise factor below, we need to derive the following fraction:

$$\frac{Z_{11}}{R_S} = Z_{11}\frac{I_{d,0}}{V_{s,0}} = Z_{11}\frac{|I_{d,1}|}{2K_{FET}V_{s,0}} = \frac{|V_{out,1}|}{2K_{FET}V_{s,0}} \approx 1.25, \tag{3.33}$$

where we have used that $|I_{out,1}| = 2K_{FET}I_{DC}$, $V_{out,1} = Z_{11}I_{out,1}$ and assumed that $K_{FET} \approx 0.6$.

The noise factor is given in (4.113) as

$$F \approx 1 + \gamma\frac{Z_{11}}{|Z_{21}|} + \frac{Z_{21}^2}{Z_{11}^2}\frac{Z_{11}}{R_S} \approx 3.14, \tag{3.34}$$

where $\gamma = 2/3$. The power efficiency can be calculated from (4.51) as

$$\eta \approx K_{FET}\frac{|V_{out,1}|}{V_{DC}} \approx 0.30. \tag{3.35}$$

Inserting the noise factor, F, and the power efficiency, η, in (3.4), we get

$$\Upsilon = \frac{\eta}{F} \approx 0.096 \tag{3.36}$$

or -10.20 dB. The phase noise is calculated from (3.1) and (3.2) to be -128.40 dBc at 10 kHz offset.

We can now calculate the power consumption, using the ODE, to be at least

$$P_{DC} = \frac{P_{DC,min}}{\Upsilon} \approx 4.6 \text{ mW}. \tag{3.37}$$

We choose P_{DC} equal to 6 mW for some extra margin and get the current consumption, I_{DC}, as 1 mA. The output-current amplitude, $I_{out,1}$, is equal to $K_{FET}I_{DC}$ and becomes approximately 1.2 mA. The input impedance to the feedback network is given by

$$Z_{11} = \frac{V_{out,1}}{I_{out,1}} \approx 2.5 \text{ k}\Omega. \tag{3.38}$$

We can now determine the component values. From (4.19), we have the input impedance, assuming that the inductor, L_B, dominates the Q-value of the oscillator, as

$$Z_{11} \approx \frac{X_A^2}{R_B} = \frac{X_A^2}{X_B}\frac{X_B}{R_B} \approx -Q_B\frac{X_A^2}{X_A + X_C}, \tag{3.39}$$

where we in the last stage used (4.18). Using

$$\frac{Z_{21}}{Z_{11}} \approx -\frac{X_C}{X_A} \tag{3.40}$$

from (4.23), we get

$$X_A \approx -\frac{Z_{11}}{Q_B}\left(1 - \frac{Z_{21}}{Z_{11}}\right) \approx -66.7 \ \Omega, \tag{3.41}$$

corresponding to a capacitance of 23.9 pF; we choose the closest value in the E12 series, which is 22 pF. We also get the reactance X_C as -22.2 Ω, corresponding to a capacitance of 71.6 pF. The reactance X_B is 88.9 Ω, corresponding to an inductance of 141.5 nH. We choose to use an inductor of value 134 nH, which together with the inductance of the wires gives approximately the wanted inductance.

We proceed with the calculation of the biasing components. The resistance R_S is given by the fraction of $V_{s,0}$ and I_{DC}, giving a value of 2.0 kΩ. This resistance in parallel with the reactance X_C gives a Q-value of approximately 90 for this reactance, high enough to have only a small impact on the total oscillator Q-value.

From the transistor parameters we get an overdrive voltage of approximately 1 V, giving a gate potential, $V_{g,0}$, of 1.0 V. This voltage is accomplished by the voltage division between R_{G1} and R_{G2}. We choose R_{G1} to

be 22 kΩ and R_{G2} to be 100 kΩ. Finally C_G is chosen to have much lower impedance then X_B at the oscillation frequency, for example 10 nF corresponding to a reactance of -0.16 Ω.

The last components to be selected are those related to the frequency tuning. We assume that we design for a nominal tuning voltage, V_C, of 5.0 V. This gives a nominal reverse-bias voltage, V_0, of 3.0 V for the diode because the source potential, $V_{s,0}$, is 2.0 V. The values for the diode used are $C_N = 35$ pF and $\psi = 0.7$ V where C_N is the small-signal capacitance when no reverse bias voltage is applied and ψ is the built-in potential, see Section 6.5.

The nominal large-signal capacitance, $\widetilde{C}$, of the diode is approximately given by (6.45) as

$$\widetilde{C} \approx \frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}} \approx 15 \text{ pF}, \tag{3.42}$$

which means that C'_C is chosen from the E12 series to be 56 pF to give the total capacitance, C_C. We finally choose the decoupling capacitance C_D to be 1 nF to provide a low-impedance path for the fundamental component, and we choose R_D equal to 1 kΩ to suppress high-frequency disturbances on the control voltage V_C.

We now want to know what VCO tuning constant, K_{VCO}, we get with the chosen component values. We first calculate the total frequency-determining capacitance, C, from (4.32) to be

$$C = \frac{C_A(C'_C+\widetilde{C})}{C_A+(C'_C+\widetilde{C})} \approx 16.9 \text{ pF} \tag{3.43}$$

and the change in total capacitance with respect to the large-signal capacitance of the diode is given by

$$\frac{\partial C}{\partial \widetilde{C}} = \frac{CC_A}{(C'_C+\widetilde{C})(C_A+(C'_C+\widetilde{C}))} \approx 0.0536. \tag{3.44}$$

From (6.43) we have the capacitance parameter C_1 as

$$C_1 \approx -\frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}}\frac{1}{2}\left(\frac{V_1}{\psi+V_0}\right) \approx -\frac{1}{2}\left(\frac{V_1}{\psi+V_0}\right)\widetilde{C} \approx -2.03 \text{ pF}. \tag{3.45}$$

We can now calculate the VCO tuning constant from (6.23) as

$$K_{VCO} \approx -\frac{f_0}{V_1}\frac{C_1}{2C}\frac{\partial C}{\partial \widetilde{C}} \approx 320 \text{ kHz/V}. \tag{3.46}$$

We also want to know how large the AM-to-PM conversion is to see if it has any impact on the phase noise. We first calculate some intermediate results from (6.32)

$$\frac{\partial \alpha}{\partial \omega_0} \approx -\frac{2Q}{\omega_0} \approx -1.59 \times 10^{-7}, \tag{3.47}$$

from (6.44)

$$C_2 \approx \frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}}\left(\frac{3}{16}\left(\frac{V_1}{\psi+V_0}\right)^2\right) \approx \left(\frac{3}{16}\left(\frac{V_1}{\psi+V_0}\right)^2\right)\widetilde{C} \approx 0.205 \text{ pF}, \tag{3.48}$$

and from (6.22)

$$\frac{\partial \omega_0}{\partial \widetilde{C}} = \frac{\partial \omega_0}{\partial C}\frac{\partial C}{\partial \widetilde{C}} \approx -\frac{\omega_0}{2C}\frac{\partial C}{\partial \widetilde{C}} \approx -9.96 \times 10^{17}. \tag{3.49}$$

We can now calculate the AM-to-PM conversion by inserting (6.29) and (6.33) in (6.28) as

$$K_{AM-PM} \approx -\frac{\partial \alpha}{\partial \omega_0}\frac{\partial \omega_0}{\partial \widetilde{C}}C_2 \approx -0.033, \tag{3.50}$$

which is small enough to give negligible contribution to the phase noise.

Fourth Step: Simulation and Optimization

The oscillator is simulated together with the measurement buffers to verify the design before implementation. The current consumption is simulated to be 1.03 mA, the input-voltage amplitude, $V_{in,1}$, is 0.99 V and the output-voltage amplitude, $V_{out,1}$, is 3.39 V. The phase noise is simulated to be -127.1 dBc at 10 kHz offset and the VCO gain is 300 kHz/V.

The oscillator does not fulfill the requirement on phase noise, but is very close. If the requirement on phase noise was very important, we should design the oscillator to have some margin to the specification at the expense of additional power consumption. However, in this case we decide that the performance is satisfactory and proceed with the implementation.

Fifth Step: Implementation and Verification

As the last step in the design procedure, the oscillator was built and its performance was measured. The measured current consumption was 1.06 mA at 6.0 V supply and the oscillation frequency was 99.0 MHz before trimming of the inductance. The phase noise could not be measured because it ended

up in the noise floor for the measurement equipment used, but it could be noted that it was less than −115 dBc at 10 kHz offset. The VCO tuning constant was measured to be 120 kHz/V at a nominal tuning voltage of 5.0 V.

Summary

The performance of the JFET VCO in room temperature is summarized in Table 3.2. The calculated, simulated and measured values agree quite well. The only parameter that does not agree well is the measured tuning constant, probably due to errors in the model of the diode and/or additional parasitic capacitances, which tend to reduce the tuning constant.

Table 3.2: Performance of JFET VCO.

	spec.	calc.	sim.	meas.	unit
I_{DC}	min	1.00	1.03	1.06	mA
$\mathcal{L}$ @ 10 kHz	−127.3	−128.4	−127.1	$< -115^a$	dBc/Hz
K_{VCO}	—	320	300	120	kHz/V

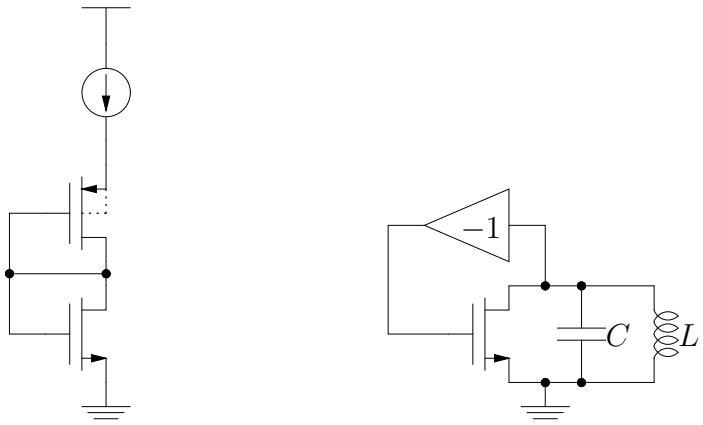
[a]Could not be measured with the measurement equipment available.

3.3.3 Integrated VCO using MOSFETs

The last design example is an integrated Voltage Controlled Oscillator (VCO). The application may be the carrier generation for a mobile communication system.

Specification

A VCO with minimum power consumption integrated in a 0.35 μm CMOS process is to be designed. The supply voltage is within the range 3.0 V to 3.7 V with a nominal value of 3.3 V. The center frequency should be 800 MHz and a tuning range of 80 MHz is wanted. The phase noise should not exceed −100 dBc at 100 kHz offset and the area must not exceed 0.1 mm^2.



(a) DC schematic. (b) AC schematic.

Figure 3.6: CMOS oscillator.

First Step: Specification Attainable?

The phase-noise performance is specified, so we can calculate what power consumption will be necessary to fulfill this requirement. From (3.1) we have

$$P_{DC,min} = \frac{k_B T}{2\mathcal{L}[\omega_m]Q^2}\frac{\omega_0^2}{\omega_m^2}, \tag{3.51}$$

which gives us a lower limit of 150 μW for the power consumption, assuming that the Q-value of the oscillator is approximately 3 (estimated using (F.11) and assuming that the inductor is implemented as two separate spiral inductors). Since the ODE probably will be in the order of -10 dB to -20 dB, we expect the power consumption, P_{DC}, to be in the range 1.5 mW to 15 mW. This power consumption is acceptable from thermal stress point of view and we may proceed with the design of the oscillator.

Second Step: Topology Selection

Since the oscillator is implemented in an integrated circuit, we choose to use a differential solution to minimize the sensitivity to noise from other circuitry on the same chip. No node voltages are allowed to exceed the supply voltage due to the rapid aging of components when the electric fields get too high. Consequently, we choose to use a complementary topology for the active part which also has the benefit of having higher transconductance per current consumption and the resulting bias scheme is shown in Figure 3.6(a).

We proceed with the choice of signal grounding. From Section 4.4.1 we have that common-gate and common-source configurations have better

phase-noise performance than common-drain and differential stage configurations. We choose to signal-ground the source in this oscillator. We choose to implement the biasing current source with a PMOS transistor since they have lower 1/f noise than NMOS transistors in this process.

We next determine the feedback network. Having a differential topology, we may choose any one of the feedback networks mentioned in Section 4.1.6. From Section 4.4.1 we have that the phase-noise performance is best when $\frac{Z_{11}}{|Z_{21}|} = 1$ for the chosen signal grounding. We choose the simplest feedback networks fulfilling our requirements – the parallel LC circuit, see Figure 3.6(b). We also choose to implement the inductor as two series connected integrated inductors to get lower sensitivity to magnetically coupled disturbances. This choice has the disadvantage of giving lower Q-value per area for the inductor. The resulting schematic is shown in Figure 3.7. The capacitor C_B performs the signal grounding of the source terminals of the PMOS transistors.

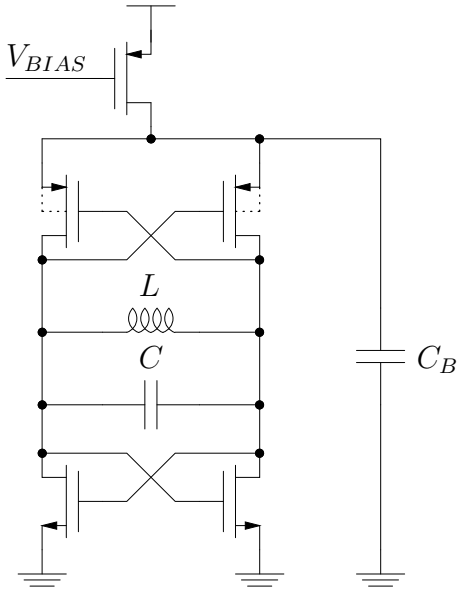


Figure 3.7: CMOS oscillator.

Since we are building a differential circuit, we need to check the common-mode stability. Using the method discussed in Section 4.2.3, we see that the equivalent common-mode circuit is simply an inverter and there is no risk of having common-mode oscillations.

Next, we design the amplitude control. To keep the design effort low, we choose to use the inherent nonlinearity of the transistors, in this case their linear regions. Consequently, no additional circuitry needs to be added.

Finally, we must implement the frequency tuning. Since we are designing in a CMOS process, we implement the varactors with MOS structures. It may be necessary to divide the tuning range into several smaller tuning ranges, depending on the requirements on the oscillator. This choice will be made later once we have the initial values for the components. The full schematic for the VCO is shown in Figure 3.8.

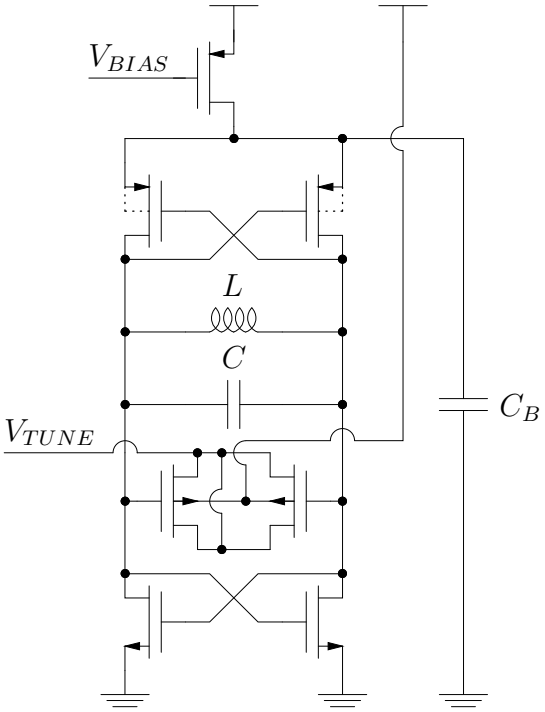


Figure 3.8: CMOS oscillator.

Third Step: Initial Component Sizing

Since the component spread is higher in integrated circuits than discrete circuits, we design with some margin – in this case for a phase noise of -103 dBc/Hz at 100 kHz offset. The fundamental power dissipated in the feedback network can be calculated from (3.3) to be

$$P_1 \approx \frac{k_B T F}{2\mathcal{L}[\omega_m] Q^2} \frac{\omega_0^2}{\omega_m^2} \approx 584\ \mu\text{W}, \tag{3.52}$$

where the noise factor, F, is given by (4.133) as

$$F \approx 1 + \gamma \tag{3.53}$$

and we have assumed that $\gamma = 1$.

The output-voltage amplitude, $V_{out,1}$, is twice the value of (4.58), which in our case is equal to the threshold voltage, V_T, which is approximately 0.6 V. The factor two comes from the differential nature of the circuit. The input impedance of the feedback network is given by

$$Z_{11} = \frac{V_{out,1}^2}{2P_1} \approx 308\ \Omega. \tag{3.54}$$

From (4.19) we have

$$Z_{11} \approx \frac{X_L^2}{R_L} = Q_L X_L = Q_L \omega_0 L, \tag{3.55}$$

where R_L is the series resistance of the inductor and Q_L is the Q-value of the inductor defined in (4.6). Solving for the inductance, L, we get 20.45 nH.

The two series-connected inductors are calculated using the expressions of Appendix F. The inductors are assumed to have octagonal shape with an outer diameter, d_{out}, of 200 μm, a turn width, w, of 6 μm, a turn spacing, s, of 2 μm, and the number of turns, n, is 10.

After the inductor design, we get an inductance, L, of 20.16 nH and a Q-value of 2.81. Assuming that the output-voltage amplitude, $V_{out,1}$, is 0.6 V, we have a fundamental power, P_1, of 631 μW. Inserting this power in (3.3), we get the phase noise as -102.78 dBc/Hz at 100 kHz offset, which still fulfills the requirement. The output-current amplitude is given by

$$I_{out,1} = \frac{V_{out,1}}{Z_{11}} = 2.105\ \text{mA}, \tag{3.56}$$

which gives the current consumption using

$$I_{out,1} = K_{FET} I_{DC} \tag{3.57}$$

as 3.508 mA assuming that $K_{FET} = 0.6$, see discussion on K_{FET} in Section 4.2.1. For a supply voltage, V_{DC}, of 3.0 V, we get a power consumption, P_{DC}, of 10.5 mW, a power efficiency, η, of 6.0%, and an ODE, Υ, of -15.2 dB. For a supply voltage of 3.7 V, we get a power consumption of 13.0 mW, a power efficiency of 4.9%, and an ODE of -16.1 dB.

We proceed with the sizing of the transistors. According to Section 4.2.3, we must have

$$V_{GT0} \leq \frac{V_{in,1}}{K_{FET}} \approx 1.0\ \text{V} \tag{3.58}$$

to guarantee start-up. We choose $V_{GT0} = 0.7$ V and get NMOS transistors of size $\frac{20\ \mu m}{0.35\ \mu m}$ and PMOS transistors of size $\frac{60\ \mu m}{0.35\ \mu m}$. The current-source PMOS transistor has then approximately 0.4 V over it when the DC supply is 3.0 V.

Next, we need to calculate the additional capacitance needed to achieve a center frequency, f_0, of 800 MHz. The total differential capacitance is found from

$$C \approx \frac{1}{\omega_0^2 L} \tag{3.59}$$

to be 1.96 pF. The parasitic capacitances between each node and ground is made up of the buffers, $C_{buf} \approx 800$ fF, the active transistors, $C_{act} \approx 130$ fF, and the inductors, $C_{ind} \approx 210$ fF. Subtracting these parasitic capacitances from the total capacitance, C, we see that an additional differential capacitance of 1.39 pF is needed.

When using integrated capacitors, we need to take the additional parasitic capacitance to the substrate, which is grounded, into account. In this technology, the parasitic capacitance is approximately 1/7 of the capacitance between the two plates. To get a total differential capacitance of 1.39 pF we can insert four capacitances with capacitance 330 fF, which gives the wanted capacitance when the additional parasitic capacitance is taken into account.

The capacitor C_B provides a low-impedance path for the higher harmonics. Choosing a capacitance of 2 pF gives an impedance of 100 Ω at 800 MHz. All bias and supply voltages are also capacitively decoupled.

Finally, we must design the frequency tuning network. We now replace some of the frequency-determining capacitance with varactors. We choose to use PMOS transistors as inversion-mode varactors since there are no dedicated varactors available in the chosen process.

We first need to calculate if we need to split the tuning range into several smaller ranges or if we can implement it as only one tuning range. The limiting factor is the AM-to-PM conversion which upconverts 1/f noise to phase noise. Assuming that the noise corner $f_{m,1/f}$ is not higher than 100 kHz in order to fulfill the phase noise specification, we can calculate the allowed AM-to-PM conversion from (3.11) as

$$|K_{AM-PM}| \approx \sqrt{\frac{4k_B T f_{m,1/f}}{(K_{1/f,f} + K_{1/f,b})\Upsilon V_{DC}}}. \tag{3.60}$$

In this process the NMOS transistors have much higher noise than the PMOS transistors and we calculate the 1/f noise constant, $K_{1/f}$, for the NMOS to be 1.8×10^{-12} A. Inserting this value in (3.60), we get that $|K_{AM-PM}|$ is approximately 0.10. We can now calculate the allowed tuning range from (6.62) to be

$$\frac{\omega_{tune}}{\omega_0} \approx \frac{\pi |K_{AM-PM}|}{2Q} \approx 0.056, \tag{3.61}$$

where we have assumed that the feedback network is fairly linear and that the amplitude limiting makes the absolute incremental large-signal loop gain much smaller than one. We see that the tuning range cannot be larger than 5.6% and we consequently need to split the tuning range into several smaller tuning ranges. The question is: How many of these smaller tuning ranges are needed? We note that each step must be smaller than the tuning range because we need some overlap. We also note that the total tuning range should be approximately 30% since we want a tuning range of 10% and we add an additional 20% to accomodate process variations and process uncertanties. The additional tuning range may be reduced if a test VCO is designed and measured upon to remove the systematic errors. We choose to make the frequency steps approximately 4% to get some overlap and still only a few frequency steps to cover the entire tuning range.

Now we size the varactor. From (6.61) and (6.21) we have

$$\frac{C_H - C_L}{C} \approx 2\frac{\omega_{tune}}{\omega_0}, \tag{3.62}$$

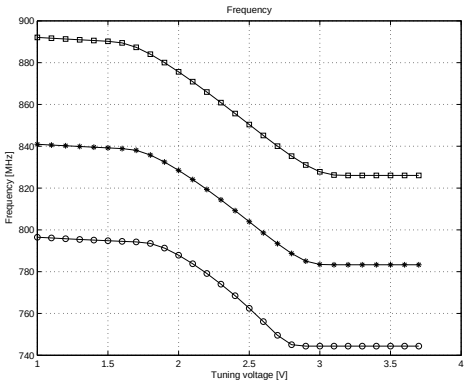
which together with the process parameters indicate that using two PMOS varactors of size $\frac{260\ \mu m}{0.5\ \mu m}$ gives the wanted tuning range. The capacitors that are used to give the frequency steps in tuning range are also implemented as PMOS varactors. Calculating the size to give nine frequency ranges and the middle range for the wanted frequency, we get varactors of size $\frac{190\ \mu m}{0.5\ \mu m}$. We also calculate the resulting maximum VCO tuning constant, K_{VCO}, from (6.23) and (6.58) to be

$$\max|K_{VCO}| \approx -\frac{\omega_0}{V_1}\frac{|C_H - C_L|}{\pi C} \approx 54 \text{ MHz/V}. \tag{3.63}$$

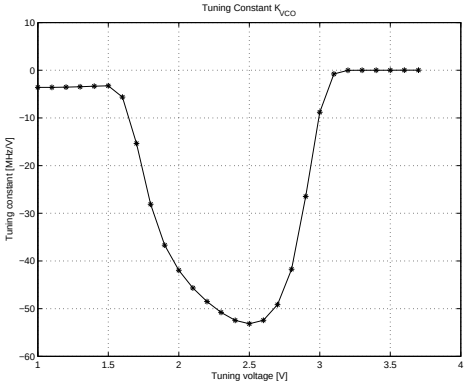
Fourth Step: Simulation and Optimization

We first simulate the oscillator without frequency tuning, that is, with integrated poly–poly capacitors. The simulated phase noise is -108.1 dBc/Hz at 100 kHz offset with a supply voltage of 3.7 V and a supply current of 3.5 mA. This simulated phase noise is much better than the specification requires and we might want to redesign the oscillator to bring the power consumption down at the expense of higher phase noise. The simulated single-sided oscillation amplitude is 0.639 V, which is close to the calculated value of 0.6 V. We choose to implement the oscillator with the values calculated above.

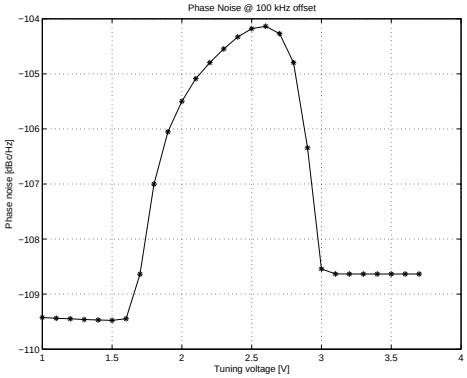
We proceed with the simulation of the VCO including the varactors. We increase the current consumption somewhat to 4.0 mA to compensate for the losses in the varactors and to guarantee operation over the entire frequency



(a) Simulated oscillation frequency as function of tuning voltage.



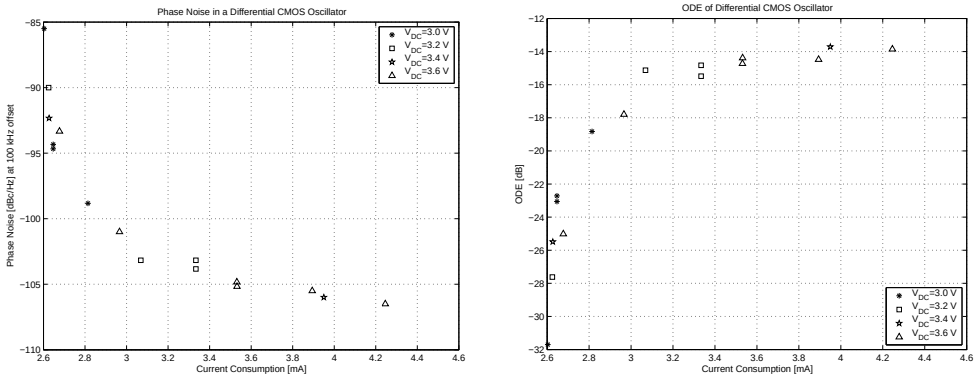
(b) Simulated tuning constant as function of tuning voltage.



(c) Simulated phase noise as function of tuning voltage.

Figure 3.9: Simulations on differential CMOS oscillator.

span. The oscillation frequency as function of tuning voltage is shown for the three center tuning bands in Figure 3.9(a). The tuning constant, K_{VCO}, for the center band is shown in Figure 3.9(b), and compared with the calculated maximum value of -54 MHz/V, we see that we have an excellent agreement. The phase noise at 100 kHz offset for the center band is shown in Figure 3.9(c) and has a maximum value of -104.1 dBc which fulfills the requirement. Noise present at the tuning voltage and switch control voltages are neglected in this simulation. The connection between AM-to-PM conversion and VCO tuning constant can clearly be seen when comparing Figure 3.9(b) and Figure 3.9(c).



(a) Measured phase noise as function of current consumption.

(b) Estimated ODE as function of current consumption.

Figure 3.10: Measurements on differential CMOS oscillator.

Fifth Step: Implementation and Verification

Only the oscillator with poly–poly capacitors has been manufactured and measured upon. The measured oscillation frequency was only 743 MHz, approximately 7% lower than the simulated value. The two main reasons for the error in frequency are the estimated inductance of the inductor and the estimated capacitances. The spread in capacitance values may also contribute.

The measured phase noise is -105 dBc/Hz at 100 kHz offset at room temperature, fulfilling the requirement with 5 dB margin. The phase noise was also measured at different current consumptions by varying the bias current. The measurement results are plotted in Figure 3.10(a). The ODE at different current consumptions are estimated, assuming that the Q-value of the oscillator is 2.81, and plotted in Figure 3.10(b). At 3.5 mA current consumption, we have an ODE of approximately -15 dB, which is close to the calculated value of -16.1 dB.

Summary

The performance in room temperature of the CMOS oscillator without frequency tuning capability is summarized in Table 3.3. The calculated, simulated and measured values differs with a few dB. The difference may be caused by the noise models in calculations and simulations, the estimated inductance and Q-value of the inductor, and the estimation of the oscillation amplitude because oscillators implemented with FETs has not as strong amplitude limiting as oscillators implemented with bipolar transistors.

Table 3.3: Performance of CMOS oscillator.

	spec.	calc.	sim.	meas.	unit
f_0	800	800	814	743	MHz
$\mathcal{L}$ @ 100 kHz	−100.0	−102.8	−108.1	−105	dBc/Hz

3.4 Discussion

The design methodology introduced in this chapter was used on three design examples, but how can we guarantee that it will work in all other cases?

Unfortunately, it is not possible to guarantee that a design methodology will always lead to a circuit that fulfills the specification if the specification set is not known when the methodology is created. If we had a closed set of specifications, we could possibly guarantee that the design methodology would always work. However, a new additional specification may conflict with one of the existing specifications, thereby the design against both these specifications may be impossible. The design methodology outlined in this chapter is flexible to encompass requirements other than those brought up here explicitly.

The proposed design methodology aims at fulfilling phase-noise requirements with minimized power consumption subject to constraints from the other requirements set by the specification and technology. Hence, if the other requirements makes the design impossible the methodology will of course fail to produce an oscillator meeting the requirements.

Chapter 4

Oscillator Topologies

In this chapter I describe the different topology choices for an oscillator and their impact on the performance of the oscillator. First, I describe different feedback networks, including frequency tuning, and different active networks. I proceed by describing different implementations for biasing of oscillators. Finally, I evaluate the phase-noise performance for each of the choices described. This chapter is meant to be used in conjunction with the preceding chapter describing the design methodology.

4.1 Feedback Network

The primary task for the feedback network is to determine the oscillation frequency. The components used in this network should have low losses to minimize the phase noise and power consumption, which precludes the usage of resistors. The components we do use are capacitors, inductors, and various electro-mechanical resonators, such as piezoelectric resonators. We first describe the characteristics of each of these components before proceeding with how these components can be used to form frequency-determining networks.

4.1.1 Capacitors

The reactance of a capacitor, C, at frequency ω is given by

$$X_C = -\frac{1}{\omega C} \tag{4.1}$$

and the derivative of the reactance with respect to the angular frequency is given by

$$\frac{\partial X_C}{\partial \omega} = \frac{1}{\omega^2 C} = -\frac{X_C}{\omega}. \tag{4.2}$$

If we assume the series resistivity, R_C, of the capacitor to be constant with frequency, the derivative of the resistance with respect to the frequency is zero. We define the Q-value of the capacitor as

$$Q_C \equiv \frac{|X_C|}{R_C}. \tag{4.3}$$

For most capacitors, the Q-value decreases for rising temperatures since the resistive losses increase with temperature while the capacitance is temperature independent.

4.1.2 Inductors

The reactance of an inductor is given by

$$X_L = \omega L \tag{4.4}$$

and the derivative of the reactance with respect to the angular frequency is given by

$$\frac{\partial X_L}{\partial \omega} = L = \frac{X_L}{\omega}. \tag{4.5}$$

If we assume the series resistivity, R_L, of the inductor to be constant with frequency, the derivative of the resistance with respect to the frequency is zero. We define the Q-value of the inductor as

$$Q_L \equiv \frac{X_L}{R_L}. \tag{4.6}$$

A real inductor has parasitic capacitances associated with it. These capacitances might contribute to the reactance at the operating frequency. When they do contribute, the derivative of the reactance is affected and we must take the capacitances into account when we calculate the Q-value for the feedback network [O, 1998].

For most inductors, the Q-value decreases for rising temperatures since the resistive losses increase with temperature while the inductance is almost temperature independent.

4.1.3 Varactors

Varactors are components with variable reactance. It could be either inductive or capacitive reactance, but only capacitive varactors are treated in this thesis.

The two most common varactors, the reverse-biased diode and the MOS structure, are described in Sections 6.5 and 6.6.

4.1.4 Crystals/Piezoelectric Resonators

Piezoelectric crystals are mechanical resonators. These resonators have excellent frequency stability and are used in many systems where a stable reference timing is needed [Parzen, 1983]. An electrical analog model of a crystal is shown in Figure 4.1. The series resistance R_1 may increase at low drive levels causing problems at start-up, especially for self-limiting oscillators which have low loop gains.

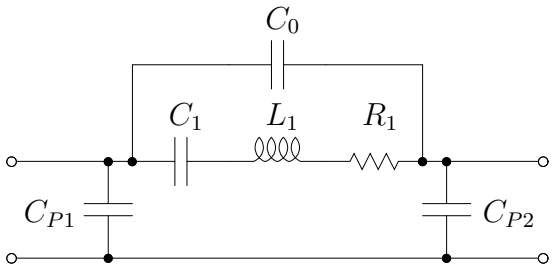


Figure 4.1: Electrical analog model of a crystal including parasitic capacitances C_{P1} and C_{P2}.

Neglecting the parasitic capacitances C_{P1} and C_{P2}, we arrive at the simplified model of Figure 4.2. Crystals actually have many modes of resonance; if we include these resonance modes in the model, we get the electrical model of Figure 4.3. An oscillator containing a crystal may be designed to oscillate at one of these higher resonance modes instead of at the fundamental mode.

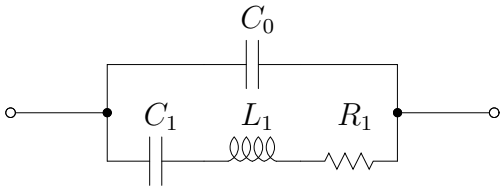


Figure 4.2: Electrical analog model of a crystal excluding parasitic capacitances.

The series Q-value of a crystal is defined as

$$Q_S \equiv \frac{1}{\omega_s C_1 R_1}, \tag{4.7}$$

where the series resonant frequency is given by

$$\omega_s = \frac{1}{\sqrt{L_1 C_1}}. \tag{4.8}$$

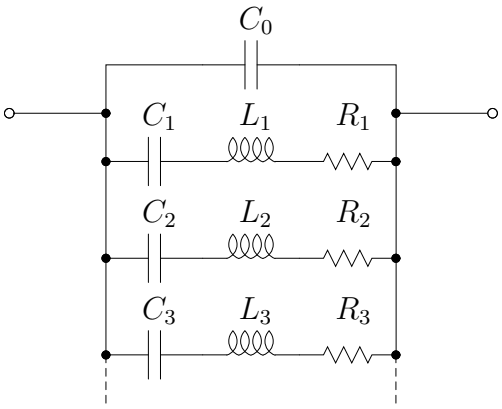


Figure 4.3: Electrical analog model of a crystal excluding parasitic capacitances. Higher order resonance modes are also included in the model.

Assuming that the oscillation frequency is $\omega_s + \omega_\Delta$, we can approximate the series reactance between the two terminals as

$$X_S \approx \frac{2}{\omega_s C_1} \frac{\omega_\Delta}{\omega_s} \tag{4.9}$$

and the series resistance can be approximated as

$$R_S \approx \frac{R_1}{\left(1 - \frac{2C_0}{C_1}\frac{\omega_\Delta}{\omega_s}\right)^2} \tag{4.10}$$

when the crystal is operating in its inductive region [Parzen, 1983]. When these approximations were derived, it was assumed that $|X_{C_1} + X_{L_1}| \gg R_1$.

The thermal noise of a crystal is caused by the resistive losses, that is, the spectral density is given by a noise voltage source in series with resistor R_1 with single-sided noise spectral density $4k_BTR_1$.

The derivative of the series reactance with respect to angular frequency around the oscillation frequency is approximately given by

$$\frac{\partial X_S}{\partial \omega} \approx \frac{2}{\omega_s^2 C_1} \approx \frac{X_S}{\omega_s}\frac{\omega_s}{\omega_\Delta}, \tag{4.11}$$

where we in the last stage used (4.9).

When a very high frequency stability is sought for a crystal oscillator, we must have a low power entering the crystal [Vittoz et al., 1988]. High input power to the crystal introduces higher harmonics in the waveform and non-linearities of the crystal become significant. Hence, the oscillation frequency changes from that of low input power to the crystal.

4.1.5 Frequency-Determining Network

The frequency-determining network, the feedback part, is described in this section. We assume that it is made up of passive inductors, capacitors and piezoelectric elements, all of which have an impedance dominated by its reactive part, *i.e.*, they have high Q-values. We choose to represent the feedback network as a two-port network described by Z-parameters. An immitance function, which is basically a one-port network, may also be represented as a two-port network. An introduction to the modeling of a two-port network using Z-parameters is found in Appendix D.

The simplest two-port transimpedance network that can represent any two-port network is shown in Figure 4.4. This implementation is called a pi type due to its graphical resemblance to the Greek letter pi (Π).

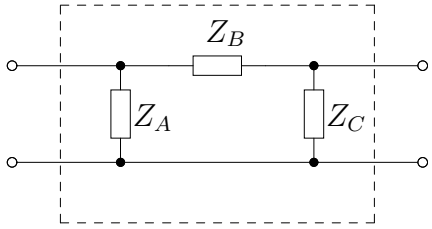


Figure 4.4: Pi two-port network with three impedances.

The Z-parameters for this type of network are given by

$$Z_{11} = \frac{Z_A(Z_B + Z_C)}{Z_A + Z_B + Z_C}, \tag{4.12}$$

$$Z_{12} = Z_{21} = \frac{Z_A Z_C}{Z_A + Z_B + Z_C}, \tag{4.13}$$

and

$$Z_{22} = \frac{(Z_A + Z_B)Z_C}{Z_A + Z_B + Z_C}. \tag{4.14}$$

We model each of the three impedances as a reactance in series with a resistance according to

$$Z_A = R_A + jX_A, \tag{4.15}$$

$$Z_B = R_B + jX_B, \tag{4.16}$$

and

$$Z_C = R_C + jX_C. \tag{4.17}$$

The new schematic is shown in Figure 4.5, where the impedances are replaced by the series combination of reactances and resistances.

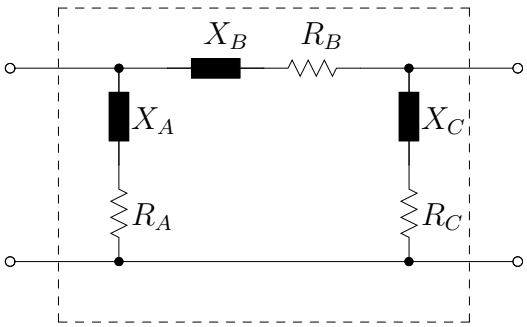


Figure 4.5: Pi two-port network where the three impedances are modeled as reactances in series with resistances.

We assume that $|X_A| \gg R_A$, $|X_B| \gg R_B$ and $|X_C| \gg R_C$. The reactances and resistances are all functions of frequency. At the oscillation frequency, f_0, we have

$$X_A + X_B + X_C \approx 0. \tag{4.18}$$

Under these assumptions, the impedance parameters can be approximated by

$$Z_{11} \approx \frac{X_A^2}{R_A + R_B + R_C}, \tag{4.19}$$

$$Z_{12} = Z_{21} \approx -\frac{X_A X_C}{R_A + R_B + R_C} \tag{4.20}$$

and

$$Z_{22} \approx \frac{X_C^2}{R_A + R_B + R_C}. \tag{4.21}$$

We also have that

$$Z_{11} Z_{22} \approx Z_{21}^2 \tag{4.22}$$

and

$$\frac{Z_{21}}{Z_{11}} \approx -\frac{X_C}{X_A}. \tag{4.23}$$

We proceed with the derivation of the Q-value of the transimpedance network. The transimpedance is given by

$$Z_{21} = \frac{R_A R_C - X_A X_C + j R_A X_C + j R_C X_A}{R_A + R_B + R_C + j X_A + j X_B + j X_C} = \frac{R_N + j X_N}{R_D + j X_D}. \tag{4.24}$$

Under the assumptions that $|X_A| \gg R_A$, $|X_B| \gg R_B$ and $|X_C| \gg R_C$, we have that $R_N \gg |X_N|$ and $R_D \gg |X_D|$. We then have

$$\alpha = \angle Z_{21} \approx \frac{X_N}{R_N} - \frac{X_D}{R_D}, \tag{4.25}$$

which gives us

$$\frac{\partial \alpha}{\partial \omega} \approx \frac{1}{R_N}\frac{\partial X_N}{\partial \omega} - \frac{X_N}{R_N^2}\frac{\partial R_N}{\partial \omega} - \frac{1}{R_D}\frac{\partial X_D}{\partial \omega} + \frac{X_D}{R_D^2}\frac{\partial R_D}{\partial \omega}. \tag{4.26}$$

For the circuits we are interested in, we can further assume that the dominant term is

$$\frac{\partial \alpha}{\partial \omega} \approx -\frac{1}{R_D}\frac{\partial X_D}{\partial \omega}, \tag{4.27}$$

which gives us the approximate Q-value as

$$Q \approx -\frac{\omega_0}{2}\frac{\partial \alpha}{\partial \omega} \approx \frac{\omega_0}{2R_D}\frac{\partial X_D}{\partial \omega} = \frac{\omega_0}{2(R_A+R_B+R_C)}\left(\frac{\partial X_A}{\partial \omega} + \frac{\partial X_B}{\partial \omega} + \frac{\partial X_C}{\partial \omega}\right). \tag{4.28}$$

Comparing (4.19), (4.20), (4.21) and (4.28) we see that a not too large increase in the resistive losses in one or several of the components will decrease Z_{11}, Z_{21}, Z_{22} and Q by approximately the same factor.

For the special case when Z_B in Figure 4.4 is equal to zero, we get the familiar parallel one-port shown in Figure 4.6; also drawn as reactances in series with resistances in Figure 4.7.

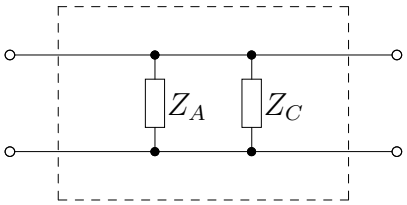


Figure 4.6: Parallel ZZ circuit.

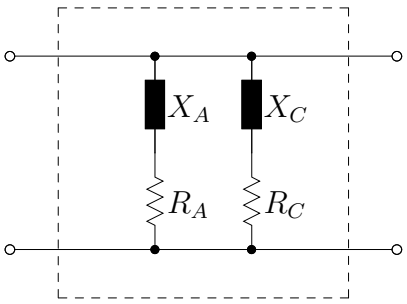


Figure 4.7: Parallel ZZ circuit where the two impedances are modeled as reactances in series with resistances.

We next discuss different implementations of the transimpedance networks using real components, that is, inductors, capacitors and crystals.

4.1.6 LC Networks

In this section, we assume that each of the three impedances Z_A, Z_B and Z_C, of Figure 4.4, is implemented by an inductor or a capacitor. Since we have that

$$X_A + X_B + X_C \approx 0 \tag{4.29}$$

we need at least one capacitor and at least one inductor for the impedances Z_A, Z_B and Z_C. The oscillation frequency can be calculated from

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.30}$$

where

$$L = L_1 + L_2 \tag{4.31}$$

in the case when two of the impedances are inductors, and

$$C = \frac{C_1 C_2}{C_1 + C_2} \tag{4.32}$$

in the case when two of the impedances are capacitors.

For inductors and capacitors we have from (4.2) and (4.5) that

$$\frac{\partial X}{\partial \omega} = \frac{|X|}{\omega} \tag{4.33}$$

and consequently the Q-value becomes

$$Q \approx \frac{1}{2} \frac{|X_A| + |X_B| + |X_C|}{R_A + R_B + R_C}, \tag{4.34}$$

using (4.33) in (4.28).

Assuming that the Q-values of the inductors are much lower than the Q-values of the capacitors we can approximate the total Q-value as

$$Q \approx \frac{\sum X_L}{\sum R_L} \tag{4.35}$$

or in the case of only one inductor with Q-value Q_L, we have $Q \approx Q_L$ using (4.6). A similar approximation can be made when the Q-values of the capacitors are much lower than the Q-values of the inductors as

$$Q \approx \frac{\sum |X_C|}{\sum R_C} \tag{4.36}$$

or in the case of only one capacitor with Q-value Q_C, we have $Q \approx Q_C$ using (4.3).

We show the simple parallel LC circuit in Figure 4.8 and summarize all possible LC pi network two-ports useful for oscillators in Figure 4.9. We also summarize the sign for the transfer function, Z_{21}, of the different impedance networks in Table 4.1. Only CLC and LCL networks are possible in a one-transistor oscillator implementation due to sign. Oscillators based on CLC and LCL feedback networks are often called Colpitts oscillators and Hartley oscillators, respectively. In most cases we prefer the CLC network over the LCL network because this latter network has more inductors and is more difficult to bias. The combination of an FET or a BJT with the CLC feedback network can be drawn according to Figure 4.10 to reveal the well-known shapes of single-transistor oscillators without bias.

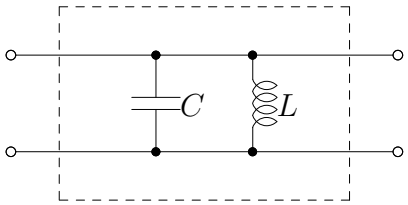
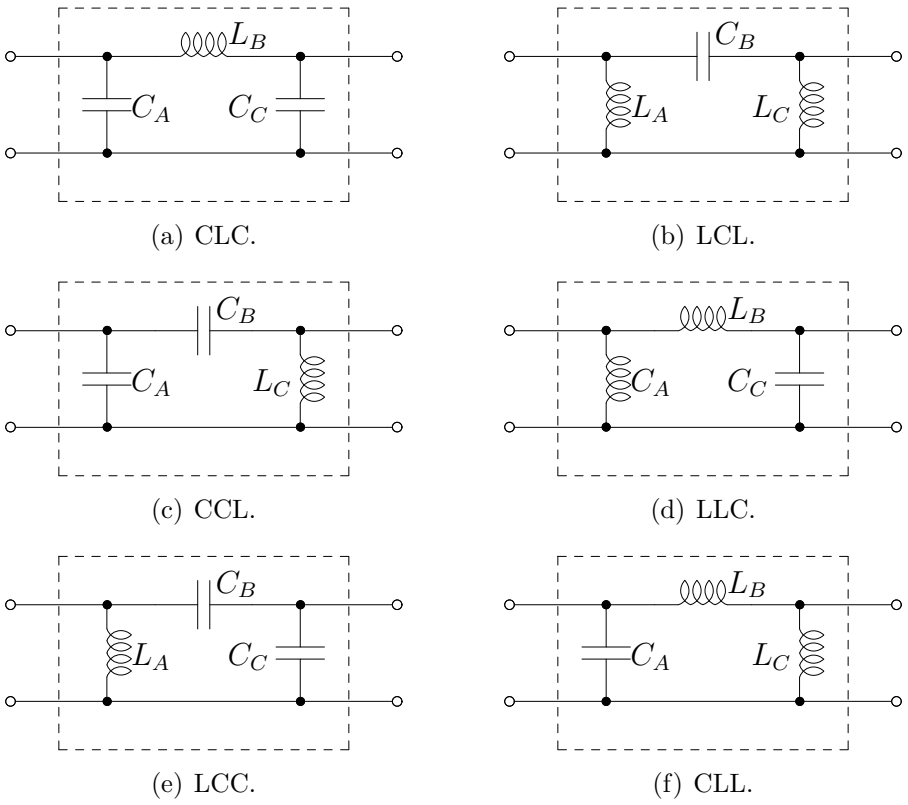


Figure 4.8: Parallel LC circuit.

Table 4.1: Sign for transfer impedance of two-port networks.

type	sign[Z_{21}]
LC	+
CLC	-
LCL	-
CCL	+
LLC	+
LCC	+
CLL	+

Sometimes it is beneficial to replace one of the components in Figure 4.9 with the series or parallel connection of two components. The reason might be that the frequency tuning is easier to implement this way. We assume that each of the components has low resistance compared to the reactance and that the series or parallel combination also have small series resistance compared to the series reactance.

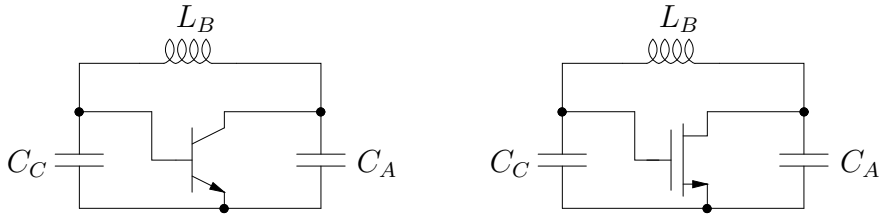


(a) CLC. (b) LCL.

(c) CCL. (d) LLC.

(e) LCC. (f) CLL.

Figure 4.9: Pi two-port networks implemented with inductors and capacitors.



(a) BJT. (b) FET.

Figure 4.10: One-transistor implementations of oscillators with CLC pi-network feedback without biasing.

Series Connected Reactances

In case of two series connected reactances, the total series reactance is simply the sum of the two reactances

$$X_S = X_1 + X_2 \tag{4.37}$$

and the total series resistance is likewise the sum of the two resistances

$$R_S = R_1 + R_2. \tag{4.38}$$

The derivative of the reactance with respect to the angular frequency is given by

$$\frac{\partial X_S}{\partial \omega} = \frac{\partial X_1}{\partial \omega} + \frac{\partial X_2}{\partial \omega}, \tag{4.39}$$

which in the case when the two reactances are capacitors and inductors is

$$\frac{\partial X_S}{\partial \omega} = \frac{|X_1| + |X_2|}{\omega}, \tag{4.40}$$

using (4.33).

Parallel Connected Reactances

In the case of two parallel connected reactances, the total series reactance is approximately given by

$$X_P \approx \frac{X_1 X_2}{X_1 + X_2} \tag{4.41}$$

and the total series resistance is approximately given by

$$R_P \approx R_1 \frac{X_2^2}{(X_1 + X_2)^2} + R_2 \frac{X_1^2}{(X_1 + X_2)^2}. \tag{4.42}$$

The derivative of the reactance with respect to the angular frequency is approximately given by

$$\frac{\partial X_P}{\partial \omega} \approx \frac{X_2 X_P}{X_1(X_1 + X_2)} \frac{\partial X_1}{\partial \omega} + \frac{X_1 X_P}{X_2(X_1 + X_2)} \frac{\partial X_2}{\partial \omega}, \tag{4.43}$$

which in the case when the two reactances are capacitors and inductors is

$$\frac{\partial X_P}{\partial \omega} \approx \frac{X_P}{\omega} \frac{X_1 \text{sign}[X_2] + X_2 \text{sign}[X_1]}{X_1 + X_2} \tag{4.44}$$

using (4.33).

In the special case where we have only one inductive reactance in the pi network and replace it with a parallel connection of an inductor and a capacitor and the Q-value of the inductor is much less than those of the capacitors, we get the approximate Q-value as $Q \approx Q_L$, where Q_L is the Q-value of the inductor.

4.1.7 Crystal Networks

We only consider crystals operating in their inductive region and use a crystal in its inductive region in the feedback network instead of an inductor. Two examples of feedback networks where an inductor has been replaced by a crystal are shown in Figure 4.11 and Figure 4.12.

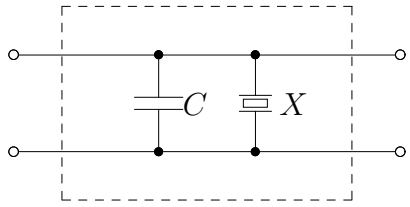


Figure 4.11: Parallel XC circuit.

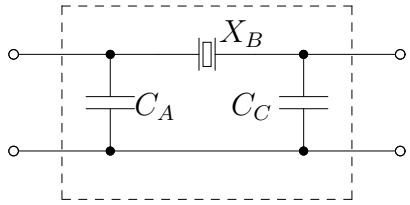


Figure 4.12: Pi-type CXC two-port network.

The shift in frequency, ω_Δ, from the series resonance frequency of the crystal, ω_s, to the oscillation frequency, ω_0, is given by

$$\omega_\Delta \approx \frac{C_1}{2(C_0 + C_L)}\omega_s, \tag{4.45}$$

where C_L is the load capacitance for the crystal which is normally given in the data sheet for the crystal for an intended oscillation frequency [Parzen, 1983].

The change in reactance with frequency is normally much higher for the crystal than for the other components. Consequently, we can approximate the Q-value for the crystal transimpedance network as

$$Q \approx \frac{X_S}{2(R_S + \sum R)}\frac{\omega_s}{\omega_\Delta}, \tag{4.46}$$

where X_S is the series reactance of the crystal, R_S is the series resistance of the crystal, and the sum in the denominator contains the series resistances for the other components. If the other components have high enough Q-values,

the resistive losses are dominated by that of the crystal and the Q-value may be approximated using (4.9) and (4.7) as

$$Q \approx \frac{X_S}{2R_S}\frac{\omega_s}{\omega_\Delta} \approx Q_S \frac{R_1}{R_S} \approx Q_S \left(\frac{C_L}{C_0 + C_L}\right)^2, \tag{4.47}$$

where Q_S is the series-resonant Q-value of the crystal and we have used

$$R_S \approx R_1 \left(\frac{C_0 + C_L}{C_L}\right)^2 \tag{4.48}$$

in the last approximation.

The other components have high enough Q-value for the crystal to dominate the total Q-value of the oscillator if

$$\frac{X_S}{\sum R} \gg \frac{\omega_\Delta}{\omega_s} Q. \tag{4.49}$$

In the case when only capacitances are used for the other components, the left-hand side of the inequality is simply the Q-value for the capacitive reactance seen by the crystal.

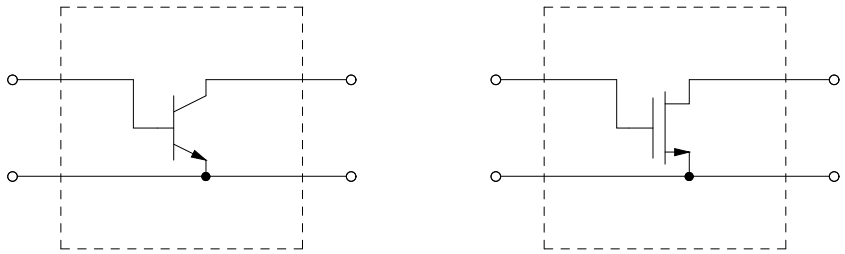
4.1.8 Frequency Tuning

Frequency tuning is accomplished by introducing electrically adjustable reactive components. The most common variable reactances, or simply varactors, are voltage-dependent capacitors, for example MOS varactors or diode varactors described in Chapter 6. Introducing voltage-dependent capacitors has the side-effect of introducing AM-to-PM conversion in the oscillator which could increase the phase noise considerably unless measures are taken to prevent this effect. When a large tuning range is sought, we must have an amplitude-regulating mechanism that prevents the AM-to-PM conversion from occurring, as discussed in Chapter 5.

Frequency tuning is physically implemented by replacing a capacitance or part of a capacitance by a varactor, or by placing a varactor in series or in parallel with an inductance in the feedback networks described above. The frequency tuning can also be implemented by placing fixed capacitances with series switches in parallel with the varactors, thereby creating several smaller frequency tuning ranges that overlap.

4.2 Active Network

The primary task for the active network is to supply the power to keep the oscillations going. The supplied power must balance the power losses in



(a) Simple BJT. (b) Simple FET.

Figure 4.13: One-transistor networks.

the lossy components in the feedback network. The components we use in this thesis to construct the active network are transistors, but for example vacuum tubes may be used as well.

The main differences between Bipolar Junction Transistors (BJTs) and Field-Effect Transistors (FETs) are the magnitude of the small-signal transconductance for a given bias current, which is much higher for the bipolar transistor, and the additional degree of freedom in the biasing of field-effect transistors. The noise factor, γ, is virtually the same with a value of $1/2$ and $\geq 2/3$ for BJTs and FETs, respectively.

Differential circuits where each of the halves acts as a single-transistor block are not described separately but in the section on one-transistor blocks. The same note applies to complementary stages where a N-type and a P-type transistor are used in parallel. Differential pairs with a high-impedance source/emitter node at high frequencies are located in the section on two-transistor networks.

4.2.1 One-Transistor Networks

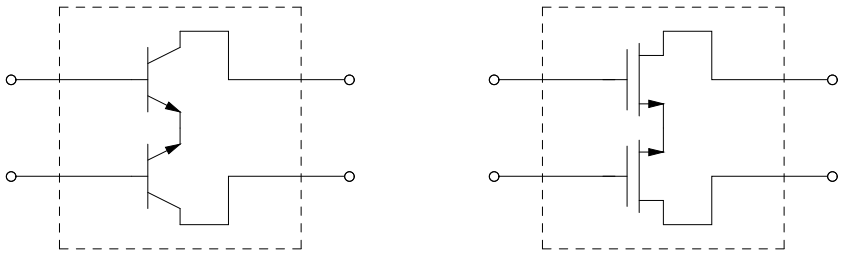
The one-transistor block is shown in Figure 4.13 where both a bipolar transistor and a field-effect transistor are shown.

Assuming that the transistor operates in Class C with an output fundamental current that is twice that of the supply current, we can approximate the power efficiency as

$$\eta \approx \frac{V_{out,1}}{V_{DC}}, \tag{4.50}$$

where V_{DC} is the supply voltage and $V_{out,1}$ is the voltage amplitude at the fundamental frequency at the output, *i.e.* $V_{ce,1}$ or $V_{ds,1}$.

An FET is difficult to operate in Class C at high frequencies since the transit frequency may be too low at the overdrive voltages needed for this



(a) Differential BJT. (b) Differential FET.

Figure 4.14: Two-transistor networks.

type of operation. Class-A or Class-B operation is often more feasible and the efficiency becomes

$$\eta \approx K_{FET}\frac{V_{out,1}}{V_{DC}}, \tag{4.51}$$

where K_{FET} usually has a value in the range $0.5 \sim 0.8$. Higher values are hard to achieve at high operation frequency and low supply voltage, and lower values give too low efficiency.

4.2.2 Two-Transistor Networks

The two-transistor block, the differential pair, is shown in Figure 4.14 where both a differential stage based on bipolar transistors and one based on field-effect transistors are included.

Assuming that the differential pair is switching completely, we can approximate the power efficiency as

$$\eta \approx \frac{V_{out,1}}{\pi V_{DC}} \leq \frac{2}{\pi} \tag{4.52}$$

where V_{DC} is the supply voltage and $V_{out,1}$ is the voltage amplitude at the fundamental frequency at the output and $V_{out,1} \leq 2V_{DC}$.

4.2.3 Biasing

Biasing provides DC voltage potentials at the terminals of the transistor or differential stages. All terminals of the transistor must have a DC potential in order for the active device to work in a predictable manner. For a bipolar transistor or a discrete FET it implies three potentials and for an integrated FET it implies four potentials that need to be supplied.

Since there are relations between voltages and currents in active devices, we can choose to supply a current instead of a voltage, which in turn decreases

the number of potentials to be supplied by one. The current that may be supplied is the source current of an FET or the base or emitter current of a BJT.

Of these different possibilities for biasing the preferred method is to supply gate/base and drain/collector voltage potentials and source/emitter current. The reason for this choice is that the variation in transconductance with process and temperature is minimized [Cherry and Hooper, 1968].

Having chosen the type of DC bias, we still need to decouple the DC and AC operation. For AC operation the impedances between the different nodes should be set by the feedback network alone, and not by the DC bias network. Since we usually want the output of the oscillator to be defined relative to the supply ground and the feedback networks we consider in this thesis do not have internal nodes, we signal ground one of the terminals of the active block.

Finally, we may need to add components to provide low impedance paths at higher frequencies to fulfill the filter hypothesis assumed during the derivations of the steady-state operation and the phase noise, that is, that the higher frequency components are filtered out by the feedback network.

A capacitor may be added when a component having low impedance at high frequencies and high impedance at low frequencies is needed. An inductor may be added when a component having high impedance at high frequencies and low impedance at low frequencies is needed. However, adding extra reactive components may increase the order of the oscillating system, *i.e.* the number of poles and zeros in the system, making it harder to analyze and guarantee operation over temperature and process variations. Therefore, it is preferable if the components in the feedback network can act as the biasing network as well.

Single-Transistor Biasing

For a single transistor, we have that the output voltage must fulfill

$$v_{OUT} \geq V_{OUT,min} \tag{4.53}$$

to stay in its active region of operation. The output voltage, v_{OUT}, is equal to v_{CE} for a BJT and equal to v_{DS} for an FET. The minimum output voltage, $V_{OUT,min}$, is the saturation voltage, approximately 0.3 V, for a BJT and the maximum overdrive voltage, $V_{GT,max}$, for an FET.

The maximum input voltage is

$$\max[v_{IN}] = V_{IN,max}, \tag{4.54}$$

where the input voltage, v_{IN}, is equal to v_{BE} for a BJT and equal to v_{GS} for an FET. The maximum input voltage is approximately 0.6∼0.7 V for a BJT and equal to the maximum gate–source voltage for a FET, given by $V_T + V_{GT,max}$, where V_T is the threshold voltage of the FET.

Assuming that each of the three nodes has a DC potential plus a fundamental AC component only, we get

$$V_{b/g,0} - V_{e/s,0} + |V_{in,1}| = V_{IN,max} \tag{4.55}$$

and

$$V_{c/d,0} - V_{e/s,0} - |V_{out,1}| \geq V_{OUT,min}, \tag{4.56}$$

which can be combined to give us

$$V_{c/d,0} - V_{b/g,0} - |V_{out,1}| - |V_{in,1}| \geq V_{OUT,min} - V_{IN,max}, \tag{4.57}$$

where $V_{IN,max} - V_{OUT,min} = V_T$ for the FET. This expression can be rewritten to give us an upper limit for the output voltage of

$$|V_{out,1}| \leq \frac{V_{c/d,0} - V_{b/g,0} + V_{IN,max} - V_{OUT,min}}{1 + \left|\frac{Z_{21}}{Z_{11}}\right|}, \tag{4.58}$$

where we have used

$$V_{in,1} = \frac{Z_{21}}{Z_{11}} V_{out,1} \tag{4.59}$$

and assumed the fraction of the transimpedances to be real and negative.

So far this derivation has been completely general. We now assume that the transistor is biased with a emitter/source current and that the base/gate and collector/drain terminals each have a fixed DC voltage. The current source is assumed to need a voltage drop of at least V_{BIAS}. We investigate the three cases when one of the three terminals provides a low impedance to supply ground for AC signals.

We begin with signal-grounding the collector/drain terminal, that is, a Common Collector (CC) or Common Drain (CD) configuration. The emitter/source potential must fulfill

$$V_{e/s,0} \geq V_{BIAS} + |V_{out,1}| \tag{4.60}$$

and consequently from (4.55) and (4.59), we get

$$V_{b/g,0} \geq |V_{out,1}| \left(1 - \left|\frac{Z_{21}}{Z_{11}}\right|\right) + V_{IN,max} + V_{BIAS}. \tag{4.61}$$

Combining this expression with (4.58), we get an upper limit for the output-voltage amplitude of

$$|V_{out,1}| \leq \frac{V_{c/d,0} - V_{OUT,min} - V_{BIAS}}{2}. \tag{4.62}$$

We proceed with signal-grounding the base/gate terminal, that is, a Common Base (CB) or Common Gate (CG) configuration. The emitter/source potential must fulfill

$$V_{e/s,0} \geq V_{BIAS} + |V_{in,1}| \tag{4.63}$$

and consequently from (4.55), we get

$$V_{b/g,0} \geq V_{IN,max} + V_{BIAS}. \tag{4.64}$$

Combining this expression with (4.58), we get an upper limit for the output-voltage amplitude of

$$|V_{out,1}| \leq \frac{V_{c/d,0} - V_{OUT,min} - V_{BIAS}}{1 + \left|\frac{Z_{21}}{Z_{11}}\right|}. \tag{4.65}$$

We finally signal-ground the emitter/source terminal, that is, a Common Emitter (CE) or Common Source (CS) configuration. The base/gate potential must fulfill

$$V_{b/g,0} \geq V_{IN,start} + V_{BIAS}, \tag{4.66}$$

where $V_{IN,start}$ is the base–emitter or gate–source voltage before oscillation has commenced. The emitter DC voltage increases once the oscillation amplitude rises. Inserting this inequality for the base potential in (4.58) and using (4.59), we get an upper limit for the output-voltage amplitude of

$$|V_{out,1}| \leq \frac{V_{c/d,0} - V_{OUT,min} - V_{BIAS} + V_{IN,max} - V_{IN,start}}{1 + \left|\frac{Z_{21}}{Z_{11}}\right|}. \tag{4.67}$$

Comparing the three cases, we see that there is not a particularly large difference in maximum oscillation amplitude. Other aspects than the oscillation amplitude usually determine which one of the three bias arrangements is the most practical to use. However, one fundamental difference between the three cases exists when a simple resistor is used as an emitter/source current source. When the base/gate or collector/drain terminals are AC grounded, the DC current decreases as the oscillation amplitude increases. When the emitter/source terminal is AC grounded, the DC current increases as the oscillation amplitude increases. Hence, the latter case is less useful than the former two cases if only a resistor is used for current biasing.

Differential Pair Biasing

A differential pair has a high-impedance middle node. This node is, however, a virtual ground for odd harmonics. The voltage in this node is lowest when the differential input is zero. We assume that the input and output common-mode DC voltages are fixed. We treat BJT and FET implementations separately since they behave somewhat differently.

We begin with BJT differential stages. The minimum DC voltage at the base of the differential pair transistors is given by

$$V_{b,0} \geq V_{BIAS} + V_{BE,0}, \tag{4.68}$$

where $V_{BE,0}$ is the base–emitter voltage of one transistor in the differential pair when $v_{IN} = 0$. Since the emitter is at virtual ground for the fundamental component and we assume that the higher harmonics are filtered out by the feedback network, we have

$$v_{B/G} \approx V_{b/g,0} + \frac{V_{in,1}}{2}\cos(\omega_0 t) \tag{4.69}$$

and

$$v_{C/D} \approx V_{c/d,0} + \frac{V_{out,1}}{2}\cos(\omega_0 t). \tag{4.70}$$

For a bipolar transistor, we have the requirement that

$$v_{CE} = v_{CB} + v_{BE} \geq V_{CE,min}, \tag{4.71}$$

where $V_{CE,min}$ is the voltage saturation limit when the base–collector diode begins to conduct current.

Inserting (4.69) and (4.70) in (4.71) and by using (4.59), we get the maximum output amplitude as

$$|V_{out,1}| \leq \frac{2}{1 + \left|\frac{Z_{21}}{Z_{11}}\right|}(V_{c,0} - V_{CE,min} - V_{b,0} + V_{BE,max}), \tag{4.72}$$

where $V_{BE,max}$ is the base–emitter voltage when one of the transistors conducts all of the tail bias current. Using (4.68), we get the maximum output amplitude as

$$|V_{out,1}| \leq \frac{2}{1 + \left|\frac{Z_{21}}{Z_{11}}\right|}(V_{c,0} - V_{CE,min} - V_{BIAS} + V_{BE,max} - V_{BE,0}). \tag{4.73}$$

For an FET differential pair, the source potential gets pushed down by the drain potential when the transistor enters its linear region. However,

the drain potential must stay somewhat over source potential, which must at least be V_{BIAS}. Thus, in order for the transistor to conduct the necessary current, we must have

$$V_{d,0} - V_{DS,min} - \frac{|V_{out,1}|}{2} \geq V_{BIAS} \tag{4.74}$$

or rewritten as

$$|V_{out,1}| \leq 2(V_{d,0} - V_{DS,min} - V_{BIAS}), \tag{4.75}$$

where $V_{DS,min}$ here is the minimum drain–source voltage needed for the transistor to conduct all of the tail current when operating in its linear region.

How to Prevent Common-Mode Oscillations

When implementing differential circuits, we also need to check the common-mode behavior. A simple way to do this is to draw an equivalent common-mode schematic, assuming that the differential and common-mode behavior does not affect each other to a high degree. If they do affect each other, which may be the case, the analysis becomes more complicated and this case is not dealt with here.

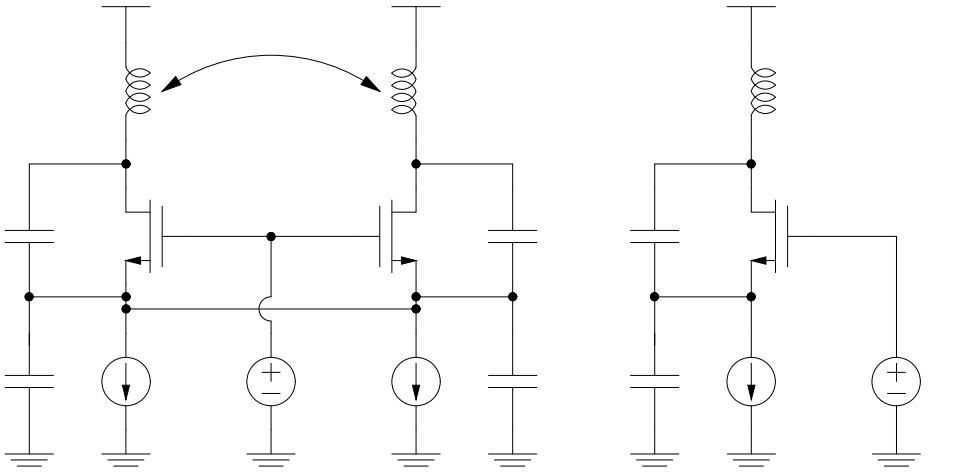
We take the differential Colpitts oscillator of Figure 4.15(a) as a first example. Drawing the equivalent common-mode schematic of Figure 4.15(b), we see that this schematic is also a Colpitts oscillator. If the mutual coupling between the two inductors is low, we have a significant common-mode inductance and the circuit may have common-mode oscillations, easily checked by calculating the small-signal loop gain.

By modifying the differential Colpitts oscillator according to Figure 4.16(a), we change the common-mode behavior but not the differential behavior. We have replaced the two lower capacitances to ground with a differential capacitance. We draw the equivalent common-mode schematic in Figure 4.16(b) and see that it is not an oscillator any more for common-mode signals.

How to Prevent Squegging

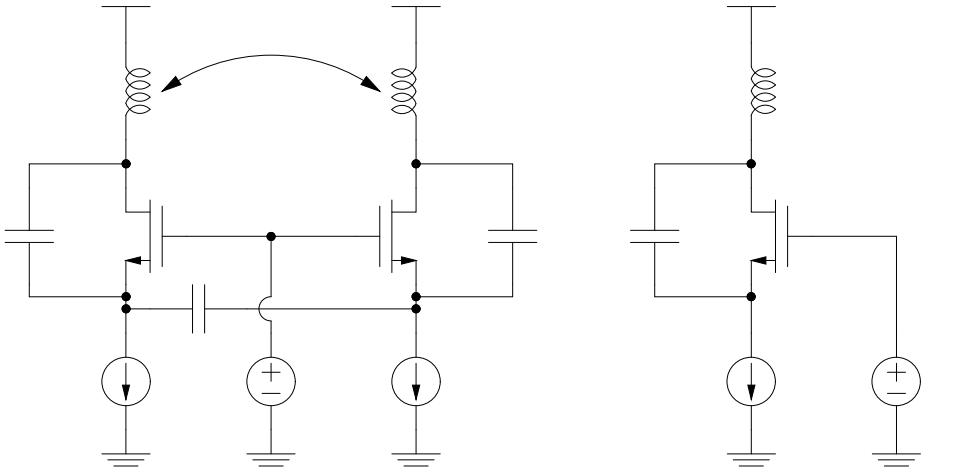
Even when no explicit amplitude control loop is present, there are still an amplitude control loop present. Since there is a feedback loop present there is a possibility for instability in the amplitude, often called squegging.

To check if there is any risk for instability in the system, we can calculate the poles of the system and verify that these are located in the left half-plane. We only check whether the system is stable around the intended operating point here, but one should also check the stability of the system



(a) Full schematic. (b) Common mode schematic.

Figure 4.15: Schematic of differential Colpitts oscillator.



(a) Full schematic. (b) Common mode schematic.

Figure 4.16: Schematic of differential Colpitts oscillator.

during start-up so the system does reach this operating point without getting into trouble.

Since we only consider the system around the operating point, we may linearize the system. The output currents of the active part are given by

$$I_{out,0}(s) = \widetilde{G}_{\Delta,00} V_{in,0}(s) + \widetilde{G}_{\Delta,01} V_{in,1}(s) \tag{4.76}$$

and

$$I_{out,1}(s) = \widetilde{G}_{\Delta,10} V_{in,0}(s) + \widetilde{G}_{\Delta,11} V_{in,1}(s), \tag{4.77}$$

where $V_{in,0}$ and $V_{in,1}$ are the low-frequency input voltage and the input-voltage amplitude, $I_{out,0}$ and $I_{out,1}$ are the low-frequency output current and output-current amplitude, and $\widetilde{G}_{\Delta,00}$, $\widetilde{G}_{\Delta,01}$, $\widetilde{G}_{\Delta,10}$ and $\widetilde{G}_{\Delta,11}$ are the incremental large-signal cross-transadmittances of the active part.

Assuming that the feedback network is almost linear, we can write the relationships between input current and output voltage of this network as

$$V_{in,0}(s) = \widetilde{H}_0(s) I_{out,0}(s) \tag{4.78}$$

and

$$V_{in,1}(s) = \widetilde{H}_1(s) I_{out,1}(s) \tag{4.79}$$

where $\widetilde{H}_0$ is the low-frequency transimpedance and $\widetilde{H}_1$ is the transfer function for the current amplitude to the voltage amplitude. The low-frequency transimpedance is given by $\widetilde{H}_0(s) = H(s)$ in the case of a linear feedback network. If the feedback transfer function, h, has two conjugate complex poles near the imaginary axis, we may approximate the transfer function for the amplitude as

$$\widetilde{H}_1(s) \approx \frac{\widetilde{H}_1}{1 + s\frac{2Q}{\omega_0}}, \tag{4.80}$$

see also Section 5.5.2. We can now analyze the stability by evaluating the system made up by (4.76), (4.77), (4.78) and (4.79).

Squegging is mostly a problem for self-limiting oscillators with low Q-value. It can often be solved by reducing the bias time constant or the coupling time constant, where the coupling time constant is the most important one. Other ways to solve the problem could be to increase the Q-value or decrease the drive voltage for the active element by making $\frac{|Z_{21}|}{Z_{11}}$ lower [Clarke and Hess, 1971]. The introduction of an explicit control loop for the oscillation amplitude may also solve the problem, see Section 5.5 for further discussion about Automatic Amplitude Control (AAC).

Start-Up

The start-up of oscillators is a non-trivial problem and is not easy to guarantee in all cases [Nguyen and Meyer, 1992]. For fairly simple feedback networks, including parasitic elements, the small-signal gain is a good indicator as to whether the oscillator could start.

A prerequisite for the oscillator to start is that the small-signal loop gain is larger than unity. Under the assumption that the feedback network is linear, this requirement becomes $|G_m| \geq |\widetilde{G}_1|$, where G_m is the small-signal transconductance of the active part and $\widetilde{G}_1$ is the large-signal transconductance of the active part.

For a BJT single-transistor implementation, we have the small-signal transconductance as

$$|G_m| = g_m \approx \frac{I_{C0}}{V_T} \tag{4.81}$$

and the large-signal transconductance as

$$|\widetilde{G}_1| = \frac{I_{c,1}}{V_{in,1}} = \frac{2I_{c,0}}{V_{in,1}}. \tag{4.82}$$

Assuming that the bias current is equal in both cases, *i.e.* $I_{c,0} = I_{C0}$, we must have $V_{in,1} \geq 2V_T$ for the oscillator to start.

For an FET single-transistor implementation, we have the small-signal transconductance as

$$|G_m| = g_m = \frac{2I_{D0}}{V_{GT0}}, \tag{4.83}$$

assuming the square-law model for the transistor, and the large-signal transconductance as

$$|\widetilde{G}_1| = \frac{I_{d,1}}{V_{in,1}} = \frac{2K_{FET}I_{d,0}}{V_{in,1}}. \tag{4.84}$$

Assuming that the bias current is equal in both cases, *i.e.* $I_{d,0} = I_{D0}$, we must have $V_{in,1} \geq K_{FET}V_{GT0}$ for the oscillator to start.

For a BJT differential pair implementation, we have the small-signal transconductance as

$$|G_m| \approx \frac{I_{DC}}{4V_T} \tag{4.85}$$

and the large-signal transconductance as

$$|\widetilde{G}_1| = \frac{|I_{out,1}|}{V_{in,1}} = \frac{2I_{DC}}{\pi V_{in,1}}. \tag{4.86}$$

Assuming that the bias current is equal in both cases, we must have $V_{in,1} \geq \frac{8}{\pi}V_T$ for the oscillator to start.

For an FET differential pair implementation, we have the small-signal transconductance as

$$|G_m| \approx \frac{I_{DC}}{2V_{GT0}} \tag{4.87}$$

and the large-signal transconductance as

$$|\widetilde{G}_1| = \frac{|I_{out,1}|}{V_{in,1}} = \frac{2I_{DC}}{\pi V_{in,1}}. \tag{4.88}$$

Assuming that the bias current is equal in both cases, we must have $V_{in,1} \geq \frac{4}{\pi}V_{GT0}$ for the oscillator to start.

It is sometimes more difficult to guarantee start-up for crystal oscillators than LC oscillators since they may have additional zeros close to the poles in the loop transfer function due to parasitics [Unkrich and Meyer, 1982].

An Automatic Amplitude Control (AAC) may be used when a short start-up time is required since it can give higher small-signal loop gain during start-up. This solution is usually used only for crystal oscillators because they have much higher Q-values and therefore much longer start-up times.

4.3 Noise from Bias Current Source

In this section, we calculate the noise contributions from simple current sources implemented with transistors. The schematics for these current sources are shown in Figure 4.17, both for implementations with a BJT and with an FET. The voltage source V_B or V_G may be another transistor implementation, as is the case when the current source is part of a current mirror, or it could be a constant voltage generator or a variable voltage, which may be the case when implementing an Automatic Amplitude Control (AAC). In any case, the bias voltage may also contribute noise which must be accounted for, but here we only consider noise coming from the transistor and from the resistor R_E or R_S.

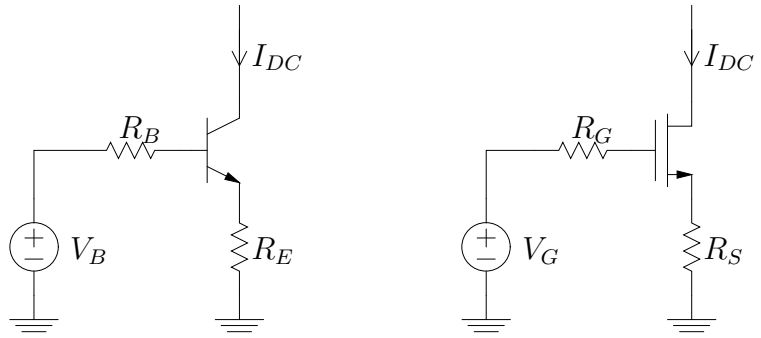
4.3.1 White Noise from Bias Current Source

Assuming that the input noise and noise from R_B and R_G are negligible, we have the noise spectral density as

$$S_b \approx 4k_BT\frac{1}{R_{E/S}} \tag{4.89}$$

when $g_mR_{E/S} \gg 1$, where g_m is the transconductance of the transistor and

$$S_b \approx 4k_BT\gamma g_m \tag{4.90}$$



(a) BJT current source. (b) FET current source.

Figure 4.17: Implementations of current source.

when R_E or R_S is negligible, and where γ is approximately 2/3 for FETs and 1/2 for BJTs.

4.3.2 1/f Noise from Bias Current Source

The bias current source may contribute with a significant amount of 1/f noise, which may be up-converted to phase noise. In this section, we calculate the noise spectral density for this 1/f noise contribution. We assume that a bias current implemented as a resistor only contributes an insignificant amount of 1/f noise, and we hence concentrate on implementations containing transistors.

BJT

For a bipolar transistor, the 1/f noise current source is located between the base and the emitter with a spectral density given in (C.18) of Appendix C as

$$\overline{i_b^2} = \frac{K_{1/f}}{f} I_B \approx \frac{K_{1/f}}{f} \frac{I_{DC}}{\beta}, \tag{4.91}$$

where $K_{1/f}$ is a noise constant, I_B is the base current, I_{DC} is the bias current, and β is the current amplification factor of the transistor.

We now have the 1/f noise from the bias current source as

$$S_b(f) \approx \left(\frac{g_m R_B + g_m R_E}{1 + g_m R_E + g_m R_B \frac{1}{\beta}} \right)^2 \frac{K_{1/f}}{f} \frac{I_{DC}}{\beta}, \tag{4.92}$$

assuming that $\beta \gg 1$, and where g_m is the transconductance of the transistor.

Writing this expression as

$$S_b(f) = \frac{K_{1/f,b} I_{DC}}{f} \tag{4.93}$$

gives the constant $K_{1/f,b}$ as

$$K_{1/f,b} \approx \left(\frac{g_m R_B + g_m R_E}{1 + g_m R_E + g_m R_B \frac{1}{\beta}} \right)^2 \frac{K_{1/f}}{\beta}. \tag{4.94}$$

Since the resistance of R_B usually is non-negligible and we have inserted a resistor R_E, we have

$$\frac{K_{1/f}}{\beta} < K_{1/f,b} < \beta K_{1/f}. \tag{4.95}$$

FET

For an FET, the 1/f noise current source is located between the drain and the source with a spectral density given in (C.32) of Appendix C as

$$\overline{i_d^2} = \frac{K_{1/f}}{f} I_{DC}, \tag{4.96}$$

where $K_{1/f}$ is a noise constant and I_{DC} is the bias source current.

We now have the 1/f noise from the bias current source as

$$S_b(f) = \left(\frac{1}{1 + g_m R_S} \right)^2 \frac{K_{1/f}}{f} I_{DC}, \tag{4.97}$$

where g_m is the transconductance of the transistor. Writing this expression as

$$S_b(f) = \frac{K_{1/f,b} I_{DC}}{f}, \tag{4.98}$$

we get the constant $K_{1/f,b}$ as

$$K_{1/f,b} = \left(\frac{1}{1 + g_m R_S} \right)^2 K_{1/f}. \tag{4.99}$$

If R_S is not present, we get

$$K_{1/f,b} = K_{1/f} \tag{4.100}$$

and if $g_m R_S \gg 1$, we get

$$K_{1/f,b} \approx \frac{K_{1/f}}{g_m^2 R_S^2}. \tag{4.101}$$

4.4 Phase-Noise Performance

To determine which bias arrangement gives the lowest phase noise due to white noise in the components, we evaluate the maximum achievable Oscillator Design Efficiency (ODE), Υ, derived in Section 3.2.1 to be

$$\Upsilon = \frac{\eta}{F}, \tag{4.102}$$

where η is the power efficiency and F is the noise factor. We evaluate the ODE both for oscillators based on FETs and for oscillators based on BJTs. Oscillators using both types of transistors are not considered here, but could easily be evaluated using the same method.

In this section, we assume that the Z-parameters are real in order to simplify the expressions. We further note that Z_{11} and Z_{22} must be positive since the input and output resistances for a passive network are positive.

4.4.1 FET

The minimum voltage needed for the operation of the bias current generator of Section 4.3 is given by

$$V_{BIAS} = V_{GT}, \tag{4.103}$$

where V_{GT} is the overdrive voltage of the bias transistor, and where we have assumed that $R_S = 0$. The approximate noise spectral density of the bias current generator is given in (4.90) as

$$S_b \approx 4k_B T \gamma g_{m,b}, \tag{4.104}$$

where the transconductance of the transistor, $g_{m,b}$, is given by

$$g_{m,b} = \frac{2I_{DC}}{V_{GT}}, \tag{4.105}$$

where I_{DC} is the bias current, and where we have assumed that the transistor can be described by the square-law model.

The output-voltage amplitude of the active part is given by

$$V_{out,1} = Z_{11} I_{out,1}, \tag{4.106}$$

where the output-current amplitude, $I_{out,1}$, for a single transistor is approximately given by

$$|I_{out,1}| \approx 2K_{FET} I_{DC}, \tag{4.107}$$

where K_{FET} is defined in Section 4.2.1. Hence, we get the minimum voltage needed for the current bias generator as

$$V_{BIAS} \approx \frac{1}{K_{FET} g_{m,b} Z_{11}} V_{out,1} \tag{4.108}$$

by combining (4.103), (4.105), (4.106) and (4.107).

For a differential pair, the output-current amplitude is approximately given as

$$|I_{out,1}| \approx \frac{2}{\pi} I_{DC} \tag{4.109}$$

when the differential pair is completely switching. Consequently, the minimum voltage needed for the bias current generator is given by

$$V_{BIAS} \approx \frac{\pi}{g_{m,b} Z_{11}} |V_{out,1}|. \tag{4.110}$$

For an oscillator based on a single FET, we have the approximate power efficiency from (4.51) as

$$\eta \approx K_{FET} \frac{|V_{out,1}|}{V_{DC}}, \tag{4.111}$$

where K_{FET} has a value less than unity.

For an oscillator based on FETs operating as a differential stage, the approximate power efficiency is given by (4.52) as

$$\eta \approx \frac{|V_{out,1}|}{\pi V_{DC}}. \tag{4.112}$$

The noise factor of oscillators where the AM-to-PM conversion is negligible is given in Section 7.2.6 as

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + K_1 K_2, \tag{4.113}$$

where

$$K_1 = \gamma g_{m,b} Z_{11} \tag{4.114}$$

and

$$K_2 = \begin{cases} 2K_{im} \leq \frac{1}{4} & \text{differential pair tail bias} \\ 1 & \text{bias at output} \\ \frac{Z_{22}^2}{Z_{21}^2} & \text{bias at input} \end{cases} \tag{4.115}$$

We assume below that $K_{im} \approx \frac{1}{8}$ and that

$$\frac{Z_{22}^2}{Z_{21}^2} \approx \frac{Z_{21}^2}{Z_{11}^2}, \tag{4.116}$$

which is the case for an oscillator designed to have low phase noise due to white noise.

Signal-Grounded Drain

For a signal-grounded drain, also termed Common Drain (CD), we have the maximum output-voltage amplitude from (4.62) as

$$|V_{out,1}| \approx \frac{V_{d,0} - V_{DS,min} - V_{BIAS}}{2}. \tag{4.117}$$

Inserting the expression for minimum voltage for supply current biasing in (4.108), we get the maximum output-voltage amplitude as

$$|V_{out,1}| \approx \frac{V_{d,0} - V_{DS,min}}{2 + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}}. \tag{4.118}$$

Inserting this expression in (4.111), we get the power efficiency as

$$\eta \approx \frac{K_{FET}(V_{d,0} - V_{DS,min})}{V_{DC}\left(2 + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}\right)}. \tag{4.119}$$

The noise factor for a signal-grounded drain is given from (4.113) as

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \gamma g_{m,b} Z_{11}. \tag{4.120}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{K_{FET}(V_{d,0} - V_{DS,min})}{V_{DC}\left(2 + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}\right)\left(1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \gamma g_{m,b} Z_{11}\right)}, \tag{4.121}$$

which can be rewritten as

$$\Upsilon \approx \frac{V_{d,0} - V_{DS,min}}{V_{DC}} \Upsilon_{norm}, \tag{4.122}$$

where

$$\Upsilon_{norm} = \frac{K_{FET}}{\left(2 + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}\right)\left(1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \gamma g_{m,b} Z_{11}\right)} \tag{4.123}$$

is the oscillator design efficiency we would get if the overdrive voltages of the transistors in the active part were negligible compared to the supply voltage and the drain potential is equal to the supply voltage. This ODE is plotted in Figure 4.18(a) for $\gamma = 1$ with $K_{FET} = 0.6$ as function of $\frac{Z_{11}}{|Z_{21}|}$ with $g_{m,b} Z_{11} = 1.29$ and as function of $g_{m,b} Z_{11}$ with $\frac{Z_{11}}{|Z_{21}|} = 1$.

Signal-Grounded Gate

For a signal-grounded gate, also termed Common Gate (CG), we have the maximum output-voltage amplitude from (4.65) as

$$|V_{out,1}| \approx \frac{V_{d,0} - V_{DS,min} - V_{BIAS}}{1 + \frac{|Z_{21}|}{Z_{11}}}. \tag{4.124}$$

Inserting the expression for minimum voltage for supply current biasing in (4.108), we get the maximum output-voltage amplitude as

$$|V_{out,1}| \approx \frac{V_{d,0} - V_{DS,min}}{1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}}. \tag{4.125}$$

Inserting this expression in (4.111), we get the power efficiency as

$$\eta \approx \frac{K_{FET}(V_{d,0} - V_{DS,min})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}\right)}. \tag{4.126}$$

The noise factor for a signal-grounded gate is given from (4.113) as

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \frac{Z_{21}^2}{Z_{11}^2} \gamma g_{m,b} Z_{11}. \tag{4.127}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{K_{FET}(V_{d,0} - V_{DS,min})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}\right)\left(1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \frac{Z_{21}^2}{Z_{11}^2} \gamma g_{m,b} Z_{11}\right)}, \tag{4.128}$$

which can be rewritten as

$$\Upsilon \approx \frac{V_{d,0} - V_{DS,min}}{V_{DC}} \Upsilon_{norm}, \tag{4.129}$$

where

$$\Upsilon_{norm} = \frac{K_{FET}}{\left(1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{K_{FET}} \frac{1}{g_{m,b} Z_{11}}\right)\left(1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \frac{Z_{21}^2}{Z_{11}^2} \gamma g_{m,b} Z_{11}\right)} \tag{4.130}$$

is the oscillator design efficiency we would get if the overdrive voltages of the transistors in the active part were negligible compared to the supply voltage and the drain potential is equal to the supply voltage. This ODE is plotted in Figure 4.18(b) for $\gamma = 1$ with $K_{FET} = 0.6$ as function of $\frac{Z_{11}}{|Z_{21}|}$ with $g_{m,b} Z_{11} = 2.60$ and as function of $g_{m,b} Z_{11}$ with $\frac{Z_{11}}{|Z_{21}|} = 5.42$.

Signal-Grounded Source

For a signal-grounded source, also termed Common Source (CS), we have the maximum output-voltage amplitude from (4.67) as

$$|V_{out,1}| \approx \frac{V_{d,0} - V_{DS,min} - V_{BIAS} + V_{GS,max} - V_{GS,start}}{1 + \frac{|Z_{21}|}{Z_{11}}}. \tag{4.131}$$

Since the noise source is short-circuited through the signal ground at the source terminal, there is no trade-off between noise and voltage drop over the bias current generator. Inserting this expression in (4.111), we get the power efficiency as

$$\eta \approx \frac{K_{FET}(V_{d,0} - V_{DS,min} - V_{BIAS} + V_{GS,max} - V_{GS,start})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}}\right)}. \tag{4.132}$$

The noise factor for a signal-grounded source is given from (4.113) as

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|}. \tag{4.133}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{K_{FET}(V_{d,0} - V_{DS,min} - V_{BIAS} + V_{GS,max} - V_{GS,start})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}}\right)\left(1 + \gamma\frac{Z_{11}}{|Z_{21}|}\right)}, \tag{4.134}$$

which can be rewritten as

$$\Upsilon \approx \frac{V_{d,0} - V_{DS,min} - V_{BIAS} + V_{GS,max} - V_{GS,start}}{V_{DC}}\Upsilon_{norm}, \tag{4.135}$$

where

$$\Upsilon_{norm} = \frac{K_{FET}}{\left(1 + \frac{|Z_{21}|}{Z_{11}}\right)\left(1 + \gamma\frac{Z_{11}}{|Z_{21}|}\right)} \tag{4.136}$$

is the oscillator design efficiency we would get if the overdrive voltages of the transistors in the active part were negligible compared to the supply voltage and the drain potential is equal to the supply voltage. This ODE is plotted in Figure 4.18(c) for $\gamma = 1$ with $K_{FET} = 0.6$ as function of $\frac{Z_{11}}{|Z_{21}|}$. We have the maximum ODE when $\frac{Z_{11}}{|Z_{21}|} = 1$.

Differential Pair

For a differential pair, we have the maximum output-voltage amplitude from (4.75) as

$$|V_{out,1}| \approx 2(V_{d,0} - V_{DS,min} - V_{BIAS}). \tag{4.137}$$

Inserting the expression for minimum voltage for supply current biasing in (4.110), we get the maximum output-voltage amplitude as

$$|V_{out,1}| \approx \frac{2(V_{d,0} - V_{DS,min})}{1 + 2\pi\frac{1}{g_{m,b}Z_{11}}}. \tag{4.138}$$

Inserting this expression in (4.112), we get the power efficiency as

$$\eta \approx \frac{2(V_{d,0} - V_{DS,min})}{\pi V_{DC}\left(1 + 2\pi\frac{1}{g_{m,b}Z_{11}}\right)}. \tag{4.139}$$

The noise factor for a differential stage is given from (4.113) as

$$F \approx 1 + \gamma\frac{Z_{11}}{|Z_{21}|} + \frac{1}{4}\gamma g_{m,b}Z_{11}. \tag{4.140}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{2(V_{d,0} - V_{DS,min})}{\pi V_{DC}\left(1 + 2\pi\frac{1}{g_{m,b}Z_{11}}\right)\left(1 + \gamma\frac{Z_{11}}{|Z_{21}|} + \frac{1}{4}\gamma g_{m,b}Z_{11}\right)}, \tag{4.141}$$

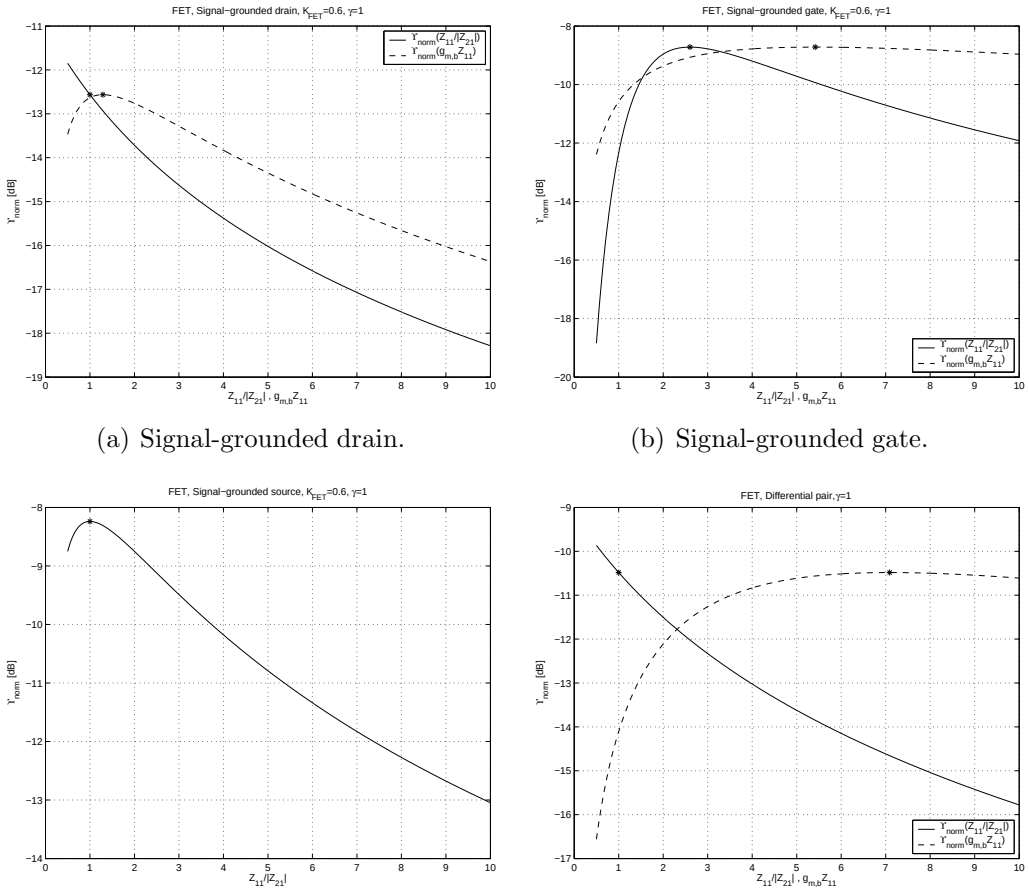
which can be rewritten as

$$\Upsilon \approx \frac{V_{d,0} - V_{DS,min}}{V_{DC}}\Upsilon_{norm}, \tag{4.142}$$

where

$$\Upsilon_{norm} = \frac{2}{\pi\left(1 + 2\pi\frac{1}{g_{m,b}Z_{11}}\right)\left(1 + \gamma\frac{Z_{11}}{|Z_{21}|} + \frac{1}{4}\gamma g_{m,b}Z_{11}\right)} \tag{4.143}$$

is the oscillator design efficiency we would get if the overdrive voltages of the transistors in the active part were negligible compared to the supply voltage and the drain potential is equal to the supply voltage. This ODE is plotted in Figure 4.18(d) for $\gamma = 1$ as function of $\frac{Z_{11}}{|Z_{21}|}$ with $g_{m,b}Z_{11} = 7.09$ and as function of $g_{m,b}Z_{11}$ with $\frac{Z_{11}}{|Z_{21}|} = 1$.



(a) Signal-grounded drain.

(b) Signal-grounded gate.

(c) Signal-grounded source.

(d) Differential stage.

Figure 4.18: Oscillator design efficiency for FET active network.

4.4.2 BJT

The minimum voltage needed for the bias current generator of Section 4.3 is given by

$$V_{BIAS} = R_E I_{DC} + V_{CE,min}, \tag{4.144}$$

where $V_{CE,min}$ is the minimum collector-emitter voltage needed for operation in the active region of the transistor. The approximate noise spectral density of the bias current generator is given in (4.89) as

$$S_b \approx 4k_B T \frac{1}{R_E}. \tag{4.145}$$

The output-voltage amplitude of the active part is given by

$$V_{out,1} = Z_{11} I_{out,1}, \tag{4.146}$$

where the output current, $I_{out,1}$, for a transistor operating in Class C is given by

$$|I_{out,1}| \approx 2I_{DC}. \tag{4.147}$$

Consequently, the minimum voltage needed for the current bias generator is given by

$$V_{BIAS} \approx \frac{R_E}{2Z_{11}} |V_{out,1}| + V_{CE,min}, \tag{4.148}$$

by combining (4.144), (4.146) and (4.147).

For a differential pair, the output current is approximately given as

$$|I_{out,1}| \approx \frac{2}{\pi} I_{DC} \tag{4.149}$$

when the differential pair is completely switching. Hence, the minimum voltage needed for the bias current generator is given by

$$V_{BIAS} \approx \frac{\pi R_E}{2Z_{11}} |V_{out,1}| + V_{CE,min}. \tag{4.150}$$

For an oscillator based on a single BJT, we have the approximate power efficiency from (4.50) as

$$\eta \approx \frac{|V_{out,1}|}{V_{DC}}. \tag{4.151}$$

For an oscillator based on BJTs operating as a differential stage, the approximate power efficiency is given by (4.52) as

$$\eta \approx \frac{|V_{out,1}|}{\pi V_{DC}}. \tag{4.152}$$

The noise factor of oscillators where the AM-to-PM conversion is negligible is given in Section 7.2.6 as

$$F \approx 1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + K_1 K_2, \tag{4.153}$$

where

$$K_1 = \frac{Z_{11}}{R_E} \tag{4.154}$$

and

$$K_2 = \begin{cases} 2K_{im} \leq \frac{1}{4} & \text{differential pair tail bias} \\ 1 & \text{bias at output} \\ \frac{Z_{22}^2}{Z_{21}^2} & \text{bias at input} \end{cases} \tag{4.155}$$

We assume below that $K_{im} \approx \frac{1}{8}$ and that

$$\frac{Z_{22}^2}{Z_{21}^2} \approx \frac{Z_{21}^2}{Z_{11}^2}, \tag{4.156}$$

which is the case for an oscillator designed to have low phase noise due to white noise.

Signal-Grounded Collector

For a signal-grounded collector, also termed Common Collector (CC), we have the maximum output-voltage amplitude from (4.62) as

$$|V_{out,1}| \approx \frac{V_{c,0} - V_{CE,min} - V_{BIAS}}{2}. \tag{4.157}$$

Inserting the expression for minimum voltage for supply current biasing in (4.148), we get the maximum output-voltage amplitude as

$$|V_{out,1}| \approx \frac{V_{c,0} - V_{CE,min} - V_{CE,min}}{2 + \frac{1}{2}\frac{R_E}{Z_{11}}}. \tag{4.158}$$

Inserting this expression in (4.151), we get the power efficiency as

$$\eta \approx \frac{(V_{c,0} - V_{CE,min} - V_{CE,min})}{V_{DC}\left(2 + \frac{1}{2}\frac{R_E}{Z_{11}}\right)}. \tag{4.159}$$

The noise factor for a signal-grounded collector is given from (4.153) as

$$F \approx 1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{Z_{11}}{R_E}. \tag{4.160}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{(V_{c,0} - V_{CE,min} - V_{CE,min})}{V_{DC}\left(2 + \frac{1}{2}\frac{R_E}{Z_{11}}\right)\left(1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{Z_{11}}{R_E}\right)}, \tag{4.161}$$

which can be rewritten as

$$\Upsilon \approx \frac{V_{c,0} - V_{CE,min} - V_{CE,min}}{V_{DC}}\Upsilon_{norm}, \tag{4.162}$$

where

$$\Upsilon_{norm} = \frac{1}{\left(2 + \frac{1}{2}\frac{R_E}{Z_{11}}\right)\left(1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{Z_{11}}{R_E}\right)} \tag{4.163}$$

is the oscillator design efficiency we would get if the saturation voltages of the transistors were negligible compared to the supply voltage and the collector potential is equal to the supply voltage. This ODE is plotted in Figure 4.19(a) as function of $\frac{Z_{11}}{|Z_{21}|}$ with $\frac{Z_{11}}{R_E} = 0.61$ and as function of $\frac{Z_{11}}{R_E}$ with $\frac{Z_{11}}{|Z_{21}|} = 1$.

Signal-Grounded Base

For a signal-grounded base, also termed Common Base (CB), we have the maximum output-voltage amplitude from (4.65) as

$$|V_{out,1}| \approx \frac{V_{c,0} - V_{CE,min} - V_{BIAS}}{1 + \frac{|Z_{21}|}{Z_{11}}}. \tag{4.164}$$

Inserting the expression for minimum voltage for supply current biasing in (4.148), we get the maximum output-voltage amplitude as

$$|V_{out,1}| \approx \frac{V_{c,0} - V_{CE,min} - V_{CE,min}}{1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{2}\frac{R_E}{Z_{11}}}. \tag{4.165}$$

Inserting this expression in (4.151), we get the power efficiency as

$$\eta \approx \frac{(V_{c,0} - V_{CE,min} - V_{CE,min})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{2}\frac{R_E}{Z_{11}}\right)}. \tag{4.166}$$

The noise factor for a signal-grounded base is given from (4.153) as

$$F \approx 1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{Z_{21}^2}{Z_{11}^2}\frac{Z_{11}}{R_E}. \tag{4.167}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{(V_{c,0} - V_{CE,min} - V_{CE,min})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{2}\frac{R_E}{Z_{11}}\right)\left(1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{Z_{21}^2}{Z_{11}^2}\frac{Z_{11}}{R_E}\right)}, \tag{4.168}$$

which can be rewritten as

$$\Upsilon \approx \frac{V_{c,0} - V_{CE,min} - V_{CE,min}}{V_{DC}}\Upsilon_{norm}, \tag{4.169}$$

where

$$\Upsilon_{norm} = \frac{1}{\left(1 + \frac{|Z_{21}|}{Z_{11}} + \frac{1}{2}\frac{R_E}{Z_{11}}\right)\left(1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{Z_{21}^2}{Z_{11}^2}\frac{Z_{11}}{R_E}\right)} \tag{4.170}$$

is the oscillator design efficiency we would get if the saturation voltages of the transistors were negligible compared to the supply voltage and the collector potential is equal to the supply voltage. This ODE is plotted in Figure 4.19(b) as function of $\frac{Z_{11}}{|Z_{21}|}$ with $\frac{Z_{11}}{R_E} = 2.44$ and as function of $\frac{Z_{11}}{R_E}$ with $\frac{Z_{11}}{|Z_{21}|} = 2.66$.

Signal-Grounded Emitter

For a signal-grounded emitter, also termed Common Emitter (CE), we have the maximum output-voltage amplitude from (4.67) as

$$|V_{out,1}| \approx \frac{V_{c,0} - V_{CE,min} - V_{BIAS} + V_{BE,max} - V_{BE,start}}{1 + \frac{|Z_{21}|}{Z_{11}}}. \tag{4.171}$$

Since the noise source is short-circuited through the signal ground at the emitter terminal, there is no trade-off between noise and voltage drop over the bias current generator. Inserting this expression in (4.151), we get the power efficiency as

$$\eta \approx \frac{(V_{c,0} - V_{CE,min} - V_{BIAS} + V_{BE,max} - V_{BE,start})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}}\right)}. \tag{4.172}$$

The noise factor for a signal-grounded emitter is given from (4.153) as

$$F \approx 1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|}. \tag{4.173}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{(V_{c,0} - V_{CE,min} - V_{BIAS} + V_{BE,max} - V_{BE,start})}{V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}}\right)\left(1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|}\right)}, \tag{4.174}$$

which can be rewritten as

$$\Upsilon \approx \frac{V_{c,0} - V_{CE,min} - V_{BIAS} + V_{BE,max} - V_{BE,start}}{V_{DC}}\Upsilon_{norm}, \tag{4.175}$$

where

$$\Upsilon_{norm} = \frac{1}{\left(1 + \frac{|Z_{21}|}{Z_{11}}\right)\left(1 + \gamma\frac{Z_{11}}{|Z_{21}|}\right)} \tag{4.176}$$

is the oscillator design efficiency we would get if the saturation voltages of the transistors were negligible compared to the supply voltage and the collector potential is equal to the supply voltage. This ODE is plotted in Figure 4.19(c) as function of $\frac{Z_{11}}{|Z_{21}|}$. The maximum ODE is achieved when $\frac{Z_{11}}{|Z_{21}|} = 1.41$.

Differential Pair

For a differential pair, we have the maximum output-voltage amplitude from (4.73) as

$$|V_{out,1}| \approx \frac{2(V_{c,0} - V_{CE,min} - V_{BIAS} + V_{BE,max} - V_{BE,0})}{1 + \frac{|Z_{21}|}{Z_{11}}}. \tag{4.177}$$

Inserting the expression for minimum voltage for supply current biasing in (4.150), we get the maximum output-voltage amplitude as

$$|V_{out,1}| \approx \frac{2(V_{c,0} - V_{CE,min} - V_{CE,min} + V_{BE,max} - V_{BE,0})}{1 + \frac{|Z_{21}|}{Z_{11}} + \pi\frac{R_E}{Z_{11}}}. \tag{4.178}$$

Inserting this expression in (4.152), we get the power efficiency as

$$\eta \approx \frac{2(V_{c,0} - V_{CE,min} - V_{CE,min} + V_{BE,max} - V_{BE,0})}{\pi V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}} + \pi\frac{R_E}{Z_{11}}\right)}. \tag{4.179}$$

The noise factor for a differential stage is given from (4.153) as

$$F \approx 1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{1}{4}\frac{Z_{11}}{R_E}. \tag{4.180}$$

Inserting the expression for the power efficiency and the expression for the noise factor in (4.102), we get the oscillator design efficiency as

$$\Upsilon \approx \frac{2(V_{c,0} - V_{CE,min} - V_{CE,min} + V_{BE,max} - V_{BE,0})}{\pi V_{DC}\left(1 + \frac{|Z_{21}|}{Z_{11}} + \pi\frac{R_E}{Z_{11}}\right)\left(1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{1}{4}\frac{Z_{11}}{R_E}\right)}, \tag{4.181}$$

which can be rewritten as

$$\Upsilon \approx \frac{(V_{c,0} - V_{CE,min} - V_{CE,min} + V_{BE,max} - V_{BE,0})}{V_{DC}}\Upsilon_{norm}, \tag{4.182}$$

where

$$\Upsilon_{norm} = \frac{2}{\pi\left(1 + \frac{|Z_{21}|}{Z_{11}} + \pi\frac{R_E}{Z_{11}}\right)\left(1 + \frac{1}{2}\frac{Z_{11}}{|Z_{21}|} + \frac{1}{4}\frac{Z_{11}}{R_E}\right)} \tag{4.183}$$

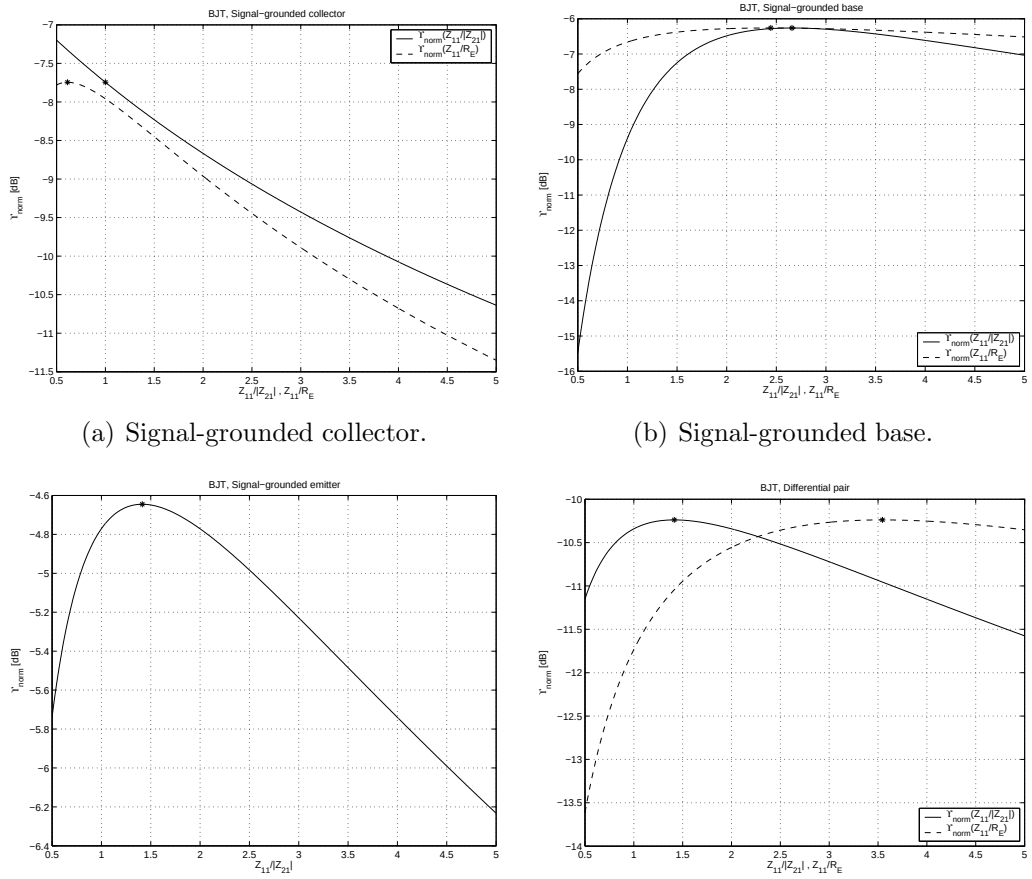
is the oscillator design efficiency we would get if the saturation voltages of the transistors were negligible compared to the supply voltage and the collector potential is equal to the supply voltage. This ODE is plotted in Figure 4.19(d) as function of $\frac{Z_{11}}{|Z_{21}|}$ with $\frac{Z_{11}}{R_E} = 3.54$ and as function of $\frac{Z_{11}}{R_E}$ with $\frac{Z_{11}}{|Z_{21}|} = 1.41$.

4.4.3 Summary

The maximum values for the ODE Υ_{norm} are summarized in Table 4.2 for different biasing options. For the FET, we assume that $K_{FET} = 0.6$ and $\gamma = 1$. In all cases, we assume that there is no filtering of noise coming from the biasing transistor. We also assume that $\frac{Z_{11}}{|Z_{21}|} \geq 1$ and that the current source gives a constant current during the entire oscillation period.

Table 4.2: Summary of optimum phase noise.

Signal-grounded	FET [dB]	BJT [dB]
Drain/Collector	−12.6	−7.7
Gate/Base	−8.7	−6.3
Source/Emitter	−8.2	−4.6
Differential stage	−10.5	−10.2



(a) Signal-grounded collector.

(b) Signal-grounded base.

(c) Signal-grounded emitter.

(d) Differential stage.

Figure 4.19: Oscillator design efficiency for BJT active network.

Chapter 5

Amplitude Control

Most practical oscillators employ some type of amplitude control to keep the oscillation voltage amplitude constant over manufacturing variations, temperature variations, and aging. This chapter describes various techniques to achieve such amplitude control and their characteristics, such as their impact on phase noise.

5.1 Introduction

The different amplitude controls can be grouped into the four categories listed below:

- Temperature-sensitive resistor
- Diode clamping
- Nonlinearity in the active network
- Automatic amplitude control

The former two methods affect the feedback network; they lower the oscillation amplitude by introducing additional losses in order to bring the amplitude down to a predefined value. The latter two methods lower the output current from the active part when the oscillation amplitude exceeds the predefined value. The first and last methods use a dynamic nonlinearity while the other methods use a static nonlinearity to control the oscillation amplitude.

We assume the feedback network to be designed such that a limitation of the voltage amplitude between two nodes will limit the voltage amplitude

between any two nodes. This assumption implies that the transimpedance, Z_{21}, of the feedback network must be proportional to its input impedance, Z_{11}. We also assume that the input impedance to the feedback network, Z_{11}, is resistive and proportional to the Q-value of the feedback network.

From Chapter 7 we have the phase noise at a frequency offset, ω_m, due to white noise sources as

$$\mathcal{L}[\omega_m] \approx \frac{k_B T F Z_{11}}{V_{out,1}^2 Q^2} \frac{\omega_0^2}{\omega_m^2}, \tag{5.1}$$

where k_B is the Boltzmann constant, T is the temperature, Q is the Q-value of the oscillator, ω_0 is the oscillation frequency, $V_{out,1}$ is the voltage amplitude at the output of the active part, and F is the noise factor given by

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + K_1 K_2 + K_{AM-PM}^2 \left(1 + \gamma |\widetilde{G}_{\Delta,1}^{(I)}| Z_{11} + K_1 K_3\right), \tag{5.2}$$

where K_{AM-PM} is the AM-to-PM conversion, Z_{11} and Z_{21} are the input impedance and transimpedance of the feedback network at the oscillation frequency, $\widetilde{G}_{\Delta,1}^{(I)}$ is the incremental large-signal transconductance of the amplifying part of the active part, γ is a noise constant depending on the transistor type used, and K_1, K_2 and K_3 are bias-dependent expressions given in Section 7.2.6.

As derived in Section 8.4, we have the AM-to-PM conversion as

$$K_{AM-PM} = \frac{|Y_1| \widetilde{H}_{\Delta,1}^{(I)} \left(\frac{\partial \alpha}{\partial |X_1|} + \frac{\partial \zeta}{\partial |X_1|}\right)}{1 - \widetilde{F}_{\Delta,1}^{(I)} \widetilde{H}_{\Delta,1}^{(I)}}, \tag{5.3}$$

where Y_1 is the fundamental output-current amplitude of the active part, X_1 is the fundamental input-voltage amplitude to the active part, α and ζ are the phase shifts of the feedback and active parts, respectively, and $\widetilde{F}_{\Delta,1}^{(I)}$ and $\widetilde{H}_{\Delta,1}^{(I)}$ are the incremental large-signal gains of the active network and of the feedback network, respectively.

The parts of the expression for the phase noise mainly affected by the amplitude control are Q, Z_{11}, Z_{21}, $\widetilde{F}_{\Delta,1}^{(I)}$ and $\widetilde{H}_{\Delta,1}^{(I)}$. The remainder of this chapter is dedicated to the four methods of amplitude control and their impact on these parts.

5.2 Limiting Using Temperature-Sensitive Resistor

A temperature-sensitive resistor is a component with a resistance that increases or decreases with temperature. The power loss in this component

will increase its own temperature which in turn increases or decreases the resistance and lowers the oscillation amplitude by introducing additional losses. The change in resistance is determined by the average power loss with a time delay equal to the thermal time constant. Hence, the nonlinearity is dynamic and not static.

The relatively high thermal time constant for such a component means that it cannot keep up with fast amplitude variations, which in turn means that it does not decrease the AM-to-PM conversion. However, the resistor might be very linear and as such could be used when high spectral purity is needed, *i.e.*, when low power at higher harmonics is sought.

For this type of limiting we have that $\widetilde{H}_{\Delta,1}^{(I)} \approx \widetilde{H}_1$, $\widetilde{F}_{\Delta,1}^{(I)}$ is not affected, and Q and Z_{11} are lowered to bring the oscillation amplitude down.

An example of an implementation of a self-regulating temperature-sensitive resistor is a light bulb. The resistance of the filament increases with its own temperature.

5.2.1 Phase-Noise Contribution

The single-sided current-noise spectral density of the temperature-sensitive resistor is simply

$$\overline{i^2} = 4k_B T_R R, \tag{5.4}$$

where R is the resistance and T_R is the operating temperature of the resistor.

In addition to the increase in phase noise due to the decrease in the Q-value, we have inserted a noisy component operating at a higher temperature and consequently contributing extra noise. If the Q-value of the feedback network is dominated by the temperature-sensitive resistor, we can approximate the noise factor as

$$F \approx \frac{T_R}{T} + \gamma\frac{Z_{11}}{|Z_{21}|} + K_1K_2 + K_{AM-PM}^2\left(\frac{T_R}{T} + \gamma|\widetilde{G}_{\Delta,1}^{(I)}|Z_{11} + K_1K_3\right), \tag{5.5}$$

where T is the temperature of the oscillator, excluding the temperature-sensitive resistor.

5.3 Diode Limiting

By inserting a diode between two nodes in the feedback network, we limit the voltage amplitude between these two nodes. A diode has an exponential relationship between voltage and current. Hence, an increase in current through the diode will only increase the voltage over the diode by a small

amount. The diode is a static nonlinearity reacting momentarily to a change in voltage amplitude.

Diode limiting makes $\widetilde{H}_{\Delta,1} \ll \widetilde{H}_1$. Consequently, the upconversion of white noise to phase noise due to the AM-to-PM conversion diminishes. The incremental large-signal gain in the active part, $\widetilde{F}^{(I)}_{\Delta,1}$, is not affected since the diode is inserted in the feedback network, and Q and Z_{11} are lowered to bring the oscillation amplitude down.

When diodes are inserted in the feedback network, we call it explicit diode limiting, and when the inherent diode of a bipolar transistor is used, we call it base–collector diode limiting. The base–collector diode limiting works in the same way as the explicit diode limiting, but uses the inherent base–collector diode of the bipolar transistor. Hence, the voltage swing between collector and base is limited such that the collector potential is not lower than one built-in diode potential below the base potential, where the built-in potential for a silicon diode is approximately 0.6∼0.7 V in room temperature.

Often diodes conducting currents in different directions are connected in parallel when a fully differential solution is designed. Otherwise, a direct current will flow between the two nodes preventing the nodes to act fully differentially.

5.3.1 Phase-Noise Contribution

From Section 7.2.4, we have that the phase-noise contribution of a diode is half that of the corresponding resistor with equal large-signal conductance. Hence, we approximate the noise factor, F, as

$$F \approx K_D + \gamma \frac{Z_{11}}{|Z_{21}|} + K_1 K_2, \tag{5.6}$$

where K_D ranges from unity when the diode limiting does not affect the Q-value to 1/2 when the Q-value is dominated by the amplitude limiting diodes.

The diode limiting affects the phase noise in several ways: by lowering the Q-value and the input impedance of the feedback network, and by its own contribution to the phase noise. The total phase noise may, however, decrease compared to the case without the amplitude regulation since the AM-to-PM conversion decreases.

5.4 Limiting Using Nonlinearity in the Active Network

The nonlinearity of the active component we discuss in this section is the linear region of the field-effect transistor. Inherent limiting in bipolar transistors is discussed in Section 5.3.

The type of limiting discussed in this section makes $\widetilde{H}_{\Delta,1} \ll \widetilde{H}_1$ in a way similar to that of diode limiting. Consequently, the upconversion of white noise to phase noise due to the AM-to-PM conversion diminishes. However, the limiting using the linear region of FETs is not as strong as that of diode limiting since the I–V characteristics is less nonlinear. We also have that $\widetilde{F}^{(I)}_{\Delta,1}$ is not affected, and Q and Z_{11} are lowered to bring the oscillation amplitude down.

5.4.1 Phase-Noise Contribution

When the drain potential comes close to that of the source terminal, the transistor enters its linear region and the drain current decreases. However, the spectral density of the drain-current noise does not decrease when the transistor enters the linear region as discussed in Appendix C.3. Assuming that the noise constant of the transistor, γ, is equal in the active and linear regions, we get the approximate noise factor as

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + K_1 K_2, \tag{5.7}$$

assuming that the limiting is strong enough to make the phase-noise contribution from the AM-to-PM conversion negligible.

5.4.2 Differential Pair Current Source

Another way of achieving amplitude limiting using the active component occurs when the voltage headroom for the current source goes down for part of the oscillation period, thus decreasing the average bias current and thereby the oscillation amplitude.

Since the potential in the middle node of a differential pair decreases when one of the transistors turns off, the current gain, A_i, from the bias current to the differential output is zero and the noise factor is still equal to

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + K_1 K_2, \tag{5.8}$$

where K_1 is taken from when the bias current source has maximum output current.

5.5 Automatic Amplitude Control

An Automatic Amplitude Control (AAC) measures the oscillation amplitude and adjusts the voltage or current to the oscillator core to adjust the oscillation amplitude to a predefined value.

The main advantage of an AAC compared to the self-limiting amplitude control is that we can have a high loop gain in the oscillator during start-up to reduce the start-up time while not introducing significant losses in the oscillator core; any additional losses cause extra phase noise.

The additional circuitry does, however, consume additional power and contribute noise, some of which is converted into phase noise. We also have to check for stability in the amplitude control loop.

The principle block diagram for the AAC in the time domain is shown in Figure 5.1. The additional block, d, measures the oscillation amplitude, X_1, and controls the gain of the active part, g, via control signal W_0 to achieve the desired oscillation amplitude.

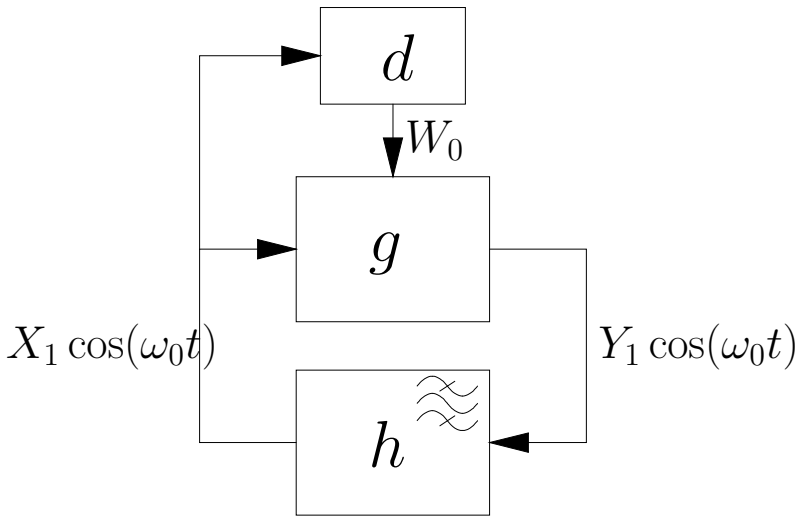


Figure 5.1: Feedback.

We can model the same functionality in the frequency domain instead which is done in Figure 5.2.

A large amplitude loop gain makes $|\widetilde{F}_{\Delta,1}\widetilde{H}_{\Delta,1}| \gg 1$ and consequently the AM-to-PM conversion decreases. Because the loop gain is high only within the amplitude control loop bandwidth, the AM-to-PM conversion is decreased only within this bandwidth. We also have that $\widetilde{H}^{(I)}_{\Delta,1} \approx \widetilde{H}_1$, and Q and Z_{11} are not significantly affected.

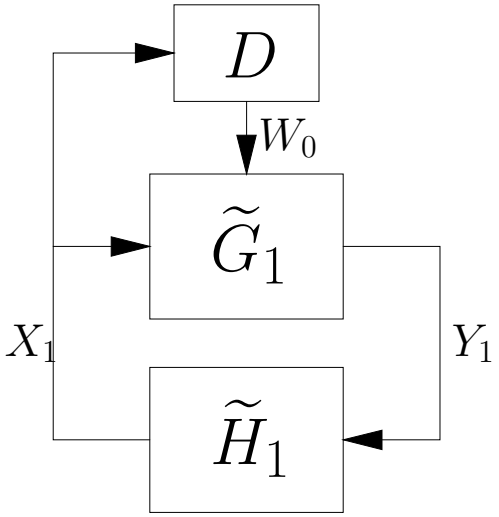


Figure 5.2: Feedback.

5.5.1 Amplitude Control Loop Stability

The task of guaranteeing stability in the amplitude control loop is a job for control theory. As long as we only consider stability around the intended operational point, linear theory will suffice. However, we must also guarantee that the oscillator reaches this operation point during start-up. See also the section about squegging in Section 4.2.3.

5.5.2 Transfer Function for the Feedback Network

The feedback network can be replaced with an equivalent transfer function for the amplitude [Clarke and Hess, 1971]. If the feedback transfer function, h, has two conjugate complex poles near the imaginary axis, the equivalent transfer function X_1/W_0 has one dominant pole approximately given by

$$\omega_p \approx \frac{\omega_0}{2Q}. \tag{5.9}$$

Depending on the feedback network, we may also have additional poles and zeros in this equivalent transfer function that are significant for the stability.

5.5.3 Amplitude Detector

The amplitude detector should cause negligible loading of the feedback network, not to reduce the Q-value of the oscillator. We also need to consider

the additional poles and zeros introduced in the amplitude control loop due to the amplitude detector.

An amplitude detector needs to have at least one nonlinear component, which could for example be a diode or a transistor, since amplitude detection is a nonlinear operation.

Different types of amplitude detectors exist; for example a peak detector only measures the peaks of the waveform while the average amplitude detector measures the average of the rectified waveform. These two types of amplitude detectors are described next.

Average Amplitude Detector

The average amplitude detector rectifies the waveform and measures the average of this rectified waveform. An example of an implementation of such a circuit is shown in Figure 5.3.

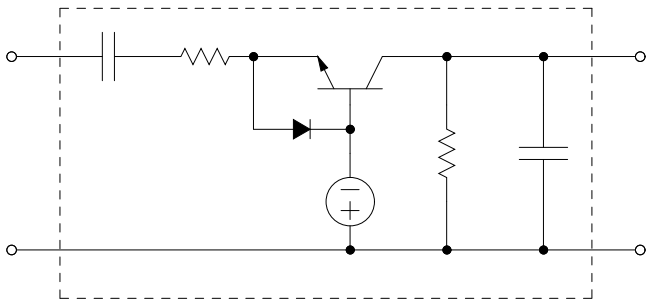


Figure 5.3: Average amplitude detector.

Peak Detector

The peak detector measures the waveform peaks only. An example of a peak detector implementation is shown in Figure 5.4.

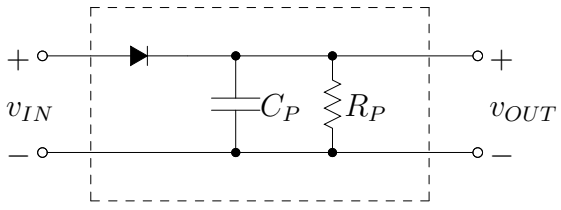


Figure 5.4: Peak detector.

We now investigate the input impedance of the peak detector in order to calculate the loading it has on the oscillator core. The input voltage to the

peak detector is approximated as

$$v_{IN}(t) \approx V_{in,0} + V_{in,1}\cos(\omega_0 t), \tag{5.10}$$

where the first term is the input DC voltage and the second term the input AC voltage. The average diode current can now be calculated as

$$I_{d,0} = \frac{v_{OUT}}{R_P}, \tag{5.11}$$

where v_{OUT} is the output voltage. Since the diode is only conducting current at the input voltage peaks, the current can be approximated as an impulse train and consequently the fundamental component is given, according to Appendix C, as

$$I_{d,1} \approx 2I_{d,0}. \tag{5.12}$$

We next calculate the output voltage of the peak detector, which is approximately given by

$$v_{OUT} \approx V_{in,0} + V_{in,1} - V_D, \tag{5.13}$$

where V_D is the voltage drop over the diode when conducting current. Combining (5.11), (5.12) and (5.13), we get the equivalent large-signal resistance for the fundamental component as

$$\widetilde{R} \approx \frac{V_{in,1}}{I_{d,1}} \approx \frac{R_P}{2}\frac{V_{in,1}}{V_{in,0} + V_{in,1} - V_D}. \tag{5.14}$$

Replacing the diode with a transistor multiplies the input large-signal resistance with the transistor current amplifying factor, β, since only a fraction of the resistor current is supplied by the base current.

5.5.4 Control Amplifier

The output signal of the amplitude detector is compared to a reference signal, the error is amplified, and the output is feed as a current or voltage to the bias circuitry of the active part of the oscillator. It is assumed that the reader is familiar with the design of amplifiers so we do not discuss it further here. This matter is also the subject of many textbooks.

5.5.5 Phase-Noise Contribution

All noise sources discussed above can be referred to the control signal, w. We can also assume that the noise is of low-pass character since the amplitude control-loop transfer function is of low-pass character.

Expressions for the additional phase noise due to these noise sources are given under filtered current bias in Section 7.2.5. We see that this additional noise is mainly a problem when we have high AM-to-PM conversion in the oscillator core.

The study of phase noise of oscillators employing AAC has been conducted in specific cases [Zanchi et al., 2001].

5.6 Summary

The impact different types of amplitude control have on various oscillator parameters are summarized in Table 5.1.

Table 5.1: Summary of different types of amplitude control.

Method	Q	$\lvert\widetilde{F}^{(I)}_{\Delta,1}\rvert$	$\lvert\widetilde{H}^{(I)}_{\Delta,1}\rvert$	$\lvert K_{AM-PM}\rvert$
Temperature-sensitive resistor	$\Downarrow$	$=$	$=$	$=$
Diode clamping	$\Downarrow$	$=$	$\Downarrow$	$\Downarrow$
Nonlinearity in the active component	$\Downarrow$	$=$	$\Downarrow$	$\Downarrow$
Automatic amplitude control	$=$	$\Uparrow$	$=$	$\Downarrow$

Which type of amplitude control to use in a particular case depends on the oscillator specification. Degrading the Q-value increases the phase noise due to white noise sources. A high value for $|K_{AM-PM}|$ makes the oscillator susceptible to phase noise due to 1/f noise sources. These two effects must be weighed against the complexity introduced by methods that minimize the phase noise at the expense of additional circuitry.

Chapter 6

Frequency Tuning

The tuning characteristics for Voltage Controlled Oscillators (VCOs) are calculated in this chapter and the effect of having a nonlinear capacitor in the feedback network on the phase noise of an oscillator is investigated. I also summarize the properties of the two most common types of varactors, diode varactors and MOS varactors, and evaluate their effect on the oscillator phase noise. Here, I only consider the case where one side of the varactor is signal grounded.

6.1 Introduction

Many oscillators employ frequency tuning of some kind. The input signal to the oscillator is either a voltage, in case of a Voltage Controlled Oscillator (VCO), or a current, in case of a Current Controlled Oscillator (CCO).

The most common method for tuning the frequency of an LC oscillator is to use nonlinear capacitors in the frequency-determining network to change the frequency. By adjusting the control voltage over these capacitors, the capacitance changes and thereby also the oscillation frequency. The expressions for the large-signal capacitance and frequency-tuning characteristics derived in this chapter have been derived earlier using a similar method [Hegazi and Abidi, 2003].

The two most common types of varactors, diode varactors and MOS varactors, are treated in this chapter and their properties are evaluated. We show that the type of varactor nonlinearity affects the phase noise in addition to determining the frequency-tuning characteristics. Increasing demands on phase noise and tuning range has rendered this effect important and substantial research has been devoted to this area recently [Rogers et al., 2000,

Levantino et al., 2002].

6.2 Large-Signal Capacitance

In this section we calculate the large-signal capacitance for a nonlinear varactor. The varactor has a voltage-dependent small-signal capacitance, c, given by

$$c(v) \equiv \frac{\partial q(v)}{\partial v}, \tag{6.1}$$

where q is the charge on the varactor.

We assume that the voltage over the varactor, v, is approximately a DC value V_0 plus a sinusoid with amplitude V_1 according to

$$v(t) = V_0 + V_1 \cos(\omega_0 t), \tag{6.2}$$

where V_0 is used to tune the large-signal capacitance and where the voltage amplitude, V_1, is assumed to be positive. We can write the small-signal capacitance as function of time as a Fourier series according to

$$c(t) = \sum_{n=0}^{\infty} C_n \cos(\omega_0 t), \tag{6.3}$$

where the capacitance parameters are given by

$$C_n = \frac{\varepsilon_n}{2\pi} \int_{-\pi}^{\pi} c(V_0 + V_1 \cos(\theta)) \cos(n\theta) d\theta, \tag{6.4}$$

where ε_n is the Neumann factor equal to 1 when $n = 0$ and equal to 2 when $n \geq 1$.

A similar series expansion can be performed for the current as function of time as

$$i(t) = \sum_{n=0}^{\infty} -I_n \sin(\omega_0 t). \tag{6.5}$$

The current as function of time can also be written as

$$i(t) = \frac{\partial q}{\partial t} = \frac{\partial q}{\partial v}\frac{\partial v}{\partial t} = c(v)\frac{\partial v}{\partial t}, \tag{6.6}$$

where we have

$$\frac{\partial v}{\partial t} = -V_1 \omega_0 \sin(\omega_0 t) \tag{6.7}$$

by taking the derivative of (6.2) with respect to time.

Inserting (6.3) and (6.7) in (6.6) and equalizing with (6.5), we can identify the fundamental frequency component of the capacitor current, I_1, as

$$I_1 = \omega_0 C_0 V_1 - \frac{1}{2}\omega_0 C_2 V_1. \tag{6.8}$$

The relationship between the fundamental current and voltage amplitudes is defined as

$$I_1 \equiv \omega_0 \widetilde{C} V_1, \tag{6.9}$$

where $\widetilde{C}$ is the large-signal capacitance, which is a function of the voltage amplitude V_1.

We now derive the large-signal capacitance as a function of the large-signal capacitance amplitudes by equalizing (6.8) and (6.9) to get

$$\widetilde{C} = C_0 - \frac{1}{2}C_2. \tag{6.10}$$

6.3 Frequency-Tuning Characteristics

To calculate the change in oscillation frequency as function of the tuning voltage, we first need to calculate the change in capacitance as function of the tuning voltage.

We first write the charge on the capacitor as a Fourier series according to

$$q(t) = \sum_{n=0}^{\infty} Q_n \cos(n\omega_0 t), \tag{6.11}$$

where

$$Q_n = \frac{\varepsilon_n}{2\pi} \int_{-\pi}^{\pi} q(V_0 + V_1 \cos(\theta)) \cos(n\theta) d\theta, \tag{6.12}$$

where ε_n is the Neumann factor equal to 1 when $n = 0$ and equal to 2 when $n \geq 1$.

Taking the derivative of (6.11) with respect to time, we get the current as

$$i(t) = \frac{\partial q(t)}{\partial t} = \sum_{n=0}^{\infty} -n\omega_0 Q_n \sin(n\omega_0 t). \tag{6.13}$$

Equating this expression for the current with the one of (6.5), we get the current amplitude components as

$$I_n = n\omega_0 Q_n. \tag{6.14}$$

Using (6.9) and (6.14), we can write the large-signal capacitance as

$$\widetilde{C} = \frac{Q_1}{V_1}. \tag{6.15}$$

We can now calculate the change in the large-signal capacitance, $\widetilde{C}$, as a function of the tuning voltage, V_0, as

$$\frac{\partial \widetilde{C}}{\partial V_0} = \frac{1}{V_1}\frac{\partial Q_1}{\partial V_0} = \frac{1}{V_1}\frac{1}{\pi}\int_{-\pi}^{\pi} c(V_0 + V_1\cos(\theta))\cos(\theta)d\theta = \frac{C_1}{V_1} \tag{6.16}$$

using (6.15) and the fundamental component for the charge, given by

$$Q_1 = \frac{1}{\pi}\int_{-\pi}^{\pi} q(V_0 + V_1\cos(\theta))\cos(\theta)d\theta. \tag{6.17}$$

The VCO tuning constant, K_{VCO}, is given by

$$K_{VCO} = \frac{\partial \omega_0}{\partial V_0} = \frac{\partial \omega_0}{\partial \widetilde{C}}\frac{\partial \widetilde{C}}{\partial V_0} = \frac{\partial \omega_0}{\partial \widetilde{C}}\frac{C_1}{V_1}, \tag{6.18}$$

where we in the last equality used the result of (6.16).

The maximum tuning constant is given by

$$\max|K_{VCO}| = \left|\frac{\partial \omega_0}{\partial \widetilde{C}}\right| \frac{\max|C_1|}{V_1}, \tag{6.19}$$

assuming that the voltage amplitude, V_1, over the capacitor is fairly constant over the tuning range.

For simple oscillators, we can usually calculate the oscillation frequency as

$$\omega_0 \approx \frac{1}{\sqrt{LC}}, \tag{6.20}$$

where the capacitance, C, and the inductance, L, can be made up of several components. The change in oscillation frequency with respect to a change in capacitance is then given by

$$\frac{\partial \omega_0}{\partial C} \approx -\frac{1}{2C\sqrt{LC}} \approx -\frac{\omega_0}{2C}. \tag{6.21}$$

Usually, the tuning capacitance, $\widetilde{C}$, is only a fraction of the total frequency-determining capacitance, C. The change in oscillation frequency with respect to a change in tuning capacitance is given by

$$\frac{\partial \omega_0}{\partial \widetilde{C}} = \frac{\partial \omega_0}{\partial C}\frac{\partial C}{\partial \widetilde{C}} \approx -\frac{\omega_0}{2C}\frac{\partial C}{\partial \widetilde{C}}, \tag{6.22}$$

where we in the last approximation used (6.21).

The VCO tuning constant, K_{VCO}, can now be calculated by inserting (6.22) in (6.18) as

$$K_{VCO} \approx -\frac{\omega_0}{V_1}\frac{C_1}{2C}\frac{\partial C}{\partial \widetilde{C}}. \tag{6.23}$$

6.4 Phase Noise due to Frequency Tuning

The frequency tuning may cause excess phase noise, mainly through the process of AM-to-PM conversion [Hegazi and Abidi, 2003].

From Section 7.2.6 we have the phase noise at frequency offset ω_m due to white noise sources as

$$\mathcal{L}[\omega_m] \approx \frac{k_B T F Z_{11}}{V_{out,1}^2 Q^2}\frac{\omega_0^2}{\omega_m^2}, \tag{6.24}$$

where k_B is the Boltzmann constant, T is the temperature, Q is the Q-value of the oscillator, ω_0 is the oscillation frequency, $V_{out,1}$ is the voltage amplitude at the output of the active part, and F is the noise factor given by

$$F \approx 1 + \gamma\frac{Z_{11}}{|Z_{21}|} + K_1K_2 + K_{AM-PM}^2\left(1 + \gamma|\widetilde{G}_{\Delta,1}^{(I)}|Z_{11} + K_1K_3\right), \tag{6.25}$$

where K_{AM-PM} is the AM-to-PM conversion, Z_{11} and Z_{21} are the input impedance and transimpedance of the feedback network at the oscillation frequency, assumed here to be real, $\widetilde{G}_{\Delta,1}^{(I)}$ is the large-signal incremental gain of the amplifying part of the active part, γ is a noise constant depending on the transistor type used, and K_1, K_2 and K_3 are bias-dependent expressions given in Section 7.2.6.

As derived in Section 8.4, we have the AM-to-PM conversion as

$$K_{AM-PM} = \frac{|Y_1|\widetilde{H}_{\Delta,1}^{(I)}\left(\frac{\partial\alpha}{\partial|X_1|} + \frac{\partial\zeta}{\partial|X_1|}\right)}{1 - \widetilde{F}_{\Delta,1}^{(I)}\widetilde{H}_{\Delta,1}^{(I)}}, \tag{6.26}$$

where Y_1 is the fundamental output current of the active part, X_1 is the fundamental input voltage to the active part, α and ζ are the phase shift of the feedback and active parts, respectively, and $\widetilde{F}_{\Delta,1}^{(I)}$ and $\widetilde{H}_{\Delta,1}^{(I)}$ are the incremental large-signal gains of the active network and of the feedback network, respectively.

If the phase change due to amplitude variations for the active part, f, is low compared to that of the feedback part, h, which is the case for a

well-designed VCO, we have that

$$K_{AM-PM} \approx |Y_1| \frac{\widetilde{H}^{(I)}_{\Delta,1}}{1 - \widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} \frac{\partial \alpha}{\partial |X_1|}. \tag{6.27}$$

We rewrite this expression as

$$K_{AM-PM} \approx \frac{|X_1|}{1 - \widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} \frac{\widetilde{H}^{(I)}_{\Delta,1}}{\widetilde{H}_1} \frac{\partial \alpha}{\partial |X_1|}, \tag{6.28}$$

where we have used that $X_1 = \widetilde{H}_1 Y_1$. For a fairly linear feedback network, we also have $\widetilde{H}^{(I)}_{\Delta,1} \approx \widetilde{H}_1$.

We now need the phase sensitivity to amplitude variations, which can be expressed as

$$\frac{\partial \alpha}{\partial |X_1|} = -\frac{\partial \alpha}{\partial \omega_0} \frac{\partial \omega_0}{\partial \widetilde{C}} \frac{\partial \widetilde{C}}{\partial V_1} \frac{\partial V_1}{\partial |X_1|}, \tag{6.29}$$

where we have used that

$$\frac{\partial \alpha}{\partial \widetilde{C}} = -\frac{\partial \alpha}{\partial \omega_0} \frac{\partial \omega_0}{\partial \widetilde{C}}, \tag{6.30}$$

which stems from the fact that the phase shift in the feedback network must be constant and hence

$$\frac{\partial \alpha(\omega_0(\widetilde{C}), \widetilde{C})}{\partial \widetilde{C}} = \frac{\partial \alpha(\omega_0, \widetilde{C})}{\partial \widetilde{C}} + \frac{\partial \alpha(\omega_0, \widetilde{C})}{\partial \omega_0} \frac{\partial \omega_0}{\partial \widetilde{C}} = 0. \tag{6.31}$$

From (E.1) in Appendix E we have the first fraction in (6.29) as

$$\frac{\partial \alpha}{\partial \omega_0} \approx -\frac{2Q}{\omega_0}, \tag{6.32}$$

where we have assumed that $\frac{\partial \zeta}{\partial \omega_0} \approx 0$.

We can calculate the change in capacitance, $\widetilde{C}$, due to a change in voltage amplitude, V_1, over the capacitance as

$$\frac{\partial \widetilde{C}}{\partial V_1} = \frac{1}{V_1} \frac{\partial Q_1}{\partial V_1} - \frac{Q_1}{V_1^2} = \frac{1}{V_1}\left(C_0 + \frac{1}{2}C_2\right) - \frac{1}{V_1}\left(C_0 - \frac{1}{2}C_2\right) = \frac{C_2}{V_1}, \tag{6.33}$$

where we have used (6.15), (6.10), and

$$\frac{\partial Q_1}{\partial V_1} = \frac{1}{\pi}\int_{-\pi}^{\pi} c(V_0 + V_1\cos(\theta))\cos^2(\theta) d\theta = C_0 + \frac{1}{2}C_2, \tag{6.34}$$

where we have used the expression for the fundamental component of the charge, Q_1, given in (6.17).

The remaining factor in (6.29) can be approximated as

$$\left|\frac{\partial V_1}{\partial |X_1|}\right| \approx \frac{V_1}{|X_1|} \tag{6.35}$$

for the cases where the transfer function from X_1 to V_1 is fairly linear.

We can now calculate the maximum sensitivity as

$$\max\left|\frac{\partial \alpha}{\partial |X_1|}\right| \approx \frac{2Q}{\omega_0}\frac{\partial \omega_0}{\partial \widetilde{C}}\frac{\max|C_2|}{V_1}\frac{\partial V_1}{\partial |X_1|} = \frac{2Q}{\omega_0}\max|K_{VCO}|\frac{\max|C_2|}{\max|C_1|}\frac{\partial V_1}{\partial |X_1|}, \tag{6.36}$$

where we have used (6.32) and (6.33) and in the last stage also (6.19).

Finally, by using (6.35) and (6.36) in (6.28), we get

$$\max|K_{AM-PM}| \approx \frac{1}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}\left|\frac{\widetilde{H}^{(I)}_{\Delta,1}}{\widetilde{H}_1}\right|\frac{2Q}{\omega_0}V_1\max|K_{VCO}|\frac{\max|C_2|}{\max|C_1|}. \tag{6.37}$$

We see that there are three ways to decrease the AM-to-PM conversion. First, we may use an amplitude-regulating mechanism that makes $\widetilde{H}^{(I)}_{\Delta,1} \ll \widetilde{H}_1$ or $|\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}| \gg 1$. Second, we may make the VCO gain, K_{VCO}, low by splitting the tuning range into several smaller parts. Third, we may choose a varactor having a low fraction $\frac{\max|C_2|}{\max|C_1|}$. We assume that the oscillation frequency, ω_0, is given, and that we do not want to decrease the Q-value, Q, considerably.

6.5 Diode Varactor

When the diode is reverse biased a depletion region is formed, creating a capacitance between the anode and the cathode. An increase in the reverse-biasing voltage increases the depletion region, thereby decreasing the capacitance.

6.5.1 Background

Diodes are available both in bipolar and in MOS technologies. They are also available as discrete components.

Depending on the doping profile, different C–V characteristics may be obtained. Diodes sold as varactors usually have a doping profile that makes the capacitance a strong function of the reverse-biasing voltage, thereby allowing a large frequency tuning range in oscillators. In processes dedicated

to analog design, there may be diodes available that are designed to be used as varactors, such as hyper-abrupt varactors. To create such specific components, additional processing steps need to be added, thereby increasing the cost. It is up to the designer of the oscillator to decide if the availability of this type of diodes is needed. Even if this type of diodes is not strictly needed, the additional cost may be acceptable if it gives other advantages such as lower power consumption.

6.5.2 Phase-Noise Parameters

The small-signal capacitance for a diode varactor with constant doping can be written as

$$c(v) = \frac{C_N}{\sqrt{1 + \frac{v}{\psi}}}, \tag{6.38}$$

where C_N is the capacitance when no reverse bias voltage, v, is applied and ψ is the built-in potential. The small-signal capacitance is plotted in Figure 6.1 as a function of the reverse voltage normalized to the built-in potential.

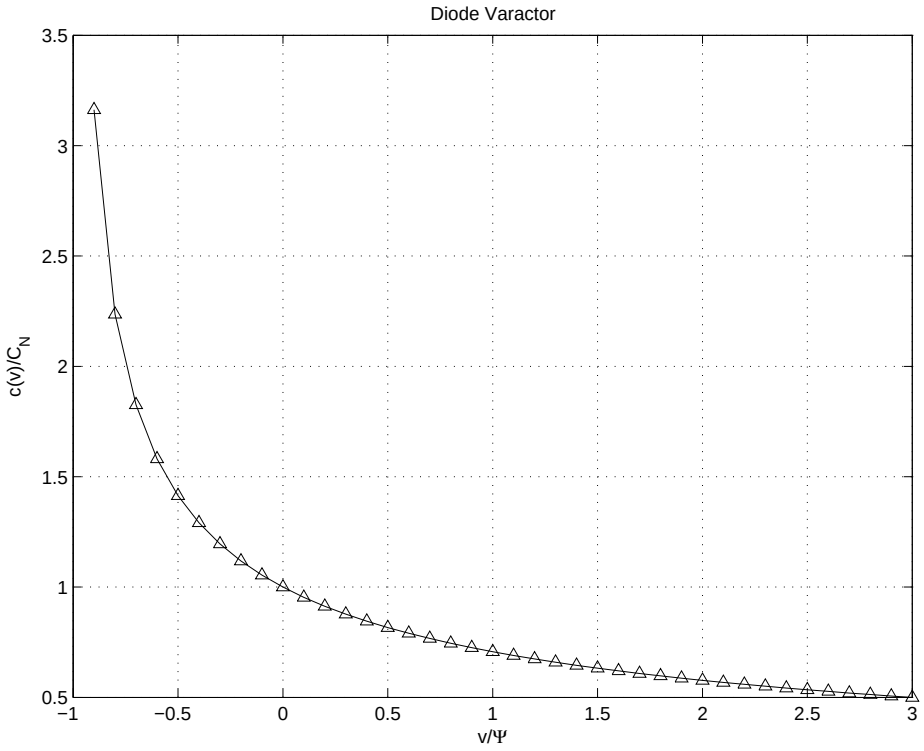


Figure 6.1: Normalized small-signal capacitance of diode varactors as function of the reverse-bias voltage, v, normalized to the built-in potential, ψ.

The control voltage, v, is approximately given by

$$v(t) = V_0 + V_1 \cos(\omega_0 t), \tag{6.39}$$

where V_0 is a DC voltage and V_1 is the voltage amplitude for the fundamental component, assumed to be positive.

When operated as a varactor, the voltage amplitude, V_1, may be considered approximately constant and the large-signal capacitance is altered by changing the reverse DC voltage, V_0. The large-signal capacitance, $\widetilde{C}$, is given in Figure 6.2 together with the large-signal capacitance parameters C_0, C_1 and C_2, defined by (6.4).

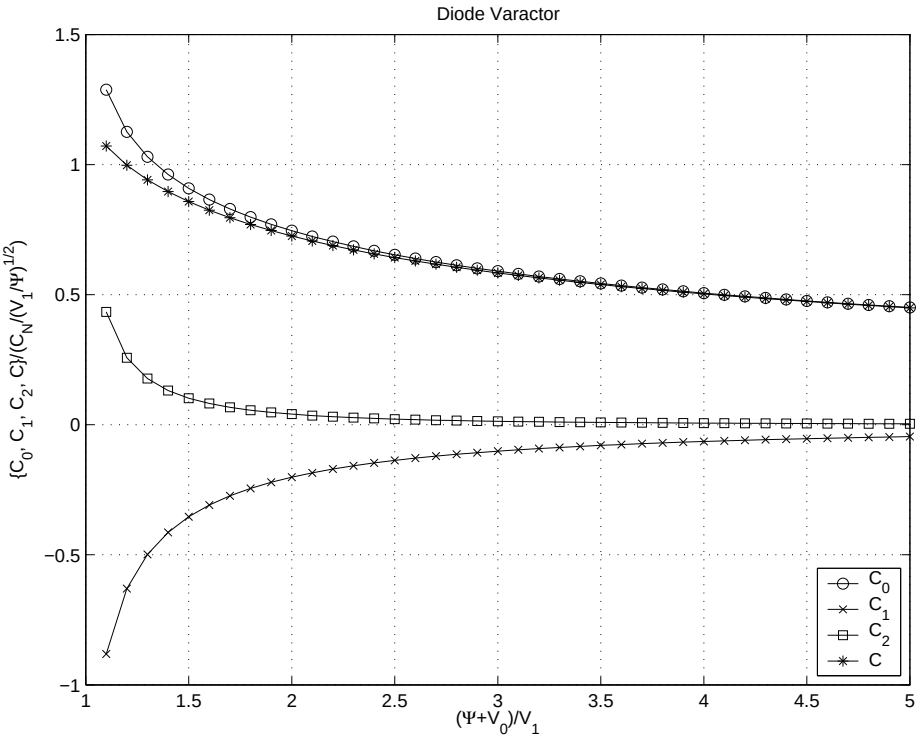


Figure 6.2: Normalized large-signal capacitance parameters of diode varactors as function of the control voltage normalized to the voltage amplitude.

For moderate voltage variations, v_Δ, over the diode, we can approximate the small-signal capacitance with the first few terms of its Taylor expansion as

$$c(v_\Delta) \approx \frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}} \left(1 - \frac{1}{2}\left(\frac{v_\Delta}{\psi+V_0}\right) + \frac{3}{8}\left(\frac{v_\Delta}{\psi+V_0}\right)^2 - \frac{5}{16}\left(\frac{v_\Delta}{\psi+V_0}\right)^3\right), \tag{6.40}$$

where the voltage over the diode is written as a DC term, V_0, plus an incremental voltage, v_Δ, according to

$$v = V_0 + v_\Delta. \tag{6.41}$$

The large-signal capacitance parameters can now be approximated as

$$C_0 \approx \frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}}\left(1+\frac{3}{16}\left(\frac{V_1}{\psi+V_0}\right)^2\right), \tag{6.42}$$

$$C_1 \approx -\frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}}\left(\frac{1}{2}\left(\frac{V_1}{\psi+V_0}\right)+\frac{15}{64}\left(\frac{V_1}{\psi+V_0}\right)^3\right) \tag{6.43}$$

and

$$C_2 \approx \frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}}\left(\frac{3}{16}\left(\frac{V_1}{\psi+V_0}\right)^2\right), \tag{6.44}$$

and the large-signal capacitance, $\widetilde{C}$, can be approximated as

$$\widetilde{C} = C_0 - \frac{1}{2}C_2 \approx \frac{C_N}{\sqrt{1+\frac{V_0}{\psi}}}\left(1+\frac{3}{32}\left(\frac{V_1}{\psi+V_0}\right)^2\right). \tag{6.45}$$

These approximations are plotted in Figure 6.3.

The quotient between C_2 and C_1 can then be approximated as

$$\frac{|C_2|}{|C_1|} \approx \frac{3}{8}\left(\frac{V_1}{\psi+V_0}\right) \tag{6.46}$$

using only the first term in the approximations for C_1 and C_2. This approximation is plotted together with the values we get for this fraction by the numerical solution of (6.4) in Figure 6.4.

For the diode varactor we also have that the maximum tuning range, ω_{tune}, is approximately given by

$$\omega_{tune} \approx \left|\frac{\partial\omega_0}{\partial\widetilde{C}}\right|(\widetilde{C}_{max}-\widetilde{C}_{min}) = \frac{V_1 \max|K_{VCO}|}{\max|C_1|}(\widetilde{C}_{max}-\widetilde{C}_{min}), \tag{6.47}$$

where we have used (6.19), and where

$$\widetilde{C}_{min} \approx C_N\sqrt{\frac{\psi}{\psi+V_{0,min}}} \tag{6.48}$$

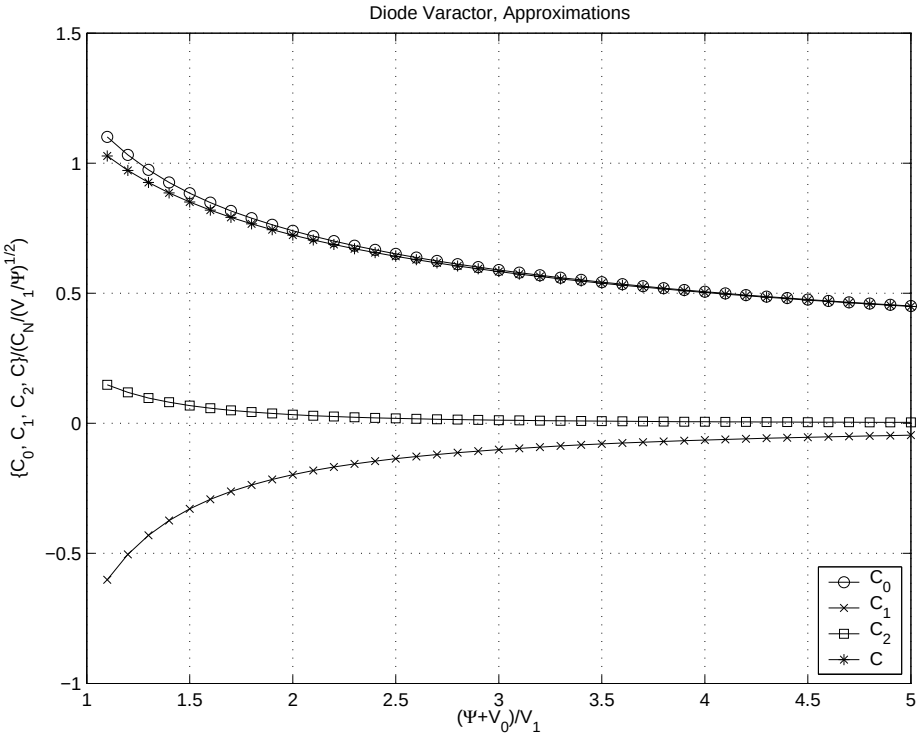


Figure 6.3: Normalized approximate large-signal capacitance parameters as function of control voltage normalized to voltage amplitude. Third order Taylor expansion has been used as approximation.

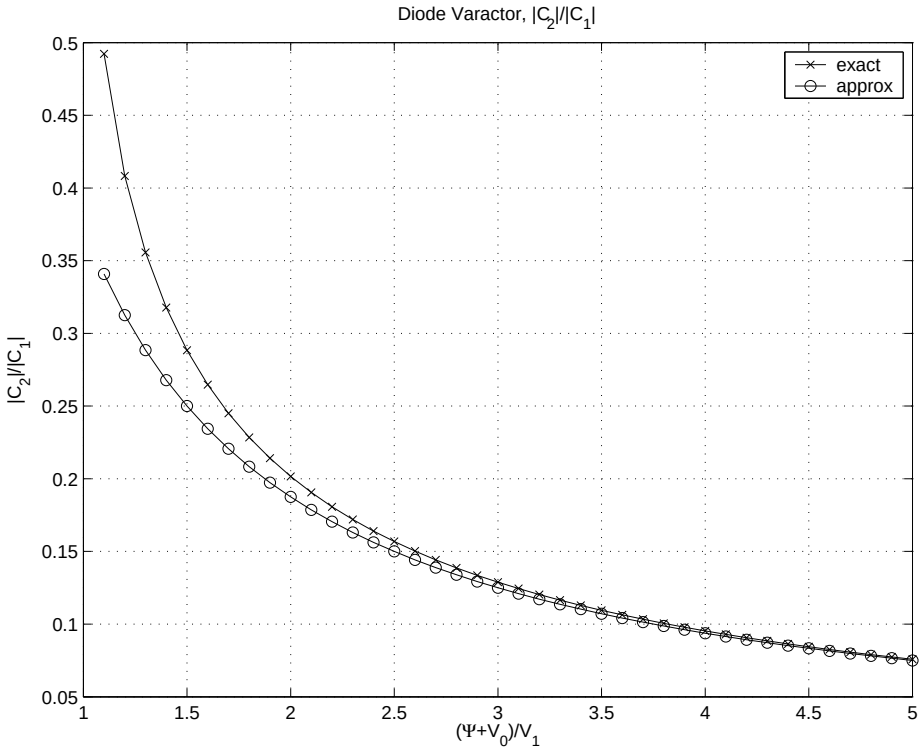


Figure 6.4: The fraction of C2 over C1 as function of control voltage normalized to the voltage amplitude.

and

$$\widetilde{C}_{max} \approx C_N \sqrt{\frac{\psi}{\psi + V_{0,max}}} \tag{6.49}$$

by using the first term of (6.45) only. Inserting (6.47), (6.46), and the first term of (6.43), given as

$$\max|C_1| \approx C_N \sqrt{\frac{\psi}{\psi + V_{0,min}}} \left(\frac{1}{2} \frac{V_1}{\psi + V_{0,min}} \right) \tag{6.50}$$

in (6.37), we get

$$\max|K_{AM-PM}| \approx \frac{1}{1 - \widetilde{F}^{(I)}_{\Delta,1} \widetilde{H}^{(I)}_{\Delta,1}} \left| \frac{\widetilde{H}^{(I)}_{\Delta,1}}{\widetilde{H}_1} \right| \frac{3Q\omega_{tune}}{8\omega_0} \frac{\left(\frac{V_1}{\psi + V_{0,min}} \right)^2}{1 - \sqrt{\frac{\psi + V_{0,min}}{\psi + V_{0,max}}}}. \tag{6.51}$$

6.6 MOS Varactor

The MOS structures used when creating transistors in a CMOS process may also be used to create capacitors. When used as a tuning capacitor, the MOS structure is called a varactor. The MOS varactor could either be designed to operate in inversion or in accumulation [Andreani and Mattisson, 2000].

6.6.1 Background

The large-signal properties of the MOS varactor has recently been investigated [Bunch and Raman, 2003, Hegazi and Abidi, 2003], both regarding its impact on tuning characteristics and its impact on the phase noise via AM-to-PM conversion. In addition to the already known expression for the large-signal capacitance, we derive an expression for the maximum AM-to-PM conversion.

6.6.2 Phase Noise Parameters

The small-signal capacitance, c, of an MOS varactor is approximated as

$$c(v) \approx \begin{cases} C_L & , v \leq 0 \\ C_H & , v > 0, \end{cases} \tag{6.52}$$

where v is the control voltage [Hegazi and Abidi, 2003]. In other words, the capacitance is equal to C_L for negative v and equal to C_H for positive v.

The control voltage, v, is approximately given by

$$v(t) = V_0 + V_1 \cos(\omega_0 t), \tag{6.53}$$

where V_0 is a DC voltage and V_1 is the voltage amplitude for the fundamental component, assumed to be positive.

The large-signal capacitance parameters are calculated, using (6.4), to be

$$C_0 = \begin{cases} C_L & , V_0 < -V_1 \\ C_L + (C_H - C_L)\frac{1}{\pi}\arccos\left(-\frac{V_0}{V_1}\right) & , |V_0| \le V_1 \\ C_H & , V_0 > V_1, \end{cases} \tag{6.54}$$

$$C_1 = \begin{cases} (C_H - C_L)\frac{2}{\pi}\sqrt{1 - \frac{V_0^2}{V_1^2}} & , |V_0| \le V_1 \\ 0 & , |V_0| > V_1, \end{cases} \tag{6.55}$$

and

$$C_2 = \begin{cases} -(C_H - C_L)\frac{2}{\pi}\frac{V_0}{V_1}\sqrt{1 - \frac{V_0^2}{V_1^2}} & , |V_0| \le V_1 \\ 0 & , |V_0| > V_1, \end{cases} \tag{6.56}$$

and the large-signal capacitance is given by

$$\widetilde{C} = \begin{cases} C_L & , V_0 < -V_1 \\ C_L + (C_H - C_L)\left(\frac{1}{\pi}\arccos\left(-\frac{V_0}{V_1}\right) + \frac{1}{\pi}\frac{V_0}{V_1}\sqrt{1 - \frac{V_0^2}{V_1^2}}\right) & , |V_0| \le V_1 \\ C_H & , V_0 > V_1, \end{cases} \tag{6.57}$$

where we have used (6.10), (6.54) and (6.56). This expression for the large-signal capacitance has also been derived by Hegazi and Abidi [Hegazi and Abidi, 2003].

Both the small-signal capacitance and the large-signal capacitance parameters are plotted in Figure 6.5.

From (6.55) we have the maximum absolute value for C_1 as

$$\max|C_1| = \frac{2}{\pi}|C_H - C_L| \tag{6.58}$$

when $V_0 = 0$, and from (6.55) we have the maximum absolute value for C_2 as

$$\max|C_2| = \frac{1}{\pi}|C_H - C_L| \tag{6.59}$$

when $V_0 = \pm\frac{1}{\sqrt{2}}V_1$.

Combining (6.58) and (6.59) we get

$$\frac{\max|C_2|}{\max|C_1|} = \frac{1}{2}. \tag{6.60}$$

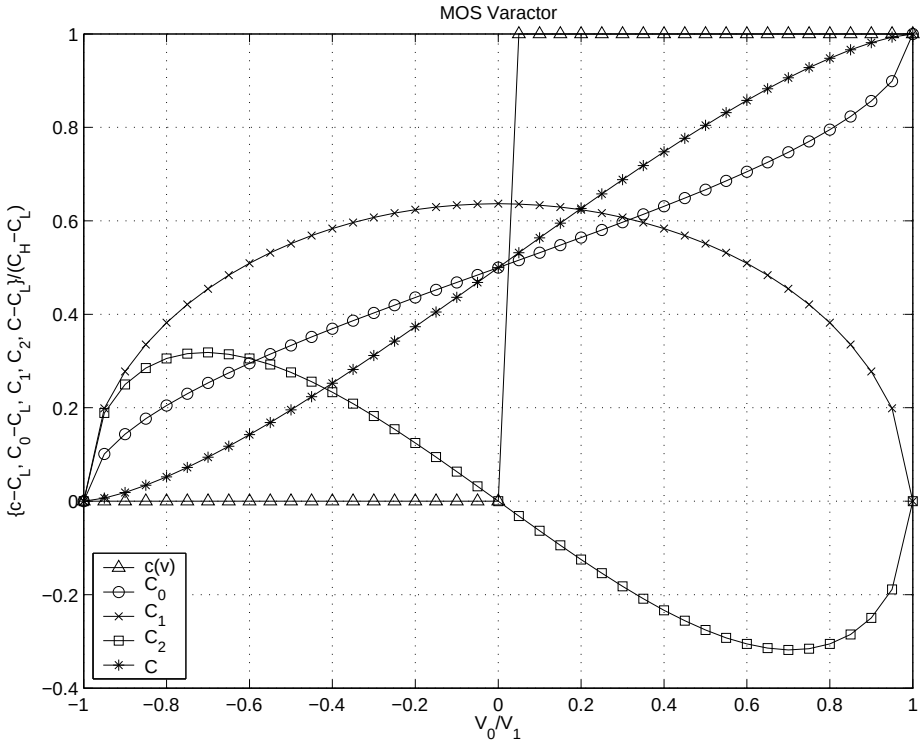


Figure 6.5: Normalized small-signal and large-signal capacitances as function of the control voltage normalized to the voltage amplitude for the MOS varactor.

For the MOS varactor we also have that the maximum tuning range, ω_{tune}, is approximately given as

$$\omega_{tune} \approx \left|\frac{\partial\omega_0}{\partial\widetilde{C}}\right| |C_H - C_L| = \frac{V_1 \max|K_{VCO}|}{\max|C_1|}|C_H - C_L| = \frac{\pi}{2}V_1 \max|K_{VCO}|, \tag{6.61}$$

where we have used (6.19). Inserting (6.61), (6.60), and (6.58) in (6.37) gives

$$\max|K_{AM-PM}| \approx \frac{1}{1 - \widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} \left|\frac{\widetilde{H}^{(I)}_{\Delta,1}}{\widetilde{H}_1}\right| \frac{2Q\omega_{tune}}{\pi\omega_0}. \tag{6.62}$$

6.7 Summary

We have shown that there are several ways to minimize the AM-to-PM conversion due to the varactor. In addition to having an amplitude-regulating mechanism that minimizes the AM-to-PM conversion or splitting the tuning range into several smaller tuning ranges, thereby decreasing the VCO tuning constant, we may choose a varactor giving low AM-to-PM conversion. The key choice is to get a varactor having a low fraction $\frac{\max|C_2|}{\max|C_1|}$, where C_1 and C_2 are defined in (6.4).

The simple varactors used today, the diode varactor and the MOS varactor, have a fraction $\frac{\max|C_2|}{\max|C_1|}$ in the order of a few tenths. However, several components may be combined to create varactors having capacitance curves different than those of the components, thereby reducing the fraction $\frac{\max|C_2|}{\max|C_1|}$ compared to the components alone [Levantino et al., 2004]. In these compound varactors, the components do not necessarily have one terminal signal grounded.

Chapter 7

Phase-Noise Calculations

Thermal and shot noise within the oscillator give a lower bound on the minimum achievable phase noise. This noise arises both in the feedback network due to lossy components and in the active components, *e.g.* transistors. In addition to thermal and shot noise, we also have components generating 1/f noise. The phase noise originating from 1/f noise may dominate the phase-noise performance at small frequency offsets from the carrier. Apart from these noise sources, we may also have disturbances originating from outside the circuit, such as noise on the supply voltage or noise coupled capacitively or magnetically into the circuit.

In this chapter I derive expressions for the phase noise of oscillators using the method of Impulse Sensitivity Functions (ISFs). The expressions used for the ISFs are derived in Chapter 8.

7.1 Introduction

Phase noise has been the topic of extensive research during the last decades. In 1966, a simple formula describing the spectral density of the phase noise was given by Leeson [Leeson, 1966]; it contained several unknown noise parameters. Later work has been devoted to the calculation of these noise parameters [Huang, 1998, Hajimiri and Lee, 1998, Samori et al., 1998, Rael and Abidi, 2000, Samori et al., 2000]

On the numerical simulator side, work has been devoted to the implementation of fast and accurate predictions of the phase noise [Kaertner, 1990, Demir, 1998, Kundert, 1999, Demir et al., 2000]. These methods are, however, not suitable to use when deriving closed-form analytical expressions for the phase noise.

Usually, some accuracy in the prediction of a performance measure may be sacrificed if we can attain a simple analytical expression for the performance measure from which we can obtain design insights. In this chapter we use the method of Impulse Sensitivity Functions (ISFs) to derive closed-form expressions for the phase noise [Hajimiri and Lee, 1998, Vanassche et al., 2003].

7.1.1 Assumptions

In Appendix B it is shown that one may calculate the single-sided phase-noise spectral density, $\mathcal{L}$, at a large frequency offset, ω_m, from the oscillation frequency, ω_0, as

$$\mathcal{L}[\omega_m] = \frac{S_{\overline{y}}(\omega_m)}{2\omega_m^2}, \tag{7.1}$$

where $S_{\overline{y}}$ is the averaged single-sideband noise spectral density. All spectral densities in this chapter are assumed to be single sided.

We assume that the active part is a transconductance with small delay compared to the oscillation period, $1/\omega_0$. Consequently, the feedback part must be a transresistance and is best described by its Z-parameters, defined in Appendix D. We use Z_{mn} as a short form for $Z_{mn}(\omega_0)$, where ω_0 is the oscillation frequency.

7.2 Phase Noise due to White Noise

The thermal noise and shot noise in lossy components are sources of white noise. The power spectral density, S_y, for these types of noise is constant with frequency for all frequencies of interest. Hence, the averaged noise spectral density, $S_{\overline{y}}$, is also white with the spectral density given by

$$S_{\overline{y}} = \overline{\Gamma_y^2 S_y}, \tag{7.2}$$

where Γ_y is the Impulse Sensitivity Function (ISF). The over-line is used to denote time averaging. The two main ISFs we use in this chapter are Γ_x for voltage noise entering at the input to the active part and Γ_y for current noise entering at the output of the active part.

7.2.1 Noise from Feedback Network

We assume that the feedback network is fairly linear such that the equivalent thermal noise spectral density at the output of the passive feedback network,

h, can be calculated as

$$S_{x,h}(\omega, t) = 4k_B T \Re[Z_{22}(\omega)], \tag{7.3}$$

where k_B is the Boltzmann constant, T is the temperature and Z_{22} is the output impedance of the feedback network, h, [Pettai, 1984, Bennett, 1960]. The noise spectral density of passive two-port networks is further discussed in Appendix D.

For oscillators with a feedback network with a fairly high Q-value we can assume that the noise is non-negligible only around the fundamental frequency, ω_0, and we consequently have to consider just the fundamental component of the ISF.

Since the noise spectral density is constant with time the averaged noise spectral density is simply

$$S_{\overline{x},h}(\omega_m) \approx \frac{1}{2}|\Gamma_{x,1}|^2 S_{x,h}(\omega_0) = 2k_B T \Re[Z_{22}]|\Gamma_{x,1}|^2. \tag{7.4}$$

We can rewrite the ISF using

$$\Im[\Gamma_{x,1}] = \frac{\Im[\Gamma_{y,1}]}{\widetilde{H}_1} = \frac{\Im[\Gamma_{y,1}]}{Z_{21}} \tag{7.5}$$

and

$$\Re[\Gamma_{x,1}] = \frac{\Re[\Gamma_{y,1}]}{\widetilde{H}^{(I)}_{\Delta,1}} = \frac{\Re[\Gamma_{y,1}]}{\widetilde{Z}^{(I)}_{\Delta,21}}, \tag{7.6}$$

using (8.68) and (8.69) from Chapter 8, where $\widetilde{H}_1$ and Z_{21} are the large-signal transfer functions for the feedback part and $\widetilde{H}^{(I)}_{\Delta,1}$ and $\widetilde{Z}^{(I)}_{\Delta,21}$ are the incremental large-signal transfer functions for the feedback part.

If the feedback network is almost linear, we can approximate $\widetilde{Z}^{(I)}_{\Delta,21}$ with Z_{21} and we get

$$\Gamma_{x,1} \approx \frac{\Gamma_{y,1}}{Z_{21}}. \tag{7.7}$$

We can now write the average noise spectral density as

$$S_{\overline{x},h}(\omega_m) \approx 2k_B T \Re[Z_{22}] \frac{|\Gamma_{y,1}|^2}{Z_{21}^2}. \tag{7.8}$$

If possible, we should choose feedback networks that fulfill

$$\Re[Z_{11}]\Re[Z_{22}] \approx Z_{21}^2 \tag{7.9}$$

in order to minimize the phase noise due to noise from the feedback network. We then get the average noise spectral density as

$$S_{\overline{x},h}(\omega_m) \approx \frac{2k_BT}{\Re[Z_{11}]}|\Gamma_{y,1}|^2; \tag{7.10}$$

see also Appendix D.3.

The average noise spectral density given in (7.10) can be rewritten as

$$S_{\overline{x},h}(\omega_m) \approx \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\left(1+\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\right), \tag{7.11}$$

where we have expanded the absolute value of the fundamental component of the ISF, $\Gamma_{y,1}$, in a real and an imaginary part.

7.2.2 Noise from Active Network

We assume that the output noise spectral density of the active part, f, is proportional to the incremental gain of the active part according to

$$S_{y,g}(\omega,t) = 4k_BT\gamma|g'(X_1\cos(\omega_0 t))|, \tag{7.12}$$

where γ is a proportionality constant equal to 1/2 for bipolar circuits and 2/3 for circuits with FETs, but may be higher for MOSFETs with high electrical fields. This assumption is true both for one-transistor stages and for differential stages as shown in Appendix C.

Since the transconductance is a periodic function with angular frequency ω_0 we can write it as a Fourier series according to

$$|g'(X_1\cos(\omega_0 t))| = \sum_{n=0}^{\infty}\widetilde{G'}_n\cos(n\omega_0 t). \tag{7.13}$$

We can now calculate the averaged noise spectral density, assuming that the fundamental component of the ISF is dominant, to be

$$S_{\overline{y},g}(\omega_m) \approx 4k_BT\gamma\left(\frac{1}{2}\widetilde{G'}_0\Gamma_{y,1}\Gamma_{y,1}^* + \frac{1}{8}\widetilde{G'}_2\left(\Gamma_{y,1}^2+{\Gamma_{y,1}^*}^2\right)\right), \tag{7.14}$$

which can be rewritten using the real and imaginary parts of $\Gamma_{y,1}$ as

$$S_{\overline{y},g}(\omega_m) \approx 4k_BT\gamma\left(\frac{1}{2}\widetilde{G'}_0\left(\Re[\Gamma_{y,1}]^2+\Im[\Gamma_{y,1}]^2\right)+\frac{1}{4}\widetilde{G'}_2\left(\Re[\Gamma_{y,1}]^2-\Im[\Gamma_{y,1}]^2\right)\right). \tag{7.15}$$

This expression can be rewritten as

$$S_{\overline{y},g}(\omega_m) \approx 2k_B T\gamma \left(|\widetilde{G}_{\Delta,1}^{(I)}| \Re[\Gamma_{y,1}]^2 + |\widetilde{G}_1| \Im[\Gamma_{y,1}]^2 \right) \tag{7.16}$$

using results from Appendix A.2, where $\widetilde{G}_{\Delta,1}^{(I)}$ is the incremental large-signal transconductance and $\widetilde{G}_1$ is the large-signal transconductance of the active part, excluding any amplitude-regulating loop.

This expression can be rewritten once more as

$$S_{\overline{y},g}(\omega_m) \approx \frac{2k_B T \Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]} \gamma \left(\frac{\Re[Z_{11}]}{|Z_{21}|} + \Re[Z_{11}] |\widetilde{G}_{\Delta,1}^{(I)}| \frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2} \right), \tag{7.17}$$

using that

$$\widetilde{G}_1 = \widetilde{F}_1 = \frac{1}{\widetilde{H}_1} = \frac{1}{Z_{21}}, \tag{7.18}$$

where we have used the Barkhausen criterion, $\widetilde{F}_1 \widetilde{H}_1 = 1$, where $\widetilde{F}_1$ and $\widetilde{H}_1$ are the large-signal gains of the active and feedback parts, respectively. Observe that $\widetilde{G}_{\Delta,1}^{(I)}$ is not equal to $\widetilde{F}_{\Delta,1}^{(I)}$ when an explicit amplitude control is used.

In addition to the noise from transistors already treated in this section we also have shot noise from the base–emitter junction in the bipolar transistor, induced gate noise in the field-effect transistor, and noisy base or gate resistances.

As shown in Appendix C, base shot noise may be neglected since the transistor is voltage-driven and induced gate noise may be neglected when the operation frequency is substantially lower than the transit frequency for the transistors.

7.2.3 Noise from Series Base and Gate Resistances

Noise from series base and gate resistances does not get filtered by the feedback network since these noise sources are located directly at the input to the active part. Consequently, we must use the total ISF for the input to the active part, Γ_x, and cannot neglect any of its harmonics.

Neglecting the AM-to-PM conversion of noise, we can use the ISF given in (8.26) as its frequency components, repeated here for convenience:

$$\Gamma_{x,n} = j \frac{n\widetilde{F}_n \omega_0}{|X_1| \widetilde{F}_1 Q} = \frac{n\widetilde{F}_n}{\widetilde{F}_1} \Gamma_{x,1}. \tag{7.19}$$

The voltage noise from the series base or gate resistance, R_I, is given by

$$S_{x,i} = 4k_B T R_I. \tag{7.20}$$

The averaged noise spectral density is given by

$$S_{\overline{x},i} = S_{x,i}\left(|\Gamma_{x,0}|^2 + \frac{1}{2}\sum_{n=1}^{\infty}|\Gamma_{x,n}|^2\right) = S_{x,i}\frac{|\Gamma_{x,1}|^2}{2}\sum_{n=1}^{\infty}\frac{|\Gamma_{x,n}|^2}{|\Gamma_{x,1}|^2}. \tag{7.21}$$

Combining (7.19), (7.20) and (7.21), we get the averaged noise spectral density as

$$S_{\overline{x},i} = 2k_BT|\Gamma_{x,1}|^2\sum_{n=1}^{\infty}\frac{n^2|\widetilde{F}_n|^2}{|\widetilde{F}_1|^2}. \tag{7.22}$$

Using (8.69), we may rewrite this expression as

$$S_{\overline{x},i} = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{R_I}{\Re[Z_{11}]}\frac{\Re[Z_{11}]^2}{Z_{21}^2}\sum_{n=1}^{\infty}\frac{n^2|\widetilde{F}_n|^2}{|\widetilde{F}_1|^2}. \tag{7.23}$$

We see that the amount of harmonics in the oscillator, coming from the nonlinearity in the transistor, affects the amount of phase noise due to series base and gate resistances. Since the nonlinearity of the transistor increases with input amplitude to the transistor, the phase noise increases with increasing input amplitude.

7.2.4 Noise from Diode Limiting

We next calculate the contribution from the diodes to the phase noise. In this section, we assume the diode series resistance to be negligible. From Appendix C we have that the noise current spectral density from a diode is given by

$$S_d(\omega,t) = 2k_BTg_{ac}(v_{AC}(t)) = 2k_BTg_{ac}(V_{ac,0} + V_{ac,1}\cos(\omega_0 t)), \tag{7.24}$$

where $V_{ac,0}$ and $V_{ac,1}$ are the DC voltage and fundamental voltage amplitude across the diode, respectively, v_{AC} is the total voltage across the diode, and the small-signal conductance of the diode, g_{ac}, is given by

$$g_{ac} = \frac{\partial i_D}{\partial v_{AC}} = \frac{i_D}{V_T}, \tag{7.25}$$

where i_D is the diode current and V_T is the thermal voltage.

Since the conductance is a periodic function with angular frequency ω_0, we can express it as a Fourier series according to

$$g_{ac}(V_{ac,0} + V_{ac,1}\cos(\omega_0 t)) = \sum_{n=0}^{\infty}\widetilde{I}'_{dn}\cos(n\omega_0 t). \tag{7.26}$$

We can now calculate the averaged noise spectral density, assuming that the fundamental component of the ISF is dominant, to be

$$S_{\overline{d}}(\omega_m) \approx 2k_B T \left(\frac{1}{2} \widetilde{I}'_{d0} \Gamma_{d,1} \Gamma^*_{d,1} + \frac{1}{8} \widetilde{I}'_{d2} \left(\Gamma^2_{d,1} + {\Gamma^*_{d,1}}^2 \right) \right), \tag{7.27}$$

where $\Gamma_{d,1}$ is the ISF for noise currents parallel to the diode. This expression can be rewritten using the real and imaginary parts of $\Gamma_{d,1}$ as

$$S_{\overline{d}}(\omega_m) \approx 2k_B T \left(\frac{1}{2} \widetilde{I}'_{d0} \left(\Re[\Gamma_{d,1}]^2 + \Im[\Gamma_{d,1}]^2 \right) + \frac{1}{4} \widetilde{I}'_{d2} \left(\Re[\Gamma_{d,1}]^2 - \Im[\Gamma_{d,1}]^2 \right) \right). \tag{7.28}$$

This expression can be rewritten once more as

$$S_{\overline{d}}(\omega_m) \approx k_B T \left(\widetilde{G^{(I)}_{ac\Delta,1}} \Re[\Gamma_{d,1}]^2 + \widetilde{G_{ac1}} \Im[\Gamma_{d,1}]^2 \right), \tag{7.29}$$

using results from Appendix A.2. From Appendix C.1, we have that

$$\widetilde{G_{ac1}} = \frac{I_{d,1}}{V_{ac,1}} \tag{7.30}$$

and

$$\widetilde{G^{(I)}_{ac\Delta,1}} \approx \frac{I_{d,1}}{V_T} = \widetilde{G_{ac1}} \frac{V_{ac,1}}{V_T}. \tag{7.31}$$

In most cases $\Re[\Gamma_{d,1}]$ is inversely proportional to $\widetilde{G^{(I)}_{ac\Delta,1}}$ and we can approximate the averaged noise spectral density with

$$S_{\overline{d}}(\omega_m) \approx k_B T \widetilde{G_{ac1}} \Im[\Gamma_{d,1}]^2 \tag{7.32}$$

when $V_{ac,1} \gg V_T$, which is half the noise we would expect from a resistor with conductance $\widetilde{G_{ac1}}$ inserted instead of the diode.

7.2.5 Noise from Biasing Network

Apart from the noise inherent to the oscillator core, we also have noise originating in the biasing network. The bias network is not part of the oscillator high-frequency feedback loop, but is nevertheless necessary for the active part to function properly. It sets the operating point such that the oscillator starts and regulates the oscillation amplitude once it has started.

We consider two types of biasing networks in detail: biasing using transistors and biasing using resistors. Preferably, the Q-value of the oscillator is not affected by the biasing components. If the Q-value is affected, the Q-value including the bias network should be used during calculations where the Q-value is needed.

Unfiltered Bias Current for Differential Pairs

We assume the phase shift of the active part, ζ, to be unaffected by the noise from the current bias. If this assumption is not fulfilled, we need the complete ISF for the current bias noise source including the sensitivity for ζ with respect to the bias current.

The phase noise due to noise in the current bias for differential stages could be calculated either using the ISF of Section 8.5 or by transforming the noise source to a corresponding noise source at the output of the active part. Here we choose to use the latter method.

The spectral density of the equivalent noise source located at the output of the active part, f, as a function of time, t, is given by

$$S_{y,b}(t) = A_i(t)^2 S_b \tag{7.33}$$

where A_i is the instantaneous small-signal current gain from the bias current to the output of the active part, given for differential pairs based on bipolar transistors and field-effect transistors in Appendix C. The noise spectral density for the bias current source is denoted S_b.

The averaged noise spectral density is

$$S_{\overline{y},b} = \overline{\Gamma_y(\omega_0 t)^2 A_i(t)^2 S_b}, \tag{7.34}$$

where the over-line is used to denote time averaging. Assuming that the fundamental component for the ISF for noise entering at the output of the active part is dominant, we get the averaged noise spectral density as

$$S_{\overline{y},b} \approx \left(\Re[\Gamma_{y,1}]^2 \left(\frac{A_0}{2} + \frac{A_2}{4} \right) + \Im[\Gamma_{y,1}]^2 \left(\frac{A_0}{2} - \frac{A_2}{4} \right) \right) S_b, \tag{7.35}$$

where we write the squared small-signal current gain as a Fourier series according to

$$A_i(t)^2 = \sum_{n=0}^{\infty} A_n \cos(n\omega_0 t). \tag{7.36}$$

The two factors

$$K_{re} = \frac{A_0}{2} + \frac{A_2}{4} \tag{7.37}$$

and

$$K_{im} = \frac{A_0}{2} - \frac{A_2}{4} \tag{7.38}$$

are plotted as function of the input amplitude to the active block, both for FET and BJT differential pairs, in Appendix C. Each of the two factors K_{re}

and K_{im} has an upper limit of 1/8. Hence, an upper limit of the averaged spectral density is given by

$$S_{\overline{y},b} \approx \left(K_{re}\Re[\Gamma_{y,1}]^2 + K_{im}\Im[\Gamma_{y,1}]^2\right) S_b \leq \frac{S_b}{8}|\Gamma_{y,1}|^2, \tag{7.39}$$

where the equality is reached as the input amplitude goes to infinity, *i.e.* instantaneous switching of the differential pair. In this extreme case half the bias noise ends up as differential noise at the output of the active part; the other half ends up as common-mode noise.

The noise spectral density, S_b, for a current-source transistor is given by

$$S_b = 4k_BT\gamma g_{m,b}, \tag{7.40}$$

where $g_{m,b}$ is the transconductance for the current-source transistor. The noise spectral density for a current-determining resistor, R_B, is given by

$$S_b = 4k_BT\frac{1}{R_B}. \tag{7.41}$$

The averaged noise spectral density for a transistor-based current source is

$$S_{\overline{y},b}(\omega_m) = 4k_BT\gamma g_{m,b}\left(K_{re}\Re[\Gamma_{y,1}]^2 + K_{im}\Im[\Gamma_{y,1}]^2\right) \tag{7.42}$$

and for a resistor-based current source it is

$$S_{\overline{y},b}(\omega_m) = \frac{4k_BT}{R_B}\left(K_{re}\Re[\Gamma_{y,1}]^2 + K_{im}\Im[\Gamma_{y,1}]^2\right). \tag{7.43}$$

Rewriting the expression for the averaged noise spectral density of a transistor-based current source, we get

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}2\gamma g_{m,b}\Re[Z_{11}]\left(K_{re} + K_{im}\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\right), \tag{7.44}$$

and for a resistor-based current source, we get

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{2\Re[Z_{11}]}{R_B}\left(K_{re} + K_{im}\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\right). \tag{7.45}$$

In a technology using bipolar transistors, a current-source transistor has a transconductance of $g_{m,b} = 4G_m$ since it conducts twice as much current as one of the transistors in the differential pair when in equilibrium and the small-signal transconductance for the differential stage, G_m, is half the transconductance of one of the transistors in the differential pair in equilibrium.

Unfiltered Bias Current at Output

A white noise source situated at the input to the feedback network can be treated in the same way as the noise from the active part. The averaged spectral density is given by

$$S_{\overline{y},b} \approx \frac{1}{2}|\Gamma_{y,1}|^2 S_{y,b}, \tag{7.46}$$

where $S_{y,b}$ is the noise spectral density for the bias.

A transistor used as bias current source will have an averaged noise spectral density of

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\gamma g_{m,b}\Re[Z_{11}]\left(1+\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\right), \tag{7.47}$$

where $g_{m,b}$ is the transconductance of the bias transistor. A bias resistor, R_B, gives an averaged noise spectral density of

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{\Re[Z_{11}]}{R_B}\left(1+\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\right). \tag{7.48}$$

Unfiltered Bias Current at Input

The averaged noise spectral density for a voltage noise source at the input to the active block is given by

$$S_{\overline{x},b} \approx \frac{1}{2}|\Gamma_{x,1}|^2 S_{x,b} \tag{7.49}$$

where Γ_x is the ISF for noise entering at the input to the active block and S_x is the noise spectral density. We can rewrite the ISF using

$$\Im[\Gamma_{x,1}] = \frac{\Im[\Gamma_{y,1}]}{\widetilde{H}_1} = \frac{\Im[\Gamma_{y,1}]}{Z_{21}} \tag{7.50}$$

and

$$\Re[\Gamma_{x,1}] = \frac{\Re[\Gamma_{y,1}]}{\widetilde{H}^{(I)}_{\Delta,1}} = \frac{\Re[\Gamma_{y,1}]}{\widetilde{Z}^{(I)}_{\Delta,21}} \tag{7.51}$$

using (8.68) and (8.69) and where $\widetilde{Z}^{(I)}_{\Delta,21} = \widetilde{H}^{(I)}_{\Delta,1}$.

We assume that the output impedance for signals in quadrature phase with the input to the active block is equal to Z_{22}, and that the output impedance for signals in phase with the input to the active block is equal to $Z^{(I)}_{\Delta,22}$. Using these two output impedances and assuming that the input

current noise is white, we rewrite the noise current source with spectral density S_b into two noise voltage sources at the input to the active part: one in quadrature phase with the oscillator with noise voltage spectral density

$$S_{x,b}^{(Q)} = |Z_{22}|^2 S_b, \tag{7.52}$$

and one in phase with the oscillator with noise voltage spectral density

$$S_{x,b}^{(I)} = |Z_{\Delta,22}^{(I)}|^2 S_b. \tag{7.53}$$

The averaged spectral density can be written as

$$S_{\overline{x},b} = \frac{1}{2}\left(\Im[\Gamma_{x,1}]^2 S_{x,b}^{(Q)} + \Re[\Gamma_{x,1}]^2 S_{x,b}^{(I)}\right), \tag{7.54}$$

which can be expressed as

$$S_{\overline{x},b} = \frac{1}{2}\left(|Z_{22}|^2\Im[\Gamma_{x,1}]^2 + |Z_{\Delta,22}^{(I)}|^2\Re[\Gamma_{x,1}]^2\right) S_b, \tag{7.55}$$

using (7.52) and (7.53). Rewriting this expression in terms of $\Gamma_{y,1}$, we get

$$S_{\overline{x},b} \approx \frac{1}{2}\left(\frac{|Z_{22}|^2}{Z_{21}^2}\Im[\Gamma_{y,1}]^2 + \frac{|Z_{\Delta,22}^{(I)}|^2}{\left(Z_{\Delta,21}^{(I)}\right)^2}\Re[\Gamma_{y,1}]^2\right) S_b, \tag{7.56}$$

using (7.50) and (7.51). Assuming that

$$\frac{|Z_{22}|}{Z_{21}} \approx \frac{|Z_{\Delta,22}^{(I)}|}{Z_{\Delta,21}^{(I)}}, \tag{7.57}$$

a final rewriting gives

$$S_{\overline{x},b} \approx \frac{2k_B T\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\gamma g_{m,b}\Re[Z_{11}]\frac{|Z_{22}|^2}{Z_{21}^2}\left(1 + \frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\right) \tag{7.58}$$

when the current source is a transistor with transconductance $g_{m,b}$ and

$$S_{\overline{x},b} \approx \frac{2k_B T\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{\Re[Z_{11}]}{R_B}\frac{|Z_{22}|^2}{Z_{21}^2}\left(1 + \frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\right) \tag{7.59}$$

when the bias current source is a resistor R_B.

Filtered Bias Current

Since the bias current is low-pass filtered, it does no longer possess a white spectrum. The averaged noise spectrum for a noise source having a low-pass spectrum is given in Section 7.3.3 which treats bias sources having 1/f noise. The averaged noise spectral density is given by (7.89) as

$$S_{\overline{w},b}(\omega_m) = \frac{|Y_1|^2}{4}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right)^2 S_{w,b}(\omega_m), \tag{7.60}$$

where $S_{w,b}$ is the noise spectral density for the bias current source.

A transistor used as bias current source has an averaged noise spectral density of

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{\gamma g_{m,b}\Re[Z_{11}]}{2}\left(\frac{\partial \zeta}{\partial W_0}|Y_1| + \frac{\Re[\Gamma_{y,1}]}{\Im[\Gamma_{y,1}]}\frac{\partial B}{\partial W_0}|X_1|\right)^2, \tag{7.61}$$

where $g_{m,b}$ is the transconductance of the bias transistor. A bias resistor, R_B, gives an averaged noise spectral density of

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{\Re[Z_{11}]}{2R_B}\left(\frac{\partial \zeta}{\partial W_0}|Y_1| + \frac{\Re[\Gamma_{y,1}]}{\Im[\Gamma_{y,1}]}\frac{\partial B}{\partial W_0}|X_1|\right)^2. \tag{7.62}$$

Under the assumption that $\frac{\partial \zeta}{\partial W_0} \approx 0$ we get

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{\gamma g_{m,b}\Re[Z_{11}]}{2}\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\left(\frac{\partial B}{\partial W_0}\right)^2|X_1|^2 \tag{7.63}$$

when a transistor is used as bias source, and

$$S_{\overline{y},b}(\omega_m) = \frac{2k_BT\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}\frac{\Re[Z_{11}]}{2R_B}\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}\left(\frac{\partial B}{\partial W_0}\right)^2|X_1|^2 \tag{7.64}$$

when a resistor is used as bias source. In both cases we have that

$$\frac{\partial B}{\partial W_0}|X_1| \leq \frac{2}{\pi} \tag{7.65}$$

for a differential pair, where the equality is reached when the transistors in the differential pair are switching instantaneously, and

$$\frac{\partial B}{\partial W_0}|X_1| \leq 2 \tag{7.66}$$

for a single transistor, where the equality is reached when the transistor is operating in deep Class C.

7.2.6 Total Noise

Summing up the contributions of all white noise sources, we write the total averaged noise spectral density as

$$S_{\overline{y},tot}(\omega_m) \approx \frac{2k_BTF\Im[\Gamma_{y,1}]^2}{\Re[Z_{11}]}, \tag{7.67}$$

where

$$F \approx 1+\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}+\gamma\frac{\Re[Z_{11}]}{|Z_{21}|}+\gamma\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2}|\widetilde{G}^{(I)}_{\Delta,1}|\Re[Z_{11}]+K_1K_2+K_1K_3\frac{\Re[\Gamma_{y,1}]^2}{\Im[\Gamma_{y,1}]^2} \tag{7.68}$$

is the noise factor.

This noise factor can be rewritten as

$$F \approx 1+\gamma\frac{\Re[Z_{11}]}{|Z_{21}|}+K_1K_2+K^2_{AM-PM}\left(1+\gamma|\widetilde{G}^{(I)}_{\Delta,1}|\Re[Z_{11}]+K_1K_3\right), \tag{7.69}$$

where K_{AM-PM} is the AM-to-PM conversion factor defined as

$$K_{AM-PM}=\frac{\Re[\Gamma_{y,1}]}{\Im[\Gamma_{y,1}]}. \tag{7.70}$$

The constant K_1 depends on the bias current noise source and is given by

$$K_1=\gamma g_{m,b}\Re[Z_{11}] \tag{7.71}$$

for a bias transistor with transconductance $g_{m,b}$ and

$$K_1=\frac{\Re[Z_{11}]}{R_B} \tag{7.72}$$

for a bias resistor R_B.

The constants K_2 and K_3 depend on where the bias current is located and are given by

$$K_2=\begin{cases} 2K_{im}\leq\frac{1}{4} & \text{differential pair tail bias}\\ 1 & \text{bias at output}\\ \frac{|Z_{22}|^2}{Z_{21}^2} & \text{bias at input}\end{cases} \tag{7.73}$$

and

$$K_3=\begin{cases} 2K_{re}\leq\frac{1}{4} & \text{differential pair tail bias}\\ 1 & \text{bias at output}\\ \frac{|Z_{22}|^2}{Z_{21}^2} & \text{bias at input}\end{cases} \tag{7.74}$$

From (8.66) in Chapter 8 we have that

$$\Im[\Gamma_{y,1}] \approx \frac{\omega_0}{|Y_1|Q} \tag{7.75}$$

and from (7.1) we get the phase noise as

$$\mathcal{L}[\omega_m] \approx \frac{S_{\overline{y}}(\omega_m)}{2\omega_m^2} \approx \frac{k_B T F}{2P_1 Q^2} \frac{\omega_0^2}{\omega_m^2}, \tag{7.76}$$

where we have used (7.75), (7.67) and where

$$P_1 = \frac{\Re[Z_{11}]|Y_1|^2}{2} \tag{7.77}$$

is the fundamental power delivered to the feedback network, h. This expression for the single-sided phase noise is equal to the one given by Leeson [Leeson, 1966], with the noise factor given by (7.69).

A theoretical lower limit for the noise factor is given by

$$F \geq 1 + \gamma \tag{7.78}$$

for active blocks where the input-voltage amplitude to the active block does not exceed the output-voltage amplitude of the active block. If higher input-voltage amplitude is allowed, the theoretical lower limit for the noise factor, F, is unity, where the phase noise is limited by the noise from the feedback network, h, alone.

7.3 Phase Noise due to 1/f Noise

The 1/f noise originates from imperfections in the components and depends on the technology. The spectral density for these noise sources is approximately inversely proportional to the frequency.

The averaged noise spectral density due to 1/f noise is given by

$$S_{\overline{y}}(\omega_m) = \left(\overline{\Gamma_y(\omega_0 t) \sqrt{S_y(\omega_m, t)}} \right)^2 \tag{7.79}$$

where $S_y(\omega_m, t)$ is the noise spectral density at offset angular frequency ω_m at time instant t [Hajimiri and Lee, 1998]. However, this expression is not valid at very small frequency offsets [Klimovitch, 2000], but we are seldom interested in the phase noise at such small frequency offsets.

In the special case when S_y is constant with time, (7.79) simplifies to

$$S_{\overline{y}}(\omega_m) = \Gamma_{y,0}^2 S_y(\omega_m). \tag{7.80}$$

7.3.1 Noise from Feedback Network

We assume that the feedback network has negligible 1/f noise compared to the active devices. Noise entering at the tuning port is not dealt with in this chapter since it does not originate from the oscillator core.

7.3.2 Noise from Active Network

The transistors in the active network contribute a considerable amount of 1/f noise, which is converted into phase noise through several mechanisms. In addition to modulating the active part itself, as treated below, it may contribute by direct low-frequency modulation of varactors which gives additional phase noise.

We now consider the case where the 1/f noise modulates the active part. We assume that the emitter/source terminal sees a high impedance at low frequencies, *i.e.* the transistor or differential pair is biased by a current at this node. We also assume that the other nodes, *i.e.* base/gate and collector/drain terminals, are at low impedance at low frequencies, which means they have fixed low-frequency voltage potentials. We also assume that noise components at frequencies higher than the oscillation frequency are filtered out by the feedback network.

We now move the 1/f noise sources from between base–emitter and drain–source, as described in Appendix C, to be parallel with the bias current. The noise spectral density for the low-frequency components in the BJT case is given by

$$S_{w,f}(\omega_m) \approx \frac{2\pi K_{1/f}}{\omega_m} \frac{I_{DC}}{\beta}, \tag{7.81}$$

using (C.18), where I_{DC} is the bias current which is approximately equal to the collector current if the current amplification factor, β, is large. We arrive at this expression both for single transistors by considering the DC value of the current only and for differential pairs where we add the two contributions to get a constant noise spectral density with time. The noise spectral density for the low-frequency components in the FET case is given by

$$S_{w,f}(\omega_m) \approx \frac{2\pi K_{1/f}}{\omega_m} I_{DC}, \tag{7.82}$$

using (C.32), where I_{DC} is the bias current.

Considering the low-frequency components only, the averaged noise spectral density is given by

$$S_{\overline{w},f}(\omega_m) \approx \Gamma_{w,0}^2 S_{w,f}(\omega_m), \tag{7.83}$$

where $S_{w,f}$ is the noise spectral density given above, and $\Gamma_{w,0}$ is the DC component of the ISF for the current source given by

$$\Gamma_{w,0} = \frac{|Y_1|}{2}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right) \tag{7.84}$$

according to (8.87) in Chapter 8. Combining these two expressions, we get the averaged noise spectral density as

$$S_{\overline{w},f}(\omega_m) = \frac{|Y_1|^2}{4}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right)^2 S_{w,f}(\omega_m). \tag{7.85}$$

Finally, by inserting (7.81) or (7.82) in (7.85) we get

$$S_{\overline{w},f}(\omega_m) = \frac{|Y_1|^2}{4}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right)^2 \frac{2\pi K_{1/f,f} I_{DC}}{\omega_m}, \tag{7.86}$$

where $K_{1/f,f} = \frac{K_{1/f}}{\beta}$ for a BJT implementation and $K_{1/f,f} = K_{1/f}$ for an FET implementation.

7.3.3 Noise from Biasing Network

In this section we treat low-frequency noise coming from the biasing network. The noise is assumed to have a spectral density, S_b, which is constant with time.

The averaged noise spectral density is given by

$$S_{\overline{w},b}(\omega_m) = \Gamma_{w,0}^2 S_b(\omega_m), \tag{7.87}$$

where S_b is the noise spectral density of the bias network controlling the bias current of the active network, and $\Gamma_{w,0}$ is the DC component of the ISF for the current source given by

$$\Gamma_{w,0} = \frac{|Y_1|}{2}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right) \tag{7.88}$$

according to (8.87) in Chapter 8. Combining these two expressions, we get the averaged noise spectral density as

$$S_{\overline{w},b}(\omega_m) = \frac{|Y_1|^2}{4}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right)^2 S_b(\omega_m). \tag{7.89}$$

Assuming that the noise spectral density of the bias network is proportional to the DC current, I_{DC}, supplied to the active part, we may write the noise spectral density as

$$S_b(\omega_m) = \frac{2\pi K_{1/f,b} I_{DC}}{\omega_m}, \tag{7.90}$$

where $K_{1/f,b}$ is a noise constant for the biasing network. The averaged noise spectral density may now be written as

$$S_{\overline{w},b}(\omega_m) = \frac{|Y_1|^2}{4}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right)^2 \frac{2\pi K_{1/f,b} I_{DC}}{\omega_m}. \tag{7.91}$$

The noise from the bias current network also contributes to the phase noise by another mechanism, via direct modulation of any nonlinear reactive components. This term may be added to the ISF for the bias current, $\Gamma_{w,0}$, if deemed significant.

Modulated Noise from Biasing Network

In some special cases of amplitude regulating circuits, the current noise source is voltage starved during a fraction of the oscillation period in order to decrease the average current. An example is the tail bias current for a differential stage where the common emitter/source node tracks the voltage waveform at the collector/drain nodes and may get lower than the voltage headroom needed for the current source to act as a current source. Consequently, the average current decreases, limiting the voltage amplitude. This modulation of the current source also modulates its noise sources, changing their frequency properties.

7.3.4 Total Noise

We sum the 1/f noise contribution from the active part, given in (7.86), with the contribution from the bias network, given by (7.91), to get the total averaged noise spectral density as

$$S_{\overline{w}}(\omega_m) = \frac{|Y_1|^2}{4}\left(\Re[\Gamma_{y,1}]\frac{1}{B}\frac{\partial B}{\partial W_0} + \Im[\Gamma_{y,1}]\frac{\partial \zeta}{\partial W_0}\right)^2 \frac{2\pi(K_{1/f,f} + K_{1/f,b})}{\omega_m} I_{DC}. \tag{7.92}$$

Inserting this expression in the expression for the phase noise, given by

$$\mathcal{L}[\omega_m] = \frac{S_{\overline{w}}(\omega_m)}{2\omega_m^2}, \tag{7.93}$$

we get the phase noise due to 1/f noise as

$$\mathcal{L}[\omega_m] = \frac{2\pi(K_{1/f,f} + K_{1/f,b})I_{DC}|Y_1|^2\Im[\Gamma_{y,1}]^2}{8\omega_m^3}\left(\frac{\Re[\Gamma_{y,1}]}{\Im[\Gamma_{y,1}]}\frac{1}{B}\frac{\partial B}{\partial W_0} + \frac{\partial\zeta}{\partial W_0}\right)^2. \tag{7.94}$$

We see that the 1/f noise has been upconverted to phase noise with a spectral density proportional to $1/f^3$. We can rewrite this expression using (7.70) and (7.75) as

$$\mathcal{L}[\omega_m] = \frac{2\pi(K_{1/f,f} + K_{1/f,b})I_{DC}}{8Q^2}\left(K_{AM-PM}\frac{1}{B}\frac{\partial B}{\partial W_0} + \frac{\partial\zeta}{\partial W_0}\right)^2\frac{\omega_0^2}{\omega_m^3}. \tag{7.95}$$

Sometimes it is of interest to know the corner frequency, $\omega_{m,1/f}$, between the phase noise obeying the $1/f^2$ spectrum and that obeying the $1/f^3$ spectrum. By equating (7.76) and (7.95), we get the corner frequency as

$$\omega_{m,1/f} = \frac{2\pi(K_{1/f,f} + K_{1/f,b})I_{DC}P_1}{4k_BTF}\left(K_{AM-PM}\frac{1}{B}\frac{\partial B}{\partial W_0} + \frac{\partial\zeta}{\partial W_0}\right)^2. \tag{7.96}$$

We see that in order to minimize phase noise due to 1/f noise we must choose components with low 1/f noise, minimize the AM-to-PM conversion, and minimize the phase sensitivity to bias current variations in the active part.

7.4 Phase Noise due to Disturbances

In addition to the noise sources treated so far, we have disturbances from the physical surrounding of the oscillator. These disturbances are usually deterministic, but may in some cases be treated as random in nature depending on the properties of the disturbances.

Examples of disturbances are noise on supply and ground lines, electric and magnetic fields coupling into the oscillator, and noise in the substrate of integrated circuits.

Depending on the properties of the disturbances, different ways to calculate the resulting spectra are appropriate. If the disturbance can be treated as a stochastic process with a given spectra, the methods used to calculate phase noise due to white noise or 1/f noise explained earlier in this chapter can be used. If the disturbance is a periodic signal, for example a sinusoid, the analysis of Section 7.5 can be used.

7.5 Injection Locking

If the frequency of a disturbance is close enough to one of the harmonics of the oscillator and the signal level of the disturbance is high enough, the oscillator may lock to the disturbing signal. We here calculate the injected level needed at a given frequency offset for an injection lock to occur. We assume that the injected signal strength is still low enough for the change in oscillation frequency to be linear with respect to the injected signal strength.

The input signal is a sinusoid according to

$$e(t) = E_n \cos(n(\omega_0 + \omega_\Delta)t), \tag{7.97}$$

where E_n is the input amplitude, ω_0 is the free-running frequency of the oscillator, and ω_Δ is the change in oscillation frequency when the oscillator has locked to the input signal.

We start with the differential equation describing the average input phase as a function of time given by

$$\frac{d\overline{\theta}}{dt} = \overline{\Gamma_e(\omega_0 t + \overline{\theta})e(t)}, \tag{7.98}$$

where $\overline{\theta}$ is the averaged phase, Γ_e is the Impulse Sensitivity Function (ISF) for the input signal e, and the over-line is used to denote time averaging. When the oscillator is in lock, we have

$$\overline{\theta}(t) = \omega_\Delta t + \varphi, \tag{7.99}$$

where φ is the phase difference between the oscillator signal and the input signal. Taking the derivative of this expression with respect to time, we get

$$\frac{d\overline{\theta}}{dt} = \omega_\Delta. \tag{7.100}$$

Inserting this expression in (7.98) and carrying out the averaging, we get the change in oscillation frequency as

$$\omega_\Delta = \frac{E_n \Re[\Gamma_n e^{jn\varphi}]}{2}. \tag{7.101}$$

Given the input amplitude, we see that the change in oscillation frequency must obey

$$|\omega_\Delta| < \frac{E_n |\Gamma_n|}{2} \tag{7.102}$$

in order for the oscillator to lock to the input signal. Given the change in oscillation frequency, the input amplitude must obey

$$E_n > \frac{2|\omega_\Delta|}{|\Gamma_n|} \tag{7.103}$$

in order for the oscillator to lock to the input signal.

If the input signal is not strong enough to make the oscillator lock, we need to solve the differential equation (7.98), which can be rewritten as

$$\frac{d\overline{\theta}}{dt} = \frac{E_n \Re[\Gamma_n e^{jn(\overline{\theta}-\omega_\Delta t)}]}{2} \tag{7.104}$$

for the input signal given in (7.97). If the oscillator does lock, this equation reduces to (7.101) when we use that the averaged phase is now described by (7.99).

7.5.1 Oscillator with Linear Feedback Network

As an example of an injection-locked oscillator, we assume that the feedback network is linear and that the input signal is injected at the input of the active block. For these assumptions, we have the frequency components of the ISF from (8.26) as

$$\Gamma_{e,n} = j\frac{n\widetilde{F}_n\omega_0}{X_1\widetilde{F}_1 Q}, \tag{7.105}$$

where X_1 is the fundamental amplitude at the input to the active part, Q is the Q-value of the oscillator and $\widetilde{F}_n$ are the describing functions for the active part, as defined in Appendix A. Concentrating on signals injected at frequencies close to the fundamental free-running oscillator, we only consider the fundamental component of the ISF, given as

$$\Gamma_{e,1} = j\frac{\omega_0}{X_1 Q}. \tag{7.106}$$

Inserting this expression in (7.101), we get the change in oscillation frequency as

$$\omega_\Delta = \frac{E_1 \Re[\Gamma_1 e^{j\varphi}]}{2} = -\frac{E_1\omega_0 \sin(\varphi)}{2X_1 Q}. \tag{7.107}$$

Rewriting this expression, we get the expression for the phase difference between the injected signal and the oscillator signal as

$$\sin(\varphi) = 2Q\frac{X_1}{E_1}\frac{\omega_\Delta}{\omega_0}. \tag{7.108}$$

Since the left-hand side must have an absolute value less than unity, the input amplitude E_1 must fulfill

$$\frac{E_1}{X_1} > 2Q\frac{|\omega_\Delta|}{\omega_0}. \tag{7.109}$$

These two last expressions agree with those given by Adler [Adler, 1946]. There is, however, a sign inversion due to the difference in definition of frequency offset.

When the oscillator does not lock to the injected signal, we have to calculate the averaged phase by inserting (7.106) in (7.104), and the differential equation to solve is now given by

$$\frac{d\overline{\theta}}{dt} = \frac{E_1\Re[\Gamma_1 e^{j(\overline{\theta}-\omega_\Delta t)}]}{2} = -\frac{E_1\omega_0\sin(\overline{\theta}-\omega_\Delta t)}{2X_1Q}. \tag{7.110}$$

This nonlinear differential equation describing the phase evolution with time has been solved by Stover [Stover, 1966]. For an injected signal, $e(t)$, which is much smaller than the oscillator signal, $x(t)$, we get two dominant sidebands at frequency offset $|\omega_\Delta|$ from the free-running frequency ω_0, with amplitudes $\frac{E_1}{4Q}\frac{\omega_0}{|\omega_\Delta|}$.

7.6 Summary

The phase-noise spectrum of an oscillator due to white noise was derived and the resulting expression as function of offset frequency, ω_m, is given by (7.76) as

$$\mathcal{L}[\omega_m] \approx \frac{S_{\overline{y}}(\omega_m)}{2\omega_m^2} \approx \frac{k_BTF}{2P_1Q^2}\frac{\omega_0^2}{\omega_m^2}, \tag{7.111}$$

where k_B is the Boltzmann constant, T is the absolute temperature, P_1 is the fundamental power dissipated in the feedback network, Q is Q-value of the oscillator, ω_0 is the oscillation frequency, and the noise factor, F, is given by (7.69).

From the expression for the noise factor, we can conclude that the phase noise is not strongly dependent on the operation of the transistors. As long as the AM-to-PM conversion, K_{AM-PM}, is much less than unity, the noise factor mainly depends on the voltage gain of the feedback network, the noise factor γ for the transistors, and the bias network.

We have also derived an expression for the corner frequency, $\omega_{m,1/f}$, between the $1/\omega_m^2$ region and the $1/\omega_m^3$ region, given in (7.96). We conclude that to minimize phase noise due to 1/f noise, we must choose components

with low 1/f noise, minimize the AM-to-PM conversion, and minimize the phase sensitivity to bias current variations in the active part.

Finally, the effect of injection locking due to disturbances has been evaluated. An expression for the minimum injected amplitude needed to achieve a lock as function of the offset frequency was derived using the method of Impulse Sensitivity Functions (ISFs).

Chapter 8

Impulse Sensitivity Functions

In this chapter, I show how one can obtain approximate expressions for the Impulse Sensitivity Functions (ISFs) of oscillators using a new method based on Describing Functions (DFs). I also derive the ISFs needed to calculate the phase noise and sensitivity to disturbances for a general oscillator modeled as a feedback system.

8.1 Introduction

The Impulse Sensitivity Function (ISF) was proposed by Hajimiri and Lee [Hajimiri and Lee, 1998] as a means for calculating the oscillator phase noise. A way to calculate the ISFs numerically in simulators was then also proposed, where a noise impulse is injected and the resulting phase shift is measured in a transient analysis. Numerical simulation cannot, however, provide the insight a closed-form analytical expression does.

Exact analytical calculation of the ISF has been performed for simple systems [Falk and Schwarz, 2000, Falk and Schwarz, 2003, Zhang et al., 2004], but the calculation is often too cumbersome and often restricted to specific topologies, such as those which can be described as second-order systems. An approximative way to calculate the ISFs for an oscillator based on the derivatives of the signal waveform has also been proposed [Hajimiri and Lee, 1998]. This method is, however, limited to the case where no AM-to-PM conversion of noise occurs within the oscillator.

In this chapter, we introduce a method for calculating the ISF which yields simple expressions at the expense of some accuracy. The method is based on the describing-function method [Atherton, 1975, Gelb and Velde, 1968]. The method gives valid results when the feedback network in the

oscillator is of bandpass character, that is, in oscillators with a relatively high Q-value. Errors related to this assumption are discussed in Chapter 9 where calculations are compared to simulations. A short introduction to Describing Functions (DFs) and Incremental Describing Functions (IDFs) is given in Appendix A.

8.1.1 Definition of Impulse Sensitivity Function

Before continuing with the derivation of Impulse Sensitivity Functions (ISFs), we first need to define the ISF. The differential equation describing the phase evolution with time, t, when a small input signal, e, is applied is given by

$$\frac{d\theta(t)}{dt} = \Gamma_e(\omega_0 t + \theta(t))e(t), \tag{8.1}$$

where θ is the phase, Γ_e is the periodic impulse sensitivity function with a periodicity of 2π, and ω_0 is the oscillation frequency of the undisturbed oscillator.

The definition of the ISF used in this thesis differs slightly from the one used in earlier work [Hajimiri and Lee, 1998, Vanassche et al., 2002]. The reason for using a different formulation is only that the definition used here is convenient both when we derive the ISFs and when we use these ISFs in calculations in other chapters. The formulation used here is similar to that of the Perturbation Projection Vector (PPV) [Demir, 1998, Demir et al., 2000], based on earlier work by Kärtner [Kaertner, 1990]. Analytical expressions for PPVs have been derived for simple systems [Ghanta et al., 2004], with similar restrictions as for the ISFs mentioned above. The difference between the use of ISFs and PPVs when evaluating oscillator performance has been discussed elsewhere [Vanassche et al., 2002].

8.2 Method of Derivations

The key idea behind the derivations is to calculate the frequency of an injection-locked oscillator using describing functions and impulse sensitivity functions, respectively, and then equate these expressions to get the ISFs in terms of DFs. A feedback model for the oscillator with the injected signal e is shown in Figure 8.1.

In the calculations to follow, we assume the input signal e to be a small-signal sinusoid with a frequency very close to one of the harmonics of the free-running oscillator. If the frequency of the input is close enough to a multiple of the free-running frequency and the signal strength is high enough,

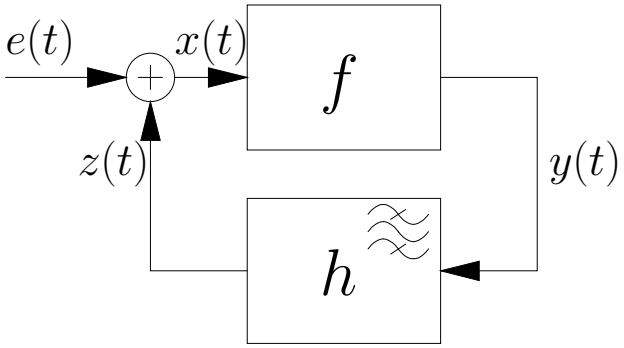


Figure 8.1: Time-domain model of a feedback system with added input signal e at the input to the active block.

the oscillator locks to the input e and the oscillator frequency changes from the free-running frequency ω_0 to the frequency $\omega = \omega_0 + \omega_\Delta$ of the input. We choose the input level and frequency offset, ω_Δ, arbitrarily small such that we may approximate the changes in oscillation frequency and gain of blocks to be linear with respect to the input level.

First, we use the describing function method to calculate the frequency offset, ω_Δ. General describing functions have previously been used to calculate injection locking with arbitrary injected input amplitude [Gustafsson et al., 1972, Jeżewski, 1974], but since we are only interested in injected signals of low amplitude, we may use the simpler Incremental Describing Functions (IDFs) [Atherton, 1975]. The definition and calculation of IDFs are described in Appendix A.2. The incremental feedback model is shown in Figure 8.2, where $\widetilde{F}_\Delta$ and $\widetilde{H}_\Delta$ are the IDFs of the active part and feedback part, respectively.

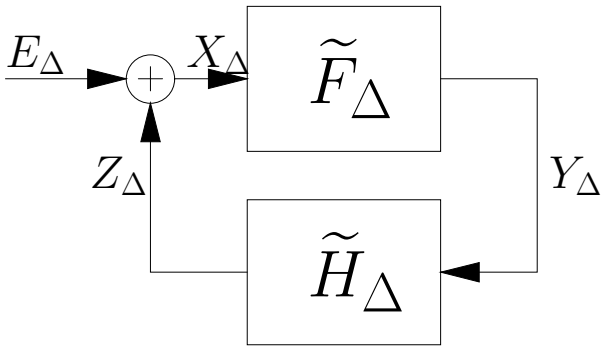


Figure 8.2: Frequency-domain model of a feedback system using the incremental describing functions $\widetilde{F}_\Delta$ and $\widetilde{H}_\Delta$.

Next, we use the ISF to calculate the frequency offset. We begin with the

differential equation describing the phase evolution with time as

$$\frac{d\theta(t)}{dt} = \Gamma_e(\omega_0 t + \theta(t))e(t), \tag{8.2}$$

where Γ_e is the ISF for input e and θ is the phase. Using the method of averaging [Vanassche et al., 2002], we can rewrite the differential equation as

$$\frac{d\bar{\theta}(t)}{dt} = \overline{\Gamma_e(\omega_0 t + \bar{\theta}(t))e(t)} = \omega_\Delta, \tag{8.3}$$

where $\bar{\theta}$ is the averaged phase.

Finally, we equate the two expressions for the frequency offset to get the ISF in terms of DFs. Since the ISF is periodic we may write it as a Fourier series according to

$$\Gamma_e(\tau) = \Re\left[\sum_{n=0}^{\infty} \Gamma_{e,n} e^{jn\tau}\right], \tag{8.4}$$

where $\Gamma_{e,n}$ is the complex amplitude of the ISF at the n:th harmonic. To simplify the calculation of the ISF in terms of DFs, we calculate each component of this Fourier series separately.

Once the impulse sensitivity function has been calculated for an input port k, impulse sensitivity functions from any port l, which has a linear transfer function to port k, can be calculated as

$$\Gamma_{l,n} = G^*_{kl}(jn\omega_0)\Gamma_{k,n} \tag{8.5}$$

where G^*_{kl} is the conjugate of the linear transfer function, G_{kl}, from port l to port k.

8.3 Linear Feedback Network and Memoryless Active Part

In this section we show how the ISF is calculated for a simple feedback system. We assume the feedback part to be linear and the active part to be memoryless, that is, the output, y, of the active part is an instantaneous function, $f(x)$, of its input, x.

8.3.1 Frequency Offset Calculation Using Describing Functions

Since the active part is memoryless the describing function for the active part, $\widetilde{F}_1$, is a real-valued function of the input amplitude, $|X_1|$, only. The

gain of the feedback part, $\widetilde{H}_1$, is a function of the oscillation frequency only and may be written in an amplitude–phase form as

$$\widetilde{H}_1 = H(j\omega) = A(\omega)e^{j\alpha(\omega)} \tag{8.6}$$

where $H(j\omega)$ is the linear gain of the feedback part h, A is the amplitude gain and α is the phase shift of the feedback part. We also have that $\alpha(\omega_0) = 0$ if $\widetilde{F}_1$ is positive and $\alpha(\omega_0) = \pi$ if $\widetilde{F}_1$ is negative, since the active part, f, is memoryless and thereby $\widetilde{H}_1$ must be real.

We now split the input disturbance to the active part, f, in an in-phase and a quadrature-phase component relative to X_1 according to

$$X_{\Delta,n} = X_{\Delta,n}^{(I)} + jX_{\Delta,n}^{(Q)} \tag{8.7}$$

for any possible harmonic component at a frequency n times higher than that of the fundamental. The incremental output, $Y_{\Delta,n}$, from the active block is described in the same way. Since the nonlinearity is memoryless, the phases of X_1 and Y_1 must be equal equal or differ by π.

We proceed with the calculation of the fundamental output $Y_{\Delta,1}$ as a function of the input components $X_{\Delta,n}$ using Incremental Describing Functions (IDFs). The gains for the in-phase and the quadrature-phase components of the IDFs, $\widetilde{F}_{\Delta n}$, are in general different and we have

$$\widetilde{F}_{\Delta,n}^{(I)} = \frac{\partial Y_n}{\partial |X_1|} = \widetilde{F}_n + X_1 \frac{\partial \widetilde{F}_n}{\partial |X_1|} \tag{8.8}$$

and, from Appendix A.2.2,

$$\widetilde{F}_{\Delta,n}^{(Q)} = n\widetilde{F}_n. \tag{8.9}$$

The in-phase output component of $Y_{\Delta,1}$ may now be calculated as

$$Y_{\Delta,1}^{(I)} = \sum_{n=0}^{\infty} X_{\Delta,n}^{(I)} \widetilde{F}_{\Delta,n}^{(I)} \tag{8.10}$$

and the quadrature-phase component as

$$Y_{\Delta,1}^{(Q)} = \sum_{n=0}^{\infty} X_{\Delta,n}^{(Q)} \widetilde{F}_{\Delta n}^{(Q)} = \sum_{n=0}^{\infty} X_{\Delta,n}^{(Q)} n\widetilde{F}_n. \tag{8.11}$$

We now consider the change in output from the linear feedback part, h, as a function of the change in oscillation frequency, ω, and get

$$\frac{\partial \widetilde{H}_1}{\partial \omega} = \left(\frac{1}{A}\frac{\partial A}{\partial \omega} + j\frac{\partial \alpha}{\partial \omega} \right) \widetilde{H}_1 \tag{8.12}$$

by taking the derivative of (8.6) with respect to ω. Since the feedback part is linear, the change in output from the feedback part, $Z_{\Delta,1}$, due to a change in oscillation frequency is simply

$$Z_{\Delta,1} = \omega_\Delta \frac{\partial \widetilde{H}_1}{\partial \omega} |Y_1|. \tag{8.13}$$

Using (8.13) and the property that the IDF of a linear part is simply the gain of that part, we calculate the in-phase and quadrature-phase components of the output from the feedback part, $Z_{\Delta,1}$, as

$$Z_{\Delta,1}^{(I)} = Y_{\Delta,1}^{(I)} \widetilde{H}_1 + \omega_\Delta |Y_1| \frac{\partial A}{\partial \omega} \tag{8.14}$$

and

$$Z_{\Delta,1}^{(Q)} = Y_{\Delta,1}^{(Q)} \widetilde{H}_1 + \omega_\Delta |X_1| \frac{\partial \alpha}{\partial \omega}, \tag{8.15}$$

respectively, since we have assumed that the feedback part, h, filters out all harmonics but the fundamental.

At the summing point, we have

$$X_{\Delta,1}^{(I)} = E_{\Delta,1}^{(I)} + Z_{\Delta,1}^{(I)}, \tag{8.16}$$

$$X_{\Delta,1}^{(Q)} = E_{\Delta,1}^{(Q)} + Z_{\Delta,1}^{(Q)}, \tag{8.17}$$

$$X_{\Delta,n}^{(I)} = E_{\Delta,n}^{(I)}, \tag{8.18}$$

and

$$X_{\Delta,n}^{(Q)} = E_{\Delta,n}^{(Q)}. \tag{8.19}$$

Solving the equation system given by (8.10), (8.11), (8.14), (8.15), (8.16), (8.17), (8.18), and (8.19), we arrive at the frequency offset, ω_Δ, as a function of the complex input amplitudes, $E_{\Delta,n}$.

8.3.2 Frequency Offset Calculation Using the ISF

We now calculate the frequency offset using the ISF according to (8.3) as

$$\omega_\Delta = \Gamma_{e,0} E_{\Delta,0} + \sum_{n=1}^{\infty} \frac{\Gamma_{e,n}^{(I)} E_{\Delta,n}^{(I)}}{2} + \sum_{n=1}^{\infty} \frac{\Gamma_{e,n}^{(Q)} E_{\Delta,n}^{(Q)}}{2}, \tag{8.20}$$

where we use that

$$\overline{\Gamma_{e,n}^{(I)} \cos(n(\omega_0 t + \bar{\theta})) E_{\Delta,n}^{(I)} \cos(n(\omega_0 t + \bar{\theta}))} = \frac{\Gamma_{e,n}^{(I)} E_{\Delta,n}^{(I)}}{2}, \tag{8.21}$$

$$\overline{\Gamma_{e,n}^{(Q)} \sin(n(\omega_0 t + \bar{\theta})) E_{\Delta,n}^{(Q)} \sin(n(\omega_0 t + \bar{\theta}))} = \frac{\Gamma_{e,n}^{(Q)} E_{\Delta,n}^{(Q)}}{2} \tag{8.22}$$

and where we also split the ISF in an in-phase and a quadrature-phase component relative to X_1 according to

$$\Gamma_{e,n} = \Gamma_{e,n}^{(I)} + j\Gamma_{e,n}^{(Q)}. \tag{8.23}$$

8.3.3 Equating the Expressions for the Frequency Offset

From the expressions for the frequency offset in terms of DFs from Section 8.3.1 and in terms of the ISF from Section 8.3.2, we may now calculate the ISF in terms of DFs. The in-phase and quadrature-phase components of each harmonic, n, of the ISF may now be calculated separately using the following method: First, set all components of E_Δ but $E_{\Delta,n}^{(I)}$ equal to zero and solve for $\Gamma_{e,n}^{(I)}$; and second, set all components of E_Δ but $E_{\Delta,n}^{(Q)}$ equal to zero and solve for $\Gamma_{e,n}^{(Q)}$. This decomposition is allowed since the equation system is linear.

Using this method, we get the components of the ISF as

$$\Gamma_{e,n} = -j\frac{2n\widetilde{F}_n}{X_1 \widetilde{F}_1 \frac{\partial \alpha}{\partial \omega}} \tag{8.24}$$

where we have taken the reference phase of x to be zero, *i.e.*, X_1 is real and positive.

Defining the Q-factor of the feedback filter, h, according to Appendix E, to be

$$Q = -\frac{\omega_0}{2}\frac{\partial \alpha}{\partial \omega}, \tag{8.25}$$

we can rewrite the components of the ISF as

$$\Gamma_{e,n} = j\frac{n\widetilde{F}_n \omega_0}{X_1 \widetilde{F}_1 Q}. \tag{8.26}$$

We see that the ISF is inversely proportional to the amplitude and to the Q-factor of the oscillator. We also notice that the sensitivity to disturbances at higher harmonics is proportional to the harmonic content in the output of the active part, f.

8.4 The General Case

When the feedback network is nonlinear, the derivations become more complicated. Therefore, only the DC and the fundamental components of the impulse sensitivity function are derived here; these components are the most important ones when calculating the phase noise.

The describing function for the fundamental component of the transfer function for the feedback network may be written in an amplitude–phase form as

$$\widetilde{H}_1(|X_1|,\omega) = A(|X_1|,\omega)e^{j\alpha(|X_1|,\omega)}, \tag{8.27}$$

where A and α are the amplitude gain and phase, respectively.

In a similar way we may write the describing function for the active part as

$$\widetilde{F}_1(|X_1|,\omega) = B(|X_1|,\omega)e^{j\zeta(|X_1|,\omega)}, \tag{8.28}$$

where B and ζ are the amplitude gain and phase, respectively.

We see that both the amplitude and the phase are functions of the input amplitude to the nonlinear blocks and the frequency of the input signal. The frequency dependency of the feedback network is obvious since it is designed to have a high frequency selectivity. The frequency dependence for the active part may come from, for example, charge transport delay in transistors when they operate at high frequencies.

Below, we derive incremental gains for the active part, f, and all references to input and output should be taken with respect to the active part. We write the output of the active block, f, on an amplitude–phase form according to

$$Y_1(|X_1|,\omega) = |Y_1(|X_1|,\omega)|e^{j\angle Y_1(|X_1|,\omega)} = \widetilde{F}_1 X_1. \tag{8.29}$$

The amplitude of the output signal, $|Y_1|$, is a function of the amplitude of the input signal, $|X_1|$, and not of the input-signal phase, $\angle X_1$. To simplify notation, we henceforth omit the dependency on the input amplitude and frequency.

The incremental gain of the active part, f, for an extra input signal orthogonal to that of the main input is

$$\frac{\partial Y_1}{\partial X_1^{(Q)}} = \widetilde{F}_1; \tag{8.30}$$

that is, an orthogonal incremental input, $X_{\Delta,1}^{(Q)}$, changes the input and output phases by the same amount and does not affect the input and output amplitudes as long as the incremental input signal amplitude is low.

On the other hand, an extra input in phase with the main input to the active part does change the input amplitude but not the input phase and the incremental gain is

$$\frac{\partial Y_1}{\partial X_1^{(I)}} = \frac{\partial Y_1}{\partial |X_1|}, \tag{8.31}$$

which may be rewritten using (8.29) and (8.28) as

$$\frac{\partial Y_1}{\partial |X_1|} = \frac{\partial |Y_1|}{\partial |X_1|} e^{j\angle Y_1} + j\frac{\partial \angle Y_1}{\partial |X_1|}|Y_1| e^{j\angle Y_1} = \left(\frac{\widetilde{F}_{\Delta,1}^{(I)}}{|Y_1|} + j\frac{\partial \zeta}{\partial |X_1|} \right) Y_1, \tag{8.32}$$

where

$$\widetilde{F}_{\Delta,1}^{(I)} = \frac{\partial |Y_1|}{\partial |X_1|} = B + |X_1| \frac{\partial B}{\partial |X_1|}. \tag{8.33}$$

We see that we have one component in phase with Y_1 and one in quadrature phase when an input in phase with X_1 is applied at the input to the nonlinear active part.

For an incremental DC input signal the conversion gain is

$$\frac{\partial Y_1}{\partial X_0} = \frac{\partial |Y_1|}{\partial X_0} e^{j\angle Y_1} + j\frac{\partial \angle Y_1}{\partial X_0}|Y_1| e^{j\angle Y_1} = \left(\frac{\widetilde{F}_{\Delta,0}}{|Y_1|} + j\frac{\partial \zeta}{\partial X_0} \right) Y_1, \tag{8.34}$$

where

$$\widetilde{F}_{\Delta,0} = \frac{\partial |Y_1|}{\partial X_0} = |X_1| \frac{\partial B}{\partial X_0}. \tag{8.35}$$

For a DC input signal the incremental gain is

$$\frac{\partial Y_0}{\partial X_0} = \widetilde{F}_{\Delta,DC}. \tag{8.36}$$

We also look at the change in output signal with respect to a shift in input signal frequency and get

$$\frac{\partial Y_1}{\partial \omega} = X_1 \left(\frac{\partial B}{\partial \omega} e^{j\zeta} + j\frac{\partial \zeta}{\partial \omega} B e^{j\zeta} \right) = \left(\frac{1}{B}\frac{\partial B}{\partial \omega} + j\frac{\partial \zeta}{\partial \omega} \right) Y_1. \tag{8.37}$$

We split the input disturbance to the active part in an in-phase component and a quadrature-phase component, relative to X_1, according to

$$X_{\Delta,1} = X_{\Delta,1}^{(I)} + jX_{\Delta,1}^{(Q)} \tag{8.38}$$

and the output is described in the same way as

$$Y_{\Delta,1} = Y_{\Delta,1}^{(I)} + jY_{\Delta,1}^{(Q)}, \tag{8.39}$$

where in phase and quadrature phase is in relation to the signal Y_1.

Using (8.32), (8.34) and (8.37) we get the output in-phase component as

$$Y_{\Delta,1}^{(I)} = X_{\Delta,1}^{(I)} \widetilde{F}_{\Delta,1}^{(I)} + \omega_\Delta |X_1| \frac{\partial B}{\partial \omega} + X_{\Delta,0} \widetilde{F}_{\Delta,0}, \tag{8.40}$$

where we use that $|Y_1| = B|X_1|$.

Using (8.30), (8.32), (8.34) and (8.37) we get the output quadrature component as

$$Y_{\Delta,1}^{(Q)} = X_{\Delta,1}^{(I)} |Y_1| \frac{\partial \zeta}{\partial |X_1|} + X_{\Delta,1}^{(Q)} B + \omega_\Delta |Y_1| \frac{\partial \zeta}{\partial \omega} + X_{\Delta,0} |Y_1| \frac{\partial \zeta}{\partial X_0}. \tag{8.41}$$

Using (8.36) we also have

$$Y_{\Delta,0} = X_{\Delta,0} \widetilde{F}_{\Delta,DC}. \tag{8.42}$$

We repeat the derivations above for the feedback part. The expressions for the feedback part, h, look similar to those for the active part, f. We write the output of the feedback network in in-phase and quadrature-phase components in relation to X_1 as

$$Z_{\Delta,1} = Z_{\Delta,1}^{(I)} + j Z_{\Delta,1}^{(Q)} \tag{8.43}$$

and the in-phase component is calculated as

$$Z_{\Delta,1}^{(I)} = Y_{\Delta,1}^{(I)} \widetilde{H}_{\Delta,1}^{(I)} + \omega_\Delta |Y_1| \frac{\partial A}{\partial \omega} \tag{8.44}$$

and the quadrature-phase component is calculated to be

$$Z_{\Delta,1}^{(Q)} = Y_{\Delta,1}^{(I)} |X_1| \frac{\partial \alpha}{\partial |Y_1|} + Y_{\Delta,1}^{(Q)} A + \omega_\Delta |X_1| \frac{\partial \alpha}{\partial \omega}. \tag{8.45}$$

The external disturbance to the oscillator is also divided in its orthogonal components according to

$$E_{\Delta,1} = E_{\Delta,1}^{(I)} + j E_{\Delta,1}^{(Q)}, \tag{8.46}$$

where in phase and quadrature phase is in relation to X_1.

We write the summation at the input to the active part as

$$X_{\Delta,1}^{(I)} = E_{\Delta,1}^{(I)} + Z_{\Delta,1}^{(I)}, \tag{8.47}$$

$$X_{\Delta,1}^{(Q)} = E_{\Delta,1}^{(Q)} + Z_{\Delta,1}^{(Q)} \tag{8.48}$$

and

$$X_{\Delta,0} = E_{\Delta,0} + Z_{\Delta,0}. \tag{8.49}$$

We can now calculate the frequency shift, ω_Δ, by solving the equation system made up of (8.40), (8.41), (8.44), (8.45), (8.47), (8.48) and (8.49).

Finally, we equate the expression for ω_Δ we get by solving the equation system with the expression for ω_Δ from Section 8.3.2 using the method in Section 8.3.3. We then get the components of the ISF as

$$\begin{aligned}\Gamma_{x,0} = &-\frac{1}{\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\frac{1}{1-\widetilde{F}_{\Delta,DC}\widetilde{H}_{\Delta,DC}}\left(\widetilde{F}_{\Delta,DC}\frac{\partial\alpha}{\partial Y_0}+\frac{\partial\zeta}{\partial X_0}+\right.\\ &\left.+\frac{\widetilde{F}_{\Delta,0}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)+\widetilde{F}_{\Delta,DC}\widetilde{H}_{\Delta,0}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}\right)\times\\ &\times\frac{1}{1+\frac{|X_1|\frac{\partial B}{\partial\omega}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)+|Y_1|\frac{\partial A}{\partial\omega}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{\left(1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}\right)\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}}\end{aligned} \tag{8.50}$$

and

$$\begin{aligned}\Gamma_{x,1} = &-\frac{2}{|X_1|\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\frac{|X_1|\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}+j\right)\times\\ &\times\frac{1}{1+\frac{|X_1|\frac{\partial B}{\partial\omega}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)+|Y_1|\frac{\partial A}{\partial\omega}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{\left(1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}\right)\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}}.\end{aligned} \tag{8.51}$$

Noise entering at the output of the active part is calculated in a similar way to give the components of the ISF as

$$\begin{aligned}\Gamma_{y,0} = &-\frac{1}{\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\frac{1}{1-\widetilde{F}_{\Delta,DC}\widetilde{H}_{\Delta,DC}}\left(\widetilde{H}_{\Delta,DC}\frac{\partial\zeta}{\partial X_0}+\frac{\partial\alpha}{\partial Y_0}+\right.\\ &\left.+\frac{\widetilde{H}_{\Delta,0}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)+\widetilde{H}_{\Delta,DC}\widetilde{F}_{\Delta,0}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}\right)\times\\ &\times\frac{1}{1+\frac{|Y_1|\frac{\partial A}{\partial\omega}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)+|X_1|\frac{\partial B}{\partial\omega}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)}{\left(1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}\right)\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}}\end{aligned} \tag{8.52}$$

and

$$\Gamma_{y,1} = -\frac{2}{|Y_1|\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\frac{|Y_1|\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}+j\right)\times \\ \times\frac{1}{1+\frac{|Y_1|\frac{\partial A}{\partial\omega}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)+|X_1|\frac{\partial B}{\partial\omega}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)}{\left(1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}\right)\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}}. \tag{8.53}$$

8.4.1 Restricted Case

The expressions for the components of the ISF derived above are a bit complicated and somewhat hard to derive any insights from. We therefore simplify them by assuming that $\frac{\partial B}{\partial\omega}=0$ and $\frac{\partial A}{\partial\omega}=0$, that is, the amplitude gains of the blocks are independent of the frequency in the vicinity of the oscillation frequency. We also assume that $\widetilde{H}_{\Delta,0}\approx 0$ and $|\widetilde{F}_{\Delta,DC}\widetilde{H}_{\Delta,DC}|\ll 1$, that is, the conversion gain from low frequencies to the fundamental frequencies in the feedback part is low and the low-frequency loop gain is much lower than unity.

The expressions for the ISF components for noise entering at the input to the active part become

$$\Gamma_{x,0} = -\frac{1}{\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\widetilde{F}_{\Delta,DC}\frac{\partial\alpha}{\partial Y_0}+\frac{\partial\zeta}{\partial X_0}+\frac{\widetilde{F}_{\Delta,0}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}\right) \tag{8.54}$$

and

$$\Gamma_{x,1} = -\frac{2}{|X_1|\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\frac{|X_1|\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}+j\right). \tag{8.55}$$

The expressions for the ISF components for noise entering at the output of the active part become

$$\Gamma_{y,0} = -\frac{1}{\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\widetilde{H}_{\Delta,DC}\frac{\partial\zeta}{\partial X_0}+\frac{\partial\alpha}{\partial Y_0}+\frac{\widetilde{H}_{\Delta,DC}\widetilde{F}_{\Delta,0}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}\right) \tag{8.56}$$

and

$$\Gamma_{y,1} = -\frac{2}{|Y_1|\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\frac{|Y_1|\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}+j\right). \tag{8.57}$$

Sometimes it is more convenient to express the phase change as a function of the output of a block instead of as a function of the input to the block. In the case for the feedback block we have the relationships

$$\frac{\partial\alpha}{\partial X_0} = \widetilde{F}_{\Delta,DC}\frac{\partial\alpha}{\partial Y_0} + \frac{\widetilde{F}_{\Delta,0}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|} + \frac{\partial\alpha}{\partial|Y_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} \tag{8.58}$$

and

$$\frac{\partial\alpha}{\partial|X_1|} = \widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|} \tag{8.59}$$

and by using these relationships and the Q-value for the oscillator defined as

$$Q = -\frac{\omega_0}{2}\left(\frac{\partial\alpha}{\partial\omega} + \frac{\partial\zeta}{\partial\omega}\right), \tag{8.60}$$

we can rewrite the components of the ISF as

$$\Gamma_{x,0} = \frac{\omega_0}{2Q}\left(\frac{\partial\alpha}{\partial X_0} + \frac{\partial\zeta}{\partial X_0}\right) \tag{8.61}$$

and

$$\Gamma_{x,1} = \frac{\omega_0}{|X_1|Q}\left(\frac{|X_1|\left(\frac{\partial\alpha}{\partial|X_1|} + \frac{\partial\zeta}{\partial|X_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} + j\right). \tag{8.62}$$

A similar conversion can be done for the ISF at the output to the active block by using that

$$\frac{\partial\alpha}{\partial Y_0} = \widetilde{H}_{\Delta,DC}\frac{\partial\alpha}{\partial X_0} + \frac{\widetilde{H}_{\Delta,DC}\widetilde{F}_{\Delta,0}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|} + \frac{\partial\alpha}{\partial|Y_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} \tag{8.63}$$

and

$$\frac{\partial\alpha}{\partial|Y_1|} = \widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|X_1|} \tag{8.64}$$

and we get

$$\Gamma_{y,0} = \frac{\omega_0}{2Q}\left(\widetilde{H}_{\Delta,DC}\left(\frac{\partial\zeta}{\partial X_0} + \frac{\partial\alpha}{\partial X_0}\right)\right) \tag{8.65}$$

and

$$\Gamma_{y,1} = \frac{\omega_0}{|Y_1|Q}\left(\frac{|Y_1|\widetilde{H}^{(I)}_{\Delta,1}\left(\frac{\partial\alpha}{\partial|X_1|} + \frac{\partial\zeta}{\partial|X_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} + j\right). \tag{8.66}$$

Comparing (8.61) and (8.65), we get

$$\Gamma_{y,0} = \widetilde{H}_{\Delta,DC}\Gamma_{x,0}. \tag{8.67}$$

Comparing (8.62) and (8.66), we get

$$\Re[\Gamma_{y,1}] = \widetilde{H}^{(I)}_{\Delta,1}\Re[\Gamma_{x,1}] \tag{8.68}$$

and

$$\Im[\Gamma_{y,1}] = \widetilde{H}_1\Im[\Gamma_{x,1}]. \tag{8.69}$$

We define the AM-to-PM conversion factor, K_{AM-PM}, as

$$K_{AM-PM} = \frac{\Re[\Gamma_{y,1}]}{\Im[\Gamma_{y,1}]}. \tag{8.70}$$

Using (8.66), we get the AM-to-PM conversion factor as

$$K_{AM-PM} = \frac{|Y_1|\widetilde{H}^{(I)}_{\Delta,1}\left(\frac{\partial\alpha}{\partial|X_1|} + \frac{\partial\zeta}{\partial|X_1|}\right)}{1 - \widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}. \tag{8.71}$$

8.5 Disturbances Entering Through the Active and Feedback Parts

In many cases the noise does not enter as an additive component in the feedback network, but is modulated by the active part as in Figure 8.3. Examples of such noise are noise from the amplitude-determining network and noise from the biasing network.

To calculate the ISF for these noise sources, we have to calculate the transfer function from the source, w, to the output of the active network, f, in the IDF model of Figure 8.4. We assume that the fundamental component of the ISF at the output of the active network, f, is the dominant one.

8.5.1 Linear Feedback Network and Memoryless Active Part

The following method is used to calculate the ISF for noise entering through the active part: The frequency shift, ω_Δ, can be calculated using either the ISF for the input port w as

$$\omega_\Delta = \Gamma_{w,0}W_{\Delta,0} + \sum_{n=1}^{\infty}\frac{\Gamma^{(I)}_{w,n}W^{(I)}_{\Delta,n}}{2} + \sum_{n=1}^{\infty}\frac{\Gamma^{(Q)}_{w,n}W^{(Q)}_{\Delta,n}}{2}, \tag{8.72}$$

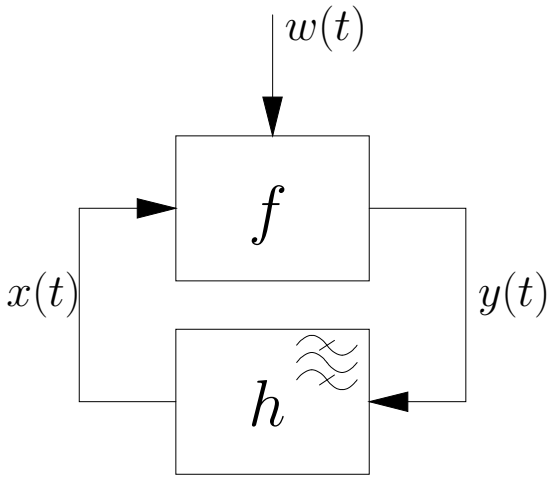


Figure 8.3: Time-domain model of a feedback system with added input signal w at the input to the active block.

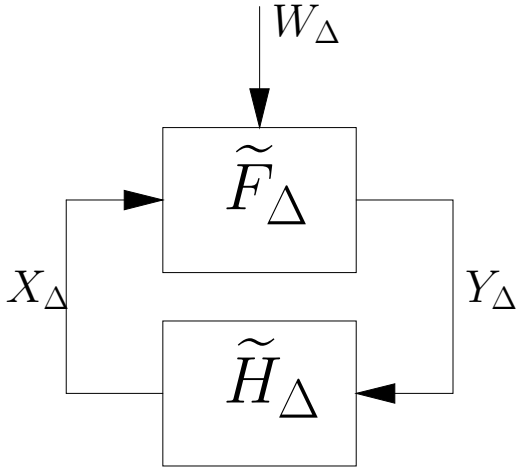


Figure 8.4: Frequency-domain model of a feedback system using the incremental describing functions $\widetilde{F}_\Delta$ and $\widetilde{H}_\Delta$.

or using the ISF for the output port y as

$$\omega_\Delta = \frac{\Gamma_{y,1}^{(I)} Y_{\Delta,1}^{(I)}}{2} + \frac{\Gamma_{y,1}^{(Q)} Y_{\Delta,1}^{(Q)}}{2}, \tag{8.73}$$

where we have assumed that the fundamental component of the ISF is dominant. Equating these two expression for the frequency offset, ω_Δ, gives us the ISF for noise at signal w in terms of the ISF for noise at signal y.

The output of the active block, y, is a function both of the input, x, and the bias signal, w, and can be written as

$$y = f(x, w). \tag{8.74}$$

By Taylor expanding this expression with respect to w, we get the incremental output signal, y_Δ, as

$$y_\Delta = \frac{\partial y(t)}{\partial w} w_\Delta, \tag{8.75}$$

where w_Δ is the incremental input signal. We denote the time-varying small-signal gain according to

$$d(t) = \frac{\partial y(t)}{\partial w}. \tag{8.76}$$

Since the input signal, $x(t)$, is a periodic signal with fundamental frequency ω_0, we can write the small-signal gain, $d(t)$, as a Fourier series according to

$$d(t) = \sum_{n=0}^{\infty} D_n \cos(n\omega_0 t). \tag{8.77}$$

First, we insert a signal w_Δ in phase and in quadrature phase in relation to the input signal, x, in (8.75), and use (8.76) and (8.77) to get the corresponding y_Δ. Second, we insert this expression for y_Δ in (8.73) and the value for w_Δ in (8.72) and equate these expressions for the frequency offset, which finally gives us the ISF for port w as

$$\Gamma_{w,0} = \frac{\Re[\Gamma_{y,1}] D_1}{2} \tag{8.78}$$

and

$$\Gamma_{w,n} = \frac{\Gamma_{y,1} D_{n-1}}{2} + \frac{\Gamma_{y,1}^* D_{n+1}}{2}. \tag{8.79}$$

Rewriting this expression as

$$\Gamma_{w,n} = \frac{\Re[\Gamma_{y,1}](D_{n-1} + D_{n+1})}{2} + j\frac{\Im[\Gamma_{y,1}](D_{n-1} - D_{n+1})}{2}, \tag{8.80}$$

we get the in-phase and quadrature-phase components of the ISF explicitly.

8.5.2 The General Case

We assume that high-frequency disturbances of w are filtered out so that the only important component of the input, w, is the low-frequency part around DC, $W_{\Delta,0}$.

The calculation is carried out in two steps: first, we calculate the conversion from the input, $W_{\Delta,0}$, to the output of the active block, $Y_{\Delta,1}$, and second, we calculate the ISF for noise entering through the input, w, using the ISF derived for noise at the output, y, in (8.53).

The conversion of low-frequency signals at the input to a fundamental component at the output is calculated using a Taylor expansion as

$$Y_{\Delta,1} = W_{\Delta,0}\frac{\partial Y_1}{\partial W_0} = W_{\Delta,0}\frac{\partial \widetilde{F}_1}{\partial W_0}X_1 = W_{\Delta,0}\left(\frac{\partial B}{\partial W_0}e^{j\zeta} + jB\frac{\partial \zeta}{\partial W_0}e^{j\zeta}\right)X_1, \tag{8.81}$$

where we have used (8.28) and (8.29).

This expression may be rewritten as

$$Y_{\Delta,1} = W_{\Delta,0}\left(\frac{1}{B}\frac{\partial B}{\partial W_0} + j\frac{\partial \zeta}{\partial W_0}\right)Y_1 \tag{8.82}$$

using (8.28) and we identify the in-phase component of the incremental output as

$$Y_{\Delta,1}^{(I)} = W_{\Delta,0}|Y_1|\frac{1}{B}\frac{\partial B}{\partial W_0} \tag{8.83}$$

and the quadrature-phase component of the incremental output as

$$Y_{\Delta,1}^{(Q)} = W_{\Delta,0}|Y_1|\frac{\partial \zeta}{\partial W_0}, \tag{8.84}$$

where in phase and quadrature phase are taken relative to Y_1.

The frequency shift, ω_Δ, can be calculated using either the ISF for the input port, w, as

$$\omega_\Delta = \Gamma_{w,0}W_{\Delta,0} \tag{8.85}$$

or using the ISF for the output port, y, as

$$\omega_\Delta = \frac{\Gamma_{y,1}^{(I)}Y_{\Delta,1}^{(I)}}{2} + \frac{\Gamma_{y,1}^{(Q)}Y_{\Delta,1}^{(Q)}}{2}, \tag{8.86}$$

assuming that the fundamental component of the ISF for noise entering at the output of the active part is dominant.

Equating these two expressions for the frequency offset, we get the ISF for port w as a function of the ISF for port y as

$$\Gamma_{w,0} = \frac{|Y_1|}{2}\left(\Gamma_{y,1}^{(I)}\frac{1}{B}\frac{\partial B}{\partial W_0} + \Gamma_{y,1}^{(Q)}\frac{\partial \zeta}{\partial W_0}\right), \tag{8.87}$$

where we have used (8.83) and (8.84). Using (8.53) we get the wanted ISF as

$$\begin{aligned}\Gamma_{w,0} = &-\frac{1}{\left(\frac{\partial \zeta}{\partial \omega}+\frac{\partial \alpha}{\partial \omega}\right)}\left(\frac{|X_1|\frac{\partial B}{\partial W_0}\left(\widetilde{H}_{\Delta,1}^{(I)}\frac{\partial \zeta}{\partial |X_1|}+\frac{\partial \alpha}{\partial |Y_1|}\right)}{1-\widetilde{F}_{\Delta,1}^{(I)}\widetilde{H}_{\Delta,1}^{(I)}}+\frac{\partial \zeta}{\partial W_0}\right)\times \\ &\times \frac{1}{1+\frac{|Y_1|\frac{\partial A}{\partial \omega}\left(\widetilde{F}_{\Delta,1}^{(I)}\frac{\partial \alpha}{\partial |Y_1|}+\frac{\partial \zeta}{\partial |X_1|}\right)+|X_1|\frac{\partial B}{\partial \omega}\left(\widetilde{H}_{\Delta,1}^{(I)}\frac{\partial \zeta}{\partial |X_1|}+\frac{\partial \alpha}{\partial |Y_1|}\right)}{\left(1-\widetilde{F}_{\Delta,1}^{(I)}\widetilde{H}_{\Delta,1}^{(I)}\right)\left(\frac{\partial \zeta}{\partial \omega}+\frac{\partial \alpha}{\partial \omega}\right)}},\end{aligned} \tag{8.88}$$

which under the assumptions that $\frac{\partial B}{\partial \omega} = 0$ and $\frac{\partial A}{\partial \omega} = 0$ simplifies to

$$\Gamma_{w,0} = -\frac{1}{\left(\frac{\partial \zeta}{\partial \omega}+\frac{\partial \alpha}{\partial \omega}\right)}\left(\frac{|X_1|\frac{\partial B}{\partial W_0}\left(\widetilde{H}_{\Delta,1}^{(I)}\frac{\partial \zeta}{\partial |X_1|}+\frac{\partial \alpha}{\partial |Y_1|}\right)}{1-\widetilde{F}_{\Delta,1}^{(I)}\widetilde{H}_{\Delta,1}^{(I)}}+\frac{\partial \zeta}{\partial W_0}\right). \tag{8.89}$$

Noise may also enter through the feedback part, h, via an input port, u, according to Figure 8.5. Signals entering to this passive part may for example come from a frequency tuning input port.

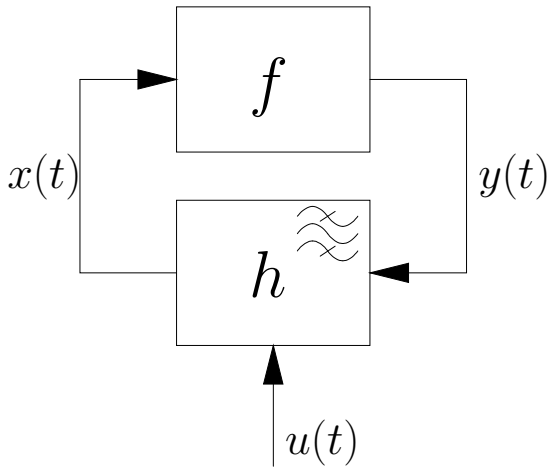


Figure 8.5: Time-domain model of a feedback system with added input signal u at the input to the feedback block.

The ISF for noise entering through this input port, u, can be calculated in a similar way to that of the port w. Carrying out these calculations, we get the ISF as

$$\Gamma_{u,0} = -\frac{1}{\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\frac{|Y_1|\frac{\partial A}{\partial U_0}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}+\frac{\partial\alpha}{\partial U_0}\right)\times \\ \times\frac{1}{1+\frac{|X_1|\frac{\partial B}{\partial\omega}\left(\widetilde{H}^{(I)}_{\Delta,1}\frac{\partial\zeta}{\partial|X_1|}+\frac{\partial\alpha}{\partial|Y_1|}\right)+|Y_1|\frac{\partial A}{\partial\omega}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{\left(1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}\right)\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}}, \tag{8.90}$$

which under the assumptions that $\frac{\partial B}{\partial\omega}=0$ and $\frac{\partial A}{\partial\omega}=0$ simplifies to

$$\Gamma_{u,0} = -\frac{1}{\left(\frac{\partial\zeta}{\partial\omega}+\frac{\partial\alpha}{\partial\omega}\right)}\left(\frac{|Y_1|\frac{\partial A}{\partial U_0}\left(\widetilde{F}^{(I)}_{\Delta,1}\frac{\partial\alpha}{\partial|Y_1|}+\frac{\partial\zeta}{\partial|X_1|}\right)}{1-\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}}+\frac{\partial\alpha}{\partial U_0}\right). \tag{8.91}$$

8.5.3 Other ISFs of Interest

In addition to the ISF calculations carried out in this chapter, we might want to calculate the other frequency components of the ISF for noise entering through the active part in the general case. These ISF components may be of interest if the phase shift of the active part is a function of the bias current or voltage, and the bias has high-frequency noise associated with it.

Chapter 9

Verification of Derived Expressions

The verification of the expressions derived in this thesis is carried out stepwise in this chapter. Discussion on the verification of the design methodology is given in Section 3.4.

First, I verify predicted performance against simulations where the active block is modeled as an ideal arc-tan nonlinearity in order to verify the approximations done in the derivation of the Impulse Sensitivity Function (ISF) and the derivation of the phase noise. This verification is performed both for linear and nonlinear feedback networks. Second, I verify the ISFs and the phase noise for an oscillator implemented with transistors. Finally, I verify predicted phase noise against measured data from many different topologies reported in literature.

9.1 Ideal Oscillator with Arc-tan Nonlinearity

The ideal oscillator used in the first set of verifications is a negative-conductance oscillator with a parallel LC tank, as shown in Figure 9.1.

The output current, y, as a function of the input voltage, x, is given by

$$y = f(x) = \frac{2y_{max}}{\pi} \arctan\left(\frac{\pi k x}{2y_{max}}\right), \tag{9.1}$$

and is plotted in Figure A.3 in Appendix A together with its derivative.

The component values are chosen to yield an oscillation frequency, f_0, of 1.0 GHz and a Q-value of 10. Maximum output current, y_{max}, is 20 mA and we have a small-signal transconductance, k, of 30 mS. The values for

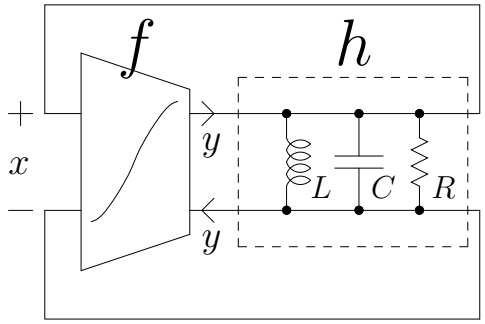


Figure 9.1: Schematic for an ideal oscillator.

the passive components are: $R = 100\ \Omega$, $L = 1.59154943$ nH, and $C = 15.9154943$ pF.

9.1.1 Linear Feedback Network

We begin by calculating the voltage amplitude for the fundamental frequency at the input to the nonlinearity. From (A.54) in Appendix A we have that the input-voltage amplitude is given by

$$X_1 = \frac{4y_{max}R}{\pi}\sqrt{1-\frac{1}{kR}}, \tag{9.2}$$

where we have used that

$$\widetilde{H}_1 = H(j\omega_0) = R. \tag{9.3}$$

We proceed with the calculation of the other harmonics by using (A.50) and

$$X_n = H(jn\omega_0)Y_n \tag{9.4}$$

where the parallel RLC tank has

$$H(jn\omega_0) = \frac{H(j\omega_0)}{1+jQ\frac{n^2-1}{n}} = \frac{R}{1+jQ\frac{n^2-1}{n}}. \tag{9.5}$$

The calculated values for the complex voltage amplitudes of the harmonics are given in Table 9.1 together with the simulated values and the magnitude errors in per cent. We note that the accuracy deteriorates for higher harmonics because the describing-function method neglects the presence of higher harmonics at the input of the nonlinearity.

Table 9.1: Complex amplitude of harmonics at input of nonlinearity.

	calculated	simulated	unit	error in mag.
X_1	$2079.2e^{j0}$	$2079.4e^{j0}$	[mV]	0.01%
X_3	$17.314e^{j1.608}$	$17.254e^{j1.610}$	[mV]	0.35%
X_5	$3.8495e^{-j1.550}$	$3.7869e^{-j1.526}$	[mV]	1.65%
X_7	$1.2833e^{j1.585}$	$1.2270e^{j1.677}$	[mV]	4.59%
X_9	$513.35e^{-j1.560}$	$462.62e^{-j1.305}$	[mV]	9.88%

To examine how the Q-value affects the accuracy of the calculations, we repeat the calculations for different Q-values ranging from 1 to 50 and plot the magnitude errors for the different harmonics in Figure 9.2. We note that we get small magnitude errors except when the Q-value is very low; especially the fundamental amplitude is well predicted.

We proceed with the calculation of the ISF for noise entering at the output of the transconductance using (8.26) and (8.5) of Chapter 8 given as

$$\Gamma_{y,n} = j\frac{n\widetilde{F}_n\omega_0 H^*(jn\omega_0)}{X_1\widetilde{F}_1 Q}, \tag{9.6}$$

where $\widetilde{F}_n$ is the describing function for the active part, f, given in (A.50) and $H(jn\omega_0)$ is given by (9.5). The different calculated frequency components of the ISF are given in Table 9.2 together with simulated results and resulting errors for the amplitude of the components in per cent.

The ideal oscillator was simulated using transient simulation with a noise impulse injected and the resulting phase error was extracted when the oscillator had eventually reached steady-state, as proposed by Hajimiri and Lee [Hajimiri and Lee, 1998].

Table 9.2: Frequency components of the impulse sensitivity function.

	calculated	simulated	unit	error in mag.
Γ_1	$30219e^{j1.571}$	$30408e^{j1.565}$	[Mrad/C]	0.62%
Γ_3	$754.95e^{-j0.037}$	$752.79e^{-j0.035}$	[Mrad/C]	0.29%
Γ_5	$279.75e^{j3.121}$	$278.76e^{j3.127}$	[Mrad/C]	0.36%
Γ_7	$130.56e^{-j0.015}$	$137.78e^{-j0.023}$	[Mrad/C]	5.24%
Γ_9	$67.150e^{j3.130}$	$66.903e^{j3.234}$	[Mrad/C]	0.37%

We also want to examine how different Q-values affect the approximation of the ISF, so we simulate the oscillator with different Q-values ranging

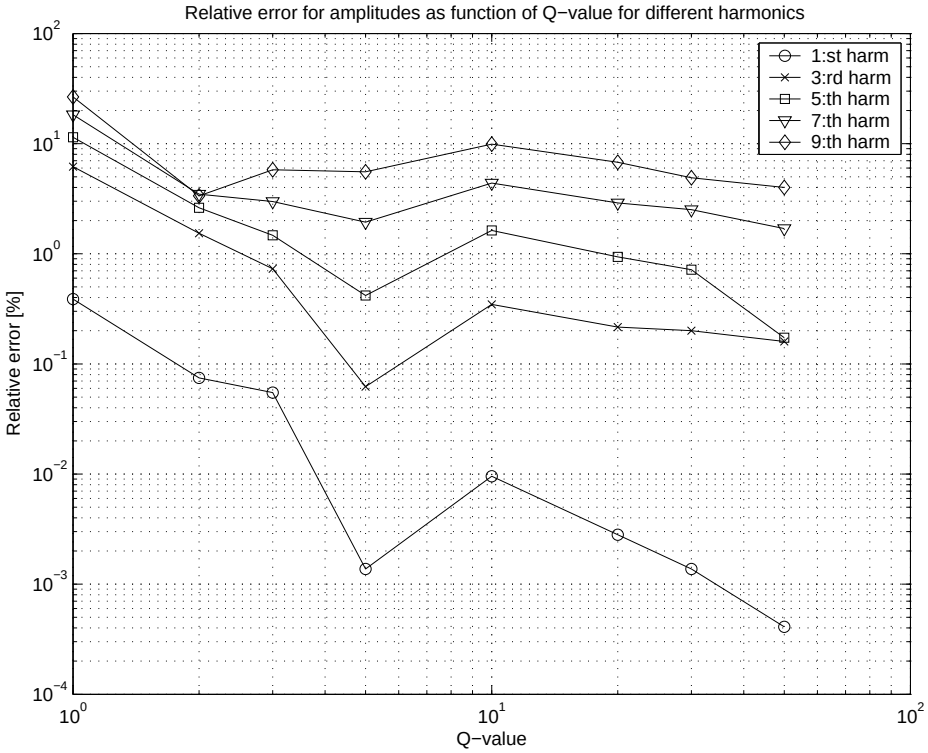


Figure 9.2: Relative error for amplitudes as function of Q-value for different harmonics.

from 1 to 50 and plot the relative resulting errors in per cent for the calculated magnitudes of the ISF components when compared to the simulated counterparts in Figure 9.3.

The fundamental frequency component has an error of less than 1% except when the Q-value is extremely low. Higher frequency components may have errors in the order of 10%, especially for low Q-values.

We finally pay our attention to the phase noise, which is what we really is after. We assume that the noise spectral density of the active part is proportional to the small-signal transfer conductance according to

$$S_{y,f}(\omega, t) = 4k_B T\gamma |f'(X_1 \cos(\omega_0 t))| \tag{9.7}$$

where γ is a proportionality constant and $f'(x)$ is used to denote the derivative of $f(x)$ with respect to x. From (7.76) in Chapter 7 we have that

$$\mathcal{L}[\omega_m] \approx \frac{k_B T R(1+\gamma)}{X_1^2 Q^2} \frac{\omega_0^2}{\omega_m^2}, \tag{9.8}$$

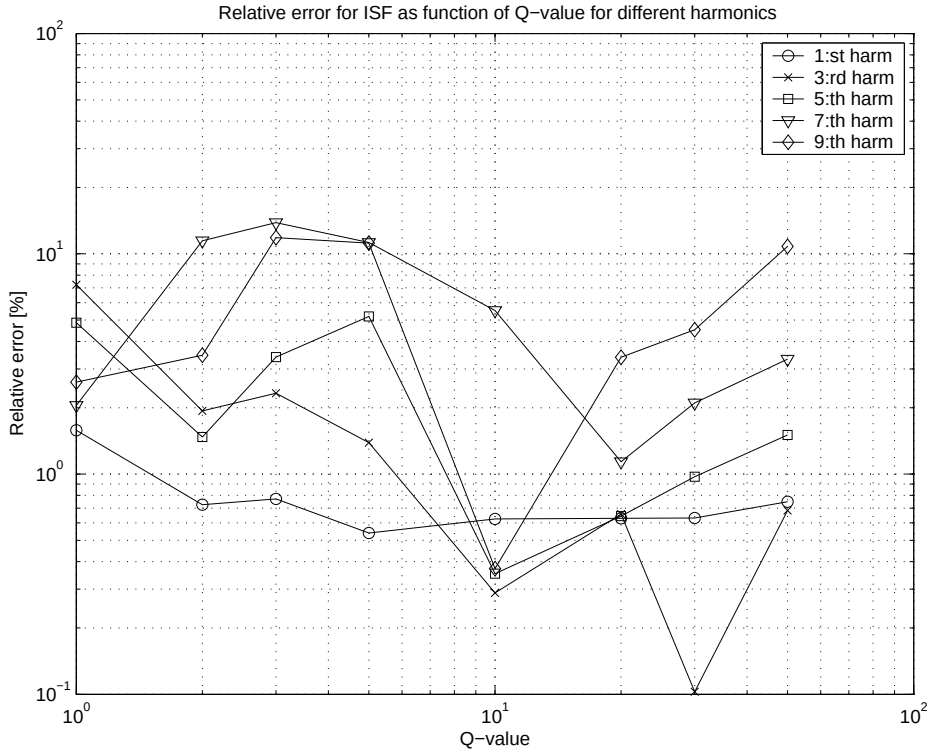


Figure 9.3: Relative error for frequency components of the ISF as function of Q-value.

where we have used that the noise factor, F, is approximately given by

$$F \approx 1 + \gamma. \tag{9.9}$$

We simulate the phase noise at an offset of 100 kHz with γ being 2/3 and 1 and give the simulated values together with those we get from (9.8) in Table 9.3. As seen, we have excellent agreement between predicted and simulated phase-noise performance.

Table 9.3: Phase noise @ 100 kHz offset.

	calculated	simulated	unit
$\gamma = 2/3$	-127.97	-127.96	[dBc/Hz]
$\gamma = 1$	-127.17	-127.17	[dBc/Hz]

We also want to know how different Q-values affect the accuracy of our phase-noise calculation, so we plot the difference between the simulated and

calculated phase noise in Figure 9.4 for Q-values ranging from 1 to 50 with $\gamma = 1$. Even for a Q-value as low as 3, we have an error in calculated phase noise of less than 0.05 dB.

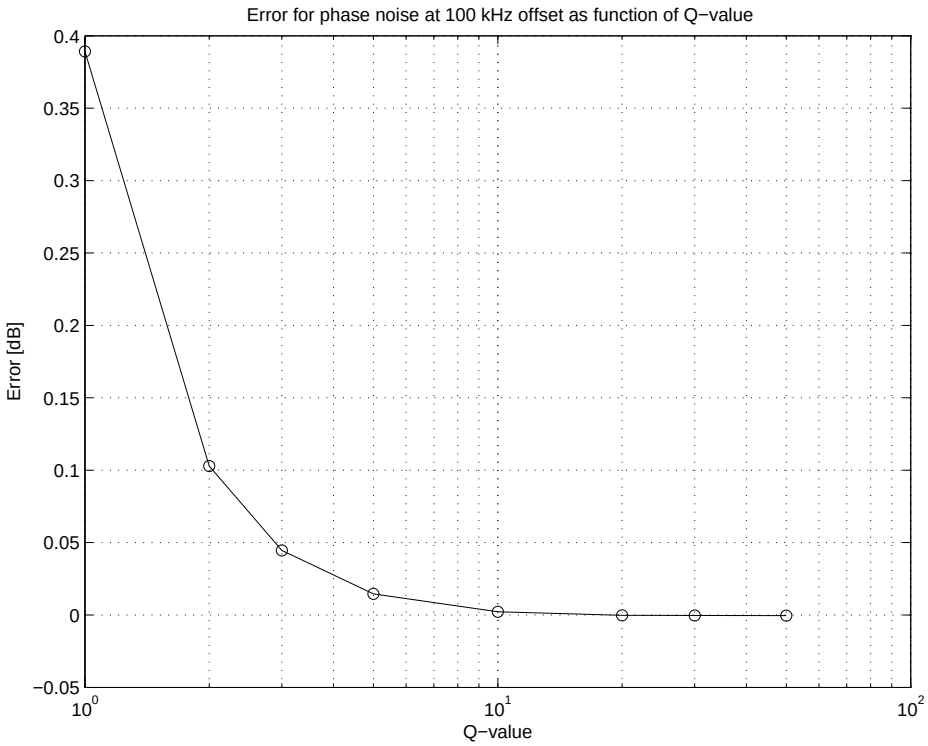


Figure 9.4: Error for phase noise at 100 kHz offset as function of Q-value.

Correction to Oscillation Frequency

Since we have neglected all higher harmonics of the signal at the output of the active block, we now consider them to be input signals to the system and calculate the frequency shift assuming that this additional signal, y_Δ, can be considered small. This additional signal is given by

$$y_\Delta(t) = \Re\left[\sum_{n=2}^{\infty} Y_n e^{jn(\omega_0+\omega_\Delta)t}\right] = \Re\left[\sum_{n=2}^{\infty} \widetilde{F}_n X_1 e^{jn(\omega_0+\omega_\Delta)t}\right]. \tag{9.10}$$

The frequency shift may now be calculated as

$$\omega_\Delta = \overline{\Gamma_y((\omega_0+\omega_\Delta)t) y_\Delta(t)}, \tag{9.11}$$

where the over-line is used to denote time averaging and the ISF, Γ_y, is given by

$$\Gamma_y((\omega_0+\omega_\Delta)t) = \Re\left[\sum_{n=0}^{\infty}\Gamma_{y,n}e^{jn(\omega_0+\omega_\Delta)t}\right], \tag{9.12}$$

where

$$\Gamma_{y,n} = j\frac{n\widetilde{F}_n\omega_0 H^*(jn\omega_0)}{X_1\widetilde{F}_1 Q} \tag{9.13}$$

from (9.6).

Performing the averaging, we get the frequency shift as

$$\omega_\Delta = \frac{1}{2}\sum_{n=2}^{\infty}\Re[\Gamma_{y,n}]Y_n, \tag{9.14}$$

where we have used that Y_n must be real since the active part is memoryless. We also have that

$$\Re[\Gamma_{y,n}] = \frac{n\widetilde{F}_n\omega_0\Im[H(jn\omega_0)]}{X_1\widetilde{F}_1 Q}. \tag{9.15}$$

For a second order system we have

$$\Im[H(jn\omega_0)] = -H(j\omega_0)\frac{Q(n-\frac{1}{n})}{1+Q^2(n-\frac{1}{n})^2}, \tag{9.16}$$

which finally gives us

$$\Delta\omega = -\frac{\omega_0}{2Q^2}\sum_{n=2}^{\infty}\frac{n^2(n^2-1)}{n^2/Q^2+(n^2-1)^2}\frac{\widetilde{F}_n^2}{\widetilde{F}_1^2}. \tag{9.17}$$

This expression is equal to that given by Groszkowski using the method of reactive power balance of harmonics [Groszkowski, 1964].

We plot the frequency shift in Figure 9.5, both simulated and calculated from (9.17) using the first nine harmonics only, *i.e.*, $n \leq 9$.

Noise from Two-Port Feedback Network

In this section we compare the phase-noise performance for two oscillators with two different transimpedance networks having the same transfer function, Z_{21}, and input impedance, Z_{11}, but different output impedance, Z_{22}. The first oscillator, shown in Figure 9.6, has a capacitive voltage division and the second oscillator, shown in Figure 9.7, has a resistive voltage division. We choose the component values such that the oscillation frequency is

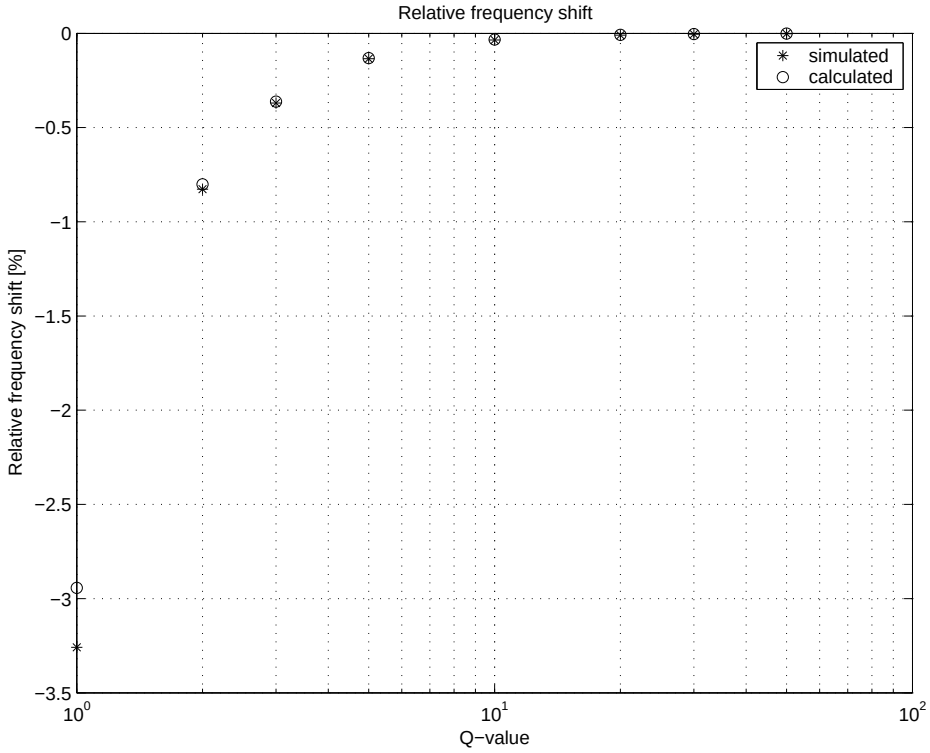


Figure 9.5: Relative frequency shift as function of Q-value.

1 GHz in both cases and the voltage amplitude is equal at the output of the active block. Consequently, the small-signal transconductance at startup, k, is chosen to be 60 mS. The voltage division factor is equal to 1/2.

The phase-noise performance is summarized in Table 9.4. The main difference between the two oscillators is that only the transimpedance network with the capacitive voltage division fulfills the approximation $Z_{11}Z_{22} \approx Z_{21}^2$. In addition to this difference, the real part of the output impedance at multiples of the fundamental frequency is much higher for the transimpedance network with the resistive voltage division.

Table 9.4: Phase noise @ 100 kHz offset.

	C div.	R div.	approx. calc.	unit
feedback only	−130.18	−125.71	−130.18	[dBc/Hz]
active only	−127.17	−127.17	−127.17	[dBc/Hz]
total	−125.41	−123.37	−125.41	[dBc/Hz]

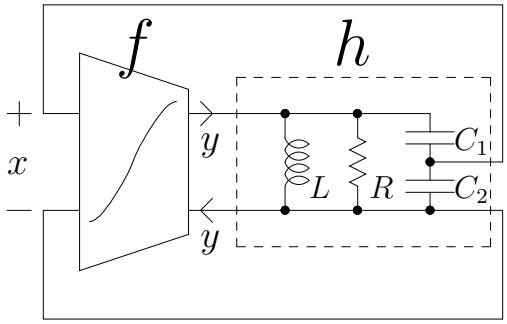


Figure 9.6: Schematic for an ideal oscillator with capacitive voltage division.

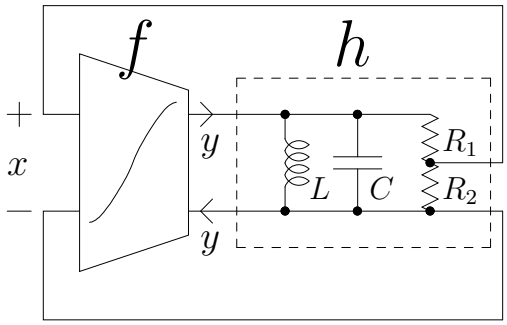


Figure 9.7: Schematic for an ideal oscillator with resistive voltage division.

We now focus on the oscillator with the capacitive voltage division. We see that the phase noise due to the active part has doubled compared to the parallel LC-tank case described earlier. This increase is due to the doubled transconductance of the active part since the transimpedance is now only half of that of the parallel LC-tank case. However, the phase noise due to the feedback network is the same as in the earlier case.

9.1.2 Nonlinear Feedback Network

We now allow the feedback network to be nonlinear while keeping the assumption that the active part is memoryless. The schematic is shown in Figure 9.8 where we now allow the capacitor and resistor in the feedback network to be nonlinear.

We have a voltage-dependent small-signal capacitance given by

$$c(v) = c_0 + c_2 v^2, \tag{9.18}$$

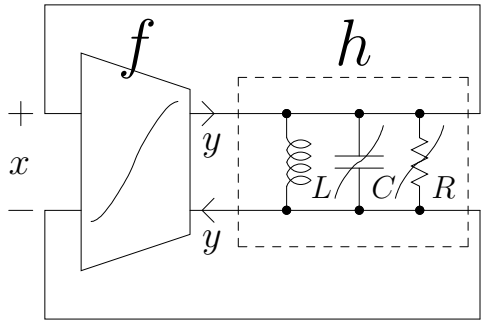


Figure 9.8: Schematic for an ideal oscillator with nonlinear feedback network.

and a resistance with the I–V characteristics given by

$$v(i) = r_1 i + r_3 i^3. \tag{9.19}$$

From (6.10) in Chapter 6 we have that

$$\widetilde{C}(X_1) = C_0(X_1) - \frac{1}{2}C_2(X_1) = c_0 + \frac{1}{4}c_2 X_1^2. \tag{9.20}$$

Keeping the large-signal capacitance, $\widetilde{C}$, constant and assuming that

$$c_0 = k_C \widetilde{C}, \tag{9.21}$$

where k_C is a constant, we get

$$c_2 = \frac{4(\widetilde{C} - c_0)}{X_1^2} = \frac{4(1 - k_C)}{X_1^2}\widetilde{C}. \tag{9.22}$$

In a similar way we can calculate the large-signal resistance as

$$\widetilde{H}_1 = \widetilde{R} = r_1 + \frac{3}{4}r_3 Y_1^2 \tag{9.23}$$

Keeping the large-signal resistance, $\widetilde{R}$, constant and assuming that

$$r_1 = k_R \widetilde{H}_1, \tag{9.24}$$

where k_R is a constant, we get

$$r_3 = \frac{4(\widetilde{H}_1 - r_1)}{3Y_1^2} = \frac{4(1 - k_R)}{3Y_1^2}\widetilde{H}_1. \tag{9.25}$$

We now calculate the Impulse Sensitivity Function (ISF) given by (8.66) as

$$\Gamma_{y,1} = \frac{\omega_0}{Y_1 Q}\left(\frac{Y_1 \widetilde{H}_{\Delta,1}^{(I)} \frac{\partial \alpha}{\partial X_1}}{1 - \widetilde{F}_{\Delta,1}^{(I)} \widetilde{H}_{\Delta,1}^{(I)}} + j\right) \tag{9.26}$$

where we have set $\frac{\partial \zeta}{\partial X_1} = 0$ since the active block is memoryless.

We also have that

$$\frac{\partial \alpha}{\partial X_1} = \frac{\partial \alpha}{\partial \widetilde{C}} \frac{\partial \widetilde{C}}{\partial X_1} = -\frac{2Q(1-k_C)}{X_1}, \tag{9.27}$$

where we have used that

$$\frac{\partial \widetilde{C}}{\partial X_1} = \frac{C_2}{X_1} = \frac{1}{2} c_2 X_1 = \frac{2(1-k_C)\widetilde{C}}{X_1} \tag{9.28}$$

and

$$\frac{\partial \alpha}{\partial \widetilde{C}} = -\frac{Q}{\widetilde{C}}. \tag{9.29}$$

The Incremental Describing Function (IDF) for the feedback network is given by

$$\widetilde{H}_{\Delta,1}^{(I)} = \frac{\partial X_1}{\partial Y_1} = \frac{\partial (Y_1 \widetilde{H}_1)}{\partial Y_1} = r_1 + \frac{9}{4} r_3 Y_1^2 = \widetilde{H}_1 (3 - 2k_R), \tag{9.30}$$

where we have used (9.23).

From (A.55) in Appendix A we have that

$$\widetilde{F}_{\Delta,1}^{(I)} = \frac{\partial Y_1}{\partial X_1} = \frac{\widetilde{F}_1}{\sqrt{1 + \left(\frac{\pi k X_1}{2 y_{max}}\right)^2}}. \tag{9.31}$$

Inserting (9.27), (9.30) and (9.31) in (9.26), we get

$$\Gamma_{y,1} = \frac{\omega_0}{Y_1 Q}\left(-\frac{2Q(1-k_C)(3-2k_R)}{1 - \frac{3-2k_R}{\sqrt{1+\left(\frac{\pi k X_1}{2 y_{max}}\right)^2}}} + j\right). \tag{9.32}$$

The fundamental component of the ISF was simulated for different values of k_C and k_R in Table 9.5 and compared to the calculated value we get from (9.32).

We see that the error in predicted ISF increases with increasing nonlinearity in the feedback network. The amount of higher harmonics increases

Table 9.5: Fundamental component of impulse sensitivity function, $\Gamma_{y,1}$.

	calculated	simulated	unit
$k_C = 1, k_R = 1$	$30.219e^{j1.571}$	$30.408e^{j1.565}$	[Grad/C]
$k_C = 0.95, k_R = 1$	$48.375e^{j2.467}$	$47.856e^{j2.460}$	[Grad/C]
$k_C = 0.9, k_R = 1$	$81.368e^{j2.761}$	$79.362e^{j2.755}$	[Grad/C]
$k_C = 0.9, k_R = 0.9$	$100.100e^{j2.835}$	$94.915e^{j2.819}$	[Grad/C]

with the nonlinearity and makes the assumption of negligible amounts of harmonics less valid.

Next, we check the phase noise of this oscillator. From (7.1), (7.67) and (7.68) we have that

$$\mathcal{L}[\omega_m] \approx \frac{k_B T \left((1+\gamma)\Im[\Gamma_{y,1}]^2 + (1+\gamma\widetilde{F}_{\Delta,1}^{(I)}\widetilde{H}_1)\Re[\Gamma_{y,1}]^2 \right)}{\widetilde{H}_1 \omega_m^2}, \tag{9.33}$$

where we used that $\Re[Z_{11}] = Z_{21} = \widetilde{H}_1$ and that there is no extra noise due to biasing networks. The values we get from evaluating (9.33) for different values of k_C and k_R are shown in Table 9.6 together with their simulated counterparts.

Table 9.6: Phase noise @ 100 kHz offset.

	calculated	simulated	unit
$k_C = 1, k_R = 1, \gamma = 0$	-130.18	-130.18	[dBc/Hz]
$k_C = 1, k_R = 1, \gamma = 1$	-127.17	-127.17	[dBc/Hz]
$k_C = 0.95, k_R = 1, \gamma = 0$	-126.10	-126.20	[dBc/Hz]
$k_C = 0.95, k_R = 1, \gamma = 1$	-124.30	-124.42	[dBc/Hz]
$k_C = 0.9, k_R = 1, \gamma = 0$	-121.58	-121.76	[dBc/Hz]
$k_C = 0.9, k_R = 1, \gamma = 1$	-120.41	-120.61	[dBc/Hz]
$k_C = 0.9, k_R = 0.9, \gamma = 0$	-119.78	-120.76	[dBc/Hz]
$k_C = 0.9, k_R = 0.9, \gamma = 1$	-118.73	-119.56	[dBc/Hz]

We see that the error in predicted phase noise increases with increasing nonlinearity. The main reasons for the error in predicted phase noise are the errors in predicted ISF and the approximation that the nonlinear resistor has the noise spectral density of a linear resistor.

9.1.3 Nonlinear Feedback Network and Diode Limiting

We saw in the last section that a nonlinear feedback network may increase the phase noise substantially, mainly due to the AM-to-PM conversion mechanism. This increase in phase noise comes from the real part of (9.26) and we see that to decrease this extra noise, we can introduce an amplitude limiting function. By introducing diode limiting, we get $\widetilde{H}^{(I)}_{\Delta,1} \ll \widetilde{H}_1$.

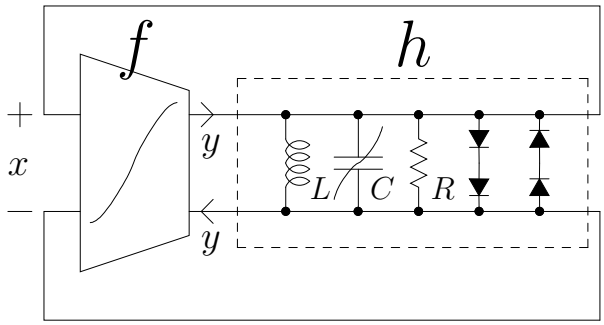


Figure 9.9: Schematic for an ideal oscillator with nonlinear feedback network with amplitude control.

The diodes used during simulations are ideal with no series resistance or parallel capacitance. We may now approximate the oscillation amplitude using

$$X_{1,nonlin} \approx 2V_T \ln\left(\frac{y_{max}}{I_S}\right) \approx 1.35 \text{ V} \tag{9.34}$$

where I_S=0.1 pA for the chosen diodes and the 2 comes from the number of series-connected diodes.

Instead of performing the full phase-noise calculation, we can get an approximate value for the phase noise by neglecting the AM-to-PM conversion and use

$$\mathcal{L}[\omega_m] \approx \mathcal{L}_{lin}[\omega_m]\frac{X^3_{1,lin}}{X^3_{1,nonlin}}, \tag{9.35}$$

where $\mathcal{L}_{lin}$ is the phase noise for an oscillator with linear feedback network, $X_{1,lin}$ is the voltage amplitude for an oscillator with a linear feedback network without limiting and $X_{1,nonlin}$ is the voltage amplitude with limiting. The cube comes from the fact that we decrease the Q-value and the input impedance to the feedback network, where the phase noise is inversely proportional to the squared Q-value and inversely proportional to the input impedance. This expression gives the phase noise as -121.54 dBc/Hz at

100 kHz offset. This expression will give a slight overestimate of the phase noise since the input-current amplitude to the feedback network, Y_1, is somewhat lower with this new lower voltage amplitude, $X_{1,nonlin}$, and the noise of the diodes are less than those of a corresponding resistor. The simulated values for the phase noise are given in Table 9.7 with $\gamma = 1$. We see that

Table 9.7: Phase noise @ 100 kHz offset.

	phase noise	amplitude
$k_C = 1$	-122.19 [dBc/Hz]	1.340 V
$k_C = 0.95$	-121.96 [dBc/Hz]	1.349 V
$k_C = 0.9$	-121.68 [dBc/Hz]	1.358 V

the phase noise is much less dependent on the nonlinearities in the feedback network compared to the unregulated case.

9.1.4 Nonlinear Feedback Network and Automatic Amplitude Control

Another amplitude control can be achieved by measuring the oscillation voltage amplitude using a peak detector, comparing it with a reference voltage, and regulating the bias current to the active part according to the block diagram of Figure 9.10. The amplitude regulation gives $|\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}| \gg 1$ in (9.26).

The values for the differential diode peak detector are: $R_P = 4$ kΩ, $C_P = 400$ pF, and the gain for the bias control is $G_m = 100$ mS. These values give a loading resistance of $\widetilde{R} \approx 2$ kΩ using (5.14), which gives a negligible load compared to the tank resistance of approximately 100 Ω.

We choose the reference voltage, x_{ref}, to get an approximate voltage limited amplitude of $X_{1,nonlin} = 1.4$ V. The phase noise can be approximated as

$$\mathcal{L}[\omega_m] \approx \mathcal{L}_{lin}[\omega_m]\frac{X^2_{1,lin}}{X^2_{1,nonlin}}, \tag{9.36}$$

where $\mathcal{L}_{lin}$ is the phase noise for an oscillator with linear feedback network, $X_{1,lin}$ is the voltage amplitude for an oscillator with a linear feedback network without limiting and $X_{1,nonlin}$ is the voltage amplitude with limiting. The square comes from the fact that we decrease the input amplitude to the feedback network, where the phase noise is inversely proportional to the squared input amplitude. This expression gives the phase noise as -123.74 dBc/Hz at 100 kHz offset. Simulated values for the phase noise of this oscillator are

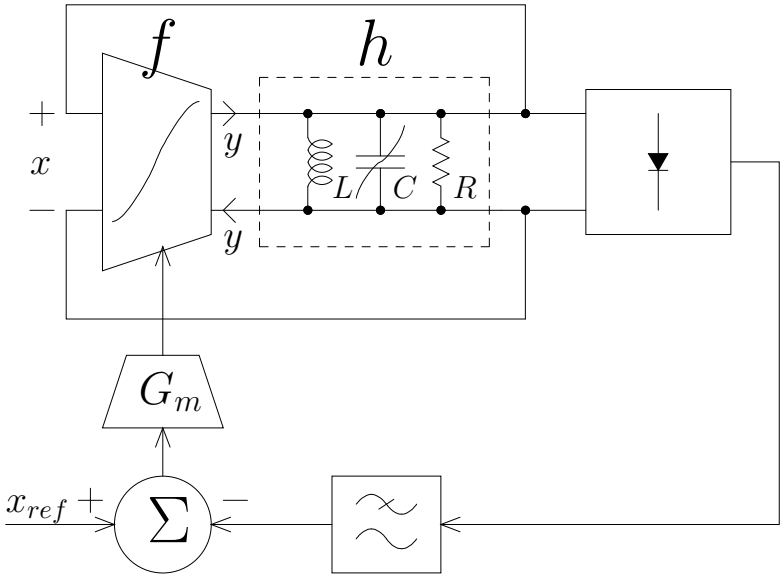


Figure 9.10: Schematic for an ideal oscillator with nonlinear feedback network with amplitude control.

Table 9.8: Phase noise @ 100 kHz offset.

	phase noise	amplitude
$k_C = 1$	−123.48 [dBc/Hz]	1.388 V
$k_C = 0.95$	−123.19 [dBc/Hz]	1.398 V
$k_C = 0.9$	−122.60 [dBc/Hz]	1.409 V

given in Table 9.8 with $\gamma = 1$. We see that the phase noise is much less dependent on the nonlinearities in the feedback network compared to the unregulated case.

9.2 Simulation of Transistor Topology

We now simulate a Colpitts oscillator using electronic building-blocks. The component models used are ideal unless otherwise stated, *e.g.* no series resistances, parasitic capacitances or delays. The reason for using idealized behavior is that we here want to know the errors in approximations done when deriving the expressions for phase noise, not the errors in component models.

This oscillator is not designed to be optimal in any way – it is only de-

signed to check the expressions derived for the design methodology, especially those for the phase noise. The essentials for the oscillator are shown in Figure 9.11 where we see that the active part is made up of a bipolar transistor and the feedback network is a CLC transimpedance network.

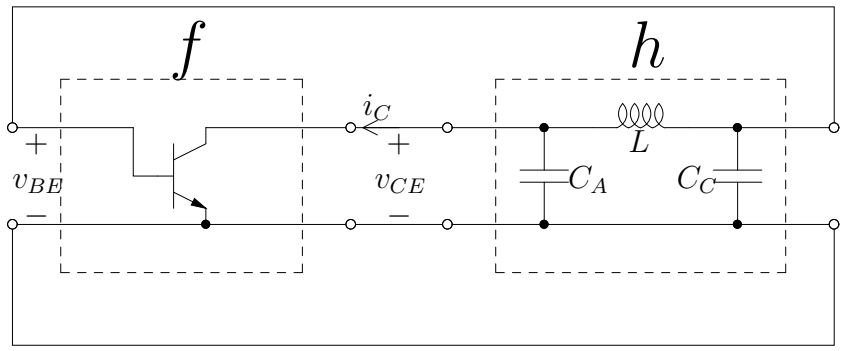


Figure 9.11: Schematic.

We assume that the capacitors have very high Q-values and that the inductor has a Q-value of 100. We have a supply voltage, V_{CC}, of 10 V and a supply current, I_{EE}, of 1 mA. The transistor has a β of 100 and the oscillation frequency, f_0, is 1 MHz. We assume that the base series resistance, r_{bb}, is negligible, which in this case means that it is much lower than 1 Ω.

The values for the feedback network are chosen such that we get the voltage amplitudes at the input to the active network as $|V_{be,1}| = 2.5$ V and at the output of the active network as $|V_{ce,1}| = 5$ V. This implies that $Z_{11} = -2Z_{21}$. We also have that the output-current amplitude is $|I_{c,1}| \approx 2I_{EE}$. The input impedance to the feedback network is given by

$$Z_{11} = -\frac{V_{ce,1}}{I_{c,1}} \tag{9.37}$$

and the transimpedance is given by

$$Z_{21} = -\frac{V_{be,1}}{I_{c,1}}. \tag{9.38}$$

The capacitances are given as $C_A = C/(1-n)$ and $C_C = C/n$, where $n = 1/3$ in this case. We can now calculate the values for the capacitances from

$$C = \frac{Qn(1-n)}{\omega_0 |Z_{21}|} \tag{9.39}$$

and the inductance as

$$L = \frac{1}{\omega_0^2 C}. \tag{9.40}$$

From these design values, we can calculate the power efficiency as

$$\eta \approx -\frac{V_{ce,1} I_{c,1}}{2 V_{CC} I_{EE}} = \frac{1}{2} \tag{9.41}$$

and the noise factor as

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} = 2, \tag{9.42}$$

where we have $\gamma = 1/2$ for bipolar transistors.

We can now calculate the resulting phase noise as

$$\mathcal{L}[\omega_m] \approx \frac{k_B T F}{2 P_{DC} Q^2 \eta} \frac{\omega_0^2}{\omega_m^2}, \tag{9.43}$$

where $P_{DC} = V_{CC} I_{EE}$ is the power consumption.

The schematic for the biased oscillator is given in Figure 9.12. The resistor R models the losses in the inductor L. The bias voltage V_{BB} is chosen to be 1.4 V to always have a positive voltage over the current bias source, I_{EE}.

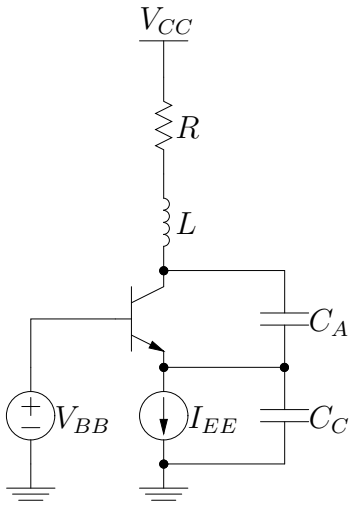


Figure 9.12: Schematic.

Simulating this schematic, we get the voltage amplitudes as $|V_{c,1}| = 7.28$ V and $|V_{e,1}| = 2.43$ V to be compared to the calculated values of $|V_{c,1}| = 7.50$ V and $|V_{e,1}| = 2.50$ V. The simulated phase noise is -140.49 dBc/Hz at 100 Hz offset compared to the calculated value of -140.82 dBc/Hz using (9.43). The

peak emitter current is simulated to be 23.95 mA compared to the calculated value of 24.58 mA using (C.23).

Adding a base resistance r_b of 2 Ω increases the phase noise. The new noise factor is given by

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \frac{4}{9} \frac{r_b}{Z_{11}} \frac{Z_{11}^2}{Z_{21}^2} \left(\frac{|V_{be,1}|}{V_T} \right)^{\frac{3}{2}}, \tag{9.44}$$

where we have used (7.23) and (C.24) for the additional term. The new value for the noise factor is 3.35. The new simulated phase noise is −138.36 dBc/Hz at 100 Hz offset compared to the calculated value of = −138.57 dBc/Hz.

We now look at the influence of the biasing network on the phase noise of the implemented oscillator. The schematic is given in Figure 9.13. The resistor R_E is chosen such that the voltage drop across this resistor is 300 mV, which gives a value of 300 Ω. The capacitor, C_E, filters out most of the noise coming from the left side of the current mirror, so the bias noise is mainly made up of the noise from the transistor and resistor acting as a current source. Since the voltage drop over R_E is much higher than the thermal voltage, V_T, the noise current from the bias network is approximately that of the resistor, R_E, alone.

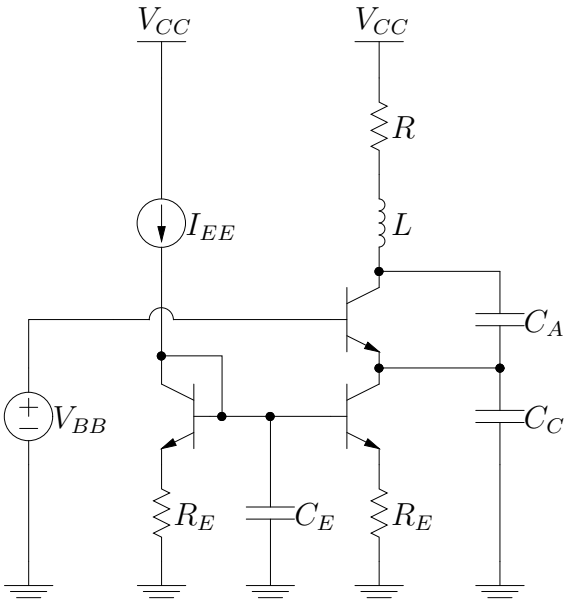


Figure 9.13: Schematic.

The new noise factor including the bias noise is given in (7.69) as

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \frac{Z_{11}}{R_E} \frac{Z_{22}^2}{Z_{21}^2} \tag{9.45}$$

and the simulated phase noise is -137.40 dBc/Hz at 100 Hz offset to be compared to the calculated value of -137.72 dBc/Hz.

From (9.45) we see that the bias network contributes approximately half of the phase noise, which means that the design is probably not optimal from the noise point of view.

We also simulate the circuit with 1/f noise in the transistors, but as expected the contribution to the phase noise is negligible since we have neither nonlinear reactive components nor delay in the transistor.

We proceed with the evaluation of the oscillator when AM-to-PM conversion is present. By introducing frequency tuning using a reverse-biased diode according to Figure 9.14, we also get AM-to-PM conversion.

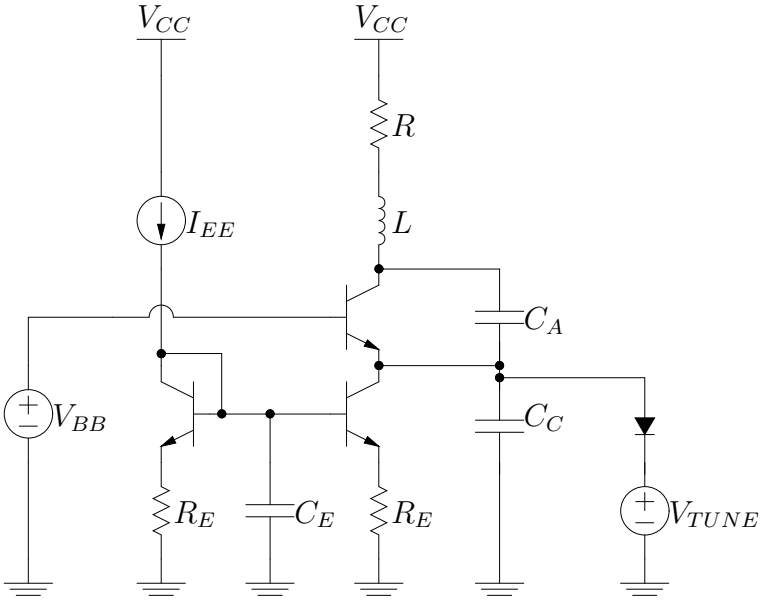


Figure 9.14: Schematic.

The Q-value of the oscillator is kept as above, the capacitance of C_C is halved, and the capacitance of the diode when no voltage over it is present, C_N, is calculated from (6.45), only using the first term as

$$\widetilde{C} \approx C_N \sqrt{\frac{\psi}{\psi + V_0}}, \tag{9.46}$$

where $V_0 = V_{TUNE} - V_{e,0}$, with the DC potential at the emitter, $V_{e,0}$, as approximately 3 V, and the built-in diode potential, ψ, equal to 1 V. We assume that we want an oscillation frequency of 1 MHz when $V_{TUNE} = 10$ V and consequently $\widetilde{C}$ must be half of the value of C_C calculated above at this voltage. Simulating the oscillator, we get the voltage amplitudes as $|V_{c,1}| = 7.15$ V and $|V_{e,1}| = 2.37$ V and the oscillation frequency as 998.66 kHz.

We now calculate the AM-to-PM conversion, K_{AM-PM}, given in (6.28) as

$$K_{AM-PM} \approx \frac{|X_1|}{1 - \widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}} \frac{\widetilde{H}^{(I)}_{\Delta,1}}{\widetilde{H}_1} \frac{\partial \alpha}{\partial |X_1|}, \tag{9.47}$$

where from (6.29) we have that

$$\frac{\partial \alpha}{\partial |X_1|} = -\frac{\partial \alpha}{\partial \omega_0} \frac{\partial \omega_0}{\partial \widetilde{C}} \frac{\partial \widetilde{C}}{\partial V_1} \frac{\partial V_1}{\partial |X_1|}, \tag{9.48}$$

where V_1 is the voltage amplitude over the varactor. In this topology, we see that $V_1 = X_1$. From (6.32) we have

$$\frac{\partial \alpha}{\partial \omega_0} \approx -\frac{2Q}{\omega_0} \tag{9.49}$$

and from (6.22) we have

$$\frac{\partial \omega_0}{\partial \widetilde{C}} = \frac{\partial \omega_0}{\partial C} \frac{\partial C}{\partial \widetilde{C}} \approx -\frac{\omega_0}{2C} \frac{\partial C}{\partial \widetilde{C}}, \tag{9.50}$$

where

$$C = \frac{C_A(C_C + \widetilde{C})}{C_A + C_C + \widetilde{C}} \tag{9.51}$$

and consequently

$$\frac{\partial C}{\partial \widetilde{C}} = \frac{C}{C_C + \widetilde{C}} - \frac{C}{C_A + C_C + \widetilde{C}}. \tag{9.52}$$

Combing these expressions and assuming that $|\widetilde{F}^{(I)}_{\Delta,1}\widetilde{H}^{(I)}_{\Delta,1}| \ll 1$ and $\frac{\widetilde{H}^{(I)}_{\Delta,1}}{\widetilde{H}_1} \approx 1$, we get

$$K_{AM-PM} \approx -Q \frac{C_2}{C} \frac{\partial C}{\partial \widetilde{C}}, \tag{9.53}$$

where we also used from (6.33) that

$$\frac{\partial \widetilde{C}}{\partial V_1} = \frac{C_2}{V_1}, \tag{9.54}$$

where C_2 is defined in Section 6.2. Inserting values, we get $K_{AM-PM} = -2.53$.

We now focus on the phase noise due to white noise. Since the AM-to-PM conversion is high, we cannot assume that the low-frequency noise contribution to the phase noise is negligible.

The new noise factor is given by

$$F \approx 1 + \gamma \frac{Z_{11}}{|Z_{21}|} + \frac{Z_{11}}{R_E}\frac{Z_{22}^2}{Z_{21}^2} + K_{AM-PM}^2 \left(1 + \gamma |\widetilde{G}_{\Delta,1}^{(I)}| Z_{11} + \frac{Z_{11}}{R_E}\frac{Z_{22}^2}{Z_{21}^2} + 4\frac{Z_{11}}{R_E}\right), \tag{9.55}$$

where K_{AM-PM} is the AM-to-PM conversion and $\widetilde{G}_{\Delta,1}^{(I)}$ is the incremental large-signal transconductance of the transistor, which we assume is small enough to be negligible since the transistor operates in Class C. The last term in the expression for the noise factor is the contribution from the two resistors R_E, since noise from neither of them are filtered out by capacitor C_E at low frequencies. Inserting values gives us a noise factor of staggering 237.4.

We now get the calculated phase noise as -120.08 dBc/Hz at 100 Hz offset to be compared to the simulated value of -119.39 dBc/Hz at 100 Hz offset. We see that the phase noise performance of the oscillator is extremely poor due to the high AM-to-PM conversion due to the diode varactor in combination with the low-frequency noise due to the biasing network.

We proceed with the calculation of phase noise due to 1/f noise. The transistors have a 1/f noise factor $K_{1/f} = 5$ fA^2/Hz, corresponding to a noise corner frequency of approximately 160 Hz. The phase noise due to 1/f noise is given in (7.95) as

$$\mathcal{L}[\omega_m] = \frac{2\pi(K_{1/f,f} + K_{1/f,b})I_{EE}}{8Q^2}\left(K_{AM-PM}\frac{1}{B}\frac{\partial B}{\partial I_{EE}} + \frac{\partial \zeta}{\partial I_{EE}}\right)^2 \frac{\omega_0^2}{\omega_m^3}. \tag{9.56}$$

From Section 7.3.2 we have that $K_{1/f,f} = \frac{K_{1/f}}{\beta}$ and from (4.94) in Section 4.3.2 we have that $K_{1/f,b} \approx \frac{4K_{1/f}}{\beta}$ since $R_B \approx R_E$. Assuming that $\frac{\partial \zeta}{\partial I_{EE}}$=0 and the transistor is operating in Class C, we get a calculated phase noise of -46.99 dBc/Hz at 1 Hz offset to be compared with the simulated value of -47.69 dBc/Hz at 1 Hz offset.

We proceed with the calculation of the noise corner frequency, given in (7.96) as

$$f_{m,1/f} = \frac{(K_{1/f,f} + K_{1/f,b})I_{EE}P_1}{4k_BTF}\left(K_{AM-PM}\frac{1}{B}\frac{\partial B}{\partial I_{EE}} + \frac{\partial \zeta}{\partial I_{EE}}\right)^2. \tag{9.57}$$

Under the same assumptions as before, we get a calculated noise corner frequency of 2.04 kHz to be compared to the simulated value of 1.44 kHz.

9.3 Comparisons with Published Measurements

The reported phase-noise performance from several papers are summarized in conjunction with parameters such as oscillation frequency f_0, Q-value Q, supply voltage V_{DC}, power consumption P_{DC}, and tuning range f_{tune}/f_0 in Table 9.9. The Q-value of the inductor is assumed to be dominant compared to those of capacitors and varactors if no other Q-values are given. When phase noise, $\mathcal{L}$, was given at several offset frequencies, f_m, from the oscillation frequency used when measuring phase noise, f_{meas}, the highest offset frequency was chosen to get phase noise from white noise only. The frequency tuning range does only consider the continuous tuning range in the band where the phase noise was measured. The product between the tuning range and Q-value, as well as the voltage division of the feedback network, $\frac{Z_{11}}{|Z_{21}|}$, are also given. In the last column we calculate the oscillator design efficiency, Υ_{mea}.

In Table 9.10, we estimate an approximative value for the Oscillator Design Efficiency, Υ_{est} and compare it to the ODEs we get from the measurements, Υ_{mea}, of Table 9.9 using the expressions of Section 4.4. Minimum overdrive or saturation voltages are assumed to be 0.3 V. For FETs, we assume that $K_{FET} = 0.6$ and $\gamma = 1$. For filtered current bias sources, we assume that the noise contribution from the bias network is negligible.

The column with title 'varactor' describes which, if any, type of varactor is used to tune the frequency. Diode means that reverse-biased diodes are used, AMOS that MOS structures operating between accumulation and depletion are used, IMOS that MOS structures operating between inversion and depletion are used, and MEMS that Micro-Electro-Mechanical Systems are used.

The column with title 'active' describes what type of transistors and type of topology is used for the active part. The abbreviations are as follows: diff = differential stage, inv = inverters, x2 = two single transistors. All the topologies are on chip and differential.

The column with title 'bias' shows what type of current source, if any, is used to bias the active part. It also shows if the bias current source is filtered with abbreviation filt. Finally it shows which terminal is signal grounded: CS = Common Source, CG = Common Gate.

The column with title 'feedback' describes what type of feedback network is used. The abbreviations are given in Section 4.1.6.

The estimated ODEs of Table 9.10 are plotted against the ODEs derived from measured data in Table 9.9 in Figure 9.15. Nearly all oscillator ODEs are estimated with an error of less than 5 dB. The errors in estimation may have several causes, such as excessive noise from bias network, voltage lim-

Table 9.9: Phase noise @ 100 kHz offset.

Reference	f_0 [GHz]	$\mathcal{L}$ @ f_m [dBc/Hz] @ [kHz]	f_{meas} [GHz]	Q	V_{DC} [V]	P_{DC} [mW]	$\frac{f_{tune}}{f_0}$	$Q\frac{f_{tune}}{f_0}$	$\frac{Z_{11}}{\lvert Z_{21}\rvert}$	Υ_{mea} [dB]
[Hung and O, 2000][1]	1.05	-125 @ 600	1.09	10	1.5	6.8	5.7%	0.57	1	-15.0
[Dec and Suyama, 2000][2]	1.9	-126 @ 600	1.9	8.3	2.7	15	9%	0.75	1	-11.0
[Svelto et al., 2000][3]	1.3	-119 @ 600	1.3	4.0	2.0	12	28%	1.12	1	-13.9
[Darabi and Abidi, 2000][4]	0.82	-98 @ 25	0.83	30	1.5	0.45	12%	3.60	1	-14.5
[Ham and Hajimiri, 2001][5]	2.33	-121 @ 600	1.91	4.5	2.5	10	26%	1.17	1	-8.8
[Hegazi et al., 2001][6]	1.2	-153 @ 3000	1.2	14	2.5	9.25	?[a]	?	1	-4.4
[Andreani and Sjöland, 2002][7]	2.16	-137.5 @ 3000	2.36	9	1.4	12.6	18%	1.62	1	-11.5
[Andreani and Sjöland, 2002][8]	1.83	-138.5 @ 3	1.96	8	2.0	12	15%	1.20	1	-10.9
[Aparicio and Hajimiri, 2002][9]	2.12	-139 @ 3000	1.8	6	2.5	10	30.5%	1.83	4	-7.8
[Fong et al., 2003][10]	4.3	-120.8 @ 1000	3	20	1.0	3	23%	4.60	1	-17.1
[Jia et al., 2004][11]	9.83	-89 @ 100	9.83	7.9	1.8	5.8	11.2%	0.88	1	-13.6
[Fong et al., 2004][12]	38.6	-109.7 @ 4000	40	8.3	1.5	11.25	7.8%	0.65	1	-16.0
[Moon et al., 2004][13]	4.34	-119 @ 1000	4.34	14	2.5	4.25	4.1%	0.57	1	-14.3
[Kao and Hsu, 2005][14]	2.06	-116 @ 600	2	4.4	3.0	22.62	9.1%	0.40	1	-16.5
[Jerng and Sodini, 2005][15]	5.32	-124 @ 1000	5.32	10	1.8	13.5	8%	0.80	1	-9.6
[Berny et al., 2005][16]	1.8	-123.5 @ 600	1.8	8	1.5	4.8	6%	0.48	1	-8.7
[Yoon et al., 2005][17]	2.16	-120.2 @ 600	1.96	8	1.7	1.87	18%	1.44	1	-7.1
[Andreani et al., 2005][18]	2.9	-142 @ 3000	2.9	12	2.0	16	5%	0.60	1	-8.8
[Andreani et al., 2005][19]	2.9	-138 @ 3000	2.9	12	2.5	22.5	5%	0.60	3	-14.2

[a]Not given, but probably low since switched-capacitor array is employed

Table 9.10: Phase noise @ 100 kHz offset.

Reference	Process	Varactor	Active	Bias	Feedback	Υ_{est} [dB]	Υ_{mea} [dB]
[Hung and O, 2000][1]	0.8-μm CMOS	Diode	PMOS x2	NMOS CS	LC	-10.4	-15.0
[Dec and Suyama, 2000][2]	0.5-μm CMOS	MEMS	CMOS inv	-	LC	-9.4	-11.0
[Svelto et al., 2000][3]	0.35-μm CMOS	AMOS	NMOS diff	NMOS	LC	-11.2	-13.9
[Darabi and Abidi, 2000][4]	0.25-μm CMOS	AMOS	NMOS diff	NMOS	LC	-11.5	-14.5
[Ham and Hajimiri, 2001][5]	0.35-μm CMOS	IMOS	CMOS diff	NMOS	LC	-14.0	-8.8
[Hegazi et al., 2001][6]	0.35-μm CMOS	AMOS	NMOS diff	NMOS filt	LC	-6.2	-4.4
[Andreani and Sjöland, 2002][7]	0.35-μm CMOS	AMOS	NMOS diff	NMOS filt	LC	-7.4	-11.5
[Andreani and Sjöland, 2002][8]	0.35-μm CMOS	AMOS	CMOS diff	NMOS filt	LC	-10.5	-10.9
[Aparicio and Hajimiri, 2002][9]	0.35-μm CMOS	IMOS	NMOS x2	NMOS CG	CLC	-9.6	-7.8
[Fong et al., 2003][10]	0.13-μm SOI CMOS	AMOS	CMOS inv	-	LC	-12.2	-17.1
[Jia et al., 2004][11]	0.18-μm CMOS	Diode	CMOS diff	NMOS	LC	-14.3	-13.6
[Fong et al., 2004][12]	0.13-μm SOI CMOS	AMOS	CMOS inv	-	LC	-10.5	-16.0
[Moon et al., 2004][13]	0.5-μm SiGe BiCMOS	Diode	NPN diff[a]	NPN?	LC	-13.7	-14.3
[Kao and Hsu, 2005][14]	0.35-μm CMOS	IMOS	CMOS diff	NMOS	LC	-14.0	-16.5
[Jerng and Sodini, 2005][15]	0.18-μm SiGe BiCMOS	Diode	PMOS diff	PMOS	LC	-11.3	-9.6
[Berny et al., 2005][16]	0.18-μm CMOS	AMOS	NMOS diff	NMOS	LC	-11.5	-8.7
[Yoon et al., 2005][17]	0.35-μm CMOS	AMOS	CMOS inv	-	LC	-7.1	-7.1
[Andreani et al., 2005][18]	0.35-μm CMOS	AMOS	NMOS diff	NMOS	LC	-11.2	-8.8
[Andreani et al., 2005][19]	0.35-μm CMOS	AMOS	NMOS x2	NMOS CG	CLC	-9.3	-14.2

[a]Biased such that $V_{b,0} = V_{c,0}$

iting, reduced voltage swing due to process restrictions, error in given or estimated Q-value, AM-to-PM conversion significance, excess noise in transistors, and errors in phase noise measurements.

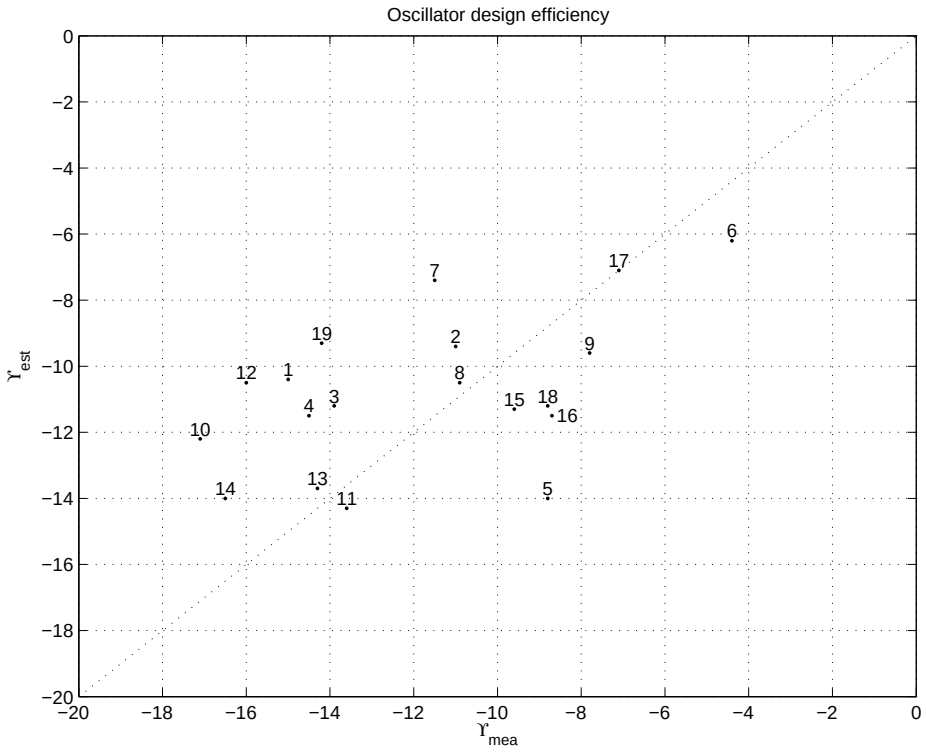


Figure 9.15: Estimated versus measured oscillator design efficiency for some published oscillators. The numbers refer to Table 9.9 and Table 9.10.

Chapter 10

Conclusions and Future Work

This final chapter contains the conclusions drawn from the work carried out in this thesis. It also includes suggestions for future work to improve the oscillator design methodology.

10.1 Conclusions

The principal conclusion drawn from the work in this thesis is that we now have a design methodology for harmonic oscillators, both for integrated and discrete implementations and both for LC and crystal oscillators.

We have also shown that the performance of an oscillator can be predicted quite accurately even before design work has begun. Hence, we can use the derived expressions, for example phase noise as function of power consumption, when doing the overall system design in order to optimize the entire system.

To be able to obtain the closed-form analytical expressions on which the design methodology is based, a new method of calculating the Impulse Sensitivity Functions (ISFs) of oscillators were derived. This new method, based on Describing Functions (DFs), has less limitations than previous methods; for example, it can cope with the nonlinear reactances needed in Voltage Controlled Oscillators (VCOs).

The conclusions drawn about the impact different means of amplitude limiting and different frequency tuning schemes have on the phase noise are discussed at the end of their respective chapter.

It was also shown that the noise factor of oscillators with one transistor or a differential stage as active network does *not* depend on the operation of the transistors to a large degree. This conclusion is contrary to the common belief

that the noise factor decreases when the single transistor works in Class C or when the differential pair switches quickly. In contrast, these operations of transistors increase the power efficiency, consequently giving lower phase noise for a given power consumption.

10.2 Future Work

Even though we now have a functioning design methodology for oscillators, there is still work to be done to improve it further. Below I outline a few important areas where further work would be beneficial to improve the design methodology.

10.2.1 Further Verification

So far, the design methodology has been used to create only three oscillators. Many more oscillators should be designed using the design methodology, by different circuit designers, to detect any flaws in the methodology and to detect if any aspects of the explanation of the design methodology are unclear or ambiguous.

10.2.2 Extensions to the Design Methodology

The design methodology is not complete since there are several specifications as well as properties that are not yet included. Below, I summarize some of the most important aspects that should be incorporated in the design methodology in the future.

More Detailed Transistor Models

The transistor models used in this thesis do not include some effects that are becoming more important nowadays with newer technologies, especially in MOSFET technologies where the Early effect, moderate inversion and body effect may become important.

Quadrature VCOs

In many communication systems today, we need quadrature signals to demodulate the RF carrier. The quadrature oscillator signal could be generated from a single oscillator signal or it may come from a quadrature oscillator. However, the design methodology does not yet support the design of quadrature oscillators.

The difference between a single oscillator and a quadrature oscillator, when it comes to phase calculations, is that the phase differential equation is replaced with two coupled differential equations in the latter case. From these coupled differential equations one can calculate the phase noise and phase error between the two quadrature outputs.

Amplitude Noise

The design methodology presented in this thesis does not consider the amplitude noise, since the amplitude noise is not a major issue in most oscillators. However, there are cases when the amplitude noise is important and the design methodology should ideally incorporate the amplitude noise as well. A similar method to that of the phase noise may be used, but the dynamics of the amplitude control must be accounted for.

Start-Up Time

Sometimes the start-up time is of importance, especially for crystal oscillators which tend to have long start-up times due to the high Q-value of the oscillator. Approximate closed-form expressions for the start-up time of oscillators are still missing and need to be derived to include this specification in the design methodology. Since the time constants of the oscillation period is usually much smaller than the other time constants of a harmonic oscillator, averaging may be performed to give a set of differential equations governing the amplitude behavior [Vanassche et al., 2004].

Oscillator and Buffer Co-Design

Since we want the loading on the oscillator to be negligible in order to avoid Q-value degradation and load pulling, we usually need a buffer to isolate the oscillator from the load it should drive. To optimize the total power consumption, it may be preferable to design the buffer together with the oscillator core in order for the bias levels and amplitudes to be optimal from a power perspective.

Design for Testability

The verification process is not included in the design methodology yet, but the verification should preferably also be done in a systematic way. Having a design methodology that also includes the verification helps the designer to make sure that all design requirements are kept track of all the way from specification to verification.

As the number of building blocks on chip increases, the testability is becoming a serious problem. Hence, the design should be made with testability in mind, already from start.

Appendix A

Describing Functions

The describing-function method is primarily used to indicate whether an oscillation might occur in a nonlinear feedback network and to calculate the amplitude and frequency of such an oscillation. In this appendix I define the Describing Function (DF) and the Incremental Describing Function (IDF). I also show how to calculate DFs and IDFs. Finally, I give the describing functions for a few common nonlinearities encountered in electronics.

In this appendix, we assume that we have an input signal, x, to a nonlinear function, f, with an output signal, y.

The describing-function method is known to produce errors in predicted amplitude, X_1, and frequency, ω_0, of less than 10% in nearly all cases when the rms value of the higher harmonics at the output of the filtering feedback network, h, does not exceed 10% of the fundamental [Atherton, 1975, Atherton and Dorrah, 1980]. An exception is when the feedback network has more than one resonance frequency. For simplicity, we do not consider such feedback networks in the following since these feedback networks are usually avoided when designing oscillators.

A.1 How to Calculate Describing Functions

Since we are working with periodic signals, we can write the input x as a Fourier series as

$$x(\tau) = \Re\left[\sum_{n=0}^{\infty} X_n e^{jn\tau}\right] \tag{A.1}$$

and the output y likewise as

$$y(\tau) = \Re\left[\sum_{n=0}^{\infty} Y_n e^{jn\tau}\right], \tag{A.2}$$

where X_n and Y_n are the complex input and output amplitudes, respectively, and τ is the normalized time, *i.e.*, $\tau = \omega_0 t$, where ω_0 is the fundamental frequency. We have chosen to define the Fourier series using only positive frequencies. This definition makes the comparison with voltage and current amplitudes easier, since they are simply the absolute values of the complex amplitudes.

Since we are working with harmonic oscillators and we have assumed that the higher harmonics are filtered out by the feedback network, we can write the input to the nonlinearity as

$$x(\tau) = X_0 + X_1 \cos(\tau), \tag{A.3}$$

where we have assumed the reference phase for the fundamental sinusoid such that X_1 becomes real and positive.

We now define the describing function $\widetilde{F}_n$ as

$$\widetilde{F}_n(X_1) \equiv \frac{Y_n}{X_1}. \tag{A.4}$$

To simplify notation we have chosen to omit the dependence on X_0 in the general case, but it may be shown explicitly as $\widetilde{F}_n(X_1, X_0)$ in special cases where X_0 is not a constant.

The most useful describing function, that for the fundamental component, might be thought of as an input-dependent gain such that the relationship between the input and output sinusoids of the same frequency can be written as

$$Y_1 = \widetilde{F}_1(X_1)X_1, \tag{A.5}$$

where $\widetilde{F}_1$ acts as the complex gain similar to the transfer function of a linear system; hence the name *equivalent linearization* is sometimes used.

We can calculate the complex output amplitudes, Y_n, according to

$$Y_n = \frac{\varepsilon_n}{2\pi}\int_{-\pi}^{\pi} y(\tau)e^{-jn\tau}d\tau, \tag{A.6}$$

where ε_n is the Neumann factor equal to 1 when $n = 0$ and equal to 2 when $n \geq 1$. Observe that this expression differs from the common complex Fourier series by a factor of two in the cases where $n > 0$ due to the definition of Y_n used here.

In the special case of a single-valued nonlinearity, the imaginary part of Y_n vanishes and we may simplify the expression to

$$Y_n = \frac{\varepsilon_n}{2\pi} \int_{-\pi}^{\pi} y(\tau) \cos(n\tau) d\tau, \tag{A.7}$$

that is, we have no memory in the nonlinearity.

The single-valued nonlinearity makes it possible to write the output of the nonlinearity simply as

$$y(\tau) = f(x(\tau)), \tag{A.8}$$

where f is a real function mapping an input value x to an output value y.

Sometimes it is more convenient to rewrite the integral using orthogonal polynomials instead. For a sinusoidal input to a nonlinearity, the orthogonal polynomials are Chebyshev polynomials, T_n, defined below. The output amplitude may now be written as

$$Y_n = \varepsilon_n \int_{-X_1}^{X_1} f(x) T_n(x/X_1) r(x) dx, \tag{A.9}$$

where $r(x)$ is the amplitude probability distribution for a sinusoid, given by

$$r(x) = \frac{1}{\pi \sqrt{X_1^2 - x^2}}. \tag{A.10}$$

The Chebyshev polynomials can be calculated recursively as

$$T_n(x) = 2xT_{n-1}(x) - T_{n-2}(x) \tag{A.11}$$

and the first four Chebyshev polynomials are shown below.

$$T_n(x) = \begin{cases} 1 & n = 0 \\ x & n = 1 \\ 2x^2 - 1 & n = 2 \\ 4x^3 - 3x & n = 3 \end{cases} \tag{A.12}$$

A.2 Incremental Describing Functions

Sometimes we are interested in the transfer function for a small input signal, e, in addition to the large input signal, x, driving the system. The output signal can be calculated using a time-varying small-signal transfer function,

where the transfer function is periodic and determined by the nonlinearity and the large signal driving the system.

In the special case when the small input signal is a sinusoid with a frequency that is a multiple of the fundamental frequency of the large signal, we can define the Incremental Describing Function (IDF) as the transfer gain for the small signal [Atherton, 1975]. This gain will be dependent on the phase of the small signal in relation to the phase of the large signal as shown below.

We can write the output of the nonlinearity with a small input, e, as

$$y(\tau) = f(x(\tau)) \approx f(x_0(\tau)) + e(t)f'(x_0(\tau)) = y_0(\tau) + e(\tau)f'(x_0(\tau)), \quad \text{(A.13)}$$

where x_0 and y_0 are the input and output of the system without the small input, respectively, and $f'(x)$ is the derivative of $f(x)$ with respect to x.

Assuming that the small-signal input is a sinusoid at a frequency n times that of the fundamental for the large signal according to

$$e(\tau) = \Re\left[E_{\Delta,n}e^{jn\tau}\right], \quad \text{(A.14)}$$

where $E_{\Delta,n}$ is the complex amplitude of the small-signal input, and writing the derivative of the function f as a Fourier series according to

$$f'(X_1\cos(\tau)) = \Re\left[\sum_{n=0}^{\infty}\widetilde{F'}_n e^{jn\tau}\right], \quad \text{(A.15)}$$

where the frequency coefficients, $\widetilde{F'}_n$, are calculated as

$$\widetilde{F'}_n = \frac{\varepsilon_n}{2\pi}\int_{-\pi}^{\pi} f'(X_1\cos(\tau))e^{-jn\tau}d\tau, \quad \text{(A.16)}$$

we get the incremental change $Y_{\Delta,1}$ in Y_1 when an input $E_{\Delta,n}$ is applied as

$$Y_{\Delta,1} = \frac{\delta_{n-1}}{2}E_{\Delta,n}\widetilde{F'}^*_{n-1} + \frac{\delta_n}{2}E^*_{\Delta,n}\widetilde{F'}_{n+1}, \quad \text{(A.17)}$$

where δ_n is equal to 2 when $n = 0$ and equal to 1 when $n \geq 1$. The incremental describing function is defined as

$$\widetilde{F}_{\Delta,n} \equiv \frac{Y_{\Delta,1}}{E_{\Delta,n}}. \quad \text{(A.18)}$$

Below, we derive the incremental describing functions for input signals, $E_{\Delta,n}$, in phase with and in quadrature phase with the driving signal, X_1.

A.2.1 In-Phase Incremental Describing Functions

The complex amplitude for the n:th harmonic at the output is given by

$$Y_n = \frac{\varepsilon_n}{2\pi}\int_{-\pi}^{\pi} f(X_1\cos(\tau))e^{-jn\tau}d\tau. \tag{A.19}$$

Taking the derivative of this expression with respect to the input signal amplitude, we get

$$\frac{\partial Y_n}{\partial X_1} = \frac{\varepsilon_n}{2\pi}\int_{-\pi}^{\pi} f'(X_1\cos(\tau))\cos(\tau)e^{-jn\tau}d\tau \tag{A.20}$$

where

$$\cos(\tau)e^{-jn\tau} = \frac{1}{2}(e^{j(n-1)\tau} + e^{-j(n+1)\tau}). \tag{A.21}$$

Splitting this integral of sums into a sum of integrals, we get

$$\frac{\partial Y_n}{\partial X_1} = \frac{1}{2}(\delta_{n-1}\widetilde{F'}^*_{n-1} + \widetilde{F'}_{n+1}), \tag{A.22}$$

where we have used (A.16).

For an input, $E_{\Delta,n}$, in phase with X_1 we have

$$E_{\Delta,n} = E^{(I)}_{\Delta,n}. \tag{A.23}$$

The in-phase IDF is defined as

$$\widetilde{F}^{(I)}_{\Delta,n} \equiv \frac{Y^{(I)}_{\Delta,1}}{E^{(I)}_{\Delta,n}}. \tag{A.24}$$

Combining (A.17), (A.22), (A.23) and (A.24), we get the IDF for in-phase components as

$$\widetilde{F}^{(I)}_{\Delta,n} = \frac{\partial Y_1}{\partial|X_n|} = \frac{\partial Y_n}{\partial|X_1|}. \tag{A.25}$$

A.2.2 Quadrature-Phase Incremental Describing Functions

The output of the nonlinearity can be described using a Fourier series according to

$$y(\tau) = f(X_1\cos(\tau)) = \sum_{n=0}^{\infty} \Re[Y_n]\cos(n\tau) - \Im[Y_n]\sin(n\tau), \tag{A.26}$$

which can be rewritten as

$$y(\tau) = f(X_1 \cos(\tau)) = \sum_{n=0}^{\infty} \Re[\widetilde{F}_n] X_1 \cos(n\tau) - \Im[\widetilde{F}_n] X_1 \sin(n\tau). \quad \text{(A.27)}$$

Taking the derivative of this expression with regard to the normalized time τ, we get

$$\frac{d}{d\tau} y(\tau) = -X_1 \sin(\tau) f'(X_1 \cos(\tau)) = \sum_{n=0}^{\infty} -n\Re[\widetilde{F}_n] X_1 \sin(n\tau) - n\Im[\widetilde{F}_n] X_1 \cos(n\tau) \quad \text{(A.28)}$$

from which

$$\sin(\tau) f'(X_1 \cos(\tau)) = \sum_{n=1}^{\infty} n\Re[\widetilde{F}_n] \sin(n\tau) + n\Im[\widetilde{F}_n] \cos(n\tau) \quad \text{(A.29)}$$

can be extracted.

The derivative of $f(x)$ with respect to x is written as

$$f'(X_1 \cos(\tau)) = \sum_{n=0}^{\infty} \Re[\widetilde{F'}_n] \cos(n\tau) - \Im[\widetilde{F'}_n] \sin(n\tau), \quad \text{(A.30)}$$

and by multiplying this expression with $\sin(\tau)$, we get

$$\sin(\tau) f'(X_1 \cos(\tau)) = \sum_{n=0}^{\infty} \Re[\widetilde{F'}_n] \cos(n\tau) \sin(\tau) - \Im[\widetilde{F'}_n] \sin(n\tau) \sin(\tau), \quad \text{(A.31)}$$

which can be rewritten as

$$\sin(\tau) f'(X_1 \cos(\tau)) = \frac{1}{2} \left(\Re[\widetilde{F'}_0] \sin(\tau) - \Im[\widetilde{F'}_0] \cos(\tau) - \Im[\widetilde{F'}_1] \right) + \\ + \frac{1}{2} \sum_{n=1}^{\infty} (\Re[\widetilde{F'}_{n-1}] - \Re[\widetilde{F'}_{n+1}]) \sin(n\tau) + (\Im[\widetilde{F'}_{n-1}] - \Im[\widetilde{F'}_{n+1}]) \cos(n\tau) \quad \text{(A.32)}$$

using the trigonometric relationships.

By identification from (A.29) and (A.32), we have

$$\Re[\widetilde{F'}_{n-1}] - \Re[\widetilde{F'}_{n+1}] = 2n\Re[\widetilde{F}_n], \quad \text{(A.33)}$$

$$\Im[\widetilde{F'}_{n-1}] - \Im[\widetilde{F'}_{n+1}] = 2n\Im[\widetilde{F}_n], \quad \text{(A.34)}$$

$$2\Re[\widetilde{F'}_0] - \Re[\widetilde{F'}_2] = 2\Re[\widetilde{F}_1], \tag{A.35}$$

$$\Im[\widetilde{F'}_1] = 0, \tag{A.36}$$

and

$$-\Im[\widetilde{F'}_2] = 2\Re[\widetilde{F}_1]. \tag{A.37}$$

Combining the real and imaginary parts give

$$\widetilde{F'}_{n-1} - \widetilde{F'}_{n+1} = 2n\widetilde{F}_n \tag{A.38}$$

and

$$2\widetilde{F'}_0 - \widetilde{F'}_2 = 2\widetilde{F}_1. \tag{A.39}$$

For an input in quadrature with X_1, we have

$$E_{\Delta,n} = jE^{(Q)}_{\Delta,n} \tag{A.40}$$

and for a memoryless nonlinearity, the describing functions $\widetilde{F'_n}$ are real and using (A.17) we get

$$Y^{(Q)}_{\Delta,1} = \frac{\delta_{n-1}}{2}E^{(Q)}_{\Delta,n}\widetilde{F'}_{n-1} - \frac{\delta_n}{2}E^{(Q)}_{\Delta,n}\widetilde{F'}_{n+1}. \tag{A.41}$$

The quadrature-phase IDF is defined as

$$\widetilde{F}^{(Q)}_{\Delta,n} \equiv \frac{Y^{(Q)}_{\Delta,1}}{E^{(Q)}_{\Delta,n}}. \tag{A.42}$$

Combining (A.38), (A.39), (A.41) and (A.42), we get

$$\widetilde{F}^{(Q)}_{\Delta,n} = n\widetilde{F}_n. \tag{A.43}$$

A.3 Polynomial Nonlinearity of Degree Three

Many weakly nonlinear functions can be approximated with a polynomial of degree three or less. The output of the nonlinearity is

$$y = k_0 + k_1x + k_2x^2 + k_3x^3 \tag{A.44}$$

and is plotted in Figure A.1 for the case when $k_0 = 0$ and $k_2 = 0$ together with its derivative.

Since the polynomial is of degree three, we cannot have frequency components of higher frequency than three times that of the input when the

nonlinearity is fed with a sinusoid. The four non-zero describing functions are

$$\widetilde{F}_0(X_1) = \frac{Y_0}{X_1} = k_0\frac{1}{X_1} + \frac{1}{2}k_2X_1, \tag{A.45}$$

$$\widetilde{F}_1(X_1) = \frac{Y_1}{X_1} = k_1 + \frac{3}{4}k_3X_1^2, \tag{A.46}$$

$$\widetilde{F}_2(X_1) = \frac{Y_2}{X_1} = \frac{1}{2}k_2X_1, \tag{A.47}$$

and

$$\widetilde{F}_3(X_1) = \frac{Y_3}{X_1} = \frac{1}{4}k_3X_1^2. \tag{A.48}$$

The describing functions $\widetilde{F}_1$ and $\widetilde{F}_3$ are plotted in Figure A.2 for the case when $k_0 = 0$ and $k_2 = 0$.

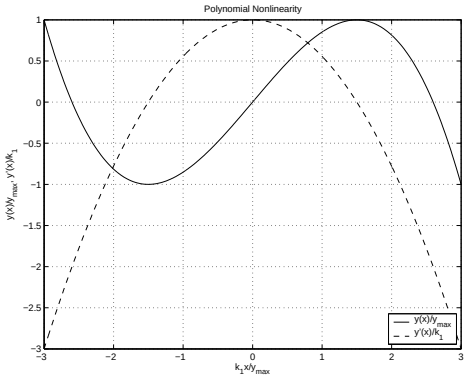


Figure A.1: Polynomial nonlinearity of degree three (solid) and its derivative (dashed).

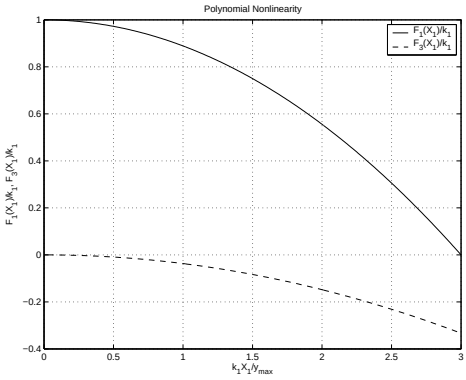


Figure A.2: Describing functions for nonlinearity of degree three.

A.4 Arc-tan Nonlinearity

The arc-tan nonlinearity is not a nonlinear function common in electronics (even though some nonlinearities may be approximated as an arc-tan function), but is nevertheless brought up here. The main reason for using it here is that it is possible to calculate the describing functions for this nonlinearity without approximations and it will thus be used in many examples where we like to see the error of other approximations and assumptions. The nonlinear function is written as

$$y = \frac{2y_{max}}{\pi}\arctan\left(\frac{\pi kx}{2y_{max}}\right), \tag{A.49}$$

and is plotted in Figure A.3 together with its derivative.

Since the function is odd, only describing functions for odd n are nonzero and these describing functions are given by

$$\widetilde{F}_n(X_1) = \frac{Y_n}{X_1} = (-1)^{\frac{n-1}{2}} \frac{\pi^{n-1} k^n X_1^{n-1}}{4^{n-1} n y_{max}^{n-1}} \left(\frac{2}{1 + \sqrt{1 + \left(\frac{\pi k X_1}{2 y_{max}}\right)^2}} \right)^n . \quad \text{(A.50)}$$

The first three non-zero describing functions

$$\widetilde{F}_1(X_1) = \frac{Y_1}{X_1} = k \frac{2}{1 + \sqrt{1 + \left(\frac{\pi k X_1}{2 y_{max}}\right)^2}}, \quad \text{(A.51)}$$

$$\widetilde{F}_3(X_1) = \frac{Y_3}{X_1} = -\frac{\pi^2 k^3 X_1^2}{48 y_{max}^2} \left(\frac{2}{1 + \sqrt{1 + \left(\frac{\pi k X_1}{2 y_{max}}\right)^2}} \right)^3 \quad \text{(A.52)}$$

and

$$\widetilde{F}_5(X_1) = \frac{Y_5}{X_1} = \frac{\pi^4 k^5 X_1^4}{1280 y_{max}^4} \left(\frac{2}{1 + \sqrt{1 + \left(\frac{\pi k X_1}{2 y_{max}}\right)^2}} \right)^5 \quad \text{(A.53)}$$

are plotted in Figure A.4.

When inserted in a feedback system where only the transfer function $\widetilde{H}_1$ for the fundamental is non-negligible, we get the amplitude at the input of the nonlinearity as

$$X_1 = \frac{4 y_{max} \widetilde{H}_1}{\pi} \sqrt{1 - \frac{1}{k \widetilde{H}_1}}, \quad \text{(A.54)}$$

where we have used that $\widetilde{F}_1 \widetilde{H}_1 = 1$ for a limit cycle.

The in-phase incremental describing function for the arc-tan nonlinearity is given by

$$\widetilde{F}_{\Delta,n}^{(I)} = \frac{\partial Y_n}{\partial X_1} = \frac{n \widetilde{F}_n}{\sqrt{1 + \left(\frac{\pi k X_1}{2 y_{max}}\right)^2}}, \quad \text{(A.55)}$$

where we have used (A.25).

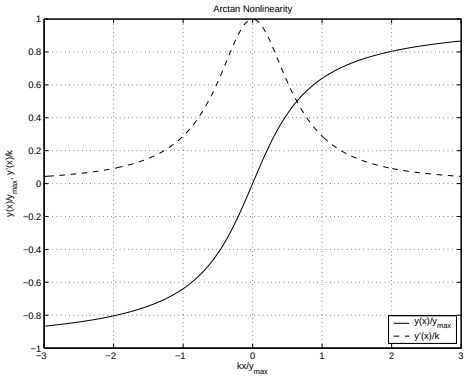


Figure A.3: Arc-tan nonlinearity (solid) and its derivative (dashed).

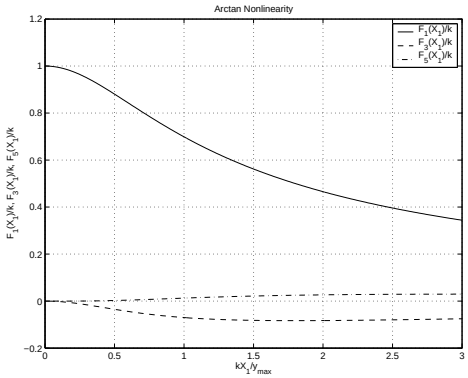


Figure A.4: Describing functions for arc-tan nonlinearity.

A.5 Tanhyp Nonlinearity

The tangens hyperbolicus nonlinearity appears for example in differential pairs based on bipolar transistors or MOSFETs operating in their weak-inversion regime. The transfer function is given by

$$y = y_{max} \tanh\left(\frac{kx}{y_{max}}\right), \tag{A.56}$$

which is plotted in Figure A.5 together with its derivative.

The describing function of this function cannot be calculated as an explicit expression, but may be approximated by

$$\widetilde{F}_1(X_1) = \frac{Y_1}{X_1} \approx \frac{k}{\sqrt{1 + \left(\frac{\pi k X_1}{4 y_{max}}\right)^2}}. \tag{A.57}$$

This approximate describing function is plotted together with the true describing function in Figure A.6.

Inserting this approximation in the equation for an oscillating feedback system, we get the approximate amplitude of the fundamental frequency component as

$$X_1 \approx \frac{4 y_{max} \widetilde{H}_1}{\pi} \sqrt{1 - \frac{1}{k^2 \widetilde{H}_1^2}}. \tag{A.58}$$

A.6 Clipping Nonlinearity

Many nonlinear system are modeled as linear systems up to the point where hard clipping occurs, possibly from supply voltage or current limitations.

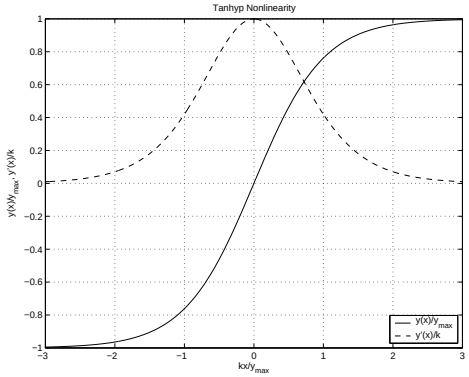


Figure A.5: Tanhyp nonlinearity (solid) and its derivative (dashed).

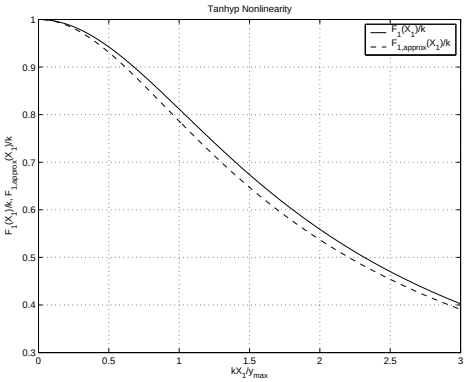


Figure A.6: First describing function for tanhyp nonlinearity. Both exact (solid) and approximate (dashed) values are shown.

The nonlinear function is given by

$$y = \begin{cases} -y_{max} & , x < -\frac{y_{max}}{k} \\ kx & , -\frac{y_{max}}{k} \leq x \leq \frac{y_{max}}{k} \\ y_{max} & , x > -\frac{y_{max}}{k}, \end{cases} \tag{A.59}$$

which is plotted in Figure A.7 together with its derivative.

The describing functions for this type of nonlinearity can be calculated exactly as

$$\widetilde{F}_1(X_1) = \frac{Y_1}{X_1} = \frac{4y_{max}}{\pi X_1}\left(\frac{kX_1}{2y_{max}}\arcsin\left(\frac{y_{max}}{kX_1}\right) + \frac{1}{2}\sqrt{1-\frac{y_{max}^2}{k^2X_1^2}}\right), \tag{A.60}$$

$$\widetilde{F}_3(X_1) = \frac{Y_3}{X_1} = -\frac{4y_{max}}{3\pi X_1}\left(1-\frac{y_{max}^2}{k^2X_1^2}\right)^{\frac{3}{2}} \tag{A.61}$$

and

$$\widetilde{F}_5(X_1) = \frac{Y_5}{X_1} = \frac{4y_{max}}{5\pi X_1}\left(1-\frac{y_{max}^2}{k^2X_1^2}\right)^{\frac{3}{2}}\left(1-\frac{8y_{max}^2}{3k^2X_1^2}\right), \tag{A.62}$$

but they are unfortunately somewhat complicated. These three describing functions are plotted in Figure A.8 as function of the input amplitude.

A.7 Limiter Nonlinearity

When driven hard enough, many amplifiers may be modeled as hard limiters where the output has either its minimum or maximum value, depending on

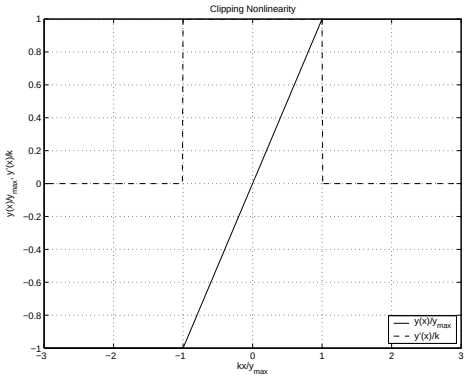


Figure A.7: Clipping nonlinearity (solid) and its derivative (dashed).

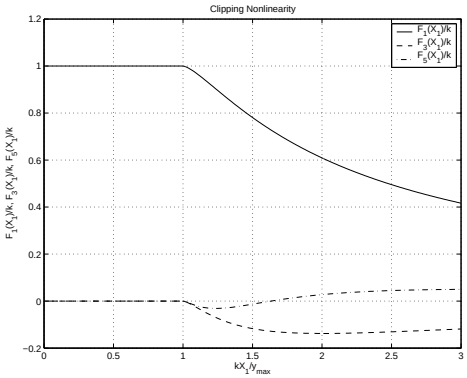


Figure A.8: Describing functions for clipping nonlinearity.

the input value. We model it as

$$y = y_{max}\text{sign}(x), \tag{A.63}$$

which is plotted in Figure A.9.

The describing functions have the simple form

$$\widetilde{F}_n(X_1) = \frac{Y_n}{X_1} = \begin{cases} 0 & \text{,if } n \text{ even} \\ (-1)^{\frac{n-1}{2}} \frac{4y_{max}}{n\pi|X_1|} & \text{,if } n \text{ odd} \end{cases} \tag{A.64}$$

and the three first nonzero describing functions are plotted in Figure A.10.

Inserted in a feedback system we get the amplitude as

$$X_1 = \frac{4y_{max}\widetilde{H}_1}{\pi}. \tag{A.65}$$

A.8 Exponential Nonlinearity

Exponential functions in electronics arises for example in the voltage–current relationships of diodes, bipolar transistors and MOSFETs operating in their weak inversion regimes. We model it as

$$y = y_0 e^{kx} \tag{A.66}$$

and get the describing functions as

$$Y_n(X_1) = \varepsilon_n y_0 I_n(kX_1), \tag{A.67}$$

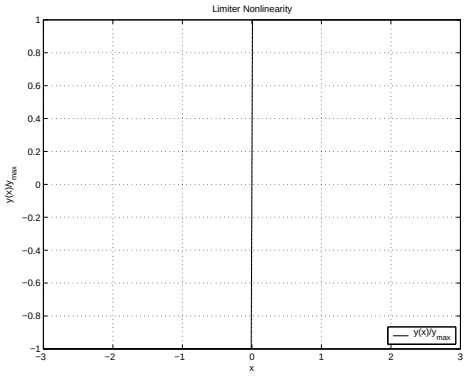


Figure A.9: Limiter nonlinearity.

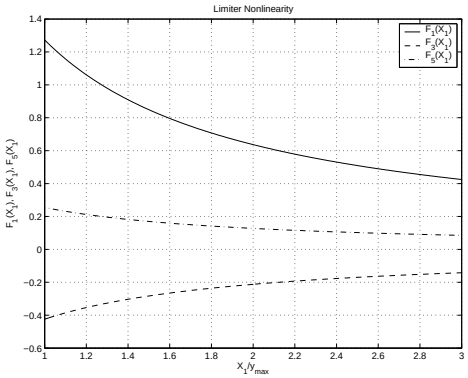


Figure A.10: Describing functions for limiter nonlinearity.

where ε_n is the Neumann factor equal to 1 when $n = 0$ and equal to 2 when $n \geq 1$, and I_n is the modified Bessel function of the first kind.

The modified Bessel function may be approximated as

$$I_n(x) \approx \begin{cases} \frac{x^n}{2^n n!} & , x \ll n \\ \\ \frac{e^x}{\sqrt{2\pi x}} & , x \gg n. \end{cases} \tag{A.68}$$

We are most often interested in the describing function for the fundamental, which we approximate with

$$\widetilde{F}_1(X_1, Y_0) = \frac{Y_1}{X_1} \approx \frac{kY_0}{\sqrt{1 + \frac{k^2 X_1^2}{4}}}, \tag{A.69}$$

which gives an error of less than 4%.

Using this approximation for the describing function we get the approximate amplitude in an oscillating feedback system as

$$X_1 \approx 2Y_0 \widetilde{H}_1 \sqrt{1 - \frac{1}{k^2 Y_0^2 \widetilde{H}_1^2}}. \tag{A.70}$$

A.9 Impulse Nonlinearity

When driven hard enough, some amplifiers like one-transistor stages produce an output which may be modeled as periodic impulses with the frequency components given by

$$Y_n(X_1) = 2Y_0(X_1). \tag{A.71}$$

We see that all frequency components have an amplitude twice that of the DC output value. Inserting this component in a feedback system, we get the amplitude at the input to the nonlinearity as

$$X_1 = 2Y_0\widetilde{H}_1. \tag{A.72}$$

Appendix B

Phase-Noise Spectrum

The phase-noise spectrum of an oscillator subject to random noise is derived in this appendix. The phase-noise spectrum is given as a function of the noise spectral density and the Impulse Sensitivity Function (ISF) at the noise injection point.

The derivations are based on those of Vanassche *et al* [Vanassche et al., 2003], but are modified to accommodate the somewhat different definition of the Impulse Sensitivity Function (ISF) used in this thesis.

We write the signal x somewhere within the oscillator as a sum according to

$$x(t) = x_s(\omega_0 t + \theta(t)) + \Delta x(t), \tag{B.1}$$

where x_s is the undisturbed steady-state solution, θ is the phase, and Δx is the orbital deviation.

The phase, θ, is described by the following differential equation:

$$\frac{d\theta}{dt} = \Gamma(\omega_0 t + \theta(t))n(t), \tag{B.2}$$

where Γ is the ISF and $n(t)$ is a stationary Gaussian process with autocorrelation

$$R_n(\tau) = \mathrm{E}[n(t+\tau)n(t)], \tag{B.3}$$

where E is the expectation operator.

Using the method of averaging [Freidlin and Wentzell, 1998], we can rewrite the differential equation as

$$\frac{d\theta}{dt} = \overline{n}(t), \tag{B.4}$$

where the over-line is used to denote averaging and $\overline{n}$ can be shown to be stationary and Gaussian with autocorrelation function, $R_{\overline{n}}$, given by

$$R_{\overline{n}}(\tau) = \mathrm{E}[\overline{n}(t+\tau)\overline{n}(t)] \approx \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} \Gamma(t+\frac{\tau}{2})\Gamma(t-\frac{\tau}{2})R_n(\tau)dt. \tag{B.5}$$

The variance for the phase change, defined as

$$V_\theta(\tau) = \mathrm{E}[(\theta(t+\tau)-\theta(t))^2], \tag{B.6}$$

fulfills the differential equation

$$\frac{d^2}{d\tau^2}V_\theta(\tau) = 2R_{\overline{n}}(\tau) \tag{B.7}$$

with the conditions

$$V_\theta(0) = 0 \tag{B.8}$$

and

$$\frac{d}{d\tau}V_\theta(0) = 0. \tag{B.9}$$

For $\tau > \tau_{noise}$, where τ_{noise} is the greatest correlation time for the noise, we have $R_{\overline{n}}(\tau) \approx 0$ and consequently

$$\frac{d}{d\tau}V_\theta(\tau) = \int_0^\tau 2R_{\overline{n}}(\tau)d\tau \approx \int_0^\infty 2R_{\overline{n}}(\tau)d\tau = S_{\overline{n}}(0), \tag{B.10}$$

where $S_{\overline{n}}$ is the spectral density for $\overline{n}$, and where we in the last stage have used the definition for the spectral density given by

$$S_{\overline{n}}(\omega) = \mathcal{F}[R_{\overline{n}}(\tau)] = \int_{-\infty}^{\infty} R_{\overline{n}}(\tau)e^{-j\omega\tau}d\tau, \tag{B.11}$$

where $\mathcal{F}$ is used to denote Fourier transformation.

The spectral density for the signal x is given by the Fourier transformation of the autocorrelation function, R_x, as

$$S_x(\omega) = \mathcal{F}[R_x(\tau)], \tag{B.12}$$

where

$$R_x(\tau) = \lim_{t\to\infty}\frac{1}{t}\int_{-\frac{t}{2}}^{\frac{t}{2}} \mathrm{E}[x(s+\tau)x^*(s)]ds. \tag{B.13}$$

Since the signal x is almost periodic, we can write it as a Fourier series according to

$$x(t) = \sum_{k=-\infty}^{\infty} X_k e^{jk(\omega_0 t+\theta(t))} \tag{B.14}$$

and we get

$$\overline{x(s+\tau)x^*(s)} \approx \sum_{k=-\infty}^{\infty} |X_k|^2 e^{jk\omega_0\tau} e^{jk(\theta(s+\tau)-\theta(s))}. \tag{B.15}$$

The autocorrelation function may now be approximated by

$$R_x(\tau) \approx \sum_{k=-\infty}^{\infty} |X_k|^2 e^{jk\omega_0\tau} e^{-\frac{k^2 V_\theta(\tau)}{2}}. \tag{B.16}$$

The autocorrelation for the k:th harmonic is thus given by

$$R_{x,k}(\tau) = e^{-\frac{k^2 V_\theta(\tau)}{2}} \tag{B.17}$$

with a spectral density given by

$$S_{x,k}(\omega) = \mathcal{F}[R_{x,k}(\tau)] = 2\int_0^\infty \cos(\omega\tau) e^{-\frac{k^2 V_\theta(\tau)}{2}} d\tau, \tag{B.18}$$

where we have used that $V_\theta(\tau) = V_\theta(-\tau)$

Performing a partial integration of this expression, we get

$$S_{x,k}(\omega) = \left[\frac{2}{\omega}\sin(\omega\tau) e^{-\frac{k^2 V_\theta(\tau)}{2}}\right]_0^\infty + \int_0^\infty \frac{k^2}{\omega}\left(\frac{d}{d\tau}V_\theta(\tau)\right)\sin(\omega\tau) e^{-\frac{k^2 V_\theta(\tau)}{2}} d\tau, \tag{B.19}$$

where the first term is zero since

$$\lim_{\tau\to\infty} V_\theta(\tau) = \infty. \tag{B.20}$$

Doing another partial integration, we get

$$\begin{aligned} S_{x,k}(\omega) = &\left[-\frac{k^2}{\omega^2}\left(\frac{d}{d\tau}V_\theta(\tau)\right)\cos(\omega\tau) e^{-\frac{k^2 V_\theta(\tau)}{2}}\right]_0^\infty + \\ &+ \int_0^\infty \frac{k^2}{\omega^2}\left(\left(\frac{d^2}{d\tau^2}V_\theta(\tau)\right) - \frac{k^2}{2}\left(\frac{d}{d\tau}V_\theta(\tau)\right)^2\right)\cos(\omega\tau) e^{-\frac{k^2 V_\theta(\tau)}{2}} d\tau, \end{aligned} \tag{B.21}$$

where the first term is zero due to (B.9) and (B.20).

We now have the spectral density as

$$S_{x,k}(\omega) = \frac{2k^2}{\omega^2}\int_0^\infty R_{\overline{n}}(\tau) R_{x,k}(\tau)\cos(\omega\tau) d\tau - \frac{k^4}{2\omega^2} S_{\overline{n}}^2(0)\int_0^\infty R_{x,k}(\tau)\cos(\omega\tau) d\tau \tag{B.22}$$

For input noise with short correlation time, we have $\cos(\omega\tau) \approx 1$ when $R_{\overline{n}}(\tau)$ is significant, and the spectral density becomes

$$S_{x,k}(\omega) \approx \frac{k^2}{\omega^2} S_{\overline{n}}(\omega) - \frac{k^4}{4\omega^2} S_{\overline{n}}^2(0) S_{x,k}(\omega). \tag{B.23}$$

Solving for the spectral density, we get

$$S_{x,k}(\omega) \approx \frac{\frac{k^2}{\omega^2} S_{\overline{n}}(\omega)}{1 + \frac{k^4}{4\omega^2} S_{\overline{n}}^2(0)}, \tag{B.24}$$

which in the case when the angular frequency, ω, fulfills

$$\omega \gg \frac{k^2}{2} S_{\overline{n}}^2(0) \tag{B.25}$$

can be approximated by

$$S_{x,k}(\omega) \approx \frac{k^2}{\omega^2} S_{\overline{n}}(\omega). \tag{B.26}$$

We are interested in the single-sided phase noise, $\mathcal{L}$, as a function of the single-sideband noise spectral density, S_y, which reads

$$\mathcal{L}[\omega_m] = \frac{S_{\overline{y}}(\omega_m)}{2\omega_m^2} = \frac{\overline{\Gamma^2 S_y}}{2\omega_m^2} \tag{B.27}$$

for large offset frequencies, ω_m.

Appendix C

Transistor Characteristics

In this appendix, I derive expressions for noise spectral densities and describing functions for bipolar and field-effect transistors as well as diodes when the transistor stages or diodes are driven by a sinusoidal input.

I assume in all discussions to follow that the transistors are operating in quasi-static fashion, that is, the terminal currents are momentary functions of the applied voltages to the transistors. All noise spectral densities are given as single-sided.

Oscillator-specific matters related to the calculation of noise from transistors are also given here, for example a discussion on which noise sources may be neglected and when it is allowed to do so.

C.1 Diode

The semiconductor diode treated in this section is assumed to be ideal, that is, it is assumed to have exponential I–V characteristics.

C.1.1 Large-Signal Characteristics

The diode current, i_D, is given by

$$i_D = I_S e^{\frac{v_{AC}}{V_T}}, \tag{C.1}$$

where I_S is a diode-specific constant, v_{AC} is the voltage over the diode, and V_T is the thermal voltage calculated as

$$V_T = \frac{k_B T}{q}, \tag{C.2}$$

where k_B is the Boltzmann constant, T is the absolute temperature, and q is the charge of an electron. In room temperature V_T is approximately 26 mV.

C.1.2 Small-Signal Characteristics

The small-signal conductance of a diode is

$$g_{ac} = \frac{\partial i_D}{\partial v_{AC}} = \frac{i_D}{V_T}. \tag{C.3}$$

The small-signal schematic for the diode is shown in Figure C.1 where any series resistance is omitted.

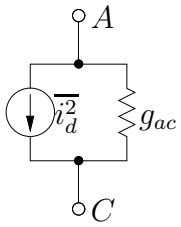


Figure C.1: Diode small-signal schematic.

C.1.3 Noise Sources

The white shot noise, here modeled as a noise current source in parallel with the diode, has a spectral density given by

$$\overline{i_d^2} = 2qi_D = 2k_BTg_{ac}. \tag{C.4}$$

C.1.4 Large-Signal Sinusoidal Operation

We assume that the voltage over the diode has a DC component, $V_{ac,0}$, and an AC component, $V_{ac,1}$, at the fundamental frequency, ω_0, according to

$$v_{AC} = V_{ac,0} + V_{ac,1}\cos(\omega_0 t). \tag{C.5}$$

From Section A.8 in Appendix A, we have the frequency components of the diode current as

$$I_{d,n} = \varepsilon_n I_S e^{\frac{V_{ac,0}}{V_T}} I_n\left(\frac{V_{ac,1}}{V_T}\right), \tag{C.6}$$

where ε_n is equal to 1 when $n = 0$ and equal to 2 when $n \geq 1$, and I_n is the modified Bessel function of the first kind.

The modified Bessel function may be approximated as

$$I_n(x) \approx \frac{e^x}{\sqrt{2\pi x}} \tag{C.7}$$

when $x \gg n$. Hence, we can approximate the frequency components, $I_{d,n}$, of the diode current as

$$I_{d,n} \approx \frac{\varepsilon_n I_S e^{\frac{V_{ac,0}+V_{ac,1}}{V_T}}}{\sqrt{2\pi \frac{V_{ac,1}}{V_T}}}. \tag{C.8}$$

The large-signal conductance for the fundamental frequency component is defined as

$$\widetilde{G}_1 = \frac{I_{d,1}}{V_{ac,1}}. \tag{C.9}$$

The incremental large-signal conductance is given by

$$\widetilde{G}^{(I)}_{\Delta,1} = \frac{\partial I_{d,1}}{\partial V_{ac,1}} \approx \frac{I_{d,1}}{V_T} = \widetilde{G}_1 \frac{V_{ac,1}}{V_T}, \tag{C.10}$$

where we have assumed that $V_{ac,1} \gg V_T$ in the approximation.

C.2 Bipolar Junction Transistor

We only discuss the modeling of the bipolar transistor here, since the operation of the transistor is discussed elsewhere [Getreu, 1976].

C.2.1 Large-Signal Characteristics

If we assume that the transistor operates in the active region, *i.e.* $v_{CE} \gtrsim 0.2$ V, the collector current is given as

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}, \tag{C.11}$$

where I_S is a transistor-specific constant, v_{BE} is the base–emitter voltage and V_T is the thermal voltage. The collector current is assumed to be a factor β higher than the base current given by

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{\frac{v_{BE}}{V_T}}. \tag{C.12}$$

C.2.2 Small-Signal Characteristics

The two most important small-signal parameters for the bipolar transistor are the transconductance, given by

$$g_m = \frac{\partial i_C}{\partial v_{BE}} = \frac{i_C}{V_T}, \tag{C.13}$$

and the base–emitter resistance, given by

$$r_{be} = \frac{1}{\frac{\partial i_B}{\partial v_{BE}}} = \frac{V_T}{i_B} = \frac{\beta}{g_m}. \tag{C.14}$$

The small-signal schematic for the bipolar transistor is shown in Figure C.2 where we have omitted any terminal resistances.

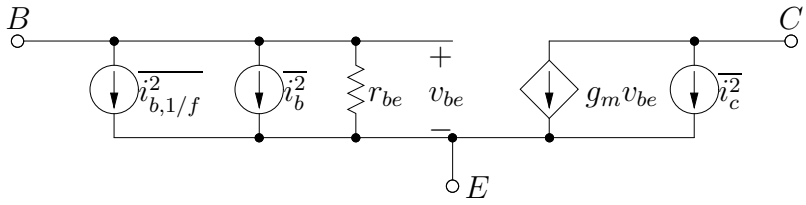


Figure C.2: BJT small-signal schematic.

C.2.3 Noise Sources

The major sources of noise in the bipolar transistors are the shot noise of the collector–emitter junction calculated as

$$\overline{i_c^2} = 2qI_C \tag{C.15}$$

and the shot noise of the base–emitter junction calculated as

$$\overline{i_b^2} = 2qI_B. \tag{C.16}$$

In addition to these noise sources, the series base resistance, r_b, also contributes thermal noise with a voltage-noise spectral density of

$$\overline{v_b^2} = 4k_B T r_b. \tag{C.17}$$

The noise from the series base resistance may be reduced to negligible levels compared to the shot noise in many cases, but not always.

Apart from the white noise sources, we also have 1/f noise originating from manufacturing imperfections. This noise is modeled as a noise current between the base and emitter with spectral density given by

$$\overline{i_b^2} = \frac{K_{1/f}}{f} I_B = \frac{K_{1/f}}{f} \frac{I_C}{\beta}, \tag{C.18}$$

where the constant $K_{1/f}$ depends on technology and is inversely proportional to the injecting emitter area.

Sometimes it is more convenient to give the collector–emitter shot noise as a function of the small signal parameter g_m and we get

$$\overline{i_c^2} = 2k_B T g_m. \tag{C.19}$$

C.2.4 Large-Signal Sinusoidal Operation

The large-signal transconductance, *i.e.* the describing function, of a bipolar transistor conducting constant DC current is shown in Figure C.3. We see

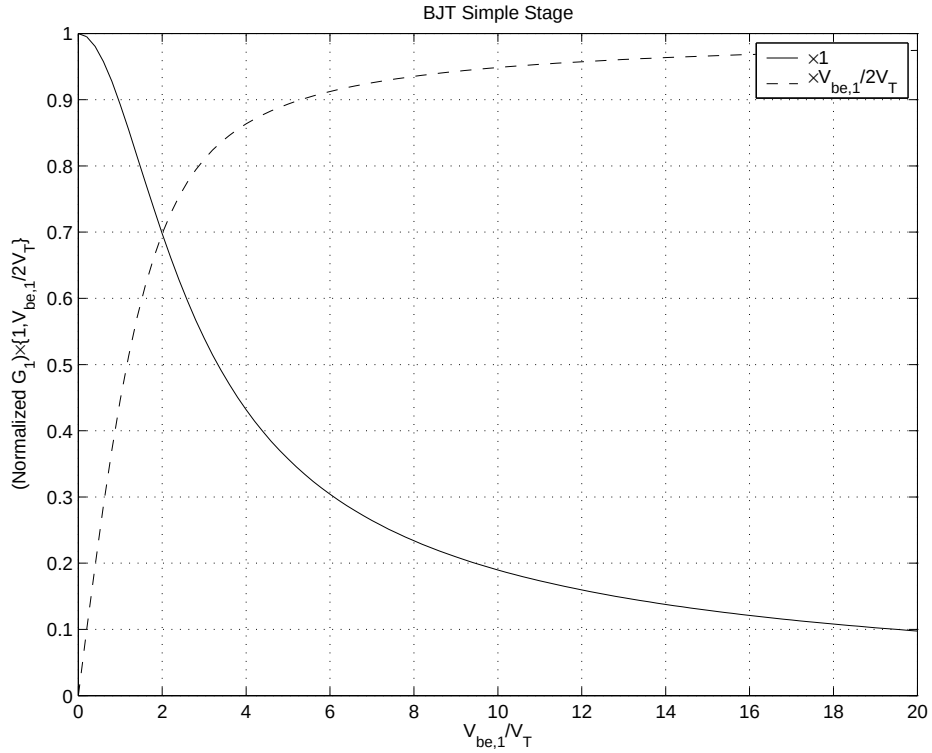


Figure C.3: Normalized describing function for a simple BJT stage.

that for an input-voltage amplitude $V_{be,1} \gtrsim 4V_T \approx 100$ mV, we can approximate the describing function with

$$\widetilde{G}_1 \approx -\frac{2I_{EE}}{V_{be,1}}, \tag{C.20}$$

where I_{EE} is the bias current.

We also want to know the peak current. We have from Appendix A that the DC current is given by

$$I_{EE} = I_S e^{\frac{V_{be,0}}{V_T}} I_0\left(\frac{V_{be,1}}{V_T}\right), \tag{C.21}$$

where I_0 is the modified Bessel function of the first kind, which can be approximated by

$$I_0\left(\frac{V_{be,1}}{V_T}\right) \approx \frac{e^{\frac{V_{be,1}}{V_T}}}{\sqrt{2\pi\frac{V_{be,1}}{V_T}}} \tag{C.22}$$

when $\frac{V_{be,1}}{V_T} \gg 0$. The peak emitter current is now given by

$$i_{E,max} = I_S e^{\frac{V_{be,0}+V_{be,1}}{V_T}} \approx I_{EE}\sqrt{2\pi\frac{V_{be,1}}{V_T}}. \tag{C.23}$$

When calculating the phase noise due to the series base resistance, we need to use the approximation of the following sum:

$$\sum_{n=1}^{\infty} \frac{n^2|\widetilde{G}_n|^2}{|\widetilde{G}_1|^2} \approx \frac{4}{9}\left(\frac{V_{be,1}}{V_T}\right)^{\frac{3}{2}}, \tag{C.24}$$

which is valid when $V_{be,1} \gg V_T$.

C.3 Field-Effect Transistor

We only discuss the modeling of the Field-Effect Transistor (FET) here, since the operation of the transistor is discussed elsewhere [Tsividis, 1999]. We use the common square-law model in the following. This model is only valid in strong inversion and when the electric fields within the transistor are low. The model is also known as the long-channel model.

C.3.1 Large-Signal Characteristics

Assuming that the transistor operates in the active region, *i.e.* $v_{DS} > v_{GS} - V_T$, we can calculate the drain current as

$$i_D = K(v_{GS} - V_T)^2 \tag{C.25}$$

where v_{GS} is the gate–source voltage, K is a technology dependent constant proportional to the width of the transistor and inversely proportional to the length of the transistor, and V_T is the threshold voltage of the transistor.

C.3.2 Small-Signal Characteristics

The most important small-signal parameter for the field-effect transistor is the transconductance given by

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = 2K(v_{GS} - V_T) = 2\sqrt{K i_D} = \frac{2i_D}{v_{GS} - V_T}. \tag{C.26}$$

The small-signal schematic for the FET is shown in Figure C.4.

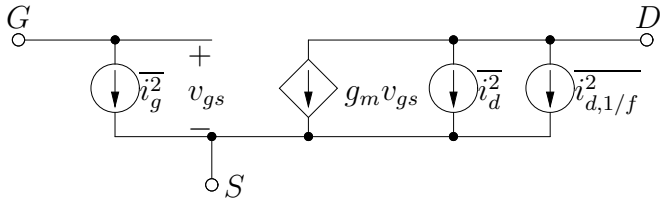


Figure C.4: FET small-signal schematic.

C.3.3 Noise Sources

The conducting channel produces a white noise of spectral density

$$\overline{i_d^2} = 4k_B T \gamma g_{d0}, \tag{C.27}$$

where g_{d0} is the small-signal conductance between drain and source for $v_{DS} = 0$, and γ is a constant ranging from 1 when the transistor operates in its linear region to 2/3 when the transistor operates in its active region. For a transistor obeying the square-law equation, we get the noise current spectral density in the active region as

$$\overline{i_d^2} = 4k_B T \gamma g_m, \tag{C.28}$$

where γ is approximately 2/3 for long-channel (low electric field) transistors operating in their active regions and up to 2–3 for short-channel transistors.

The same noise mechanism also produces an induced gate noise by capacitive coupling between the channel and the gate, modeled as a voltage noise with spectral density

$$\overline{v_g^2} = 4k_B T \delta r_g \tag{C.29}$$

with r_g given by

$$r_g = \frac{1}{5g_m} \tag{C.30}$$

and where δ is approximately 4/3 for long-channel (low electric field) transistors and up to 4–6 for short-channel transistors. There is correlation between the white drain noise and the gate induced noise since they have the same origin: noise in the conducting channel.

Sometimes it is more convenient to regard the gate induced noise as a current noise between the gate and source with the spectral density given by

$$\overline{i_g^2} = 4k_B T \delta r_g \omega^2 C_{GS}^2, \tag{C.31}$$

where C_{GS} is the gate–source capacitance, which is seen to have a noise spectral density increasing with frequency.

Apart from the white channel noise, we also have 1/f noise in the channel, originating from manufacturing imperfection, with a spectral density given by

$$\overline{i_d^2} = \frac{K_{1/f}}{f} I_D, \tag{C.32}$$

where the constant $K_{1/f}$ depends on technology and is inversely proportional to the active transistor area. The 1/f noise may be lower if the transistors are cycled between inversion and accumulation in operation [Bloom and Nemirovsky, 1991, Dierickx and Simoen, 1992].

C.3.4 Large-Signal Sinusoidal Operation

The large-signal transconductance, *i.e.* the describing function, of an FET conducting constant DC current is shown in Figure C.5 normalized to the small-signal transconductance.

We see that for an input-voltage amplitude $V_{gs,1} \gtrsim 2V_{GT0}$, where V_{GT0} is the overdrive voltage at start-up, we can approximate the describing function with

$$\widetilde{G}_1 \approx -\frac{2I_{SS}}{V_{gs,1}}, \tag{C.33}$$

using (C.26) and where I_{SS} is the bias current.

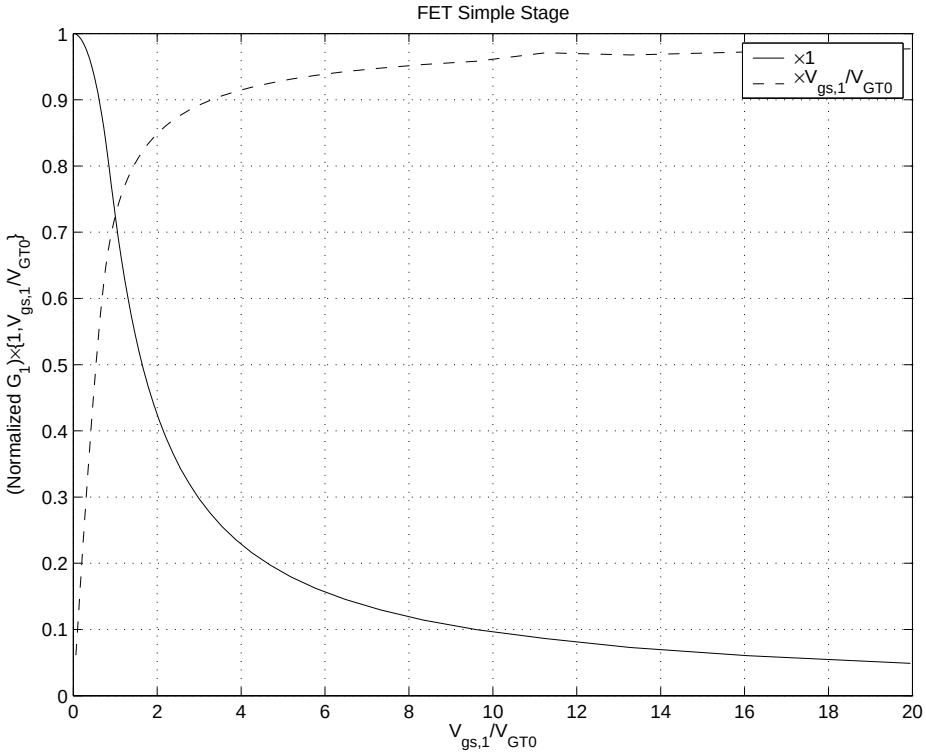


Figure C.5: Normalized describing function for a simple FET stage.

C.4 BJT Differential Stage

The schematic for a differential stage based on bipolar transistors is shown in Figure C.6.

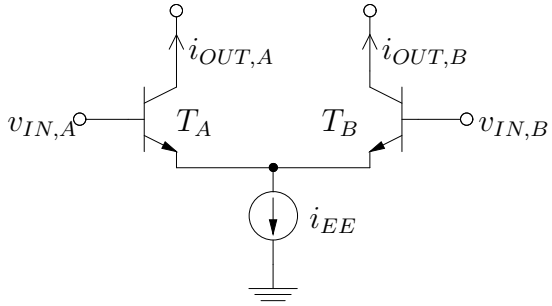


Figure C.6: Schematic of a BJT differential stage.

C.4.1 Large-Signal Characteristics

The input differential voltage is defined as

$$v_{IN} = v_{IN,A} - v_{IN,B}. \tag{C.34}$$

The differential output current is defined as

$$i_{OUT} = \frac{i_{OUT,A} - i_{OUT,B}}{2}, \tag{C.35}$$

that is, the current flowing from terminal A to terminal B. Given as a function of the differential input voltage v_{IN}, we have the output current as

$$i_{OUT} = -\frac{i_{EE}}{2} \tanh\left(\frac{v_{IN}}{2V_T}\right). \tag{C.36}$$

The normalized output current i_{OUT} is shown in Figure C.7 as a function of the input voltage v_{IN} normalized to V_T.

C.4.2 Small-Signal Characteristics

The small-signal transconductance from a differential input voltage to a differential output current is given by

$$G_m = \frac{\partial i_{OUT}}{\partial v_{IN}} = -\frac{i_{EE}}{4V_T \cosh^2\left(\frac{v_{IN}}{2V_T}\right)}, \tag{C.37}$$

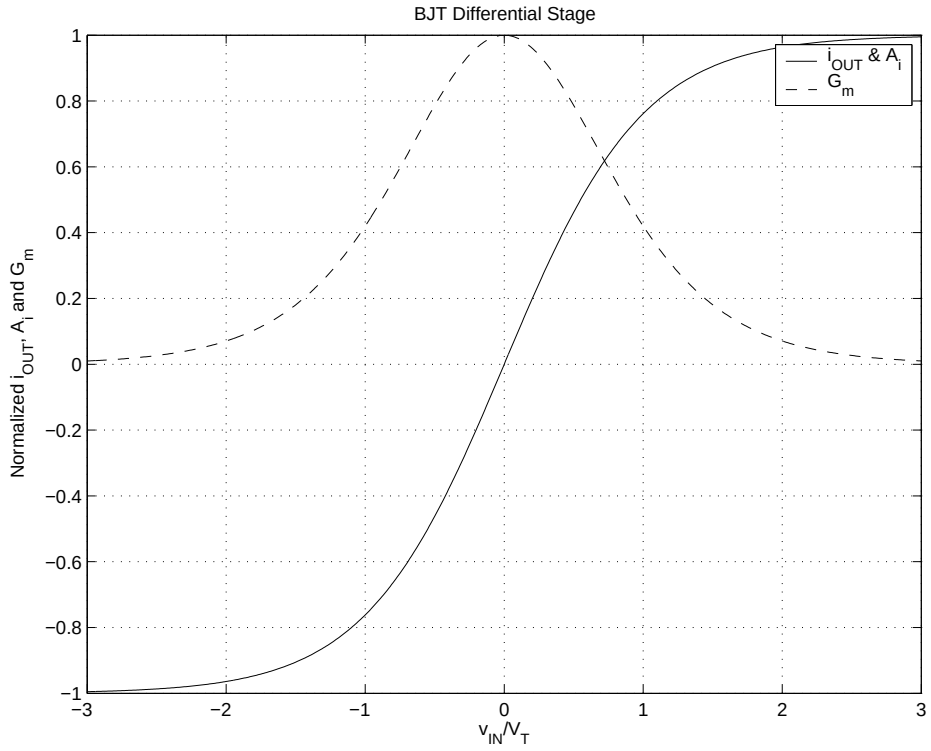


Figure C.7: Normalized output current, current gain and transconductance as function of input voltage normalized to V_T for a BJT differential stage.

which could also be written using the transconductances of the individual transistors as

$$G_m = -\frac{g_{mA}g_{mB}}{g_{mA}+g_{mB}}, \tag{C.38}$$

where g_{mA} and g_{mB} are the transconductances of transistor T_A and T_B, respectively.

The current gain from tail current to differential output current is given in large-signal parameters as

$$A_i = \frac{\partial i_{OUT}}{\partial i_{EE}} = -\frac{1}{2}\tanh\left(\frac{v_{IN}}{2V_T}\right) \tag{C.39}$$

or in small-signal parameters as

$$A_i = -\frac{1}{2}\frac{g_{mA}-g_{mB}}{g_{mA}+g_{mB}}. \tag{C.40}$$

The normalized small-signal transconductance and current gain are shown in Figure C.7 as function of the input voltage, v_{IN}, normalized to V_T.

C.4.3 Output Noise

The collector shot noise from the transistors are

$$\overline{i_{dA}^2} = 2k_BTg_{mA} \tag{C.41}$$

and

$$\overline{i_{dB}^2} = 2k_BTg_{mB}, \tag{C.42}$$

respectively. Summing these two noise contributions at the output, we get the total output noise as

$$\overline{i_{out}^2} = \overline{i_{dA}^2}\left(\frac{g_{mB}}{g_{mA}+g_{mB}}\right)^2 + \overline{i_{dB}^2}\left(\frac{g_{mA}}{g_{mA}+g_{mB}}\right)^2, \tag{C.43}$$

which can be rewritten as

$$\overline{i_{out}^2} = 2k_BT\frac{g_{mA}g_{mB}}{g_{mA}+g_{mB}} = 2k_BT|G_m|, \tag{C.44}$$

where we have used (C.38).

C.4.4 Large-Signal Sinusoidal Operation

The describing function of a bipolar transistor differential stage is shown in Figure C.8. We see that for an input-voltage amplitude $V_{in,1} \gtrsim 4V_T \approx 100$ mV we can approximate the describing function with

$$\widetilde{G}_1 \approx -\frac{2I_{EE}}{\pi V_{in,1}}, \tag{C.45}$$

where I_{EE} is the tail bias current.

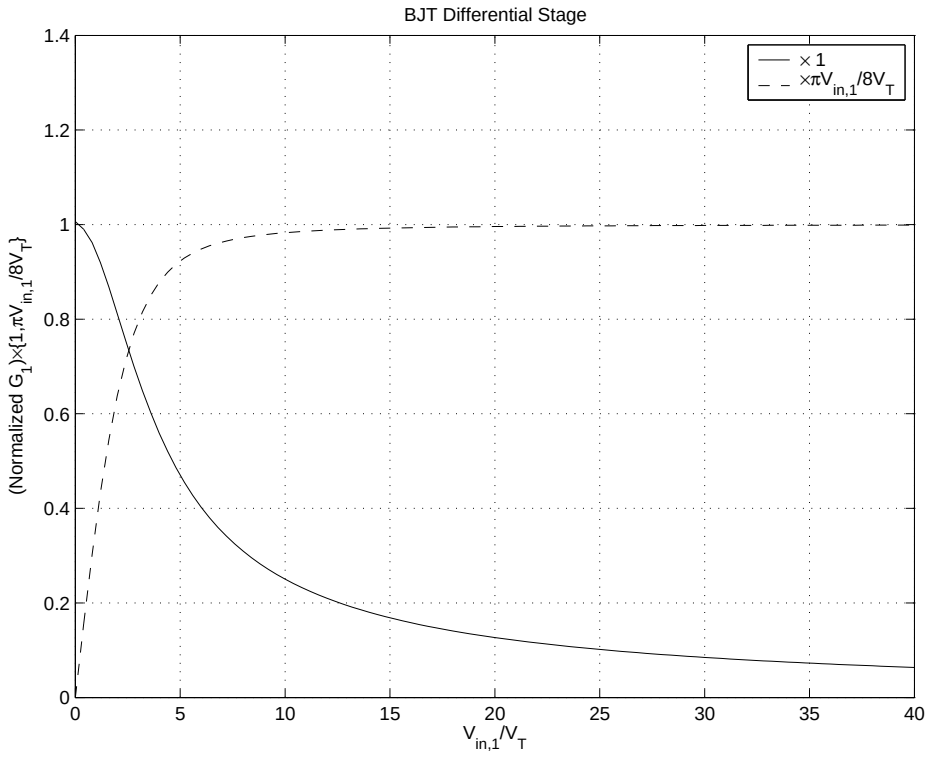


Figure C.8: Normalized describing function for a BJT differential stage.

The two factors K_{re} and K_{im}, defined in Section 7.2.5 and related to the noise conversion from the bias current source i_{EE} to the output, are plotted in Figure C.9 as function of the input amplitude, $V_{in,1}$, normalized to the thermal voltage, V_T.

When calculating the phase noise due to the series base resistance, we need to use the approximation of the following sum:

$$\sum_{n=1}^{\infty} \frac{n^2|\widetilde{G}_n|^2}{|\widetilde{G}_1|^2} \approx \frac{1}{4}\frac{V_{in,1}}{V_T}, \tag{C.46}$$

which is valid when $V_{in,1} \gg 2V_T$.

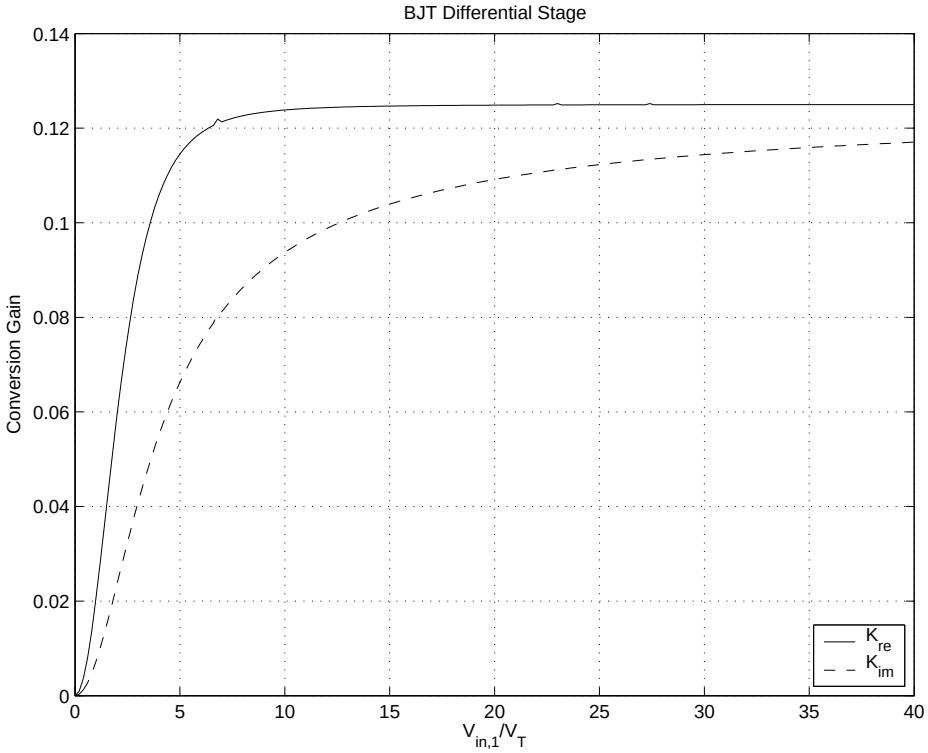


Figure C.9: Plot of K_{re} and K_{im} for BJT differential stage.

C.5 FET Differential Stage

The schematic for a differential stage based on FETs is shown in Figure C.10.

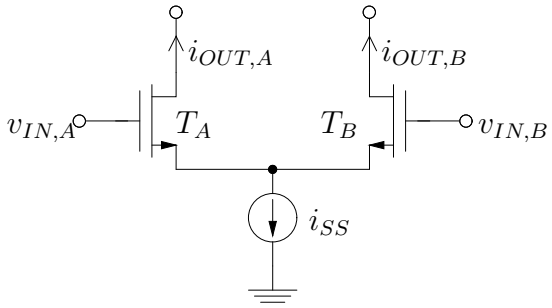


Figure C.10: Schematic of an FET differential stage.

C.5.1 Large-Signal Characteristics

The input differential voltage is defined as

$$v_{IN} = v_{IN,A} - v_{IN,B}. \tag{C.47}$$

The differential output current is defined as

$$i_{OUT} = \frac{i_{OUT,A} - i_{OUT,B}}{2}, \tag{C.48}$$

that is, the current flowing from terminal A to terminal B. Given as a function of the differential input voltage v_{IN} we have the output current as

$$i_{OUT} = \begin{cases} Kv_{GT0} & , v_{IN} \leq -\sqrt{2}v_{GT0} \\ -\frac{Kv_{IN}}{2}\sqrt{4v_{GT0}^2 - v_{IN}^2} & , -\sqrt{2}v_{GT0} > v_{IN} > \sqrt{2}v_{GT0} \\ -Kv_{GT0} & , v_{IN} \geq \sqrt{2}v_{GT0} \end{cases} \tag{C.49}$$

or as

$$i_{OUT} = \begin{cases} \frac{i_{SS}}{2} & , v_{IN} \leq -\sqrt{\frac{i_{SS}}{K}} \\ -\frac{Kv_{IN}}{2}\sqrt{\frac{2i_{SS}}{K} - v_{IN}^2} & , -\sqrt{\frac{i_{SS}}{K}} > v_{IN} > \sqrt{\frac{i_{SS}}{K}} \\ -\frac{i_{SS}}{2} & , v_{IN} \geq \sqrt{\frac{i_{SS}}{K}} \end{cases} \tag{C.50}$$

using that the overdrive voltage for the transistors at start-up is given by

$$v_{GT0} = \sqrt{\frac{i_{SS}}{2K}}. \tag{C.51}$$

A normalized plot of the output current as function of normalized input voltage is shown in Figure C.11.

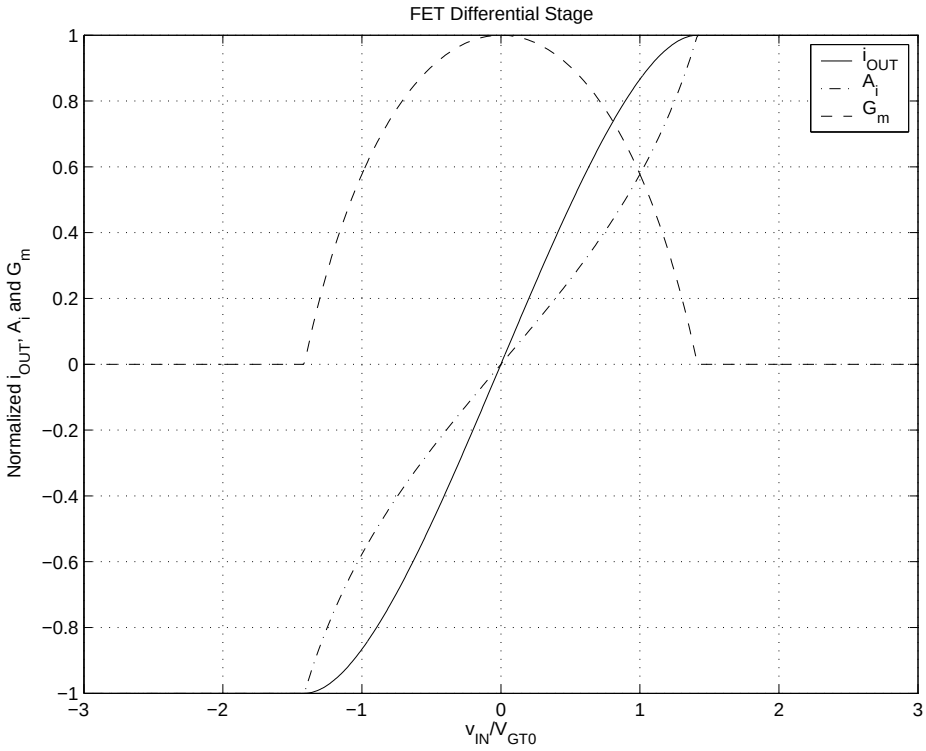


Figure C.11: Normalized output current, current gain and transconductance as function of input voltage normalized to V_{GT0} for an FET differential stage.

C.5.2 Small-Signal Characteristics

The small-signal transconductance defined as

$$G_m = \frac{\partial i_{OUT}}{\partial v_{IN}} \tag{C.52}$$

is given by

$$G_m = \begin{cases} 0 & , v_{IN} \leq -\sqrt{2}v_{GT0} \\ -\frac{K(2v_{GT0}^2 - v_{IN}^2)}{\sqrt{4v_{GT0}^2 - v_{IN}^2}} & , -\sqrt{2}v_{GT0} > v_{IN} > \sqrt{2}v_{GT0} \\ 0 & , v_{IN} \geq \sqrt{2}v_{GT0} \end{cases} \tag{C.53}$$

or by

$$G_m = \begin{cases} 0 & , v_{IN} \leq -\sqrt{\frac{i_{SS}}{K}} \\ -\frac{K\left(\frac{i_{SS}}{K} - v_{IN}^2\right)}{\sqrt{\frac{2i_{SS}}{K} - v_{IN}^2}} & , -\sqrt{\frac{i_{SS}}{K}} > v_{IN} > \sqrt{\frac{i_{SS}}{K}} \\ 0 & , v_{IN} \geq \sqrt{\frac{i_{SS}}{K}} \end{cases} \tag{C.54}$$

The small-signal current gain from the tail current source to the differential output current, defined as

$$A_i = \frac{\partial i_{OUT}}{\partial i_{SS}}, \tag{C.55}$$

is given by

$$A_i = \begin{cases} 0 & , v_{IN} \leq -\sqrt{2}v_{GT0} \\ -\frac{v_{IN}}{2\sqrt{4v_{GT0}^2 - v_{IN}^2}} & , -\sqrt{2}v_{GT0} > v_{IN} > \sqrt{2}v_{GT0} \\ 0 & , v_{IN} \geq \sqrt{2}v_{GT0} \end{cases} \tag{C.56}$$

or by

$$A_i = \begin{cases} 0 & , v_{IN} \leq -\sqrt{\frac{i_{SS}}{K}} \\ -\frac{v_{IN}}{2\sqrt{\frac{2i_{SS}}{K} - v_{IN}^2}} & , -\sqrt{\frac{i_{SS}}{K}} > v_{IN} > \sqrt{\frac{i_{SS}}{K}} \\ 0 & , v_{IN} \geq \sqrt{\frac{i_{SS}}{K}} \end{cases} \tag{C.57}$$

Normalized plots of transconductance, G_m, and current gain, A_i, as function of normalized input voltage, v_{IN}, are shown in Figure C.11.

The small-signal transconductance from differential input voltage to differential output current using the small-signal parameters of transistors is given by

$$G_m = -\frac{g_{mA}g_{mB}}{g_{mA} + g_{mB}}. \tag{C.58}$$

Likewise, the small-signal current gain from tail current to differential output current using the small-signal parameters of transistors is given by

$$A_i = \frac{1}{2}\frac{g_{mA} - g_{mB}}{g_{mA} + g_{mB}}. \tag{C.59}$$

C.5.3 Output Noise

The noise from the transistors is given by

$$\overline{i_{dA}^2} = 4k_B T\gamma g_{mA} \tag{C.60}$$

and

$$\overline{i_{dB}^2} = 4k_B T\gamma g_{mB}, \tag{C.61}$$

respectively. Adding the noise contributions to the output current from these two noise sources, we get the output current noise as

$$\overline{i_{out}^2} = \overline{i_{dA}^2}\left(\frac{g_{mB}}{g_{mA} + g_{mB}}\right)^2 + \overline{i_{dB}^2}\left(\frac{g_{mA}}{g_{mA} + g_{mB}}\right)^2 \tag{C.62}$$

which can be rewritten as

$$\overline{i_{out}^2} = 4k_B T\gamma\frac{g_{mA}g_{mB}}{g_{mA} + g_{mB}} = 4k_B T\gamma|G_m|, \tag{C.63}$$

where we have used (C.58).

C.5.4 Large-Signal Sinusoidal Operation

The describing function of an FET differential stage is shown in Figure C.12. We see that for an input-voltage amplitude $V_{in,1} \gtrsim 2V_{GT0}$, where V_{GT0} is the overdrive voltage of one transistor when conducting half the tail current, we may approximate the describing function with

$$\widetilde{G}_1 \approx -\frac{2I_{SS}}{\pi V_{in,1}}, \tag{C.64}$$

where I_{SS} is the tail bias current.

The two factors K_{re} and K_{im}, defined in Section 7.2.5 and related to the noise conversion from the bias current source, i_{SS}, to the output, are plotted in Figure C.13 as function of the input amplitude.

C.6 Contribution from Other Noise Sources

In this section we focus on the noise sources which are not considered above. We only deal with the small-signal case here.

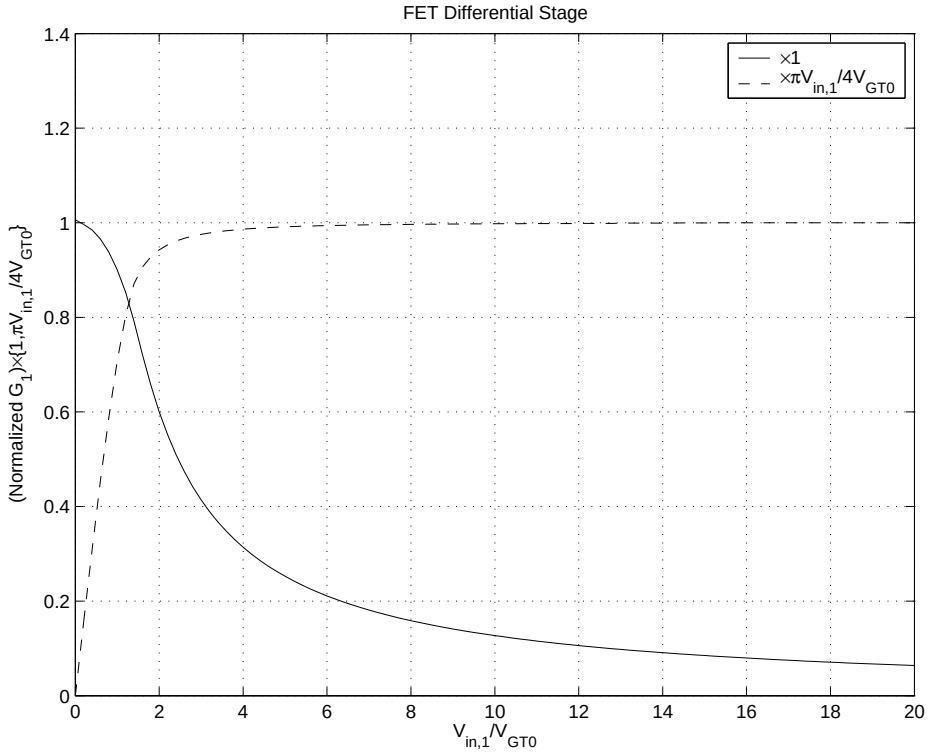


Figure C.12: Normalized describing function for an FET differential stage.

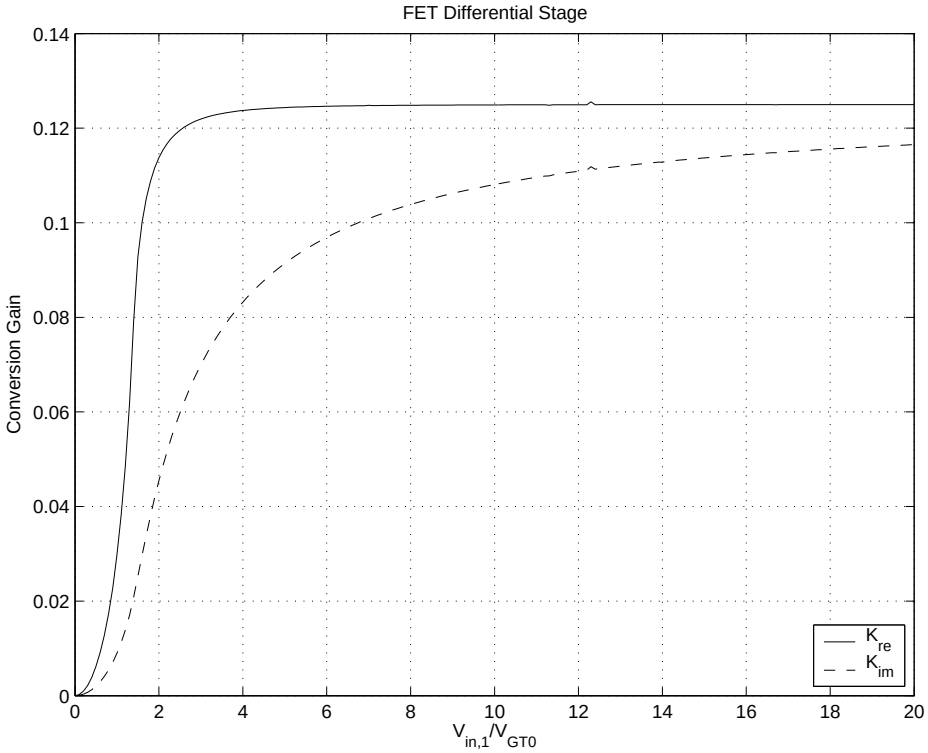


Figure C.13: Plot of K_{re} and K_{im} for FET differential stage.

C.6.1 Base–Emitter Resistance

We begin with the output impedance of the feedback network given by

$$Z_{22} = \frac{Z_{22}}{Z_{21}} Z_{21} \approx \frac{Z_{21}}{Z_{11}} \frac{1}{g_m}, \tag{C.65}$$

where we in the last approximation used that

$$Z_{21} = \frac{1}{g_m} \tag{C.66}$$

and assumed that $Z_{11}Z_{22} \approx Z_{21}^2$, which is the case for low-phase-noise oscillators. The base–emitter junction will contribute shot noise with a spectral density given by

$$\overline{i_b^2} = 2k_B T \frac{g_m}{\beta}. \tag{C.67}$$

Calculating the noise spectral density close to the fundamental frequency on the collector terminal, we arrive at

$$\overline{i_{c,b}^2} = \overline{i_b^2}\beta^2 \left(\frac{Z_{22}}{Z_{22} + \frac{\beta}{g_m}} \right)^2 \approx 2k_B T g_m \beta \left(\frac{\frac{Z_{21}}{Z_{11}} \frac{1}{g_m}}{\frac{Z_{21}}{Z_{11}} \frac{1}{g_m} + \frac{\beta}{g_m}} \right)^2, \tag{C.68}$$

where we in the last approximation have used (C.65). Rewriting this expression once more, we get

$$\overline{i_{c,b}^2} \approx 2k_B T g_m \beta \left(\frac{\frac{Z_{21}}{Z_{11}}}{\frac{Z_{21}}{Z_{11}} + \beta} \right)^2 \ll 2k_B T g_m = \overline{i_c^2}, \tag{C.69}$$

where we in the last comparison assume $\frac{Z_{21}}{Z_{11}} \leq 1$ and $\beta \gg 1$.

C.6.2 Induced Gate Noise

In the FET we have induced gate noise coupling from the conducting channel to the gate terminal with a spectral density of

$$\overline{i_g^2} = 4k_B T \delta r_g \omega^2 C_{GS}^2, \tag{C.70}$$

where $\delta \approx 2\gamma$ and

$$r_g = \frac{1}{5g_m}. \tag{C.71}$$

Combing these three expressions, we get

$$\overline{i_g^2} = \frac{8k_B T \gamma}{5g_m} \omega^2 C_{GS}^2, \tag{C.72}$$

which gives a noise spectral density around the fundamental frequency at the drain terminal of

$$\overline{i_{d,g}^2} = g_m^2 Z_{22}^2 \frac{8k_B T\gamma}{5g_m}\omega^2 C_{GS}^2 \approx \frac{2}{5}\frac{Z_{21}^2}{Z_{11}^2}4k_B T\gamma g_m \frac{\omega^2 C_{GS}^2}{g_m^2} = \frac{2}{5}\frac{Z_{21}^2}{Z_{11}^2}4k_B T\gamma g_m \frac{\omega^2}{\omega_T^2} \ll \overline{i_c^2}, \tag{C.73}$$

where we in the last comparison assume $\frac{Z_{21}}{Z_{11}} \leq 1$ and $\frac{\omega}{\omega_T} \ll 1$ where the transit frequency, ω_T, is defined as

$$\omega_T \equiv \frac{g_m}{C_{GS}}. \tag{C.74}$$

Appendix D

Two-Port Parameters

In this appendix, I give a short introduction to the modeling of passive two-port networks. In addition to the transfer functions, I also give the noise of a general two-port network described by its Z-parameters.

This appendix also contains a proof of a relationship for two-port networks described by Z-parameters. It gives a lower bound on the product of input resistance and output resistance in terms of the squared transfer resistance.

D.1 Two-Port Networks

Two-port networks have, as the name indicates, two ports as shown in Figure D.1.

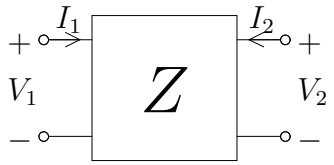


Figure D.1: Two-port network.

The relations between the four signal quantities, I_1, V_1, I_2 and V_2 can be described with four parameters. Depending on the use of the two-port, different descriptions may be suitable. In Table D.1, four different descriptions are given suited when the information signal is given as a current or voltage. There are more ways to describe a two-port network, for example chain-matrices which are useful when cascading several two-port networks. The properties of two-port networks are extensively covered in literature about network analysis and synthesis.

Table D.1: Types of two-ports.

Input	Output	Parameters
Voltage	Voltage	G
Voltage	Current	Y
Current	Voltage	Z
Current	Current	H

D.2 Z-Parameters

Z-parameters are best suited to model a two-port networks when the input signal is a current, I_1, and the output signal is a voltage, V_2. For a general two-port network, we have the relationships

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{D.1}$$

between the currents and voltages of the two ports. If the two-port network is reciprocal we also have that $Z_{12} = Z_{21}$.

The noise of a two-port network may be modeled by two noise sources, voltages and/or currents, with cross-correlation [Rothe and Dahlke, 1956, Bennett, 1960]. In the special case when the two-port network is passive and is not impedance loaded, the output noise voltage spectral density of the two-port network is simply

$$\overline{v_2^2} = 4k_B T \Re[Z_{22}], \tag{D.2}$$

assuming that all components in the two-port network have the same temperature, T. However, this result does not necessarily hold for time-varying networks [Coram et al., 2000].

D.3 Impedance Parameter Inequality

We assume that the two-port network is passive and hence reciprocal with $Z_{12} = Z_{21}$. Since we assume that the two-port network is passive, we must have an input impedance with positive real part for each port. We also assume that all Z-parameters are real.

Setting $I_2 = 0$, we have

$$Z_{11} \geq 0 \tag{D.3}$$

and setting $I_1 = 0$, we have

$$Z_{22} \geq 0. \tag{D.4}$$

Setting $V_1 = 0$, we have

$$Z_{22} - \frac{Z_{12}Z_{21}}{Z_{11}} \geq 0. \tag{D.5}$$

Combining (D.3), (D.4) and (D.5), we get

$$Z_{11}Z_{22} \geq Z_{21}^2. \tag{D.6}$$

The equality is fulfilled for example for a one-port network, which may be modeled by a two-port network with input and output ports connected together. In this case we have that $Z_{11} = Z_{12} = Z_{21} = Z_{22}$.

Appendix E

Definition of Q-value

In this appendix, we treat a few matters related to the definition of Q-value used in this thesis. In addition to a discussion of the connection between the Q-value and indirect frequency stability, we show that the definition gives us a positive Q-value.

We choose to define the Q-value for an oscillator as

$$Q \equiv -\frac{\omega_0}{2}\left(\frac{\partial\alpha}{\partial\omega}+\frac{\partial\zeta}{\partial\omega}\right). \tag{E.1}$$

The indirect frequency stability, S_F, is defined as

$$S_F \equiv \omega_0\left(\frac{\partial\alpha}{\partial\omega}+\frac{\partial\zeta}{\partial\omega}\right) = -2Q \tag{E.2}$$

and is a measure of the frequency sensitivity against change in the loop phase, $\alpha+\zeta$.

E.1 Sign of Q-value

In this section, we show that the definition of Q above gives a positive value for stable limit cycles.

To make this derivation simple, we assume that the feedback network determines the frequency and does not depend on the amplitude, according to

$$\widetilde{H}_1(\omega) = A(\omega)e^{j\alpha(\omega)}. \tag{E.3}$$

We also assume that the active part determines the amplitude and does not depend on the frequency and is given by

$$\widetilde{F}_1(X_1) = B(X_1), \tag{E.4}$$

where X_1 is the amplitude of the input signal to the active part at the fundamental frequency. This last assumption simplifies the Q-value to

$$Q = -\frac{\omega_0}{2}\frac{\partial\alpha}{\partial\omega}. \tag{E.5}$$

For a limit cycle, the Barkhausen criterion given as

$$\widetilde{H}_1(\omega)\widetilde{F}_1(X_1) = 1 \tag{E.6}$$

is fulfilled.

Considering only the fundamental tone, we have the limit cycle signal as $\Re[X_1 e^{j\omega_0 t}]$. Consider now a perturbation that changes the amplitude from X_1 to $X_1 + X_{\Delta,1}$ and the complex frequency from ω_0 to $\omega_0 + \omega_\Delta + j\sigma_\Delta$. If the oscillator is to return to its limit cycle, σ_Δ must be positive for the new factor $e^{-\sigma_\Delta}$ to converge to unity.

We rewrite the Barkhausen criterion as

$$Ae^{j\alpha(\omega)}B_1(X_1) = 1. \tag{E.7}$$

If we Taylor expand this expression and keep only the first term, we get

$$(\omega_\Delta + j\sigma_\Delta)\left(B_1(\omega)\frac{\partial A_1(\omega)}{\partial\omega} + j\frac{\partial\alpha(\omega)}{\partial\omega}\right) + X_{\Delta,1}A(\omega)\frac{\partial B_1(X_1)}{\partial X_1} = 0. \tag{E.8}$$

This expression can be split into its real part, given by

$$\omega_\Delta B_1(\omega)\frac{\partial A_1(\omega)}{\partial\omega} - \sigma_\Delta\frac{\partial\alpha(\omega)}{\partial\omega} + X_{\Delta,1}A(\omega)\frac{\partial B_1(X_1)}{\partial X_1} = 0, \tag{E.9}$$

and its imaginary part, given by

$$\omega_\Delta\frac{\partial\alpha(\omega)}{\partial\omega} + \sigma_\Delta B_1(\omega)\frac{\partial A_1(\omega)}{\partial\omega} = 0. \tag{E.10}$$

Eliminating ω_Δ from these two equations, we get

$$X_{\Delta,1}A(\omega)\frac{\partial B_1(X_1)}{\partial X_1}\frac{\partial\alpha(\omega)}{\partial\omega} = \sigma_\Delta\left(\left(\frac{\partial\alpha(\omega)}{\partial\omega}\right)^2 + \left(B_1(\omega)\frac{\partial A_1(\omega)}{\partial\omega}\right)^2\right). \tag{E.11}$$

Since we want σ_Δ to be positive for a positive amplitude step $X_{\Delta,1}$, the following inequality must hold:

$$A(\omega)\frac{\partial B_1(X_1)}{\partial X_1}\frac{\partial\alpha(\omega)}{\partial\omega} > 0. \tag{E.12}$$

We finally assume that the absolute value of the describing function $\widetilde{F}_1(X_1) = B(X_1)$ is a monotonously decreasing function of the amplitude X_1 around the limit cycle and thereby get

$$\frac{\partial \alpha(\omega)}{\partial \omega} < 0, \tag{E.13}$$

which in turn gives a positive value for the quality factor Q when inserted in (E.5).

Appendix F

Spiral Inductors

When using spiral inductors on chip, we usually want inductors with a high Q-value (quality factor). The Q-value depends on the process and area, but also on the layout. In this appendix, the layout that maximizes the Q-value for a given process and area consumption is derived.

We use the modified Wheeler formula [Mohan et al., 1999], which gives the inductance of a planar spiral inductor as

$$L = \frac{K_1 \mu_0 n^2 d_{avg}}{1 + K_2 \rho}, \tag{F.1}$$

where ρ is the fill ratio defined as

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{F.2}$$

and d_{avg} is the average diameter of the spiral inductor, calculated as

$$d_{avg} = \frac{d_{out} + d_{in}}{2}. \tag{F.3}$$

The coefficients K_1 and K_2 are layout dependent and are given in Table F.1. The different layouts are shown in Figure F.1.

The number of turns can be calculated as

$$n = \frac{d_{out} - d_{in}}{2(w + s)}, \tag{F.4}$$

where w is the turn width and s is the turn spacing.

For lower frequencies where the losses in the substrate can be neglected, the losses are mainly due to the series resistance of the inductor, which is calculated as

$$R = \frac{K_3 R_S n d_{avg}}{w}, \tag{F.5}$$

Table F.1: Coefficients for inductance, resistance and Q-value expressions.

Layout	K_1	K_2	K_3	K_4	K_5	ξ_{opt}
Square	2.34	2.75	4.00	0.0828	0.0828	0.248
Hexagonal	2.33	3.82	3.46	0.0771	0.0828	0.323
Octagonal	2.25	3.55	3.31	0.0816	0.0897	0.307

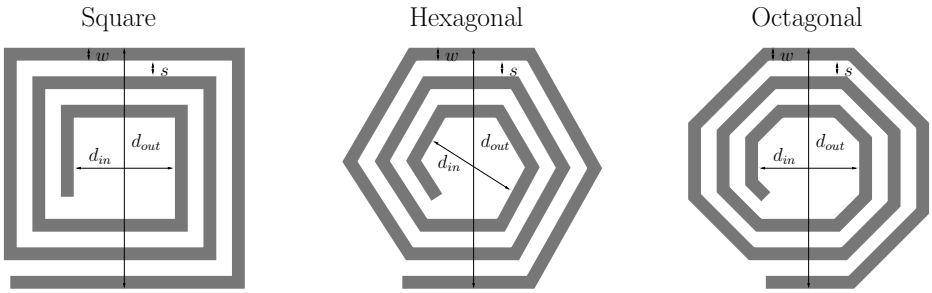


Figure F.1: Spiral inductor geometries.

where R_S is the sheet resistance of the conductor (including possible skin effect) and K_3 is a coefficient which gives the length of one turn when multiplied with the diameter of that turn (and would be equal to π for a circular inductor). Values for the coefficient K_3 are given in Table F.1 for the different layouts.

The Q-value of an inductor is by definition

$$Q \equiv \frac{\omega L}{R} = \frac{\omega K_1 \mu_0 d_{out} w}{2K_3 R_S (w+s)} \frac{1-\xi^2}{1+K_2+\xi(1-K_2)}, \tag{F.6}$$

where we define the ratio between inner and outer diameter as

$$\xi = \frac{d_{in}}{d_{out}}. \tag{F.7}$$

We calculate the ξ that gives maximum Q-value by taking the derivative of the second fraction and equating to zero. We get the following optimum ratio:

$$\xi_{opt} = \frac{\sqrt{K_2}-1}{\sqrt{K_2}+1} \tag{F.8}$$

with the following expression for Q-value when $\xi = \xi_{opt}$:

$$Q_{opt} = \frac{\omega K_4 \mu_0 d_{out} w}{R_S (w+s)}, \tag{F.9}$$

where

$$K_4 = \frac{K_1}{2K_3} \frac{1 - \xi_{opt}^2}{1 + K_2 + \xi_{opt}(1 - K_2)}. \tag{F.10}$$

Values for the optimum ratio ξ_{opt} and the coefficient K_4 are given in Table F.1.

The different layouts have different area, A, for the same outer diameter, d_{out}, which makes comparisons based on the expression above misleading. Rewriting (F.9), we get

$$Q_{opt} = \frac{\omega K_5 \mu_0 \sqrt{A} w}{R_S(w + s)}, \tag{F.11}$$

where K_5 is a coefficient with the values given in Table F.1 for different layouts. As seen from the values in Table F.1, the three different layouts give approximately the same Q-value. We also see that the Q-value is not strongly dependent on ξ close to the optimum at $\xi = \xi_{opt}$ in Figure F.2.

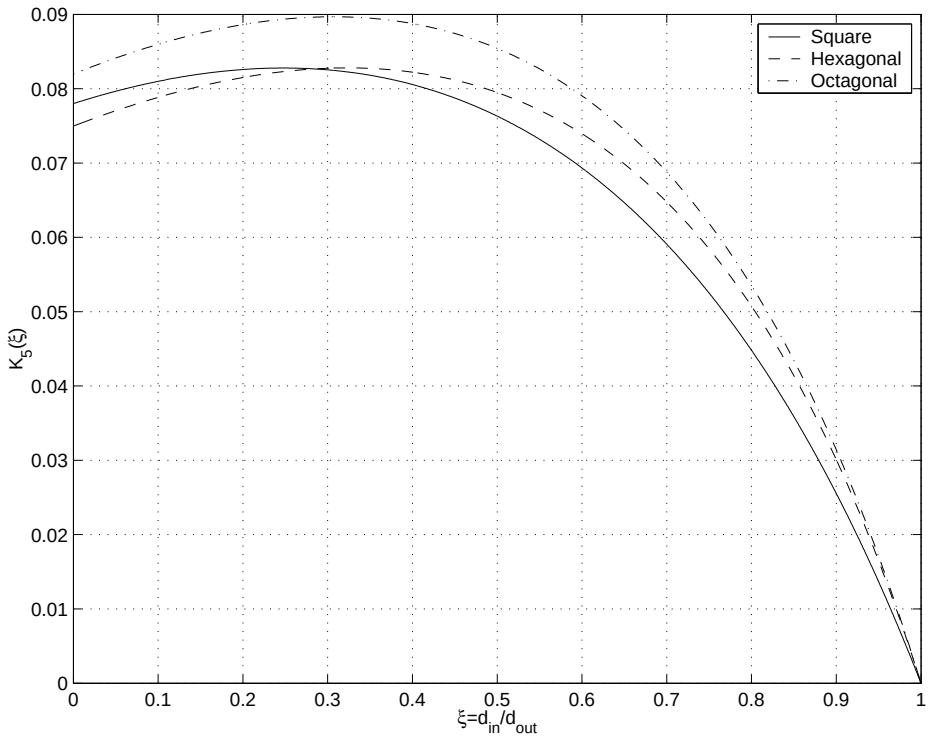


Figure F.2: Plot of coefficient K_5 as function of the ratio $\xi = d_{in}/d_{out}$ for three different inductor layouts.

The layouts of inductors used in the calculations of this appendix are not the optimal ones and better performance can be achieved if one do not use fixed conductor widths and spacings. If the substrate losses are not negligible,

special arrangements such as shielding may reduce these losses and increase the Q-value.

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