Thesis for the Degree of Licentiate of Engineering

Fabrication of Integrated HBV Multipliers for THz Generation

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Cover: *Left:* SEM image of a silicon integrated heterostrucutre barrier varactor diode. *Right:* TEM composite image of the transferred HBV material on silicon substrate. *Top:* Magnified $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$/ AlAs; *bottom:* bonding interface showing ca 5 nm thick amorphous oxide at the $In_{0.53}Ga_{0.47}As$/ Si interface.

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Abstract

The main objective of this licentiate thesis is to demonstrate silicon integrated HBV frequency multipliers for THz generation with RF performance comparable with InP technology. The choice of silicon is motivated by better thermal and mechanical properties, cost and ease of integration compared to III-V semiconductor substrates. Moreover, micromachining of silicon allows fabrication of membranes, antennas and waveguides suitable for THz frequencies.

A W-band silicon integrated frequency tripler is demonstrated. Plasma assisted wafer bonding was utilised to integrate InP-based HBV material on silicon substrate. The transferred material was characterised using: atomic force microscopy, transmission electron microscopy, X-ray diffractometry and Auger spectroscopy. The maximum output power measured for this device was more than 180 mW, corresponding to 23 % of efficiency. For comparison, a monolithically integrated HBV frequency multiplier on InP substrate was fabricated and demonstrated. The peak efficiency and output power for both the Si and the InP based tripler are comparable.

Finally, a fix tuned 175 GHz frequency quintupler is presented. The multiplier is based on a single HBV diode that is flip-chip soldered into a microstrip matching circuit. The circuit is fabricated from AlN substrate, a material that has a good thermal conductivity. This device delivers 60 mW output power corresponding to 6.3 % of efficiency.

Keywords: Epitaxial transfer, frequency multipliers, heterogeneous integration, heterostructure barrier varactors, indium phosphide, power sources, silicon.

List of publications

Appended papers

This thesis is based on the following publications:

[A] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "Silicon Integrated InGaAs/ InAlAs/ AlAs HBV Frequency Tripler", *submitted to IEEE Electron Device Letters*, 2013.

[B] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "High Efficiency and Broad-Band Operation of Monolithically Integrated W-Band HBV Frequency Tripler," *24^{th} International Conference on Indium Phosphide and Related Materials*, Santa Barbara, USA, 27-30 August 2012.

[C] T. Bryllert, A. Malko, J. Vukusic, and J. Stake, "A 175 GHz HBV Frequency Quintupler With 60 mW Output Power," *IEEE Microwave and Wireless Components Letters*, vol. 22 no. 2, pp. 76-78, February 2012.

Other papers and publications

The following publications are not included in this thesis due to an overlap in the content or the content is beyond the scope of this thesis.

[a] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "Integrated III-V Heterostructure Varactor Frequency Tripler on a Silicon Substrate," *7^{th} European Microwave Integrated Circuits Conference*, Amsterdam, Netherlands, 2012.

[b] J. Stake, T. Bryllert, R. Dahlbäck, V. Drakinskiy, J. Hanning, A. Malko, A. Y. Tang, J. Vukusic, H. Zhao, and P. Sobis, "Integrated Terahertz Electronics for Imaging and Sensing," *19^{th} International Conference on Microwaves, Radar and Wireless Communications*, pp. 122-123, Warsaw, Poland, 2012.

[c] A. Malko, J. Liljedahl, T. Bryllert, J. Vukusic, and J. Stake, "Investigation of passivation methods for HBV diodes," *GigaHertz Symposium*, Lund, Sweden, 2010.

[d] J. Stake, T. Bryllert, P. Sobis, A. Y. Tang, H. Zhao, J. Vukusic, A. Malko, V. Drakinskiy, A. Ø. Olsen, and A. Emrich, "Development of Integrated Submillimeter Wave Diodes for Sources and Detectors," *5^{th} European Microwave Integrated Circuits Conference*, pp. 226-229, Paris, France, 2010.

List of abbreviations

ADS	Advanced Design System
AFM	Atomic Force Microscope
AlN	Aluminium Nitride
Au	Gold
BHF	Buffered Hydrofluoric acid
CH_4	Methane
CMOS	Complementary Metal Oxide Semiconductor
CS	Compliant Substrate
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
D	Diamond crystal structure
DC	Direct Current
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GHz	Gigahertz (10^9 Hz)
HBV	Heterostrucutre Barrier Varactor
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HFSS	High Frequency Structure Simulator
IMPATT	IMPact-ionization Avalanche Transit Time
InP	Indium Phosphide
IF	Intermediate Frequency
IR	Infrared
LO	Local Oscillator
LT	Low Temperature
MBE	Molecular Beam Epitaxy
MEMS	Micro-Electro-Mechanical System
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Microwave Monolithic Integrated Circuit
MOCVD	Metal-Organic Chemical Vapor Deposition
Ni	Nickel
Pd	Palladium
PMGI	Polydimethylglutarimide

RF	Radio Frequency
RCA	A standard silicon wet chemical clean
RT	Room Temperature
RTA	Rapid Thermal Annealing
SD	Schottky Diode
SI	Semi-insulating
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SiO_2	Silicon Dioxide
SI	Semi-Insulating
SEM	Scanning Electron Microscope
SOI	Silicon-On-Insulator
STO	Strontium Titanate
TEM	Transmission Electron Microscope
Ti	Titanium
THz	Terahertz (10^{12} Hz)
UV	Ultraviolet
W	Wurtizte crystal strucutre
XRD	X-Ray Diffraction
ZB	Zinc Blende crystal strucutre

List of notations

A	Device area
b	Barrier width
C_j	Junction capacitance
d	Lattice constant
ΔS	Elastance swing
E_d	Electric field in modulation layer
E_g	Energy gap
ϵ_0	Permittivity in vacuum
ϵ_b	Dielectric constant of the barrier material
ϵ_d	Dielectric constant of the modulation material
ϵ_r	Dielectric constant
η	Efficiency
f	Frequency
f_c	Dynamic cut-off frequency
f_p	Pump frequency
k	Boltzman constant
κ	Thermal conductivity
L_d	Debye length
L_n	Conversion loss
n	Multiplication factor
N	Number of barriers
N_d	Doping concentration
ω	Angular frequency
$\mathrm{P}_{IN,AVA}$	Available input power
$\mathrm{P}_{OUT,AVA}$	Available output power
q	Elementary charge
R_s	Series resistance
S_{11}	Power reflected
s	Spacer width
S	Differential elastance
T	Temperature
$\tan\,\delta$	Loss tangent
w	Depletion width
V_{br}	Breakdown voltage
V_d	Voltage across depleted region

Contents

Chapter 1

Introduction

A growing interest for applications operating at terahertz (THz) frequencies has been observed [1, 2]. The main areas of interest are radio astronomy, climate and atmosphere science, wireless communication, security imaging and biology. The active components for these applications utilise mainly the III-V compound semiconductors. These operate at room temperature, and do not require an additional cooling. The III-Vs offer direct bandgap and high carrier mobilities. In addition, the epitaxial growth allows for fabrication of complex structures. However, materials like InP and GaAs are fragile, expensive and are limited to small wafer sizes. Moreover, these materials have relatively low thermal conductivity, which when driven with high input power limits the performance of the active devices. Hence, heterogenous integration of III-Vs on other materials like silicon is an interesting solution. Silicon offers large scale of integration and two times higher thermal conductivity than InP or GaAs. Additionally, it is robust and is suitable for micromachining of complex 3D structures [3]. Furthermore, silicon is compatible with CMOS technology. Therefore, the integration of III-Vs on silicon substrates is a very attractive approach. This integration will result in an additional degree of freedom in the circuit design and fabrication. Taking advantage of the micromechanical properties of silicon, the high frequency active devices on membranes, integrated with waveguide modules and their components will be possible [4, 5]. Both epitaxial growth and epitaxial transfer techniques have been used for the integration of III-Vs on silicon substrate [6]. Among the microwave applications utilising circuitry on silicon and III-Vs for active components MESFETs [7], HBTs [8,9] and GaN HEMTs [10] can be distinguished.

The main part of this licentiate thesis is dedicated to a silicon integrated HBV based frequency tripler. The InP-based material was transferred onto silicon carrier wafer utilising the epitaxial transfer technique. The performance of the developed device motivates further development of applications operating at THz frequencies, taking advantage of silicon micromachining properties and CMOS compatibility.

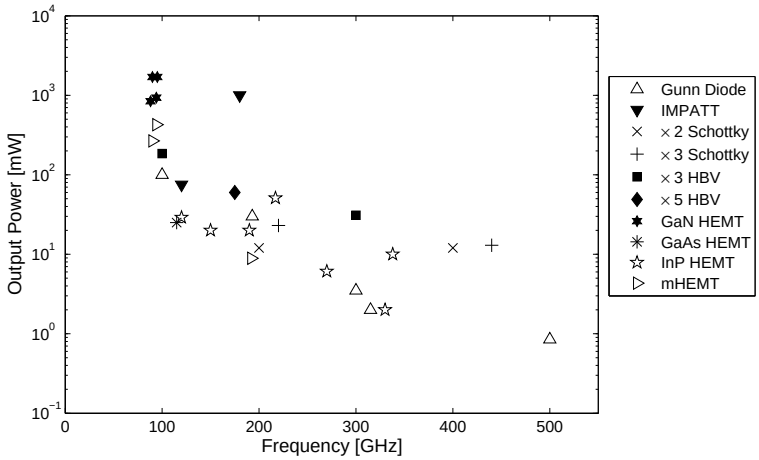


Fig. 1.1: Conventional high frequency power sources: Gunn diodes [12, 13], IMPATT diodes [14, 15], Schottky diodes [16–18], HBVs [19–21], GaN HEMTs [22–24], GaAs HEMT [25], mHEMT [26] and InP HEMT [27–32] power amplifiers.

1.1 Background

As the frequency of operation increases the output power of the conventional solid-state sources drops rapidly [2,11,12]. A comparison between Gunn diodes, IMPATT, Schottky diodes and HBV-based frequency multipliers as well as the performance of mHEMT, GaAs, InP and GaN HEMT power amplifiers is given in Fig. 1.1.

Conventional fundamental oscillators are based on two port devices in particular resonant-tunneling diodes (RTDs), tunnel-junction transit-time devices (TUNNETT), impact- ionization avalanche transit-time (IMPATT) and transferred- electron devices (TEDs, also known as Gunn diodes). All of these devices exhibit negative differential resistance, but the mechanism of operation differs.

The available output power from Gunn diode harmonic frequency oscillators around 100 GHz is ca 100 mW [13]. The IMPATT diodes efficiency under ideal conditions can approach 40 %. The current density for these devices is very high, hence the available output power will be high. However, at high frequencies of operation the output power will decrease, as for other mm-wave and THz devices. Presented in [14] IMPATT diode on GaAs gave 75 mW at 120 GHz. To deliver sufficient LO power to high frequency mixers additional amplifiers and multipliers are required in the LO module.

Up to date, the state-of-the-art GaAs amplifiers are based on metamorphic HEMT technology. In particular a 320 GHz amplifiers stage with a 20 dB gain

Table 1.1: Performance of HBV-based frequency multipliers

$\mathbf{f}_{center}$ [GHz]	$\mathbf{P}_{RF,out}$ [mW]	η [%]	BW[1] [%]	Technology	Ref.
97	85	20	—	× 3 integrated InP	[37]
102	32	21	—	× 3 hybrid Quartz	[38]
107	185	23	15	× 3 integrated InP, Si	[21, 39]
112	15	5	17	× 3 hybrid AlN	[40]
113	195	15	1.5	× 3 hybrid AlN	[41]
175	60	6.3	4.5	× 5 hybrid AlN	[20]
221	7.1	7.9	—	× 3 integrated Copper	[42]
282	31	7	—	× 3 integrated InP	[19]
288	6	6	15	× 3 integrated Quartz	[43]
290	9.5	8	8.6	× 3 hybrid, AlN	[44]
450	1	1.45	—	× 3 hybrid GaAs	[45]

has been reported in [33]. Progress has been made over the last years in the GaN technology. An example of a three-stage GaN amplifier operating at W-band, with an output power of 1.7 W and 21 % small signal gain is given in [24]. A broad review of the power amplifiers performance can be found in [34].

Frequency multipliers are based on nonlinear devices and are realised with transistor, Schottky diode (SD) and other varactor technologies. Interesting examples of transistor based multiplier chains can by found in [35].

Frequency multipliers based on SDs operate in varistor or varactor mode and generate even and odd harmonics of the input signal. Thus, SD based doubler and tripler designs have been demonstrated [16–18, 36].

An alternative technology to SD frequency multipliers are heterostructure barrier varactors (HBVs). The HBV exhibits a symmetric, voltage-dependent capacitance [46]. Due to the capacitance modulation property the HBV generates only odd harmonics of the input signal. The capacitance modulation is possible by stacking a semiconductor characterised by high energy bandgap in between two semiconductors with low barrier energy. The relatively simple structure of the HBV allows growth of several barriers using molecular beam epitaxy (MBE) or metalo-organic chemical vapor deposition (MOCVD). The device power handling capability can be enhanced by increase of the number of barriers [47]. Some of the HBV based frequency multipliers and their performance are presented in Table 1.1. In particular × 3 multiplier for 100 GHz and for 300 GHz, and × 5 multiplier for 175 GHz have shown that the HBV-based multipliers are capable to compete with the Schottky diode technology [19–21]. Worth noticing in Table 1.1 is that the epitaxial transfer approach of HBV diodes on substrates like quartz [43, 48] and copper [42] have been reported. In the presented cases, the HBV material was first epitaxial grown on a lattice matched substrate, and then transferred onto a carrier wafer with a use of an intermediate layer (polymer, metal alloy).

[1] 3-dB Bandwidth in [%].

1.2 Thesis outline

The following licentiate thesis summarizes the work accomplished towards development of a 100 GHz InP-based HBV frequency multiplier on silicon substrate. First, in *Chapter 2* an introduction to HBV and HBV-based frequency multipliers is given. Next, in *Chapter 3* methods of III-Vs integration on silicon substrate employing epitaxial growth and transfer are compared. The process of low temperature plasma assisted bonding [49] was utilised to transfer $In_{0.53}Ga_{0.47}As$ /$In_{0.52}Al_{0.48}As$ /AlAs material structure on silicon host substrate. Comparison of major results and RF performance of the integrated frequency tripler on silicon and on InP substrates are put together in *Chapter 4*.

Chapter 2

Basic principles of heterostructure barrier varactor multipliers

The following chapter provides an overview of the properties of the varactor devices and varactor-based frequency multipliers. The main focus of this chapter is on the heterostructure barrier varactors (HBVs). The concept of the HBV diode and its electrical and physical properties are presented. This is followed by the HBV model and the device performance. Further, existing and possible material systems for HBV devices are discussed. In addition, a higher-order harmonic generation with use of HBVs is described. Finally, a discussion of the limiting factors preventing high frequency operation of HBVs closes this chapter.

2.1 Background

A *varactor* is a device whose operation principle is nonlinear reactance. In particular, a semiconductor junction diode under a reverse DC-bias exhibits a voltage dependent reactance [50]. Depending on the physical properties of the device, the shape of the differential capacitance (differential elastance) can be asymmetrical or symmetrical with respect to the zero volt bias point, Fig. 2.1. To the group of varactors with asymmetrical nonlinear capacitance belong reverse-biased Schottky and p^+n diodes, while HBVs and back-to-back diodes generate symmetrical nonlinear capacitance.
An equivalent circuit of a pure varactor model is presented in Fig. 2.2 [51]. It consists of a variable capacitor connected in series with a resistance (R_s).

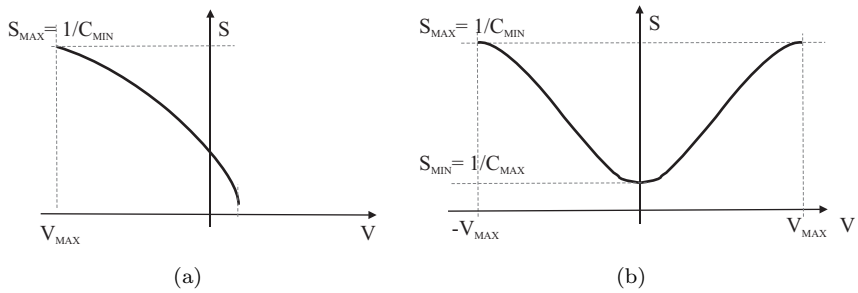


Fig. 2.1: (a) assymetric and (b) symmetric differential elastance characteristics of varactor devices.

Fig. 2.2: Equivalent varactor circuit model.

2.2 Varactor frequency multipliers

The applications where the varactors have found use are mainly higher-order harmonics generation (frequency multipliers). Varactors are as well used for subharmonic generation, and to some extend as frequency converters (down-converters and upconverters) [52] and as parametric amplifiers [53].

As presented in Manley-Rowe formula [54], the conversion efficiency (η) of an ideal varactor based frequency multiplier is equal to 1. While for devices operateing in the varistor mode the maximum conversion efficiency is in the best case $1/n^2$, where n is the multiplication factor [55]. However, the performance of varactor devices is limited by the series resistance R_s, see Fig. 2.2. Thus, the conversion efficiency is a ratio between the generated power ($P_{OUT,AVA}$) and the available input power ($P_{IN,AVA}$):

$$\eta = \frac{P_{OUT,AVA}}{P_{IN,AVA}} \tag{2.1}$$

The conversion efficiency can be expressed in $[dB]$, a conversion loss:

$$L_n = 10log\left(\frac{P_{IN,AVA}}{P_{OUT,AVA}}\right) \tag{2.2}$$

The lower value of L_n the lower loss during conversion of the input power to the output power. In addition, a sharper shape of S(V) characteristic provides a higher efficiency, and a lower L_n [56].

Another parameter defining the performance of a varactor-based frequency multiplier is its dynamic cut-off frequency (f_c), and it can be calculated from:

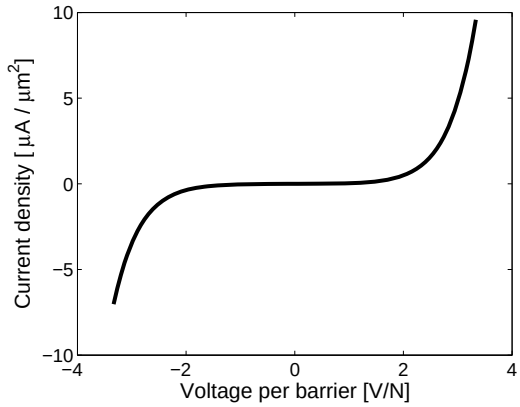
$$f_c = \frac{S_{max} - S_{min}}{2\pi\ R_s} \tag{2.3}$$

where S_{min} and S_{max} are the minimum and maximum elastance for a given device, and R_S is the series resistance, see Fig. 2.1 and Fig. 2.2.

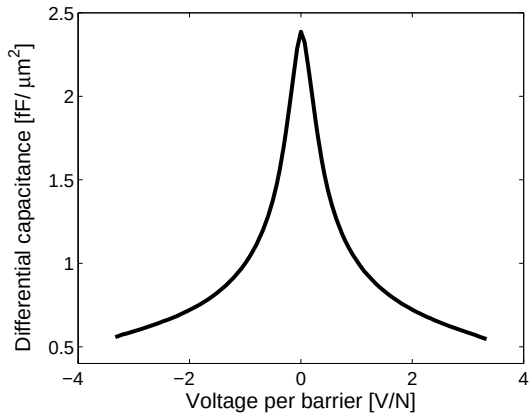
2.3 Heterostructure barrier varactors

2.3.1 Basic principle of operation

The heterostructure barrier varactor (HBV) is a symmetric semiconductor device, which under the applied voltage exhibits an anti-symmetric I-V characteristic and nonlinear, voltage dependent capacitance with its maximum at 0 V, Fig. 2.3(a) and Fig. 2.3(b), respectively. The modulation of the capacitance



(a)



(b)

Fig. 2.3: Principle of conduction current density (dark measurements) and voltage dependent capacitance measurements at room temperature for a 3 barrier HBV diode. The diode area is 60×60 μm^2.

Table 2.1: Typical HBV material layer structure. By × N repeated growth of layers 4–6, the epilayer will contain × N barriers.

Layer No.	Comment	Type	$N_D\ (cm^{-3})$	Thickness $(\AA)$
7	Contact	n^{++}	1.0e19	4000
6	Modulation	n	1.0e17	2500
5	Spacer	i	—	50
4	Barrier	i	—	130
3	Spacer	i	—	50
2	Modulation	n	1.0e17	2500
1	Buffer	n^{++}	1.0e19	10000
0	Substrate	n^{++} or SI	—	—

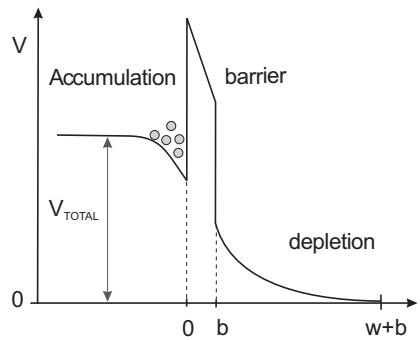


Fig. 2.4: Conduction band of HBV under applied bias. V_{TOTAl} is the applied voltage, b is the barrier thickness and w is the depletion layer width.

is possible by stacking a layer of semiconductor characterised by high bandgap energy (barrier), in between two, moderately doped layers of another semiconductor material with lower bandgap energy (modulation) [46]. Table 2.1 presents a typical material structure of the HBVs. The undoped barrier region (layer 4) prevents electron transport through the structure. Thick and high bandgap energy barrier is preferable since it minimise the thermionic emission and carrier tunneling [57]. The thin (5 nm), undoped regions surrounding the barrier act as spacers (layer 3 and 5). The spacer prevents diffusion of dopants into the barrier.

When a voltage is applied to the device, the electrons are accumulated at one side of the barrier extending the depletion region width (w) at the another side of the barrier, see Fig. 2.4.

2.3.2 HBV model

An extended HBV quasi-static equivalent circuit is presented in Fig. 2.5. In this model the device leakage current is modeled by the current source. The series resistance R_S is a sum of the ohmic contact resistance, the resistance of the

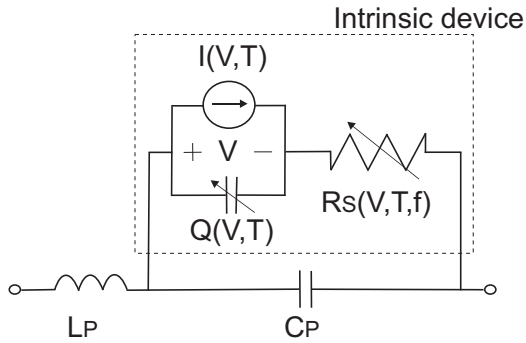


Fig. 2.5: Quasi-static equivalent circuit model of HBV.

undepleted active layer, and the spreading resistance. Thus it is dependent on the material parameters, device area and temperature. The R_s is dependent on the applied voltage through the extension of the depleted region and frequency dependent through the skin effect. The L_P and C_P parasitic elements model the connection to the diode (wire bonding, airbridges) and packaging, respectively.

2.3.3 HBV performance

The HBV exhibits a voltage dependent capacitance, see section 2.3.1. Under a DC bias the capacitance on HBV can be described by the following equation:

$$S = \frac{1}{C} = \frac{N}{A}\left(\frac{b}{\epsilon_b} + \frac{s}{\epsilon_d} + \frac{w}{\epsilon_d}\right) \tag{2.4}$$

where S is the elastance, A is the device area and N is the number of barriers. b and s are the thickness of the barrier and the spacer region, respectively. ϵ_b and ϵ_d are the dielectric constants of the barrier and the modulation layer, respectively. w is the depletion-layer width and can be calculated from:

$$w = \sqrt{\frac{2\epsilon_d |V_d|}{qN_d}} \tag{2.5}$$

where V_d is the voltage across the depleted region in each of modulation layers, N_d is the doping concentration in the modulation layers, and q is the elementary charge. Equation 2.5 is valid when $w > L_D$. L_D is known as the Debye length, and is given by:

$$L_D = \sqrt{\frac{\epsilon_d kT}{q^2 N_d}} \tag{2.6}$$

where k is the Boltzmann constant and T is the temperature in [K] units.

The maximum width of the depleted region (w_{max}) should not exceed the width of the modulation layer m. Under condition $w_{max} > m$ a punch-through

will occur, causing the breakdown of the device. The w_{max} can be calculated as:

$$w_{max} = \frac{\epsilon_d E_{d,max}}{qN_d} = \sqrt{\frac{2\epsilon_d V_{br}}{qN_d}} \tag{2.7}$$

where $E_{d,max}$ and V_{br} are the maximum electric field and the breakdown voltage in the modulation layer, respectively. V_{br} for a semiconductor device is given by [58]:

$$V_{br} = 60 \left(\frac{E_g}{1.1eV}\right)^{3/2} \left(\frac{N_d}{10^{16} cm^{-3}}\right)^{-3/4} \tag{2.8}$$

where E_g is the barrier height of the semiconductor in the modulation layer at room temperature.
At zero bias, when the w is equal to $2L_D$, the eq. 2.4 is reduced to:

$$S_{min} = \frac{1}{C_{max}} = \frac{N}{A}\left(\frac{b}{\epsilon_b} + \frac{2s}{\epsilon_d} + \frac{2L_D}{\epsilon_d}\right) \tag{2.9}$$

2.3.4 Material systems

The HBV material structures are grown with molecular beam epitaxy (MBE) and metal- organic vapor phase epitaxy
(MOVPE) processes. The symmetry of the material is one of the main advantages of the HBV devices, see Table 2.1. Due to the symmetry several barrier layers can be grown in one process, increasing the device power handling capability. Depending on the mounting technique the HBV material is grown on semi-insulating (SI) of a highly doped substrate.

The very first HBV structures were grown on a lattice matched GaAs substrates [46, 59]. The undoped barrier region was
GaAs/ $Al_{0.7}Ga_{0.3}As$/ GaAs. However, the low barrier height of GaAs resulted in a large leakage current, which consequently limited the device performance [60]. To increase the barrier height, hence reduce the leakage current, a thin layer of AlAs in the middle of the barrier was implemented [61].

Nowadays, the HBV material structures are grown on InP substrates. The barrier is created by undoped region of
$In_{0.52}Al_{0.48}As$/ AlAs/ $In_{0.52}Al_{0.48}As$. Its advantage over the GaAs system is higher electron mobility of the InGaAs, which is used to form the contact and the modulation layers, and higher E_g. State-of-the-art HBV based frequency triplers employ InGaAs/ InAlAs/ AlAs material structures on InP have been presented [19, 20, 62, 63].
Due to a rather high cost of the InP substrates a metamorphic grown InGaAs/InAlAs on GaAs substrates could substitute the HBV on InP. The metamorphic growth allows growth of a lattice mismatched, step graded $In_yAl_{1-y}As$ buffer layers on GaAs substrates [64], and further growth of the InAlAs/InGaAs of the active device region.

Besides common III-V semiconductors, also AlSb grown on InAs buffer layer

has been used for the HBV material structure [65]. The main advantage of InAs is its very high electron mobility (33000 cm^2/Vs). However, the alloys containing Sb are sensitive to water and air, and the device fabrication is challenging [66].

Studies with GaN materials for HBV devices have been proposed and carried out [67, 68]. The GaN is characterised by large energy bandgap, and high saturation velocity of electrons is achievable. However, due to a spontaneous polarization and stress induced piezoelectric field in the AlGaN and GaN, an asymmetric C-V characteristics is obtained [67].

2.4 HBV frequency multipliers

The fact that the HBV generates only odd harmonics of the input signal greatly simplifies the circuit design of high order frequency multipliers. The design simplicity is related to the required number of idlers. Idlers are harmonics which are essential for the multiplier performance, although these are not part of any input or output [50]. For example, a tripler ($\times$ 3) circuitry does not require an idler, while a quintupler ($\times$ 5) requires only one idler at $3 \times \omega_0$. In comparison with an abrupt-junction diode, a tripler and quadrupler will require one idler at $2 \times \omega_0$, while a quintupler will require two idlers at $2 \times \omega_0$ and $4 \times \omega_0$ [50]. The importance of the idler circuit at $3 \times \omega_0$ for a quintupler design has been studied in [56]. It was shown that if no currents at the idler frequency are provided the expected efficiency of the frequency quintupler is significantly lower, compared to the case when the currents at idler frequency are maximised.

The efficiency of a HBV frequency multiplier pumped with an input frequency (f_p) and a dynamic cutoff frequency (f_c) eq. 2.3, can be estimated as:

$$\eta = \frac{100}{1 + \alpha \left(\frac{f_p}{f_c}\right)^{\beta}} \tag{2.10}$$

when α and β parameters are extracted from a large-signal simulations, and are equal to 200 and 1.5, respectively [47].

2.5 Diode optimisation

From the discussion in section 2.3.4 we know that the performance of the HBV diode is determined by the physical properties of the semiconductor material. These material properties will reflect on the leakage current, junction capacitance (C_j), series resistance (R_s) and breakdown voltage (V_{br}).

According to the studies presented in [69, 70] a leakage current is dependent on the barrier thickness (b) and its height ($\Delta\ E_g$). For thin barriers at low voltage bias levels the tunneling current will be dominant, and at high bias levels the thermionic emission will contribute to the current across the barrier.

The C_j is dependent on the material properties like its dielectric constants, physical barrier and spacer thickness and the device contact area [71].

The R_s is a sum of the ohmic contact resistance, the undoped active layer

resistance and the spreading resistance. Due to its thermal dependence, R_s is one of the limiting factor of the HBV.

In [60] it was shown, that the main contribution to the thermal resistance is through the contact and the buffer to substrate layers. Due to a low ($0.05\ Wcm^{-1\circ}C^{-1}$) thermal conductivity of $In_{0.53}Ga_{0.47}As$ at high input frequencies, the heat generated in the device limits its RF performance.

The V_{br} (eq. 2.8) is strongly dependent on the doping concentration (N_d) in the modulation layer. For lightly doped modulation layer the V_{br} will be higher, therefore enhanced RF power handling capability will be achieved.

The dynamic cut-off frequency f_c defines the maximum frequency of operation of the HBV device. It is dependent on the elastance swing (ΔS) and the R_s. To obtain high f_c, the R_s should be chosen to be as small as possible.

Chapter 3

III-Vs integration on silicon

The interest in combining optoelectronic and high frequency electronic components with CMOS technology is growing rapidly. The compound semiconductors offering high electron mobility and direct bandgap, integrated on silicon which is a robust material, characterised by good mechanical and thermal properties could overcome the limitations of the Si technology. Combining these dissimilar materials would result in an even higher scale of integration, cost reduction, and higher speed of commercial applications (computers, wireless and fiber communication). However, the high quality direct growth of III-Vs on Si is limited by almost 3.3 % and 8 % lattice mismatch, and 45 % and 55 % difference in the Coefficient of Thermal Expansion (CTE) for GaAs - Si and InP - Si, respectively. For the material parameters of InP, GaAs and Si see Table 3.1. A great research effort has been made to integrate compound semiconductors on silicon substrates using methods of epitaxial growth and transfer.

This chapter begins with an overview of the properties of some commonly used semiconductor substrates. Next, in section 3.2 the methods of integration on silicon are presented. The epitaxial growth and transfer methods are compared. Further, in section 3.3 the HBV material structure is presented. Then, an introduction to low temperature plasma assisted bonding is given. The epitaxial transferred material was studied using methods like transmission electron microscopy and Auger spectroscopy. The results of this characterisation are presented. The chapter ends with a description of the fabrication procedure for the HBV diodes and integrated frequency multipliers in section 3.4.

3.1 Substrates for millimetre-wave and THz applications

Low loss transmission lines at THz frequencies require substrates with a low loss tangent ($\tan \delta$), a low dielectric (ϵ_r) constant and a high resistivity (ρ). Table 3.1 summaries electrical and physical attributes of some commonly used substrate materials. These will define the design, the choice of process technology, and finally the properties of the active and passive components.

Table 3.1: Material parameters of commonly used substrate materials [72–75] at RT.

Parameter	InP	GaAs	Si	AlN	SiC	SiO_2[1]	C[2]
E_g (eV)	1.35	1.42	1.12	6	3	—	5.47
ϵ_r	12.6	12.9	11.7	8.5	9.66	3.78	5.7
κ ($Wcm^{-1}K^{-1}$)	0.68	0.55	1.56	1.75	3.6	0.10	6-20
tan$\times$ δ 10^{-4}	2	1.6	1[3]	6	80[4]	0.6	0.6
d (Å) at 300 K	5.86	5.65	5.43	3.1	3.08	—	3.56
CTE $10^{-6}/°C$	4.6	5.7	2.6	4.15	—	0.55	0.8
Strucutre	ZB	ZB	D	W	—[5]	AG[6]	D

Semi-insulating InP and GaAs substrates are broadly used in the millimeter-wave and THz applications. These materials are characterised by low loss tangent and high resistivity. However, high power handling is limited by poor thermal conductivity of InP and GaAs [60]. Moreover, these materials are fragile, expensive and are limited to small wafer sizes. High resistivity silicon has electrical properties similar to InP and GaAs. But, silicon has two times higher thermal conductivity, and its mechanical properties allow for the process of membranes, waveguides, and other components for high frequency applications [4, 78–82].

AlN is a wide-bandgap III-N material. Its main attributes are low loss tangent and almost three times higher thermal conductivity than the one offered by InP or GaAs. However, AlN is a hard material, which makes the micromechanical processes difficult. Very good performance of HBV-based frequency multipliers on AlN substrate have been demonstrated [20, 40].

Along with AlN, SiC is classified to the group of wide-bandgap materials. It serves as a host substrate for high power GaN HEMTs and for microwave monolithic integrated circuits MMICs [83–85]. Although its excellent thermal properties, SiC is more attractive for applications operating at low frequencies due to its high loss tangent value.

Fused quartz has very good electrical properties (tan δ of 0.6×10^{-4}) and relatively low dielectric constant of 3.78. Therefore, it is commonly used as a substrate for circuitry for variety of high frequency applications.

Commercially available diamond substrates are prepared by chemical vapor deposition (CVD). CVD diamond is characterised by very low loss tangent and high thermal conductivity, thus it is a great candidate for high frequency and power applications [74, 86, 87].

[1] SiO_2 refers to silica glass (fused quartz).
[2] Data are given for CVD Diamond.
[3] In here data refer to Si with σ=11 000 Ωcm [76].
[4] At 80 GHz [77].
[5] SiC CTE and crystal structure depend on the type of SiC.
[6] AG stands for Amorphous Glass.

3.2 Methods of integration

3.2.1 Epitaxial growth

The main limitation to a direct growth of the compound semiconductors on the Si substrate is the lattice mismatch, which for GaAs - Si and InP - Si is 3.3 % and 8 %, respectively. During the epitaxial growth the strain induced due to the large lattice mismatch will be released through formation of dislocations. For the lattice mismatch < 2 % the density of dislocations is ca 10^5 cm^{-2}. For large lattice mismatch, like in the case of GaAs - Si and InP - Si, the density of dislocations is much higher and consequently the electrical and optical properties of the grown epilayers will be degraded. A number of growth techniques have been presented in order to reduce the density of the threading and misfit dislocations.

One of the methods is an epitaxial growth on a compliant substrate (CS)[3] [88]. When a lattice matched epitaxial layer is grown on a very thin CS, the relaxation stress penetrates into the CS instead of the epilayer. Hence, the critical thickness of the epilayer increases to infinity [88]. Using this method a high quality GaAs epitaxial layers on Si were demonstrated [89].

The nucleation and propagation of antiphase boundaries and treading dislocations can be minimised by introducing a metamorphic buffer layer. As a buffer layer a graded $Si_{1-x}Ge_x$ can be used. Ge is lattice matched to GaAs, thus further growth of dislocation free Ga compounds is obtained [90]. Alternatively, the Ge can be first transferred onto Si, and lattice matched GaAs grown. The GaAs serves as a buffer for a metamorphic InAlAs, which is introduced as a transition between GaAs and InP. This method was successfully implemented for metamorphic HEMTs and HBTs [91].

A patterned substrate technology for the growth of compound semiconductors on Si has recently attracted more attention. It was shown that when the growth area is reduced the number of dislocations can be minimised to zero. The employed methods are narrow trenches, or patterned in SiO_2 or SiN openings of nm to μm^2 diameter.

Besides the lattice mismatch the CTE is another parameter which will influence the quality of the epitaxial films. The typical growth temperatures of compound semiconductors are in the range of 400 - 600 °C. At these temperature levels the substrate and epilayer maintain their own lattice constants. When wafer is cooled down to RT the interface atoms will follow the lattice constant of Si causing a strain deformation. As a result wafer bending, or epilayer cracking is observed. One of the methods to overcome the CTE mismatch is to combine CS with amorphous oxide layer as the buffer. Presented in [7] a thin layer of strontium titanate ($SrTiO_3$ or STO) as a compliant buffer was used. The STO reduces the mechanical strain and the thermal mismatch between the epitaxial GaAs layer and the silicon.

The very last material property limiting the quality of III-Vs grown on Si is the materials polarity. The GaAs and InP are polar semiconductors, while Si

[3] A CS is a very thin, usually tens or few hundreds of nm thick, substrate. Due to a reduced thickness, it uses a mechanical host substrate with a buffer or interface layer in between.

belongs to the group on non-polar materials. The difference in the polarity will lead to creation of antiphase boundaries, and consequently the final epilayer may behave like a highly compensated semiconductor. A detailed discussion of antiphase domain and the techniques to suppress their formation are described in [92].

3.2.2 Epitaxial transfer

An alternative method to the epitaxial growth is an epitaxial transfer, also known as *bonding*. It is a process of joining two surfaces [93]. It enables combination of almost all materials, while the epitaxial growth is limited to the lattice parameters, CTE and to the crystal structure. To obtain a good quality bonding the surfaces of the joined wafers must have micro roughness (rms) below 1 nm [94]. Another requirement is the cleanliness. Any surface contamination (dust, hair, hydrocarbons or metal ions) may cause creation of voids (an area where the bonding did not occur). For example, a particle of a 1 μm diameter on a 4$''$ substrate will lead to a 1 cm diameter void [95], therefore proper cleaning of the wafers is essential.

The process of wafer bonding is of a great interest for micromechanics, microelectronics and optoelectronics. Depending on the applications and the properties of the combined materials different bonding techniques can be utilised. The bonding can be direct or indirect. In the indirect method a thin intermediate layer of resist or metallisation is used. Some of the wafer bonding methods require an additional thermal annealing, which is performed during or after the process. However, if the thermal expansion coefficient mismatch is taken under consideration, a low temperature (LT) procedure is preferable. For optoelectronic and electronic applications an oxygen plasma assisted wafer bonding can be used. The plasma activated wafers bond spontaneously, and the strength of the bonding is comparable with thermally treated wafers [96]. For oxide-free interfaces the fluorine [97] or argon plasma [98] can be used. Prior to wafer joining, outgassing channels can be wet etched in the silicon what minimises the density of voids [99]. In table 3.2 the commonly used bonding methods for semiconductor technology are presented and shortly described.

In comparison with the epitaxial growth the epitaxial transfer method of III-Vs onto silicon is considered to be expensive. The high cost is related to the price of the InP and GaAs wafers which serve as the donor wafers for epitaxial growth. After the growth and transfer onto a host substrate, the donor wafer is usually removed by wet chemical etching or lapping. To save in the material cost and reuse the donor wafer, methods involving mechanical splitting [102], undercutting by selective chemical etching [103] and ion-cut [104], also known as SmartCut^{TM}, processes were developed.

Table 3.2: Commonly used wafer bonding processes is semiconductor technology [6, 94, 96, 100, 101].

Technique		Remarks
Direct	Anodic	Ionic bonding; high electric fields
	Direct	Surface roughness <1 nm; thermal anneling
	Plasma assisted	Low temperature; Oxygen or fluorine plasma. Suitable for thermally mismatched materials.
Indirect	Adhesive	Thin (μm) adhesive layer (polymer, spin-on glass).
	Eutectic	Metal alloys for soldering.

3.3 Experimental procedure

3.3.1 HBV material structure

The HBV material for the epitaxial transfer was grown on a lattice matched 3″ InP substrate by molecular beam epitaxy (MBE). In Fig. 3.1 an SEM image of a integrated RF diode is presented, with the depicted material layers. A single mesa consists of three undoped barrier regions created by $In_{0.52}Al_{0.48}As$/ AlAs/ $In_{0.52}Al_{0.48}As$. The 3 nm thick layer of AlAs, sandwiched in between 5 nm thick layers of $In_{0.52}Al_{0.48}As$, further increases the barrier height, reducing the conduction current [61, 70, 105]. In order to prevent diffusion of dopants to the barrier, a 5 nm thick, undoped spacer regions on both sides of the barrier are used. The moderately doped (N_d= 10^{17} cm^{-3}), 250 nm thick $In_{0.53}Ga_{0.47}As$ layers allow for capacitance modulation. This region is also optimised for minimum resistivity and maximum breakdown voltage. Highly doped (N_D= 10^{19} cm^{-3}), 400 nm and 1000 nm thick $In_{0.53}Ga_{0.47}As$ layers are optimised for low series resistance and act as contact and buffer, respectively.

Prior to the bonding, the HBV material structure is grown up-side-down on

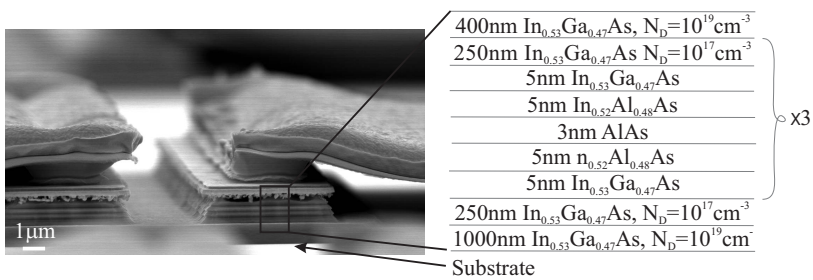


Fig. 3.1: SEM image of an RF diode with depicted material layers on the silicon substrate.

the lattice matched InP substrate. The up-side-down growth suggests that epitaxial structure will be grown in the reverse order, compared to the case when devices are processed directly on the donor wafer. For the up-side-down growth initially the 400 nm thick $In_{0.53}Ga_{0.47}As$ is grown on InP substrate, followed by other layers and at last the 1000 nm $In_{0.53}Ga_{0.47}As$ layer is deposited. By doing so the 400 nm thick $In_{0.53}Ga_{0.47}As$ contact layer is on top after the epitaxial transfer of the HBV material and wet etch removal of the InP substrate. An easy access to the contact layer is therefore obtained.

3.3.2 LT plasma assisted wafer bonding

In this thesis a LT plasma assisted bonding for the material transfer is utilised. In this method the agent activating the wafer bonding is an oxide, which is plasma deposited on a cleaned and contamination free surface. Some of the bonding techniques require an additional thermal annealing (> 400 °C), in order to induce the bonding strength, and reduce the number of voids. In the presented technology the annealing is avoided due to the CTE mismatch between InP and Si. It is possible that annealing instead of improving the bonding quality will cause its degradation.

The transfer process is illustrated in Fig. 3.2. Prior to the bonding the sili-

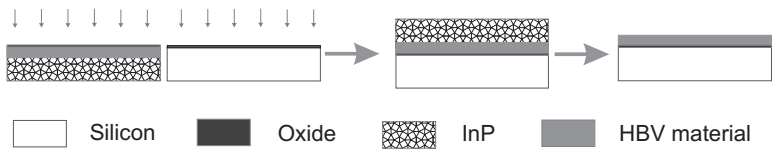


Fig. 3.2: Process flow of LT plasma activated bonding. From *left* surface preparation, O_2 plasma treatment, *(*middle) bringing the wafers into the contact and bonding at RT. *(*right) After the InP substrate chemical wet etching.

con wafer is first wet chemically cleaned in the standard cleaning solution (RCA) for 10 min. The RCA is a mixture of NH_4:H_2O_2:H_2O (1:5:20). The temperature of the batch is 60 °C. The RCA solution removes organic contaminants from the Si surface. Subsequently, the native oxide from the Si surface is removed by dipping the wafer in 2 % HF solution for 30 s. The native oxide removal step is usually performed just before plasma oxidation of the silicon surface. Unless a visible surface contamination, the InP-wafer with the HBV epitaxial structure is not cleaned.

In the next process step, both wafers are oxidized separately, under the same chamber conditions for 30 s.

Then, the oxidized surfaces are brought into the contact (pre-bonded) ex-situ and transferred to the substrate bonder. In the substrate bonder the wafers are left under the pressure of 1000 mbar and at room temperature (RT) to complete the process of the epitaxial transfer. An additional storage at RT and an applied force on the wafers increases the bonding strength.

In the last process step, the InP substrate is removed by wet chemical etching in HCl:H_2O (5:1) solution, and the wafer is ready for the process.

3.3.3 Characterisation of InGaAs/InAlAs/AlAs on silicon

To characterise the transferred material a number of measurements were carried out. These were: infrared (IR) inspection, atomic force microscopy (AFM), transfer electron microscopy (TEM), and X-ray diffraction (XRD). In addition an Auger electron spectroscopy was done, and the HBV/Si interface was studied.

The very first procedure after the wafer joining is the IR inspection. This will characterise the quality of the bonded pair and reveal the presence of voids. In Fig. 3.3 an IR image of the bonded structure is shown. The diameter of the InP substrate is 3″. A dark area visible on the picture indicates a single void, with a diameter of ca 15 mm.

The roughness of the transferred material was studied with an atomic force

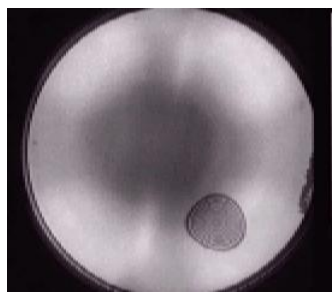
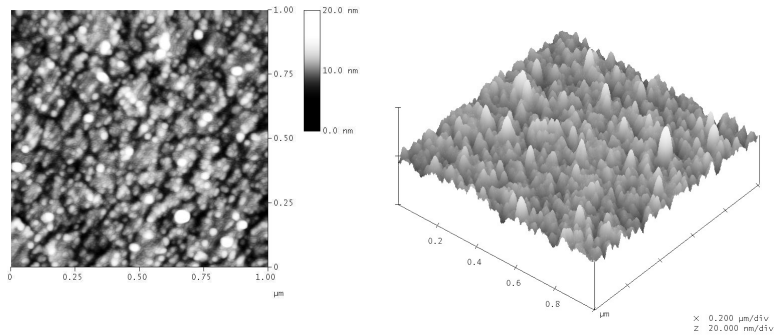


Fig. 3.3: Infrared inspection image of the transferred InGaAs/ InAlAs/ AlAs on silicon. The InP wafer size is 3″. The dark area indicates an unbonded region (a void).

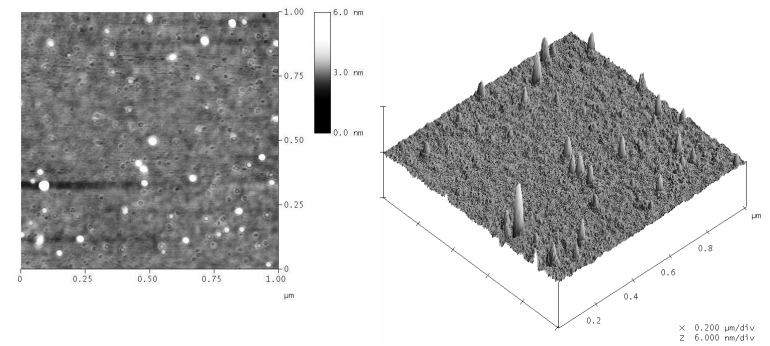
microscopy (AFM). The surface profile was measured after the chemical wet removal of the InP donor wafer, and is shown in Fig. 3.4(a). The scanned area was 1 μm^2. The maximum peak height found on the scanned surface is 200 Å, and the AFM root-mean-square (rms) roughness is 18 Å. An AFM scan of the silicon host wafer is shown in Fig. 3.4 b, and the rms for the used wafer is 3 Å.

A TEM image presenting the cross section of the transferred material on the silicon carrier substrate is shown in Fig. 3.5. The smooth and clean $In_{0.53}Ga_{0.47}As$/Si interface is visible. A magnification of the interface shows a presence of ∼5 nm thick amorphous oxide layer. In addition, a TEM image of the barrier region is shown. The bright region is the 3 nm thick AlAs, surrounded by darker layers of 5 nm thick $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$.

To verify the presence of InGaAs on silicon a 2D X-ray scan was taken, Fig. 3.6. Total of three peaks one assigned to InGaAs and two assigned to silicon-on-insulator were detected. The HBV material structure was grown on lattice matched InP substrate, thus a peak was detected at 63°and 31.7°for 2θ and ω. SOI wafers are obtained by direct wafer bonding or SmartCut^{TM} technology. Hence, presence of two peaks at 69°for 2θ and separated at ω angle with 3°was expected.



(a)



(b)

Fig. 3.4: AFM scan of (a) $In_{0.53}Ga_{0.47}As$ after wet etch removal of the InP substrate; (b) silicon substrate. The roughness of the $In_{0.53}Ga_{0.47}As$ and silicon is 18 Åand 3 Å, respectively.

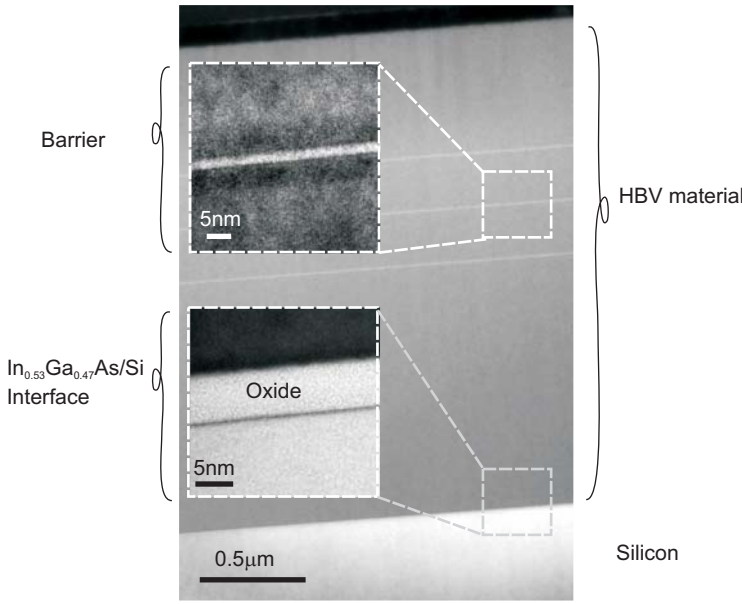


Fig. 3.5: Transmission electron microscopy image of the HBV material structure transferred on silicon substrate with insert showing the magnified barrier and bonding interface. The thickness of the amorphous oxide is approximately 5 nm.

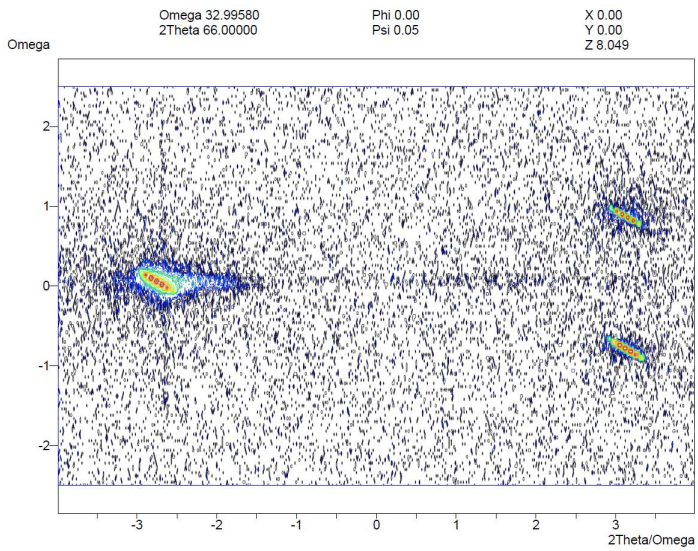


Fig. 3.6: 2D X-ray diffraction scan showing InGaAs (2θ=63°, ω=31.7°) and two peaks related to SOI carrier wafer (2θ=69°and ω of 31.5°and 34.5°for substrate and top layer, respectively).

The last method used to characterise the material, and prove the presence of

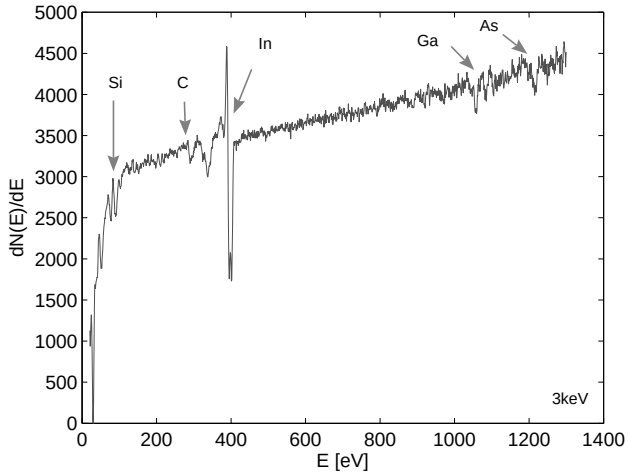


Fig. 3.7: Auger electron spectroscopy data revealing presence of InGaAs on Si substrate.

the InGaAs on silicon was the Auger electron spectroscopy. A spectrum at the InGaAs/Si interface is shown in Fig. 3.7. The electron beam energy was 3 keV, and the beam size was 30 units (3 μm). The chip before the characterisation was cleaned in argon atmosphere. The detected components were: Si at 92 eV, In at 404 eV, Ga at 1170 eV and As at 1220 eV. A peak at 272 eV reveals the presence of carbon (C) which is related to the surface contamination.

3.4 Fabrication of the monolithic integrated HBV frequency multipliers

Fabrication of monolithically integrated HBV frequency multipliers consist of standard III-V processes. The process flow is presented in Fig. 3.8.

First, the wafer is split into 20×20 mm^2 chips, which are cleaned from organic contaminations before the process. Then, an UV negative photolithography is applied to define the ohmic contact area. A 30 s long wet etch in $HCl : H_2O$ (1:100) is used prior to the contact deposition and removes a native oxide from $In_{0.53}Ga_{0.47}As$ surface. Subsequently, an e-beam evaporation is utilised to deposit the ohmic metallisation. Depending on the process and material an alloyed or non-alloyed ohmic contact are deposited. The former one (Ni/ Ge/ Au (10 nm/ 50 nm/ 150 nm)) requires an additional temperature treatment, which provides better adhesion to the semiconductor and reduces the contact resistance, R_c of 6×10^{-6} Ωcm [106]. For the epitaxial transferred material a non-alloyed ohmic contact is preferred. It is a combination of Ti/ Pd/ Au (20 nm/ 40 nm/ 200 nm). The R_c is approximately 2.5×10^{-6} Ωcm [106].

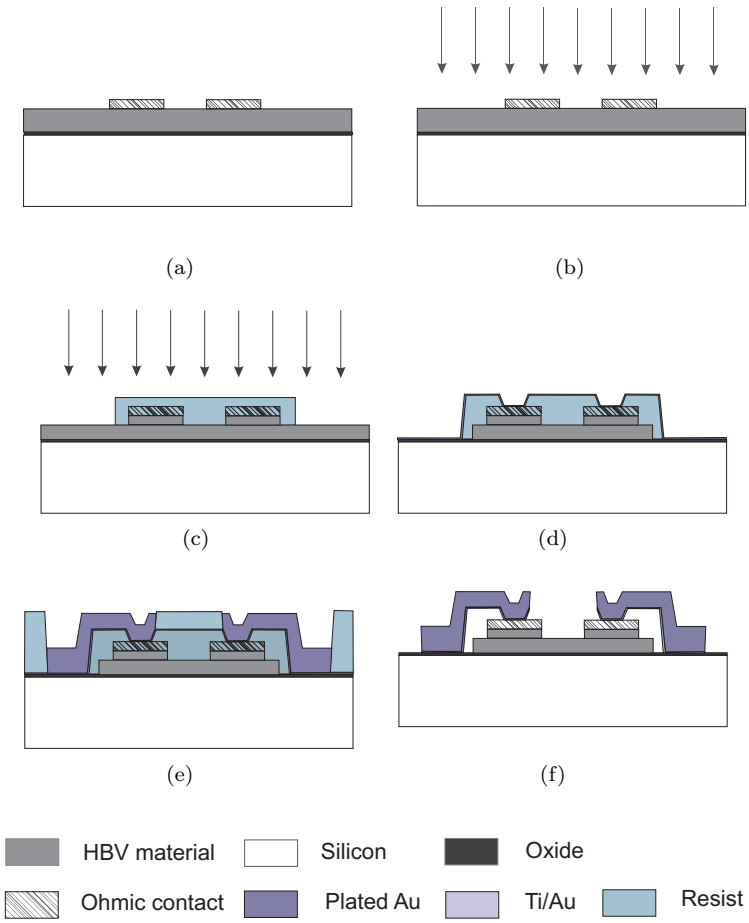


Fig. 3.8: Integrated HBV-based frequency multipliers process steps.
(a) Ohmic contact evaporation. (b) Mesas dry and wet etching. (c) Photolithography and wet etching of the diode isolation. (d) Photolithography and seed layer sputtering. (e) Photolithography and Au plating of the air bridges and circuits. (f) Removal of spun resist, reactive ion beam etching of the seed layer and dissolve of the PMGI e-beam resists.
The drawings are not in scale.

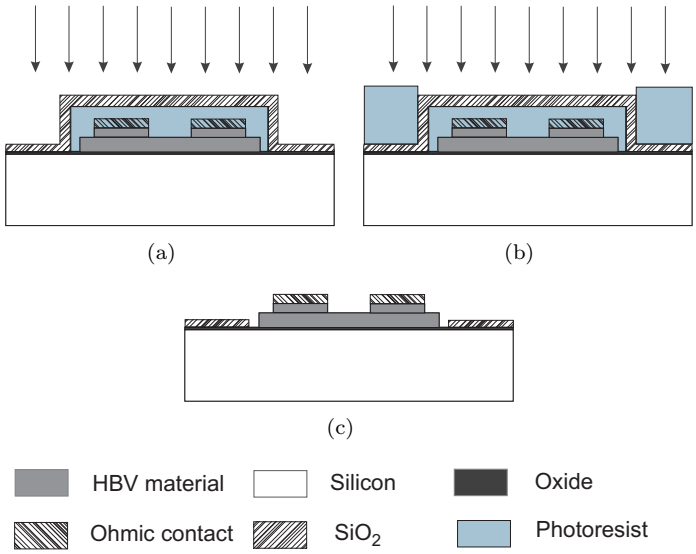


Fig. 3.9: Substrate passivation steps.
(a) Deposition of the SiO_2. (b) Wet etch of the SiO_2 from the diode area. (c) Removal of the resist.
The drawings are not in scale.

Prior to mesas dry etching, a 200 nm thick layer of Ti is evaporated on top of the metallisation. Ti masks and protects the contact against degradation during the dry etching.

After the e-beam contact evaporation and lift-off, the mesas are defined by dry etching in CH_4 atmosphere. During this process, the barriers and spacers layers are etched away until the buffer layer is reached.

In order to decrease the damage of the mesa side walls caused by the dry etching, the mesas are wet etched in the H_2O_2: H_2SO_4: H_2O (1:4:200) solution. It is believed that the roughness of the mesa side walls, may contain traps, which will attract electrons and result in increased conduction current over the device.

In the next step the individual diodes are isolated. First, the mesas are protected with a positive photoresist, and then the buffer layer is wet etched down to the substrate in the
H_2O_2:H_3PO_4:H_2O (1:1:25) solution. Due to a strong under-etch of the isolation area, the wet etch process is divided into two part. After first few minutes of etching, the resist is dissolved in the acetone and the photolithography and wet etching is repeated. A change in the surface color indicates that the buffer layer is removed and the substrate is reached.

For this thesis work the silicon surface was covered with a sputtered, 100 nm thick SiO_2 layer and is used in order to reduce the substrate DC-losses. The substrate passivation was introduced after the diode isolation, and required four process steps, see Fig. 3.9. First, by photolithography, the diodes are covered

with a thick layer of the resist. Then, the SiO_2 is deposited. Next, the sample is patterned with a second layer of resist, and the passivation is wet etched in a dilute solution of buffer hydrofluoric acid (BHF:H_2O (1:3)) from the diode area. A hydrophobic surface indicates that the SiO_2 is completely removed.

In the last process step the microstrip circuit and air bridge connections to the mesas are electroplated. A PMGI e-beam resist is used to pattern the chip. Then, a Ti/ Au (10 nm/ 100 nm) seed layer is sputtered. A 3.6 μm thick photoresist layer is spun on the seed and the plating area is defined by the UV photolithography. The thickness of the electroplated gold is approximately 2 μm.

After the Au plating the resist is stripped and the seed layer is removed by Argon ion milling. Finally, the substrate is diced into individual chips and the substrate thickness is brought to the design specifications using backside lapping.

Chapter 4

Integrated HBV frequency multipliers

The following chapter begins with a short description of a tripler circuit design. Subsequently, the DC characterisation and its results are presented. Further, the set-up for the RF characterisation of the frequency multiplier is described. Finally, the experimental data of the RF characterisation of silicon integrated and monolithically integrated frequency tripler on the InP substrate are presented. The parameters like maximum available output power, 3-dB bandwidth, conversion loss and efficiency are compared for circuits on silicon and InP.

4.1 Design and characterisation

4.1.1 Tripler circuit design

The multiplier design was done using Ansys HFSS and Agilent ADS design software. The input signal is coupled from the waveguide (WR-22, 33 - 50 GHz) to the circuit with a waveguide probe. The matching is done with open stubs at the input side. The reflected 3^{rd} and higher harmonics are filtered with the bandpass filter. If higher harmonics were generated, these will be effectively blocked with a band-pass filter at the diode output. A second waveguide probe is used at the output to couple the generated signal to the output waveguide (WR-10, 75 - 110 GHz). Due to the properties of HBV devices described in section 2.3.3, no external DC-bias is required, hence the design and assembly procedures of the frequency multiplier circuit are greatly simplified.

A scanning electron microscopy image of a ready circuit is presented in Fig. 4.1. The dimensions of the tripler chip are 4.7 mm × 0.8 mm × 0.08 mm (length × width × thickness).

The × 3 frequency multiplier was originally designed for an InP-substrate [21, 37]. The same design layout was kept for the silicon integrated frequency multipliers, due to the small difference in the material permittivity, 12.6 and 11.9 for InP and Si, respectively.

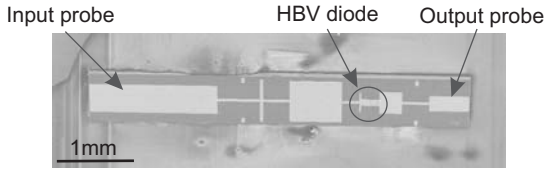


Fig. 4.1: SEM image of an integrated HBV frequency tripler on silicon substrate. The chip size is 4.7mm × 0.8 mm× 0.08 mm (length × width × thickness). The diode consists of 4 mesas connected in a series (12 barriers). The contact area is 7 × 100 μm^2.

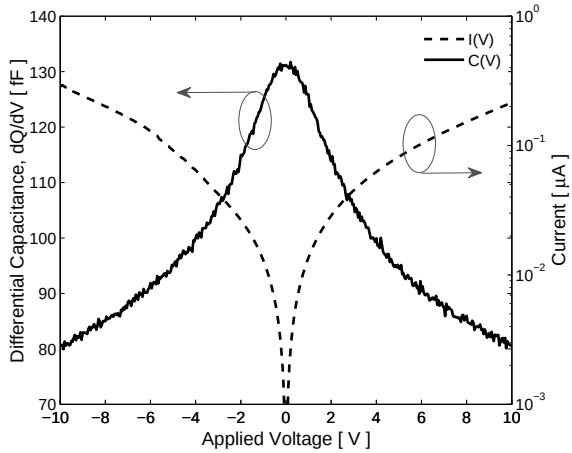


Fig. 4.2: C-V and dark I-V characteristics for a 4 mesas, 12 barriers, 700 μm^2 HBV diode measured at RT.

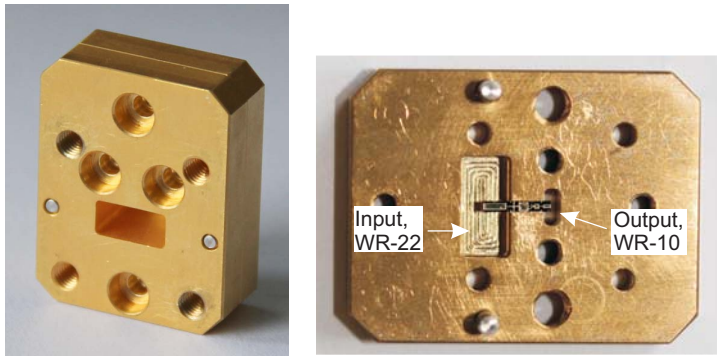
4.1.2 DC characterisation

A DC characterisation provides the first indication of semiconductor material quality and active device performance. The DC measurements are performed with a Keithley LCR meter and an Agilent semiconductor device analyser (Agilent B1500A). A typical DC response of a HBV diode is shown in Fig.4.2. The barrier height is estimated from the I-V measurements taken at different temperature points (thermionic emission), and the doping concentration is extracted from the the $1/C^2$ slope.

4.1.3 RF characterisation

Prior to the RF characterisation the circuits are mounted in a machined metal channel block connecting the input and output waveguide. For the chip assembling a nonconducting glue or wax are used. In Fig. 4.3(a) and Fig. 4.3(b) an image of a 100 GHz frequency multiplier block and the mounted chip are shown, respectively.

The RF characterisation set-up is presented in Fig. 4.4(a). The input signal



(a) (b)

Fig. 4.3: (a) Mounting block for the 100 GHz frequency multiplier; (b) assembled circuit chip in the waveguide channel.

was provided by an Agilent E8257D signal generator. The maximum output power of the signal generator is 18 dBm. The required RF input power to drive a HBV frequency multiplier is in the range of 20 dBm to 30 dBm. Thus, a Spacek Labs Ka-band amplifier was introduced after the signal generator. The maximum power of the used amplifier is 29 dBm.

An isolator was placed in between the power amplifier and the 10dB directional coupler to minimise the influence of standing waves. Use of a coupler in the set-up allowed accurate monitoring of the input power ($P_{IN,AVA}$) Fig. 4.4(b). The 10 dB coupler was as used for the measurements of the reflected power (S_{11}), as shown in Fig. 4.4(c). An additional attenuator was placed between the coupler and the power sensor. Both $P_{IN,AVA}$ and the reflected power (S_{11}) were measured with an Agilent E4418B power sensor.

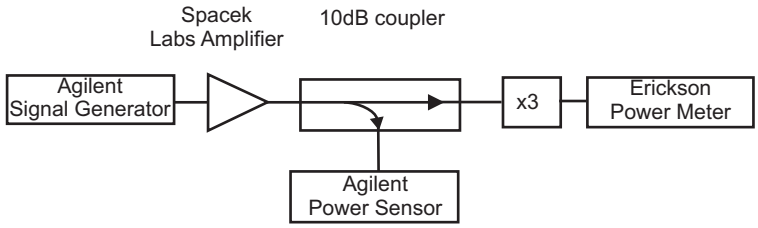
The power generated at the 3^{rd} harmonic was monitored with an Erickson PM4 power meter. The maximum measurable power by the power meter is 200 mW (23 dBm). Hence, an additional isolator with ca 2dBm insertion loss was placed in between the device and the output power sensor in the configuration presented in Fig. 4.4(b).

4.2 Results and discussion

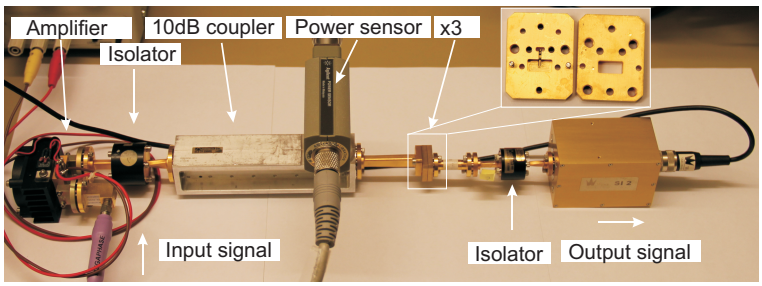
The RF characterised experimental data for the silicon integrated and monolithically integrated HBV frequency multipliers on InP substrate operating at W-band are presented in Fig. 4.5 - Fig. 4.8. All the data are given for HBV diodes with the following physical dimensions: 4 mesas connected in series, 12 barriers and 7×100 μm^2 contact area.

During the characterisation the devices were supplied with the $P_{IN,AVA}$ in the range of 20 to 29 dBm.

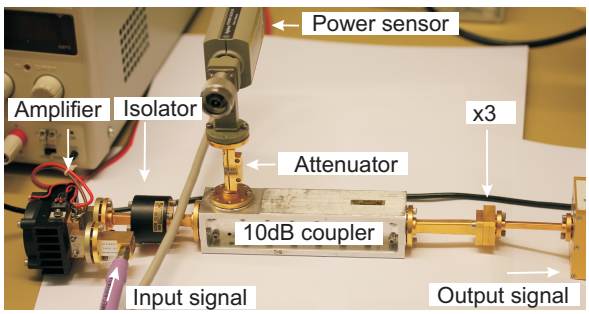
In Fig. 4.5(a) and Fig. 4.5(b) the measured output power as a function



(a)

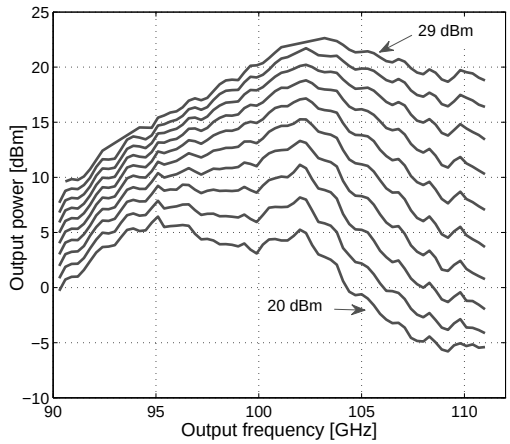


(b)

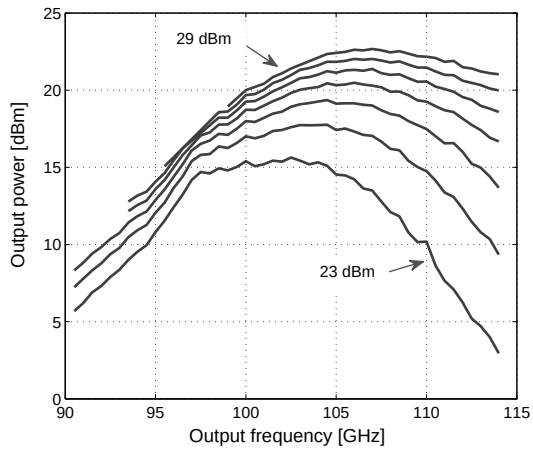


(c)

Fig. 4.4: (a) Schematic of the RF characterisation set-up. (b) Input power monitoring, (c) Reflection power measurements.



(a)



(b)

Fig. 4.5: Generated output power at 3^{rd} harmonic for the (a) silicon integrated and (b) monolithically integrated HBV frequency multipliers on InP substrate. The input power was swept from 20 - 29 dBm with 1 dBm increment.

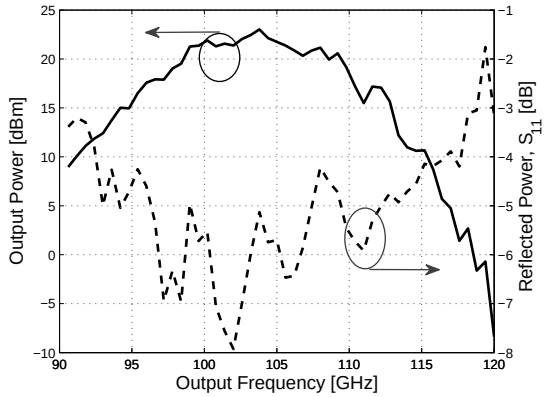


Fig. 4.6: Output (solid line) and reflected power (dashed line) measured at 29 dBm of $P_{IN,AVA}$ for the silicon integrated case. S_{11} was better than -6 dBm at the center frequency.

of the output frequency for a swept input power is presented. Worth noticing is the center frequency, which is 103 GHz and 107 GHz for the circuit on Si and InP substrate, respectively. This difference in the center frequencies for the circuit on Si and InP substrates could be attributed to the fact that the circuits were fabricated independently. Moreover, there is a distinct difference in the ohmic contact type (alloyed and non-alloyed for Si and InP, respectively), hence different contact resistances (R_c) are expected.

Measurements of S_{11} using the set-up configuration presented in Fig. 4.4(c) were performed to verify how much of the drive power that was reflected. The results of these characterisation at the peak output power for the silicon integrated frequency tripler together with the output power data is given in Fig. 4.7. The ripples in $P_{OUT,AVA}$ and S_{11} are caused by the variation of $P_{IN,AVA}$.

The 3-dB bandwidth was measured at the peak output power. Both circuits exhibits broad-bandwidth of operation. The integrated frequency multiplier on silicon and the circuit on InP show a 9 % and a 15 % bandwidth, respectively, Fig. 4.7.

Conversion loss (L_n) and maximum available output power measured at the center frequency against the $P_{IN,AVA}$ are plotted in Fig. 4.8, to compare the perfomrance of the demonstrated circuits. The circuit on InP substrate exhibits a better performance at lower input power levels. However, when the devices are driven with the maximum $P_{IN,AVA}$ (29 dBm), their performance is comparable. The maximum $P_{OUT,AVA}$ for both cases is equal to 22.6 dBm. L_n is ca 6.5 dB, corresponding to almost 23 % efficiency, Fig. 4.9.

Due to the limitations of the power amplifier ($P_{IN,AVA} \geq 29$ dBm) the circuits were not driven into saturation, therefore the maximum output power and efficiency were not reached. It is expected that these diodes are able to withstand at least 30 dBm (1 W) of input power.

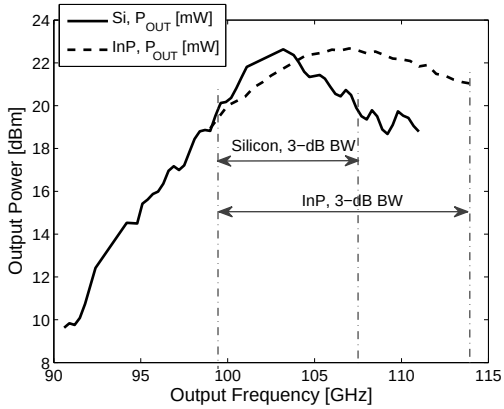


Fig. 4.7: 3-dB bandwidth at peak output power for circuit on Si (solid line) and InP (dashed line). 3-dB bandwidth is 9 % and 15 % for circuit on Si and InP, respectively.

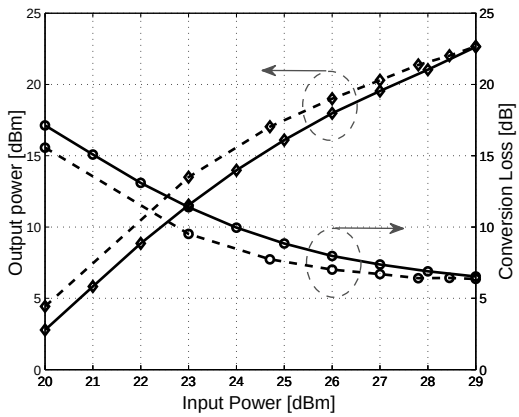


Fig. 4.8: Available output power and a conversion loss as a function of the input power measured at 103 GHz and 107 GHz for devices on Si (solid line) and InP (dashed line), respectively.

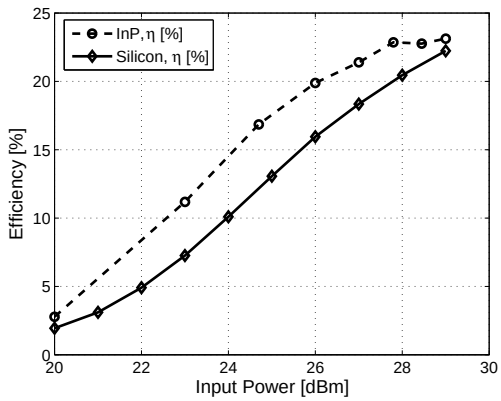


Fig. 4.9: Data for the maximum conversion efficiency at 103 GHz and 107 GHz, for Si and InP, respectively.

Chapter 5

Conclusions and future work

The main achievement of this work is the fabrication, characterization and demonstration of a silicon integrated InP-based HBV frequency multiplier. The InGaAs/ InAlAs/ AlAs HBV material structure has been transferred onto silicon employing a plasma activated wafer bonding.

In terms of multiplier performance the achieved 184 mW of output power, corresponding to 23 % conversion efficiency, and 9 % bandwidth is comparable with the monolithically integrated HBV frequency tripler on InP substrate. These results motivate for further development of heterogeneous integrated frequency multipliers employing HBVs.

Taking advantage of the mechanical properties of silicon, an advanced micromachining of membranes, via holes and filters can be easily realised. Moreover, waveguide channels integrated with antennas can be obtained in one process. This will eliminate a possible misalignment which at THz frequencies is detrimental.

In addition, silicon has two times higher thermal conductivity than InP or GaAs, which might result in an improved heat transfer and better power handling.

Summary of appended papers

Paper A

Silicon Integrated InGaAs/ InAlAs/ AlAs HBV Frequency Tripler

The results presenting a silicon integrated InGaAs/ InAlAs/ AlAs frequency tripler operating at W-band frequency range. The performance of the device is comparable with the state-of-the-art monolithically integrated HBV $\times$ 3 frequency multiplier described in **paper B**.
I personally contributed in the epitaxial transfer of InP-based HBV material structure onto silicon, fabrication, DC and RF characterisation, data analysis, and writing the paper.

Paper B

High Efficiency and Broad-Band Operation of Monolithically Integrated W-Band HBV Frequency Tripler

In this conference publication a monolithically integrated HBV frequency tripler on InP substrate is presented. The circuit delivers 185 mW output power, corresponding to 23 % efficiency, and 15 % of 3-dB bandwidth.
I personally contributed in the fabrication, DC and RF characterisation, data analysis and writing the paper.

Paper C

A 175 GHz HBV Frequency Quintupler With 60 mW Output Power

In this publication, a fixed tuned frequency quintupler at 175 GHz is described. The discrete HBV diode is flip-chip soldered into a microstrip matching circuitry. The circuit utilises the AlN as the substrate material to ensure an enhanced heat-dissipation from the active component.
I personally contributed in the fabrication and DC characterisation of the discrete devices, and writing.

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