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Modelling and Characterisation of Terahertz Planar Schottky Diodes

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Gothenburg, Sweden 2013

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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ISBN 978-91-7385-820-5

Doktorsavhandlingar vid Chalmers tekniska högskola
Ny serie Nr 3501
ISSN 0346-718X

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Technical Report MC2-241
ISSN 1652-0769

Cover: From left to right, a cross-sectional view of the EM field plot for a planar Schottky diode, a SEM image of a planar Schottky diode, an IR thermal image of 6-anode Schottky-based multiplier. Background: Smithchart showing measured S-parameters.

Printed by Kompendiet
Göteborg, Sweden, February, 2013

Abstract

This thesis deals with the modelling and characterisation of THz planar Schottky diodes, focusing on analyses of geometry-dependent electrical parasitics and the thermal management of the diode chip. Moving towards higher operating frequencies, the diode performance degrades due to high frequency losses, parasitic couplings and self-heating effects.

For geometry-dependent electrical parasitics analyses, the diode equivalent circuit parameters can be extracted from the measured or 3-D EM calculated S-parameters. For planar Schottky diodes, the available parameter extraction methods are typically based on an optimisation approach. In this work, a parameter extraction method based on an analytical approach is proposed. The proposed method allows for a fast and more reliable diode model extraction.

In this work, the high frequency diode parasitic resistance model is extended to include the eddy current and a mixture of skin and proximity effects. Due to the eddy current and proximity effects, the upper boundary of the buffer layer thickness is approximately one skin depth at the operating frequency, whereas the lower boundary is limited by the spreading resistance at DC.

Reactive energies stored in the parasitic capacitances and inductances cause an inherent limitation in the power coupling bandwidth to the intrinsic diode junction. The influence of diode geometry on fundamental power coupling bandwidth limitation is analysed using the Bode-Fano criterion. The result shows a trade-off between the parasitic capacitance and finger inductance, determined by the pad-to-pad distance, in optimising the diode geometry for a wide band diode matching.

A systematic thermal analysis of a 200 GHz multiplier chip developed by JPL is performed. The result shows that the chip thermal resistance is in the order of 10^3 K/W, whereas the overall thermal settling time is more than tens of milliseconds. The simulation result is verified through thermal imaging using infrared microscopy. Taking the thermal analysis a step further, a self-consistent electrothermal model for the multiplier chip is proposed. Compared to the circuit analysis without the thermal model, analysis with the electrothermal model shows a better agreement with the measured result, e.g., an error reduction from $\sim 13\%$ to $\sim 4\%$ between the simulated and measured maximum output power, by including the thermal effect.

Keywords: Bandwidth, Current crowding, Electromagnetic, Electrothermal, Geometric modelling, Proximity effect, Schottky diodes, Skin effect, Submillimetre wave generation and detection, S-parameter extraction, Thermal.

List of publications

Appended papers

This thesis is based on the following papers:

- [A] **A.Y. Tang**, V. Drakinskiy, K. Yhland, J. Stenarson, T. Bryllert, and J. Stake, “Analytical Extraction of a Schottky Diode Model based on Broadband S-Parameters,” accepted for publication in *IEEE Transactions on Microwave Theory and Techniques*, Jan. 2013.
- [B] **A.Y. Tang** and J. Stake, “Impact of Eddy Currents and Crowding Effects on High Frequency Losses in Planar Schottky Diodes,” in *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3260-3269, Oct. 2011.
- [C] **A.Y. Tang**, T. Bryllert, and J. Stake, “Geometry Optimization of THz Sub-harmonic Schottky Mixer Diodes,” *37th International Conference on Infrared, Terahertz and Millimeter Waves (IRMMW-THz)*, Wollongong, Australia, Sept. 2012.
- [D] **A.Y. Tang**, E. Schlecht, G. Chattopadhyay, R. Lin, C. Lee, J. Gill, I. Mehdi, and J. Stake, “Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes,” *22nd International Symposium on Space Terahertz Technology (ISSTT)*, Tucson, AZ, USA, Apr. 2011.
- [E] **A.Y. Tang**, E. Schlecht, R. Lin, G. Chattopadhyay, C. Lee, J. Gill, I. Mehdi, and J. Stake, “Electro-Thermal Model for Multi-Anode Schottky Diode Multipliers,” in *IEEE Transactions on Terahertz Science and Technology*, vol. 2, no. 3, pp. 290-298, May 2012.

Other papers and publications

The following publications are not included due to an overlap in contents or the contents are beyond the scope of this thesis.

- [a] J. Stake, T. Bryllert, R. Dahlbäck, V. Drakinskiy, J. Hanning, A. Malko, **A.Y. Tang**, J. Vukusic, H. Zhao, and P. Sobis, “Integrated Terahertz Electronics for Imaging and Sensing,” *19th International Conference on Microwaves, Radar and Wireless Communications (MIKON)*, Warsaw, Poland, May, 2012.

- [b] H. Zhao, V. Drakinskiy, P. Sobis, J. Hanning, T. Bryllert, **A.Y. Tang**, and J. Stake, "Development of a 557 GHz GaAs Monolithic Membrane-diode Mixer," *24th International Conference on Indium Phosphide and Related Materials (IPRM)*, Santa Barbara, CA, USA, Aug., 2012.
- [c] V. Drakinskiy, P. Sobis, **A.Y. Tang**, T. Bryllert and J. Stake, "Development of Planar THz Schottky Diodes," *6th ESA Workshop on Millimetre-Wave Technology and Applications*, Espoo, Finland, May, 2011.
- [d] J. Stake, H. Zhao, P. Sobis, **A.Y. Tang**, and V. Drakinskiy, "Development of a Compact 557 GHz Heterodyne Receiver," *6th ESA Workshop on Millimetre-Wave Technology and Applications*, Espoo, Finland, May, 2011.
- [e] H. Zhao, **A.Y. Tang**, P. Sobis, T. Bryllert, K. Yhland, J. Stenarson, and J. Stake, "Submillimeter Wave S-Parameter Characterization of Integrated Membrane Circuits," in *IEEE Microwave and Wireless Components Letters*, pp. 110-112, February, 2011.
- [f] H. Zhao, T.D.T. Ngoc, P. Sobis, **A.Y. Tang**, K. Yhland, J. Stenarson, and J. Stake, "Characterization of Thin-Film Resistors and Capacitors Integrated on GaAs Membranes for Submillimeter Wave Circuit Applications," *23rd International Conference on Indium Phosphide and Related Materials (IPRM)*, Berlin, Germany, May, 2011.
- [g] J. Stake, T. Bryllert, P. Sobis, **A.Y. Tang**, H. Zhao, J. Vukusic, A. Malko, V. Drakinskiy, A. Olsen, and A. Emrich, "Development of Integrated Submillimeter Wave Diodes for Sources and Detectors," *5th European Microwave Integrated Circuits Conference*, September, 2010.
- [h] **A.Y. Tang**, P. Sobis, H. Zhao, V. Drakinskiy, T. Bryllert, and J. Stake, "Analysis of the High Frequency Spreading Resistance for Surface Channel Planar Schottky Diodes," *35th International Conference on Infrared, Millimeter and Terahertz Wave (IRMMW-THz)*, Rome, Italy, September, 2010.
- [i] **A.Y. Tang**, P. Sobis, V. Drakinskiy, H. Zhao, and J. Stake, "Parameter Extraction and Geometry Optimisation of Planar Schottky Diodes," *21st International Symposium on Space Terahertz Technology (ISSTT)*, Oxford, UK, March, 2010.
- [j] H. Zhao, **A.Y. Tang**, P. Sobis, V. Drakinskiy, T. Bryllert, and J. Stake, "Characterization of GaAs Membrane Circuits for THz Heterodyne Receiver Applications," *21st International Symposium on Space Terahertz Technology (ISSTT)*, Oxford, UK, March, 2010.
- [k] H. Zhao, **A.Y. Tang**, P. Sobis, T. Bryllert, K. Yhland, J. Stenarson, and J. Stake, "VNA-Calibration and S-Parameter Characterization of Submillimeter Wave Integrated Membrane Circuits," *35th International Conference on Infrared, Millimeter and Terahertz Wave (IRMMW-THz)*, Rome, Italy, September, 2010.

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- [l] H. Zhao, **A. Y. Tang**, P. Sobis, V. Drakinskiy, T. Bryllert, and J. Stake, “340 GHz GaAs Monolithic Membrane Supported Schottky Diode Circuits,” *Gigahertz Symposium*, Lund, Sweden, March, 2010.
- [m] J. Stake, O. Habibpour, **A.Y. Tang**, H. Zhao, V. Drakinskiy, P. Sobis, J. Vukusic, and T. Bryllert, “Schottky Receivers and Graphene for Future THz Electronics,” *International Symposium on Terahertz Science and Technology between Japan and Sweden*, Göteborg, Sweden, November, 2009.
- [n] **A.Y. Tang**, V. Drakinskiy, P. Sobis, J. Vukusic, and J. Stake, “Modeling of GaAs Schottky Diodes for Terahertz Application,” *34th International Conference on Infrared, Millimeter and Terahertz Wave (IRMMW-THz)*, Busan, Korea, September, 2009.
- [o] J. Stake, Z. Herbert, **A.Y. Tang**, B. Banik, V. Drakinskiy, P. Sobis, J. Vukusic, S. Cherednichenko, A. Emrich, S. Rudner, T. Bryllert, and P. H. Siegel, “Terahertz Technology and Applications,” *International Symposium on Terahertz Science and Technology between Japan and Sweden*, Tokyo, Japan, May, 2008.

List of notations

c_p	Specific heat
f	Frequency
g	Heat generation rate per unit volume
k_B	Boltzmann's constant
m^*	Effective mass
q	Elementary charge
\vec{q}	Heat flux
t	Time
t_{buf}	Buffer layer thickness
t_{epi}	Epi-layer thickness
w_d	Junction depletion width
A	Area
A^{**}	Effective Richardson constant
C_j	Junction capacitance
C_{j0}	Zero-biased junction capacitance
C_{fp}	Finger-to-pad capacitance
C_{pp}	Pad-to-pad capacitance
C_S	Displacement capacitance
C_{th}	Thermal capacitance
D_{anode}	Anode contact diameter
E_F	Fermi energy
E_g	Bandgap energy
I_C	Junction displacement current
I_d	Total diode current
I_S	Reverse saturation current
I_j	Junction conduction current
L_f	Air-bridge finger inductance
L_S	Inertial inductance
L_M	Mixer conversion loss
N_d	Doping concentration
P^{dis}	Power dissipation
P_{loss}	Power loss
Q_j	Junction charge
$R_{contact}$	Ohmic contact series resistance
R_{epi}	Epi-layer series resistance
R_{finger}	Air-bridge finger series resistance
R_S	Series resistance

$R_{spreading}$	Spreading resistance
R_{th}	Thermal resistance
R_{\square}	Sheet resistance
S	Elastance
T	Temperature
T_{amb}	Ambient temperature
T_j	Junction temperature
V_{bd}	Breakdown voltage
V_d	Diode voltage
V_F	Forward-bias voltage
V_j	Junction voltage
V_R	Reverse-bias voltage
V_T	Thermal voltage
Z_S	Series impedance
Z_{bulk}	Bulk impedance
Z_{skin}	Skin effect impedance
Z_{th}	Thermal impedance
χ_s	Semiconductor electron affinity
δ_S	Skin depth
η	Diode ideality factor
η_{eff}	Multiplier conversion efficiency
κ	Thermal conductivity
λ	Wavelength
μ_n	Electron mobility
μ_p	Hole mobility
μ_0	Permeability in vacuum
ω	Angular frequency
ω_d	Dielectric relaxation frequency
ω_p	Plasma frequency
ω_s	Scattering frequency
ϕ_b	Barrier height
ϕ_m	Metal work function
ϕ_s	Semiconductor work function
ψ_{bi}	Semiconductor built-in potential
ρ_m	Material mass density
ρ_c	Specific contact resistivity
σ	Electrical conductivity
τ_{th}	Thermal time-constant
$v_{e,sat}$	Electron velocity saturation
$v_{e,peak}$	Electron peak velocity
ϵ_0	Permittivity in vacuum
ϵ_r	Material relative permittivity
ϵ_s	Semiconductor permittivity
Γ	Reflection coefficient

List of abbreviations

AC	A lternating current
Au	Gold (' A urum' in Latin)
CPW	C o- p lanar w aveguide
CVD	C hemical vapour d eposition
DC	D irect current
EM	E lectromagnetic
FD	F inite d ifference
FEM	F inite e lement m ethod
GaAs	G allium a rsenide
GaN	G allium n itride
GHz	G igahertz (10^9 Hz)
HBV	H eterostructure b arrier v aractor
HEB	H ot e lectron b olometer
IF	I ntermediate frequency
IR	I nfrared
JPL	J et P ropulsion L aboratory
LO	L ocal o scillator
MHz	M egahertz (10^6 Hz)
NB	Note well (' n ota b ene' in Latin)
PEC	P erfect e lectric c onductor
Pt	P latinum
RF	R adio frequency
SI	S emi- i nsulating
SIS	S uperconductor- i nsulator- s uperconductor
SiO ₂	S ilicon d ioxide
S-parameters	S cattering p arameters
THz	T erahertz (10^{12} Hz)
Ti	T itanium
VNA	V ector n etwork a nalysis
3-D	3 dimensional

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Chapter 1

Introduction

The terahertz (THz) spectrum is a part of the electromagnetic (EM) band located between the microwave and optical domains, circa 300 GHz ($\lambda = 1$ mm; photon energy=1.2 meV) to 3 THz ($\lambda = 100$ μm ; photon energy=12.4 meV). For the last few decades, there has been an increasing interest in THz applications [1, 2], such as in communication, biology, security imaging, radio astronomy and earth science applications. Among these multi-discipline applications, the primary driving force for the technology advancement is a strong need for THz heterodyne receivers [3] in radio astronomy and earth science applications. The success in building such receivers depends mainly on the receiver front-end performance.

The Schottky diode technology is one of the key technologies in building THz heterodyne receiver front-ends [3–6]. This is mainly due to its capability for room temperature operation and ease of integration enabling the development of long operating lifetime and compact instrumentations [7]. Several astronomy and earth science missions, such as Odin [8], Earth Observing System Microwave Limb Sounder [9] and Herschel Space Observatory [10], have been using Schottky diode technology as mixers and as multipliers in the local oscillator (LO) chains. Future missions call for more efficient receiver front-end designs operating at higher frequencies [11]. However, progressing upward in frequency, the Schottky diode performance degrades, i.e., there is an increase in the mixer noise temperature and a decrease of the mixer and multiplier power conversion efficiency.

This research work is devoted to the development of a better understanding of the planar Schottky diode operation in the THz region. In particular, the diode extrinsic properties, i.e., the diode parasitics and thermal properties, are investigated. Models are proposed for the diode performance optimisation.

1.1 Background

In general, THz detection and generation can be realised with a solid state electronic approach, by optical means or in a combination of both. This section introduces different THz detector and source technologies, and the Schottky diode technology is put into perspective. Following this, the Schottky diode historical development and progress in THz applications are briefly reviewed.

1.1.1 THz detectors and sources

At present, commonly deployed THz detectors are superconductor-insulator-superconductor (SIS) diode [12], hot electron bolometer (HEB) [13] and Schottky diode [4]. The ultimate low noise heterodyne detector technology is based on the superconducting mixers, i.e., SIS and HEB mixers. A comparison of the mixer noise temperature is shown in Fig. 1.1. For frequencies up to ~ 1 THz, the SIS mixer-based receiver noise temperature is excellent, i.e., close to the quantum limit ($\sim hv/k$). Beyond 1.2 THz, the performance of SIS mixers degrades significantly and the state-of-the-art noise performance is achieved by using HEB mixers.

Referring to Fig. 1.1, Schottky diode mixers exhibit higher noise temperatures compared to the superconducting mixers. However, the advantage of using Schottky diode mixers is their wide operating temperature range, either in a cooled or an uncooled condition. For room temperature (uncooled) operation, a cryogenic cooling system is not required. Thus, the receiver operating lifetime is not limited by the availability of cryogenic coolant. In addition to the room temperature operational capability, the Schottky diode mixers are also capable of operating in a wider intermediate frequency (IF) range and thus are able to cover a wider spectral instantaneously. However, in comparison to the superconducting mixers, a higher local oscillator (LO) power, typically in the milliwatts range, is required to pump the Schottky mixers. At present, developing compact high power THz sources is still a challenge in the THz technology development.

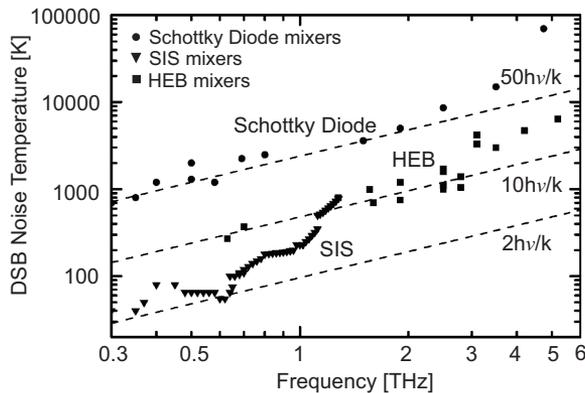


Fig. 1.1: Mixer noise temperature for THz heterodyne receivers [3].

High output power THz sources are available using vacuum-tube technology, such as gyrotrons, klystrons and backward wave oscillators (BWOs). However, this type of sources are bulky, large and/or expensive. Comparatively, low power sources are available through the solid state electronic technology [14], e.g., transistor amplifiers [15] and two-terminal device oscillators [16], such as Gunn diodes and IMPATT diodes. The oscillator output frequencies can be further multiplied to higher frequencies using devices with nonlinear electrical properties, such as heterostructure barrier varactor diodes (HBVs) [17–20] and Schottky diodes [4, 21]. In the optical domain, major effort has been devoted

to develop sources using quantum cascade lasers (QCLs) [22, 23], optically pumped gas laser [24] and difference frequency generator sources [25].

Fig. 1.2 shows a comparison of the output power for several THz source technologies. Progressing upward in frequency, output power of the solid-state electronic sources decreases. In contrast, the output power of the optical sources decreases when the frequency is reduced. Thus, the lack of high power sources in the THz region is known as the ‘THz gap’.

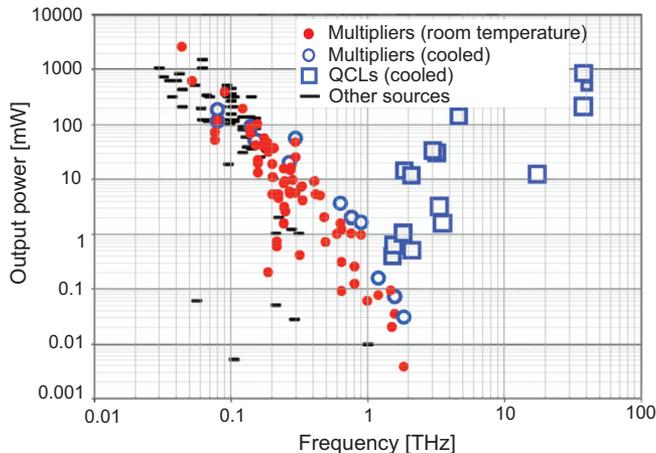


Fig. 1.2: Output power for THz sources [4].

Despite the availability of the above mentioned technologies, there are still plenty of room for development towards compact, portable and long operating lifetime type of detectors and sources. Considering either space-borne or ground-based commercial imaging applications, light weight and compact instruments are desired. Due to these practical demands on the instrumentation, the solid state electronic technology is a prevailing solution for THz detection and generation. In particular, the Schottky diode technology is an important solution in this respect.

1.1.2 Schottky diodes

Schottky diodes are based on the metal-semiconductor interface systems. The earliest study on the metal-semiconductor system was performed by Karl Ferdinand Braun back in 1874 [26]. In 1937, a German physicist, Walter H. Schottky, showed that a potential barrier arises from stable space charges in the semiconductor alone without the presence of a chemical layer [27]. The potential barrier is known as the Schottky barrier and this type of diode is named Schottky diode.

Since the introduction of Schottky diodes, they have been widely utilised. Dating back to 1904, Schottky type of diodes were used as radio detectors (up to 60 GHz) by Jagadis C. Bose [28, 29]. During the Second World War, the diodes were deployed as microwave radar detectors. In the 1960s, the diodes were used as clamps to enhance the switching speed of bipolar integrated circuits [30] and as gates for field-effect transistors (FETs) [31]. Since the

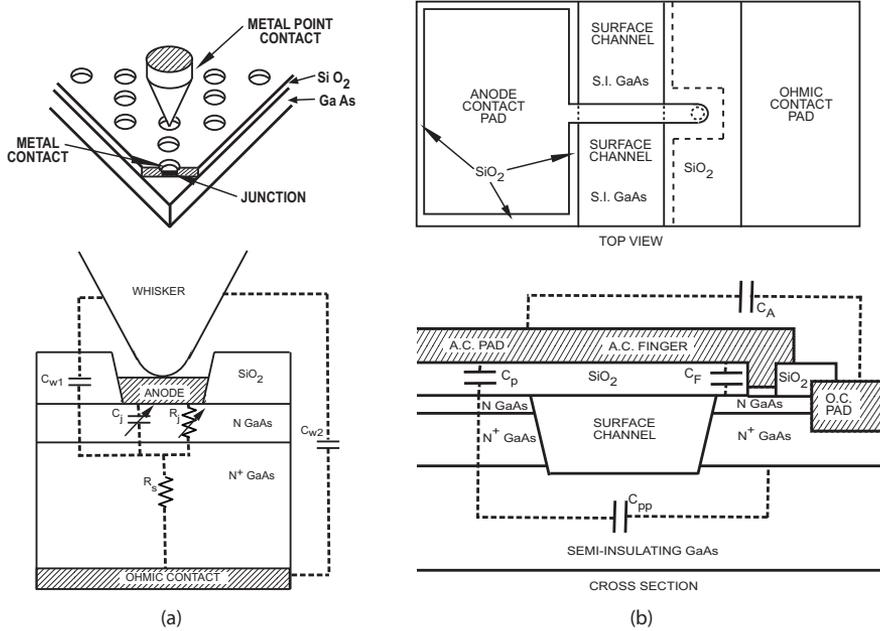


Fig. 1.3: (a) Honeycomb structure of whisker-contacted Schottky diode [32,35]; (b) Planar Schottky diode structure [35].

1970s, Schottky diodes have seen commercial importance as fast-switching devices, i.e., as saturation-prevention clamps and microwave diodes. Today, Schottky diodes are key components in room temperature THz heterodyne receiver front-ends.

For many years, gallium arsenide (GaAs)-based whisker-contacted Schottky diodes have been used in millimetre and submillimetre wavelength heterodyne receivers [32–34]. In this diode structure, the Schottky contact is formed by mechanically contacting an anode contact with a metal whisker probe (see Fig. 1.3(a)). This structure is inherently simple and it enables the fabrication of a very small area device with a low junction capacitance. In addition, the parasitic shunt capacitance in this structure is extremely low. In spite of the advantages of such a simple structure, the assembly and reliability of the whisker-contacted Schottky diode are of concern. In practice, multiple anode contacts are formed on the semiconductor to increase the probability for a proper whisker-anode contact. Attributed to its array geometry of close packed Schottky anodes, diodes with such structure are also known as honeycomb diodes.

In 1987, a planar structure diode technology was introduced by Bishop et al. at University of Virginia [35]. Compared to the whisker-contacted diodes, the planar diodes offer ease of assembly and ruggedness. Moreover, the introduction of planar structure Schottky diodes also opens the door for circuit integration towards building compact and low cost transmitters and receivers. However, the planar structure diodes exhibit higher parasitic shunt capacitance, which affects the planar diode high frequency performance. Sev-

eral possible planar structures, such as mesa structure, proton bombarded and surface-channel planar diodes, were investigated [35–37]. The investigation led to a conclusion that the lowest possible parasitic capacitance can be achieved using the surface-channel type of planar diode (see Fig. 1.3(b)). Therefore, the planar Schottky diode technology has been further developed and optimised based on the surface-channel planar configuration.

Since the late 1990s, significant effort has been devoted to optimise the planar diode circuit performance, ranging from diode device level physics and parasitics [38–41] to diode-circuit integration. In order to reduce substrate losses, the diode substrate transfer technology [36,42–45] and the monolithic diode-circuit integration technology, using membrane monolithic diode (MOMED) [46] and substrateless techniques [47], are developed. For thermal optimisation, technology for wafer bonding to CVD diamond substrate [48,49] is used. In addition to the surface channel planar structure, a quasi-vertical planar Schottky diode (QVD) structure has also been investigated [50].

Thus far, mixers using the whisker-contacted Schottky diode structure have been built for an operating frequency of 5 THz [34]. Meanwhile, the planar Schottky diode based mixers and multipliers have been demonstrated up to a frequency of 2.7 THz [7, 21, 46, 51–56]. Fig. 1.4 shows some examples of THz diode chip topologies and monolithic integrated circuits.

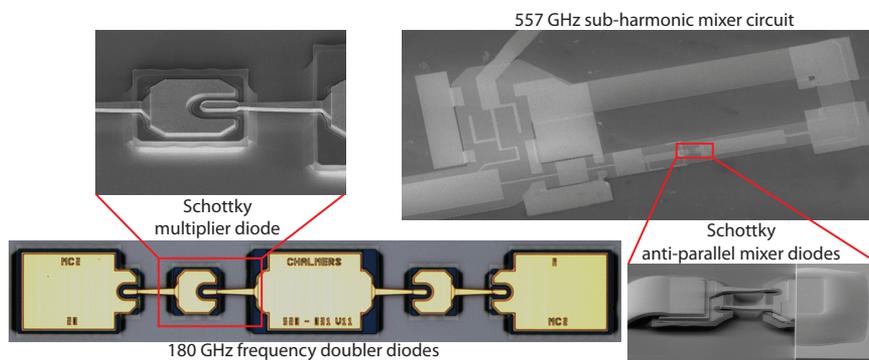


Fig. 1.4: Example of Schottky diode multiplier and mixer diode integrated circuits fabricated in the Nanofabrication Laboratory, Chalmers University of Technology.

1.2 Motivation and result

This research work is mainly motivated by the need for further optimisation of the diode performance in the THz frequency range. Although Schottky diode technology has been widely deployed in direct current (DC) and millimetre wave applications for decades, the state-of-the-art diode performance at submillimetre wave is still not fully understood. In view of this, a better understanding of the diode high frequency behaviour is needed, in order to extend the existing diode models and further optimise the diode performance.

In developing high frequency diode models, parameter extraction is an important ‘work horse’. For THz planar diodes, most of the parameter extrac-

tion methods are based on fitting S-parameters generated from the lumped-equivalent circuit model to those from measurement or 3-D EM numerical calculation. In other words, the extraction method is based on minimisation of a global error function defined using both sets of S-parameters. However, this method is sensitive to local minimum errors. In addition, a proper extraction of the diode air-bridge finger inductance and series resistance are challenging. Paper [A] proposed an analytical method to extract the planar Schottky diode equivalent circuit parameters from broadband S-parameters. The method has been validated using measured and 3-D EM calculated S-parameters. The frequency range required for a proper air-bridge finger and series resistance extraction is also addressed in this paper.

In the conventional diode series resistance models, the only current crowding effect considered is the skin effect. However, THz planar diodes exhibit a stronger frequency-dependent loss behaviour than that caused by skin effect. In Paper [B], the strong frequency-dependent loss is investigated. This work shows that, in addition to skin effect, the eddy current and a mixture of skin and proximity effect play a significant role in the loss mechanisms. Thus, careful diode geometry optimisation is needed to minimise losses. This paper proposes that the optimum buffer layer thickness is approximately one skin depth at the operating frequency. The volume of GaAs buffer layer material beneath the air-bridge finger has to be minimised, e.g., by fabricating diodes with a straight mesa wall instead of a slanted mesa wall, in order to minimise additional eddy current generation.

Another aspect of diode performance optimisation is to maximise the power coupling to the diode intrinsic junction. Moving towards higher frequencies, the impact of diode parasitics becomes increasingly important and limits the bandwidth for the power coupling. Paper [C] presents a systematic analysis of the geometry-dependent parasitics and their influence on the power coupling bandwidth.

Optimisation of diode electrical performance for high frequencies favors diode design with small anode contact area, as well as thin and low loss supporting substrate. These approaches have negative impact on the diode thermal management capability, e.g., resulting in higher power density in anodes and higher thermal impedance. For high power applications, the diode performance becomes thermally limited. Thermal modelling work for THz planar Schottky diodes is needed. Paper [D] presents a systematic thermal analysis of a current state-of-the-art multiplier. The diode 3-D geometrical and non-linear thermal behaviour are taken into account in this analysis. Several multiplier layouts, semiconductor materials and heat sinking approaches are investigated.

For a proper diode electrothermal co-analysis, the thermal effect has to be included in the diode electrical circuit analysis in a self-consistent approach. However, such a model is not available for THz planar Schottky diodes. Paper [E] proposed a self-consistent electrothermal model, which introduces a practical approach in co-analysing the diode electrical and thermal properties. This model is verified experimentally, showing a better agreement with the experimental data compared to the result predicted by a model without including the thermal effect.

1.3 Thesis outline

This thesis presents developments in modelling and characterisation of THz planar Schottky diodes. In Chapter 1, the interest in THz applications and the related challenges are discussed. The Schottky diode technology and its corresponding technology progress are then presented. Finally, the motivation and the result of this work are briefly introduced.

Chapter 2 provides a general description of the Schottky diode for THz applications. This chapter begins with the basic diode operating principle, and further discusses the high frequency and high power related behaviour which results in the diode performance degradation. Following this, issues specifically related to the planar diode structure are elaborated. At the end of this chapter, diode design and optimisation principles, for both mixer and multiplier applications, are presented.

Chapter 3 presents a brief review of the electrical and thermal characterisation methods, whereas Chapter 4 describes the overview of modelling work for THz planar Schottky diodes. These two chapters also place a summary of my research work (presented in Paper [A] to Paper [E] and other unpublished work) in relation to the overall work in the THz planar Schottky diode research field. Chapter 5 concludes the research work and discusses the future outlook.

Chapter 2

THz planar Schottky diodes

This chapter provides an overview of the Schottky diode operation, as well as the high frequency and high power related diode behaviour. General physics of the metal-semiconductor interface, forming a Schottky barrier, and the corresponding diode equivalent circuit model are presented. The diode operation as a varistor and a varactor is described. This is followed by a discussion focusing on the planar structure type of Schottky diode. Finally, the varistor and varactor diode design parameters for mixer and multiplier performance optimisation are discussed.

2.1 Overview of Schottky diode operation

The fundamental operation of a Schottky diode is attributed to carrier transport mechanisms over a Schottky barrier, which is formed at a metal-semiconductor interface. Fig. 2.1 illustrates the metal-semiconductor interface and the corresponding diode terminal notations in the diode symbol.

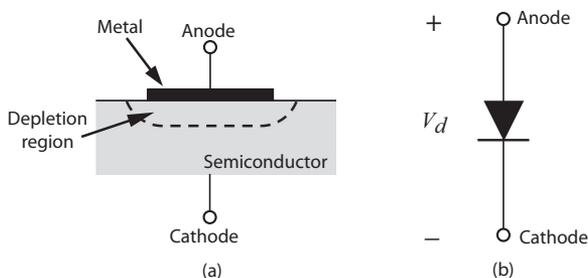


Fig. 2.1: (a) Schematic of a metal-semiconductor interface; (b) Symbol of a diode. V_d is the voltage drop across the diode anode and cathode terminals.

In designing Schottky diodes, both n- or p-type semiconductors can be used. Commonly used semiconductors are gallium arsenide (GaAs), silicon

(Si), gallium nitride (GaN), silicon carbide (SiC), indium phosphide (InP) and indium gallium arsenide (InGaAs). Examples of metals used for Schottky anode contacts are titanium (Ti), platinum (Pt), chromium (Cr), tungsten (W), molybdenum (Mo), and various alloys.

For THz applications, n-doped GaAs is a typical semiconductor used due to its high electron mobility and the relatively low current leakage through the Schottky barrier. The GaAs material data is listed in Table 2.1. The typical metal system for the anode contact is Ti/Pt/Au. Thus, the foundation of Schottky diode operation in this thesis is built based on the Ti/Pt/Au contact deposited on GaAs metal-semiconductor system.

Table 2.1: Material properties of GaAs at room temperature [57, 58].

Material Properties	Symbol	Value	Unit
Bandgap energy	E_g	1.42	eV
Relative dielectric constant	ϵ_r	12.9	-
Effective mass	(m^*/m_0)		
- electrons	m_e^*	0.063	-
- holes	m_{lh}^*	0.076	-
	m_{hh}^*	0.50	-
Drift mobilities (intrinsic)			
- electrons	μ_n	8000	$\text{cm}^2/\text{V} \cdot \text{s}$
- holes	μ_p	400	$\text{cm}^2/\text{V} \cdot \text{s}$
Saturation velocity	v_{sat}	7×10^6	cm/s
Peak velocity	v_{peak}	2×10^7	cm/s
Thermal conductivity	κ	50.6	W/m·K
Specific heat	c_p	327	J/kg·°C
Density	ρ_m	5.317	g/cm ³

Fig. 2.2 illustrates the formation of a Schottky barrier. For an ideal contact, a barrier height, ϕ_b , can be calculated as the difference between the metal work-function, ϕ_m , and the semiconductor electron affinity, χ_s . In practice, the barrier height dependency on metal work function is weak compared to the ideal case. Experimental characterisations showed that the metal-GaAs barrier height is close to 0.8 V, regardless of the metal contact work-function [59]. The nearly constant barrier height scenario is related to an imperfect metal-GaAs interface, due to the existence of semiconductor surface states [60] and image-force lowering effect. Thus, the estimation of a practical barrier height is rather complicated [61]. Today, literature in treating the physics of the metal-semiconductor system is vastly available [26, 27, 57, 60–67].

In thermal equilibrium, the semiconductor region adjacent to the metal contact is depleted of electrons. Electron transport from the semiconductor to the metal contact is blocked by an energy barrier, known as the built-in potential, ψ_{bi} . The width of the depletion region, $w_d(V_j)$, and energy barrier can be modulated by altering the potential between the metal and semiconductor, i.e., by applying voltage across the diode terminals (see Fig. 2.3).

Under a forward-biased condition, the energy barrier is lowered by the amount of forward-bias voltage, V_F . In this case, the diode operates as a

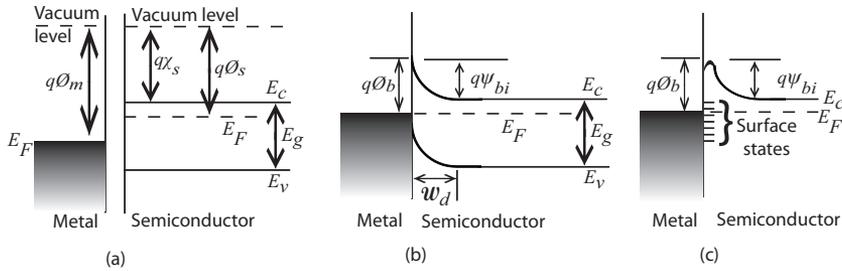


Fig. 2.2: Energy-band diagram of a metal-semiconductor system: (a) prior contact; (b) ideal contact; (c) practical contact in thermal equilibrium. E_F is the Fermi energy, E_g is the semiconductor bandgap energy, E_c is the bottom edge of the conduction band, E_v is the top edge of the valence band, ϕ_s is the semiconductor work function, and ψ_{bi} is the built-in potential.

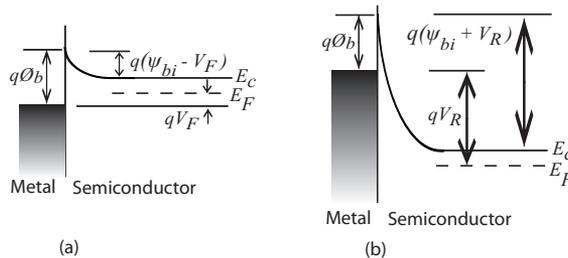


Fig. 2.3: Energy-band diagram for a metal-semiconductor system under: (a) a forward-biased condition; (b) a reverse-biased condition.

voltage-controlled resistor, i.e., a variable resistor (varistor) [68]. On the contrary, when the diode is reverse-biased with V_R , the energy barrier is increased and the depletion width is widened. The diode acts as a voltage-controlled capacitor, i.e., a variable capacitor (varactor) [69].

Fig. 2.4(a) illustrates a cross-sectional view of a GaAs-based Schottky diode. Comparing to Fig. 2.1, a buffer layer and an ohmic contact are shown. A buffer layer is a highly doped GaAs layer, i.e., with a doping concentration $N_{d,buf} > 10^{18} \text{ cm}^{-3}$, which is used to facilitate the current flow from the epilayer to the ohmic contact. Meanwhile, an ohmic contact allows current flow between the semiconductor and the external circuit.

A typical Schottky diode equivalent circuit consists of a voltage-dependent current source, $I_j(V_j)$, charge source, $Q_j(V_j)$, and a series resistor, R_S [70] (see Fig. 2.4(b)). The diode intrinsic properties are dependent on the junction voltage, V_j . The series resistor represents the total resistance beginning from the edge of depleted semiconductor to the cathode ohmic-contact, written as

$$R_S(V_j, f) \approx R_{epi}(V_j, f) + R_{spreading}(f) + R_{contact}(f), \quad (2.1)$$

where R_{epi} is the resistance due to undepleted epi-layer, $R_{spreading}$ is the resistance due to current spreading in the buffer layer and $R_{contact}$ is the resistance due to semiconductor-ohmic contact. Although the R_{epi} is voltage-

dependent, its voltage-dependency is usually weak and the series resistance is treated as an extrinsic element.

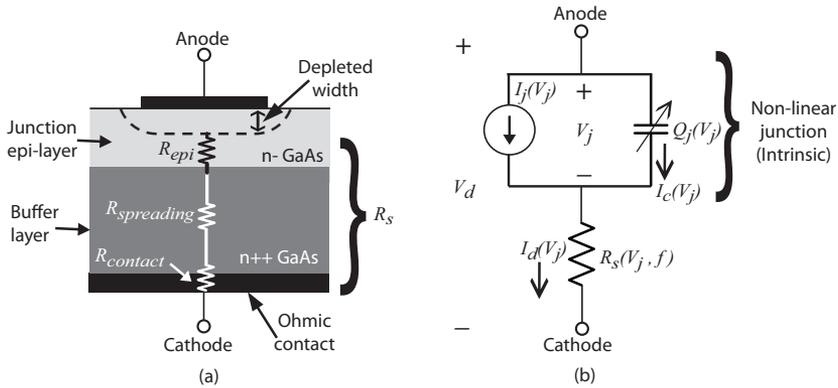


Fig. 2.4: (a) Cross-sectional view of a GaAs-based Schottky diode; (b) diode equivalent circuit.

2.1.1 Current-voltage characteristic

For a good metal-GaAs Schottky contact, the overall carrier transport mechanism is dominated by thermionic emission. A typical current-voltage ($I - V$) relationship [57, 66] of a Schottky diode is

$$I_j(V_j, T) = I_S \left(e^{\frac{qV_j}{\eta k_B T}} - 1 \right), \quad (2.2)$$

where

$$I_S(T) = AA^{**}T^2 e^{\frac{-q\phi_b}{k_B T}}, \quad (2.3)$$

I_j = diode junction conduction current,

I_S = reverse saturation current,

V_j = junction voltage,

q = elementary charge (1.6×10^{-19} Coulomb),

η = ideality factor,

A = Schottky anode junction area,

A^{**} = effective Richardson's constant,

T = absolute temperature,

ϕ_b = barrier height,

k_B = Boltzmann's constant (1.37×10^{-23} J/K).

Ideally, the ideality factor, η , in (2.2) is close to unity. However, in practice, the ideality factor departs from unity due to the onset of other carrier transport mechanisms, such as tunnelling. The carrier transport mechanism based on tunnelling is more pronounced at a lower temperature and a higher doping concentration in the junction epi-layer, $N_{d,epi}$. The effects of doping concentration and temperature on the ideality factor are formulated as

$$\eta = \left(k_B T \left(\frac{\tanh\left(\frac{E_{00}}{k_B T}\right)}{E_{00}} - \frac{1}{2E_B} \right) \right)^{-1}, \quad (2.4)$$

where

$$E_{00} = 18.5 \times 10^{-12} \sqrt{\frac{N_{d,epi}}{m_r^* \varepsilon_r}}, \quad (2.5)$$

E_B is the band bending $q(\psi_{bi} - V_F)$, E_{00} is a material constant in eV, m_r^* is the effective tunneling mass in unit of free electron mass, $N_{d,epi}$ is the epi-layer doping concentration in cm^{-3} and ε_r is the semiconductor relative permittivity [64]. For $k_B T \gg E_{00}$, the overall electron transport mechanism is dominated by thermionic emission.

When the diode is highly forward-biased, i.e., $V_j > 3k_B T/q$, the diode current expression can be simplified to

$$I_j(V_j, T) \approx I_S e^{\frac{qV_j}{\eta k_B T}}, \quad (2.6)$$

where

$$V_j = V_d - I_d R_S. \quad (2.7)$$

In a reverse-biased condition, the region of semiconductor under the metal contact is depleted of electrons and only occupied by the ionized donors. As the diode junction is further reverse-biased, the electric field across the junction increases and the electron conduction current reduces. Theoretically, at a limit of $V_j \rightarrow -\infty$, $I_j \rightarrow -I_S$. However, in practice, a high reverse-bias voltage results in a high electric field across the junction, causing the junction to breakdown. The breakdown voltage, V_{bd} , can be estimated using

$$V_{bd} = 60 \left(\frac{E_g}{1.1} \right)^{\frac{3}{2}} \left(\frac{N_{d,epi}}{10^{16}} \right)^{-\frac{3}{4}} \quad (2.8)$$

where $N_{d,epi}$ is the epi-layer doping concentration in cm^{-3} and E_g is the bandgap energy in eV [57].

2.1.2 Capacitance-voltage characteristic

When the depletion region is depleted of electrons, the diode capacitance-voltage ($C - V$) relation can be derived using Poisson's equation, giving the voltage-dependent junction charge and capacitance as

$$Q_j(V_j) = -2C_{j0} \psi_{bi} \sqrt{1 - \frac{V_j}{\psi_{bi}}} \quad (2.9)$$

and

$$C_j(V_j) = \frac{dQ_j(V_j)}{dV_j} = C_{j0} \sqrt{\frac{\psi_{bi}}{\psi_{bi} - V_j}}, \quad (2.10)$$

respectively [70]. Here, the C_{j0} is the zero-biased junction capacitance, written as

$$C_{j0} = A \sqrt{\frac{q \varepsilon_s N_{d,epi}}{2 \psi_{bi}}}, \quad (2.11)$$

where ε_s is the semiconductor dielectric constant.

The diode can be modelled as a parallel plate capacitor, with the depletion width, $w_d(V_j)$, as the distance between both plates. For a diode with an anode contact area of A , the junction capacitance, $C_j(V_j)$, is calculated using

$$C_j(V_j) = \frac{\varepsilon_s A}{w_d(V_j)}, \quad (2.12)$$

where

$$w_d(V_j) = \sqrt{\frac{2\varepsilon_s(\psi_{bi} - V_j)}{qN_{d,epi}}}. \quad (2.13)$$

For small anode diodes, e.g. sub-micron anode diodes, a first order edge fringing effect correction term can be included by adding a geometry-dependent constant, $\frac{3\varepsilon_s A}{D_{anode}}$, to (2.12) [71], with D_{anode} as the diameter of anode contact.

The above mentioned capacitance-voltage characteristic is only valid in the absence of electrons in the depletion region. For forward-biased cases at or beyond the flat-band condition, the electron conduction current increases and affects the carrier distribution. Thus, in this case, the capacitance has to be calculated numerically using semiconductor transport equations [72].

2.1.3 Series resistance

The diode series resistance, R_S , is a non-trivial parasitic element where power is dissipated. Referring to Fig. 2.4, the series resistance of a diode comprises epi-layer resistance, spreading resistance and contact resistance, as in (2.1).

- **Junction epi-layer resistance, R_{epi}**

A junction epi-layer resistance, R_{epi} , arises due to the undepleted epi-layer. For a typical THz diode, the junction epi-layer thickness, t_{epi} , is within a range of tens to hundreds of nanometres. The electrical conductivity of the epi-layer, σ_{epi} , is lower than that of the buffer layer. Therefore, the current flow path in the undepleted epi-layer to or from the buffer layer can be assumed to be confined under the anode contact. By assuming a negligible current spreading effect, the epi-layer resistance is approximated by

$$R_{epi}(V_j) = \frac{t_{epi} - w_d(V_j)}{A\sigma_{epi}}, \quad (2.14)$$

where

$$\sigma_{epi} = q\mu_{n,epi}N_{d,epi}, \quad (2.15)$$

and $\mu_{n,epi}$ is the electron mobility in the junction epi-layer.

For a highly forward-biased diode, the depletion width is assumed to be zero, providing an upper limit of the resistance. In a reverse-biased mode, the epi-layer can be fully depleted. Thus, alternatively, the epi-layer resistance can be estimated by taking into account the dynamic depletion width [69]. With this, the epi-layer resistance can be written as

$$R_{epi}(V_j) = R_{epi,min} + \frac{1}{qN_{d,epi}A^2\sigma_{epi}} (Q_{j,max} - Q_j(V_j)), \quad (2.16)$$

where $R_{epi,min}$ and $Q_{j,max}$ are the minimum series resistance and maximum junction charge, respectively. These are usually values at the maximum depletion width.

- **Buffer layer spreading resistance, $R_{spreading}$**

Attributed to a higher buffer layer conductivity and a larger ohmic contact area, the current is spread out in this layer. Due to the nature of current spreading, the calculation of the spreading resistance is inherently geometry-dependent. For a vertical diode with a circular anode contact (see Fig. 2.4(a)), the DC spreading resistance is estimated using

$$R_{spreading} = \frac{1}{2\sigma_{buf}D_{anode}} \frac{2}{\pi} \arctan \frac{4t_{buf}}{D_{anode}}, \quad (2.17)$$

where

$$\sigma_{buf} = q\mu_{n,buf}N_{d,buf}, \quad (2.18)$$

and $N_{d,buf}$, $\mu_{n,buf}$ and t_{buf} are the buffer layer doping concentration, electron mobility and thickness, respectively [73]. When $D_{anode} \ll t_{buf}$, (2.17) can be simplified to

$$R_{spreading} \approx \frac{1}{2\sigma_{buf}D_{anode}}. \quad (2.19)$$

The spreading resistance of a planar diode is more complicated due to the lateral current flow from the anode contact to the ohmic cathode contact (see Chapter 2.2.2).

- **Ohmic contact resistance, $R_{contact}$**

For a vertical diode, the ohmic contact resistance is a function of the ohmic contact area, A_{ohmic} , and the technology-dependent specific contact resistivity, ρ_c , as in

$$R_{contact} = \frac{\rho_c}{A_{ohmic}}. \quad (2.20)$$

For a planar diode, the ohmic contact resistance can be estimated using

$$R_{contact} = \frac{\sqrt{R_{\square}\rho_c}}{W_{ohmic}} \coth \left(L_t \sqrt{\frac{R_{\square}}{\rho_c}} \right), \quad (2.21)$$

where R_{\square} is the buffer layer sheet resistance in Ω/\square while L_t and W_{ohmic} are the current transfer length and ohmic contact width, respectively [59, 74].

Typical metallisation systems used for Schottky diode ohmic-contact are the Ni/Ge/Au [75] and Pd/Ge/Au [76, 77]. Contact technology based on these metallisation systems yields a low specific contact resistance, which is in the order of $10^{-6} \Omega \cdot \text{cm}^2$ or lower.

2.1.4 Thermal properties

Heat is generated when power is dissipated, i.e., when electrical current is passed through a resistive conductor. Various cooling mechanisms, such as

conduction, convection and radiation, are involved in the heat transfer. By considering only the dominating cooling mechanism, i.e., the conduction mechanism, the thermal problem can be analysed by solving the heat equation, expressed as

$$\rho_m c_p(T) \frac{\partial T(x, y, z, t)}{\partial t} = \nabla \cdot (\kappa(T) \nabla T(x, y, z, t)) + g, \quad (2.22)$$

where ρ_m is the material mass density, $c_p(T)$ is the material specific heat, $T(x, y, z, t)$ is the local temperature, $\kappa(T)$ is the material thermal conductivity and g is the heat generation rate per unit volume [78].

For a steady-state case, this equation is reduced to Fourier's heat law

$$\vec{q} = -\kappa(T) \nabla T, \quad (2.23)$$

where \vec{q} is the heat flux. Generally, the thermal problem can be modelled using an interdisciplinary electrical analogy as presented in Table 2.2.

Table 2.2: Analogy between the electrical and the thermal disciplines.

Electrical discipline		Thermal discipline
Electrical current, I [A]	\longleftrightarrow	Heat rate, P [W]
Electrical potential, V [V]	\longleftrightarrow	Temperature, T [K]
Electrical resistance, R [Ω]	\longleftrightarrow	Thermal resistance, R_{th} [K/W]
Electrical conductivity, σ [S/m]	\longleftrightarrow	Thermal conductivity, κ [W/m · K]
Charge storage capacity, C [F]	\longleftrightarrow	Thermal heat capacity, C_{th} [J/K]

For most semiconductors, the thermal problem is a nonlinear phenomenon. The thermal conductivity and thermal capacity for GaAs and other semiconductor materials are temperature-dependent. The conductivity-temperature relation of GaAs is approximated by

$$\kappa_{GaAs}(T) = 50.6 \left(\frac{300}{T} \right)^{1.28} \quad (2.24)$$

for $150 \text{ K} < T < 1500 \text{ K}$ [58].

For specific cases, e.g., within a narrow temperature range, the thermal problem can be linearised. With the electrical analogy, the linearised steady-state and transient junction temperature, T_j , can be calculated using

$$T_j - T_{amb} = R_{th}(T) P^{dis}, \quad (2.25)$$

$$T_j(t) = T_j(0) \left(1 - e^{-\frac{t}{\tau_{th}}} \right) + T_{amb}, \quad (2.26)$$

where

$$\tau_{th} = R_{th} C_{th}, \quad (2.27)$$

τ_{th} is the thermal time constant, T_{amb} is the ambient temperature, R_{th} is the thermal resistance and C_{th} is the thermal capacitance. Thus, the effectiveness of the heat transport away from the diode junction is characterised by a thermal impedance, Z_{th} , as illustrated in Fig. 2.5.

For a complete nonlinear thermal solution, a numerical approach is typically used [79, 80].

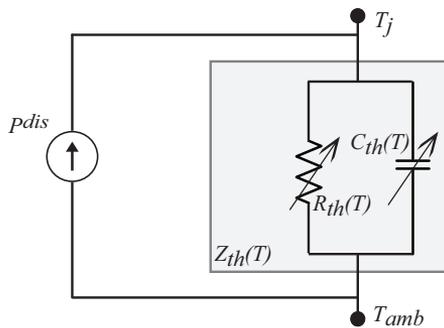


Fig. 2.5: A linearised thermal model.

2.1.5 High frequency and high power behaviour

The diode performance is degraded when the operating frequency and/or the operating power is increased above a certain limit. To date, several phenomena resulting in the performance degradation have been identified, such as

- frequency-dependent series resistance
- current saturation effect
- self-heating effect

• Frequency-dependent series resistance

For high frequency operation, studies show that an increase in the series resistance, in particular the spreading resistance, is related to the semiconductor carrier-inertia, displacement current, and skin effect [38, 81, 82]. As a consequence, the low frequency semiconductor spreading resistance model has to be expanded to a complex impedance model, Z_S , written as

$$Z_S = Z_{skin} + Z_{bulk}, \quad (2.28)$$

where Z_{skin} is the skin effect impedance and Z_{bulk} is the bulk material frequency-dependent impedance (see Fig. 2.6) [38].

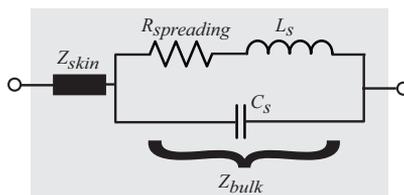


Fig. 2.6: High frequency spreading impedance.

The skin effect arises due to the magnetic field induced by the time-varying current flowing in a conductor. The onset of the skin effect reduces the effective current flow cross-section. Maximum current flows at the surface of the conductor and then the current decreases inside the conductor. The depth from the surface of the conductor at which the current density is reduced to $1/e$ of the current density at the surface of conductor is known as the skin depth, δ_S [83]. Considering an operating frequency that is far below the dielectric relaxation frequency, the skin depth can be estimated using

$$\delta_S = \sqrt{\frac{2}{\omega\mu_0\sigma}}, \quad (2.29)$$

where ω is the angular frequency and μ_0 is the vacuum permeability [84]. For a case where significant displacement current exists, the skin depth has to be calculated from the real part of the propagation constant.

As in Fig. 2.6, the bulk spreading impedance consists of a DC spreading resistance, an inertial inductance, L_S , and a displacement capacitance, C_S . The inertial inductance is related to the scattering frequency, ω_s , whereas the displacement current is related to the dielectric relaxation frequency, ω_d . These frequencies are calculated using

$$\omega_s = \frac{q}{m_e^*\mu_n}, \quad (2.30)$$

and

$$\omega_d = \frac{\sigma}{\varepsilon_s}, \quad (2.31)$$

where m_e^* is the electron effective mass, μ_n is the electron mobility and σ is the electrical conductivity [38]. The classical plasma frequency, ω_p , can then be calculated with

$$\omega_p = \sqrt{\omega_s\omega_d}. \quad (2.32)$$

By using the empirical low-field mobility model by Sotoodeh et al. [85], the frequencies described in (2.30)-(2.32) are calculated for several doping concentrations and presented in Table 2.3. An analytical expression of the spreading impedance for a bulk-type (vertical) diode is developed in [38]. In short, the impedance-frequency relation can be approximated by

$$Z_{skin} \propto \left(\frac{1}{1 + j\frac{\omega}{\omega_s}} + j\frac{\omega}{\omega_d} \right)^{-\frac{1}{2}} \quad (2.33)$$

and

$$Z_{bulk} \propto \left(\frac{1}{1 + j\frac{\omega}{\omega_s}} + j\frac{\omega}{\omega_d} \right)^{-1}. \quad (2.34)$$

Table 2.3: Bulk carrier scattering, dielectric relaxation and plasma frequency.

N_d [cm ⁻³]	$\frac{\omega_s}{2\pi}$ [THz]	$\frac{\omega_d}{2\pi}$ [THz]	$\frac{\omega_p}{2\pi}$ [THz]
5×10^{16}	0.9	5.7	2.2
5×10^{17}	1.4	35.6	7.0
5×10^{18}	2.4	204	22

In addition to the high frequency carrier transport phenomena, the spreading resistance is also affected by the diode geometry-dependent electromagnetic coupling, e.g., the eddy current and proximity effects (see Chapter 2.2.2.1). Taking these high frequency phenomena into consideration, the series impedance is inherently a complex function of device geometry and material property.

- **Current saturation effect**

For a diode operating as a varactor, the dominating current through the diode junction is the displacement current, $i_C(t)$, written as

$$i_C(t) = C_j(t) \frac{dv_j(t)}{dt}. \quad (2.35)$$

During normal diode operation, the displacement current in the junction is matched to the electron conduction current, $i_d(t)$, in the undepleted epi-layer. However, the conduction current in the undepleted epi-layer is limited by the velocity saturation current

$$i_d^{vsat} = qAN_{d,epi}v_{e,max}, \quad (2.36)$$

where $v_{e,max}$ is peak electron velocity. As the displacement current is increased above the velocity saturation current, the limited conduction current can be modelled as an increase in the effective epi-layer series resistance [40].

- **Self-heating effect**

As a consequence of excess heat in the junction area, the diode electrical properties, such as electron mobility, thermal voltage and thermionic emission carrier transport mechanism, are modified. The temperature-dependent electron mobility generally results in an increase in the series resistance, when the temperature is raised. The temperature dependencies of the diode thermal voltage and current are

$$V_T(T) = \frac{k_B T}{q}, \quad (2.37)$$

and

$$I_j(T) \propto T^2 e^{\frac{-\phi_b}{V_T}} e^{\frac{V_j}{V_T}}. \quad (2.38)$$

Besides degrading the diode performance, thermal effects also influence the diode reliability as well as causing issues such as thermal instability. Thus, the thermal management has to be considered during the diode design [86]. For example, the maximum operating temperature should be maintained below 450 K.

2.2 Schottky diode in a planar structure

The motivation and progress of Schottky diode technology development, from whisker-contacted to planar structure type of diode, is presented in Chapter 1.1.2. Also indicated in Chapter 1.1.2, the surface-channel configuration of planar diodes is the configuration with lowest possible parasitic capacitances among other types of planar diodes [36]. This section focuses on the discussion of surface-channel planar diodes.

2.2.1 Physical structure

Fig. 2.7 shows the physical structure of a surface-channel planar Schottky diode.

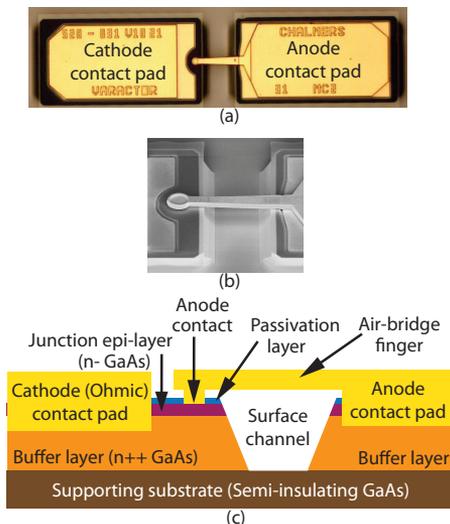


Fig. 2.7: Planar Schottky diode: (a) Microscope picture; (b) Scanning electron micrograph; (c) Cross-sectional view around the anode contact and surface-channel area. (NB! The drawing is not to scale.)

The anode contact is formed by depositing metal on the low-doped junction epi-layer (n-GaAs layer). By etching through the epi-layer down to the buffer layer, the ohmic contact is formed at a distance of a few micrometres away from the Schottky anode contact. For diode to circuit connection, a narrow metal connection is formed across the surface-channel to route the Schottky anode path to a large anode contact pad. This narrow metal connection is known as the air-bridge finger.

The GaAs material beneath the air-bridge finger is removed in order to isolate the anode and cathode pads, forming a surface air channel. The semi-insulating GaAs substrate serves as a supporting structure for the diode, whereas the silicon dioxide (SiO_2) or silicon nitride (Si-N) layer passivates the top semiconductor surfaces. Further details on the diode fabrication process can be found in [35, 37, 46, 52, 87].

2.2.2 Planar diode equivalent circuit

Fig. 2.8 shows a cross-sectional view of the planar diode, with its intrinsic model and parasitic elements. A typical planar diode lumped equivalent circuit is presented in Fig. 2.9. In the diode equivalent circuit, the cathode and anode pads are modelled using C-L-C π networks. All of the resistive elements indicated in Fig. 2.8 are modelled as a resistor, R_S , in Fig. 2.9. The fringing field between the anode and cathode contact pads, via air and substrate, is

modelled as a pad-to-pad capacitance, C_{pp} , written as

$$C_{pp} = C_{pp}^{air} + C_{pp}^{subs}. \quad (2.39)$$

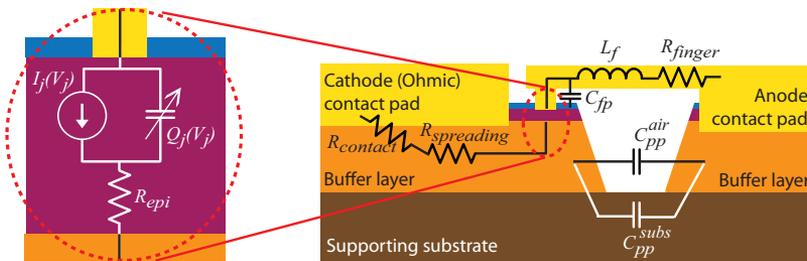


Fig. 2.8: Diode intrinsic model and parasitic elements. (NB! The drawing is not to scale.)

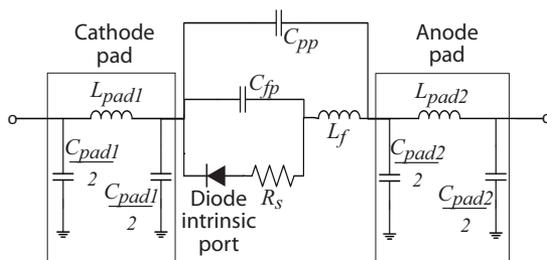


Fig. 2.9: Planar diode lumped equivalent circuit.

2.2.2.1 Parasitic resistances

The parasitic series resistance formulation for a planar diode is similar to that of a vertical diode, described using (2.1). However, in this case an air-bridge finger resistance component, R_{finger} , is added. Due to the lateral current flow nature and a less than 360° circumferential enclosure of the ohmic-contact around the anode contact, the calculation of the spreading resistance in the buffer layer is not straightforward. For a planar diode, a 3-D numerical approach is a common method for the DC spreading resistance estimation.

At high frequencies, the current crowding phenomenon causes significant increase in the spreading resistance. According to the Faraday's law, AC voltage is induced in a conductor which is subjected to a time-varying magnetic field. The induced voltage then forces eddy current to circulate in a closed path within the conductor. Following Lenz's law, the induced eddy current generates its own magnetic field to oppose the original magnetic field. The circulation of eddy current results in a nonuniform current density distribution (current crowding) and an increased conduction power loss. The power loss due to eddy current, P_{loss}^{eddy} , is proportional to the square of frequency [84], as

in

$$P_{loss}^{eddy} \propto f^2. \quad (2.40)$$

The eddy current results in two effects, i.e. the skin and proximity effects. Skin effect occurs when eddy current is induced in a conductor (e.g., buffer mesa), which is subjected to a time-varying magnetic field originating from the current flowing in the conductor itself. On the contrary, proximity effect occurs when the eddy current is induced in a conductor due to a time-varying magnetic field originating from an adjacent conductor, e.g., the generation of eddy current in the buffer mesa due to a time-varying magnetic field originated from the air-bridge finger. The frequency dependency of the power loss due to skin effect is

$$P_{loss}^{skin} \propto \sqrt{f}. \quad (2.41)$$

A general mathematical expression to represent the high frequency proximity loss, P_{loss}^{prox} , is rather complex [84]. In [88](Paper [B]), an EM analysis of a planar diode showed that the high frequency loss can be related to the onset of a mixture of skin and proximity effect, modelled as

$$P_{loss}^{skin+prox} \propto f^4. \quad (2.42)$$

In addition to the current crowding phenomena, high frequency spreading resistance is also affected by the semiconductor carrier inertia and displacement current phenomena, which have been discussed in Section 2.1.5.

2.2.2.2 Parasitic reactances

The parasitic capacitances and inductances model the electric and magnetic coupling within the diode structure [35, 36, 53, 89]. In general, only the parasitics in the close proximity to the Schottky anode contact and the surface channel (see Fig. 2.10(a)) are considered in the modelling and optimisation work.

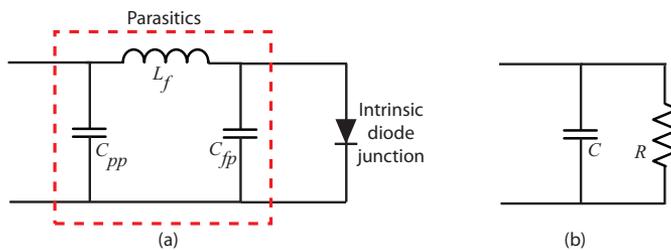


Fig. 2.10: (a) Diode equivalent circuit in a lossless case; (b) A simple RC load.

The diode pad-to-pad capacitance is described in (2.39). The electrical coupling between the air-bridge finger to the top of the mesa is modelled as a finger-to-pad capacitance, C_{fp} . Generally, the total parasitic capacitance, C_p^{total} , of a planar diode is calculated as a sum of all the parasitic capacitance components

$$C_p^{total} = C_{pp} + C_{fp}. \quad (2.43)$$

The self-inductance current in the air-bridge finger can be modelled as an air-bridge finger inductor, L_f . For anti-parallel diodes, the magnetic coupling between both air-bridge fingers are modelled as mutual inductors [37].

Referring to Fig. 2.10(a), the parasitic capacitances are placed in parallel to and the parasitic inductance in series with the diode intrinsic junction. At high frequencies, the parasitic capacitances resemble low impedance paths between the diode junction terminals, whereas the parasitic inductance resembles a high impedance path in series with the diode junction. As a result, the power coupling capability to the diode intrinsic junction becomes difficult for a wide frequency band. Thus, there is an inherent limitation of the bandwidth for power coupling to such a complex diode load.

For a simple RC load (see Fig. 2.10(b)), Bode has shown that the fundamental bandwidth limitation for power coupling can be calculated using

$$\int_0^\infty \ln \frac{1}{|\Gamma|} d\omega \leq \frac{\pi}{RC} \quad (2.44)$$

where Γ is the reflection coefficient of a given load, R [90]. The fundamental bandwidth limitation theory is then extended by Fano to include a more general equivalent circuit [91]. However, for a complex load with more than two lossless elements, the derivation of Bode-Fano equation becomes mathematically complicated. For planar Schottky diode, a total of three lossless parasitic elements have to be considered in the power coupling bandwidth limitation analysis. This complicated mathematic derivation has been solved by Hesler [92].

2.3 Diode design and optimisation

The performance of mixer and multiplier circuits depends greatly on the diode device properties. Therefore, it is crucial to identify the figures of merits and possible diode parameters to be optimised. A general understanding of trade-offs between the diode parameters and the corresponding effects on the performance is essential in designing a high performance diode.

2.3.1 Mixer diode

The efficiency of a resistive mixer is characterised by the conversion loss, L_M , defined as

$$L_M = \frac{P_{RF,av}}{P_{IF,av}}, \quad (2.45)$$

where $P_{RF,av}$ and $P_{IF,av}$ are the available input power at RF frequency and output power at IF frequency, respectively.

In an ideal case, the theoretical conversion loss is 3.9 dB for a mixer terminated with similar load for other mixing frequencies [93–95]. However, in practice, the conversion performance is degraded by the parasitic series resistance, non-ideal impedance matching and losses in the matching circuit.

Another figure of merit for the mixer circuit is the receiver noise temperature, T_R . The receiver noise temperature is related directly to the diode mixer

noise temperature, T_M . Moreover, the receiver noise temperature is degraded by an increase of the diode conversion loss as shown in (2.46). Thus, it is important to reduce the mixer conversion loss.

$$T_R = T_M + L_M T_{LNA} \quad (2.46)$$

The diode cut-off frequency, f_c , is a figure of merit in describing the upper limit of the diode frequency response. It is related to the parasitic series resistance, R_S , and total capacitance, C_{tot} .

$$f_c = \frac{1}{2\pi R_S C_{tot}}, \quad (2.47)$$

where

$$C_{tot} = C_{j0} + C_p^{total}, \quad (2.48)$$

with C_{j0} and C_p^{total} defined as (2.11) and (2.43), respectively. The diode cut-off frequency is usually calculated from DC or low-frequency measurements of the diode's characteristic. As a rule of thumb for a mixer diode design, the mixer cut-off frequency should be at least 10 times higher than the operating frequency [70].

Due to a trade-off between the junction capacitance and series resistance, the choice of Schottky anode area for a maximum cut-off frequency is difficult. In general, the capacitance range is chosen by considering limitations in the matching circuits.

Besides adjusting the anode contact size, minimisation of the series resistance can also be accomplished by increasing the epi-layer doping concentration. However, a higher doping concentration in the epi-layer results in a higher tunnelling current, i.e., an increase in the diode ideality factor. The relationship between ideality factor and the doping concentration is stated in (2.4). For a typical mixer diode design, the ideality factor of 1.2 or lower is desired. A high ideality factor increases the conversion loss. Finally, the epi-layer thickness is calculated as the zero-biased depletion width for a desired doping concentration, using (2.13).

2.3.2 Multiplier diode

In frequency multiplication applications, the diode can be used as either a varistor (resistive) multiplier [68, 96] or a varactor (reactance) multiplier [68, 69]. The conversion efficiency of a multiplier circuit is

$$\eta_{eff} = \frac{P_{nRF,av}}{P_{RF,av}}, \quad (2.49)$$

where $P_{RF,av}$ and $P_{nRF,av}$ are the available input power and output power at the n^{th} harmonic, respectively.

For an n^{th} order varistor multiplier, the best achievable conversion efficiency is $1/n^2$ [96]. On the contrary, according to the Manley-Rowe equations [97], an ideal varactor multiplier is capable of achieving a 100% conversion efficiency. However, the achievable operation bandwidth of a varactor multiplier is typically narrower than that of a resistive multiplier. Thus, there

is a trade-off between conversion efficiency and bandwidth between these two types of multiplier diodes.

In reality, the varactor multiplier performance is still far below the theoretical limits. The conversion performance degradation of a varactor multiplier is caused by the series resistance, non-ideal impedance matching and losses in the matching circuit. In addition, it is also attributed to the onset of resistive multiplication, when the diode is forward-biased for a fraction of the operation cycle. Thus, the varactor multiplier performance is further degraded by the losses in resistive multiplication during the forward-biased fraction of the operation cycle.

Another figure-of-merit for a pure varactor multiplier is the dynamic cut-off frequency, f_{cd} ,

$$f_{cd} = \frac{1}{2\pi R_S} (S_{max} - S_{min}) = \frac{1}{2\pi R_S} \left(\frac{1}{C_{j,min}} - \frac{1}{C_{j,max}} \right), \quad (2.50)$$

where S_{max} and S_{min} are the maximum and minimum elastance, respectively.

Contrary to the mixer diode, the capacitance swing from C_{min} to C_{max} instead of the total capacitance is taken into consideration for the cut-off frequency estimation. The possible capacitance swing region is limited by the junction breakdown, punch-through or current saturation phenomena.

For a breakdown voltage limited case, the minimum capacitance is limited by the doping concentration dependent breakdown voltage, defined as (2.8). The maximum depletion width prior to junction breakdown is

$$w_{d,bd} = \sqrt{\frac{2\varepsilon_{s,epi}}{qN_{d,epi}} (\psi_{bi} + V_{bd})}. \quad (2.51)$$

For a punch-through limited case, the thickness of the epi-layer is designed to be less than $w_{d,bd}$ for the corresponding doping concentration. Thus, the punch through condition is reached prior to breakdown. In a current saturation limited case, the capacitance swing is limited by the incapability of conduction current to match the displacement current.

Chapter 3

Planar diode electrical and thermal characterisation

Device characterisation is an important tool for diode evaluation, monitoring of the fabrication process and for developing models for circuit design. This chapter presents a review of electrical and thermal characterisation methods for THz planar Schottky diodes. The diode electrical characterisation methods and their corresponding parameter extraction methods are first presented. A brief review of the thermal characterisation methods then follows.

3.1 Electrical characterisation methods

The diode electrical characterisation includes DC and impedance measurements. For DC characterisation, the DC I - V method is a basic characterisation step to check the fundamental diode response. The DC measurement are used to model the diode DC non-linear behaviour, as well as finding the safe operating region for further characterisation using other methods. For impedance measurements, several methods are available [98]. Commonly used impedance measurement method for planar Schottky diode characterisation are the auto balancing bridge and vector network analysis methods. De-embedding or compensation are also performed during characterisation to reduce the effect of errors due to test fixtures, connection configurations etc [99].

3.1.1 DC characterisation methods

For DC I - V measurement, a voltage difference is applied across the diode terminals and the terminal current is measured, or vice versa. The diode DC non-linear (intrinsic) behaviour is described in (2.2). Common parameters extracted from this characterisation method are the η , R_S and I_S . In some cases, the barrier height, ϕ_b , can be extracted if the anode contact area is known. To-date, there is a substantial literature on DC I - V parameter extraction methods [100–105].

Generally, diode DC parameter extractions are performed using the forward-biased I - V data, when (2.2) can be simplified to the (2.6). The highly forward-

biased I - V region is favoured for extraction since the series resistance effect is more observable. A typical extraction method is a direct calculation of the diode parameters from the slope of forward-biased I - V characteristic, when it is presented in a logarithm current versus voltage scale, and the interception of the slope to the logarithm current axis (see Fig. 3.1(b)). The extracted parameters can be further fine-tuned using a least square fit method [105].

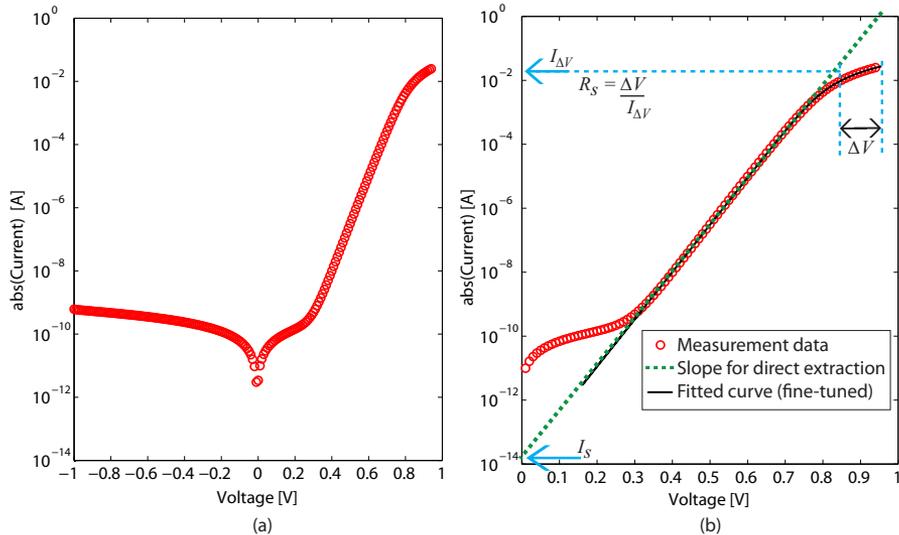


Fig. 3.1: (a) Measured I - V characteristic; (b) Parameter extraction via direct extraction and least square error fit method.

In the conventional I - V measurement, a bias voltage (or current) is applied constantly during the measurement. This measurement method is known as a static I - V measurement. However, Schottky diodes are temperature sensitive devices and their I - V characteristic are influenced by self-heating [106, 107]. The amount of heating is dependent of the diode thermal resistance, R_{th} , and the junction current density. The self-heating increases as the current increases. As a consequence of self-heating, the extracted series resistance is underestimated [70, 108].

In order to isolate the self-heating effect, a pulsed I - V measurement can be used. For the pulsed I - V measurement, the diode is subjected to a pulsed voltage (or current). The pulse width can be configured to be less than the diode junction thermal time-constant, τ_{th} . For a planar Schottky diode, the thermal time-constant at the junction is estimated to be in sub-microsecond range [109].

In addition to the self-heating problem, accuracy of the extracted series resistance is also affected by extra resistance from the measurement setup, e.g., probe contact resistance and cable resistance. In a conventional I - V measurement, a two-point probe technique is used. For a low level resistance measurement, i.e., when the diode resistance level is comparable to or lower than the setup resistance, the error in measurement result becomes significant. Thus, a four-point probe (Kelvin probe) DC I - V measurement technique is

recommended. Alternatively, the extra resistance can also be calibrated away manually, e.g., via estimating the extra resistance by probing both probes on a high conductivity contact pad.

3.1.2 Impedance characterisation methods

For impedance characterisation, two quantities are measured, which are the real and imaginary part of the impedance. The characterisation result depends on the measurement settings, such as test signal frequency and signal level, as well as the DC bias. Similar to the DC I - V case, the diode characteristic is affected by the self-heating, and this can also be isolated by using a pulsed I - V method. However, the setup for impedance characterisation using pulsed bias can be laborious [108, 110].

3.1.2.1 Auto balancing bridge

The auto balancing bridge (or LCR meter) method is capable of measuring a wide impedance range, i.e., from milliohm to hundreds of megaohms. However, this method is only accurate for measurement up to hundreds of megahertz range. For Schottky diodes, this method is typically used to characterise the diode C - V behaviour. An open/short compensation procedure is performed prior to the measurement to correct for extra parasitics from the test fixtures.

The diode voltage-dependent capacitance is acquired by converting the measured impedance vector to a parallel capacitance and admittance (C_p - G_p) equivalent circuit (see Fig. 3.2(a)) for a certain DC bias voltage range. Since the diode is a non-linear device, the AC test signal level has to be chosen carefully. The test signal has to be small enough in order for the C_p - G_p equivalent circuit to be valid at a DC bias point and large enough to surpass the measurement noise level.

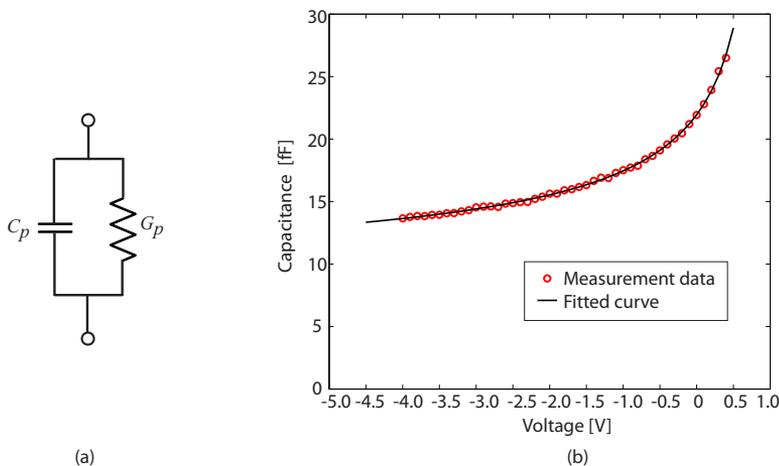


Fig. 3.2: (a) A C_p - G_p model; (b) Parameter extraction by curve-fitting method.

The measured capacitance is a sum of the intrinsic voltage-dependent junc-

tion capacitance, $C_j(V_j)$, (2.10) and the total parasitic capacitance, C_p^{total} (2.43), written as

$$C_{meas}^{total} = C_{j0} \sqrt{\frac{\psi_{bi}}{\psi_{bi} - V_j}} + C_{par}^{total}. \quad (3.1)$$

The C_{j0} , ψ_{bi} , and C_p^{total} parameters are extracted by fitting (3.1) to the measured capacitance [102, 111] (see Fig. 3.2(b)). The extraction of C_p^{total} is sensitive to the open/short compensation procedure performed prior to the diode characterisation [111]. Errors are introduced into the measurement result when the parasitic capacitance in the setup is either over- or under-estimated from the open/short compensation of the LCR meter.

3.1.2.2 Vector network analysis

For high frequency broadband characterisation (hundreds of kilohertz onwards), the vector network analysis (VNA) method is an accurate method to use. In this method, the impedance is characterised by measuring the incident, transmitted and reflected waves. Thus, this method is also known as a scattering-wave or S-parameter measurement. The limitation of this method is a narrower measurable impedance range compared to the auto balancing bridge method. This limitation is imposed by the characteristic impedance.

Planar Schottky diode S-parameters measurement have been performed in a co-planar waveguide (CPW) test environment. The discrete diodes are either flip-chip mounted [102, 111–113] or wire-bonded [114] to the CPW test mount. In [113], the flip-chip mounted diodes are characterised up to 125 GHz. Monolithically integrated Schottky diodes have also been characterised up to 110 GHz ([111] and Paper [A]). Fig. 3.3(a) shows an example of the planar diode integrated with a 50Ω CPW transmission line and close views of several diode structures.

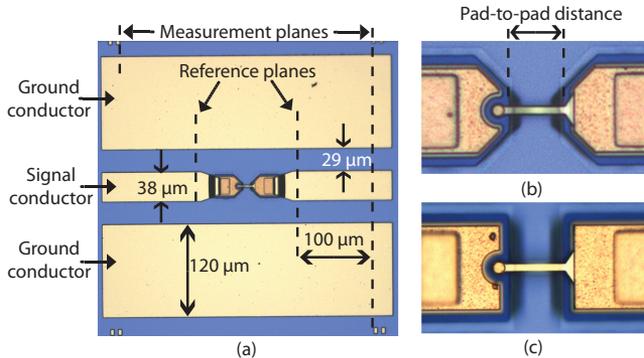


Fig. 3.3: (a) Planar Schottky diodes in a CPW configuration; (b) Tapered pad diode; (c) Rectangular pad diode.

During characterisation, the diode is DC biased and S-parameters are measured with a low level RF test signal, e.g. -27 dBm, for a specific frequency range. With a low level test signal, the measured impedance can be approximated to be linear under the corresponding DC bias. Therefore, the model

extracted from this measurement is known as a small signal model. Fig. 3.4 shows a small signal model for a planar diode, presented as an equivalent circuit. A non-linear model can be developed from a set of multi-biased S-parameters [113] and verified using large signal analysis [115].

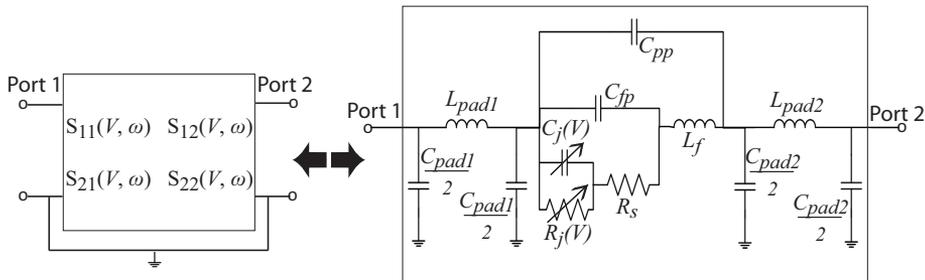


Fig. 3.4: Extraction of the diode equivalent circuit model parameters from S-parameters.

Several methods have been used to extract the planar diode equivalent circuit parameters from the S-parameters, e.g.,

- fitting the S-parameters generated by the model to those measured or 3-D EM calculated (optimisation method) [89, 111, 112, 116, 117]
- similar as the above method, but the matching procedure is guided by direct extracted values followed by parameter fine-tuning iterations (Paper [B])
- analytical calculation (Paper [A])

The parameter extraction method used in [89, 111, 112, 116, 117] is based on a minimisation of a global error function over a frequency band of interest in an iterative manner. Thus, the extraction result is sensitive to the definition of the global error function, as well as the initial values and the range of parameter values. This method is modified in Paper [B] by guiding the parameter fitting with a series of guided fine-tuning procedures. However, this method is time consuming and still subject to convergence issues in certain cases. A more efficient method is then proposed in Paper [A], where the circuit parameters are calculated analytically.

Fig. 3.5 shows an example of the measured S-parameters and those from the extracted model (using the analytical method) for several bias points. For the forward-biased cases, the models agree well with the measurement data throughout the measured frequency range. For the reverse-biased cases, the models start to deviate from the measurement data beyond 30 GHz. This is due to energy loss in parasitic propagation modes [118, 119].

The geometry-dependent total parasitic capacitances, C_{par}^{total} , extracted from S-parameter measurements are compared to those extracted from auto-balancing bridge method in Fig. 3.6. The C_{par}^{total} extracted from both methods agree with each other, with a relatively small offset.

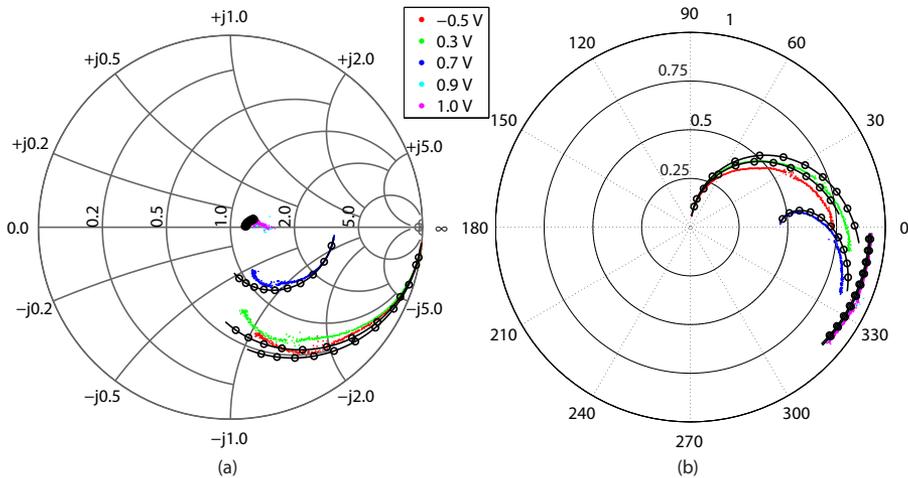


Fig. 3.5: Multi-biased S-parameters from 5 to 110 GHz for a diode with tapered shape pad and a mesa gap of $10\ \mu\text{m}$: (a) S_{11} ; (b) S_{21} . Markers are the measurement data; Solid lines are the corresponding extracted model responses; Circles on the solid lines indicate frequency points from 10 to 100 GHz at a 10 GHz step.

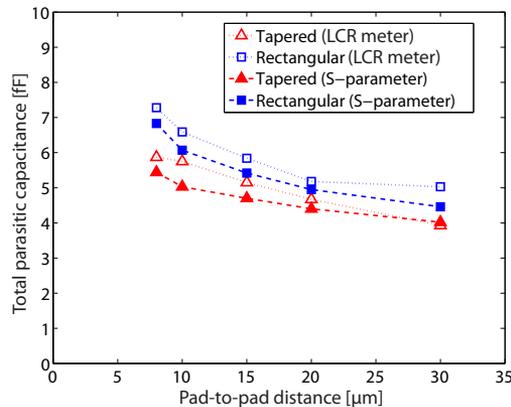


Fig. 3.6: Geometry-dependent diode model capacitances.

In addition to proposing an analytical parameter extraction method, Paper [A] also showed that for a proper parameter extraction of the finger inductance in the model, a frequency higher than 110 GHz is needed. However, for higher frequencies, a design of a proper CPW test fixture is challenging due to the excitation of parasitic propagation modes [118–120]. On wafer measurement at such high frequencies is extremely challenging but not impossible. For InP HEMT transistors, on-wafer S-parameter characterisation has been performed up to 500 GHz using WR-2.2 (325–508 GHz) waveguide wafer probe [121].

In the past, some effort has been devoted to characterise planar diodes using scaled models [37, 122]. In a scaled model approach, the physical device

geometry is scaled up by a factor n and the measurement frequency is scaled down by a factor of $1/n$. However, the linear frequency scalability is only valid for the lossless elements, i.e., inductance and capacitance, but not for the conductive losses. In addition, the ratio between the largest and smallest important features in the planar diode geometry is large, e.g. >100 for a sub-micron size of anode contact and a tens of μm size of contact pads. Thus, this measurement method has not been widely used.

Another possible solution for S-parameter measurements at higher frequencies is to characterise diodes in a waveguide environment. The waveguide-based S-parameter measurement technique has been developed and demonstrated for passive circuit characterisation in WR-3 band (220-325 GHz) [123, 124]. This technique can also be used to characterise THz planar Schottky diodes up to 325 GHz or higher. For higher frequency characterisation, it is foreseen that the parameter extraction is becoming more challenging, and more sophisticated extraction methods are needed.

Alternatively, the high frequency diode behaviour can be modelled using a numerical electromagnetic calculation approach. Advancements in the computer aided design and analysis tools allow accurate high frequency device modelling via 3-D full-wave EM simulations (refer to Chapter 4).

3.2 Thermal characterisation methods

For THz planar Schottky diodes, the self-heating effect on the diode performance is significant. However, literature related to the Schottky diodes thermal characterisation work is limited. In general, the available methods for thermal characterisation of electronic components are the pulsed measurement [125], imaging [126–128] and electrical junction measurement [129] methods. Thermal characterisation methods used for planar Schottky diodes include the infrared (IR) thermal imaging ([79] and Paper [D]) and the electrical junction temperature measurement [109] methods.

3.2.1 IR thermal imaging

The IR thermal imaging method is a non-contacting thermal characterisation based on the emission of thermal radiation. The IR thermal imaging method has been used to characterise the steady-state thermal behaviour of THz Schottky diode based multipliers ([79] and Paper [D]). In addition to the steady-state thermal characterisation, the transient thermal behaviour of the multiplier is also measured in Paper [D]. In these measurements, the multiplier chip is mounted on a half waveguide split block (see Fig. 3.7). The steady-state and transient thermal imaging result are presented in Fig. 3.8.

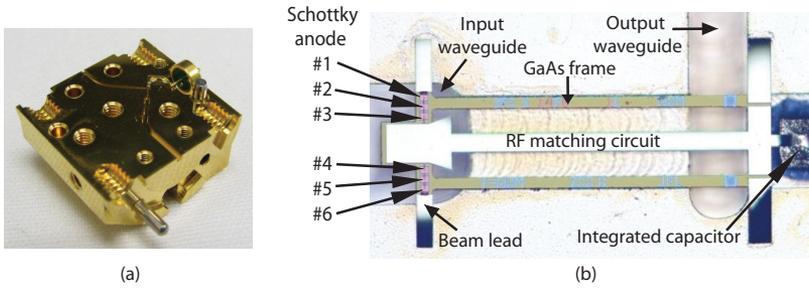


Fig. 3.7: (a) Waveguide split block; (b) Top view of the multiplier chip.

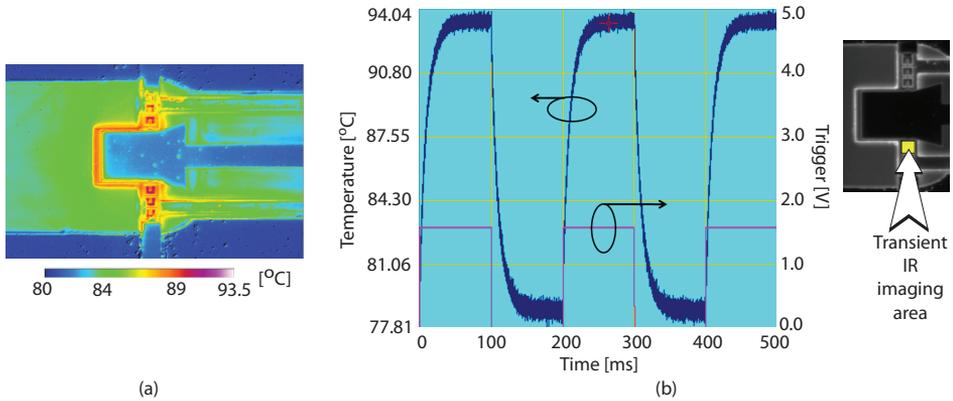


Fig. 3.8: (a) Steady-state IR thermal image; (b) Transient temperature behaviour and the imaging area during transient characterisation.

3.2.2 Electrical junction temperature measurement

With the electrical junction temperature measurement method, the device temperature can be deduced from the temperature-dependent I - V relation. This method has been used to characterise planar Schottky diodes [109]. The characterisation procedure is similar to that of MIL-STD-750E thermal impedance testing of diodes [130] standard. However, in [109], the temperature sensitive parameter is the forward-current, instead of the forward-voltage. In addition, a voltage pulse, instead of a current pulse, is used to heat up the diode junction.

Chapter 4

Planar diode electromagnetic and thermal modelling

This chapter discusses the THz planar Schottky diode modelling work. The motivation and a brief review of the work on modelling planar diodes, together with results in Paper [B]-[E], are presented.

4.1 Overview of planar diode modelling work

Presently, planar Schottky diode mixers and multipliers are used for operation up to ~ 3 THz. A typical circuit design approach is to analyse the circuit performance using a combination of the diode intrinsic and extrinsic models. The conventional diode intrinsic model is usually described analytically using the diode quasi-static I - V and C - V relation, as in (2.2) and (2.10), respectively. In this model, a series resistance is also included. The extrinsic models are calculated via a 3-D full-wave EM approach, where the conductors are usually assumed to be lossless or with a finite surface conductivity during the calculation.

At high frequencies, the diode experimental performance is normally inferior to the predicted results. At certain occasions, the series resistance has to be scaled empirically to a much higher value in order to match the diode conversion loss in the experimental results [131]. This is partly due to the lack of proper diode models in describing the diode behaviour, such as high frequency carrier transport behaviour, high frequency losses, parasitic coupling, and thermal effects, in the THz region. Thus, there is a strong need to develop accurate high frequency models, either to minimise the costly device development iterations or to optimise the device performance.

In general, optimising the diode high frequency performance can be divided into two areas, i.e., maintaining a reasonable non-linear electrical property in the junction (intrinsic) and maximising the input power coupling to the junction (extrinsic). The latter area includes minimising the parasitic resistances

and reactances, as well as the self-heating effect. Fig. 4.1 shows an illustration of the areas of the modelling work.

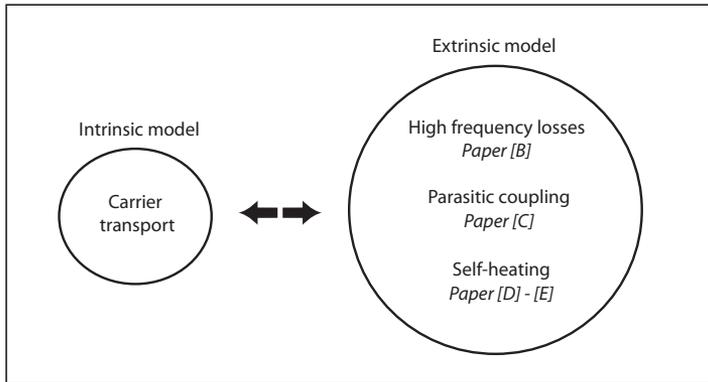


Fig. 4.1: Overview of the modelling work.

• Intrinsic model

Due to the macroscopic nature of the conventional analytic intrinsic model, it is not adequate to describe the carrier transport phenomena in the high frequency and high field region. Thus, device physics-based numerical models, which are based on the Boltzmann's transport equation or its approximations, are needed. Examples of these models are drift diffusion and hydrodynamic models [132, 133].

For Schottky diodes, these models have been used to perform studies of phenomena such as high frequency noise [134], hot electron [72, 135], current saturation [40, 136] and degenerately-doped diodes [137]. Inherently, these models provide a clearer insight into the device physics. Moreover, these models can also be coupled to the circuit simulator for device-circuit co-analysis [138–140]. However, due to the microscopic numerical approach, physics-based numerical models are slow and require high computational power. Therefore, physics-based numerical models are not ideal to be used during the circuit design phase.

• Extrinsic model

During circuit design, the 3-D EM response of diode structures can be simulated. However, the simulated result, i.e., S-parameters, are usually treated as a black box and the diode geometry-dependent parasitic couplings are not analysed explicitly. In addition, during circuit design, the conductors are usually assumed to be perfect electric conductor (PEC) or with a certain surface impedance. In other words, the EM fields are not solved inside the conductors in these simulations. This is because solving the EM fields inside conductors is a rather computational power consuming process. Thus, the diode extrinsic properties in relation to the high frequency losses, parasitics coupling and thermal behaviour have not been investigated systematically for diode optimisation.

The high frequency losses are related to the carrier inertia, dielectric effect and current crowding effects. Several efforts have been devoted to develop the high frequency series impedance model [38, 81, 82]. However, for all these models, the electromagnetic coupling between the diode physical structures, such as air-bridge finger and buffer mesa, are not taken into account. Paper [B] presents a high frequency loss model which shows a strong frequency-dependent loss due to the electromagnetic coupling between the diode air-bridge finger and the buffer mesa. The losses are due to the onset of eddy current and a mixture of skin and proximity effects, beyond 200 GHz and 400 GHz, respectively. This is further discussed in Chapter 4.2.1.

In addition to high frequency loss, the diode lossless parasitics also impose a limitation on the wide bandwidth coupling capability to the intrinsic diode junction. However, little work has been done in this area. In order to analyse this matter, a power coupling bandwidth analysis based on the Bode-Fano criterion [90, 91] has been proposed by Hesler [92]. In Paper [C], this analysis method is used to study the effect of diode geometry-dependent parasitics on the coupling bandwidth in a systematic way. This is further discussed in Chapter 4.2.2.

There is a significant trade-off between the diode electrical and thermal properties. For high power applications, the need for a diode thermal model is becoming increasingly important. However, compared to transistors [141–147], HBV [148–150] and Gunn diodes [151–153], literature for the planar Schottky diode thermal modelling work is limited. Thus far, the thermal modelling work is devoted to the Schottky varactor diode analysis due to the high power requirement for frequency multipliers [51, 154, 155].

For the developed multiplier thermal models, only the steady-state thermal behaviour is analysed. Furthermore, the diode junction power dissipation and the junction temperatures are not coupled self-consistently between the electrical and thermal models. Paper [D] presents a thermal model which is capable of analysing both the multiplier steady-state and transient thermal behaviours, including the GaAs temperature-dependent thermal properties. Paper [E] further proposed a self-consistent electrothermal model, which provides circuit designers an important tool for electro-thermal co-analysis. This is further discussed in Chapter 4.3. Although the models are developed for multipliers, they can also be used for analysing the self-heating effect in mixer diodes due to high current density in the small anode area.

4.2 Electromagnetic model

A common approach in analysing the parasitic coupling is by performing the full-wave EM analysis, which is a method to analyse the EM wave propagation via solving the Maxwell's equations. This analysis is usually performed using a finite difference (FD) or a finite element method (FEM). The simulated response is used to develop an equivalent circuit, which is suitable for circuit analysis and important for diode geometry optimisation. For planar Schottky diodes, the EM field interaction within the diode structure is modelled via a lumped-equivalent circuit (see Fig. 2.8 and Fig. 2.9). The equivalent circuit is extracted using the parameter extraction method which has been discussed

in Chapter 3.1.2.2. Detailed descriptions and guidelines for the EM analysis using FEM method are presented in Paper [B].

4.2.1 High frequency losses

Several efforts have been reported to model the influence of skin effect on the series impedance which causes increased high frequency loss. For a point-contact diode, Dickens has introduced a frequency-dependent spreading resistance [81]. The spreading resistance model is extended by Champlin and Eisenstein [38] to include the electron inertia and dielectric effects. Bhapkar et. al [82] then investigated the series impedance including a moderately doped junction epi-layer, a highly doped buffer layer and a non-ideal ohmic contact. In their work, Maxwell's equations are solved in a 2-D lattice using the FD method. For planar Schottky diodes, a series impedance model up to 500 GHz has been developed by Bhaumik et. al [156]. Due to the planar structure, an analytical approach for planar diode modelling is difficult. Thus, a numerical approach is usually used.

Nevertheless, all of these series impedance models do not take into consideration the EM field coupling within the diode structure. In order to investigate this matter, Paper [B] presents a 3-D full-wave EM analysis of a planar diode using FEM, where the EM field inside the buffer mesa is solved. A cross-sectional view of the magnetic field plot and the corresponding current density vectors are illustrated in Fig. 4.2(a). Due to the high frequency time-varying magnetic field, eddy currents are induced inside the buffer mesa as described by Faraday's law, which further result in current crowding effects, i.e., skin and proximity effects.

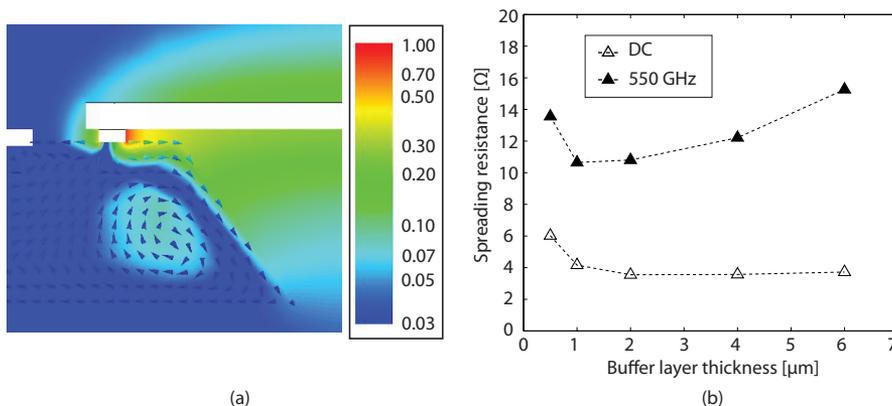


Fig. 4.2: (a) Normalised magnetic field and current density vectors for a 6 μm thick buffer-layer at 550 GHz (Paper [B]); (b) A comparison of the spreading resistance at DC and 550 GHz.

Therefore, in addition to the skin effect, the eddy current and proximity effects play a significant role in the strong frequency-dependent loss in planar diodes. Paper [B] also shows that the onset of high frequency loss due to eddy current and a mixture of skin and proximity effect occurs at approximately

200 and 400 GHz, respectively. Fig. 4.2(b) shows the spreading resistance as a function of the buffer layer thickness. At DC, a thicker buffer layer is preferred for a lower spreading resistance. However, at high frequencies, the spreading resistance increases beyond a certain critical buffer layer thickness due to the onset of eddy current and current crowding effects. The critical thickness is approximately one skin depth at the operating frequency.

4.2.2 Power coupling bandwidth

Diode lossless parasitics, i.e. parasitic capacitances and inductances, limit the bandwidth of power coupling into the diode intrinsic junction. For operating frequencies beyond 1 THz, the effect of diode parasitic reactances on the power coupling become significant [92]. Thus, it is important to understand the geometry-dependent parasitics in order to optimise the diode geometry for wide band power coupling.

Several diode geometry optimisation parameters are: the pad-to-pad distance, pad shape and substrate thickness. These geometry parameter influences the parasitics in the planar diode equivalent circuit (see Fig. 2.10), i.e., C_{pp} , C_{fp} and L_f . Fig. 4.3 shows an example plot of the pad-to-pad capacitance and finger inductance as a function of the pad-to-pad distance.

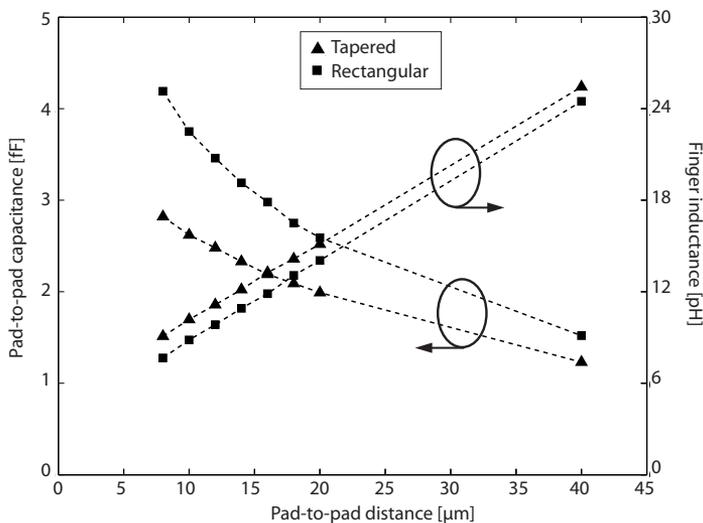


Fig. 4.3: A plot of the pad-to-pad capacitance and finger inductance as a function of the pad-to-pad distance for diodes with tapered and rectangular shapes.

Theory of the fundamental power coupling bandwidth limitation for a simple RC load has been developed by Bode [90] and further extended by Fano [91]. The Bode-Fano theory has been used by Kerr to study some fundamental and practical limits on SIS mixer design [157]. The low pass matching case in Fano's theory has been modified by Kerr for bandpass matching analysis, without a lowpass to bandpass transformation. A combination of Bode-Fano's theory and Kerr's modification for bandpass matching analysis

is then used by Hesler to analyse the power coupling bandwidth limitation of planar Schottky diodes [92].

Thus far, optimisation of the planar diode geometry by maximising the power coupling bandwidth has not been widely investigated. In Paper [C], a similar analysis method as in [92] is implemented to optimise the diode geometry in terms of power coupling bandwidth for anti-parallel diode structures. The challenges in this work also lies in the capability in extracting and proving the validity of the diode equivalent circuit in the THz range. The result shows an inherent trade-off between the pad-to-pad capacitance and finger inductance when optimising the pad-to-pad distance.

4.3 Thermal model

For planar Schottky diodes, the heat conduction is usually assumed to be the dominant heat transport mechanism, and thus other mechanisms, such as radiation and convection, are assumed to be negligible. With this assumption, the thermal problem is analysed by solving the heat equation (2.22) for a certain geometry, with proper boundary conditions. The problem can be solved either analytically, or by using FD or FEM methods. Example of the setup can be found in Paper [D].

4.3.1 Thermal analysis

For thermal analysis, a 3-D finite element heat flow analysis on a planar multiplier chip is performed by Jones [154]. Porterfield then presented an analytical 2-D thermal model for a multi-anode multiplier chip [155]. The multiplier is flip-chip mounted on a quartz substrate, which was wire-bonded to a waveguide housing. However, these two models do not take into consideration the GaAs temperature-dependent thermal conductivity. A 3-D thermal analysis using a FD method, taking into consideration the temperature-dependent thermal conductivity, is developed by Schlecht et. al [51] for a multi-anode substrateless multiplier chip. Nevertheless, only the steady-state thermal characteristics are analysed in all these models.

In Paper [D], a 3-D thermal model with the capability of analysing both the steady-state and transient thermal characteristics of a multi-anode multiplier chip is developed using FEM. The model is used to perform a systematic thermal analysis on a multi-anode substrateless multiplier chip (see Fig. 4.4). The hot spots and thermal constraints in the substrateless multiplier chip are identified and the power handling capability of the multiplier chip is studied.

Fig. 4.5 shows an example of the steady-state temperature distribution within the multiplier chip and the anode junction temperatures. At high power dissipation levels, the temperatures differ between the anodes. The hot spot is observed in the 3rd anode, which is the anode located nearest to the chip centre. It is also observed that the junction temperature response is nonlinear as a function of power.

For transient thermal analysis, the thermal time constant, τ_{th} , is of interest. In the region close to the anode junction, the transient thermal characteristic shows several thermal time constants. This is due to the distributed thermal mass and the thermal coupling between adjacent anodes. The overall thermal

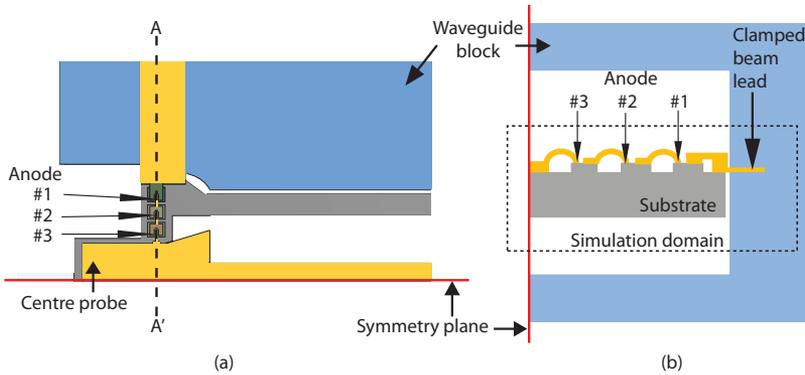


Fig. 4.4: Schematic of a 6-anode substrateless multiplier chip: (a) top view; (b) A-A' cross-section view. Only half of the multiplier chip is analysed due to its symmetrical geometry.

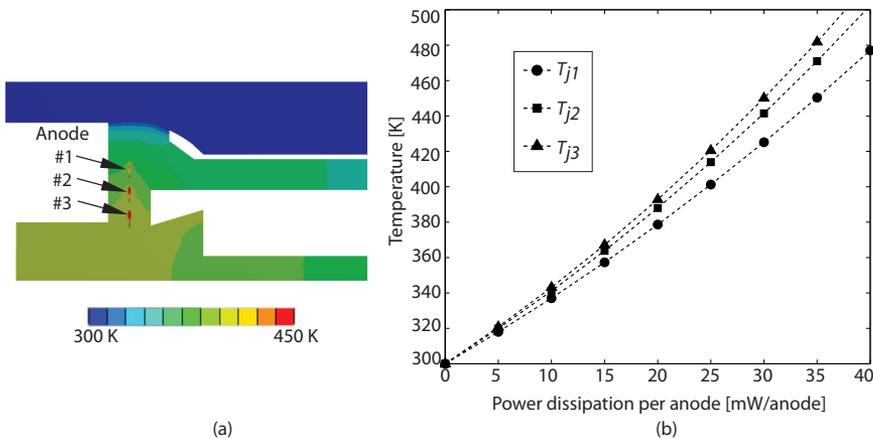


Fig. 4.5: (a) Top view of the temperature distribution for a multiplier chip with $50 \mu\text{m}$ thick GaAs substrate at power dissipation level of 30 mW per anode; (b) A comparison of the junction temperatures as a function of power dissipation levels (Paper [D]).

settling time is more than 10 ms. Considering electrical RF operation in the GHz range, the thermal time constant is longer than the electrical RF cycles. Thus, the thermal transient characteristic can be ignored during the multiplier electrical analysis. However, for applications with time-constants comparable to or lower than the thermal time constant, the thermal transient characteristic has to be considered.

4.3.2 Self-consistent electrothermal coupling

For the thermal models developed so far [51,154,155], equal power dissipation is assumed for all the anodes in a multi-anode multiplier. However, Paper [D] shows that, in a multi-anode multiplier chip, the anode junction temperatures

differ from each other. For each anode, the junction temperature-sensitive electrical properties are locally modified as a function of the junction temperature. In addition, the electrical properties, e.g., series resistance, prior to self-heating effect are not equal for all the diodes. Thus, the equal-power dissipation assumption within a multi-anode multiplier chip is in question.

For a proper electrothermal analysis, the instantaneous electrical power has to be coupled to the thermal model. Therefore, a self-consistent electrothermal model is proposed in Paper [E]. This model is an important tool for co-analysing the electrical and thermal properties of the multiplier. In addition, the model can be further extended to include the transient effect for applications with complex modulation schemes, such as those used in radar applications.

The self-consistent electrothermal model developed in Paper [E] is based on a thermal resistance matrix approach, by using a linear temperature approximation for the thermal resistance [145, 146]. The model is demonstrated using two 6-anode multipliers and verified experimentally. Due to the symmetrical geometry, a 3×3 thermal resistance matrix is adequate for modelling a 6-anode multiplier. Fig. 4.6 shows a schematic of the thermal model in the thermal resistance matrix representation, where the corresponding mathematical expression is written as

$$\begin{bmatrix} T_{j1} - T_{amb} \\ T_{j2} - T_{amb} \\ T_{j3} - T_{amb} \end{bmatrix} = \begin{bmatrix} R_{th11}(T_{j1}) & R_{th12}(T_{j1}) & R_{th13}(T_{j1}) \\ R_{th21}(T_{j2}) & R_{th22}(T_{j2}) & R_{th23}(T_{j2}) \\ R_{th31}(T_{j3}) & R_{th32}(T_{j3}) & R_{th33}(T_{j3}) \end{bmatrix} \begin{bmatrix} P_1^{dis} \\ P_2^{dis} \\ P_3^{dis} \end{bmatrix}. \quad (4.1)$$

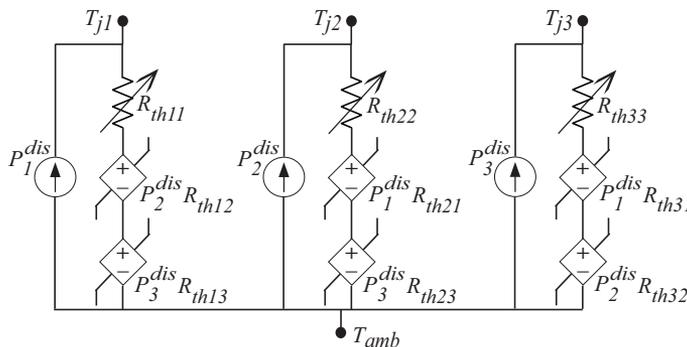


Fig. 4.6: Thermal resistance matrix representation of the multi-anode thermal model using a linear temperature approximation.

Compared to the model developed in [51], the diode temperatures in this self-consistent electrothermal model are calculated from the electrical instantaneous power and allows unequal power loading for the anodes. Furthermore, the information of the junction temperatures are accessible from the electrothermal model. A schematic of the electrothermal coupling is shown in Fig. 4.7.

The multiplier efficiency degradation can be caused by either current saturation or thermal effects, or a combination of both. The current saturation

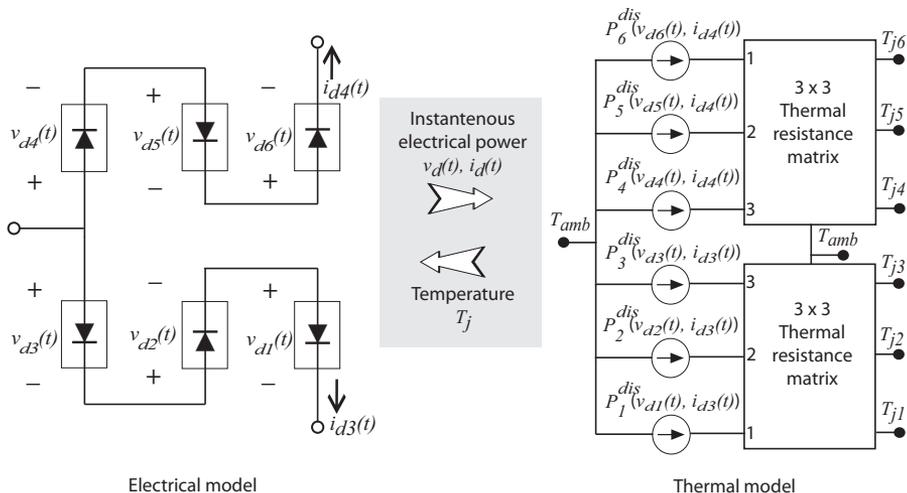


Fig. 4.7: Schematic of the self-consistent electrothermal model.

level of the multiplier can be estimated using (2.36). As in a conventional electrical simulation (without the electrothermal simulation), the electrothermal model is also capable of providing the current-voltage information. Thus, with the self-consistent electrothermal model in Paper [E], the multiplier performance can be identified as current saturation limited or thermal limited.

Inherently, the self-consistent electrothermal model is an important tool for analysis from both electrical and thermal perspectives. However, the procedure for thermal resistance extraction from the 3-D FEM simulations is slightly tedious. Thus, further work is required to improve this procedure towards developing a more efficient model for diode-circuit co-design.

Chapter 5

Conclusions and future outlook

The main objective of this research work is to study and optimise the planar Schottky diode operation in the THz regime. The work presented in this thesis includes the investigation of the high frequency power loss and power coupling phenomena, as well as thermal effects on the diode performance.

Today, submillimetre wave characterisation methods are being actively developed by several key players in the THz field. This includes the development of the waveguide embedded membrane circuit characterisation method in the WR-3 band (220-325 GHz) and the advent of on-wafer probes for WR-2.2 (325-508 GHz) and higher frequency bands. In addition, the computational numerical-based approach is also a common method for high frequency device parasitic analysis. However, for planar Schottky diodes, a high frequency broadband model parameter extraction method is still lacking. Thus, a systematic and analytical parameter extraction method has been proposed and verified experimentally up to 110 GHz (Paper [A]).

Regarding diode operation at THz frequencies, the diode parasitics have a significant impact on the diode performance due to high frequency losses and EM couplings. Conversion of the electromagnetic energy into heat results in power loss, which is known as ohmic loss. High frequency loss analysis performed in this work shows that the strong frequency dependent series resistance is attributed to the onset of eddy current, skin and proximity effects (Paper [B]). From a high frequency perspective, it is beneficial that the volume of the semiconductor in close proximity to the metal conductor is minimised, e.g., minimising the highly-doped buffer material underneath the air-bridge finger. In addition, the eddy current generation, skin and proximity effects have to be taken into account in optimising the distance between the metal conductors and semiconductor material.

The power coupling to the diode junction is limited by the geometry-dependent parasitic capacitance and inductance. In order to design a diode which can be matched easily, it is important to minimise the parasitics. Paper [C] shows that there is a significant trade-off between the diode pad-to-pad capacitance and finger inductance in optimising the diode geometry.

For high power applications, current frequency multiplier designs are lim-

ited by the relatively poor thermal properties of GaAs and the restricted heat conduction path to the heat sink. Several thermal optimisation solutions are explored and analysed in this work. These solutions includes attaching a heat spreader under the chip, improving the heat spreading at the regions of thermal constraint and designing high power multiplier based on material with better thermal conductivity (Paper [D]).

Albeit having the thermal optimisation options available, a quantitative estimation of the effect that the thermal solution has on the electrical performance is not straightforward. Thus, a self-consistent electrothermal model is developed, where the trade-offs between the electrical and thermal designs can be evaluated (Paper [E]). This model serves as an important tool in analysing the multiplier design, aimed at for instance increasing the multiplier output power. Moreover, this model can also be implemented to investigate the mixer chip thermal behaviour, as well as a tool for device reliability studies.

This work indicates the need for diode characterisation at higher frequencies for a proper parameter extraction of the finger inductance, where the impedance of the finger inductance is approximately $>15\%$ of the characteristic impedance. Today, accurate characterisations up to 1 THz and beyond is possible and it allows the characterisation of the complex high frequency device phenomena. This further leads to the need for a more robust parameter extraction method, where the diode equivalent circuit has to be expanded to include high frequency phenomena.

This work relates the eddy current and current crowding phenomena to the strong frequency dependent loss mechanisms in planar Schottky diodes. However, these loss mechanisms are not excluded to planar Schottky diodes. They should be also considered in all other high frequency semiconductor devices (such as transistors) with similar structures.

From a thermal perspective, improvement of the diode design in terms of material system and geometry is needed. Attributed to a better thermal conductivity and a higher breakdown field in wide bandgap materials, recent advancements in GaN device technologies, such as GaN-HEMTs, offer almost a tenfold increase in the available power in the millimetre wave region. With this, a higher pump power can be offered to reach a higher output power beyond 1 THz with the multiplier chain. This development will cause significant impact in the THz solid-state electronics field, by providing an enabling technology for the development of more powerful THz sources to be used in transmitters and receivers. With further research on thermal management and power combining concepts, this technological development can potentially close the THz gap. More efficient sources will also enable the realisation of more advanced circuit topology and functionality, such as receiver array concepts for THz imaging applications.

In short, a better understanding of the diode operation at submillimetre wave is acquired through the research work presented in this thesis. With this, further optimisation of diode performance, e.g., pushing limits of the diode conversion loss and output power, in the submillimetre wave region can hopefully be foreseen.

Chapter 6

Summary of appended papers

This chapter provides summary of the appended papers and outlines my contribution for each paper.

Paper A

Analytical Extraction of a Schottky Diode Model based on Broadband S-Parameters

This paper presents an analytical method to extract the parasitic elements for planar Schottky diode models. In particular, a new extraction algorithm for the diode finger inductance is proposed. This method is more reliable and straight-forward compared to the conventional extraction method, where the S-parameters are fitted to the model via minimisation of a global error function.

My contribution: Proposed the new method, designed and measured the on-wafer CPW TRL-calibration kit and diode structures, developed the diode 3-D EM models, analysed the data and wrote the paper.

Paper B

Impact of Eddy Currents and Crowding Effects on High Frequency Losses in Planar Schottky Diodes

This paper investigates the strong frequency-dependent loss in planar Schottky diodes, which is not explainable by loss due to the skin effect. For the first time in the THz planar Schottky diode literature, this paper relates the high frequency loss with the eddy currents and current crowding effects. With this finding, a high frequency loss model is proposed.

My contribution: Developed the 3-D EM diode models, extracted the diode equivalent circuit parameters, analysed the data, proposed the high frequency loss model and wrote the paper.

Paper C

Geometry Optimization of THz Sub-harmonic Schottky Mixer Diodes

This paper presents a fundamental limitation of the power coupling bandwidth for anti-parallel Schottky mixer diodes, due to the geometry-dependent parasitics. The Bode-Fano analysis is performed on simplified equivalent circuits of the sub-harmonic mixer diodes.

My contribution: Developed the 3-D EM diode models, extracted the diode equivalent circuit parameters, performed Bode-Fano analysis and wrote the paper.

Paper D

Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes

This paper presents a systematic thermal analysis of the Schottky diode based multiplier chips for high power applications. Thermal limitations due to the material properties and chip layouts are analysed. Several heat-sinking approaches and the corresponding limitations are discussed. This work is performed in collaboration with the Jet Propulsion Laboratory (JPL)/Caltech.

My contribution: Developed the 3-D thermal models, extracted the thermal model parameters, participated the IR thermal transient and steady-state characterisation, analysed the data and wrote the paper.

Paper E

Electro-Thermal Model for Multi-Anode Schottky Diode Multipliers

This paper proposes a self-consistent electro-thermal model, which enables co-optimisation of the thermal and electrical properties for high power multiplier design. The model is verified via measurement data from 200 GHz multipliers developed by the Jet Propulsion Laboratory (JPL)/Caltech.

My contribution: Proposed the self-consistent electro-thermal model, developed and extracted the thermal models, implemented the model for circuit analysis, analysed the data and wrote the paper.

Acknowledgment

First of all, I would like to express my gratitude to all those who have encouraged and given me support in my study and career. Special thanks to my examiner and main supervisor, Prof. Jan Stake, for giving me the opportunity to pursue my PhD degree in the Terahertz and Millimetre Wave Laboratory (TML) and for his guidance throughout this challenging journey. I would also like to thank my co-supervisors, Dr. Tomas Bryllert and Dr. Josip Vukusic, for the advices and helps.

I would like to express my gratitude to Dr. Tapani Närhi (ESA) for the discussions and feedbacks on my research work. Also, I am very thankful to Prof. Peter Siegel and Dr. Imran Mehdi in giving me the opportunity to work with the Submillimeter Wave Advanced Technology team (SWAT) in JPL/Caltech. I gratefully acknowledge the SWAT team for all the fruitful discussions and supports during my research visit. Many thanks to adjunct Prof. Klas Yhland and Dr. Jörgen Stenarson (SP Technical Research Institute of Sweden) for the guidance in the S-parameter characterisation related matters.

To all the members of TML, thank you for the support and friendship. Thanks to Prof. emeritus Erik Kollberg for the feedbacks to my papers and thesis, Vladimir Drakinskiy for the diode fabrications, Robin Dahlbäck for managing heavy simulations in the server, and Catharina Forssén for all the administrative support. I would like to express my deepest gratitude for the hospitalities from my friends/colleagues during my stay in Sweden, especially Kristina Svensson family, Katarina Sobis family, Aleksandra Malko and Stella Bevilacqua. Also, thanks to Hillary Hunter and friends in California for all the enjoyable moments during my research stay in California. To my beloved family and friends, thank you for keeping me strong in facing every challenge in my life even though I am far away from home.

Last but not least, I would like to acknowledge the funding agencies and collaboration partners. The research work receives funding from the European Community's Seventh Framework Programme ([FP7/2007-2013]) and the European Space Agency. This research is also partially carried out in the Giga-Hertz Centre in a joint research project financed by the Swedish Governmental Agency of Innovation Systems (VINNOVA), Chalmers University of Technology, Omnisys Instruments AB, Wasa Millimeter Wave AB, Low Noise Factory and SP Technical Research Institute of Sweden. Part of the research result presented in this thesis also received financial support from VINNOVA, Security Link, Ericsson's Research Foundation, Solveig och Karl G Eliassons Minnesfond, and Chalmersska Forskningsfonden 2010.

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Paper A

Analytical Extraction of a Schottky Diode Model based on Broadband S-Parameters

A.Y. Tang, V. Drakinskiy, K. Yhland, J. Stenarson, T. Bryllert and J. Stake

accepted for publication in *IEEE Transactions on Microwave Theory and Techniques*, Jan. 2013.

Paper B

Impact of Eddy Currents and Crowding Effects on High Frequency Losses in Planar Schottky Diodes

A.Y. Tang and J. Stake

in *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3260-3269, Oct. 2011.

Paper C

Geometry Optimization of THz Sub-harmonic Schottky Mixer Diodes

A.Y. Tang, T. Bryllert and J. Stake

in *37th International Conference on Infrared, Terahertz and Millimeter Waves (IRMMW-THz)*, Wollongong, Australia, Sept. 2012.

Paper D

Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes

A.Y. Tang, E. Schlecht, G. Chattopadhyay, R. Lin, C. Lee, J. Gill, I. Mehdi, and J. Stake

in *22nd International Symposium on Space Terahertz Technology (ISSTT)*, Tucson, AZ, USA, Apr. 2011.

Paper E

Electro-Thermal Model for Multi-Anode Schottky Diode Multipliers

A.Y. Tang, E. Schlecht, R. Lin, G. Chattopadhyay, C. Lee, J. Gill, I. Mehdi, and J. Stake

in *IEEE Transactions on Terahertz Science and Technology*, vol. 2, no. 3, pp. 290-298, May 2012.