Thesis for The Degree of Doctor of Philosophy

Ultra-Low Power InAs/AlSb HEMTs for Cryogenic Low-Noise Applications

Giuseppe Moschetti

Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
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Giuseppe Moschetti

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Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
SE-412 96 Göteborg, Sweden
Phone: +46 (0) 31 772 1000

Cover: A high resolution STEM cross-section image of InAs channel, a STEM image of a threading dislocation and a pit in the InAs/AlSb heterostructure, a STEM image of a T-gate, a SEM image of a 4×50 μm gate-width HEMT and a photograph of a three-stage hybrid LNA module.

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Abstract

The InAs/AlSb high electron mobility transistor (HEMT) is an emerging microwave device technology for ultra-low power and low noise applications. Due to the low bandgap (0.36 eV) and to the high mobility and peak velocity of electrons in the InAs channel, promising performance of InAs/AlSb HEMT-based circuits has been demonstrated at room temperature. However, the characterization of the cryogenic properties had not been reported prior to this work. The study of the device performance at cryogenic temperatures, which is of large importance in scientific instrumentation where lowest noise figure and power consumption are essential, was the initial objective of this work. Throughout this investigation, results advancing the state-of-the-art in InAs/AlSb HEMTs were found and are presented in this thesis.

Anisotropic transport in the InAs/AlSb heterostructure grown on InP bulk substrate has been investigated. Significant differences in sheet resistance and electron mobility along the different crystal orientations were observed due to elongated pits in the channel. InAs/AlSb HEMTs fabricated along the favorable orientation delivered drain current and peak transconductance up to 25% higher.

The electrical performance and stability against oxidation of shallow-mesa InAs/AlSb HEMTs have been improved through the development of a fabrication process based on *in-situ* passivation. Moreover, a true planar technology based on ion implantation has been demonstrated, with state-of-the-art performance and excellent stability against oxidation. This paves the way for reliable InAs/AlSb HEMT monolithic microwave integrated circuits (MMICs).

The electrical properties InAs/AlSb HEMTs have been investigated as a function of temperature, showing an overall improvement of the device under cryogenic operation in the low-power regime. Significantly lower on-resistance and gate leakage as well as improved drain current saturation and up to 40% higher peak transconductance have been measured. At 6 K and for a drain bias of 0.1 V, the cut-off frequency and the maximum oscillation frequency increased by 72% and 100%, respectively, whereas the minimum noise figure at 8 GHz was reduced from 2.3 dB to 0.6 dB.

The suitability of the InAs/AlSb HEMT for cryogenic and ultra low-power applications was demonstrated in a three-stage low noise amplifier operating in the 4-8 GHz frequency range. At 13 K, a minimum noise temperature of 19 K and a gain above 24 dB were measured at a total DC power consumption of only 6 mW. This corresponded to an ultra-low power consumption of only 600 μW in the HEMT device.

Keywords: InAs/AlSb, high electron mobility transistor (HEMT), metamorphic, cryogenic, low power, high frequency, low noise, ion implantation.

List of Publications

Appended papers

This thesis is based on the work contained in the following papers:

[A] G. Moschetti, H. Zhao, P.-Å. Nilsson, S. Wang, A. Kalabukhov, L. Desplanque, X. Wallart and J. Grahn "Anisotropic transport properties in InAs/AlSb heterostructures", *Applied Physics Letters*, vol. 97, no. 24, pp. 243510, December, 2010.

[B] G. Moschetti, N. Wadefalk, P.-Å. Nilsson, Y. Roelens, A. Noudeviwa, L. Desplanque, X. Wallart, F. Danneville, G. Dambrine, S. Bollaert and J. Grahn "InAs/AlSb HEMTs for cryogenic LNAs at ultra-low power dissipation", *Solid-State Electronics*, vol. 64, no. 1, pp. 47-53, July, 2011.

[C] G. Moschetti, E. Lefebvre, M. Fagerlind, P.-Å. Nilsson, L. Desplanque, X. Wallart and J. Grahn "DC, RF and noise performance of InAs/AlSb HEMTs with *in-situ* CVD SiN_x-film for early-protection agaist oxidation", Submitted to *Solid-State Electronics*, 2012.

[D] G. Moschetti, P.-Å. Nilsson, A. Hallén, L. Desplanque, X. Wallart and J. Grahn "Planar InAs/AlSb HEMTs With Ion-Implanted Isolation", *IEEE Electron Device Letters*, vol. 33, no. 4, pp. 510-512, April, 2012.

[E] G. Moschetti, A. Morteza, P.-Å. Nilsson, A. Hallén, L. Desplanque, X. Wallart and J. Grahn "True planar InAs/AlSb HEMTs with Ion-Implantation Technique for Low-Power Cryogenic Applications", *Accepted for Publication in Solid-State Electronics*, 2012.

[F] G. Moschetti, P.-Å. Nilsson, A. Hallén, L. Desplanque, X. Wallart and J. Grahn "Source-Drain Scaling of Ion-Implanted InAs/AlSb HEMTs", in *IEEE IPRM International Conference on Indium Phosphide & Related Materials*, August, 2012.

[G] G. Moschetti, N. Wadefalk, P.-Å. Nilsson, A. Morteza, L. Desplanque, X. Wallart and J. Grahn "Cryogenic InAs/AlSb HEMT Wideband Low-Noise IF Amplifier for Ultra-Low-Power Applications", *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 3, pp. 144-146, March, 2012.

Other papers and publications

The following papers and publications are not appended to the thesis, either due to contents overlapping with appended papers, or due to contents not related to the thesis.

[a] E. Lefebvre, G. Moschetti, M. Malmkvist, L. Desplanque, X. Wallart and J. Grahn "Comparison of shallow-mesa InAs/AlSb HEMTs with and without early-protection for long-term stability against Al(Ga)Sb oxidation", To be Submitted to *Semiconductor Science and Technology*, 2012.

[b] G. Moschetti, N. Wadefalk, P.-Å. Nilsson, A. Morteza, L. Desplanque, X. Wallart and J. Grahn "Cryogenic Operation of InAs/AlSb HEMT Hybrid LNAs", in *42nd European Microwave Conference Proceeding*, October, 2012.

[c] A. Westlund, G. Moschetti, H. Zhao, P.-Å. Nilsson and J. Grahn "Fabrication and DC characterization of InAs/AlSb Self-Switching Diodes", in *IEEE IPRM International Conference on Indium Phosphide & Related Materials*, August, 2012.

[d] L. Desplanque, S. El Kazzi, J.L. Codron, Y. Wang, P. Ruterana, G. Moschetti, J. Grahn, and X. Wallart "AlSb nucleation induced anisotropic electron mobility in AlSb/InAs heterostructures on GaAs", *Applied Physics Letters*, vol. 100, no. 26, pp. 262103, June, 2012.

[e] B. G. Vasallo, H. Rodilla, T. González, G. Moschetti, J. Grahn and J. Mateos "Kink effect and noise performance in isolated-gate InAs/AlSb High Electron Mobility Transistors", *Semiconductor Science and Technology*, vol. 27, no. 6, pp. 065018, May, 2012.

[f] G. Moschetti, P-Å Nilsson, L. Desplanque, X. Wallart and J. Grahn, "InAs/AlSb HEMTs for Ultra Low-Power Cryogenic LNAs," in *GigaHertz Symposium*, Stockholm, Sweden, March, 2012.

[g] Y. Alimi, C. Balocco, H. Zhao, A. Westlund, G. Moschetti, P.-Å. Nilsson, J. Grahn, and A.M. Song "Fabrication of Novel Unipolar Nanodiodes in InAs/AlSb for Microwave Detection", in *IEEE IRMMW International Conference on Infrared, Millimeter, and Terahertz Waves*, October, 2011.

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[i] G. Moschetti, H. Zhao, P.-Å. Nilsson, S. Wang, A. Kalabukhov, G. Dambrine, S. Bollaert, L. Desplanque, X. Wallart, and J. Grahn "Anisotropic Transport of InAs/AlSb Heterostructures grown on InP Substrates," in *Workshop on Compound Semiconductor Devices and Integrated Circuits, WOCSDICE*, May, 2011.

[j] B. G. Vasallo, H. Rodilla, T. González, G. Moschetti, J. Grahn and J. Mateos "Monte Carlo study of kink effect in isolated-gate InAs/AlSb High Electron Mobility Transistors", *Journal of Applied Physics*, vol. 108, no. 9, pp. 094505 - 094505-5 , November, 2010.

[k] A. Noudeviwa, Y. Roelens, F. Danneville, A. Olivier, N. Wichmann, N. Waldhoff, S. Lepilliet, G. Dambrine, L. Desplanque, X. Wallart, G. Moschetti, J. Grahn and S. Bollaert "Sb-HEMT: Toward 100-mV Cryogenic Electronics", *IEEE Transactions on Electron Devices*, vol. 57, no. 8, pp. 1903-1909, June, 2010.

[l] G. Moschetti, P.-Å. Nilsson, L. Desplanque, X. Wallart, H. Rodilla, J. Mateos and J. Grahn "DC and RF cryogenic behavior of InAs/AlSb HEMTs", in *IEEE IPRM International Conference on Indium Phosphide & Related Materials*, May, 2010.

[m] H. Rodilla, T. González, M. Malmkvist, E. Lefebvre, G. Moschetti, J. Grahn and J. Mateos "Isolated-Gate InAs/AlSb HEMTs: a Monte Carlo study", in *IEEE IPRM International Conference on Indium Phosphide & Related Materials*, May, 2010.

[n] G. Moschetti, P-Å Nilsson, Y. Roelens, F. Danneville, S. Bollaert, G. Dambrine, L. Desplanque, X. Wallart, H. Zirath and J. Grahn, "Cryogenic behaviour of InAs/AlSb HEMTs for low-noise amplifiers," in *GigaHertz Symposium*, Lund, Sweden, March, 2010.

[o] G. Dambrine, S. Bollaert, Y. Roellens, A. Noudeviwa, F. Danneville, A. Olivier, N. Wichmann, L. Desplanque, X. Wallart, J. Grahn, G. Moschetti, P.-Å. Nilsson, M. Malmkvist, E. Lefebvre "Narrow band gap III-V based-FET for ultra low power high frequency analog applications", in *Device Research Conference*, pp.149-151, June, 2009.

[p] G. Moschetti, P.-Å. Nilsson, N. Wadefalk, M. Malmkvist, E. Lefebvre, Y. Roelens, A. Noudeviwa, A. Olivier, S. Bollaert, F. Danneville, L. Desplanque, X. Wallart, G. Dambrine and J. Grahn "DC characteristics of InAs/AlSb HEMTs at cryogenic temperatures", in *IEEE IPRM International Conference on Indium Phosphide & Related Materials*, May, 2009.

[q] F. Roccaforte, F. Iucolano, F. Giannazzo, G. Moschetti, C. Bongiorno, S. Di Franco, V. Puglisi, G. Abbondanza, V. Raineri, "Influence of thermal annealing on Ohmic contacts and device isolation in AlGaN/GaN heterostructures," *Materials Science Forum*, vol. 615-617, pp. 967-970, 2009.

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Ni-Si Ohmic Contacts to 3C-SiC, *Materials Science Forum*, vol. 615-617, pp. 569-572, 2009.

Notations and abbreviations

Notations

a	Lattice constant
μ_n	Electron mobility
d_{sd}	Source-Drain distance
E_g	Energy gap
E_L	Energy separation between L valley and Γ valley
E_X	Energy separation between X valley and Γ valley
ΔE_C	Conduction band discontinuity
ε	Normalized error function
f_{max}	Maximum frequency of oscillation
f_T	Current gain cut-off frequency
g_{DS}	DC output conductance
g_{ds}	RF output conductance
g_m	DC transconductance
g_{mi}	Small-signal transconductance
I_{DS}	Drain to source current
I_G	Gate current
I_{off}	Off-state current
I_{on}	On-state current
L_g	Gate length
m_e^*	Electron effective mass
n_s	Electron density
$NF_{50\Omega}$	Noise figure at 50Ω
NF_{min}	Minimum noise figure
P_{DC}	DC power consumption
q	Electron charge
R_d	Drain resistance
R_{DS}	Access resistance
R_{off}	Off-resistance
R_{on}	On-resistance
R_s	Source resistance
R_g	Gate resistance
R_{sh}	Sheet resistance
S	Subthreshold slope

T_n	Noise temperature
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
v_{sat}	Electron saturation velocity
W_g	Gate width

Abbreviations

2DEG	Two Dimensional Electron Gas
ABCS	Antimonide Based Compound Semiconductors
ALD	Atomic Layer Deposition
AlGaSb	Aluminium Gallium Antimonide
AlSb	Aluminium Antimonide
CAT	Cold Attenuator System
CVD	Chemical Vapor Deposition
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
EDS	Energy Dispersive Spectroscopy
FIB-SEM	Scanning Electron Microscope Focused Ion Beam
GaAs	Gallium Arsenide
HEMT	High Electron Mobility Transistor
ICP	Inductive Coupled Plasma
InAlAs	Indium Aluminium Arsenide
InAs	Indium Arsenide
InP	Indium Phosphide
LNA	Low Noise Amplifier
MBE	Molecular Beam Epitaxy
MMIC	Microwave Monolithic Integrated Circuit
RF	Radio Frequency
RIE	Reactive Ion Etching
RMS	Root Mean Square
RS	Reactive Sputtering
SiN_x	Silicon Nitride
SSM	Small Signal Model
STEM	Scanning Transmission Electron Microscopy
S.I.	Semi Insulating
TLM	Transfer Length Method
VNA	Vector Network Analyzer

Contents

Chapter 1

Introduction

The first high electron mobility transistor (HEMT) based on the InAs/AlSb heterostructure was demonstrated by Tuttle *et al.* in 1987 [1]. Due to the transport properties of InAs bulk, the electron mobility and peak velocity in the two dimensional electron gas (2DEG) are almost twice as high as in InP HEMTs [2]. Moreover, this is combined with the narrow bandgap of about 0.36 eV and with an extraordinary electron confinement in the well which is due to the staggered band alignment of the heterojunction. The combination of such properties makes the InAs/AlSb HEMT a potential device candidate for applications in mobile microwave-millimeter wave communication systems or active phased arrays where high speed must be combined with very low power consumption [3, 4]. The InAs/AlSb HEMT can operate with half or less power consumption of equivalent InP HEMTs exhibiting similar RF performances [3, 5]. Integrated InAs/AlSb HEMT-based amplifiers have been demonstrated at room temperature with excellent RF performance [5–8].

Several challenges have hindered the introduction of the InAs/AlSb HEMT in industrial applications. The lack of semi-insulating (S.I.) semiconductor substrates which are lattice matched to the 6.1 Å lattice constant of the InAs channel makes the growth of high quality epitaxial layers very difficult. The low bandgap of the InAs channel leads to severe impact ionization effects already at low electric fields causing elevated gate leakage current and high output conductance. In addition, AlSb-based alloys are extremely sensitive to oxidation when exposed to the environment, rendering the fabrication of stable and reliable devices based on these heterostructures very challenging. In contrast to the GaAs and InP HEMT technologies, qualified industrial InAs/AlSb HEMT processes are not yet available for circuit designers.

One of the unexplored subjects of InAs/AlSb HEMT technology is its potential for cryogenic applications. Cryogenic operation at 5-15 K of microwave low-noise amplifiers (LNAs) is crucial to reduce the noise temperature in scientific instrumentation found in radio astronomy and space-borne communication systems. In such applications, the antenna noise temperature is typically one order of magnitude less than in terrestrial applications (300 K). For this reason the receiver noise temperature is usually the dominant part in a system's noise temperature. Thus, cryogenic cooling allows to reduce the noise temperature of the receiver improving its sensitivity [9].

The electron transport improvement in the channel and the reduction of the thermal noise generated by the parasitic elements [9, 10] at low temperature make the InAs/AlSb HEMT potentially suitable for cryogenic receivers. While room temperature operation of microwave InAs/AlSb HEMTs has been extensively reported during the last ten years [4, 5, 11–19], very few studies have been published on the cryogenic operation of the InAs/AlSb HEMT.

In this thesis work, the potential of the InAs/AlSb HEMT as a key component in cryogenic low-noise amplifiers with ultra-low power consumption has been investigated. The results clearly demonstrate that the DC, RF and noise properties of InAs/AlSb HEMTs are much improved under low-bias operation when cooled. The anisotropic behaviour of the electron transport in the channel has been discovered and investigated through morphological, structural and electrical characterization. Furthermore, the reliability issues related to the high tendency of oxidation of AlSb layers have been addressed by solving material and process related challenges. The HEMT process has been developed along two directions: by introducing a new *in-situ* early-passivation and by developing a process based on ion implantation for device isolation. This lead to better electrical performance as well as to a significantly higher stability against oxidation which allowed the demonstration of the first cryogenic hybrid LNA based on InAs/AlSb HEMT technology.

Chapter 2 provides a brief background of the InAs/AlSb heterostructure. Chapter 3 describes the investigation of the anisotropic behaviour in the InAs/AlSb HEMT structure through morphological and structural characterization, as well as via electrical characterization at different temperatures. Chapter 4 concerns the description of the HEMT fabrication process and its development, as well as the electrical characterization at room temperature. Moreover, the performance related to the lateral scaling of the source-drain distance for the planar InAs/AlSb HEMTs is discussed. In Chapter 5, the DC, RF and noise behavior of the device at cryogenic temperature are presented. The cryogenic characterization of a 4-8 GHz hybrid LNA built with the fabricated InAs/AlSb HEMTs is presented in Chapter 6. Finally, conclusions and suggestions for future work are found in Chapter 7.

Chapter 2

Background

High speed HEMTs for low-power and low-noise applications are evolving towards narrower bandgaps and larger lattice constants. After the first and second generation based on GaAs and InGaAs channel, respectively, the need for even better performance has lead to the third HEMT generation based on the pure InAs channel. This trend as well as the relationship between bandgap and lattice constant of the most important compound semiconductors is shown in Fig. 2.1. Advantages of the InAs compound include a very high electron mobility and peak velocity of about 33,000 $\mathrm{cm}^2/\mathrm{Vs}$ and 4.4×10^7 cm/s, respectively, at room temperature [20]. Such properties, combined with the low bandgap of 0.36 eV, potentially make transistors based on InAs channel excellent candidates for low-noise microwave/millimeter wave amplifiers with ultra-low power consumption. However, the low bandgap and the large lattice constant of InAs also results in drawbacks which will be discussed in this chapter.

2.1 InAs bulk properties

InAs, a compound semiconductor formed by indium (group III) and arsenic (group V), is based on the cubic zinc blende structure with a lattice constant a = 6.1 Å. The main InAs properties are summarized and compared to other III-V based channel materials as well as to the most widely used semiconductor in commercial applications (Silicon) in Table 2.1. The very high bulk electron mobility μ_n of InAs, compared to other channel materials, is due to the low electron effective mass m_e^* in the central valley. The schematic of the band structure of InAs is presented in Fig. 2.2. Due to the low bandgap, impact ionization becomes important even at low electric fields. Moreover, it is also very important to observe the large energy distance between the central Γ valley and the energies of the satellites L and X valleys, compared to the bandgap. These energies E_L and E_X are respectively 1.08 eV and 1.37 eV, thus much larger than the bandgap E_g. The energy which causes impact ionization phenomena is hence lower than that needed by the electrons in order to reach the L and X valleys. Consequently, the impact ionization occurs before any intervalley scattering processes, thus confining the electrons to the Γ valley. For this reason, in pure InAs, the dominant scattering mechanism is due to

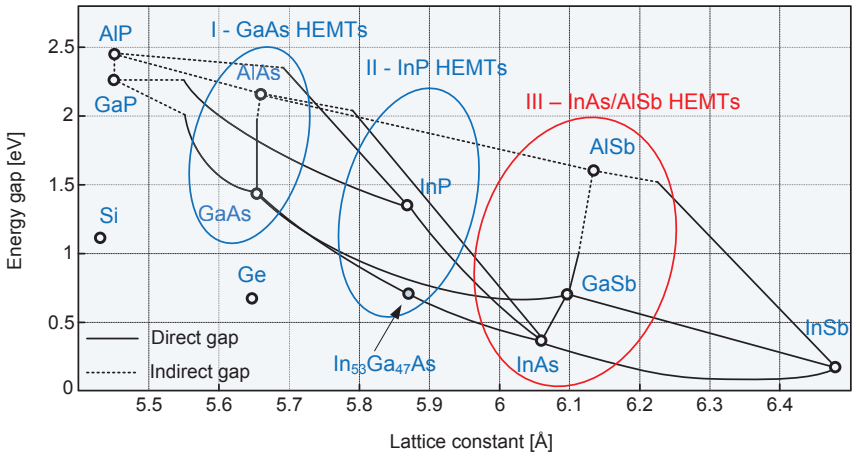


Fig. 2.1: Evolution of high speed transistors towards lower bandgap and larger lattice constant for low-power operation [21].

polar optical phonons. The effect of intervalley scattering on the drift velocity becomes important only at very high applied fields [22, 23].

2.2 InAs/AlSb heterostructure

A heterostructure is formed when two dissimilar materials are placed into contact. In case of a semiconductor-semiconductor heterostructure, the two materials have different bandgaps. Because of this, the valence band and the conduction band cannot be simultaneously continuous at the interface between the two different materials [29]. This leads to a discontinuity in the conduction and/or valence bands at the interface between the two semiconductors. In addition, electrons are transferred from the wide bandgap semiconductor to the narrow bandgap semiconductor to align the Fermi level. This electron transfer causes the bending of the conduction band in the narrow bandgap semiconductor. The conduction band bending and discontinuity forms a quantum well. Depending on the properties of the two semiconductors, among which bandgap and affinity differences, different band lineups can occur. There are three kinds of band alignment which gives heterostructures of type-I, type-II

Table 2.1: Material properties of different semiconductor channel materials [24–28].

Properties	Si	2H-GaN	GaAs	$In_{53}Ga_{47}As$	InAs	InSb
E_g [eV]	1.12	3.4	1.42	0.74	0.36	0.18
μ_n [cm^2/Vs]	1400	1000	8500	14000	33000	77000
v_{sat} [10^7 cm/s]	1.0	2.5	2.0	3.4	4.4	5.0
m_e^* [m_0]	0.19	0.2	0.067	0.041	0.023	0.014
E_L [eV]	-	1.1	0.3	0.7	1.1	0.7
a [Å]	5.43	3.19	5.65	5.87	6.06	6.48

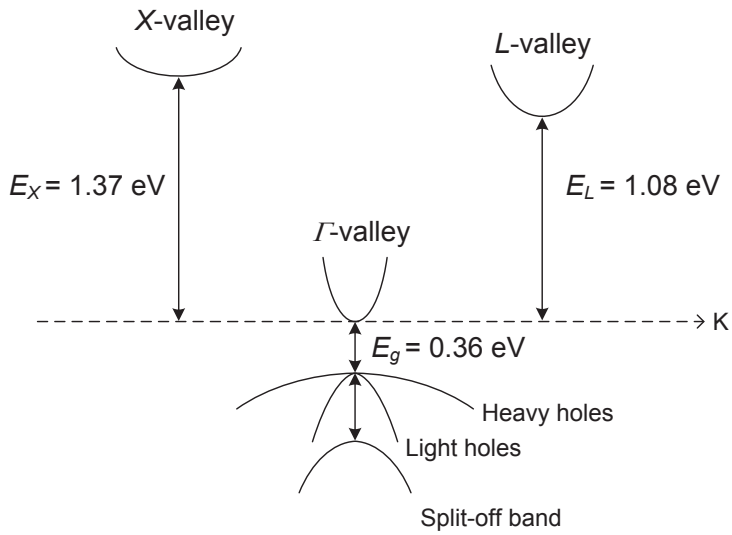


Fig. 2.2: Schematic band structure of InAs.

and type-III; See Fig. 2.3.

Antimonide based compound semiconductors (ABCS) are formed by alloying elements of the III-group, such as In, Al, Ga together with elements of the V-group such as Sb, As etc. [25]. The ABCS are often referred to as "the 6.1 Å family" because of the lattice constant around 6.1 Å [30]. The InAs/AlSb heterostructure is formed by joining a wide bandgap AlSb barrier with a narrow bandgap InAs channel. The combination of these two semiconductors leads to a band lineup of type-II (staggered) as well as to one of the largest conduction band discontinuities ΔE_C ($\sim$1.35 eV) among III-V based heterostructures [31]. Such a deep well allows excellent electron confinement and high electron concentration. The first attempts to use the InAs/AlSb junction in high electron mobility heterostructures were performed at the University of California Santa Barbara by the group of Prof. Herbert Kroemer in the early 1990s [1, 32, 33].

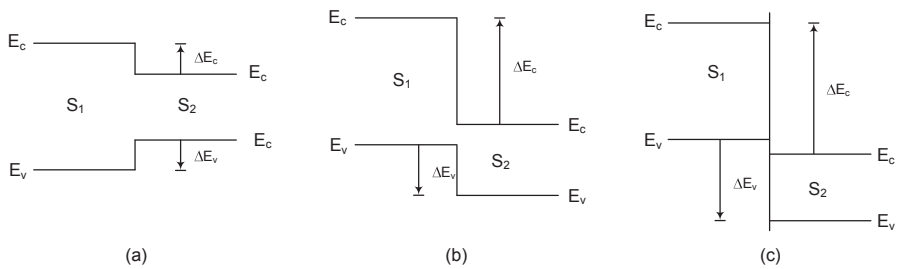


Fig. 2.3: The three type of heterostructures that can be formed by joining two different semiconductors S_1 and S_2: (a) type-I (straddled), (b) type-II (staggered) and (c) type-III (broken gap)

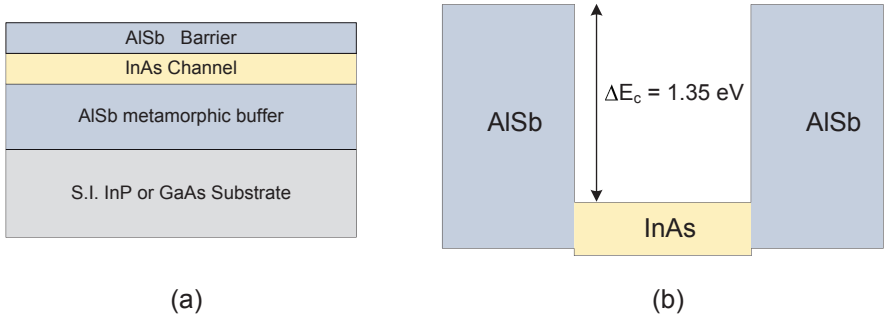


Fig. 2.4: Schematic of InAs/AlSb HEMT (a) epitaxial layers and (b) band diagram.

The InAs/AlSb heterostructure presents both advantages and drawbacks. One of the main drawbacks of using a pure InAs channel is the lack of S.I. semiconductor substrates which are lattice matched to the large lattice constant of 6.1 Å. The only lattice matched semiconductor substrate available is GaSb which however presents a p-type residual doping preventing its use in high-speed devices [34]. Therefore InAs/AlSb heterostructures are usually grown on GaAs or InP substrates through a metamorphic approach. High electron mobility of 27,000 cm^2/Vs has also been demonstrated for InAs/AlSb heterostructures grown on Si substrates [35], but no transistor data has been reported so far. The strain between channel and substrate is accommodated by growing a relatively thick (1 μm or above) AlSb metamorphic buffer which has a low lattice mismatch of about 1.2% to InAs. The need of a thick AlSb buffer is a major drawback for InAs/AlSb HEMT devices, because of the high tendency to oxidation which characterizes the AlSb compound semiconductor when exposed to air, water or basic solutions. The development of oxidation resistant fabrication processes of InAs/AlSb HEMTs will be discussed in Chapter 4.

Fig. 2.4 presents schematic images of the AlSb/InAs/AlSb epitaxial layers and the band lineup of type-II in the quantum well. Due to the exceptionally high ΔE_C, the electron sheet concentration in the 2DEG is fairly high, above $3{\times}10^{11}\,cm^{-2}$, even in not-intentionally doped wells. The origin of this high amount of electrons can be attributed to shallow bulk donors, to surface states on the AlSb top barrier and to deep bulk donors near or at the InAs/AlSb hetero-interface [30, 32]. The shallow bulk donors, intentionally placed into the barrier rather than into the well (modulation doping), are spatially separated from the electrons, allowing low impurity scattering and hence high electron mobilities. Typical donors used for modulation doping in InAs/AlSb heterostructures are elements of the VI-group, like Te [36]. Si can also be used as donor but, due to its amphoteric behavior in III-V compounds [37], it acts as acceptor in the AlSb compound. Surface states located on the outside of the AlSb top barrier are another source of electrons in the well. The amount of electrons due to surface states are related to the barrier thickness as well as to the material used as capping layer on top of the barrier. Deep bulk donors have been attributed to *Tamm states* in the InAs/AlSb interface [38]

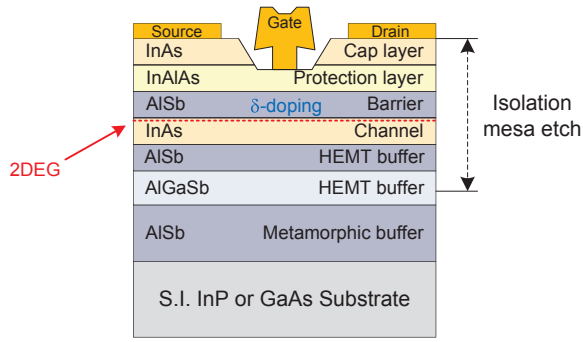


Fig. 2.5: Schematic of the InAs/AlSb HEMT structure.

and to states associated with Al_{Sb} antisite defects (Al atoms on Sb sites) [39], however the nature of these deep donors is still not clear.

If the electron confinement in the channel constitutes one of the strengths of the InAs/AlSb band lineup, the hole confinement is instead a weak point. The low bandgap of the InAs compound leads to generation of a high amount of holes in the channel which are free to flow through the AlSb barrier since the valence band in the channel is at a lower energy than that of the barrier. This can lead to leakage problems in gated structures such as HEMT devices.

Another important property of the InAs/AlSb quantum well is the strong dependence of the electron mobility not only to the electron sheet concentration but also to the well width. The optimal values of sheet concentration and well width have been reported to be, respectively, $1.5\times10^{12}\,\mathrm{cm}^{-2}$ and 15 nm [30]. Narrower wells can lead to a reduced mobility due to interface roughness scattering [40, 41], whereas in wells wider than 15 nm the electron mobility tends to decrease due to inter-subband scattering [30].

2.3 InAs/AlSb HEMT

The schematic of a typical InAs/AlSb HEMT epitaxial structure is shown in Fig. 2.5. The epilayers are usually grown on semi insulating InP or GaAs substrates by molecular beam epitaxy (MBE). As described in Section 2.2, the large lattice mismatch between channel and substrate is accommodated by the growth of a thick AlSb metamorphic buffer. An AlGaSb layer is usually added into the buffer because of its enhanced chemical stability compared to AlSb. The AlGaSb layer provides a more stable mesa floor in planar technologies based on dry or wet shallow mesa etching [36]. A drawback of the AlGaSb alloy is that its resistivity is lower than that of AlSb. This causes losses which can degrade the device performance and introduces a tradeoff between electrical performance and stability against oxidation making the mesa isolation etch a very critical step [42]. Furthermore, even if more stable than AlSb, the AlGaSb alloy still tends to suffer from oxidation.

The doping of the AlSb barrier, known as δ-doping, can be either Si or Te. In case of Si δ-doping the donors are introduced in a quantum-well formed by a sandwich of InAs monolayers. Because of its amphoteric behaviour in III-V

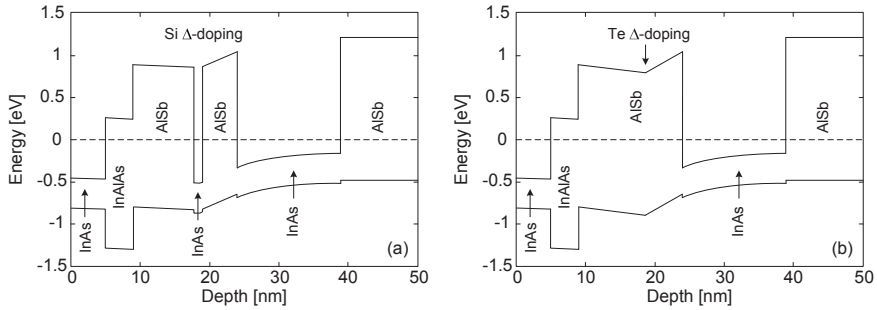


Fig. 2.6: Energy band diagrams at thermal equilibrium of the InAs/AlSb HEMT structure with (a) Si δ-doping and with (b) Te δ-doping [43].

compounds, Si would provide holes if placed directly in contact with AlSb [13]. The band diagram of the InAs/AlSb heterostructure with Si δ-doping and Te δ-doping are plotted in Fig. 2.6 (a) and in Fig. 2.6 (b), respectively. The conduction band minima and valence band maxima are plotted versus the depth in the heterostructure. The δ-doping enhances the amount of electrons which fill the quantum well forming the 2DEG. Such electrons are free to move in the directions parallel to the channel interface but are confined along the direction orthogonal to the channel.

Exposure to the environment of the AlSb barrier is prevented by the InAlAs protection layer. As can be seen in the band diagram of Fig. 2.6, this layer also acts as a barrier for the holes generated in the channel by impact ionization, thus limiting the hole component of the gate leakage current in the HEMT. However, due to the lack of confinement in the valence band related to the type-II band lineup, most of the holes pile up in the AlSb buffer underneath the channel. The holes lose energy in the AlSb buffer because of scattering and cannot return back to the channel [44]. The accumulation of positive charges underneath the channel acts as a positively biased back gate, increasing the current through the channel and thus the output conductance of the HEMT. This leads to severe degradation of the RF and noise performance of the device.

The contact resistance at the metal-semiconductor interface in the source and drain contacts of the HEMT is reduced by growing a highly doped InAs cap layer on top of the InAlAs protection layer. This highly conductive cap layer is removed through a recess etch in the region underneath the gate in order to avoid a low resistive path between gate and source/drain contacts. The recess etch of the InAs cap layer leads to another challenge of the HEMT fabrication since a non-uniform etch may result in either a poor gate channel control (too shallow etch) or to exposure of the AlSb barrier to the environment (too deep etch) [19].

2.4 State-of-the-art low noise HEMTs

The first generation of HEMT devices was based on the AlGaAs/GaAs heterostructure grown on a GaAs substrate [45]; See Fig. 2.1. In order to improve the electron mobility and confinement in the quantum well, indium was added to the channel leading to AlGaAs/InGaAs heterostructure based devices also known as pseudomorphic HEMTs (pHEMT) [21]. The need of even higher operation frequency has been accomplished by increasing the In content in the channel above 50% and by using the InAlAs alloy as a barrier material. The InP substrate was then introduced in order to accommodate the large lattice mismatch due to the high In content. The InAlAs/InGaAs/InP transistors are known as InP HEMTs and represent the second generation of HEMTs. In parallel, a growth technology known as metamorphic was developed. This allowed to grow devices incorporating high In-content layers on GaAs substrates but without alleviating device performance, as it otherwise happens due to the roughness or to crystallographic defects (threading dislocations) resulting from the large lattice mismatch. Pioneering attempts were done in 1988 for FET and HBT with 50%-InGaAs layers on GaAs substrate. This device, know as the metamorphic HEMT (mHEMT), was first demonstrated by Win et al. [46].

During the last 20 years, the InP HEMT technology has been the work horse for the design of ultra-low noise cryogenic amplifiers with state of the art performance at microwave and millimeter-wave frequencies [9, 47–55]. Record low noise temperatures of about 1.6 - 1.8 K have been demonstrated in 4-8 GHz cryogenic InP HEMT LNAs with power consumption in the range 4 - 5 mW [56, 57]. Furthermore, InP HEMTs with extremely high cut-off frequencies $f_T > 600\,\text{GHz}$ and maximum oscillation frequency $f_{max} > 1200\,\text{GHz}$ have been demonstrated thanks to scaling of the gate length L_g down to 30 nm [58, 59]. The metamorphic HEMT technology has shown competitive performance against the InP HEMT in terms of f_T, noise figure and low-power consumption at room temperature [60–63]. However, its noise performance at cryogenic temperature is not as good as for the InP HEMT so far [64–66].

Compared to the mature and established HEMT technologies, the InAs/AlSb HEMT can theoretically provide large improvements in terms of power consumption, RF and noise performance because of the combination of a narrower bandgap with significantly higher electron mobility and peak velocity in the channel. The pure InAs channel has in fact μ_n and v_{sat} which are, respectively, 100% and 30% higher compared to $In_{53}Ga_{47}As$; See Table 2.1. However, the InAs/AlSb HEMT still suffers from high gate leakage current and high output conductance due to the impact ionization occurring in the narrow bandgap InAs channel. This tends to degrade the RF and noise performance. State-of-the-art InAs/AlSb HEMTs have been reported at room temperature with f_T up to 270 GHz and with noise figure between 0.6 and 1.5 dB in the frequency band 2 - 20 GHz [5, 12, 14, 16, 67–71]. These values are not yet competitive compared to InP and metamorphic HEMT technology. However, InAs/AlSb HEMT based LNAs operating at very low power consumption, down to about 1 mW, have been demonstrated at room temperature [5, 72, 73] showing the potential of this device technology for ultra-low power applications. Improvements of the RF and noise performance through proper scaling and fabrication process development are hence needed in order to achieve the outstanding re-

sults expected from the InAs electronic properties.

In addition, the performance of InAs/AlSb HEMTs are expected to improve under cryogenic operation. This, mainly related to the reduced phonon scattering upon cooling which enhances the electron mobility in the 2DEG, can potentially lead to the demonstration of cryogenic microwave amplifiers with state-of-the-art noise and gain performance under ultra-low power conditions. However, the cryogenic behavior of the InAs/AlSb HEMT has not been thoroughly investigated so far. Moreover, the demonstration of this device technology in cryogenic amplifiers is not reported yet. All this present lack of investigation and demonstration of cryogenic InAs/AlSb HEMTs constituted the underlying motivation for this thesis. The results will be presented in the rest of this work.

Chapter 3

InAs/AlSb HEMT Anisotropic Behaviour

The growth of InAs channel on InP or GaAs substrates is achieved through the use of a AlSb metamorphic buffer, which accommodates the large compressive strain [34, 74]. This results in a tensile strain in the InAs channel and in a compressive strain in the AlSb metamorphic buffer which can lead to the formations of threading dislocations [75]. During the course of this work, variations in HEMT electrical properties were observed. It was found that there existed a relation between electrical performance and orientation of the device. Anisotropic electron transport in HEMT devices based on strained layers of III-V alloys have previously been reported [76–78]. In this chapter, the anisotropic transport phenomena in InAs/AlSb heterostructures grown on the (001) InP substrate have been investigated through morphological, structural and electrical characterization. The investigation resulted in a consistent explanation of the anisotropic transport with the presence of elongated pits in the InAs channel which are related to threading dislocations in the AlSb buffer.

3.1 Epitaxial structure

The InAs/AlSb HEMT epitaxial structure used was grown by MBE on a S.I. InP substrate and is shown in Fig. 3.1. The growth started with a 100 nm thick $In_{50}Al_{50}As$ smoothing layer needed to reduce the roughness of the substrate. A metamorphic buffer formed by a 700 nm thick AlSb layer was subsequently grown in order to accommodate the lattice mismatch between the InP substrate and the InAs channel. This AlSb layer suffers from very strong oxidation when exposed to the environment [79]. In order to improve the chemical stability of the device, a 250 nm thick $Al_{80}Ga_{20}Sb$ layer was grown over the AlSb buffer. This allows a more stable shallow mesa floor since the $Al_{80}Ga_{20}Sb$ is less reactive compared to the AlSb layer [13]. A 15 nm thick InAs channel was then grown above a 50 nm AlSb HEMT buffer to form the active device layers. Furthermore a 5 nm thick AlSb spacer, a Te δ-doping and an 8 nm thick AlSb Schottky barrier layer were grown and protected against oxidation

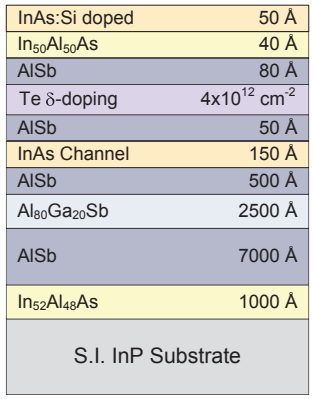


Fig. 3.1: InAs/AlSb HEMT epitaxial structure

by a 4 nm $In_{50}Al_{50}As$ protection layer. This $In_{50}Al_{50}As$ layer also acts as a barrier against holes generated in the channel, reducing the impact ionization gate leakage current [18]. Finally, a 5 nm thick Si-doped InAs layer, for ohmic contact formation, was grown. Heterostructures based on Si δ-doping were also grown.

3.2 Morphological and structural characterization

Atomic force microscopy (AFM) measurements, on top of the InAs cap layer of the structure of Fig. 3.1, were performed by using a DI 3000 Veeco equipment in tapping mode. As shown in Fig. 3.2, cracks elongated in the $[1\bar{1}0]$ direction were clearly visible in the InAs surface. This leaded to anisotropy in the root-mean-square (RMS) roughness of 1.13 nm and 1.67 nm along the $[1\bar{1}0]$ and [110] directions, respectively. Similar cracks in the InAs/AlSb material system have been observed also in [80,81]. The presence of these cracks could be attributed to the tensile strain in the $In_{0.5}Al_{0.5}As$ protection layer resulting from a large lattice mismatch compared to the InAs/AlSb system. Due to the different lattice constant between the AlSb barrier layer and the $In_{0.5}Al_{0.5}As$ protection layer, the formation of dislocation may occur if the thickness of $In_{0.5}Al_{0.5}As$ is larger than the critical thickness t_c. This can be seen in Fig. 3.3. The t_c above which the relaxation of the strain occurs through the formation of dislocation at the interface can be calculated using the following empirical formula [82]:

$$t_c \approx \frac{a_1^2}{2|a_1 - a_2|} \tag{3.1}$$

where a_1 and a_2 are the lattice constants of $In_{0.5}Al_{0.5}As$ and AlSb layers, respectively. It should be noted that Eq. (3.1) is an approximation since t_c can also be affected by other growth parameters such as the temperature [83]. According to Eq. (3.1) the t_c of a $In_{0.5}Al_{0.5}As$ layer grown on top of an AlSb layer is about 5.3 nm, and thus larger than the thickness of the $In_{0.5}Al_{0.5}As$ protection layer. Therefore, dislocations are probably not caused by this layer.

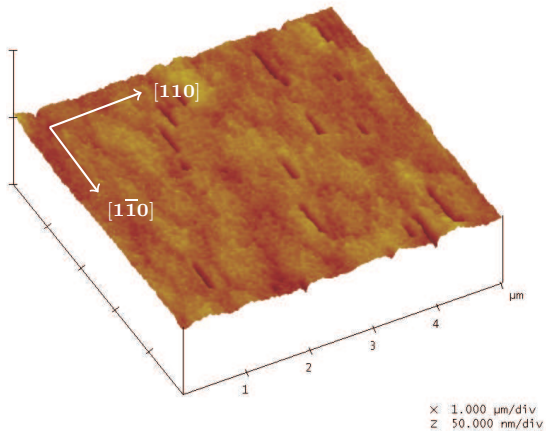


Fig. 3.2: AFM measurement (scaled to 5 μm × 5 μm) performed on top of the InAs cap layer.

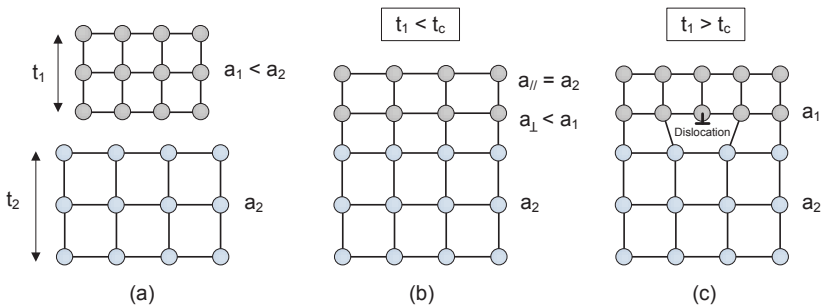
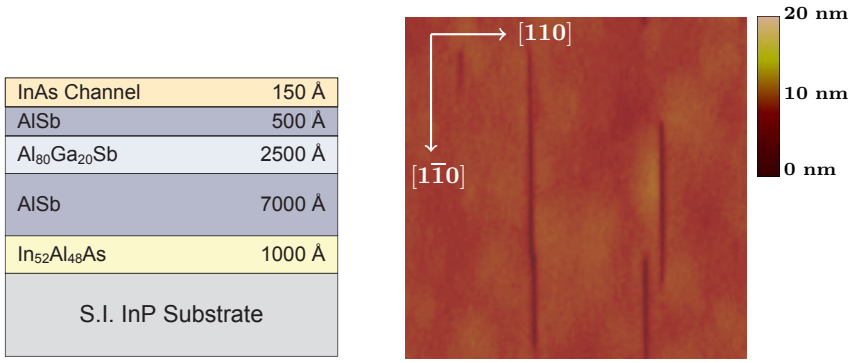


Fig. 3.3: Epitaxial growth of materials with different lattice constants a_1 and a_2. (a) Materials in separation. (b) t_1 is lower than the critical thickness t_c and hence the top layer is under tensile strain. (c) t_1 is higher than t_c and thus relaxation occurs through the formation of dislocation at the interface.

In order to experimentally investigate if the observed cracks in the surface are related to the strain in the $In_{0.5}Al_{0.5}As$ cap layer, a test heterostructure was grown up to the InAs channel, thus omitting the growth of all the subsequent layers. This heterostructure cross-section is shown in Fig. 3.4(a). AFM measurements performed on top of the InAs channel layer revealed that the elongated cracks were still present, even if the $In_{0.5}Al_{0.5}As$ protection layer was not grown; See Fig. 3.4(b). Therefore, this experiment indicated that the elongated cracks were not caused by the strain in the $In_{0.5}Al_{0.5}As$/AlSb interface. A cross-sectional analysis of the InAs/AlSb HEMT heterostructure was performed through scanning transmission electron microscopy (STEM), in order to clarify the origin of the elongated features. In Fig. 3.5 the STEM image of the heterostructure cross-section cut along the [110] direction is shown. Fig. 3.5 clearly shows that a threading dislocation, starting from the AlSb metamorphic buffer, propagates throughout the structure. The threading dis-



(a) (b)

Fig. 3.4: InAs/AlSb HEMT epitaxial structure grown up to the InAs channel. (a) Schematic cross-section. (b) AFM measurement (scaled to 2 μm × 2 μm) performed on the top InAs channel layer.

location induces a pit in the InAs channel as shown in the magnified image of Fig. 3.6. The pit cannot be smoothed out by the subsequent growth of the upper barrier and cap layers, resulting in the crack observed from the AFM measurements of the surface. Similar phenomena of such threading dislocation associated pits have also been found in GaInN structures [84].

In order to investigate the quality of the AlSb metamorphic buffer in terms of roughness, a structure formed by a 1 μm thick AlSb layer was grown on top of a 100 nm thick $In_{0.52}Al_{0.48}As$ layer on a semi insulating (001) InP substrate. AFM measurements performed on top of the AlSb layer showed an anisotropic surface RMS roughness of 0.73 nm and 1.60 nm along the [1$\bar{1}$0] and [110] directions, respectively. Furthermore, an equivalent structure was grown on a GaAs substrate, where the lattice mismatch between substrate and buffer is even higher. In this case the RMS roughness was 0.45 nm along the [1$\bar{1}$0] direction and 0.67 nm along the [110] direction. The AFM measurements of the top AlSb surface of the two structures are shown in Fig. 3.7. A different behaviour of the InP surface, compared to the GaAs surface, has also been found in [85]. The anisotropic roughness observed in the AlSb buffer is related to the anisotropy of the initial strain relaxation near the AlSb/InAlAs/InP interface and of diffusion lengths of adatoms along different crystallographic directions [86].

3.3 Test structures characterization

Test structures as TLM (Transfer Length Method), van der Pauw and Hall bar have been fabricated with different orientations and characterized in order to investigate the effect of the physical channel pinch on the electrical properties of the heterostructure. As can be seen in Table 3.1, TLM structures oriented along the three different directions have shown a strong dependence of the sheet resistance R_{sh} to the orientation of the material. The measured R_{sh} was 118±0.5 Ω/□ along the [1$\bar{1}$0] direction, while a higher value

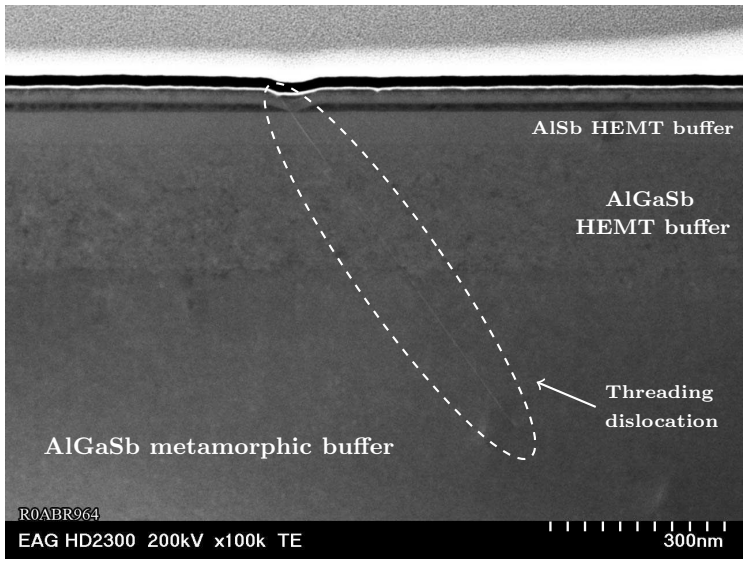


Fig. 3.5: STEM pictures of the InAs/AlSb HEMT cross-section cut along the direction [110], showing the threading dislocation starting in the AlSb metamorphic buffer.

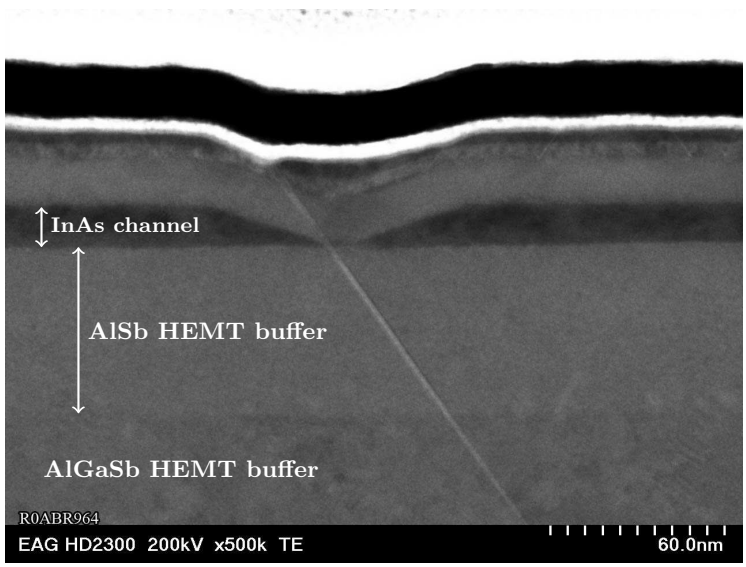


Fig. 3.6: STEM pictures of the InAs/AlSb HEMT cross-section cut along the direction [110], showing the pit in the channel and the threading dislocation.

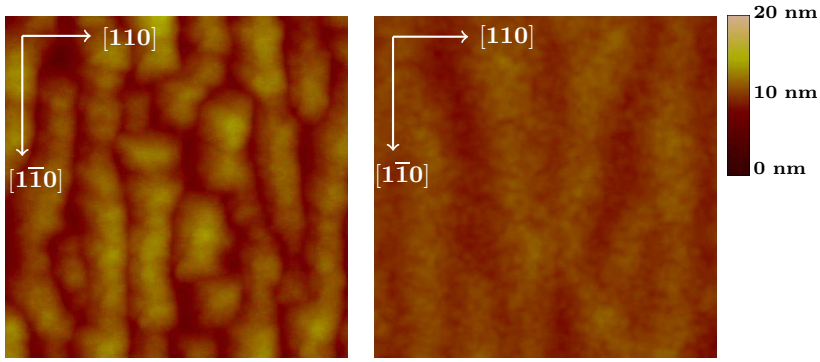


Fig. 3.7: AFM measurements (scaled to 1 μm × 1 μm) performed on top of the AlSb metamorphic buffer (a) grown on InP substrate and (b) grown on GaAs substrate (right).

of 174±0.9 Ω/□ was observed along the [110] direction. An intermediate R_{sh} value of 140±0.3 Ω/□ was measured along the diagonal direction [100]. The normalized contact resistance R_c and the specific contact resistivity ρ_c have also been extracted from TLM measurements, showing a negligible dependence to the orientation; See Table 3.1. Van der Pauw structures rotated at 45 degrees have also been characterized, showing an R_{sh} value of 143±1.3 Ω/□. These results are in good agreement with the TLM oriented along the diagonal direction [100].

Hall bar test structures have been fabricated along the three different orientations and characterized in a range of temperatures from 300 K down to 2 K. This gave direct information of the temperature dependence of the anisotropic behaviour. The electron mobility μ_n and the R_{sh} obtained from the Hall measurements are shown as a function of temperature in Fig. 3.8. The measured μ_n is higher along the [1$\bar{1}$0] direction compared to that measured along the [110] direction in the whole temperature range. Moreover, the anisotropy in the mobility is enhanced when reducing the temperature. Compared to 300 K, μ_n at 2 K is 178% higher along the [1$\bar{1}$0] direction and 59% higher along the [110] direction. Thus, at 2 K the scattering of electrons occurring

Table 3.1: Measurements results of TLM structures oriented along three different directions in the InAs/AlSb heterostructure.

TLM orientation	[1$\bar{1}$0]	[110]	[100]
R_{sh} (Ω/□)	118 ± 0.5	174 ± 0.9	140 ± 0.3
R_c (Ω·mm)	0.050 ± 0.002	0.045 ± 0.005	0.040 ± 0.001
ρ_c (10^{-7}Ω·cm^2)	2.17 ± 0.13	1.13 ± 0.18	1.15 ± 0.05

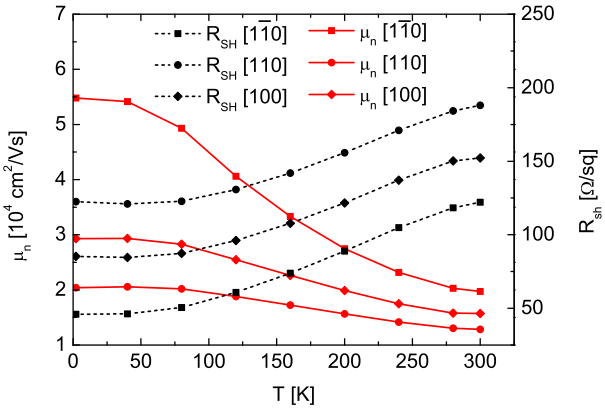
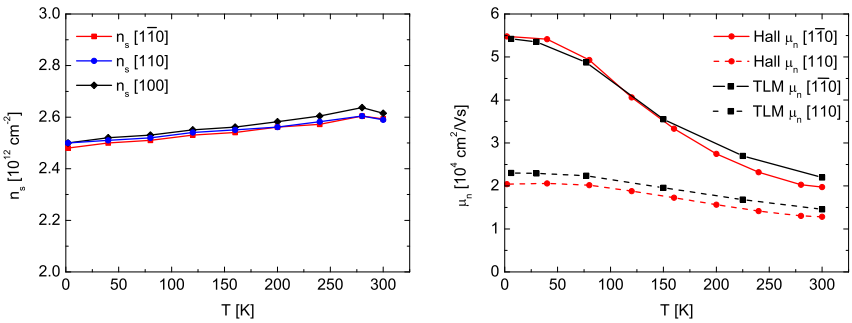


Fig. 3.8: R_{sh} and μ_n as a function of temperature for the crystal directions [1$\bar{1}$0], [110] and [100].



(a) (b)

Fig. 3.9: Behaviour as a function of temperature for (a) n_s and (b) Hall μ_n and calculated (from TLM data) μ_n along different crystal orientations.

against the asymmetric defects in the channel is the dominant mechanism. When the temperature is increased, the polar optical scattering [87] increases leading to a lower anisotropy in the mobility. As shown in Fig. 3.9(a), the sheet carrier density n_s in the channel, extracted from Hall bar measurements, is independent with respect to the orientation and shows a negligible variation (lower than 5%) when sweeping the temperature in the range between 2 K and 300 K. Since n_s is almost constant with temperature, the electron mobility in the channel can be extracted from TLM measurements through the following equation:

$$\mu_n = \frac{1}{q \cdot n_s \cdot R_{sh}} \tag{3.2}$$

where q is the elementary charge and R_{sh} is the sheet resistance obtained from the linear interpolation of TLM measurements. In Fig. 3.9(b), the Hall mobility as well as the mobility calculated from Eq. (3.2), considering

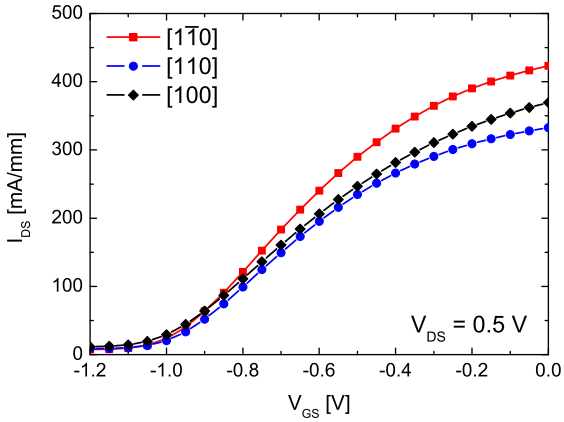


Fig. 3.10: $I_{DS}(V_{GS})$ at a drain voltage $V_{DS} = 0.5\,\mathrm{V}$ for InAs/AlSb HEMTs oriented along the directions [1$\bar{1}$0], [110] and [100].

$n_s \approx 2.55 \times 10^{12}\,\mathrm{cm}^{-2}$, are plotted along the [1$\bar{1}$0] and [110] orientations as a function of temperature. As expected from the negligible dependence of n_s with temperature, observed in Fig. 3.9(a), the two mobilities obtained from Hall and TLM data are very similar.

3.4 HEMT characterization

HEMT devices with gate width W_g of $2{\times}50\,\mu$m, L_g of $2\,\mu$m and with a source-drain distance of $5.6\,\mu$m were fabricated and characterized along the three different orientations, as in the case of TLM structures (a detailed description of the HEMT fabrication process will be reported in Chapter 4). The drain-source current as a function of gate-source voltage, $I_{DS}(V_{GS})$, of adjacent HEMT devices oriented along the three direction is shown in Fig. 3.10. In good agreement with the mobility measurements, the HEMT with the channel oriented along the [1$\bar{1}$0] direction exhibits the highest maximum I_{DS} of 420 mA/mm at a drain-source voltage, V_{DS}, of 0.5 V and $V_{GS} = 0\,\mathrm{V}$. In contrast, the HEMT with the channel oriented along the [110] direction shows a maximum I_{DS} of 330 mA/mm. The HEMT oriented along the diagonal [100] direction exhibits a maximum I_{DS} of about 375 mA/mm. The maximum I_{DS} for the HEMT oriented along this direction is hence a mean value compared to the two orthogonal directions. This is indeed related to the mobility behaviour as a function of orientation observed in Fig. 3.8. As a consequence, the transconductance g_m shows a dependence from the HEMT channel orientation as well. In Fig. 3.11, the g_m of the HEMT devices is plotted versus V_{GS}, showing peak g_m about 23% higher along the [1$\bar{1}$0] direction compared to the HEMT oriented along the [110] direction. The anisotropic electrical properties of the InAs/AlSb heterostructure are closely related to the elongated cracks. Since the cracks are along the [1$\bar{1}$0] direction, the scattering along the [110] direction is much larger than that along the [1$\bar{1}$0] direction, resulting in a lower electron mobility. Therefore, the presence of threading dislocation in

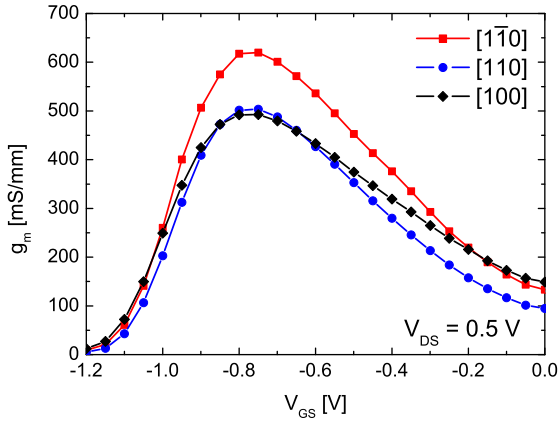


Fig. 3.11: $g_m(V_{GS})$ at a drain voltage $V_{DS} = 0.5\,\mathrm{V}$ for InAs/AlSb HEMTs oriented along the directions [1$\bar{1}$0], [110] and [100].

highly strained heterostructures, makes the choice of orientation in the HEMT channel crucial for achieving optimum device performances.

3.5 Summary

Anisotropic transport in InAs/AlSb heterostructures was discovered and investigated. A large anisotropy with 30% lower R_{sh} along the [1$\bar{1}$0] direction was measured using TLM structures. Hall bar measurements confirmed the anisotropy in R_{sh} and showed also an enhanced anisotropy in the electron mobility at 2 K. HEMT devices showed that the anisotropy is present in the channel. The electrical anisotropy has been related to the presence of cracks elongated in the [1$\bar{1}$0] direction. Furthermore, the investigation of the InAs/AlSb heterostructure cross-section showed that the cracks are related to the formation of threading dislocation in the relaxed AlSb metamorphic buffer. The anisotropic behaviour of HEMTs based on the InAs/AlSb heterostructure should be taken in to account when designing circuits for low-noise and low-power applications where high mobility and low channel resistance are needed. In addition, the enhanced anisotropy at cryogenic temperature makes the impact of this behaviour even more important for cryogenic LNA applications.

Chapter 4

InAs/AlSb HEMT Fabrication and Room Temperature Operation

The need for a thick AlSb metamorphic buffer for the epitaxial growth of pure InAs channel on InP or GaAs substrates introduces a number of challenges during the fabrication of InAs/AlSb HEMTs. The high chemical instability of the AlSb compound to air and chemicals seriously limits the yield as well as the reliability of the fabricated devices. This is indeed a critical issue for the realization of reliable circuits. In this chapter, the development of the InAs/AlSb HEMT fabrication process for high stability against oxidation and improved electrical performance is presented. Early-protection of the metamorphic buffer through deposition of silicon nitride (SiN_x) films with different techniques as well as the use of ion implantation will be described. The room temperature (300 K) device characteristics are shown as well.

4.1 Shallow-mesa technology

The fabrication process has been initially developed from a previous first-generation of InAs/AlSb HEMTs reported in [43, 88]. This process suffered from poor yield and unreliable HEMT characteristics associated with the degrading of samples in air. The process is based on five main processing steps where both optical and electron beam lithography (EBL) techniques are used. The fabrication process sequence is illustrated in Fig. 4.1.

1. **Electrical isolation:** The first step consists in the mesa isolation etch performed by a time-controlled Cl_2:Ar ICP/RIE dry etching process [88]. The patterns are defined using photoresist and optical lithography. This step is needed in order to achieve electrical isolation between adjacent devices as well as between the probing pads and the active region of the device. The dry etching is directly followed by a mesa-sidewall wet etching using a citric acid/H_2O_2 (1:1) solution to ensure the gate-to-channel electrical isolation at the mesa edge.

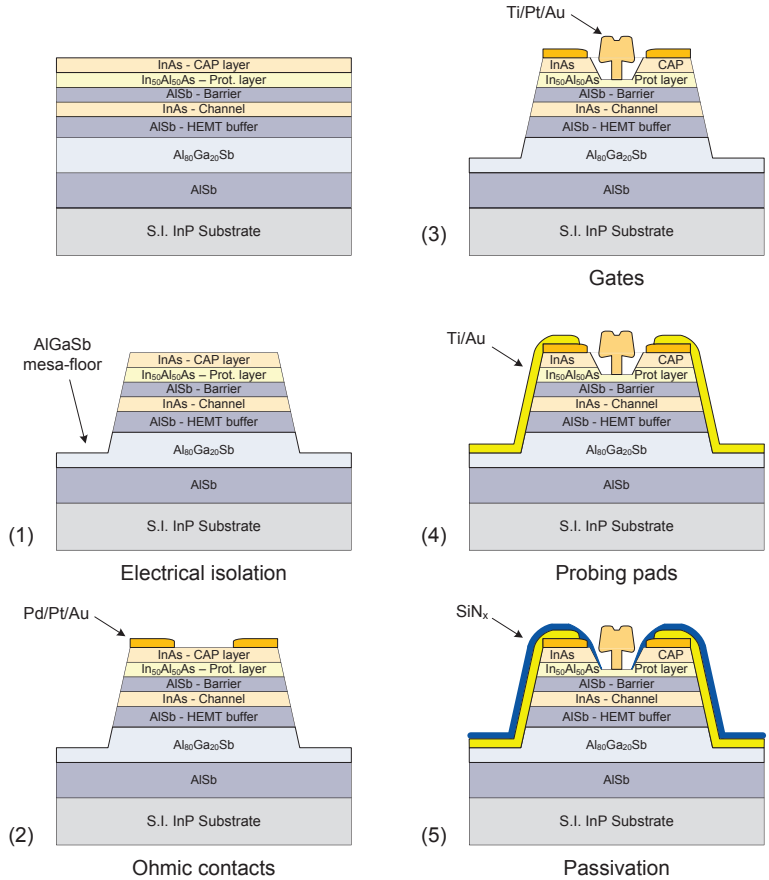
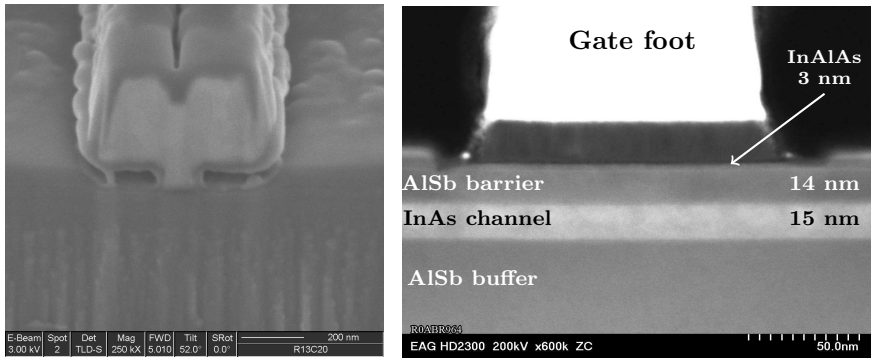


Fig. 4.1: Fabrication process sequence for shallow-mesa InAs/AlSb HEMT.

2. **Ohmic contacts:** After pattern definition by optical lithography, a Pd/Pt/Au metal stack is deposited by electron beam (e-beam) evaporation. Ohmic contacts are subsequently alloyed through thermal annealing at 275°C for 15 minutes in H_2/Ar (1:9) gas mixture in order to form the source and drain ohmic contacts of the HEMT. A low contact resistance R_c in the order of 0.05 Ω·mm is usually achieved. The typical source-to-drain distance is 2 μm.

3. **Gates:** Ti/Pt/Au T-shaped gates are defined using a two-layer resist by e-beam lithography. A gate-recess etch, selectively stopped on the InAlAs protection layer, is performed by a citric-acid based wet etchant prior to gate metallization [19]. Gate lengths of 110 nm and 80 nm were achieved. However, 80 nm devices are not reported in this thesis due to the non-optimized epitaxial structure which resulted in short channel effects.

4. **Probing pads:** A Ti/Au metal stack is deposited by reactive sputtering after pattern definition through optical lithography. The probing



(a) (b)

Fig. 4.2: (a) FIB-SEM picture of a 80 nm T-shaped gate of an InAs/AlSb HEMT. (b) STEM cross-section of a 110 nm InAs/AlSb HEMT. The InAs channel is clearly visible.

pads provide large area metallic connections needed for the electrical characterization of the device.

5. **Passivation:** Finally, a 80 nm thick SiN_x passivation layer is deposited through reactive sputtering. An ICP/RIE dry etching step is used to access the probing pads.

It is important to underline that the mesa etch for the electrical isolation step must stop in the relatively stable AlGaSb buffer in order to avoid exposure of the sensitive AlSb buffer to the subsequent processing steps. This is a critical step for the reliability of the device and requires an excellent control of the etch rate of the epilayers. A finalized InAs/AlSb HEMT with 80 nm gate footprint is illustrated by focused ion beam scanning electron microscope (FIB-SEM) in Fig. 4.2(a). The reduced thickness of the SiN_x passivation below the gate hat is due to the anisotropic nature of the sputtering technique used. The STEM device cross-section, including the gate foot, for a 110 nm InAs/AlSb HEMT is shown in Fig. 4.2(b). From the cross-sectional analysis it is clear that the gate-recess does not reach the AlSb Schottky barrier layer. This is essential in order to avoid a fast and uncontrolled oxidation process below the gate which can quickly deteriorate the device performance [19]. However, a compromise in etch depth should be chosen since a too shallow recess can lead to reduced pinch-off capability in addition to the degradation of the gate-length/gate-to-channel aspect ratio.

4.1.1 Early-protection by reactively sputtered SiN_x film

The extremely high tendency to oxidation of the AlSb material has lead to the introduction of the more chemically stable AlGaSb alloy in the buffer [36]. As discussed in the previous section, this allows the fabrication of InAs/AlSb HEMTs in a planar technology by etching shallow-mesa down to the AlGaSb layer for electrical isolation of the transistors. However, the AlGaSb layer reduces the electrical resistivity of the buffer [42], leading to a tradeoff between

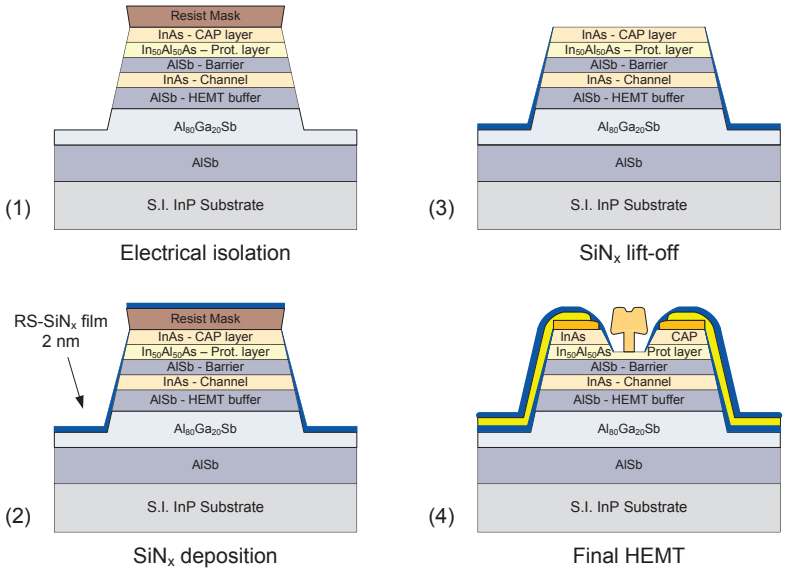
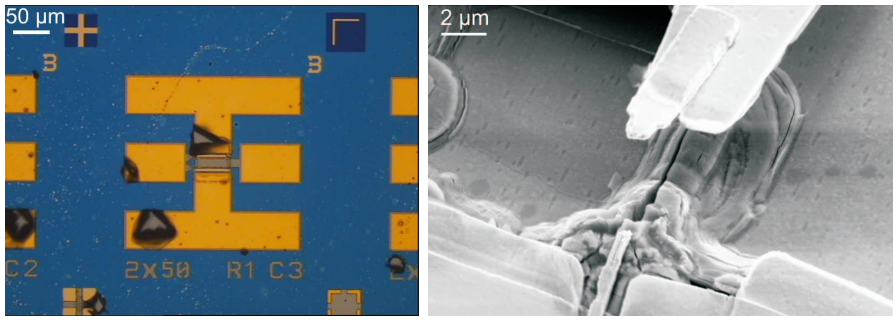


Fig. 4.3: Fabrication process schematic showing the deposition and subsequent lift-off from the active region of the early SiN_x film protection layer. The schematic of the final InAs/AlSb HEMT protected with the early passivation is also shown.

electrical performance and stability against oxidation. In order to maximize the electrical performance of the HEMT, the residual AlGaSb layer thickness must be minimized by stopping the mesa isolation etch as close as possible to the bottom AlSb/AlGaSb interface. This may lead to strong oxidation of the mesa floor in case of a non-uniform thickness and/or etch of the epilayers. Moreover, the use of the AlGaSb layer does not ensure long term stability of the devices [89]. Even though the AlGaSb alloy is more chemically stable than AlSb, oxidation of the AlGaSb mesa floor has been observed in the devices fabricated according to the process flow described in Section 4.1. This oxidation leaded to the progressive destruction of fabricated devices within a few months.

Wafer level packaging (WLP) techniques have been used by Chou *et al.* in [89] for improving the stability against oxidation of InAs/AlSb HEMTs. However, details about the WLP fabrication process have not been revealed. The problem of the chemical instability of InAs/AlSb HEMTs has also been recently addressed by Lin *et al.* in [90] by depositing, right after the exposure of the AlGaSb during the shallow-mesa etch step, a 5 nm SiO_2 layer by e-beam evaporation. The instability of the AlGaSb layer in ambient was initially addressed at Chalmers in 2008 by depositing, right after the shallow-mesa etch for electrical isolation (first step discussed in Section 4.1), a 2 nm thick SiN_x film by reactive sputtering (RS) [91]. As shown in step 2 of Fig. 4.3, the SiN_x film is deposited with the active regions of the future devices still covered by the 1 μm thick resist pattern used during the dry etching. In order to avoid the encapsulation of the resist, the thickness of the film is kept about 500 times lower than the resist mask. This allows lateral dissolution of the resist and



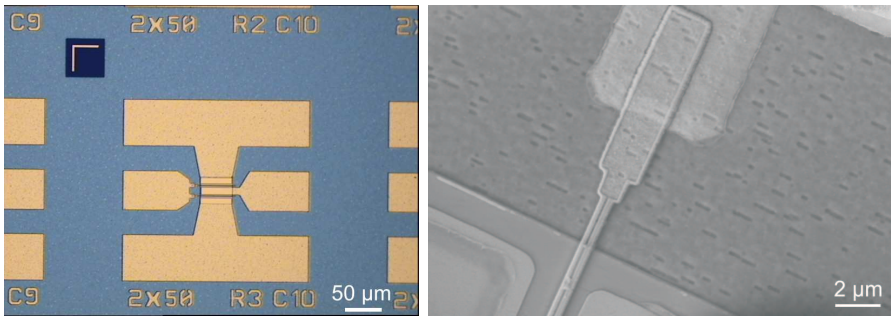
(a) (b)

Fig. 4.4: (a) Optical micrograph and (b) SEM picture of 2×50 μm InAs/AlSb HEMTs protected with the RS-SiN_x film illustrating the point-like oxidation of the AlGaSb surface observed using the RS-SiN_x process.

hence lift-off of the SiN_x film from the active region of the HEMT; See step 3 in Fig. 4.3. The AlGaSb mesa floor as well as the mesa sidewalls composed by the highly reactive AlSb layers are instead protected by the SiN_x film. The subsequent process steps are unchanged compared to the conventional HEMT fabrication process discussed in Section 4.1.

The early RS-SiN_x deposition is a first attempt to introduce a SiN_x film protection in the fabrication process of InAs/AlSb HEMTs based on shallow-mesa technology. This approach, even if it brings valuable improvements in term of long term stability, can be further improved. First, the exposure to air of the AlGaSb surface prior to its protection with a thin film is a contradiction in principle, whatever the selected material and deposition method [90, 91]. Moreover, through the experience of several batches processed with the use of the early RS-SiN_x film, it appeared that this technological approach does not always achieve a long term stability. Oxidation of AlGaSb and AlSb materials sometimes take place as illustrated in Fig. 4.4(a).

The observed oxidation of processed InAs/AlSb HEMTs is ascribed to the presence of pits in the InAs channel, discussed in Chapter 3, which act as preferential etching places during the shallow-mesa dry etching. The masking effect of the pits leads to large elongated cracks on the exposed surface of the AlGaSb buffer. These cracks are clearly visible in the SEM picture shown in Fig. 4.4(b). Their depth is estimated to be in the 10-50 nm range from SEM and atomic force microscopy measurements. This, in combination with their elongated shape, can induce a shadowing effect during the RS-SiN_x film deposition. As a consequence, the coverage of a 2 nm thin SiN_x film and the related efficiency of its protection is not guaranteed at these particular places. Moreover, due to the depth of the cracks, it could also happen that the highly reactive AlSb metamorphic buffer is exposed in these places since the mesa dry etching needs to be stopped as close as possible to the bottom interface of the AlGaSb layer. The use of a thicker film appears as a logical solution. However, attempts using the reactive sputtering method failed due to issue during the lift-off of the resist mask, likely because of its encapsulation by the RS-SiN_x film.



(a) (b)

Fig. 4.5: (a) Optical micrograph and (b) SEM picture of 2×50 μm InAs/AlSb HEMTs protected with the *in-situ* CVD-SiN_x film. The devices show no oxidation thanks to the *in-situ* process as well as to the improved coverage of the cracks on the AlGaSb surface.

4.1.2 Early-protection by *in-situ* CVD SiN_x-film

A solution to the oxidation issues is the *in-situ* deposition of a thicker SiN_x-film directly after the dry-etching step. In this way any exposure to air or chemicals is avoided, whereas a thicker coverage ensures an efficient protection even in case of cracks on the buffer. This has been done by using a dual chamber Oxford Plasmalab system tool, where a 25 nm thick SiN_x-film is deposited through chemical vapor deposition (CVD) in one chamber right after the shallow-mesa dry etching was performed in the adjacent chamber. The transfer between the two chambers is under vacuum. The process sequence is the same as in the case of the RS fabrication process showed in Fig. 4.3. Optical microscopy and SEM images of an InAs/AlSb HEMT based on the *in-situ* CVD process are shown in Fig. 4.5.

Unlike the RS-method, the increase of the SiN_x-film thickness up to 25 nm did not induce any issues of resist encapsulation when the CVD process was used. Even with a thickness ratio against the 1 μm thick photoresist of only 40, compared to 500 for the 2 nm RS-SiN_x film, a successful lift-off was obtained. The higher SiN_x film thickness achieved with the *in-situ* CVD process is also crucial during the gate-recess wet etch performed prior to gate metallization. The citric-acid based wet etchant used for the etch of the InAs cap layer underneath the gate causes a strong oxidation of the metamorphic buffer which in turn mechanically destroys the gate fingers; See Fig. 4.4(b). The better coverage of the cracks ensured by the *in-situ* CVD process also suppresses the oxidation phenomena shown in the SEM image of Fig. 4.4(b). Hence, the development of the *in-situ* CVD-SiN_x process allows the fabrication of InAs/AlSb HEMTs with very high stability against oxidation. Devices fabricated with this process did not show any sign of oxidation so far, 2 and a half years after their fabrication.

The long term stability ensured by the *in-situ* CVD-SiN_x process is utilized in the first cryogenic InAs/AlSb HEMT LNA demonstrated in this thesis and discussed in Chapter 6.

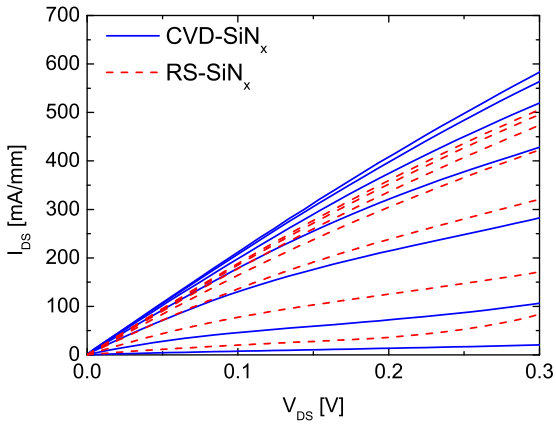


Fig. 4.6: $I_{DS}(V_{DS})$ with V_{GS} ranging from 0 V to -1.2 V for InAs/AlSb HEMTs protected with a RS-SiN$_x$ or an *in-situ* CVD-SiN$_x$ film. The devices have a gate width of 2×50 μm.

4.2 RS- versus CVD-SiN$_x$ HEMTs: Electrical characterization

The electrical performance at room temperature of InAs/AlSb HEMTs with L_g of 110 nm based either on the RS-SiN$_x$ or the CVD-SiN$_x$ fabrication process has been investigated. All the transistor measurements were limited to a V_{DS} up to 0.3 V as a higher value results in irreversible device degradation detrimental for low-noise application. The degradation is likely caused by impact ionization and has been observed independently of fabrication process, also for other devices without SiN$_x$ film protection. The output characteristics of the HEMTs based on the two different fabrication processes are shown in Fig. 4.6. In both cases, a large output conductance g_{DS} and no saturation of I_{DS} for V_{GS} close to 0 V is observed. The lack of I_{DS} saturation at room temperature is consistent with other InAs/AlSb HEMTs in the literature [5, 19, 92] and can be attributed to hole accumulation in the metamorphic buffer below the InAs channel [44].

At 0.3 V, the device based on the CVD-SiN$_x$ process exhibits an I_{on}/I_{off} ratio of 28, whereas the RS-SiN$_x$ process achieves a lower I_{on}/I_{off} ratio of 6. Therefore, a better pinch-off of the current is demonstrated by the CVD-SiN$_x$ HEMT. This can be related to the improved coverage of the conductive AlGaSb mesa floor, through the thicker film of the CVD-SiN$_x$ process which lead to a better electrical isolation between the extrinsic part of the gate fingers and the AlGaSb layer. A schematic of the extrinsic part of the gate electrode on top of the passivation is illustrated in Fig. 4.7. In Fig. 4.8, a schematic view of the HEMT shows the presence of the entire heterostructure underneath the probing pads. This layout has been developed in order to improve the adhesion of the pads. A poor adhesion of the pad metallization has been observed when depositing it directly on top of the SiN$_x$ film, impeding the wire-bonding of the HEMTs in hybrid circuits. This layout allowed the mounting and wire-bonding of CVD-SiN$_x$ HEMT devices in the hybrid LNA demonstrated in

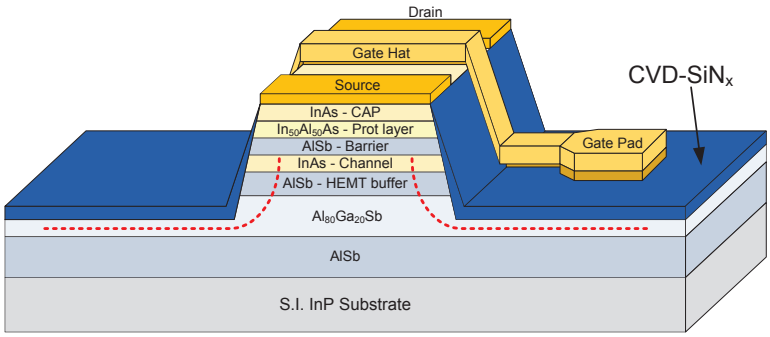


Fig. 4.7: Schematic view of the InAs/AlSb HEMT active region showing the extrinsic part of the gate finger on top of the passivation. The higher thickness of the CVD-SiN_x film improves the electrical isolation between gate electrode and the conductive AlGaSb mesa floor.

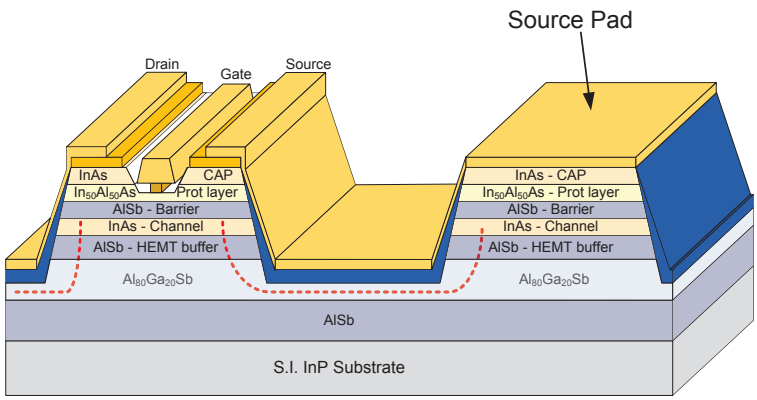


Fig. 4.8: Schematic view of the pads metallization with the heterostructure underneath for improving the metal adhesion. A leakage path through the AlGaSb buffer reduces the pinch-off capability of the HEMT.

Chapter 6. However, such layout leads to the drawback of a conductive path between the pads and the HEMT channel through the AlGaSb layer; See illustration in Fig. 4.8. This path can degrade the pinch-off of the drain current if the residual thickness of the AlGaSb layer in the etched regions is not small enough. This explains why the pinch-off of the CVD-SiN_x HEMT, even if strongly improved compared to the RS-SiN_x HEMT, is still not excellent. Poor pinch-off of InAs/AlSb HEMTs based on the same epitaxial structure has also been observed in [93]. In the optical microscopy picture of Fig. 4.9(a) a device based on the CVD-SiN_x process, but with additional deep mesa trenches etched between the active region and the mesas underneath the pads, is shown. In these trenches, the AlGaSb buffer has been etched almost completely, leading to a strong improvement of the current pinch-off and to an I_{on}/I_{off} ratio of 330 at room temperature; See Fig. 4.9(b).

An important observation for the device based on the CVD-SiN_x process

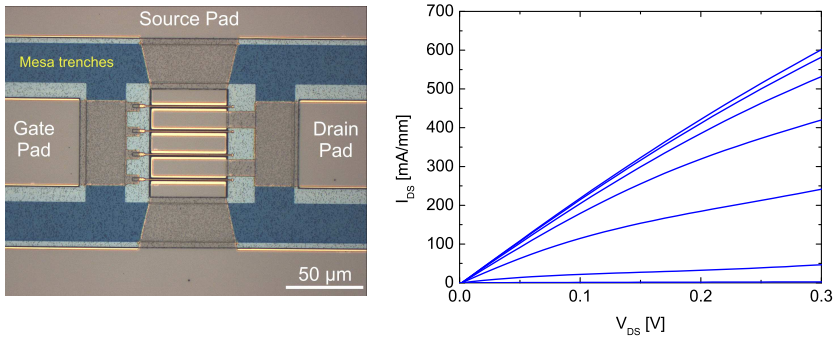


Fig. 4.9: (a) Optical micrograph of a 4×50 μm InAs/AlSb HEMT protected with the *in-situ* CVD-SiN$_x$ film and with mesa trenches for improved electrical isolation. (b) $I_{DS}(V_{DS})$ with V_{GS} ranging from 0 V to -1.2 V of a 2×50 μm CVD-SiN$_x$ HEMT with mesa trenches.

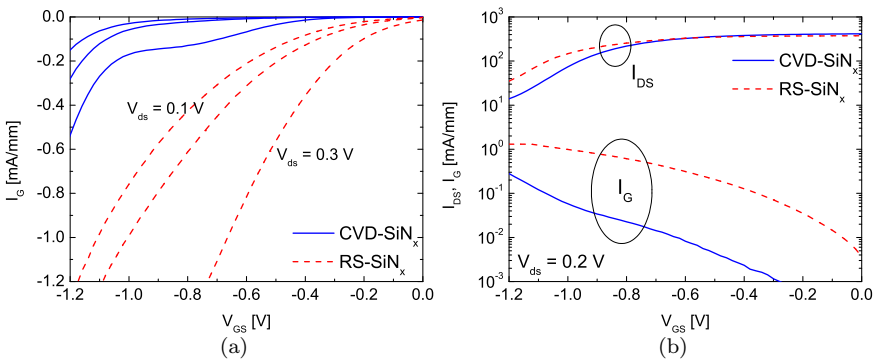


Fig. 4.10: (a) $I_G(V_{GS})$ with V_{DS} ranging from 0.1 V to 0.3 V in steps of 0.1 V and (b) subthreshold gate and drain current characteristics at $V_{DS} = 0.2$ V for InAs/AlSb HEMTs protected with a RS-SiN$_x$ or an *in-situ* CVD-SiN$_x$ film.

is that the gate leakage current I_G is reduced up to one order of magnitude, compared to the RS-SiN$_x$ process. In Fig. 4.10(a) I_G is plotted versus V_{GS} at V_{DS} of 0.1, 0.2 and 0.3 V for the two different devices. Therefore, the overall improvement in the DC performance for the CVD-SiN$_x$ process with respect to the RS-SiN$_x$ process can be understood to be due to the thicker SiN$_x$-film. This improves not only the process reliability in term of protection against the AlSb-based materials oxidation, but also the electrical isolation between the extrinsic part of the gate and the source and drain probing pads. In Fig. 4.10(b), I_{DS} and I_G are plotted versus V_{GS} in logarithmic scale for the V_{DS} bias of 0.2 V. Due to the better electrical isolation with the AlGaSb buffer, the main contribution to I_G is the Schottky current through the barrier.

The subthreshold slope S, extracted from the linear region of $I_{DS}(V_{GS})$

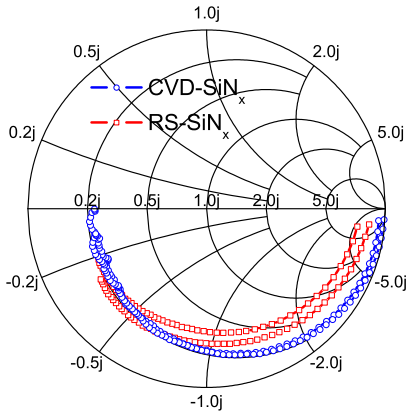


Fig. 4.11: Input reflection coefficient S_{11} at drain bias V_{DS} of 0.1 V and 0.3 V for InAs/AlSb HEMTs protected with a RS-SiN_x or an *in-situ* CVD-SiN_x film. The frequency is ranging from 1 to 55 GHz.

[94], is reduced from 300 mV/dec for the RS-SiN_x device to 260 mV/dec, confirming the improved gate control when using the CVD-SiN_x process. Moreover, in the HEMTs with deep mesa trenches (see Fig. 4.9), S reaches values of 140 mV/dec.

4.2.1 RF characterization

On-wafer S-parameter measurements have been performed up to a frequency of 50 GHz. In Fig. 4.11, the input reflection coefficient S_{11} at V_{DS} of 0.1 V and 0.3 V is shown for both processes. At a low frequency of 1 GHz, the CVD-SiN_x HEMT shows higher input impedance already at a low drain bias of 0.1 V, as well as a much smaller variation of the input impedance when increasing V_{DS} up to 0.3 V. The decrease in the input impedance with increasing drain bias has been modeled in [17] using the shunt R_{gs} and R_{gd} resistors. At V_{DS} = 0.3 V, the CVD-SiN_x device exhibits R_{gs} and R_{gd} values of 55 kΩ and 20 kΩ respectively, revealing a much better isolation resistance than for the RS-SiN_x device, which shows corresponding values of 4.3 kΩ and 1.8 kΩ. These results confirm the improved steady-state behavior of the devices when using a thicker SiN_x film in the CVD process. The dominant mechanism for the input impedance lowering in the case of the CVD-SiN_x device appears to be related to the Schottky and impact ionization components of I_G. For the RS-SiN_x device, the input impedance lowering is partly related to these two components of I_G, but the main contribution is ascribed to the leakage around the device mesa through the AlGaSb layer. The thick CVD-SiN_x film induces a larger horizontal capacitance. The values extracted from small-signal modeling shows 50% larger pad capacitances C_{pg}/C_{pd} (15 fF) at 0.3 V for the CVD-SiN_x device. This explains the reduced difference in S_{11} at high frequency between the two types of devices observed in Fig. 4.11.

In Fig. 4.12, the current gain $|h_{21}|^2$ and the Mason's gain U are plotted versus frequency at 0.2 V. The f_T and f_{max} values are extracted from $|h_{21}|^2$

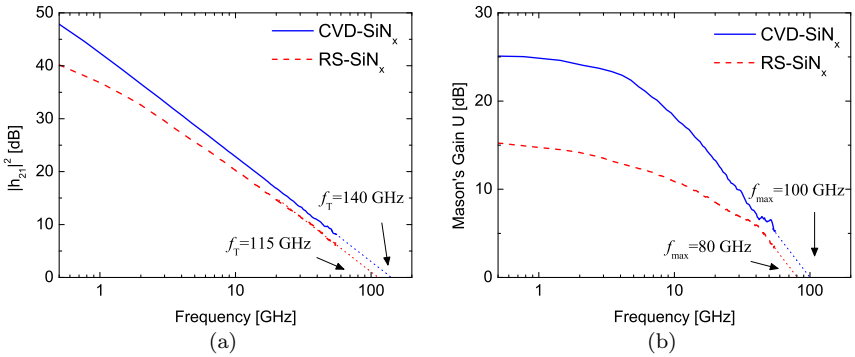


Fig. 4.12: Evolution versus frequency at $V_{DS} = 0.2\,\text{V}$ of (a) the current gain $|h_{21}|^2$ and (b) the Mason's gain U for InAs/AlSb HEMTs protected with a RS-SiN$_x$ or an *in-situ* CVD-SiN$_x$ film.

and U, respectively, using a -20 dB/decade slope. Compared to the RS-SiN$_x$ device, the CVD-SiN$_x$ HEMT exhibits a 22% higher value of f_T (from 115 GHz to 140 GHz) and a 25% higher value of f_{max} (from 80 GHz to 100 GHz). The improvement of f_T and f_{max} can be related to the better pinch-off, to the lower output conductance and to the one order of magnitude lower gate current leakage ensured by the thicker SiN$_x$ film used with the CVD process. The Mason's gain U is 70% higher for the CVD-SiN$_x$ device at 1 GHz (25 dB instead of 14.7 dB), but the difference is reduced for frequencies above 5 GHz. This again shows that a thicker SiN$_x$-film provides a benefit mainly in the low frequency range, whereas its advantages vanish at higher frequencies due to the horizontal capacitance between the metallic pads.

4.2.2 Noise characterization

Noise measurements have been performed using an Agilent N9030A noise figure analyzer. The measured noise figure at 50 Ω, $NF_{50\Omega}$, is shown in Fig. 4.13(a) in the frequency range from 6 GHz to 18 GHz and for $V_{DS} = 0.2\,\text{V}$. This bias was selected since impact ionization becomes dominant at higher V_{DS} values, degrading the noise figure. The standing wave pattern observed in the measurements is due to the not optimal matching to 50 Ω of the 2×50 μm device layout at the measured frequencies. From S-parameter measurements, the small-signal model for both devices has been obtained using the direct extraction method [95, 96]. Thereafter, by fitting the $NF_{50\Omega}$ measurements with the noise from the small-signal model, a noise model for each device has been obtained using the Pospieszalski method [97]. At 12 GHz, the modeled $NF_{50\Omega}$ for the RS-SiN$_x$ device is 4 dB whereas the CVD-SiN$_x$ device shows, at the same drain bias and frequency, an $NF_{50\Omega}$ of 2.8 dB. In Fig. 4.13(b), the minimum noise figure NF_{min} is plotted versus frequency for the RS- and CVD-SiN$_x$ devices, showing values of NF_{min} in, respectively, the 2.3-2.8 dB and 1.4-2 dB ranges at 0.2 V and for frequency between 6 and 18 GHz. The improvement in $NF_{50\Omega}$ and NF_{min} (up to 40%) observed in the CVD-SiN$_x$

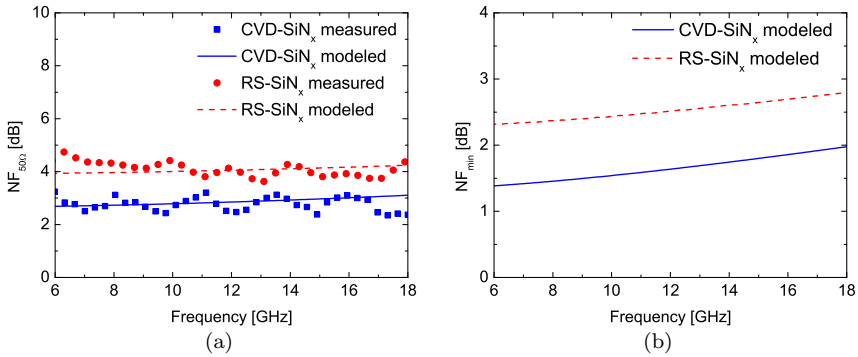


Fig. 4.13: Evolution versus frequency at $V_{DS} = 0.2\,\mathrm{V}$ of (a) the measured and modeled $NF_{50\Omega}$ and (b) the modeled NF_{min} for InAs/AlSb HEMTs protected with a RS-SiN$_x$ or an *in-situ* CVD-SiN$_x$ film.

device is ascribed to the much lower total gate current, the better pinch-off behavior and the lower g_{DS}.

4.3 True planar technology

The shallow-mesa technology with an *in-situ* CVD-SiN$_x$ film has demonstrated large improvements in terms of device stability against oxidation and electrical performance. However, as described in Section 4.2, this technique requires an extremely accurate control of the depth during the mesa etch for electrical isolation. The AlGaSb buffer layer creates a leakage path which can deteriorate the overall electrical performance of the device depending on its residual thickness after the etch. Another drawback of the CVD-SiN$_x$ film is due to the increased horizontal capacitance between the metallic pads which can degrade the high frequency performance of the device. Good electrical isolation can alternatively be achieved by etching the AlSb buffer down to the substrate, thus employing an air-bridge gate technology [14,92,98,99]. This technology is however not feasible for integration in MMIC applications due to the very large thickness ($> 1\ \mu$m) of the AlSb metamorphic buffer which makes the realization of passive components very challenging. Moreover, the stability against oxidation at the deep mesa walls is questionable. Air-bridge gate InAs/AlSb HEMTs have been fabricated during this thesis work, showing poor long term reliability since the oxidation taking place in the AlSb mesa walls mechanically destroyed the gate electrodes and thus the whole devices; See Fig. 4.14.

A radically different approach for device isolation, originally proposed by Werking *et al.* [100], consists of implantation of ions through the heterostructure. The most important advantage of this method is that the highly reactive AlSb and AlGaSb layers are never exposed to ambient since no physical etch is required. This can basically allow the fabrication of oxidation-resistant InAs/AlSb HEMTs without the need of *in-situ* SiN$_x$ films. Moreover, the planar nature of the this method enables the use of InAs/AlSb HEMTs in MMIC applications. However, poor electrical isolation and thus low DC performance

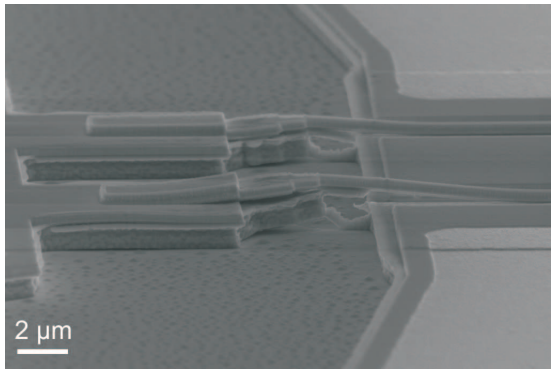


Fig. 4.14: SEM image of a 2×50 μm InAs/AlSb HEMT with air-bridge gates, four months after fabrication. Even if passivated with a 80 nm thick SiN_x film right after the mesa etch, oxidation at the AlSb mesa walls lifted the gate electrodes leading to the destruction of most devices on the wafer.

were reported in the literature for ion implanted InAs/AlSb HEMT prior to this thesis work [100]. The authors concluded that a physical mesa etch is required in order to achieve a suitable electrical isolation. In this thesis work, planar InAs/AlSb HEMTs based on the ion implantation for device isolation with state-of-the-art DC and RF performance were demonstrated.

4.3.1 Implantation process development

The InAs channel is the most critical layer to be damaged by the ion implantation process in order to achieve the highest electrical isolation. Simulations with TRIM [101] software have been carried out in order to find the correct ion species to be implanted and their associated implantation energy. Ar ions have been chosen due to their large mass compared to H or He which were penetrating too far in the heterostructure and creating thus a too low damage in the channel. Ar ions also produce a broader distribution of the damage and require substantially lower dose in order to reach the same damage as He ions. As can be seen in Fig. 4.15, for energy levels of 50 keV and 100 keV, the maximum number of displacements per atom (DPA) reaches values above 5 in this layer. This pronounced peak of the DPA is presumably due to a larger nuclear stopping power in the InAs material. The 100 keV energy level was chosen because of the higher damage in the buffer layer as well.

In order to find the optimal dose of Ar ions needed to achieve the highest isolation, several doses ranging from $1\times10^{13}\,cm^{-2}$ to $1\times10^{16}\,cm^{-2}$ were tested. The isolation resistance as a function of the implantation dose has been characterized through dedicated test structures patterned by using optical lithography. A detailed description of these test structures can be found in Paper [E]. The measured sheet resistance of the bombarded regions, right after the implantation, increases with the dose but is still below $10^5\,\Omega$/sq, probably due to hopping conductivity caused by traps [102]; See Fig. 4.16(a). However, a thermal treatment of the implanted samples leads to a strong variation of the isolation resistance. Samples implanted with low doses show a degrada-

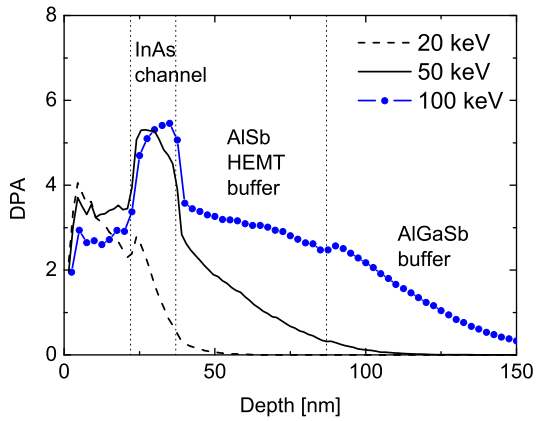
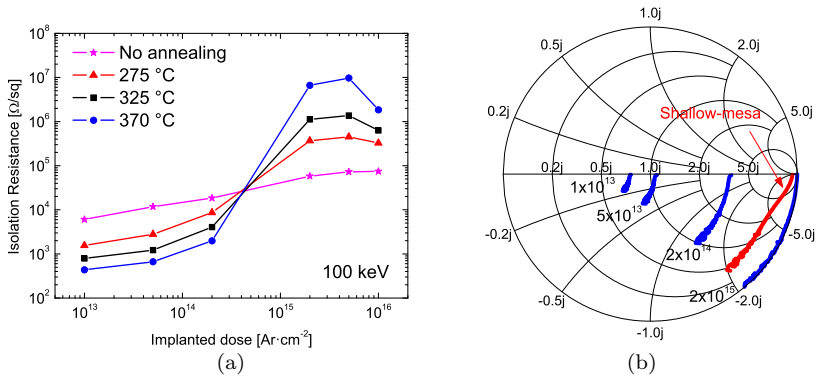


Fig. 4.15: TRIM simulated displacements per atom versus depth in the InAs/AlSb HEMT heterostructure for Ar ion implantation with energy levels of 20, 50 and 100 keV.



(a) (b)

Fig. 4.16: (a) Isolation sheet resistance versus implantation dose for different annealing temperatures. (b) Input reflection coefficient S_{11} for isolation test structures implanted with doses of 1×10^{13}, 5×10^{13}, 2×10^{14} and $2\times10^{15}\,\mathrm{cm}^{-2}$ after annealing at 370 °C. The measured S_{11} for a CVD-SiN_x shallow-mesa technology is also shown in red.

tion of the isolation. This happens because the damage induced by the Ar bombardment is annealed out. An opposite behavior of the isolation after annealing is observed for high doses ($\geq 2\times10^{15}\,\mathrm{cm}^{-2}$) and a maximum sheet resistance slightly above $10^7\,\Omega$/sq is achieved when annealing at 370 °C. An increase of the isolation resistance after annealing was reported for an InGaAs HEMT with Ar ions implantation [103]. S-parameter measurements on the test structures shows a good electrical isolation also in RF operation, better than using a CVD-SiN_x shallow-mesa technology, for the dose of $2\times10^{15}\,\mathrm{cm}^{-2}$; See Fig. 4.16(b). The ion implantation technology does not need the use of the thick SiN_x film responsible for the increase in the horizontal capacitance. Another crucial advantage of the ion implantation technology is that the use of

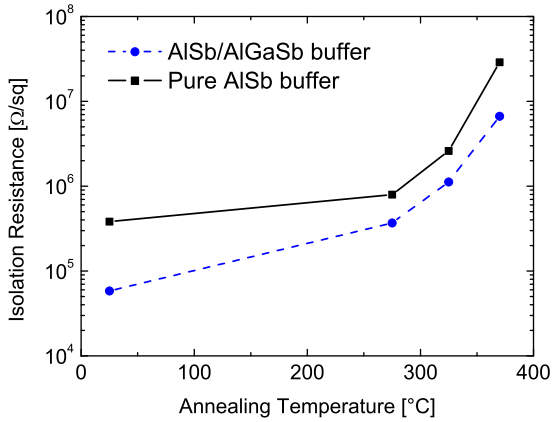


Fig. 4.17: Isolation sheet resistance versus annealing temperature for implanted InAs/AlSb heterostructures with mixed AlSb/AlGaSb as well as with pure AlSb buffer. The implantation energy and dose are 100 keV and 2×10^{15} cm^{-2}, respectively.

the conductive AlGaSb buffer layer can be avoided since the Sb-based epilayers are never exposed to ambient. This, as demonstrated by Fig. 4.17, allows a further increase of the electrical isolation of the buffer and thus can enhance the overall performance of devices based on this technology.

In order to investigate the damage induced by the ion bombardment through the heterostructure, suitable test structures for cross-sectional analysis have been fabricated. The test structures are formed by adjacent Au strips defined by electron beam lithography with both width and separation ranging from 100 nm to 1 μm. These strips act as implantation masks allowing implantation of only a small area of the heterostructure. Thanks to the larger stopping power of Au, compared to resist, a significantly thinner mask can be used allowing a better resolution for pattern definition. Moreover, an Au mask is much more radiation tolerant and, hence, can withstand higher implantation doses compared to resist. In order to protect the heterostructure during the mask fabrication and removal, a 70 nm thick SiN film was deposited prior to the Au mask definition. A STEM cross-section of such a test structure is shown in Fig. 4.18. From the close up view shown in Fig. 4.19 a different contrast is observed in the epitaxial layers not protected by the implantation mask during the ion bombardment. Energy dispersive spectroscopy (EDS) analysis showed traces of In and As in the AlSb barrier and traces of Al and Sb in the InAs channel. This may explain the color variation of the implanted area and is most likely due to the atom rearrangement caused by the collisions of the Ar ions. Fig. 4.19 clearly shows that the damage reaches a depth of about 50 nm, which is below the InAs channel as expected from the electrical measurements. The lateral spreading of the damage is approximately 40 nm with respect to the bottom opening of the mask. However, due to the V-shape of the Au strips, an accurate estimation of the lateral spreading cannot be done. The damage induced in the crystal structure of the InAs channel is clearly visible in the high resolution STEM image of Fig. 4.20. Even though the electrical characterization showed an isolation level comparable and even

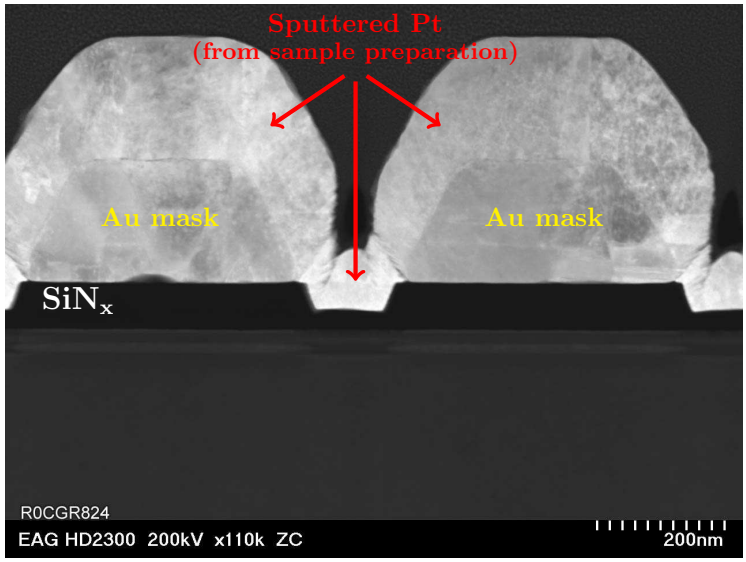


Fig. 4.18: STEM cross-section of the Au mask strips and epitaxial layers underneath. Pt coating has been applied during the sample preparation for STEM analysis.

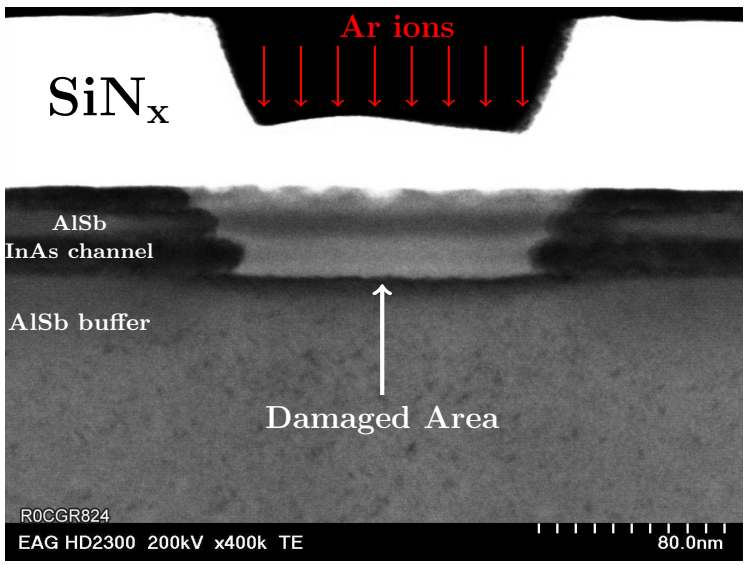


Fig. 4.19: Close up view of the epitaxial layers exposed to the Ar ions implantation. The sample was implanted with dose and energy of $2\times10^{15}\,\mathrm{cm}^{-2}$ and 100 keV, respectively.

better than that achieved by the the shallow-mesa technology, experiments with multiple implantation energies have been carried out in order to further improve the isolation. The use of several ions energies can achieve a deeper isolation region. Test samples were implanted with multiple energies of 70-

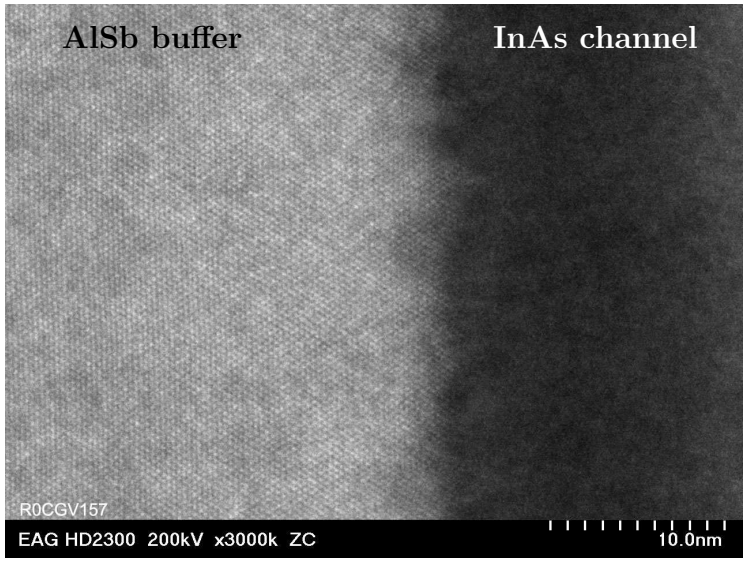


Fig. 4.20: High resolution STEM image showing the atomic layered structure in the region of AlSb buffer not reached by the implanted Ar ions. The InAs channel does not show atomic patterning due to the large crystal damage induced by the ion implantation. Note that the image is 90 degrees rotated compared to Fig. 4.19

120-240 keV and with doses ranging from 3×10^{15} to $9\times10^{15}\,\mathrm{cm}^{-2}$. The use of such high energies in combination with high doses was enabled by the developed Au mask. Although a better isolation resistance was expected, the first test was not successful as the measured isolation was found to be lower than that achieved with the implantation at single energy of 100 keV. Further development will be required in order to push the isolation level closer to that achieved by the air-bridge gate technology.

4.3.2 Ion implanted InAs/AlSb HEMTs

Since high level of electrical isolation were demonstrated by the developed ion implantation, this technique was directly implemented in the HEMT process. The fabrication process for ion implanted InAs/AlSb HEMTs is essentially the same as the standard process described in Section 4.1. The only difference consists in the bombardment with ions, rather than etching the epilayers below the channel, during the first step. The active areas of the future HEMT devices are first protected by a photoresist mask and Ar ions are implanted at the Ion Technolgy Centre, Uppsala University [104], with a dose of $2\times10^{15}\,\mathrm{cm}^{-2}$ and an energy level of 100 keV. Thereafter, a thermal annealing at 370 °C is performed for enhancing the electrical isolation. All the subsequent processing steps are identical to those described in Section 4.1.

The DC output characteristic of a $2\times20\,\mu$m InAs/AlSb HEMT with L_g of 110 nm and fabricated on an heterostructure with mixed AlSb/AlGaSb buffer is shown in Fig. 4.21(a). The device shows the same lack of I_{DS} saturation as observed in shallow-mesa and air-bridge gate technologies [5, 19, 92]. The cur-

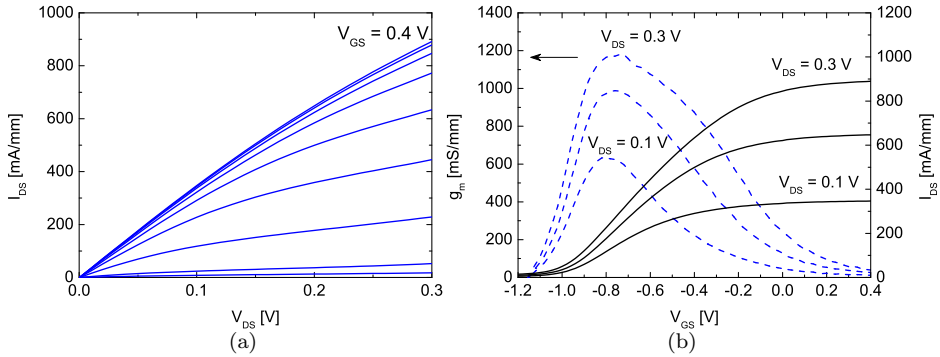


Fig. 4.21: (a) $I_{DS}(V_{DS})$ with V_{GS} ranging from -1.2 V to 0.4 V for a 2×20 μm ion implanted InAs/AlSb HEMT. (b) I_{DS} and g_m as functions of V_{GS} with V_{DS} of 0.1, 0.2, and 0.3 V

rent pinch-off has an I_{on}/I_{off} ratio of 52 which is higher than that achieved by the CVD-SiN_x HEMT with no deep mesa trenches discussed in Section 4.2. A further improvement of the I_{on}/I_{off} ratio is expected for future ion implanted HEMTs fabricated on heterostructures with pure AlSb buffer. Moreover, further development of the ion implantation process with multiple implantation energy will also contribute in achieving higher I_{on}/I_{off} ratios. Nevertheless, the pinch-off demonstrated is by far better than that reported in [100] thanks to the high electrical isolation of this developed technology. In Fig. 4.21(b), I_{DS} and g_m are plotted versus V_{GS} for V_{DS} biases of 0.1, 0.2, and 0.3 V. The device shows a peak g_m of 630 mS/mm at a drain bias of only 0.1 V. At 0.3 V, the peak g_m reaches a value of 1180 mS/mm. The HEMT also shows a maximum gate leakage current below 0.5 mA/mm at the highest drain bias of 0.3 V. The high frequency performance of the ion implanted InAs/AlSb HEMT was also measured. As shown in Fig. 4.22 the device exhibits, at a V_{DS} of 0.3 V, f_T and f_{max} of 210 GHz and 180 GHz, respectively. The DC power, P_{DC}, dissipated in the device at this bias is 80 mW/mm. The DC and RF performance of the ion implanted HEMT are thus comparable to state-of-the-art InAs/AlSb HEMTs with similar gate length but based on shallow-mesa or air-bridge gate technology. A comparison of f_T for this device against published values in the literature can be found in Fig. 3(b) of Paper [D]. This is the first demonstration of a working InAs/AlSb HEMT based on ion implantation isolation technology.

4.3.3 Lateral Optimization

The overall electrical performance of a HEMT is strongly related to the extrinsic source and drain resistances, R_s and R_d [105, 106]. High values of R_s and R_d can severely limit the low-power and low-noise capabilities of InAs/AlSb HEMTs. One approach to reduce R_s and R_d consist in the scaling of the source-drain distance d_{sd}. Ion implanted InAs/AlSb HEMTs with d_{sd} ranging from 2.5 μm, down to 1 μm were fabricated and compared. Electron beam

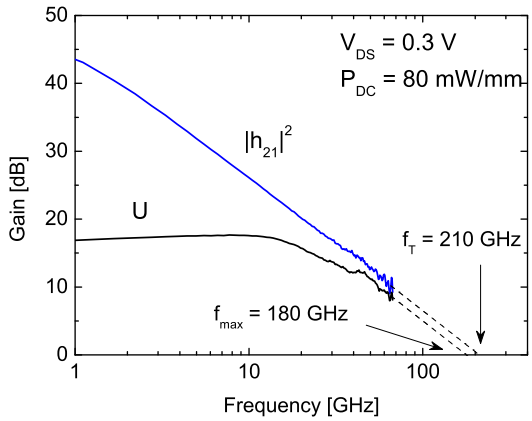


Fig. 4.22: Measured $|h_{21}|^2$ and U at V_{DS} = 0.3 V and V_{GS} = -0.75 V. The extrapolated values of f_T and f_{max} are 210 and 180 GHz, respectively.

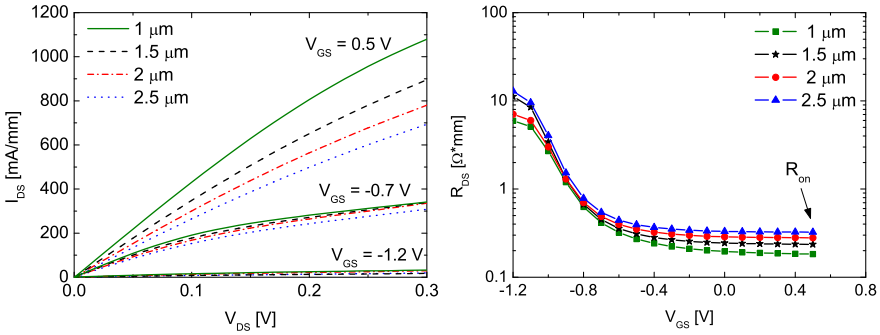
lithography was used for the definition of ohmic contacts. In Fig. 4.23, the output characteristics as well as the access resistance R_{DS} are shown as a function of V_{GS} for devices with different values of d_{sd}. When d_{sd} is scaled from 2.5 μm to 2 μm, 1.5 μm and 1 μm, the maximum I_{DS}, at V_{DS} of 0.3 V, increases by 12%, 29% and 56%, respectively. Moreover, the on-resistance R_{on}, given by the access resistance R_{DS} at high gate voltage, scales with d_{sd}, ranging from 0.32 Ω·mm down to 0.18 Ω·mm when d_{sd} is scaled from 2.5 μm to 1 μm. As a result, f_T is improved by 32%. However, as discussed in Paper [F], a trade-off in terms of pinch-off, gate leakage and unilateral gain is observed when scaling d_{sd} below 1.5 μm. In Table 4.1, R_{on} as well as the most important small-signal parameters are summarized.

Table 4.1: R_{on} and small-signal model parameters (at V_{DS} = 0.3 V) for ion implanted InAs/AlSb HEMTs with different d_{sd}.

Parameter	d_{sd} = 1 μm	d_{sd} = 1.5 μm	d_{sd} = 2 μm	d_{sd} = 2.5 μm
R_{on} [Ω·mm]	0.18	0.23	0.28	0.32
R_s [Ω·mm]	0.08	0.1	0.116	0.14
R_d [Ω·mm]	0.096	0.124	0.152	0.172
g_{mi} [mS/mm]	1450	1425	1330	1350
g_{ds} [mS/mm]	520	500	450	425
C_{gs} [fF/mm]	945	825	800	730
C_{gd} [fF/mm]	500	375	350	320
C_{ds} [fF/mm]	1000	850	600	455

4.4 Summary

The development of the shallow-mesa and ion implanted technology for InAs/AlSb HEMTs with high stability against oxidation and state-of-the-art electrical



(a) (b)

Fig. 4.23: (a) $I_{DS}(V_{DS})$ and (b) $R_{DS}(V_{GS})$ for $2{\times}20\,\mu$m ion implanted InAs/AlSb HEMTs with d_{sd} ranging from $2.5\,\mu$m, down to $1\,\mu$m. The on-resistance R_{on} is extracted at $V_{GS} = 0.5\,$V.

performance was carried out. The shallow-mesa technology based on the *in-situ* CVD-SiN_x process demonstrated a strong improvement of the device reliability as well as better electrical performance in terms of pinch-off, gate current leakage and f_T/f_{max}, compared to a standard shallow-mesa process. However, the real breakthrough for the InAs/AlSb HEMT was the first demonstration of a working ion implantation process for this device technology. The ion implantation for device isolation enables oxidation-resistant HEMTs since the highly reactive AlSb layers are never exposed to air and processing steps. Moreover, this technique also allows fabricating InAs/AlSb HEMTs in structures with a pure AlSb metamorphic buffer, hence omitting the conductive AlGaSb layer. This will lead to further improvements in isolation and, hence, to better electrical performance. The combination of the properties described above with the planar nature of the ion implanted technology and with the excellent DC and RF performances demonstrated in this work, paves the way for reliable InAs/AlSb HEMT based MMICs.

Chapter 5

InAs/AlSb HEMT cryogenic operation

The absence of carrier freeze-out [107] as well as the transport improvement in the 2DEG at cryogenic temperatures make the HEMT a suitable device for cryogenic applications. The low temperature behaviour of InAs/AlSb HEMTs has not been extensively reported prior to this thesis work. In this chapter, the cryogenic DC, RF and noise performance of shallow-mesa InAs/AlSb HEMTs is investigated and compared to operation at room temperature (300 K). An equivalent trend upon cooling was observed for HEMT isolated with ion implantation which are therefore not reported in this chapter. Furthermore, a comparison between InAs/AlSb HEMT and the mature InP HEMT technology is presented.

5.1 DC characterization

The DC measurements were performed on-wafer at 300 K, 77 K and at 6 K using a LakeShore cryogenic probestation and a HP4156B semiconductor parameter analyzer. The output characteristic for an InAs/AlSb HEMT based on shallow-mesa isolation with *in-situ* CVD-SiN_x passivation is shown in Fig. 5.1. No noticeable current saturation is observed at 300 K resulting in a high output conductance. This resistor-like behavior of the device could be due to accumulation of holes in the metamorphic buffer [44,108,109]. When the temperature is reduced down to 77 K and 6 K, the device performance is greatly improved as can be seen in Fig. 5.1. At low temperatures, higher electric field in the gate is needed for the impact ionization phenomena to occur [22] and therefore the number of holes which accumulate beneath the InAs channel is lower when V_{GS} is close to 0 V. As a result, an improved saturation of the drain current is clearly observed as the temperature is reduced. At $V_{GS} = 0$ V and $V_{DS} = 0.3$ V, g_{DS} decreases from 338 mS/mm at 300 K to 94 mS/mm at 6 K. The impact ionization is shifted toward more negative V_{GS}, leading to a slight kink effect that can be recognized at drain voltages above 0.2 V. This behavior is observed in all HEMTs fabricated either with shallow-mesa (Paper [B]) or ion implantation technology (Paper [E]). The I_{on}/I_{off} ratio

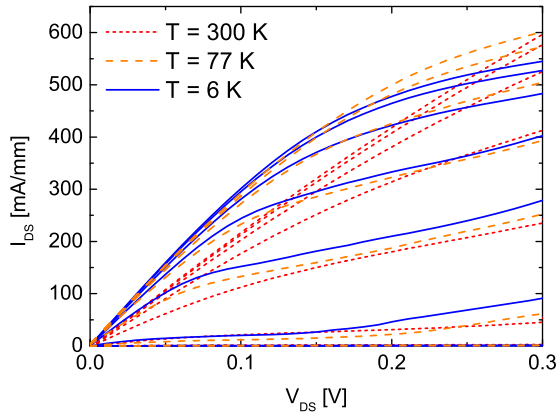


Fig. 5.1: $I_D(V_{DS})$ at 300 K, 77 K and 6 K with gate voltage V_{GS} ranging from -1.3 V to 0 V. The device gate width is 2×50 μm.

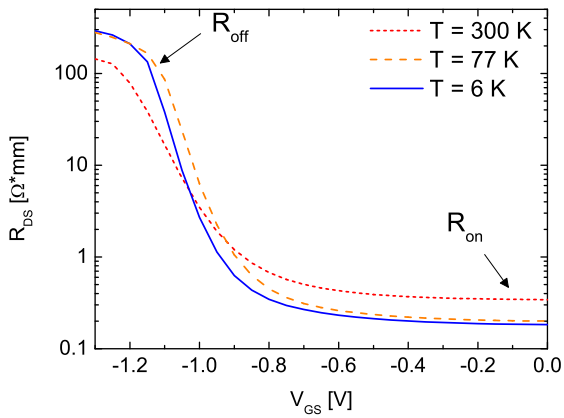


Fig. 5.2: $R_{DS}(V_{GS})$ at 300 K, 77 K and 6 K measured at a V_{DS} bias of 10 mV.

increases from 330 at 300 K up to 770 at both 77 K and 6 K.

The measured R_{on} decreases from 0.34 Ω·mm at 300 K, to 0.18 Ω·mm at 6 K. The improvement of R_{on} is related to the reduction of the access resistance due to transport improvement in the channel at low temperature. In Fig. 5.2, the DC R_{DS} is plotted as a function of V_{GS} at the three different temperatures, showing the trend of R_{on}. The negative V_{GS} bias was not increased further than -1.3 V in order to avoid device degradation due to breakdown. The channel resistance at pinch-off ($V_{GS} = -1.3$ V), R_{off}, is also increased as the temperature is lowered. Moreover, no significant difference is observed between 77 K and 6 K. R_{off} is 144 Ω·mm, 279 Ω·mm and 292 Ω·mm at 300 K, 77 K and 6 K, respectively.

The dependence of the gate leakage current with temperature and bias is shown in Fig. 5.3. The total gate current is formed of two main components; the hole current component generated in the narrow bandgap InAs channel due

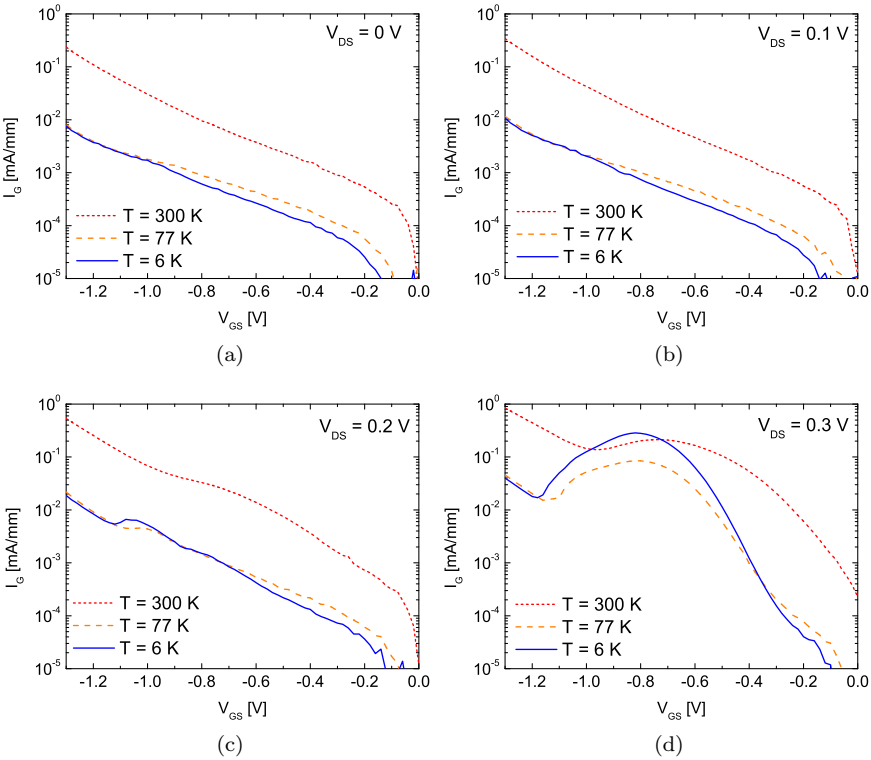


Fig. 5.3: $I_G(V_{GS})$ with drain voltage V_{DS} ranging from 0 V to 0.3 V at 300 K, 77 K and 6 K.

to the impact ionization effect, and the Schottky leakage current component governed by thermal and tunneling electrons flowing above and/or through the AlSb barrier [110]. From Fig. 5.3(a) and 5.3(b), it is clear that the impact ionization is negligible in the whole range of V_{GS} for V_{DS} up to 0.1 V. At this bias the dominant component of the gate current is the Schottky leakage, which is more than one order of magnitude lower compared to 300 K. The Schottky component reduction of the gate leakage is attributed to the lower energy of the electrons and hence to the lower thermionic emission of electrons over the barrier [111] at low temperature. At 0.2 V (Fig. 5.3(c)), the impact ionization component starts to be visible in I_G for all the three temperatures. When increasing V_{DS} up to 0.3 V, the impact ionization component becomes the dominant part of the gate current, as indicated by the bell-shaped behavior in Fig. 5.3(d). Moreover, at the lowest temperature of 6 K, the total gate current is even larger compared to that at 300 K due to the large impact ionization. This is probably due to the reduced electron scattering with phonons, and hence to the higher mobility, at low temperature. It is also important to note how the bell-shape in I_G is shifted towards more negative values of V_{GS} when the temperature is reduced. In the region where V_{GS} is close to 0 V, no bell-shape is observed at both 77 K and 6 K, in contrast to the 300 K curve.

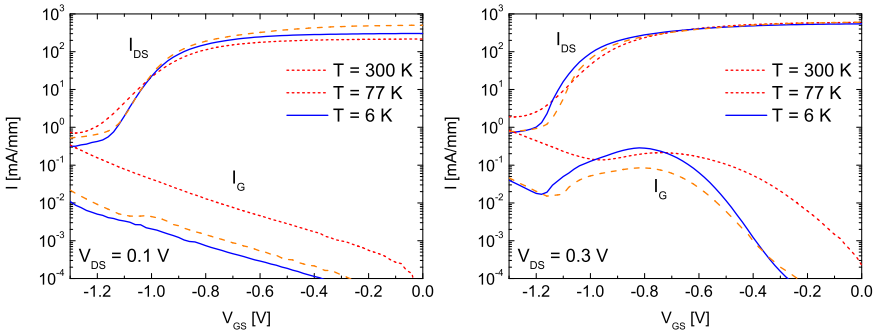


Fig. 5.4: $I_{DS}(V_{GS})$ and $I_G(V_{GS})$ for drain voltage V_{DS} of (a) 0.1 V and of (b) 0.3 V at 300 K, 77 K and 6 K.

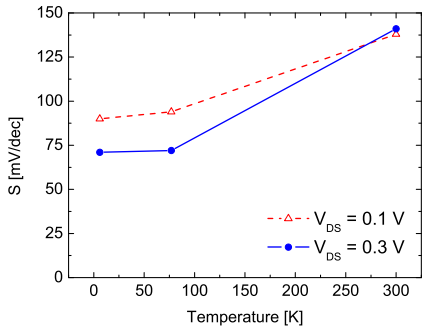


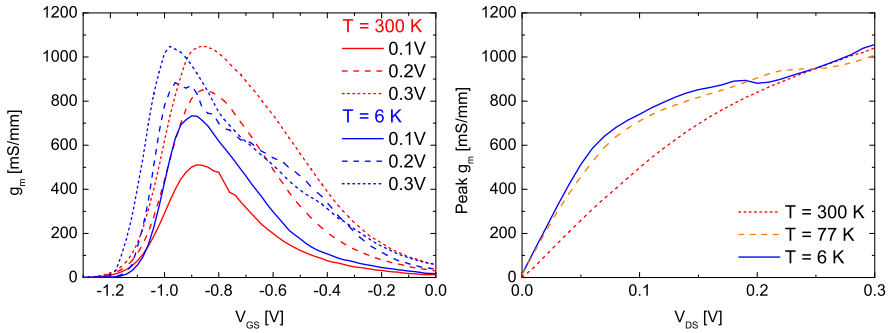
Fig. 5.5: Subthreshold slope S as a function of temperature for V_{DS} biases of 0.1 V and 0.3 V.

This is consistent to the saturation improvement of I_{DS} observed at cryogenic temperatures and for V_{GS} values close to 0 V as shown in Fig. 5.1.

The improvement in the subthreshold region for both I_{DS} and I_G characteristics upon cooling is evident in Fig. 5.4. For large negative V_{GS} values the impact ionization becomes negligible since the concentration of electrons in the channel is very small. It is interesting to observe that the minimum subthreshold drain current is dominated by Schottky gate leakage at 300 K. At cryogenic temperatures, the subthreshold drain current is about 50% lower due to the improved Schottky component of I_G. However, at the highest bias of 0.3 V, the impact ionization leads to an increased drain current in the V_{GS} range -1.15 to -0.4 V; See Fig. 5.4(b). This can also be observed in Fig. 5.1.

At 300 K, the subthreshold slope is 140 mV/dec at V_{DS} up to 0.3 V. When cooling to 6 K, a minimum S of 70 mV/dec is measured, thanks to the lower Schottky gate leakage under cryogenic operation described above. Fig. 5.5 shows S as a function of the operating temperature at different drain biases.

The measured transconductance g_m versus V_{GS} is shown in Fig. 5.6(a). Because of the lower access resistance and of the enhanced electron mobility,



(a) (b)

Fig. 5.6: (a) $g_m(V_{GS})$ at 300 K and 6 K for drain voltages of 0.1 V, 0.2 V and 0.3 V. (b) Peak $g_m(V_{DS})$ at 300 K, 77 K and 6 K.

the peak value of g_m is expected to be higher at 6 K. However due to the enhanced impact ionization effect, the increase in g_m becomes less as V_{DS} is increased. At 0.1 V, the peak g_m is 43% higher (733 mS/mm) than its value at 300 K. When increasing V_{DS} to 0.2 V, the increase in peak g_m is only 2%. At 0.3 V the two peaks are equal at 300 K and 6 K and approximately 1050 mS/mm. Generally it is observed that the peaks are moved to lower gate voltages at cryogenic temperatures due to impact ionization. Furthermore, the g_m curve at 6 K and 0.3 V exhibits a shoulder known also as "impact ionization transconductance" [15]. The improvement of the peak g_m upon cooling, mainly at low bias, is clearly visible in Fig. 5.6(b). This behavior, together with the reduced I_G and R_{on}, shows that, for low V_{DS} ($\sim$ 0.1 V), the DC performances of the InAs/AlSb HEMT are significantly improved upon cooling.

5.2 RF characterization

S-parameters measurements of the CVD-SiN_x HEMT were performed on-wafer at 300 K and at 6 K. The current gain $|h_{21}|^2$ and Mason's gain U are shown for three different V_{DS} values at each temperature in Fig. 5.7. At 300 K, interesting observations can be made. First, due to impact ionization, U does not show any improvement in the low frequency region when increasing V_{DS} from 0.2 V to 0.3 V. U overcomes its value at 0.2 V when the frequency is above 2 GHz. This is due to the fact that impact ionization influences the RF performance of the device mainly at low frequency, because of the lower hole velocity, compared to that of the electrons [112]. A large amount of holes tend to accumulate in the drain side of the buffer underneath the InAs channel [44]. Another important observation in the behavior at 300 K is that $|h_{21}|^2$ at high frequency is significantly higher compared to U at the same drain bias. This leads to f_T/f_{max} ratios lower than 1.

Measurements performed at 6 K show a large improvement of both $|h_{21}|^2$ and U at the lowest bias of 0.1 V, compared to 300 K; See Fig. 5.7(b). This is consistent with the enhanced peak g_m mainly at low V_{DS} observed in

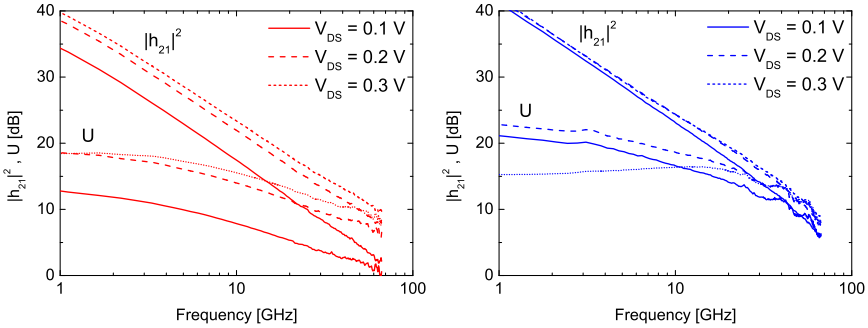


Fig. 5.7: Mason's gain U and current gain $|h_{21}|^2$ for a CVD-SiN$_x$ InAs/AlSb HEMT (a) at 300 K and (b) at 6 K for $V_{DS} = 0.1$ V, 0.2 V and 0.3 V.

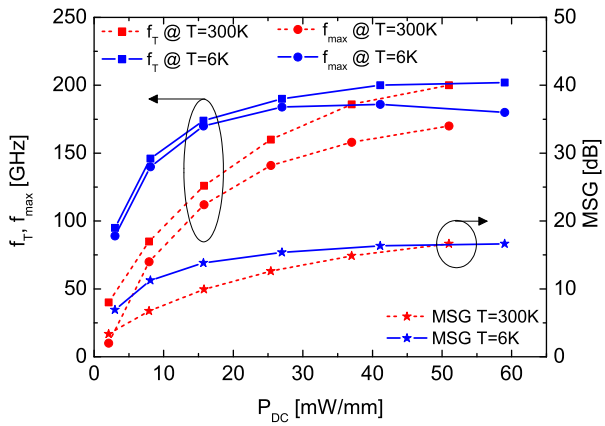


Fig. 5.8: f_T, f_{max} and MSG at 300 K and 6 K. V_{DS} is swept from 0.1 V to 0.3 V in steps of 0.05 V. The MSG is measured at 40 GHz.

Fig. 5.6(b). Moreover, it is interesting to observe the reduced difference between $|h_{21}|^2$ and U at high frequency which leads to an improved f_T/f_{max} ratio upon cooling. However, due to the large impact ionization occurring at 6 K and for $V_{DS} = 0.3$ V, U is reduced more than 7 dB at low frequency. At this bias, U becomes higher compared to the value at 0.2 V for frequencies above 30 GHz. Thus, the impact ionization influence on the RF performance is extended to a wider frequency range at low temperatures.

f_T, f_{max} and the maximum stable gain MSG at 40 GHz are shown as a function of P_{DC} in Fig. 5.8. It is possible to observe that below 40 mW/mm all three parameters increase with P_{DC} irrespective of temperature. Moreover, f_T, f_{max} and MSG are all significantly higher at 6 K than at 300 K in the low power range. A very strong increase in f_T (+72%) and f_{max} (+100%) at a low P_{DC} of about 8 mW/mm is observed at 6 K. This is mainly explained by the increased peak g_m and lower output conductance at low drain bias upon

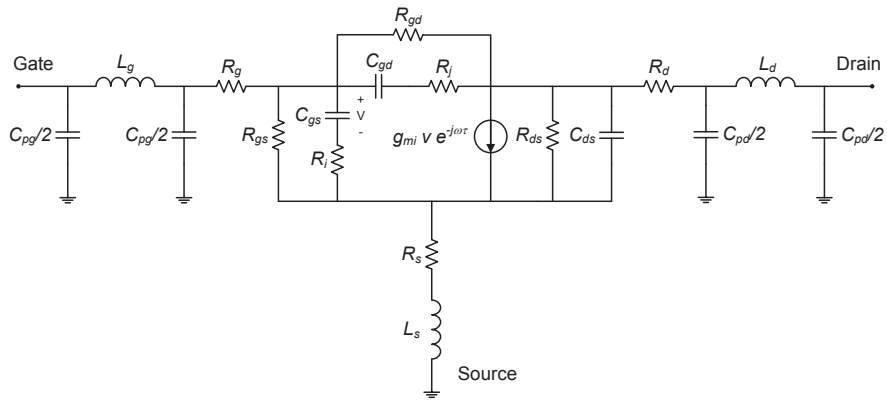


Fig. 5.9: Small-signal model of the InAs/AlSb HEMT.

cooling. Moreover, the improved f_T/f_{max} ratio at low temperature and in the low power range is clear in Fig. 5.8. At a higher P_{DC} of about 25 mW/mm, f_T and f_{max} show a smaller improvement of +19% and +30%, respectively. The improvement in both f_T and f_{max} upon cooling becomes negligible when increasing P_{DC} up to 50-60 mW/mm ($V_{DS} = 0.3$ V). This is indeed related to the reduced improvement of peak g_m upon cooling observed at 0.3 V. Peak f_T and f_{max} of, respectively, 200 GHz and 180 GHz are measured at this bias.

5.2.1 Small-signal modeling

The InAs/AlSb HEMT modeling was carried out through the direct extraction method reported in [95, 96]. The small-signal model (SSM) used at both room and cryogenic temperature is presented in Fig. 5.9. Two shunt resistances R_{gd} and R_{gs} are included in order to model the relatively high Schottky gate leakage current [17]. In Table 5.1 the extracted intrinsic small-signal parameters are summarized at 300 K and 6 K. It is interesting to observe the reduction upon cooling of the small-signal output conductance, g_{ds}, also at high V_{DS} of 0.3 V. This behaviour, opposite to that of g_{DS} observed from DC measurements, is explained by the lower influence of holes at high frequency. The extrinsic resistances show a strong dependence with temperature

Table 5.1: Intrinsic small-signal parameters at 300 K and 6 K for V_{DS} of 0.1 V, 0.2 V and 0.3 V.

T [K]	V_{DS} [V]	g_{mi} [mS/mm]	g_{ds} [mS/mm]	C_{gs} [fF/mm]	C_{gd} [fF/mm]	C_{ds} [fF/mm]
300	0.1	665	940	600	355	825
	0.2	1015	430	645	315	840
	0.3	1200	320	690	285	815
6	0.1	930	450	585	335	975
	0.2	1110	300	640	295	1140
	0.3	1150	275	700	270	1210

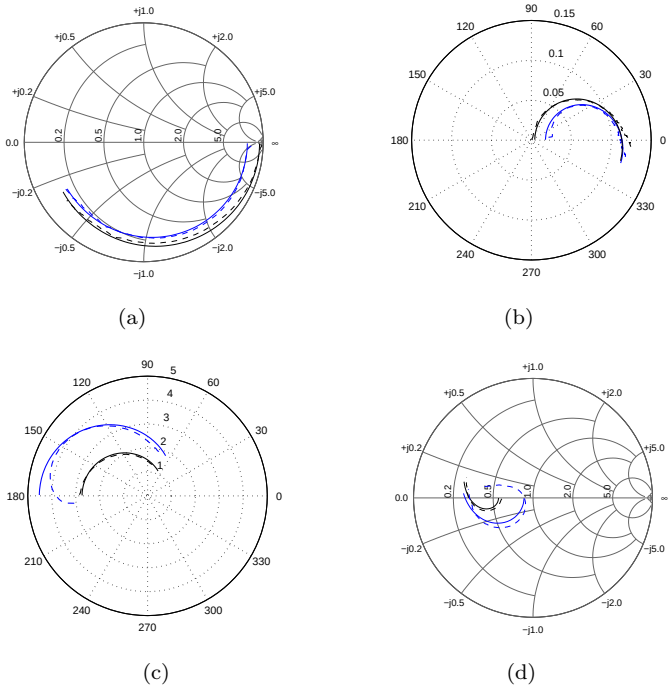


Fig. 5.10: Measured S-parameters (dash) versus model (solid) at 6 K for V_{DS} = 0.1 V (black) and 0.3 V (blue). (a) S_{11}, (b) S_{12}, (c) S_{21}, (d) S_{22}.

as expected. The extrinsic gate resistance R_g is reduced from 10 Ω/mm down to 3 Ω/mm when cooling. Dedicated gate resistance test structure, adjacent to the transistors, have been implemented in order to accurately extract R_g values. Moreover, the drain and source resistances R_d and R_s are 50% lower at 6 K. The reduction of the extrinsic resistances contributes to the improved f_T and f_{max} of the device when operating at cryogenic temperature.

Fig. 5.10 shows the measured and modeled S-parameters at V_{DS} of 0.1 V and 0.3 V in the frequency range 0.1-40 GHz. Because of the enhanced gate leakage due to impact ionization, the measured S_{11} is pulled towards lower impedance in the Smith chart at 0.3 V. Note that the measurements were performed at a V_{GS} bias of -0.9 V, *i.e.* where the impact ionization is dominant. Moreover, the enhanced I_G occurring at this bias produces a large inductive behavior in S_{22} as well as a reduction of S_{21} at low frequency. Therefore, a high accuracy of the InAs/AlSb HEMT model becomes more difficult to achieve under cryogenic operation for high V_{DS} values. The deviation of the model from the actual measured device is evaluated through the use of the normalized error function ε defined as [113]:

$$\varepsilon = \frac{1}{4N} \sum_{j=1}^{2} \sum_{i=1}^{2} \frac{1}{\max|S_{ij}^{\text{meas}}|^2} \sum_{k=1}^{N} |S_{ij}^{\text{meas}}(k) - S_{ij}^{\text{model}}(k)|^2 \qquad (5.1)$$

where N represents the number of frequency points whereas, S_{ij}^{model} and S_{ij}^{meas}

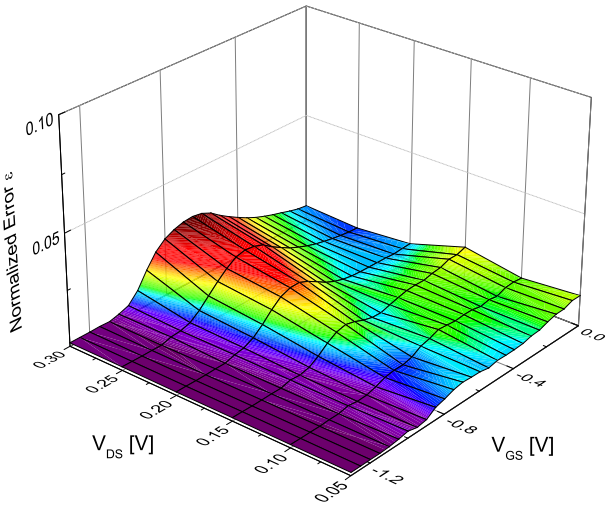


Fig. 5.11: Normalized error of the extracted model as a function of V_{DS} and V_{GS} at 6 K.

are the modeled and the measured S-parameter, respectively. The normalized error as a function of gate and drain biases is shown in Fig. 5.11. The effect of the impact ionization leads to an increased ε and thus to lower accuracy of the model for high V_{DS} and for -1.1 $\leq V_{GS} \leq$ -0.4 V.

5.3 Noise characterization and modeling

The 50 Ω noise figure $NF_{50\Omega}$ of a 2×50 μm InAs/AlSb HEMT based on the RS-SiN$_x$ technology was measured up to 40 GHz using a cryogenic microwave probe station JANIS ST 500-2 at room temperature and at 77 K. Noise characterization at 6 K was not carried out due to limitations of the measurement setup used.

In Fig. 5.12, the $NF_{50\Omega}$ at 8 GHz is plotted as a function of V_{GS}. For V_{DS} = 0.1 V, the minimum $NF_{50\Omega}$ is reduced from 4.4 dB to 1.7 dB upon cooling. At a higher V_{DS} bias of 0.24 V, the minimum $NF_{50\Omega}$ is 3.7 dB at 300 K and 2.5 dB at 77 K. Therefore, at 300 K, the lowest minimum $NF_{50\Omega}$ is achieved when biasing the device at the higher voltage of 0.24 V. This is explained by the increase of the peak g_m as a function of V_{DS} observed in Fig. 5.6(b), as well as by the less dominant impact ionization in the gate current at 300 K. Upon cooling, the minimum value of $NF_{50\Omega}$ is reduced for both drain bias values. In this case, however, the minimum $NF_{50\Omega}$ at 77 K is observed for the lower V_{DS} of 0.1 V because of the stronger impact ionization in I_G at reduced temperature when operating above 0.2 V. Therefore, under cryogenic operation, the best noise performance are achieved at very low V_{DS} bias where impact ionization becomes negligible.

The noise model of the InAs/AlSb HEMT was extracted at 300 K and

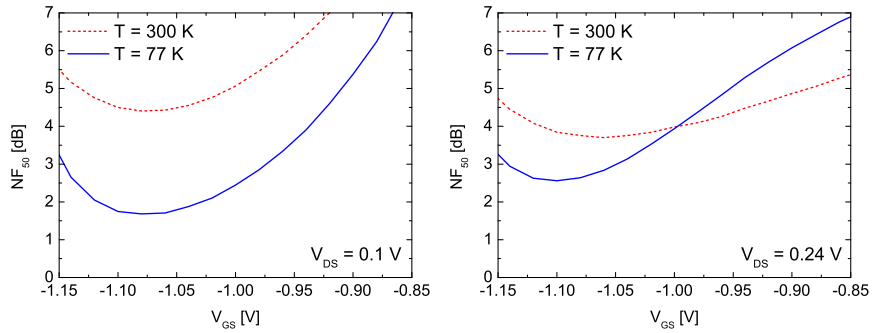


Fig. 5.12: $NF_{50\Omega}$ (@ 8 GHz) for 2×50 μm RS-SiN$_x$ InAs/AlSb HEMT at 300 K and at 77 K for (a) $V_{DS} = 0.1$ V and (b) for $V_{DS} = 0.24$ V.

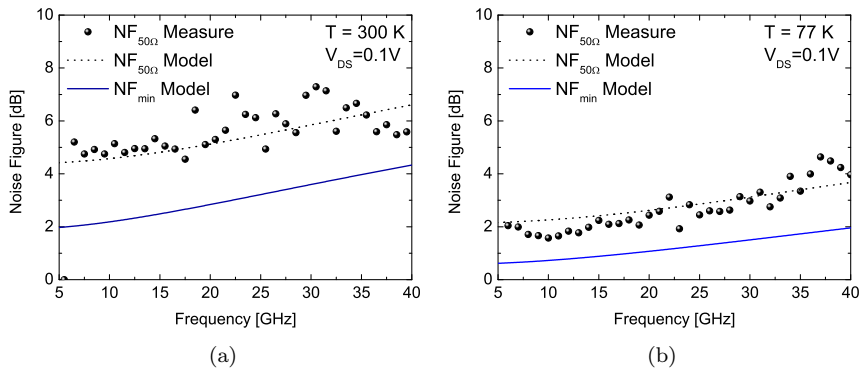


Fig. 5.13: Measured $NF_{50\Omega}$, modeled $NF_{50\Omega}$ and modeled NF_{min} at 300 K (a) and at 77 K (b) for $V_{DS} = 0.1$ V.

77 K using the Pospieszalski method [97] described in Section 4.2.2. At 300 K, the extracted NF_{min} is already above 2 dB at 8 GHz and close to 5 dB at 40 GHz. Upon cooling, NF_{min} drops to 0.57 dB at 8 GHz and furthermore, is below 2 dB up to a frequency of 40 GHz. In Fig. 5.13, the measured and modeled $NF_{50\Omega}$, as well as the modeled NF_{min} are plotted at 300 K and at 77 K between 6 GHz and 40 GHz for $V_{DS} = 0.1$ V. The reduced NF_{min} at 77 K is indeed related to the enhanced electron mobility at cryogenic temperature. Moreover, an important role in the noise performance improvement is played by the reduced gate leakage and extrinsic resistances, as well as by the higher peak g_m observed at low bias under cryogenic operation. It is also important to note that the NF_{min} curve becomes flat at low frequency, mainly due to the shot noise originating from the high gate leakage current.

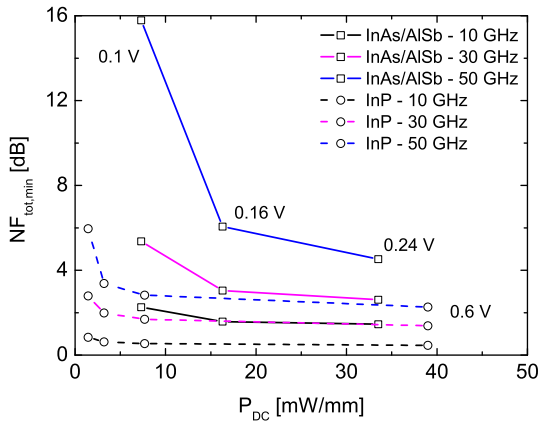


Fig. 5.14: $NF_{tot,min}$ for InAs/AlSb HEMT (solid lines) and for InP HEMT (dashed lines) at 300 K. Both HEMTs were biased at $V_{DS} = 0.1$ V, 0.16 V and 0.24 V. The InP HEMT was biased also at $V_{DS} = 0.6$ V.

5.4 Benchmarking InAs/AlSb HEMTs versus InP HEMTs

The DC, RF and noise measurements demonstrated that a number of InAs/AlSb HEMT parameters, crucial for the design of a cryogenic LNA, significantly improve when cooling, in particular for low V_{DS} values. However, the performances of the InAs/AlSb HEMT in cryogenic LNA designs are challenged by the more mature InP HEMT. This technology is well known to exhibit enhanced microwave device properties upon cooling [114, 115]. A benchmarking between a RS-SiN_x InAs/AlSb HEMT and a InP HEMT with the same gate length (110 nm) and gate width ($2\times50\,\mu$m) was carried out. In order to elucidate the potential for InAs/AlSb HEMTs in cryogenic LNAs, the investigation should however not be restricted to the NF_{min}. The reason is that at frequencies close to f_{max}, the gain of each stage is small and the noise contribution from the second, and sometimes even the third stage of a multistage LNA, cannot be ignored. A better figure of merit taking into account both gain and noise of the device is the minimum total noise figure $NF_{tot,min}$ defined in Eq. (5.2). For details on $NF_{tot,min}$ derivation see appended Paper [B].

$$NF_{tot,min} = \frac{NF_{min} - 1}{1 - \frac{1}{G_{max}}} + 1 \tag{5.2}$$

It is important to note that even though NF_{min} and G_{max} cannot be achieved simultaneously, $NF_{tot,min}$ can still be used as a first order estimation of the best result achievable in terms of noise and gain.

In Fig. 5.14, $NF_{tot,min}$ for the InP HEMT and for the InAs/AlSb HEMT is plotted versus P_{DC} at 300 K, for frequencies of 10 GHz, 30 GHz and 50 GHz. Both HEMTs are biased at $V_{DS} = 0.1$ V, 0.16 V and 0.24 V. The InP HEMT is measured also at 0.6 V in order to reach similar P_{DC} as the InAs/AlSb HEMT. Generally, it can be observed that the $NF_{tot,min}$ is lower in the InP HEMT for all bias points, in particular at higher frequency.

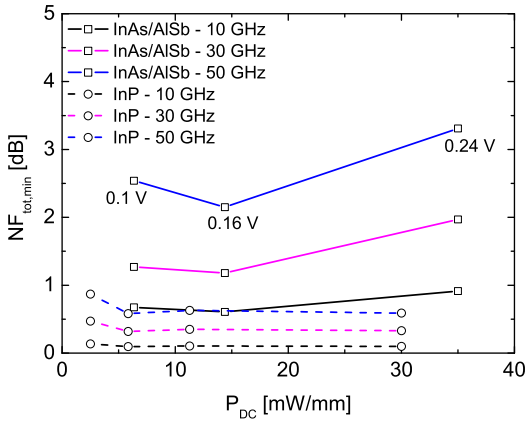


Fig. 5.15: $NF_{tot,min}$ for InAs/AlSb HEMT (solid lines) and for InP HEMT (dashed lines) at 77 K. Both HEMTs were biased at $V_{DS} = 0.1$ V, 0.16 V and 0.24 V. The InP HEMT was biased also at $V_{DS} = 0.6$ V.

As can be seen in Fig. 5.15, the performance of both technologies is significantly improved upon cooling. The InAs/AlSb HEMT shows a $NF_{tot,min}$ reduction from 15.8 dB (300 K) to 2.5 dB (77 K) at 0.1 V and 50 GHz, due to the higher gain and reduced I_G at low V_{DS}. Furthermore, the InAs/AlSb HEMT exhibits a minimum for 0.16 V since the impact ionization component of I_G, and hence the noise, increases rapidly for $V_{DS} > 0.2$ V. However, the InP HEMT still exhibits a lower $NF_{tot,min}$ in every bias point. The poorer behavior of the InAs/AlSb HEMT, compared to the InP HEMT, can be attributed to a number of factors, such as the significantly higher I_G and g_{DS} as well as to the leakage through the AlGaSb buffer which negatively influences the gain of the device.

5.5 Summary

In this thesis, an overall improvement of the InAs/AlSb HEMT under cryogenic conditions is demonstrated. Enhanced saturation of $I_D(V_{DS})$, 47% lower R_{on}, 43% higher peak g_m and significantly lower I_G are measured under low-power conditions ($V_{DS} < 0.2$ V). Furthermore, also RF and noise performance are enhanced at cryogenic temperature: f_T and f_{max} increase 72% and 100%, respectively, whereas the $NF_{tot,min}$ is more than 80% lower at $V_{DS} = 0.1$ V. This shows that the InAs/AlSb HEMT is a potential candidate for ultra-low power cryogenic LNA designs. However, a direct benchmark shows that the InAs/AlSb HEMT is not yet capable of challenging the mature InP HEMT in ultra-low noise cryogenic applications. A significant improvement of the overall noise performance is however expected for InAs/AlSb HEMTs based on the ion implantation and with pure AlSb metamorphic buffers, leading to the enhanced electrical isolation and thus lower gate leakage and output conductance.

Chapter 6

InAs/AlSb HEMT cryogenic LNA

The overall performance improvement demonstrated at very low drain voltage (∼0.1 V) upon cooling, makes the InAs/AlSb HEMT a potential device candidate for cryogenic microwave and millimeter wave circuits operating under very low power conditions. The reduction of the total power consumption is essential in applications such as radar arrays, space communication and portable systems. High-gain and low-noise circuits based on the InAs/AlSb HEMT technology and operating at DC power consumption below 10 mW have been reported [5–8]. In this chapter, the demonstration of a cryogenic 4-8 GHz hybrid LNA based on CVD-SiN_x InAs/AlSb HEMTs operating at very low power consumption is presented. The LNA has been characterized at both 300 K and 13 K, showing significant improvement with respect to noise temperature and power consumption when cooled. This is the first demonstration of a cryogenic LNA based on InAs/AlSb HEMTs.

6.1 Amplifier design

The amplifier used for the demonstration of the InAs/AlSb HEMT is a 4-8 GHz state-of-the-art three-stage single-ended hybrid LNA, originally designed for an in-house InP HEMT technology [56, 116]. Common source CVD-SiN_x InAs/AlSb HEMTs with gate length and width of 110 nm and 4×50 μm, respectively, are wire-bonded in each stage. The four gate finger layout with a total gate width of 200 μm is chosen due to the lower R_g and broader noise circles which minimize the noise performance sensitivity to input matching in the selected frequency range [117]. A SEM image of an InAs/AlSb HEMT after substrate thinning and dicing is shown in Fig. 6.1.

In order to achieve high gain and good input match without degrading the noise performance, inductive source feedback is used for the first stage of the amplifier. The inductance is realized by two 500 μm long parallel bond wires. Resistive loads are used on the drain for each stage to improve the stability of the amplifier. The input, inter-stage and output matching networks are based on microstrip lines fabricated on a 15 mil Rogers Duroid 6002 substrate.

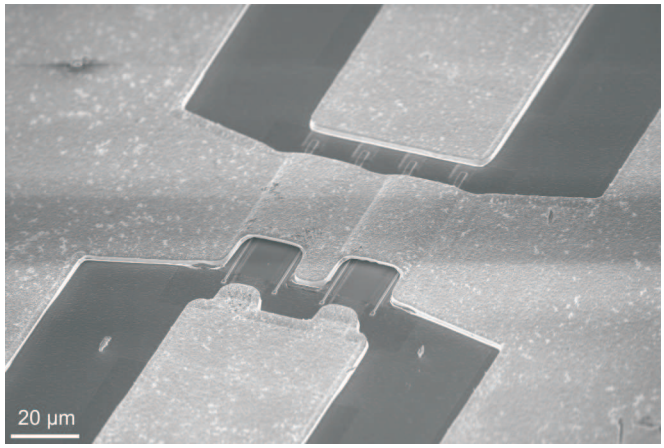


Fig. 6.1: SEM image of a 4×50 μm InAs/AlSb HEMT used in the cryogenic amplifier. Substrate thinning to 100 μm and dicing have been performed prior the HEMT mounting in the hybrid LNA.

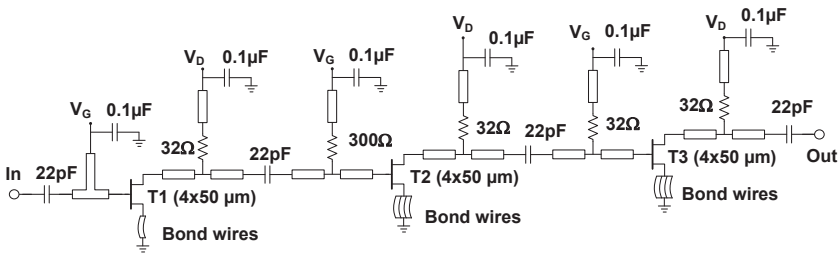


Fig. 6.2: Schematic of the three-stage single-ended InAs/AlSb HEMT hybrid LNA.

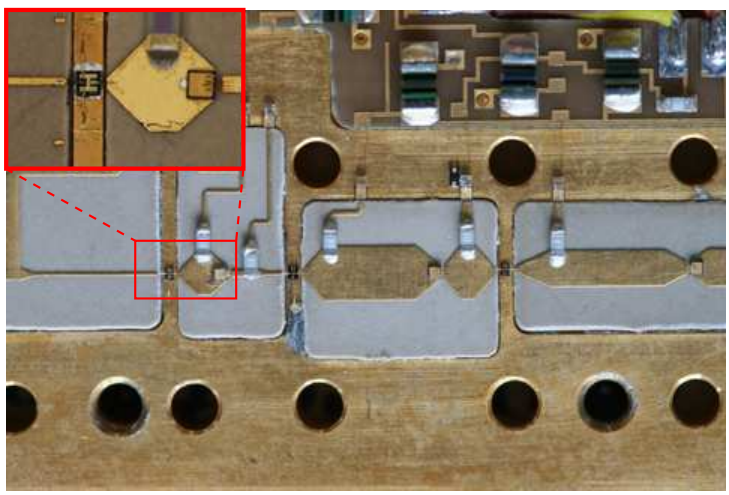
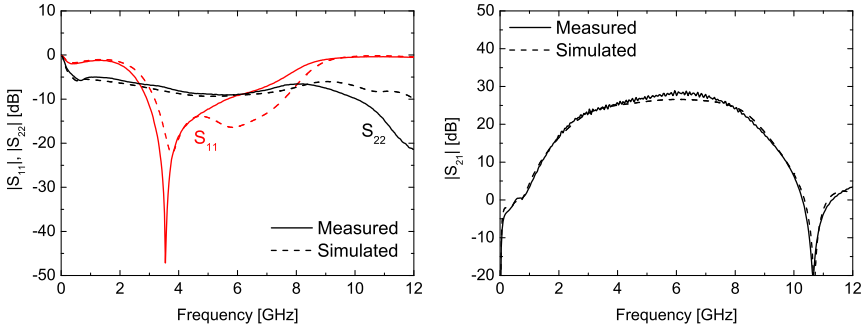


Fig. 6.3: Photograph of the 4-8 GHz hybrid LNA with a close-up view of the wire bonded InAs/AlSb HEMT.



(a) (b)

Fig. 6.4: Simulation and measurement at 300 K for (a) input and output reflection coefficients S_{11}, S_{22} and (b) gain S_{21}. The drain bias used for the amplifier is 0.65 V at a total drain current of 42 mA.

The circuit schematic of the LNA is shown in Fig. 6.2. A photograph of the amplifier module with a close-up view of the wire bonded input HEMT is shown in Fig. 6.3.

6.2 Amplifier characterization

The simulated and measured input and output reflection coefficients as well as the gain of the amplifier module at room temperature are plotted in Fig. 6.4 for an external drain bias of 0.65 V and a total supply current of 42 mA. S_{11} and S_{22} are below -7 dB in the 4-8 GHz bandwidth; See Fig. 6.4(a). Moreover, S_{21} is flat over the entire bandwidth and exhibits excellent agreement ($\pm$2 dB) with the simulated S_{21} in the whole measured frequency range; See Fig. 6.4(b). The good agreement between measured and simulated S-parameters demonstrates that a trustworthy small-signal model has been extracted for the InAs/AlSb HEMT. S-parameter measurements of the amplifier at cryogenic temperature are not shown since performing an accurate full-two port calibration including de-embedding of the connector losses is very challenging.

Fig. 6.5 presents noise temperature T_n and gain versus frequency of the amplifier at 300 K and 13 K. The bias point is adjusted at each temperature aiming for the lowest T_n. At 300 K, V_{DS} and the total current are 0.55 V and 32 mA, respectively, corresponding to a total P_{DC} dissipated in the amplifier of 17.6 mW. The intrinsic values of power consumption and drain bias, respectively, P_{DCi} and V_{DSi} in the HEMTs are 6.4 mW and 0.2 V. The lower voltage in the drain contact of the transistors is due to the voltage drop in the load resistors. At this bias, the LNA shows a minimum T_n of 150 K and a transducer gain of 29 dB at 6 GHz. A maximum gain of 33 dB can be reached when V_{DS} is increased but the noise performance degrades.

When the amplifier is cooled down to cryogenic temperature, a T_n of 19 K and a gain of 24 dB are measured. These values are obtained for a V_{DS} and a supply current of 0.3 V (V_{DSi} = 90 mV) and 20 mA, respectively, correspond-

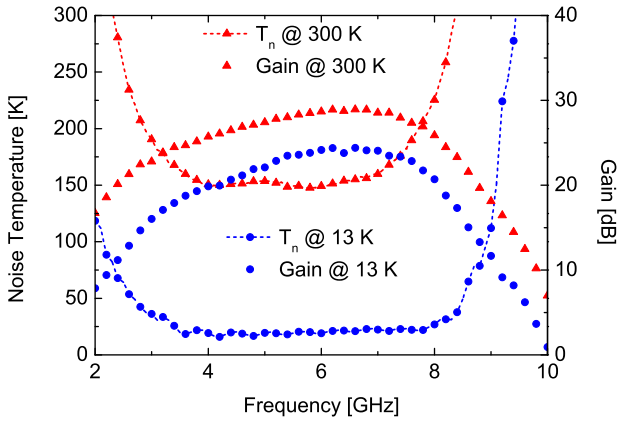


Fig. 6.5: Measured gain and noise temperature versus frequency at 300 K and 13 K at biases for lowest noise temperature.

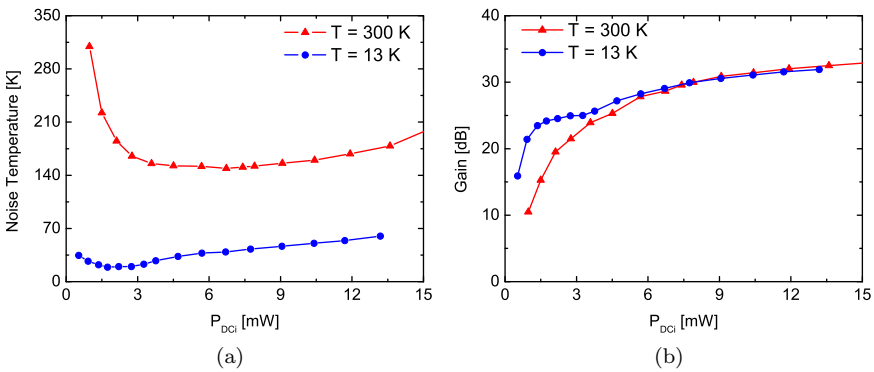


Fig. 6.6: (a) Noise temperature and (b) gain versus power consumption in the HEMT devices of the amplifier at 300 K and 13 K.

ing to a total P_{DC} of only 6 mW, 66% lower compared to 300 K. The intrinsic P_{DCi} dissipated by the three HEMTs is as low as 1.8 mW. A large amount of power is therefore dissipated in the resistive loads used for the amplifier stability. Simulations of the InAs/AlSb HEMT amplifier show that the resistive loads can be replaced with inductors without degrading the noise performance and stability. The use of inductive loads could potentially allow similar performance of the LNA at a much reduced total P_{DC}.

In Fig. 6.6, T_n and gain as a function of P_{DCi} in the HEMT devices are shown. From these plots, the reduction of the power consumption upon cooling is clear. At 300 K, T_n has its minimum in the range 5-10 mW. For higher P_{DCi}, a degradation of T_n is observed due to enhanced impact ionization in the InAs/AlSb HEMT devices. At 13 K, T_n minimum is shifted to the range 1.5-2.5 mW. Moreover, in this low P_{DCi} range, the gain is strongly enhanced compared to 300 K. The shift of the optimum LNA performance towards

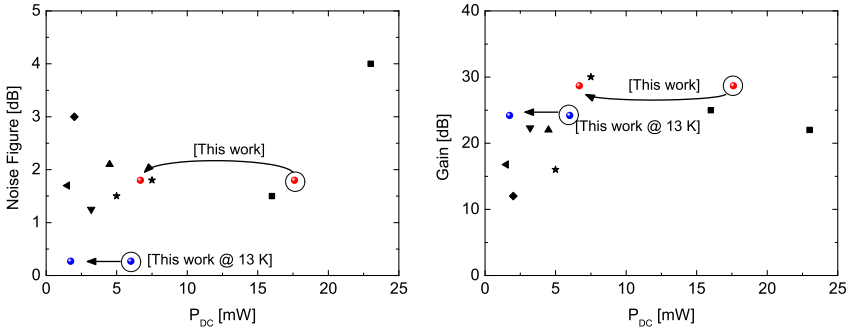


Fig. 6.7: (a) Noise and (b) gain performance of the presented hybrid LNA in comparison with state-of-the-art InAs/AlSb based MMIC LNAs [2,5–8]. The arrows illustrate the potential reduction of the total P_{DC} with the use of inductive loads.

significantly lower P_{DCi} values is related to the overall improvement of the InAs/AlSb HEMT under cryogenic operation with low drain bias.

The performance of the presented hybrid LNA is compared to other published state-of-the-art InAs/AlSb based MMIC LNAs in terms of noise figure and gain in Fig. 6.7. Fig. 6.7(a) shows the measured noise as a function of the total P_{DC} dissipated by the amplifiers. The noise figure exhibited at 300 K is comparable to the best results published for InAs/AlSb HEMT MMIC LNAs. Good performance is also demonstrated in terms of amplifier gain; See Fig. 6.7(b). The large improvement of noise temperature and power consumption demonstrated at 13 K points to the suitability of InAs/AlSb HEMTs for cryogenic LNAs operating at very low power. However, as previously discussed, most of the power of the demonstrated hybrid LNA is dissipated in the load resistors. The LNA layout, non optimized for this device technology, does not demonstrate the full potential of the InAs/AlSb HEMT device in a cryogenic LNA. The arrows of Fig. 6.7(a) and 6.7(b) indicate the potential performance of the demonstrated LNA using inductive loads with no power consumption outside the HEMT devices.

Further improvements in terms of noise and gain are expected for amplifiers designs fully optimized for the InAs/AlSb HEMT model. In addition, the use of InAs/AlSb HEMTs based on ion implantation for device isolation with pure AlSb metamorphic buffer is expected to further narrow the performance gap to the ultra-low noise performance achieved by today's InP HEMT technology.

Chapter 7

Conclusions

This thesis has dealt with the InAs/AlSb HEMT technology, presenting four main results which advance the state-of-the-art in the field: the explanation of anisotropic transport properties in the channel, the development of the fabrication process for higher HEMT reliability and improved electrical performance, the demonstration of improved microwave properties upon cooling and the first cryogenic LNA.

The anisotropic electron transport in the 2DEG of the InAs/AlSb HEMTs has been characterized through electrical measurements of test structures such as TLM, van der Pauw, Hall bar and HEMTs fabricated along different orientations. TLM and Hall bar exhibited a strong anisotropy with 32% lower sheet resistance and 53% higher electron mobility along the $[1\bar{1}0]$ direction. Furthermore, the HEMT devices exhibited 25% higher maximum I_D and g_m along the $[1\bar{1}0]$ direction. Surface morphological analysis as well as cross-sectional analysis demonstrated that the anisotropy in the electron transport is due to the presence of elongated pits in the channel. These pits are related to the threading dislocations occurring in the thick AlSb metamorphic buffer.

The HEMT fabrication process based on standard shallow-mesa technology has been significantly improved with respect to the electrical performance and stability against oxidation of AlSb-based materials using an *in-situ* early passivation. Furthermore, planar InAs/AlSb HEMTs based on ion implantation for device isolation with state-of-the-art performance and with high stability against oxidation have been demonstrated, potentially enabling the realization of reliable InAs/AlSb HEMT MMICs.

Cryogenic properties of the InAs/AlSb HEMT have been examined. Compared to room temperature, the device showed an overall DC improvement under cryogenic conditions, with enhanced drain current saturation, 47% lower R_{on}, 43% higher peak g_m at a bias of 0.1 V and a reduction of the Schottky component of the gate current of more than one order of magnitude. However, due to the enhanced electron mobility at low temperature, the impact ionization became more severe when cooling. The RF and noise performances also improved at cryogenic temperature: f_T and f_{max} increased 72% and 100%, respectively, whereas $NF_{tot,min}$ was about 1.7 dB lower at 0.1 V.

Finally, the developed InAs/AlSb HEMT technology has been demonstrated in a cryogenic three-stage hybrid low-noise amplifier which exhibited

minimum noise temperature of 19 K and gain above 24 dB at a DC power consumption of only 600 μW in the InAs/AlSb HEMT device.

7.1 Future work

The overall performance improvement demonstrated under cryogenic operation at low bias indicates that the InAs/AlSb HEMT is a promising candidate for microwave circuits operating at ultra low-power conditions. However, the ultimate low-noise capabilities of the mature InP HEMT technology have not been reached, so far, mainly because of the high gate leakage caused by impact ionization in the narrow bandgap channel. Further improvements in this area are indeed required in order to close the gap with the InP HEMT. A possible way of reducing the gate leakage could be the development of MOS-HEMT devices by using atomic-layer-deposited (ALD) films for gate isolation. Moreover, the heterostructure engineering should be also considered as a possible path. For instance, Kim *et al.* have limited the impact ionization by sandwiching a pure InAs sub-channel inside a wider bandgap $In_{53}Ga_{47}As$ channel [118].

Another critical issue of the InAs/AlSb HEMT, the high chemical instability of the AlSb compound, has been addressed in this thesis by developing a fabrication process based on the ion implantation. In order to further improve the electrical isolation, preliminary tests based on the implantation with multiple energies have been initiated but leaded to an unexpected poorer isolation, compared to the implantation at a single energy. Therefore, further material studies will have to be performed in order to have a full understanding of the physical mechanisms beyond the damage generated in the quantum well. Moreover, the fabrication of ion implanted InAs/AlSb HEMTs on heterostructures grown using a pure AlSb buffer has to be tested as well.

It is expected that the combination of all these improvements could potentially make the InAs/AlSb HEMT, the device technology with outmost performance in both noise level and power consumption, eventually taking full advantage of the outstanding transport properties of the InAs compound.

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