# Efficient and Wideband Power Amplifiers for Wireless Communications

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*To My Beloved Family*

# Abstract

The rapid evolution of wireless communication systems and the development of new standards require that wireless transmitters process several types of standards across multiple bands. Power amplifiers (PAs) are key components in wireless transmitters because they have a big impact on the overall system performance in terms of their bandwidth, efficiency, and linearity. This thesis presents various design techniques that improve bandwidth and efficiency characteristics of the PA.

For narrowband transmitters, a circuit design methodology that enables first-pass design of high efficiency single-ended PAs is presented. The method, based on employing bare-die transistors, specialized modeling technique, and optimization of harmonic impedances, is validated with excellent experimental results. A class-$F^{-1}$ PA at $3.5\,$GHz and a harmonically tuned PA at $5.5\,$GHz are designed and implemented demonstrating $78\,\%$ and $70\,\%$ PAE respectively.

For broadband transmitters, a design methodology for single-ended PAs with octave bandwidth is presented and verified. The method is based on a harmonic tuning approach combined with a systematic design of broadband matching networks. The demonstrator PA achieves 50-63 % PAE across 1.9-$4.3\,$GHz. Then, extending the bandwidth beyond one octave while maintaining high efficiency is investigated by adopting a push-pull configuration. For this reason, a novel push-pull harmonic load-pull measurement setup is proposed and a push-pull PA operating between 1-3 GHz is implemented. The investigation demonstrates the proposed setup as an important tool for understanding and optimizing PAs and baluns for wideband push-pull microwave PAs.

For multi-band transmitters, using signals with large peak-to-average power ratio, the design of dual-band Doherty PAs (DPAs) is considered. A detailed analysis of each passive structure constituting the DPA is given, leading to different configurations to implement dual-band DPAs. One of the configurations is implemented, leading to state-of-the-art results for dual-band DPAs. Finally, the multi-band branch-line coupler (BLC) is a key component for also extending the design of DPAs to multi-band in the future. A closed form design approach for multi-band BLCs operating at arbitrary frequencies is presented and validated by the successful design of dual-band, triple-band, and quad-band BLCs.

The excellent results obtained demonstrate the success of the developed design methodologies for high efficiency and multi-band/wideband PAs. These methods will contribute to the design of future wireless systems with improved performance in terms of efficiency, bandwidth and hence cost.

**Keywords:** Branch-line coupler, Doherty power amplifier, GaN-HEMT, high efficiency, multi-band, power amplifier, wideband.

# List of Publications

## Appended papers

This thesis is based on the following papers:

[A] **Paul Saad**, Christian Fager, Hossein Mashad Nemati, Haiying Cao, Herbert Zirath, and Kristoffer Andersson "A Highly Efficient 3.5 GHz Inverse Class-F GaN-HEMT Power Amplifier," in *International Journal of Microwave and Wireless Technologies*, vol. 2, no. 3-4, pp. 317-324, August, 2010.

[B] **Paul Saad**, Hossein Mashad Nemati, Kristoffer Andersson, and Christian Fager "Highly efficient GaN-HEMT power amplifiers at 3.5 GHz and 5.5 GHz," in *IEEE Wireless and Microwave Technology Conference*, April, 2011.

[C] **Paul Saad**, Christian Fager, Haiying Cao, Herbert Zirath, and Kristoffer Andersson "Design of a Highly Efficient 2-4 GHz Octave Bandwidth GaN-HEMT Power Amplifier," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 7, pp. 1677-1685, July, 2010.

[D] **Paul Saad**, Mattias Thorsell, Kristoffer Andersson, and Christian Fager, "Investigation of push-pull microwave power amplifiers using an advanced measurement setup," submitted to *IEEE Transactions on Microwave Theory and Techniques*.

[E] **Paul Saad**, Paolo Colantonio, Junghwan Moon, Luca Piazzon, Franco Giannini, Kristoffer Andersson, Bumman Kim, and Christian Fager "Concurrent Dual-Band GaN-HEMT Power Amplifier at 1.8 GHz and 2.4 GHz," in *IEEE Wireless and Microwave Technology Conference*, April, 2012.

[F] Luca Piazzon, **Paul Saad**, Paolo Colantonio, Franco Giannini, Kristoffer Andersson, and Christian Fager "Design Method For Quasi-Optimal Multi-Band Branch-Line Couplers," submitted to *International Journal of RF and Microwave Computer-Aided Engineering*.

[G] **Paul Saad**, Paolo Colantonio, Luca Piazzon, Franco Giannini, Kristoffer Andersson, and Christian Fager "Design of a Concurrent Dual-Band 1.8 GHz-2.4 GHz GaN-HEMT Doherty Power Amplifier," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1840-1849, June, 2012.

# Other papers and publications

The following papers and publications are not appended to the thesis, either due to contents overlapping that of appended papers, or due to contents not related to the thesis.

[a] **Paul Saad**, Luca Piazzon, Paolo Colantonio, Junghwan Moon, Franco Giannini, Kristoffer Andersson, Bumman Kim, and Christian Fager "Multi-band/Multi-mode and Efficient Transmitter Based on a Doherty Power Amplifier" in $42^{nd}$ *European Microwave Conference Proceeding*, October, 2012.

[b] Junghwan Moon, **Paul Saad**, Junghwan Son, Christian Fager, and Bumman Kim "2-D Enhanced Hammerstein Behavior Model for Concurrent Dual-Band Power Amplifiers" in $42^{nd}$ *European Microwave Conference Proceeding*, October, 2012.

[c] **Paul Saad**, Paolo Colantonio, Luca Piazzon, Franco Giannini, Kristoffer Andersson, and Christian Fager "Design of High Efficiency Concurrent Dual-Band Doherty Power Amplifier," in *GigaHertz 2012 Symposium*, Stockholm, March, 2012.

[d] Ulf Gustavsson, Thomas Eriksson, Hossein Mashad Nemati, **Paul Saad**, Peter Singerl, and Christian Fager "An RF Carrier Bursting System Using Partial Quantization Noise Cancellation," in *IEEE Transactions on Circuits and Systems*, vol.59, no.3, pp. 515-528, March, 2012.

[e] Luca Piazzon, **Paul Saad**, Paolo Colantonio, Franco Giannini, Kristoffer Andersson, and Christian Fager "Branch-Line Coupler Design Operating in Four Arbitrary Frequencies," in *IEEE Microwave and Wireless Components Letters*, vol.22, no.2, pp. 67-69, February, 2012.

[f] Hossein Mashad Nemati, **Paul Saad**, Kristoffer Andersson, and Christian Fager "High-Efficiency Power Amplifier," in *IEEE Microwave Magazine*, pp. 81-84, February, 2011.

[g] **Paul Saad**, Hossein Mashad Nemati, Mattias Thorsell, Kristoffer Andersson, and Christian Fager "An inverse class-F GaN-HEMT power amplifier with 78% PAE at 3.5 GHz," in *European Microwave Conference Proceedings*, vol.12, no.1, pp. 89-94, October, 2009.

[h] **Paul Saad**, Hossein Mashad Nemati, Mattias Thorsell, Kristoffer Andersson, and Christian Fager "Design of High Efficiency Power Amplifiers using a Bare-die Approach," in *2nd Workshop on Future Microwave Products*, University of Gävle, October, 2009.

[i] Uroshanit Yodprasit, **Paul Saad**, Cyril Botteron, and Pierre Andre Farine "Bulk-source-coupled CMOS quadrature oscillators," in *IEEE Electronics Letters*, pp. 2-3, January, 2009.

[j] **Paul Saad**, Roman Merz, Frederic Chastellain, Christian Robert, Uroshanit Yodprasit, Cyril Botteron, Pierre Andre Farine, Regis Caillet, Alexander Heubi, and Noureddine Senouci "A low-power, low data-rate, ultra-wideband receiver architecture for indoor wireless systems," in *IEEE International Conference on Ultra-Wideband*, pp. 37-40, September, 2008.

[k] **Paul Saad**, Roman Merz, Cyril Botteron, and Pierre Andre Farine "Performance comparison of UWB impulse-based multiple access schemes in indoor multipath channels," in *5th Workshop on Positioning, Navigation and Communication*, pp. 89-94, March, 2008.

# Notations and abbreviations

## Notations

| | |
|---|---|
| $C$ | Capacitance |
| $f$ | Frequency |
| $f_0$ | Center frequency or fundamental frequency |
| $I$ | Current |
| $I_\mathrm{A}$ | Current level of the auxiliary amplifier |
| $I_\mathrm{dc}$ | Drain bias current |
| $I_\mathrm{di}$ | Intrinsic drain-to-source current |
| $I_\mathrm{ds}$ | Drain-to-source current |
| $I_\mathrm{M}$ | Current level of the main amplifier |
| $I_\mathrm{max}$ | Maximum current |
| $L$ | Inductance |
| $L_\mathrm{bwg}$ | Inductance of bondwires at gate side |
| $L_\mathrm{bwd}$ | Inductance of bondwires at drain side |
| $P_\mathrm{in}$ | Input power |
| $P_\mathrm{out}$ | Output power |
| $P_\mathrm{out,avg}$ | Average output power |
| $P_\mathrm{1\text{-}dB}$ | 1-dB compression point |
| $Q$ | Q-factor |
| $R$ | Resistance |
| $R_\mathrm{L}$ | Load resistance |
| $S$-parameters | Scattering-parameters |
| $V$ | Voltage |
| $V_\mathrm{br}$ | Breakdown voltage |
| $V_\mathrm{DC}$ | DC supply voltage |
| $V_\mathrm{di}$ | Intrinsic drain-to-source voltage |
| $V_\mathrm{ds}$ | Drain-to-source voltage |
| $Y_\mathrm{C}$ | Common mode conductance |
| $Z_\mathrm{A}$ | Load seen by the auxiliary amplifier |
| $Z_\mathrm{D}$ | Differential mode impedance |
| $Z_\mathrm{M}$ | Load seen by the main amplifier |

| | |
|---|---|
| $Z_\mathrm{L}$ | Load impedance |
| $\omega$ | Angular frequency |
| $\epsilon_r$ | Dielectric constant |
| $\eta$ | Drain efficiency |
| $\infty$ | Infinity |
| $\lambda$ | Wavelength |
| $\Gamma$ | Reflection coefficient |
| $\theta$ | Electrical length |
| $\Theta$ | Conduction angle |

# Abbreviations

| | |
|---|---|
| ACLR | Adjacent channel leakage ratio |
| AM | Amplitude modulation |
| BJT | Bipolar-Junction Transistor |
| BLC | Branch line coupler |
| CAD | Computer-aided design |
| CN | Common node |
| $CO_2$ | Carbon dioxide |
| CW | Continuous wave |
| CRLH | Composite Righ/Left Handed |
| EB | Exabyte |
| EER | Envelope elimination and restoration |
| EM | Electromagnetic |
| ET | Envelope tracking |
| DC | Direct current |
| DPA | Doherty power amplifier |
| DPD | Digital predistortion |
| EER | Envelope elimination and restoration |
| ET | Envelope tracking |
| FET | Field Effect Transistor |
| GaN | Gallium Nitride |
| GaAs | Gallium Arsenide |
| GSM | Global system for mobile |
| HT | Harmonically tuned |
| HEMT | High Electron Mobility Transistor |
| ICT | Information and Communication Technologies |
| IIN | Impedance inverter network |
| IPS | Input power splitter |
| ITN | Impedance transformer network |
| LTE | Long term evolution |
| MC | Monte-Carlo |
| MMIC | Microwave monolithic integrated circuits |
| OBO | Output back-off |
| OFDM | Orthogonal frequency-division multiplexing |

| | |
|---|---|
| PA | Power Amplifier |
| PAE | Power-added efficiency |
| PAPR | Peak-to-average power ratio |
| PCB | Printed circuit board |
| PCN | Phase compensation network |
| PM | Phase modulation |
| Q | Quality factor |
| QAM | Quadrature amplitude modulation |
| RBS | Radio base station |
| RF | Radio Frequency |
| Si | Silicon |
| SMPA | Switched mode power amplifier |
| TL | Transmission Line |
| TWA | Traveling Wave Amplifier |
| UMTS | Universal mobile telecommunications system |
| Vs | Versus |
| WCDMA | Wideband code division multiple access |
| WiFi | Wireless fidelity |
| WiMAX | Worlwide interoperability for microwave access |
| 4G | The fourth generation of cellular wireless standards |

# Contents

# Chapter 1

# Introduction

## 1.1 Motivation

Mobile and wireless communications systems have revolutionized our daily life and business. We are observing a rapid growth in these technologies where mobile and wireless communications have become so important in our society and indispensable for our daily lives. Consequently, due the increasing growth of user subscribers and the emergence of new technologies in the mobile communication systems, the data traffic is estimated to increase to $10.8\,\text{EB}^1$ per month by 2016 [1]. As shown in Fig. 1.1, this corresponds to an 18-fold increase over 2011. To handle growing mobile data traffic requirements, mobile network operators have begun to introduce small cells into their networks in order to keep up with demand. This will further increase the number of radio base stations (RBSs) installed and hence, results in increased energy consumption caused by the Information and Communication Technologies (ICT).
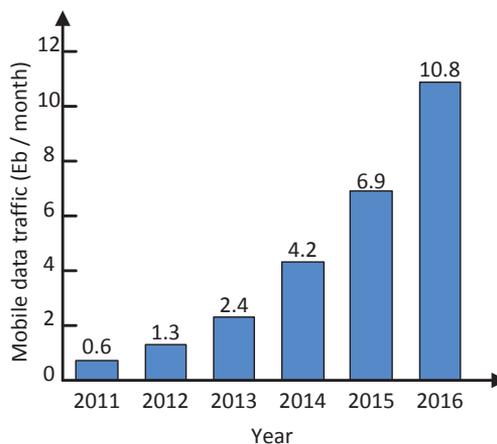
**Fig. 1.1:** Global Mobile Data Traffic forecast, 2011 to 2016 [1].

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[1] 1 Exabyte $= 1.048576 \cdot 10^6$ Terabytes $= 1.1529215 \cdot 10^{18}$ Bytes

The RBS consumes power in order to transmit RF signals and to process the incoming signals from subscriber cell phones. The total efficiency of the RBS, which is usually very low, is calculated as the ratio of the total RF output power to the total consumed power. The RBSs are the main contributor to the energy consumption of the wireless infrastructure and are therefore, the highest contributors of $CO_2$ emissions in mobile networks [2]. To reduce the $CO_2$ emission, the energy consumption of the RBS has to be minimized and hence its efficiency should be maximized. The energy per function distribution of a RBS blocks presented in [3], shows that RF power amplifiers (PAs) are the most energy-consuming blocks of RBSs and therefore their energy efficiency have a high impact on the total energy consumption of RBSs. Increasing the energy efficiency of PAs does not only reduce the total energy consumption and the $CO_2$ emission. It also affects other critical parameters of wireless systems such as weight and reliability. Higher efficiency means that less power is dissipated and less heat removal is needed which directly translates to the weight, the volume, and the cost of the RBS.
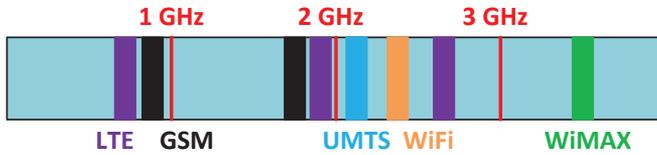


**Fig. 1.2:** Spectral position of the main communication standards.

In addition to the efficiency issue, and as shown in Fig. 1.2, the number of mobile radio standards (GSM, UMTS, WiFi, 4G LTE, WiMAX, etc.) and frequency bands (0.9, 1.8 GHz, 2.1 GHz, 2.4 GHz,0.8, 1.9, 2.6 GHz, 3.5 GHz, etc.) have increased and therefore, the demand for multiband/multistandard capable RBSs arise in order to reduce system manufacturers product diversity and to support the flexibility of mobile operators. This makes multiband/wideband PAs that cover many frequency bands while maintaining high efficiency an important and hot research topic.

Usually, the design of PAs is the result of trade-offs, trying to accomplish several conflicting requirements such as efficiency vs. linearity and efficiency vs. bandwidth. These conflicting requirements are addressed in the following.

## 1.2   Efficiency versus linearity

A typical output power versus input power characteristic of a PA is shown in Fig. 1.3(a) while a typical output power probability density function of a modulated mobile communication signal and the power-added-efficiency (PAE) of a PA are shown versus output power in Fig. 1.3(b). As the input power increases (Fig. 1.3(a)), the output power increases until it reaches saturation where it does not increase any further (compression). The PA is usually driven so that the peaks of the input signal reaches the beginning of the saturation region where the output power has dropped by 1- dB compared to an ideal linear behavior (the so-called 1 dB compression point). This typically occurs close to the point where the efficiency is maximized [4].
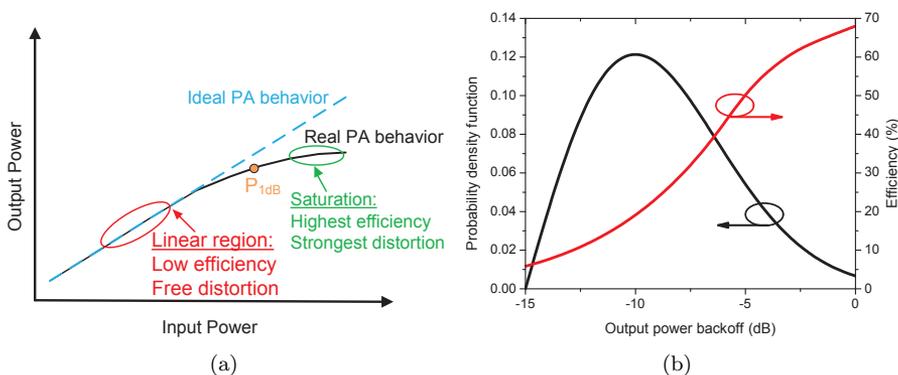
**Fig. 1.3:** (a) Output power versus input power of an ideal and a real power amplifier (b) efficiency and typical probability density function of a mobile communication signal versus output power backoff.

In earlier communication systems, like Global System for Mobile (GSM), the communication signal has a constant amplitude. This allows the PA to be operated in compression and hence in high efficiency. In contrast, modern wireless communication systems employ modulation schemes such as Orthogonal Frequency-Division Multiplexing (OFDM) and Quadrature amplitude modulation (QAM) in order to maximize the spectral efficiency [4]. These modulation schemes result in signals with large amplitude variations and peak-to-average power ratios (PAPRs) in the range of 6-12 dB [5,6]. In order to prevent clipping of the signal peaks and thereby strong distortion of the signal, these signals requires the PA to operate at an average output power far below the saturation region and hence, at low efficiency levels as illustrated in Fig. 1.3(b).

Different high efficiency architectures have been proposed to increase the average efficiency of PAs defined as the ratio between average output power and average supplied DC power [7]. Envelope elimination and restoration (EER) [8], envelope tracking (ET) [9], Doherty amplifiers [10] and varactor based dynamic load modulation [11] are the most common. In EER and ET, the supply voltage of the power amplifier is designed to track the instantaneous envelope of the modulated signal. Hence, it operates in saturation and recovers its peak efficiency for a wider range of output power levels [8,9]. In Doherty amplifiers and varactor based load modulation transmitters, high average efficiency is achieved by dynamically adapting the PA load impedance to keep the amplifier in compression during modulation [4,10,12,13].

The average efficiency of the PA is scaled by the PA peak efficiency and hence, the average efficiency is limited by the peak efficiency of the PA. Therefore, the peak efficiency has a direct implication on the average efficiency when the PA is used in a high efficiency architecture, e.g. ET or EER. In such architectures, the PA is kept in saturation for a large output power dynamic range. Our main goal in this thesis is to investigate methods for improvement of PA peak and average efficiencies.

## 1.3   Efficiency versus bandwidth

As discussed earlier, efficient wideband PAs are highly demanded for modern and future communication systems. Usually, high efficiency PAs operate over narrow bandwidth, since for a given device technology, the bandwidth of the PA decreases as the efficiency increases. The basic limitations in designing efficient and wideband amplifiers are associated with the device technology used.

The output impedance of the device is usually characterized by a complex impedance, i.e shunt $R - C$ circuit. In [14], it is demonstrated that the bandwidth over which a good match of a complex load can be obtained is limited by the $RC$ product. If the impedance at the interface of the transistor (die) is very low, then the quality factor ($Q$) value of the transformation, between a low impedance at the transistor to a $50\,\Omega$ load, is high and consequently decreases the useful bandwidth. Hence, it is of great importance to have devices with high output impedance to facilitate the matching and to obtain wider bandwidth. In the following, a comparison of the different devices used for RF PA stages is given.

### 1.3.1   Comparison of different devices characteristics

Different types of RF solid state transistors are used in the design of PAs. These transistors can be divided in two main groups, the Field Effect Transistors (FETs) and the Bipolar-Junction Transistors (BJTs) [15]. Usually, these devices are fabricated from Silicon (Si) or from III-V compound semiconductors like Gallium Arsenide (GaAs) and the recently developed wide bandgap semiconductor Gallium Nitride (GaN). Table. 4.5 shows a comparison of some performance metrics of Si, GaAs, and GaN.

**Table 1.1:** Si, GaAs, and GaN Material Properties [13]

| Properties | Si | GaAs | GaN |
|---|---|---|---|
| Bandgap ($eV$) | 1.12 | 1.42 | 3.20 |
| Breakdown Field ($10^5 V/cm$) | 3.80 | 4.20 | 50.00 |
| Saturated Velocity ($10^7 cm/sec$) | 0.70 | 2.00 | 1.80 |
| Electron Mobility ($cm^2/V \cdot sec$) | 1500 | 8500 | 2000 |
| Thermal conductivity ($W/cm \cdot^\circ$ C) | 1.40 | 0.45 | 1.70 |

A wider bandgap semiconductor means supporting higher internal electric fields before the dielectric breakdown occurs. Consequently, the device will be able to allow higher output voltage swings and thus, attain higher output power levels. The wide bandgap of GaN semiconductors offers the potential to fabricate RF devices with an order of magnitude improved RF output power compared to traditional devices based on Si and GaAs [16]. The improved RF

output power is made possible due to the unique material properties of the GaN semiconductor presented in Table. 4.5. The electron mobility mainly determine the ON-resistance, the knee voltage, and the maximum operating frequency of a power device, while higher thermal conductivity means that the material is able to conduct more heat. GaN has higher thermal conductivity than GaAs or Si meaning that GaN devices can operate at higher power densities than either GaAs or Si [13].

The high breakdown voltages and high power densities of GaN offer a number of advantages for PA design with respect to Si and GaAs devices [17]. GaN technology offers high power per unit channel width that translates into smaller devices for the same output power. This results in smaller parasitic capacitances and thus increases the gain and the impedance level at the input and output of the device. Consequently, the matching networks will be simpler and exhibit broader bandwidth. This makes GaN technology better than other technologies for the realization of efficient and wideband PAs. This latter conclusion is also supported by the dramatic increased research on high efficiency PAs using GaN devices during the last decade.

## 1.4 Thesis Contributions

This thesis addresses the performance improvement of RF PAs used in wireless transmitters. In particular, the thesis concentrates on enhancing the efficiency of the PA, on operating the PA simultaneously in different bands, and on widening its operating frequency bandwidth.

Regardless of the well established PA theory [4,13], the real implementation of efficient PAs is often based on experience of the designer, where tuning of the fabricated PA is used to achieve the same performance predicted by Computer-aided design (CAD) simulations. To enable first-pass design and to improve the peak efficiency of the single-band PAs, a complete systematic design procedure is proposed. The procedure includes a bare-die mounting technique, dedicated transistor modeling technique, and circuit design methodology. The latter includes comprehensive source-pull/load-pull simulations at fundamental and harmonics, Monte-Carlo (MC) simulations that study the impact of the components variability on the PA performance, and Electromagnetic (EM) simulations that enable accurate synthesis of the matching networks. This procedure has allowed us to implement first-pass designs having excellent performance. We demonstrated the success of this procedure at S-band in [paper A], and at C-band in [Paper B].

Having this procedure as a basis, we have tried to widen the frequency operation bandwidth of the PA while maintaining high efficiency. The high-efficiency wideband PAs reported in the literature generally have a bandwidth of less than one octave [18–21]. Moreover, they rarely present any general method or analytical derivation for the design of the wideband matching networks used. In this thesis, a design procedure based on a source pull/load pull simulation approach together with an extensively detailed method for the design of suitable broadband matching network solutions. In [Paper C], we demonstrate the success of the proposed approach by the design and implementation of an octave bandwidth PA.

Increasing the bandwidth to more than one octave while maintaining high efficiency was investigated by adopting a push-pull configuration. Even though the bandwidth potential of the push-pull configuration has been demonstrated [22], there is no possibility to investigate or verify the true operation and interaction between PA and balun. In [Paper D], we propose a novel push-pull harmonic load-pull measurement setup able to emulate the balun operation, at the output of a push-pull PA, while setting any fundamental and second harmonic loading conditions. By using the proposed measurement setup, together with a push-pull PA prototype, we demonstrate the importance of the even mode second harmonic response of the output balun for the design of wideband push-pull microwave PAs.

To increase the average efficiency, the efficiency in back-off must increase. Therefore, the design of the DPA has been considered in the thesis. So far, lot of work has been done on DPAs [12, 23–32]. However, most of the published DPAs were designed to work in a single-band and therefore they do not satisfy the multi-band, multi-standard requirements of the modern RBSs. Recently, there have been some efforts to optimize a DPA for dual-band operation. The first prototype of dual-band DPA reported in [33] was working only in the first band. Two working dual-band DPAs are presented in [34, 35]. However, there is no general theoretical analysis presented and the achieved performance is quiet modest. In [Paper E], a dual-band single-ended PA is firstly designed to serve as Main PA for the Doherty PA. In [Paper G], a detailed design methodology, based on comprehensive design of the passive structures, for dual-band is presented and validated by successfully state-of-the-art experimental results.

To develop multi-band DPAs in the future, multi-band BLCs are needed. Solutions to design BLCs having more than two operating bands can be found in [36–39]. However, the methods proposed in [36–38] are not assisted with a full theoretical analysis that demonstrates the possibility to extend them for an arbitrary number of operating frequencies. Moreover, the approach presented in [39] is limited to commensurate frequencies. In this thesis, a design approach for multi-band BLCs for arbitrary operating frequencies is presented. The complete theoretical analysis of the topology is derived in [paper F], leading to a closed form system of equations for its design. Three couplers based on the proposed structure are implemented for dual-, triple-, and quad-band operation to validate the methodology.

## 1.5    Thesis outline

This thesis focuses on the design of highly efficient single-band, dual-band, and wideband PAs using GaN-HEMT devices. Chapter 2 reviews some of the most typical classes of PAs and presents the design and implementation of an inverse class-F PA and a harmonically tuned PA with high peak efficiency. Chapter 3 focuses on design techniques developed to design highly efficient and wideband single-ended PAs. Moreover, a comprehensive investigation on the interaction between push-pull PAs and baluns for broadband microwave applications is also presented. In Chapter 4, design approaches for dual-band DPAs and multi-band BLCs are presented and experimentally validated. Chapter 5 concludes by summarizing the main points discussed in the different chapters,

followed by some suggestions for future research directions. In Chapter 6, a short introduction of appended papers is given and the contributions of the author are specified.

# Chapter 2

# Efficient single-band saturated power amplifiers

As already discussed in Chapter 1, high efficiency saturated PAs are important components to obtain small, and low cost transmitters for wireless communications systems. To date, lot of effort has been put to obtain the highest possible efficiency values in a PA. Therefore, several classes, e.g. class-D, -E, -F, -F$^{-1}$, -J, have been proposed [4,25]. In these classes, the transistor current and voltage waveforms are tailored by specific load network designs to prevent an overlap between them, thus minimizing power dissipation and ensuring the highest efficiency level.

This chapter focuses on the design of PAs used in high efficiency architecture where the PA is kept in saturation for a large output power dynamic range. In the following, an overview of PA operation classes is given and a design procedure for first-pass design of high efficiency saturated PAs is presented. The design procedure consists of using a bare-die technique, an optimized transistor model, and a methodology to locate the fundamental and harmonic impedances. The success of the presented procedure is demonstrated by the design of an inverse class-F GaN-HEMT PA at 3.5 GHz and a harmonically tuned PA at 5.5 GHz.

## 2.1 Idealized power amplifier classes

PAs can (in general) be classified into two main categories: Transconductance amplifiers and switched mode power amplifiers (SMPAs). The transconductance amplifiers are traditionally categorized into class-A, class-AB, class-B, and class-C amplifiers. The classification of the transconductance amplifiers depends on the quiescent bias point of the active device or, equivalently, on the device current conduction angle. In SMPAs, where the device is operated like a switch rather than a current source, the classification is related to the active device dynamic operating conditions (e.g. class-E) or to the matching network terminating conditions (e.g. class-F) [4,25].

The mentioned classes above, except for class-A, require termination for all harmonics of the input signal. This becomes difficult when the operating

frequency range is moved towards the microwave region [25]. Therefore, in practice, only the fundamental and first few harmonics (second and third or just second) can be controlled. Consequently, class-J amplifier has been proposed in [4]. It provides same efficiency and linearity as Class-B amplifiers by controlling only the fundamental and second harmonic while the higher order harmonics are assumed to be short-circuited by the output capacitance of the device.

### 2.1.1   Traditional transconductance amplifiers

Class-A, Class-AB, Class-B, and Class-C amplifiers, known as transconductance amplifiers, use active transistors as voltage controlled current sources [4, 40–42]. Fig. 2.1(a) shows a simplified circuit topology of these amplifiers consisting of a transistor, RF choke ($L_{RFC}$), DC blocking capacitor, and a bandpass filter to short circuit the out of band tones. This parallel resonator configuration also ensures a sinusoidal voltage waveform across the transistor.
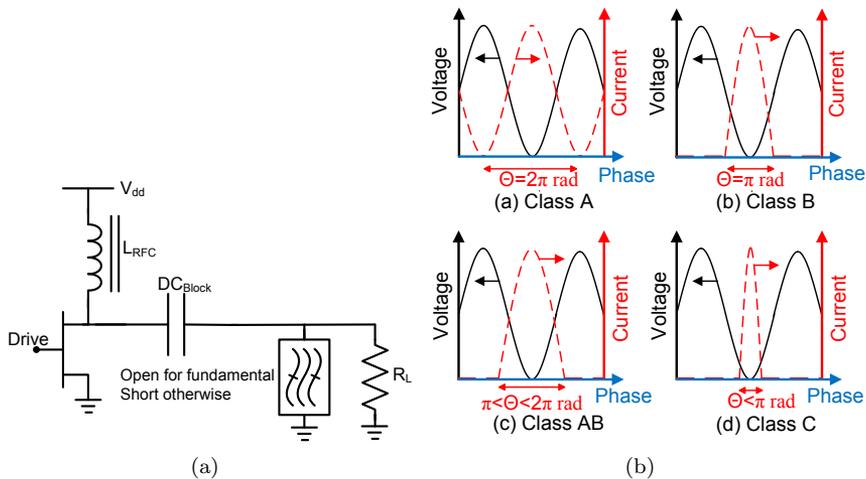


**Fig. 2.1:** Transconductance amplifiers (a) Circuit topology (b) Voltage and current waveforms.

These four types of PAs are distinguished by the device conduction angle, i.e., the portion of $2\pi$ rad over which a current is flowing through the transistor. Voltage and current waveforms for different classes are shown in Fig. 2.1(b). The class-A amplifier has a conduction angle of $\Theta = 2\pi$ rad. It has in practice the highest linearity but the lowest peak efficiency (50 %) over the other classes. The class-B amplifier operates ideally at zero quiescent current so the transistor will be conducting for a half cycle ($\Theta = \pi$ rad). Therefore, its theoretical efficiency (78 %) is higher than that of the class-A amplifier. The class-AB amplifier is a compromise ($\pi < \Theta < 2\pi$ rad) between class A and class B in terms of efficiency and therefore often employed in traditional transmitter implementations such as RBSs. The transistor is biased slightly above pinch-off, typically at 10 % to 15 % of the drain saturation current. In this case, the transistor will be conducting for more than a half cycle, but less than a full cycle of the input signal. The Class-C amplifier can achieve an ideal efficiency

of 100 % when the conduction angle is reduced to zero. However, there are several drawbacks in this class of operation at microwave frequencies. The first drawback is that the gain and the output power approaches zero, as the efficiency approaches 100 %. The second drawback is that the amplifier is highly nonlinear, so it has to be used with linearization techniques.

### 2.1.2 Switched mode power amplifiers

In contrast to the transconductance amplifiers, where the device is operating as a current source, SMPAs are based on the notion that the transistor is operating as a switch. In the on-state, while the device acts as a short circuit and the current flows through it, the voltage across it should be zero. In the off-state, the device acts as an open circuit and no current flows through it. Therefore, ideally, in both states there is no power dissipated in the device and hence 100 % efficiency is theoretically achieved [43].

Unfortunately, in practical high frequency SMPAs the efficiency is degraded from 100 % due to non-idealities of the components. Typical non-idealities are parasitic elements, finite on-resistance, non-zero transition time, and non-zero knee voltage [4, 44].

Inverse Class-F is very popular in microwave applications because the designer only need to control the fundamental and the second harmonic. Short circuiting the third harmonic may be obtained by the output capacitor of the device. A description of ideal inverse class-F is given hereafter.

#### 2.1.2.1 Ideal inverse class-F power amplifiers

Due to the active device physical limits for output current and voltage swings, the output current and voltage of a PA with large-signal drive are no longer purely sinusoidal but contains a large number of harmonics. The wave shaping of these harmonics leads to high power conversion efficiency [25] and hence Inverse-F PA definition. The structure of an inverse class-F PA is shown in Fig. 2.2(a) where filters are used to control the harmonic contents of the drain current and voltage. Fig. 2.2(b) shows the ideal voltage and current waveforms of the inverse class-F PAs. They have half-sinusoidal voltage and square-wave current signals. The ideal waveforms can be analyzed using Fourier series expansion, which gives expressions for voltage and current waveforms and their harmonics [4, 25]. The values of impedance terminations can be easily obtained by the ratio between respective Fourier voltage and current components.

In order to achieve 100% drain efficiency with ideal waveforms, the following impedance conditions should be met for inverse Class-F amplifiers:

$$Z_L[f_0] = Z_{opt}, \tag{2.1}$$

$$Z_L[2nf_0]_{n>1} = \infty, \tag{2.2}$$

$$Z_L[2(n+1)f_0]_{n>1} = 0, \tag{2.3}$$

where $f_0$ is the fundamental frequency, $n$ is the harmonic number, and $Z_{opt}$ is the optimal load impedance at the fundamental frequency. It is important
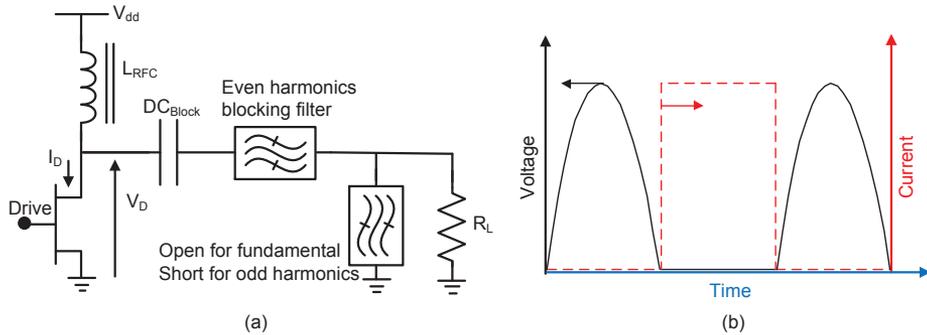
**Fig. 2.2:** (a) Circuit topology of inverse Class-F amplifiers (b) Idealized voltage and current waveforms of inverse Class-F amplifiers.

to note that class-F is a dual of the inverse class-F PA. Therefore, to obtain class-F operation, the harmonics impedance conditions, as well as the current and voltage waveforms, are interchanged.

### 2.1.3  Practical high frequency power amplifiers

In the previous section, the ideal impedance termination conditions for the different classes of operation are given. In practice, it is not possible to control all the harmonics and obtain ideal operation. Therefore, the so-called harmonically tuned and class-J PAs can be regarded as a practical solution for their implementation.

#### 2.1.3.1  Harmonically tuned power amplifiers

In low frequency applications, a large number of harmonic terminations can be controlled. Hence, it is possible to achieve performances close to the ideal figures when the device has low knee voltage $V_k$ and/or high breakdown voltage $V_{BR}$. However, this is not the case for high frequency applications (microwave region and beyond), where the performance is degraded compared to the theoretical ones. The main reason for this degradation is the limited number of harmonics that can be controlled in practice. As the frequency increases, the control of higher order harmonics becomes very difficult, because the output capacitance of the device short-circuit higher frequency components, therefore not allowing the desired wave-shaping. According to [45, 46], controlling the second, $2f_0$, and the third, $3f_0$, harmonics is usually enough for practical applications. Trying to control more harmonics will increase the complexity of the circuit without improving the performance considerably [47].

As an example, when designing a practical inverse class-F PA, typically the fundamental and one or two harmonics are only controlled. However, this opens up the question if this still corresponds to an inverse-F operation or to another operation mode. In this case, studying the intrinsic drain current and voltage waveforms can be very helpful to determine the mode of operation of the PA. Therefore, a device model that allow the intrinsic waveforms to be inspected during simulations is highly desirable.

### 2.1.3.2   Class-J power amplifiers

A new class of operation named as Class-J was introduced recently by Cripps [4]. Class-J became popular due to its high performance in terms of efficiency and linearity obtained with simple load network. The key features of Class-J are a complex impedance presented at the fundamental and reactive termination for second harmonic that can be physically realized using the device output capacitance. In [48], it is shown that impedance pairs of fundamental and second harmonic that form a design space for the class-J exist. All these pairs provide the same efficiency and linearity as harmonic tuned linear PA, like Class-AB or Class-B. This means that class-J is still kind of a linear PA and the efficiency predicted by theory only covers up to compression. However, peak efficiency is expected to happen at higher input power where it is no longer sure that the class-J terminations are giving the highest efficiency. This explains why some of the reported Class-J PAs provide better efficiency than the theoretical expectation [20, 49].

In the following, we propose an empirical design approach that is directly aimed to get the highest peak efficiency of the PA.

## 2.2   Design procedure for high efficiency power amplifiers

The proposed design procedure for high efficiency PAs includes a bare-die mounting technique, an accurate nonlinear transistor model that allows reliable simulations, and a circuit design methodology. This latter involves comprehensive fundamental and harmonic source-/load-pull simulations. Moreover, EM and MC simulations are finally used to allow accurate simulations and ensure first-pass design.

### 2.2.1   Bare-die mounting technique

Two of the most important transistor parasitics, the lead inductances and tab capacitances ($L_1$ and $C_1$ in Fig. 2.3(a)) associated with transistor packages have in our work been eliminated by using a transistor chip without any package (Fig. 2.3(b)). Using this approach, we reduce the extrinsic parasitics, and therefore facilitating a more wideband and less sensitive harmonic matching. The bare-die transistor chip is mounted to the PA fixture and connected di-
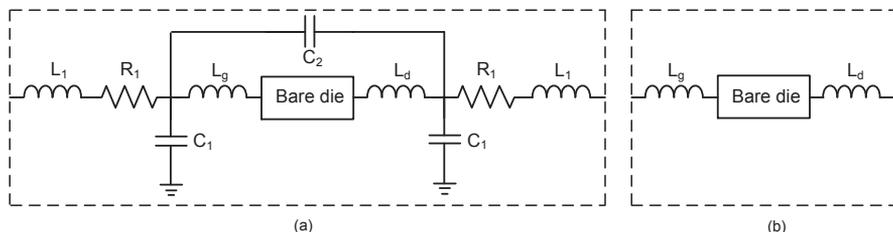


**Fig. 2.3:** Model for (a) Packaged device [50]; (b) Bare-die device. $L_g$ and $L_d$ model the bondwires used to connect the drain and gate pads of the bare-die transistor.

rectly to the printed circuit boards (PCBs) using wire bonding ($L_g$ and $L_d$ in Fig. 2.3). The thickness of the ridge where the transistor chip is mounted, is carefully adjusted to align the surface of the chip to the transmission lines (TLs). Hence, the distances between the TLs and the transistor chip are minimized as shown in Fig. 2.4(a). The bond wires used are of gold, and as depicted in Fig. 2.4(b), we use at least three bond wires to connect the transistor chip to the TLs. An equivalent inductance in the range $0.15\text{-}0.2\,\mathrm{nH}$ is estimated on each side.
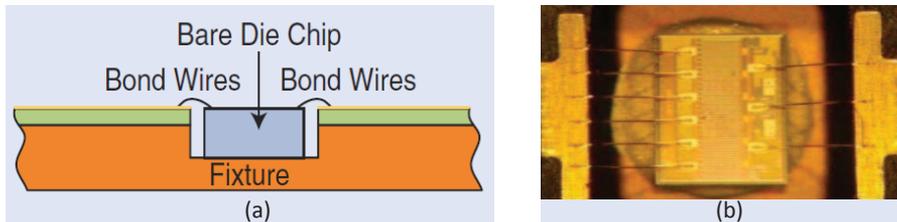


**Fig. 2.4:** Bare-die transistor mounting technique: (a) Cross section view; (b) Top view.

## 2.2.2   Transistor modeling for high efficiency power amplifiers

The determination of the optimum impedances of fundamental and harmonics that maximize the efficiency can be obtained by either using a load-pull measurement setup [51–53] or a device model that can be used for performing load-pull in a circuit-simulator [49, 54, 55]. The use of a non-linear transistor model has many advantages over the load-pull measurement setup. It allows the investigation of the drain voltage and current intrinsic waveforms and therefore the PA class of operation. The effect of fundamental and harmonic impedances is easy to carry out. Moreover, it allows multi-harmonic PAE sensitivity analysis, which is useful in determining how deviations in matching network design affect the PA performance.

Accurate modeling of the bare-die transistor is important to achieve first-pass high efficiency PA design. To obtain an accurate model, the mode of operation of the transistor in the specific application must be considered. Unlike the traditional PAs, the transistor for high efficiency PAs operates in the on- and off-regions. This is illustrated in Fig. 2.5 where the loadline of a traditional class-AB PA is compared with the loadline of high-efficiency PA. In general, the available transistor models are optimized for class-AB operation. This implies that the model may not be accurate in the high-efficiency loadline region.

In [Paper A] and [Paper B], an in-house model optimized for high efficiency operation is developed for the bare-die transistors. The extracted model is based on simplified expressions for the nonlinear currents and capacitances where focus is put on accurately predicting on- and off-regions where the high-efficiency loadline is located [49]. As mentioned in section 1.2, the PA is used in
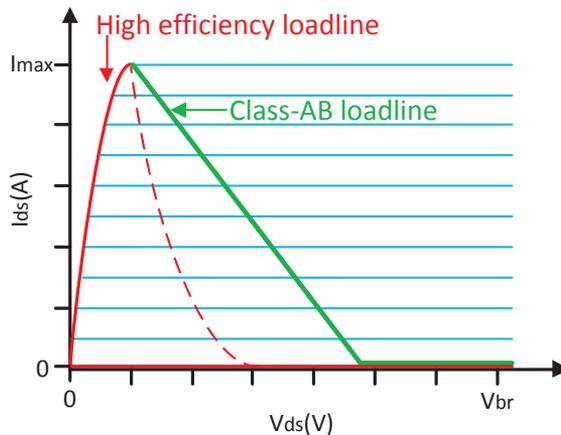
**Fig. 2.5:** Loadline of class-AB and switched-mode operation.

a high efficiency architecture which keeps the PA in saturation for a large output power dynamic range, therefore the linearity and the agreement in backoff were not taken much into consideration. The model has been extracted from DC- and S-parameter measurements referred to the die surface reference plane. The simplified expressions ensure a good convergence during simulations and an excellent accuracy in high-efficiency PA operation. Moreover, the model permits the intrinsic waveforms to be inspected during simulations and therefore allows a careful study of the transistor operation which is usually not possible with commercial models.

### 2.2.3 Circuit design methodology

As mentioned in section 2.1.2, the high efficiency PAs impose different tailored waveforms for drain-current and drain-to-source voltage, respectively. These waveforms can be obtained by the control of the harmonic content of the voltage and current waveforms at the transistor intrinsic terminals. The procedure that we have followed for optimizing the fundamental and harmonic impedances is summarized below:

Step 1 Perform a fundamental load-pull/source-pull simulation to find the optimum fundamental load and source impedances that maximize the efficiency. The harmonic loads can be initially set to values like open or short circuit.

Step 2 Using the impedances found in the previous step, perform a harmonic load-pull/source-pull simulation to find the optimum second and third harmonic load and source impedances for high efficiency operation. Step 1 is then repeated to re-optimize the fundamental impedances so the influence of the new harmonic impedances are taken into account.

Step 3 Design of suitable matching networks that provides those impedances at the device input and output terminals.

Step 4 Check the intrinsic voltage and current waveforms excursions to prevent dangerous operation, and to verify that the overlap between the waveforms is minimized.

Step 5 Perform MC and EM simulations to study the reliability and the robustness of the design and thus, to ensure first-pass design. We perform EM simulations on the TL parts to ensure accurate synthesis of the input and output matching networks, while MC simulations study the uncertainties introduced by the lumped components and the manufacturing process.

A stability network has to be designed to stabilize the PA and to avoid any oscillation in band or at low frequencies. The stabilization network can be designed either before starting step 1 or after completing step 3 by modifying the input matching network. To improve the stability in the high-frequency band, a series resistance can often be added at the input of the amplifier. A parallel resistance is also needed to reduce the low-frequency gain and hence to increase low-frequency stability.

In the next section, the proposed design procedure is validated by the design and implementation of two high efficiency PAs operating at 3.5 GHz and 5.5 GHz.

## 2.3   3.5 GHz Inverse Class-F power amplifier design example

In paper [A], a 3.5 GHz, high efficiency inverse class-F PA is presented. This PA demonstrates excellent efficiency performance considering the output power, the particular topology and transistor generation used. The parasitic lead inductances and package tab parasitic capacitances degrade the performance in high frequency applications. Thus, in our design and following the discussion in Section 2.2.1, we use bare-die (unpackaged) devices in order to eliminate the effects of the package and get maximum performance. In this design, a 15 W GaN-HEMT bare-die device from Cree [56] is used.

A simplified transistor model, optimized for SMPAs, is developed in-house and used in the PA design. The model is based on simplified expressions for the nonlinear currents and capacitances where focus is put on accurately predicting the high efficiency, on- and off-regions of the transistor characteristics. The model allows the intrinsic waveforms to be studied in the PA design and therefore allows a careful investigation of the transistor operation. Using the transistor model, the optimum impedances have been determined using the procedure presented in section 2.2.3. Fig. 2.6 shows the simulated intrinsic drain voltage and current waveforms of the transistor (obtained when the transistor see the determined optimum impedances). We notice that the drain voltage waveform is a half-sinusoid whereas the drain current waveform is close to a square wave, which correspond to the inverse class-F waveforms (see Fig. 2.2(b)).

The input and output matching networks were designed to provide, at the fundamental and harmonics, the optimum impedances obtained from the
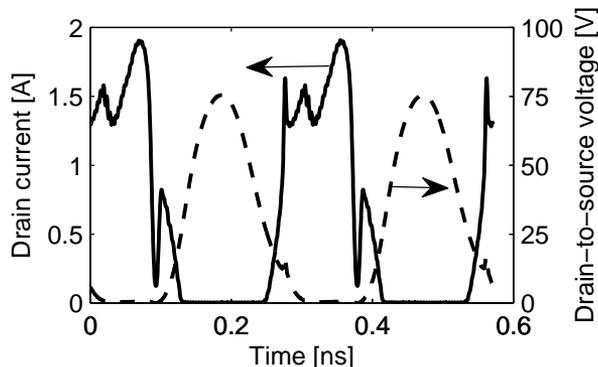
**Fig. 2.6:** Simulated intrinsic current and voltage waveforms of the transistor resulting in 80 % PAE at 3.5 GHz.
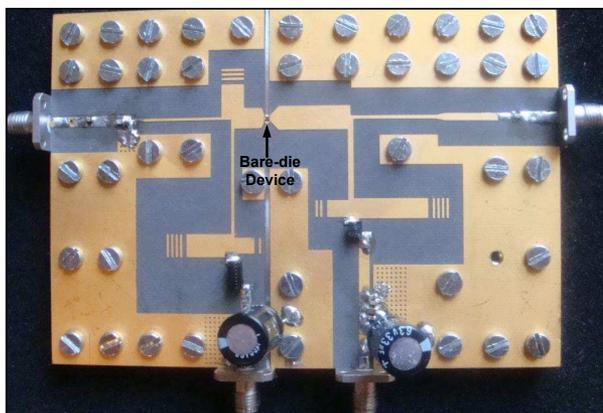


**Fig. 2.7:** Fabricated inverse class-F 3.5 GHz PA. Size: $11 \times 8cm^2$.

source/load pull simulations. Details about the circuit design is presented in [Paper A]. A photo of the implemented PA is shown in Fig. 2.7.

It is important to remind here that the intention was to obtain the highest peak efficiency in this design. The optimization result of the proposed method has lead to inverse class-F. Moreover, the recent published work on high efficiency PAs are demonstrating peak results in this mode of operation. These results demonstrate that inverse class-F is an excellent mode of operation for maximum peak efficiency at these frequencies using GaN-HEMT devices.

### 2.3.1 Static measurements

Large signal measurements have been performed in order to evaluate the PA performance under static conditions and to evaluate the agreement vs. circuit simulations. A frequency sweep measurement between 3 GHz and 4 GHz has been performed to study the PA performance versus frequency. The PAE and

gain of the PA are plotted versus frequency in Fig. 2.8(a) and compared with simulations. A maximum gain and PAE of $12\,\mathrm{dB}$ and $78\,\%$ respectively are located at $3.5\,\mathrm{GHz}$ corresponding to a drain efficiency of $82\,\%$ at this frequency. The amplifier exhibits higher than $50\,\%$ PAE between $3.32\,\mathrm{GHz}$ and $3.72\,\mathrm{GHz}$, which corresponds to greater than $10\,\%$ fractional bandwidth. Fig. 2.8(b) shows the simulated and measured gain and PAE versus input power. A peak PAE of $78\,\%$ is measured for an input drive level of $29\,\mathrm{dBm}$. As expected, good agreement between simulation and measurement results is obtained at high power levels, where the transistor is operated in a high efficiency mode that the model was optimized for.
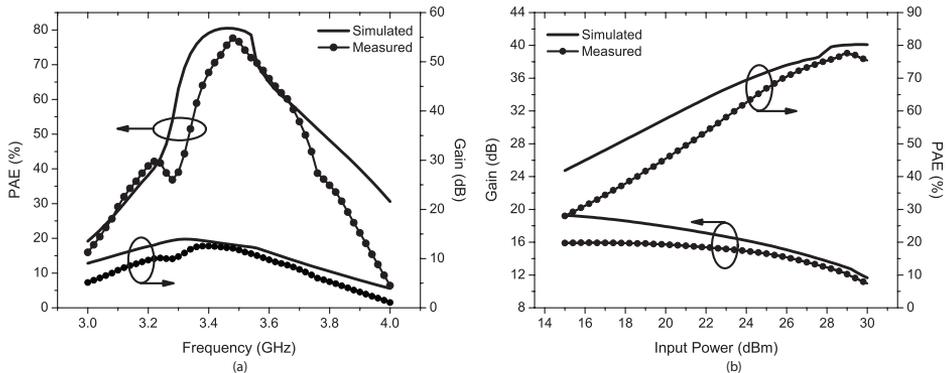


**Fig. 2.8:** Simulated and measured (a) PAE and Gain vs. frequency for 29dBm input power; (b) PAE and gain vs. input power.

## 2.3.2   Linearized modulated measurements

The purpose was to design a PA for saturated applications and focus was on obtaining the highest peak efficiency. However, it is still interesting to investigate its performance in a linear application. Therefore, linearized modulated measurements have been performed using realistic input signals such as WCDMA and LTE.

AM-AM and AM-PM have been traditionally used to develop behavior models for the PA in which the output characteristic of the PA is approximated as a complex polynomial of instantaneous input power level [57]. However, as the bandwidth of the signal increases, memory effects in the transmitter become significant. Memory effects are attributed to the frequency response of the matching networks, nonlinear capacitances of the transistors, and the response of the bias networks [58]. In our work, we have used the memory polynomial model, presented in [57], that captures both memory effects and nonlinear behavior of the PA. The structure of the corresponding DPD scheme is shown in Fig. 2.9 where $U_n$ and $X_n$ are the input and output of the DPD function. The downconverted and normalized output of the PA, $Y_n$, is compared to $X_n$ for characterization of the PA.

The linearized modulated measurements were performed using the memory polynomial model. In the modulated experiments, both a $20\,\mathrm{MHz}$ LTE signal
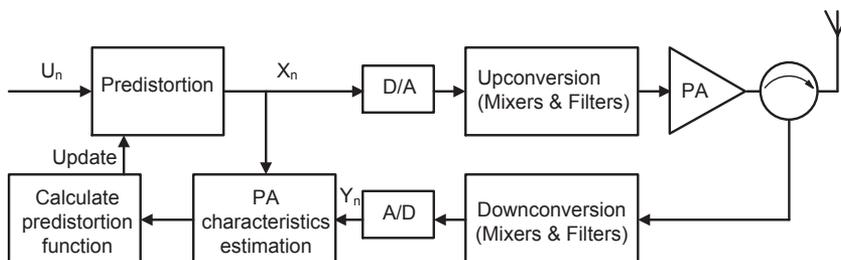
**Fig. 2.9:** Digital predistortion scheme [57].

with 11.2 dB Peak-to-Average Power Ratio (PAPR) and a 5 MHz WCDMA signal with 6.6 dB PAPR were used. The measured output spectrum at 3.5 GHz of the WCDMA and LTE signals, before and after DPD are shown in Fig. 2.10.
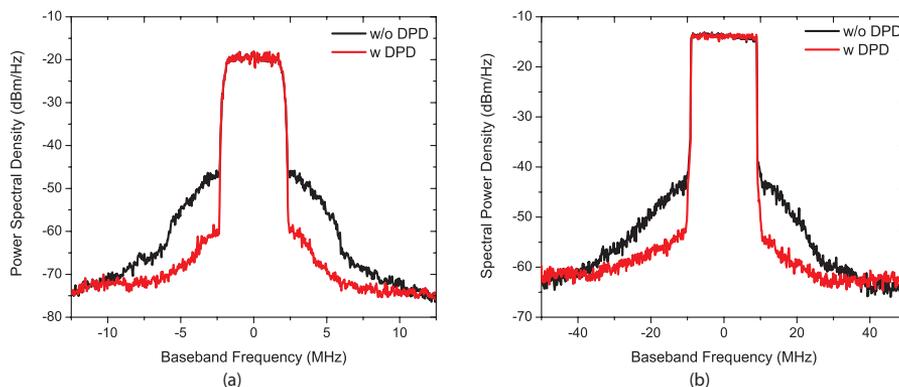


**Fig. 2.10:** PA output signal spectrum of at 3.5 GHz before and after DPD (a) 5 MHz WCDMA signal; (b) 20 MHz LTE signal.

Table 2.1 summarizes the average performance of output power and PAE obtained from these experiments, highlighting the minimum ACLR level as well. These results show that standard DPD methods can be used to linearize the PA to meet modern wireless communication system standards.

**Table 2.1:** Measured average output power, average PAE and minimum ACLR level, without (w/o) and with (w) DPD.

|  | Pout (dBm) | | PAE (%) | | ACLR (dBc) | |
|---|---|---|---|---|---|---|
|  | w/o | w | w/o | w | w/o | w |
| WCDMA | 35 | 34 | 45 | 40 | -34 | -47 |
| LTE | 33 | 32 | 35 | 30 | -32 | -44 |

## 2.4   5.5 GHz harmonically tuned power amplifier design example

After the successful validation of the design methodology at 3.5 GHz, we explored, in [paper B], the high frequency capabilities of the design methodology by the design of a harmonically tuned PA at 5.5 GHz. In the design, a 10 W GaN bare-die device from Triquint Semiconductors, Inc. has been used [59]. An in-house model optimized for high efficiency operation is developed for the bare-die transistor and used in the design. Using the design methodology presented in section 2.2.3, the simulations showed that the effect of the third harmonic on the efficiency is very small. This is expected since the third harmonic frequency in this case is very high (16.5 GHz) and effectively short circuited by the output capacitance. Therefore, the source and load impedances at fundamental and second harmonic have been considered in the design of the matching networks.
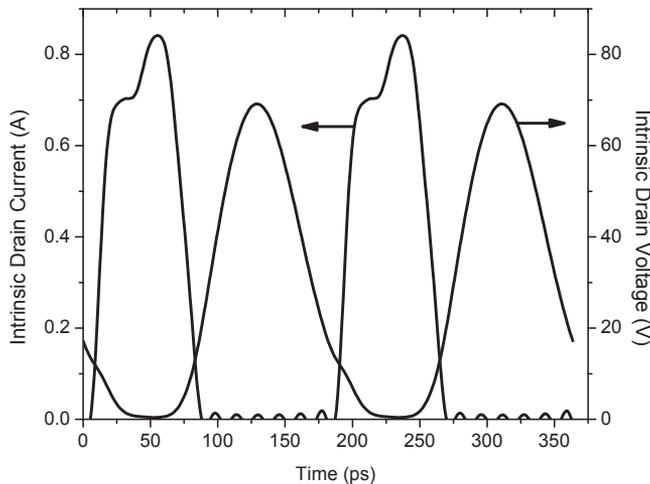


**Fig. 2.11:** Simulated intrinsic current and voltage waveforms.

To verify the high efficiency operation of the PA, it has been simulated and the intrinsic waveforms are shown in Fig. 2.11. These waveforms correspond to 75 % simulated PAE. Investigation of the waveforms confirm that the voltage/current overlap is minimized which explains the high efficiency obtained. Finally, Fig. 2.12 shows a picture of the PA that has been implemented on the same substrate as the 3.5 GHz-PA.

The main difference of this design compared to the 3.5 GHz-PA is that the effect of the third harmonic was not taken into consideration. Comparing the intrinsic waveforms of the two PAs, we notice the squaring effect of the third harmonic on the drain current in Fig. 2.6, however, this effect is very small for the 5.5 GHz-PA in Fig. 2.11.

The performance of the implemented PA has been evaluated by means of large signal measurements. The PA has been characterized versus frequency between 5.2 GHz and 5.8 GHz with 25 dBm input power drive level. The results
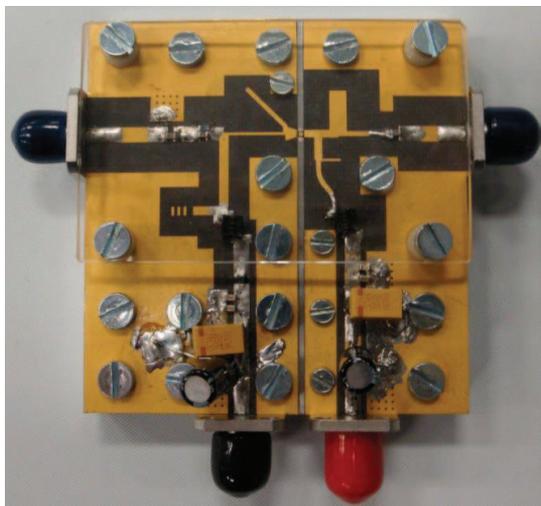
**Fig. 2.12:** Fabricated harmonically tuned 5.5 GHz PA. Size: $6 \times 6 cm^2$.



(a)

(b)
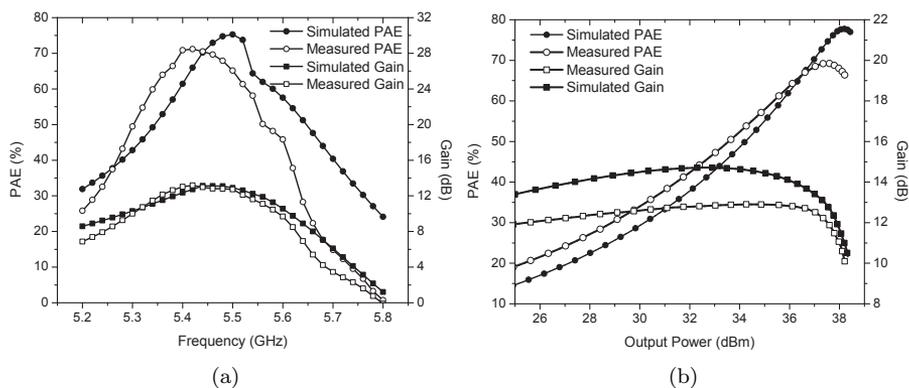
**Fig. 2.13:** Simulated and measured (a) PAE and Gain vs. frequency for 25 dBm input power (b) PAE and gain vs. output power.

presented in Fig. 2.13(a), show that a maximum gain of 12.5 dB is located at 5.42 GHz with a corresponding 70 % PAE. Fig. 2.13(b) shows measured gain and PAE versus output power at 5.42 GHz while the presented simulations are performed at 5.5 GHz. The output power compresses at 37.5 dBm and the PAE reaches 70 % PAE.

## 2.5 Performance comparison

The performance of the PAs presented in [paper A] and [paper B] is compared to recently published highly efficient GaN-HEMT based PAs in S- and C-bands [28, 51–55, 60–77]. In Fig. 2.14(a) we notice that the PA in [paper A] outperforms all published S-band PAs in terms of PAE except for the ones published in [51, 61, 66]. However, as shown in Fig. 2.14(a), the operating

frequency of the amplifier published in [51, 61](2 GHz) is much lower than our operating frequency (3.5 GHz). [66] has same operating frequency of the PA in [paper A], slightly higher PAE but lower output power. Moreover, as depicted in Fig. 2.14(c), it has been published three years after the the PA in [paper A]. In Fig. 2.14(a), we notice that for similar frequency of operation in C-band, the PA in [paper B] has similar PAE performance as the one published in [77] but outperforms all the other published PAs.
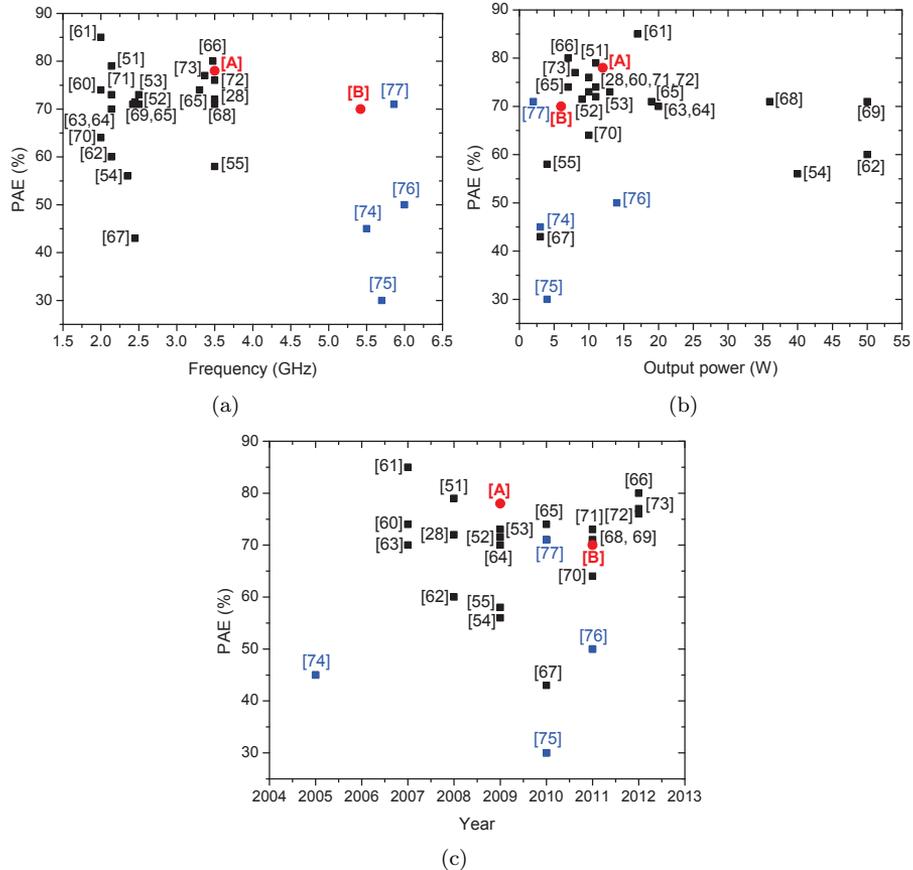


**Fig. 2.14:** State-of-the-Art PAs using GaN-HEMT technology in S- and C-band, (a) PAE vs. frequency; (b) PAE vs. output power; (c) PAE vs. year of publication.

In conclusion, the 3.5 GHz-PA presented in [paper A] and the 5.5 GHz-PA presented in [paper B] are among the best published PAs in S- and C-bands respectively. Therefore, these results demonstrate the success of the selected bare-die mounting, modeling, and circuit design methodologies used to implement PAs with high peak efficiency performance.

# Chapter 3

# High efficiency wideband power amplifier design

Due to the narrowband spectrum allocations, the design of PAs for wireless communications has traditionally been targeted for low RF bandwidths similar to the ones presented in Chapter 2. However, modern and future wireless systems will require larger spectrum allocations to support increased data rates [5]. Moreover, efficient wideband PAs are needed to reduce the operational costs of multi-standard transmitters. This makes wideband PAs that cover many frequency bands while maintaining high efficiency a hot research topic.
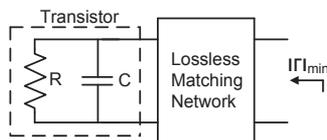


**Fig. 3.1:** Network for which Bode-Fano limit applies.

One of the important factors for designing wideband PAs is the device technology. The output impedance of the device is usually characterized by a shunt $R - C$ circuit. Using a lossless network as shown in Fig. 3.1, Fano [14] describes the best theoretical match that can be achieved across a bandwidth to a load. He demonstrated that the bandwidth, over which a good match of a complex load impedance can be obtained, is limited. A fundamental limitation, for a parallel $R - C$ network is derived in [14] and given below:

$$\int_0^\infty \frac{1}{\mid \Gamma \mid} d\omega \preceq \frac{\pi}{RC}.  \tag{3.1}$$

Solving for the reflection coefficient $\mid \Gamma \mid$, we obtain [14]:

$$\Delta\omega \ln \frac{1}{\mid \Gamma \mid} \preceq \frac{\pi}{RC}.  \tag{3.2}$$

This result shows that the bandwidth over which a good match is obtained is limited by the $RC$ product.

Since LDMOS RF power transistors, which are the devices currently used in base stations, have large output capacitance, according to (3.2), the design of wideband power amplifiers is very challenging. The impedance at the interface of the transistor die can be lower than $1\,\Omega$. Thus, it is very difficult or impossible to achieve the necessary high $Q$ transformation to $50\,\Omega$ across a wide bandwidth. Referring to section 1.3.1, the impedances at the interface of the recently developed GaN RF power transistors are much larger which opens up possibilities for wideband designs. Compared to LDMOS, the output capacitance of a GaN-HEMT is reduced by almost an order of magnitude for a given output power [78]. Hence, according to (3.2), GaN with its lower capacitance is easier to match over a wider bandwidth.

In the remainder of this chapter, an overview of different conventional broadband PA topologies are reviewed. Then, a proposed design approach for wideband PAs and a systematic method for the design of suitable broadband matching networks is presented. They are validated through the design of a high efficiency 2-4 GHz octave bandwidth PA. Then, a novel push-pull harmonic load-pull measurement setup is proposed to investigate the potential of broadband push-pull PAs for microwave applications and a prototype 1-3 GHz push-pull PA has been implemented for this purpose.

## 3.1  Broadband power amplifiers

In this section, different techniques used for designing broadband amplifiers in hybrid or monolithic technologies will be reviewed. Traveling wave distributed circuit, lossy matched circuit, and feedback circuit are among the most popular techniques. Other approaches to design wideband high power and efficiency PAs that have been recently published will also be discussed.

### 3.1.1  Traveling wave amplifier

The problem of the input and output capacitances of the transistor that is limiting broadband match, is overcome in the Traveling Wave Amplifier (TWA), also referred to as distributed amplifier, by incorporating the input and output capacitances of several transistors into an artificial transmission-line structure as shown in Fig. 3.2. The amplifier consists of an input line incorporating the input capacitances of the transistors and an output line incorporating the
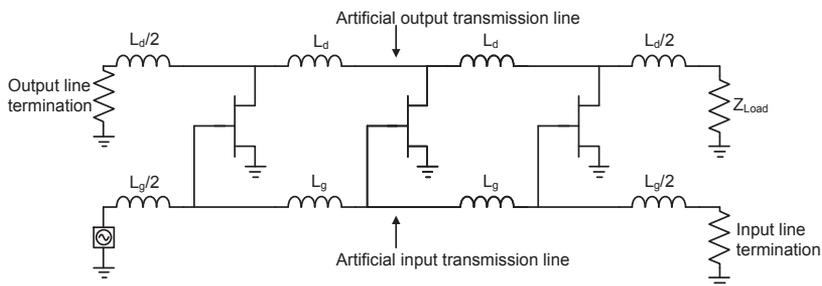


**Fig. 3.2:** Circuit topology of the traveling wave amplifier.

output capacitances. By amplifying the signal at the input line and feeding it to the output line, a broadband amplifier from low frequencies to the cut-off frequency of the artificial lines can be obtained [79].

The main advantages of the TWA are the simple circuit topology and the achievable wide bandwidth. Multi-octave and even multi-decade TWAs have been already demonstrated [80, 81]. However, the disadvantages of this approach lie in the high number of active devices needed to achieve the same gain as of a single device which results in large size and high manufacturing cost. Moreover, its low output power results in low PAE performance [80–82].

### 3.1.2 Lossy matched amplifier

The lossy matched amplifier uses resistors within its input- and output-matching networks in order to guarantee flat gain over a wide bandwidth [83]. Fig. 3.3 illustrates the lossy matched amplifier. The resistors help increasing the impedance levels and thus according to (3.2) enable more wideband operation.
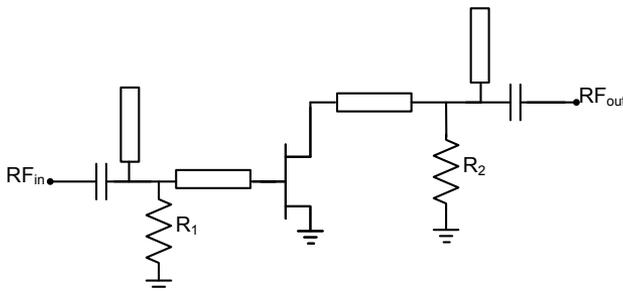


**Fig. 3.3:** Circuit topology of the lossy amplifier.

A theoretical analysis of this configuration is presented in [83]. Simulations results show that the gain, up to 5 GHz, of a single stage lossy matched amplifier is the same as for a four-stage traveling wave amplifier. Moreover, its PAE is at least four times higher than the four stage TWA [83]. However, its moderate bandwidth compared to a TWA is its main disadvantage.

### 3.1.3 Feedback amplifier

The feedback amplifier, shown in Fig. 3.4, employs a negative feedback by connecting a resistor $R_{fb}$ between the gate and drain of the transistor [84]. This, helps stabilizing the device and makes the input and output impedances much closer to the desired $50\,\Omega$ [79]. The value $R_{fb}$ controls the gain and bandwidth of the amplifier. $L_{fb}$ and $L_2$ can be optimized to extend the amplifiers bandwidth [85]. $L_1$, $C_1$, and $C_2$ are used to achieve very good input and output return loss [79]. In comparison with the TWA, the feedback amplifier is less complex and gives higher PAE. The main disadvantage of this type of amplifier is its low output power due to loss associated with the feedback resistor.

When implemented with discrete components, the frequency response of the feedback amplifier can be very sensitive, therefore it is mainly implemented
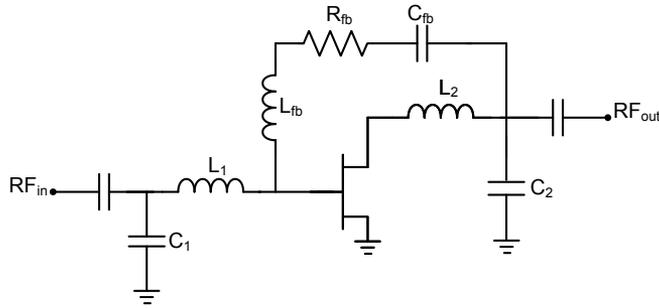
**Fig. 3.4:** circuit topology of the feedback amplifier.

in MMIC technology [85]. A recent attempt to design a hybrid wideband high efficiency feedback power amplifier is presented in [38]. The results showed a decade bandwidth (0.3 GHz-3 GHz) but the obtained output power levels and PAE (20%-40%) are quite low.

### 3.1.4   Amplifiers with resistive harmonic terminations

Another approach used to design wideband PAs is based on the optimization of the fundamental impedance while resistive terminations are presented for high order harmonics. Using this approach, it is possible to achieve multioctave bandwidths, however, leading to low efficiency levels.

In [86], a 10 W octave bandwidth (0.7-1.5 GHz) PA using lumped matching networks is presented. However, the design approach does not involve any harmonic tuning, which explains the low PAE levels obtained (30-35 %).

A 2 W, mutli-octave (0.8-4.0 GHz) PA in GaN technology is presented in [87]. The design approach is similar to Class-AB using matching networks. The results show a gain and PAE less than 7 dB and 40 % respectively.

In [88], a decade bandwidth (0.4-4.1 GHz) PA, using a Chebychev transformer to design the wideband matching networks, is presented. The gain and PAE are between 10-15 dB and 40-60 %, respectively.

### 3.1.5   Wideband switched-mode power amplifiers

The techniques presented previously offer wide bandwidth but not the required high efficiency levels. To increase the efficiency, techniques like harmonic tuning [4, 43] or switching mode [44] should be used as discussed in Chapter 2.

In this context, many wideband class-E PAs are reported in literature. A wideband class-E PA using synthesized low-pass matching networks operating between 1.2-2.0 GHz is presented in [89]. Two Class-E power amplifiers, with moderate bandwidth (2.0-2.5 GHz), are presented in [18] and [19]. The design approach is similar to conventional Class-E PA but using a wideband matching network. The PAE levels obtained are approximately 50 % and 70 % respectively. The difference in performance is due to the technology, where the former is a MMIC PA while the latter is a hybrid design using a bare-die technique. As we notice, such amplifiers have modest bandwidth because

the required harmonic terminations cannot be realized over large bandwidths due to the device parasitics and the required high quality factor matching networks.

### 3.1.6 Continuous modes power amplifiers

Recently, continuous modes of operation have been explored for class-B/J [48], class-F [90] and inverse class-F [91] PAs. The investigations demonstrated that a continuum of PAs modes, with high constant efficiency over a continuous range of fundamental and harmonic terminations, exists. In [48], it has been demonstrated that starting from class-B mode, a continuum of solutions between class-B and class-B/J allow high efficiency performance when the fundamental and second harmonic impedances are manipulated. Similar study, conducted on class-F PAs [90], shows that controlling the fundamental and second harmonic impedances can lead to better performance than class-B/J mode in terms of output power, efficiency and bandwidth. Moreover, for inverse class-F [91] PAs, it is shown that changing simultaneously the susceptance of fundamental and the second harmonic termination, constant high efficiency and high output power levels can be maintained over wide bandwidth.

Circuit demonstrators of continuum class-B/J, -F modes have been implemented. However, this is not the case for continuum inverse class-F mode. In [20], a 10 W wideband Class-B/J PA demonstrates 60-70 % efficiency across 1.35-2.25 GHz. Two Class-B/J PAs are presented in [92], where the first PA covers 1.6-2.2 GHz with 55-68 % efficiency while the second covers 0.5-1.8 GHz with 50-69 % drain efficiency. The practical behavior of continuous class-B/J modes for high power ranges is successfully investigated in [93], where 53-63 % efficiency and 60-75 W output power are obtained across 0.9-2.3 GHz. A continuum class-F PA [94], demonstrated at low frequencies 0.55-1.1 GHz, achieves 9-13 W output power and 65-80 % drain efficiency.

A mode-transferring technique for designing high-efficiency wideband PAs is presented in [95]. The adopted matching network provides wideband fundamental matching and proper tuning of the second and third harmonics that allow the PA to operate between inverse class-F and class-F modes. The implemented 1.3-3.3 GHz PA demonstrates high efficiency at 1.8 GHz and 2.8 GHz where the PA operates in inverse class-F and class-F modes. However, the efficiency drops by about 25 % across the rest of the band.

## 3.2 Harmonically tuned wideband PA design approach

In this section, we present a design approach for high-efficiency PAs limited to one octave bandwidth. The approach, presented in [paper C], is based on realizing the optimal fundamental and second harmonic impedances derived from harmonic sourcepull/loadpull simulations. Moreover, a detailed method for the design of suitable broadband matching network solutions will be presented.

### 3.2.1    Design approach

The suggested approach can, in general, be used to design any wideband PA. However, the achieved bandwidth depends strongly on the type of device used as discussed in the introduction of this chapter. The main steps are enumerated hereafter:

Step 1 Perform a fundamental load-pull/source-pull simulation (or load-pull measurement) to find the optimum source and load impedances that maximize the device's efficiency performance. Repeat for a number of frequencies spanning the bandwidth of interest.

Step 2 The effect of the second harmonic on the performance is very critical; therefore this step consists of varying the impedance of the second harmonic, at different frequencies, across the periphery of the Smith-chart while the device sees the optimum source and load impedances obtained in step 1 at the corresponding frequency. This step determines the region where the second harmonic maximizes the efficiency.

Step 3 The device output impedance can be approximated by a shunt $R - C$ circuit. This step consists of determining, from the optimum impedances found in step 1, the load line $R$ and the output capacitance of the transistor $C$. For simplicity, the values of $R$ and $C$ can be calculated from the optimum impedance at the center frequency of the band.

Step 4 A wideband matching network should be designed to match the determined $R - C$ circuit to $50\,\Omega$ across the bandwidth.

Step 5 The second harmonic of the designed wideband matching network must be checked to verify that it is located in the region that maximize the efficiency as determined by step 2.

Step 6 In case the second harmonic is degrading the performance, the designed network must be modified so it can take care of the second harmonic impedance.

This procedure is illustrated with a practical design of a high efficiency GaN-HEMT octave bandwidth, 2-4 GHz, PA in [paper C]. Step 1 is performed by doing load-pull/source-pull simulations to find the optimum impedances at 2, 2.5, 3, 3.5, and 4 GHz. A typical example, of how the first step may look in practice, is illustrated in Fig. 3.5(a).

Step 2 of this procedure is performed by varying the impedance of the second harmonic, at different frequencies, across the periphery of the Smith-chart while the device sees the optimum source and load impedances at 3 GHz. A practical example of how the PAE of the device versus the phase variation of the unity magnitude second harmonic reflection coefficient may look is shown in Fig. 3.5(b). We notice that PAE is dramatically degraded when the phase of the second harmonic approaches the short circuit region (180 °). This means that there is no need for additional design efforts for the second harmonics if the matching network does not approach the short circuit region.

In the following section, Step 4 of the proposed procedure is addressed by presenting a systematic method to design a wideband matching network.
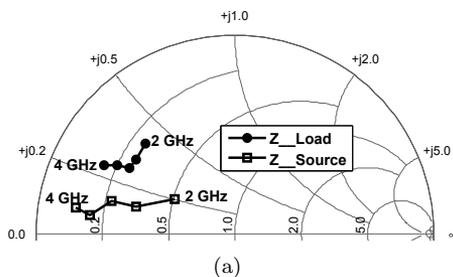
(a)
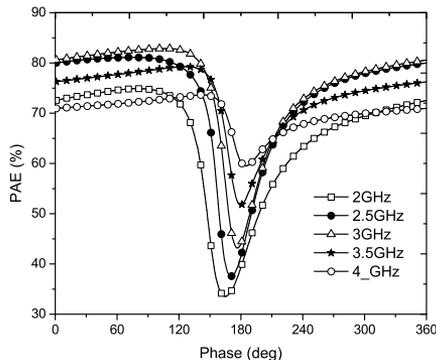


(b)

**Fig. 3.5:** (a) Efficiency optimized source and load impedances (b) Simulated PAE versus phase of the unity magnitude second harmonic reflection coefficient.

## 3.2.2 Wideband matching network design

Fano [14,96], derived exact simultaneous transcendental equations for the design of wideband matching networks. However, these equations appeared to need computer iteration for their solution. Fortunately, an analytic solution of these equations has been recently derived in [97]. Starting from the solutions of these equations, a step-by-step derivation of a wideband lumped element network is presented. Then, the lumped network is approximated by a corresponding distributed network in realization of a practical circuit.

The output impedance of the device of a power transistor is typically a parallel $R-C$ circuit, where $R$ is much lower than $50\,\Omega$. The required equations for the design of the lumped network are given in detail in this section since they were not presented in [Paper C] due to lack of space. However, it is important to note that if the transistor impedance is modeled as a series $R-C$ circuit instead, similar approach can be also used. However, new equations must be derived.

The normalized admittances, $g$ elements, for the prototype low-pass matching network, Fig. 3.6(a), can be calculated using equations found in [97]. They represent a low-pass filter in a $1\,\Omega$ system with $1\,\text{rad/s}$ corner frequency. The low-pass prototype network corner frequency is scaled from the nominal $1\,\text{rad/s}$ to the design value $(\omega_c)$ by dividing the elements by $2\pi(f_2 - f_1)$ [97], where
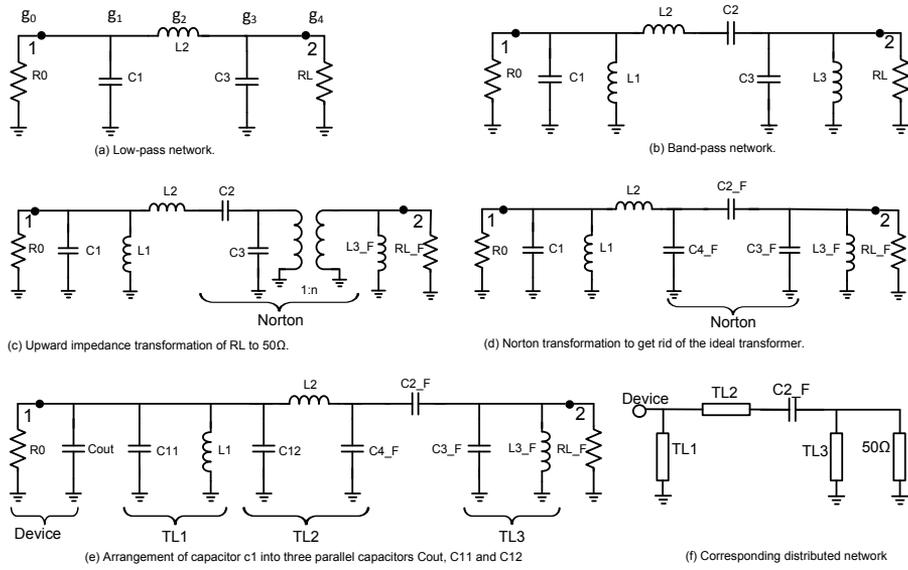
**Fig. 3.6:** Step by step third order lumped matching network design and its equivalent distributed network.

$f_1$ and $f_2$ are the lower and upper bandpass frequencies respectively. For impedance scaling, the series elements $g_0$, $g_2$, and $g_4$ are multiplied by $R$ while the shunt elements $g_1$ and $g_3$ are divided by $R$.

$$C_1 = g_1/2\pi(f_2 - f_1)R_0, \tag{3.3}$$

$$L_2 = g_2R_0/2\pi(f_2 - f_1), \tag{3.4}$$

$$C_3 = g_3/2\pi(f_2 - f_1)R_0, \tag{3.5}$$

$$R_L = g_4R_0. \tag{3.6}$$

Applying the above scaling formulas, the values $C_1$, $L_2$, $C_3$, and $R_L$ can be obtained and hence, the low-pass network Fig. 3.6(a). The low-pass network is transformed into a bandpass network, by resonating each series or shunt element at the geometric mean frequency $2\pi\sqrt{f_1f_2}$ [97]. The bandpass network is shown in Fig. 3.6(b) and the resonating elements are given by:

$$L_1 = 1/4\pi^2 f_1 f_2 C_1, \tag{3.7}$$

$$C_2 = 1/4\pi^2 f_1 f_2 L_2, \tag{3.8}$$

$$L_3 = 1/4\pi^2 f_1 f_2 C_3, \tag{3.9}$$

An ideal transformer with an impedance transformation ratio of $50/R_L$ is inserted at the output. By shifting the transformer to the left as shown in Fig. 3.6(c), $R_L$ is transformed to $50\,\Omega$ and $L_3$ is scaled upwards in impedance.

$$R_{L\_F} = n^2 R_L, \tag{3.10}$$

$$L_{3\_F} = n^2 L_3. \tag{3.11}$$

A Norton transformation is then used to remove the ideal transformer by transforming it, together with the two capacitors $C_2$ and $C_3$, into a $\Pi$ arrangement of capacitors as shown in Fig. 3.6(d) [98]. The values of the resulting capacitors $C_{2\_F}$, $C_{3\_F}$, and $C_{4\_F}$ are given by the following formulas:

$$C_{2\_F} = C_2/n, \tag{3.12}$$

$$C_{3\_F} = (C_3 + (1-n)C_2)/n^2, \tag{3.13}$$

$$C_{4\_F} = (n-1)C_2/n. \tag{3.14}$$

By applying equations (3.3)-(3.14), all the element values in Fig. 3.6(d) can be determined and therefore, matching to $50\,\Omega$ over a wide bandwidth can be achieved. The capacitor $C_1$ can be replaced by three parallel capacitors; $C_{11}$, $C_{12}$, and the transistor output capacitance $C_{out}$ as shown in Fig. 3.6(e). Finally, some transformations between lumped and distributed elements, well explained in [Paper C], have been used to transform the lumped elements matching network into the final distributed network shown Fig. 3.6(f).

## 3.3  Wideband power amplifier design example

The design approach of high efficiency wideband PA presented in previous sections, is validated through the design, manufacturing, and test of an octave bandwidth 2-4 GHz PA. The design is described in detail in [Paper C], but summarized below.

### 3.3.1  2-4 GHz power amplifier design

By calculating the inverse of the conjugate value of the optimum fundamental load impedance obtained at $3\,\text{GHz}$, a load line of $R_0 = 32\Omega$ and a transistor output capacitance of $C_{out} = 2.4\text{pF}$ can be estimated. In summary, the matching network should therefore be designed to match $R_0$ and $C_{out}$ to $50\Omega$ across the 2-4 GHz bandwidth. Using the method presented in the previous section a wideband lumped element matching network have been derived for the output side and finally converted to a distributed matching network. An analogous procedure has been used for the input matching network.

Fig. 3.7 shows the impedance of the output matching network as well as the impedance of the second harmonic. We notice that the second harmonic is
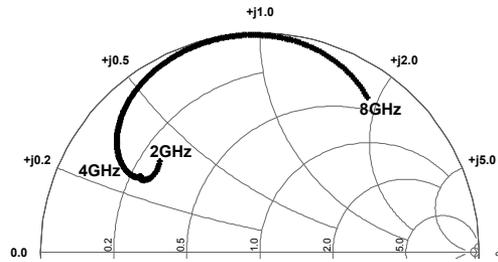
**Fig. 3.7:** Simulated impedance of the distributed output matching network versus frequency. The fundamental and second harmonic impedance frequency ranges are given by 2-4 GHz, and 4-8 GHz, respectively.

far away from short circuit and hence, according to the results in Section 3.2, high PAE performance is expected across the bandwidth.

The resulting PA topology is shown in Fig. 3.8(a). The input and output matching networks are surrounded by the dashed and solid boxes respectively. The output matching network is dominated by $TL_6 - TL_8$ and $C_5$, which are given by the network in Fig. 3.6(f). $TL_1$ and $TL_5$ are short transmission lines added to facilitate the physical connections to the transistor die. The input matching network has been slightly modified in order to stabilize the PA. The series resistance $R_{g2}$, and the parallel resistance $R_{g3}$, are added at the input of the amplifier to improve the stability in the high and low frequency bands, respectively. $L_{bwg}$ and $L_{bwd}$ are used to model the input and output bondwire inductances respectively. Finally, the inductors $L_g$ and $L_d$ are used to prevent the leakage of RF into the DC supply lines. The PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and a thickness of 0.4 mm. Its size is $65 \times 65 \, \text{mm}^2$. Fig. 3.8(b) shows a picture of the fabricated PA using the bare-die GaN-HEMT device.



(a)                              (b)
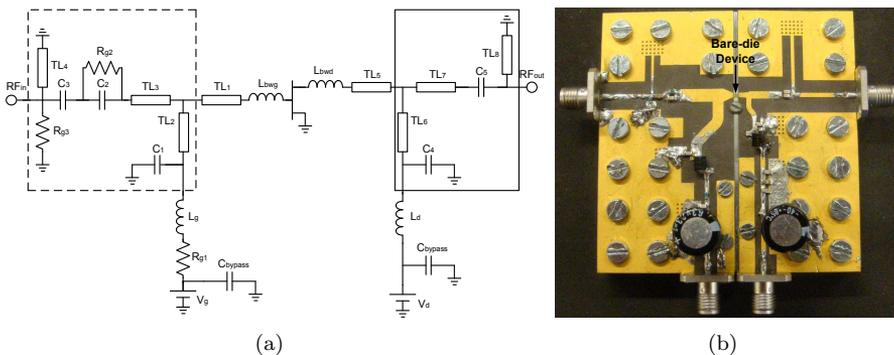
**Fig. 3.8:** (a) PA topology; the dashed rectangle represent the input matching network while the solid rectangle surrounds the output matching network (b) Photo of the implemented wideband PA.

### 3.3.2 Static measurements

Large signal CW measurements have been performed in order to evaluate the PA performance under static conditions. In Fig. 3.9-(a) and Fig. 3.9-(b) the PA performance in terms of output power and drain efficiency is plotted versus frequency, for a fixed input power of $31\,$dBm. The results show an output power between $40 - 42$dBm in the frequency range of $1.9\,$GHz-4.3 GHz which means that less than $2\,$dB ripple in the output power, and hence in the power gain, is obtained across the band. Within the same band the drain-efficiency of the amplifier is between $57\,\%$ and $72\,\%$. This corresponds to a PAE between $50\,\%$ and $63\,\%$ and a fractional bandwidth of $78\,\%$ about a center frequency of $3.1\,$GHz. It is important to note that the simulations and measurements agree well, which validates the models and design methods used.

Fig. 3.9-(c) and Fig. 3.9-(d) show the power gain and the PAE plotted versus output power at 2, 2.5, 3.5, $4\,$GHz. We notice that in Fig. 3.9-(d), the gain decreases at low input power levels. The reason behind this behavior is that the gate bias voltage used in the measurements is selected slightly below the pinch-off voltage in order to maximize the peak efficiency. To get a constant back-off gain, the gate bias must be slightly increased.
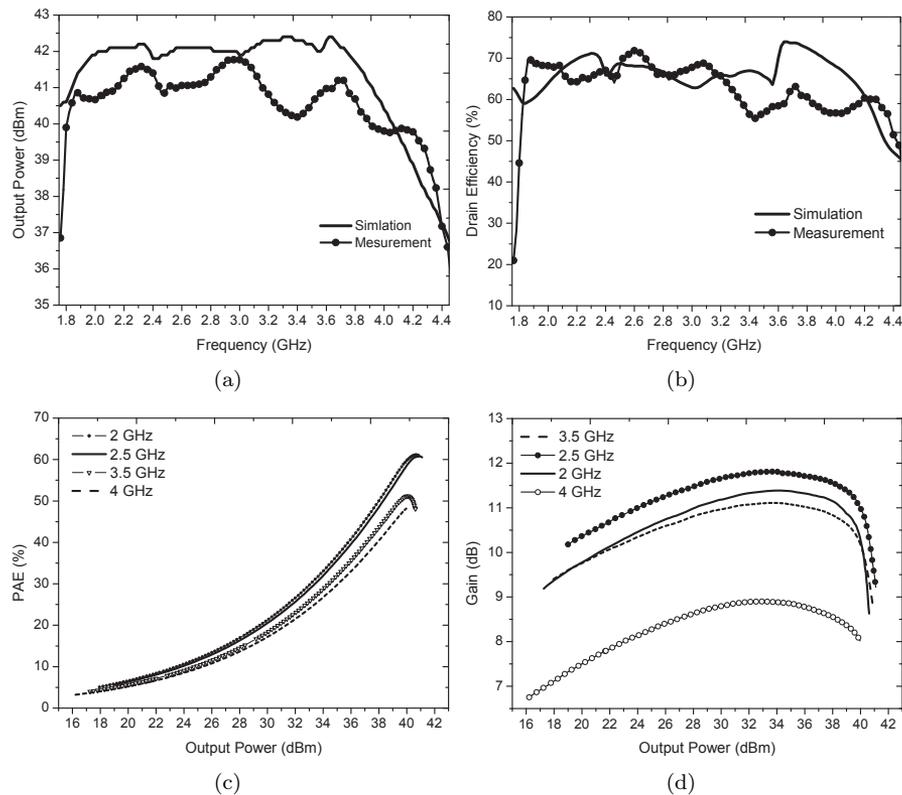


**Fig. 3.9:** (a) output power vs. frequency for a fixed input power of $31\,$dBm (b) drain efficiency vs. frequency for a fixed input power of $31\,$dBm (c) PAE vs. output power at 2, 2.5, 3.5 and $4\,$GHz (d) gain vs. output power at 2, 2.5, 3.5 and $4\,$GHz.

### 3.3.3   Performance comparison

The performance of the presented PA is compared to recently reported wideband amplifiers in Table 3.1.

We notice that the PA in [19, 94] have higher efficiency than the PA in [Paper C]. However, the PA in [Paper C] has larger bandwidth and higher operating frequency.

In [38, 87, 88], the reported PAs have higher relative bandwidth compared to the PA reported in [Paper C]. However, the gain, the output power, and the efficiency in [Paper C] are much higher.

**Table 3.1:** State-of-the-Art Wideband Power Amplifiers, $f \geq 500\,\text{MHZ}$, $P_{out} \geq 1\,\text{W}$

| Reference | BW(GHz) | BW(%) | Pout(W) | Gain(dB) | Drain Eff(%) |
|---|---|---|---|---|---|
| 2006 [18] | 1.9-2.4 | 23 | 5-7 | 9-10 | 57-62 |
| 2008 [87] | 0.8-4.0 | 133 | 1-2 | 5-7 | 40-55 |
| 2008 [86] | 0.7-1.5 | 73 | 9-10 | 10-11 | 33-38 |
| 2009 [19] | 2.0-2.5 | 22 | 7-12 | 10-13 | 74-77 |
| 2009 [20] | 1.3-2.2 | 50 | 9-11 | 11-12 | 60-70 |
| 2010 [38] | 0.3-3.0 | 163 | 5-10 | 5-10 | 25-50 |
| 2010 [21] | 1.9-2.9 | 42 | 35-50 | 10-12 | 60-65 |
| 2011 [99] | 1.3-2.7 | 70 | 10-15 | 10-12 | 56-70 |
| 2011 [94] | 0.55-1.1 | 67 | 9-13 | 9-12 | 65-80 |
| 2011 [100] | 1.0-2.0 | 67 | 60-90 | 9-11 | 30-65 |
| 2011 [101] | 0.9-2.2 | 84 | 10-20 | 10-13 | 63-89 |
| 2012 [95] | 1.3-3.3 | 87 | 10-14 | 11-12 | 58-86 |
| 2012 [93] | 0.9-2.3 | 87 | 60-75 | 11-12 | 53-63 |
| 2012 [88] | 0.4-4.1 | 164 | 10-15 | 10-15 | 40-62 |
| 2012 [92](a) | 1.6-2.2 | 33 | 10-13 | 10-12 | 55-68 |
| 2012 [92](b) | 0.5-1.8 | 113 | 8-12 | 12-15 | 50-69 |
| [Paper C] | 1.9-4.3 | 78 | 10-15 | 9-11 | 57-72 |

The PAs reported in [95, 101] outperform the PA in [Paper C] in terms of bandwidth and efficiency. However, their measurements were performed at variable drain bias voltage. At each frequency, the drain bias voltage was optimized to get the highest possible efficiency performance. Moreover, the variation in the efficiency performance across the bands of both PAs is exceeding 25 %.

The PAs reported in [92, 93] outperforms the PA in [Paper C] in terms of bandwidth and output power. However, their efficiency and operating frequencies are lower. Regarding the other reported PAs, our PA outperforms all of them in terms of bandwidth, efficiency and operating frequencies. This comparison shows that the PA in [Paper C] has state-of-the-art efficiency, bandwidth and output power performance for GaN PAs covering the S-band.

In conclusion, the PA in [Paper C] shows an excellent performance in terms of output power, gain, efficiency and linearity. This performance demonstrates the success and the usefulness of the proposed approach for the design of wideband PAs for future wireless systems combining wide bandwidth and high efficiency.

## 3.4   Push-pull microwave power amplifiers

The design methodology presented above is valid for PAs with octave bandwidth or lower. It cannot be extended for more than one octave because the harmonics fall inside the required bandwidth and hence harmonic tuning will not possible. To overcome this problem, the push-pull design technique that allows second harmonic tuning over bandwidths exceeding one octave can be used. The principle of operation of push-pull PAs is therefore first reviewed.

### 3.4.1   Principle of operation

The push-pull PA consists of two devices driven differentially so that the equivalent circuit shows the two devices being driven in antiphase [4]. To combine the branches of the two devices and to achieve the required phase shift, push-pull PAs require baluns to be connected at the input and output of the PA.

To illustrate the principle of operation, consider a differential ideal T-section network connected between the two devices as shown in Fig. 3.10(a). The T-network is composed of a differential impedance $Z_D$ and a common-mode conductance $Y_C$. The behavior of the circuit at even harmonics will be different from its response at fundamental and odd harmonics. The fundamental and odd harmonics voltage components of each PA will be equal in amplitude, but opposite in phase. Consequently, a virtual ground develops at the line of symmetry at the center of the differential impedance so the devices share the impedance $Z_D$, and hence, the equivalent circuit in differential mode will be equivalent to the one shown in Fig. 3.10(b). However, at the even harmonics, the harmonic voltage components are equal in amplitude and phase. Therefore, the line of symmetry becomes a virtual open circuit and the devices share the conductance $Y_C$ as shown in Fig. 3.10(c).

Thus, the advantage of the presented push-pull topology comes from the different responses at even and odd harmonics. They add a degree of freedom

that allows fundamental and second harmonic frequency impedances both to be optimized without the bandwidth restrictions in a single-ended design.
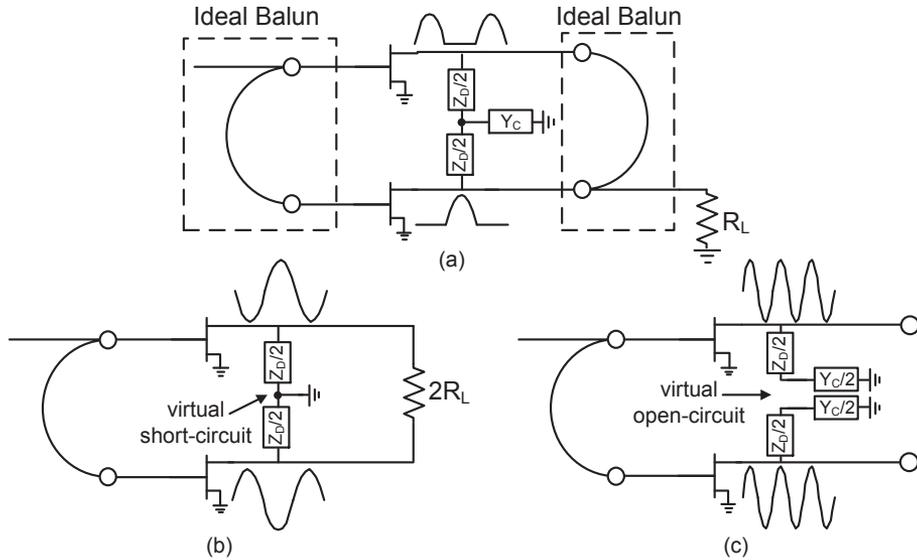


**Fig. 3.10:** Push-pull with a T network load, (a) circuit topology, (b) equivalent circuit at fundamental and odd harmonics, (c) equivalent circuit at even harmonics.

### 3.4.2    Push-pull microwave power amplifiers in literature

Generally, broadband push-pull PAs were mostly targeted for low frequency applications [102–105]. At microwave frequencies, different push-pull architectures have been proposed. A push-pull PA using periodic structures for harmonic tuning is proposed in [106] while a push-pull PA based on an extended resonance technique is presented in [107]. The benefit of separating the effects of the even and odd harmonic frequencies in push-pull configurations is used in [108] by the simple connection of a pair of inverse class-F PAs and in [109] by the connection of a pair of the newly introduced class-E/F PAs. However, the mentioned architectures were targeted for narrowband applications because the realization of broadband baluns at microwave frequencies is very challenging [4].

Recently, efforts have been put to design broadband balun suitable for common mode operation at microwave frequencies [110]. Moreover, using this latter balun, a decade bandwidth push-pull PA has been demonstrated in [22]. The PA operates between 250 MHz and 3.1 GHz with a drain efficiency higher than 45 %. This result demonstrates the bandwidth potential of the push-pull configuration at microwave frequencies. However, in general, there is a lack in understanding the true operation and interaction between push-pull PAs and output baluns. In [Paper D], we propose a push-pull harmonic load-pull measurement setup that allows the influence of the balun on PA performance to be investigated in detail under realistic push-pull operating conditions.

**Fig. 3.11:** Proposed push-pull harmonic load-pull setup.

### 3.4.3   Investigation of push-pull microwave power amplifiers

In the following, the proposed measurement setup, the implemented push-pull PA used in the experiments, and the results of the study that investigates the influence of the balun characteristics on the overall PA characteristics are presented.

#### 3.4.3.1   Proposed push-pull harmonic load-pull setup

The push-pull harmonic load-pull setup, developed for our experimental investigations and shown in Fig. 3.11, is based on an active load-pull technique [111–114]. It can provide, at the calibrated reference plane, any impedance for fundamental and second harmonic frequencies, as well as measuring the voltage and current waveforms at fundamental and all harmonics. A Large Signal Network Analyzer (LSNA, Maury/NMDG MT4463) is used to measure the traveling voltage waves $a_1$, $b_1$, $a_2$ and $b_2$ at the calibrated reference plane. The fundamental ($f_0$) input signal to the PA is generated with a synthesized CW RF signal generator. Two automated mechanical tuners (Maury MT982) are used to present the required impedance for fundamental frequencies at the calibrated reference plane. Then, in order to set the load reflection coefficient at the second harmonic ($2f_0$), another synthesized CW RF signal generator is used. The amplitude and phase control of the injected signal at the second harmonic is achieved by using vector modulators.

The proposed setup will be used to emulate a balun at the output of a push-pull PA and to study the effect of the balun on the PA performance. This kind of measurement cannot be performed by measuring the output branches of the PA independently with a traditional harmonic load-pull setup because, according to Fig. 3.10, the matching networks seen at the fundamental and second harmonics look different and they are only different when the other branch is operated in a balanced mode.

Based on the measured voltage waveforms, the performance of the push-pull PA can be easily calculated

$$P_{out} = \underbrace{\frac{\mid b_1 \mid^2}{2Z_0}}_{\text{upper PA branch}} + \underbrace{\frac{\mid b_2 \mid^2}{2Z_0}}_{\text{lower PA branch}} \tag{3.15a}$$

$$\eta = \frac{P_{out}}{P_{dc}} \tag{3.15b}$$

$$Gain = \frac{P_{out}}{P_{avs}} \tag{3.15c}$$

where $Z_0$ is the impedance of the single-ended PA branch. $P_{dc}$ and $P_{avs}$ are the total DC power consumption and the available input power, respectively.

### 3.4.3.2   1-3 GHz push-pull power amplifier prototype

The prototype PA used in the investigation uses the same operational principle described in section 3.4.1. As shown in its topology depicted in Fig. 3.12, the push-pull PA consists of two identical PA branches and a balun. Each PA is a wideband single-ended PA, designed following the same approach used in Sec 3.2. The two PAs are connected at the input through a commercial balun [115]. However, the output is kept in balanced configuration to be able to study the effect of the balun on the performance of wideband PAs. The two, $TL_e$, output lines are added to facilitate the connection to the output; they are not a part of the matching networks and they will be de-embedded during the measurements.
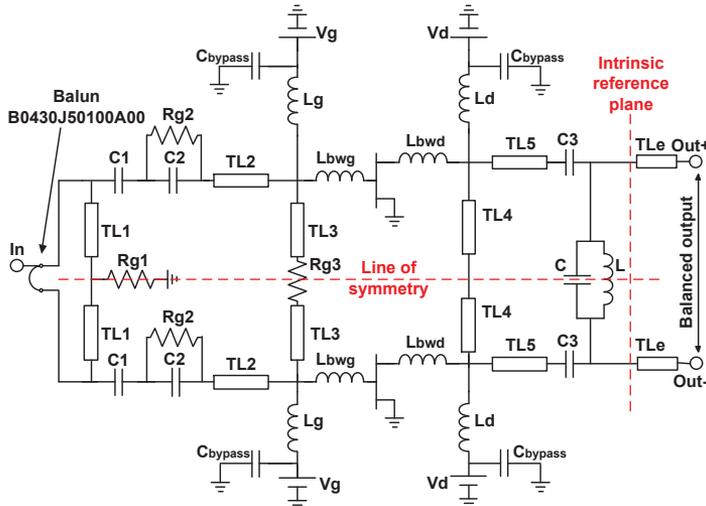


**Fig. 3.12:** Proposed push-pull power amplifier topology.

The push-pull PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of $0.8\,\text{mm}$. Its size is $65 \times 55\,\text{mm}^2$. Fig. 3.13 shows a photo of the fabricated push-pull PA using bare-die GaN-HEMT devices.
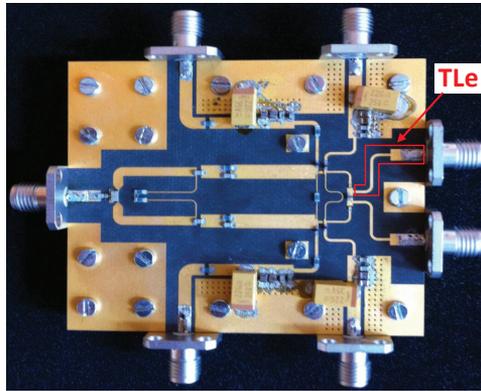
**Fig. 3.13:** Photo of the implemented wideband push-pull power amplifier.

### 3.4.3.3 Experimental results
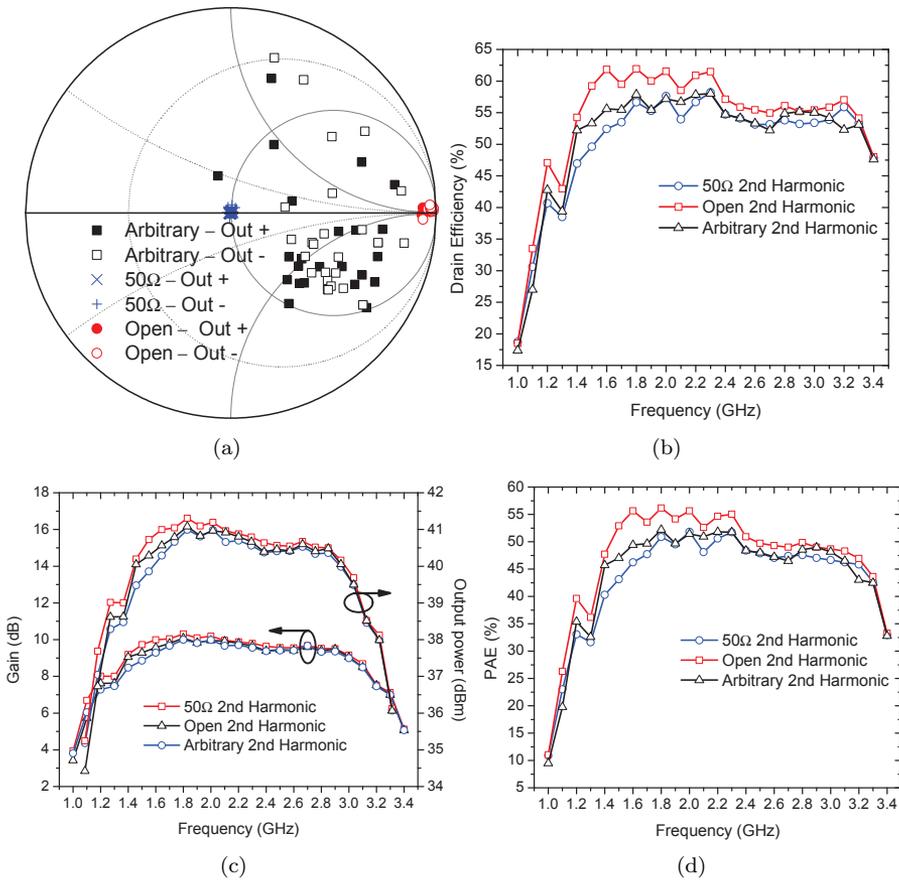


**Fig. 3.14:** Measured performance for a fixed input power of 31 dBm (a) output power versus frequency (b) drain efficiency vs. frequency (c) output power and gain vs. frequency (d) PAE vs. frequency.

The measurement setup presented above has been used to accomplish the push-pull load-pull measurements at the intrinsic reference plane indicated in Fig. 3.11.

The PA was firstly characterized versus frequency between $1\,$GHz and $3.4\,$GHz. Three different terminations of the second harmonic impedance of the output balun have been used. The realized terminations for the second harmonic (common mode) impedance were: Open, $50\Omega$, and arbitrary impedances as shown in Fig. 3.14(a). The arbitrary impedances are obtained when no signal is injected at the second harmonic. Fig. 3.14(b), Fig. 3.14(c), and Fig. 3.14(d) show the measured frequency response of the push-pull PA for three different terminations. It is clear that the common mode second harmonic termination of the output balun has big impact on the performance of the PA, in particular for the lower frequencies where the second harmonic falls within the fundamental frequency range. The drain efficiency is improved at certain frequencies by $10\,\%$ when open termination is used instead of $50\Omega$ and about $5\,\%$ when arbitrary termination is realized.

In case of the open second harmonic, the measured output power is between $38 - 41$dBm in the frequency range of $1.3\,$GHz-$3.3\,$GHz which means that the power gain, is between $7 - 10$dB. Within the same band the drain-efficiency of the PA is between $45\,\%$ and $63\,\%$. This corresponds to a PAE between $40\,\%$ and $57\,\%$ and a fractional bandwidth of $87\,\%$ about a centre frequency of $2.3\,$GHz.

Many conclusions can be drawn from the results obtained in [Paper D]. The investigation shows that the setup allows the interaction between the push-pull PA and balun operation to be isolated from each other and is therefore an important tool for such investigations. Moreover, although the push-pull operation can separate the fundamental and second harmonic impedances, the problem is instead to design an output balun that avoids the common mode second harmonic reflection phases that degrade the efficiency. The common mode frequency response of the balun, like the one presented in [22], needs to be carefully mapped to the areas where high efficiency can be preserved. The fundamental bandwidth limitations imposed by the balun (or balanced antenna) common mode impedance response is still matter for future research where the setup proposed in [paper D] can play an important role.

# Chapter 4

# High efficiency dual-band Doherty power amplifier design

In the previous chapters, the focus was on maximizing the high peak efficiency of single-band and wideband PAs. The peak efficiency of the PA is obtained close to its saturated output power. However, as shown in Fig. 1.3(b), the efficiency of the PA decreases dramatically as the signal power is backed-off.

In fact, the never-ending demand on increasing data traffic and achieving higher data rate transfer resulted in nonconstant envelope modulation schemes. The high PAPR of the involved signals causes the PA to operate at an average output power far below the saturation region resulting in low average efficiency levels. Among the different techniques proposed to increase the average efficiency, the Doherty PA has demonstrated to be a promising and effective solution [10]. It operates at a nearly constant efficiency for a targeted range of input and/or output power levels, typically of 6 dB [10, 12, 24, 27, 116–118].

So far, lot of work has been done on single-band DPAs [12, 23–32]. However, this does not satisfy the multi-band and multi-standard requirements of modern and future RBSs as discussed in section 1.1. Some efforts have been put to increase the bandwidth of the DPA by using reconfigurable matching networks [119] or by exploiting wideband matching networks [120–125]. However, the experimental results showed that the obtained bandwidths are still not wide enough to cover many bands at the same time. Moreover, another drawback is that, wideband DPAs do not always have ideal operation over the bandwidth of operation. This leads to significant degradation in the DPA performance compared to the case where DPAs are designed for single frequency operation.

To overcome these limitations, dual-band DPAs arise as a good candidate because the flexibility of choosing the operating bands. Moreover, the performance of the dual-band DPAs can be similar to single-band DPAs since the passive networks can be optimized simultaneously for the two operating bands. Recently, there have been some efforts to optimize a DPA for dual-band operation [33, 35, 89]. However, they present architectural overviews without any comprehensive or general design methodology. In the following, a detailed

design methodology for high efficiency dual-band DPAs is presented.

## 4.1   Design approach

The DPA basic operational principle will be reviewed before thoroughly presenting the design approach of dual-band DPAs.

### 4.1.1   Conventional Doherty power amplifier

A simplified diagram of the conventional Doherty power amplifier is shown in Fig. 4.1. It consists of two current sources representing the Main amplifier and Auxiliary amplifier, and quarter-wavelength impedance transformer ($Z_T$. The load seen by each current source ($Z_M$ and $Z_A$) is controlled by the current level of the other one ($I_M$ and $I_A$). The quarter-wavelength impedance transformer acts as an impedance inverter. Thus, when the current supplied by the Auxiliary amplifier ($I_A$) increases, the load impedance of the Main amplifier, $Z_M$, decreases.
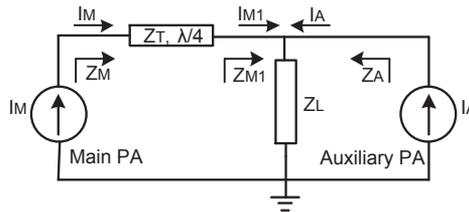


**Fig. 4.1:** Simplified schematic of the Doherty power amplifier.
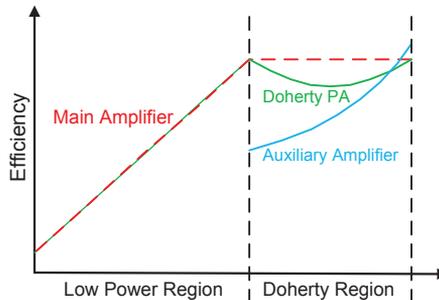


**Fig. 4.2:** Efficiency behavior of Main, Auxiliary and Doherty amplifiers.

Two different regions, according to the power level, can be distinguished in the DPA operation; the low power region and the Doherty region. At the low power region, the Main amplifier is only active, and hence the load modulation does not appear. When the Main amplifier reaches its maximum efficiency, the Auxiliary amplifier is turned on and the load impedances of the amplifiers are varied according to the current ratio. As the input power increases, $Z_M$ and $Z_A$ decrease respectively from $Z_T^2/Z_L$ and $\infty$ to both reach $R_{opt}$, which is the load impedance for the maximum output power. The theoretical expected

behavior of drain efficiencies of the Main and Auxiliary amplifiers and the one of the DPA are shown in Fig. 4.2.

A general block diagram of the conventional DPA is shown in Fig. 4.3. It is composed of the Main and Auxiliary amplifiers that are connected through an Input Power Splitter (IPS), Phase Compensation Network (PCN), an Impedance Inverter Network (IIN), and an Impedance Transformer Network (ITN).
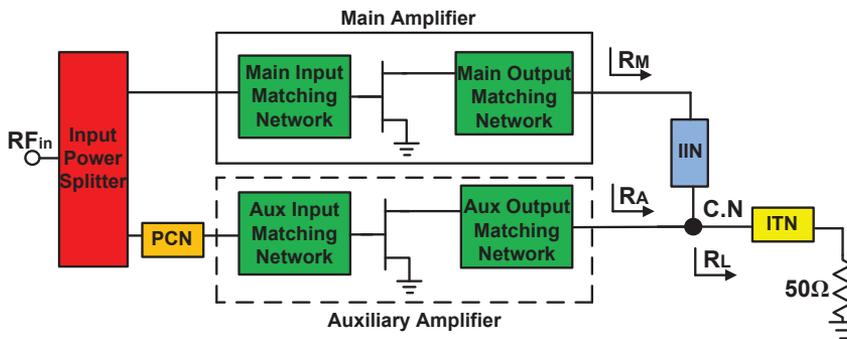


**Fig. 4.3:** Circuit topology of conventional Doherty power amplifier.

## 4.1.2 Dual-band design of the passive structures

To obtain a dual-band operation in a DPA, the passive structures, such as Main and Auxiliary matching networks, IPS, PCN, IIN, and ITN, must be designed to ensure Doherty behavior in both frequency bands.

### 4.1.2.1 Impedance inverter network

The IIN must function as a quarter wave impedance transformer, at the two frequency bands, independently of the termination impedance. using a T- or a Π-network, shown in Fig. 4.4, an equivalent quarter-wave length TL of characteristic impedance $Z_0$ can be realized at two uncorrelated frequencies $f_1$ and $f_2$. Design equations for the T-network are derived in [126]. For the Π-network, a similar method to the on in [126] is used to derive the design equations. In the design equations for the T- and Π-networks, the integers $n$ and $m$ should be selected accounting for physical constraints, i.e. realizability and dimension of the resulting TLs. Moreover, depending on the chosen $n$ value, the phase response of the T- and Π-networks may be different at the two operating frequencies as shown in Table 4.1.

**Table 4.1:** Phase shift introduced by the different structures of Fig. 4.4

| | $T - Shape$ | $\Pi - Shape$ $n$ odd | $n$ even |
|---|---|---|---|
| $phase\,(S_{21})\,@f_1$ | $-90°$ | $-90°$ | $-90°$ |
| $phase\,(S_{21})\,@f_2$ | $+90°$ | $-90°$ | $+90°$ |
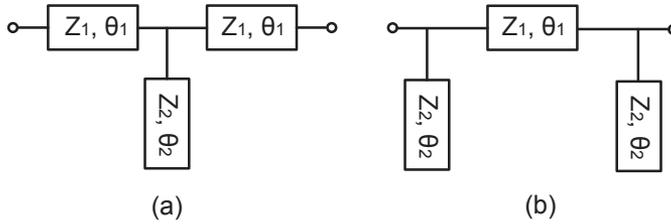
**Fig. 4.4:** Dual-Band impedance inverter network: a) T-network; b) Π-network.

#### 4.1.2.2   Impedance transformer network

The ITN is used to transform the output load $(50\,\Omega)$ to the required resistance value, at the DPA common node (C.N.) as shown in Fig. 4.3. The T- and Π-networks used for the IIN can be used for the ITN as well. However, a much simpler transformer exists [127]. It is formed by two TLs, with characteristic impedances $Z_1$, $Z_2$ and electrical lengths $\theta_1$, $\theta_2$ as depicted in Fig. 4.5. It can achieve ideal impedance matching at any two arbitrary frequencies.
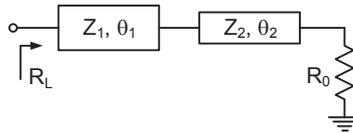


**Fig. 4.5:** Dual-Band impedance transformer network. The load $R_0$ is transformed to a resistance $R_L$.

#### 4.1.2.3   Input power splitter and phase compensation network

The Wilkinson divider [128] and the Branch-Line Coupler (BLC) [129] are the most used power dividers allowing an input power signal to be equally or unequally divided, to the output ports, while ensuring high isolation between the output ports. In principle, to create the dual-band dividers, the dual-band T- or Π−networks shown in Fig. 4.4 are used. The main difference between the two dividers is the phase relationship between the two output ports. The Wilkinson divides the output power in phase while the BLC introduces a 90° phase shift. The relative phase shifts between the signals of the two output ports of the different dual-band IPS are summarized in Table. 4.2.

To ensure proper Doherty operation, the phase shift introduced at the two frequencies by the IIN has to be compensated by suitable IPS-PCN structure. If The IPS is realized through a BLC, then the PCN is directly integrated in this element, providing the correct output port connections. Conversely, if Wilkinson structure is adopted, then a suitable PCN is required at the input of the Auxiliary or Main amplifiers. In this case, the required PCN network can be realized by using one of the dual-band structures presented in Section 4.1.2.2.

**Table 4.2:** Phase shift between the two output ports of the input power splitter

| Dual-Band IPS | Phase Difference | $T - Shape$ | $\Pi - Shape$ | |
|---|---|---|---|---|
| | | | $n$ odd | $n$ even |
| Wilkinson | $\Delta\phi$ @ $f_1$ | $0°$ | $0°$ | $0°$ |
| | $\Delta\phi$ @ $f_2$ | $0°$ | $0°$ | $0°$ |
| Branch-Line | $\Delta\phi$ @ $f_1$ | $-90°$ | $-90°$ | $-90°$ |
| | $\Delta\phi$ @ $f_2$ | $+90°$ | $-90°$ | $+90°$ |

#### 4.1.2.4 Dual-Band DPA Topologies

In this section, the possible configurations to implement a dual-band DPA will be reviewed. Each configuration is selected so the structures adopted for the realization of the passive networks ensure in-phase addition of the output signals from the Main and Auxiliary amplifiers at the common node (C.N.). Referring to the data reported in Table 4.1 and Table 4.2, the possible configurations for realizing dual-band DPAs are summarized in Table 4.3.

**Table 4.3:** Dual-band DPA configurations

| | IPS | PCN | IIN |
|---|---|---|---|
| Wilkinson | $T$, $\Pi$, or Wideband | $T$ | $T$ <br> $\Pi$ (n-even) |
| | | $\Pi$ $(n - odd)$ | $\Pi$ $(n - odd)$ |
| | | $\Pi$ $(n - even)$ | $\Pi$ $(n - odd)$ <br> $T$ |
| Branch-Line | $T$ | - | $T$ <br> $\Pi$ $(n - even)$ |
| | $\Pi$ $(n - odd)$ | - | $\Pi$ $(n - odd)$ |
| | $\Pi$ $(n - even)$ | - | $T$ <br> $\Pi$ $(n - even)$ |
| | Wideband | - | $\Pi$ $(n - odd)$ |

The configurations that most closely resembles the general topology shown in Fig. 4.3, are certainly the ones that require the presence of a dual-band Wilkinson input divider, two dual-band quarter-wave TLs to realize the IIN and the PCN, and a two-section transformer to realize the ITN. However, in this case the overall structure of the DPA is very cumbersome, due to the simultaneous presence of a dual-band Wilkinson divider and two impedance inverters. A more compact solution can be obtained by selecting the configurations adopting a Branch-Line splitter, since the phase relation of the outgoing signals from the Branch-Line avoids the need of the PCN at the input of the Auxiliary amplifier.
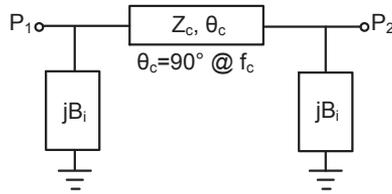
**Fig. 4.6:** Π-shaped network which is equivalent to a quarter-wave transmission line at two frequencies. $B_i$, $i = 1, 2$, represent the susceptances at the two frequencies.

### 4.1.3  Multi-band branch-line couplers

To extend the presented dual-band approach into multi-band approach, the passive structures must be designed to operate simultaneously at multiple bands. In this thesis, we have made a step towards the design of multi-band DPAs in the future by proposing a new design approach for multi-band BLCs. The single-band BLC is made of four quarter-wave TLs. Therefore, to obtain multi-band BLCs, the design of multi-band quarter-wave TLs must be considered first. These multi-band TLs can be used as well to realize the IIN and ITN in multi-band DPAs.

In [paper F], a closed-form design approach for multi-band BLCs for arbitrary operating at incommensurate frequencies is presented. The proposed method, presented hereafter, is validated by the design and implementation of dual-band, triple-band, and quad-band microstrip BLCs.

#### 4.1.3.1  Design approach

The approach starts from the dual-band quarter-wave TL topology then it is extended to any number of arbitrary incommensurate bands. The Π-network, shown in Fig. 4.6, can reproduce, at two arbitrary frequencies ($f_1$ and $f_2$), the behavior of a $\lambda/4$-TL having characteristic impedance $Z_T$ if [130]:

1. The electrical length of the series TL is 90° at the center frequency, $f_c = (f_1 + f_2)/2$.

2. Its characteristic impedance ($Z_c$) and the shunting elements ($B_i$) match the following conditions:

$$Z_{c,i} = \frac{Z_T}{\sin\left(\frac{\pi}{2} \cdot \frac{f_i}{f_c}\right)} \qquad (4.1)$$

$$B_i = \frac{1}{Z_c \tan\left(\frac{\pi}{2} \cdot \frac{f_i}{f_c}\right)} \qquad (4.2)$$

Since $Z_{c,1} = Z_{c,2}$ in (4.1), the parameter $Z_c$ in Fig. 4.6 is unique.

In case of three arbitrary frequencies ($f_1 < f_2 < f_3$), it is not possible to obtain a unique value for $Z_c$ from (4.1). For $f_c = (f_1 + f_3)/2$; the following values for $Z_c$ will be obtained:
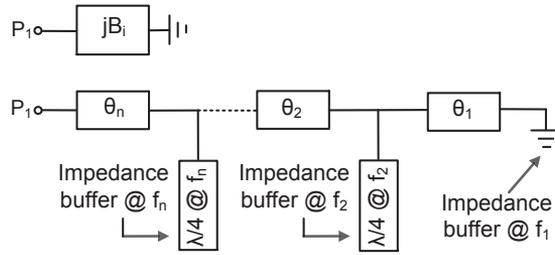
**Fig. 4.7:** Ladder network obtained applying the Impedance Buffer Methodology to synthesize the $B_i$ susceptances for a multi-band quarter-wave transmission line.

$$Z_{c,1\&3} = \frac{Z_T}{\sin\left(\frac{\pi}{2} \cdot \frac{f_{1\&3}}{f_c}\right)} \tag{4.3a}$$

$$Z_{c,2} = \frac{Z_T}{\sin\left(\frac{\pi}{2} \cdot \frac{f_2}{f_c}\right)} \tag{4.3b}$$

The best choice for $Z_c$ is an optimum value between $Z_{c,1\&3}$ and $Z_{c,2}$ that allows equal scattering parameter magnitudes to be obtained for the network in Fig. 4.6 at the three frequencies. Therefore, the optimum value of $Z_c$ should verify the condition $|S_{11}(f_{1\&3})| = |S_{11}(f_2)|$ for the network in Fig. 4.6. The derivation of the optimum value of $Z_c$, demonstrated in [paper F], leads to the following solution,

$$Z_c = \sqrt{Z_{c,1\&3} \cdot Z_{c,2}} \tag{4.4}$$

The approach can be easily generalized for an arbitrary number, $N$, of uncorrelated frequencies (i.e. $f_1 < f_2 < \cdots < f_m < \cdots < f_N$). Selecting $f_c = (f_1 + f_N)/2$, $N-1$ different values for $Z_c$ are obtained from 4.1: $\{Z_{c,1} = Z_{c,N},$ $Z_{c,2}, Z_{c,3}, \ldots, Z_{c,m}, \ldots, Z_{c,N-1}\}$ where $Z_{c,N}$ and $Z_{c,m}$ are the largest and smallest values among the available $Z_{c,i}$ values. By applying the same analysis applied in the case of three frequency bands, $Z_c$ becomes $Z_c = \sqrt{Z_{c,1\&N} \cdot Z_{c,m}}$ and the same matching condition, $|S_{11}(f_{1\&N})| = |S_{11}(f_m)|$, will be obtained at $f_1$, $f_N$ and $f_m$, where $f_m$ is the frequency corresponding to $Z_{c,m}$. The resulting value from $Z_c = \sqrt{Z_{c,1\&N} \cdot Z_{c,m}}$ is closer to the remaining $Z_{c,i}$ at the other frequencies, hence, the expected matching condition at the other frequencies is better than the one achieved at $f_1$, $f_m$ and $f_N$.

In our design, we use the impedance buffer approach [87, 131], shown in Fig. 4.7, to realize the obtained susceptances $B_i$. Starting from the input port of the network ($P_1$ in Fig. 4.7), the operating frequencies are controlled in descending order, i.e., from $f_N$ to $f_1$. The impedance buffers at $f_N \ldots f_2$ are realized by quarter-wave open circuit stubs, while the one at $f_1$ is obtained with a ground connection to reduce the size of the structure.

The single-band BLC is obtained by properly combining four single-band quarter-wave TLs. To achieve the multi-band BLC topology, each quarter-wave TL of the single-band BLC has to be replaced with the multi-band equivalent one, following the design methodology described above.

### 4.1.3.2    BLC circuit demonstrators

To verify the approach described above, the design of dual-, triple-, and quad-band BLCs has been carried out. The realized multi-band BLCs are shown in Fig. 4.8, while their performance in terms of simulated (schematic and EM simulations) and measured S-parameters is reported in Fig. 4.9.



(a)                              (b)                              (c)
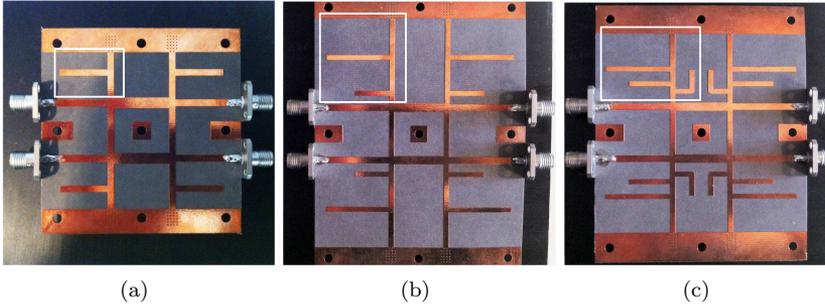
**Fig. 4.8:** Photos of the realized (a) dual-band, (b) triple-band (c) quad-band BLCs.

The performance of the three BLCs is degraded when passing from simulations with ideal elements to simulations with real elements. This can be attributed to the losses in microstrip lines and non-predicted behavior of actual cross/tee junctions. The measured results for the three BLCs, well in agreement with the theoretical and simulated ones, show satisfactory levels of matching, balance, and isolation at each of the operating bands. The results confirm the feasibility of the proposed design approach and highlights its usefulness for multi-band circuits and in particular for multi-band DPAs.



(a)                              (b)                              (c)
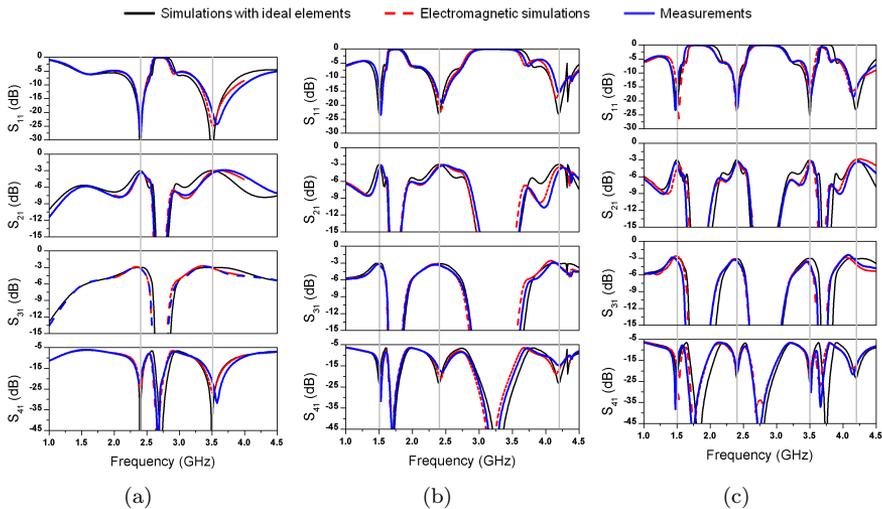
**Fig. 4.9:** Measured and simulated results of the (a) dual-band, (b) triple-band, and (c) quad-band branch line couplers.

A design example of dual-band DPA based on the proposed approach in section 4.1.2 is presented in the following.

## 4.2   Dual-band DPA circuit demonstrator

The design approach of dual-band DPAs is demonstrated through the design and implementation of a dual-band DPA operating at 1.8 GHz and 2.4 GHz. The DPA parameters have been theoretically inferred from the DC-IV curves of the device by applying the design approach in [24].

### 4.2.1   Dual-band Main PA design

The first step was to design the dual-band Main PA. Several concurrent dual-band PA architectures have been investigated and reported in recent years [132–136]. However, the design approach we use in our design is similar to the one proposed in section 2.2, but applied at the two operating frequencies. Load-pull/source-pull simulations were performed to find the optimum load and source impedances fulfilling the intrinsic load conditions at 1.8 GHz and 2.4 GHz, respectively. Harmonic load-pull/source-pull simulations were also



**Fig. 4.10:** Photo of the realized dual-band Main PA.

performed to further improve the efficiency performance. The latter simulations showed that only the second harmonic at the output has big influence on the performance. Therefore, in the design of the input matching network, only the fundamental frequencies have been considered, while the fundamental and the second harmonic have been considered in the design of the output matching network. The Main PA, shown in Fig. 4.10, has been implemented and tested in [Paper E]. It has been characterized versus frequency for a fixed input power of 30 dBm. The measured peak PAE, shown in Fig. 4.11(a), is 64 % in the two bands, with a measured output power of 42.3 dBm at 1.8 GHz
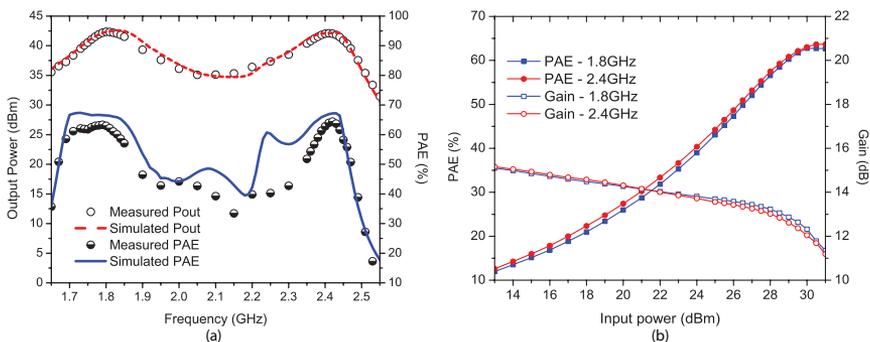


**Fig. 4.11:** Performance of the dual-band PA (a) Measured and simulated PAE and gain vs. frequency (b) Measured PAE and gain versus output power.

and 42 dBm at 2.4 GHz. Fig. 4.11(b) shows measured gain and PAE versus input power at 1.8 GHz and 2.4 GHz, respectively. It can be noticed the performance and behavior of the PA are similar in the two operating bands. The performance is in general very well predicted by the simulations, which is important when considering the use of this design in the more complex design of a dual-band DPA.

## 4.2.2   Dual-band DPA design

The same structure of the Main PA has been replicated for the Auxiliary PA and the remaining passive networks of the DPA have been designed. For the IIN, a Π-network with $n = 3$ has been adopted. For the IPS, a wideband topology [137] has been used to reduce the design sensitivity related to practical frequency shifts occurring in the realization of other passive networks. Moreover, the selected topology provides the same phase-shift introduced by the IIN at the two operating frequencies. Finally, the two section dual-band impedance transformer discussed in Sec. 4.1.2.1 is adopted for the ITN. A photo of the manufactured dual-band DPA is shown in Fig. 4.12.
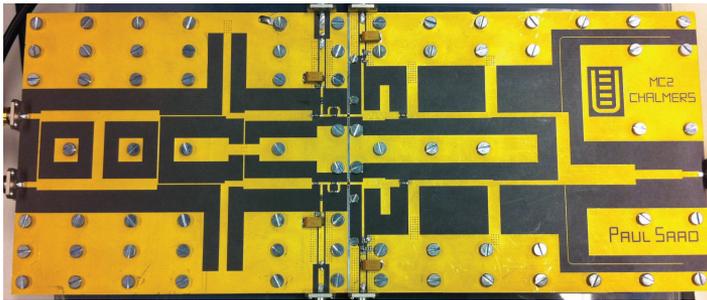


**Fig. 4.12:** Photo of the implemented dual-band Doherty power amplifier.

The simulated and measured drain efficiency and output power versus frequency of the DPA under a constant input power of 33 dBm, corresponding to saturated operation, are shown in Fig. 4.13(a). The measured measured
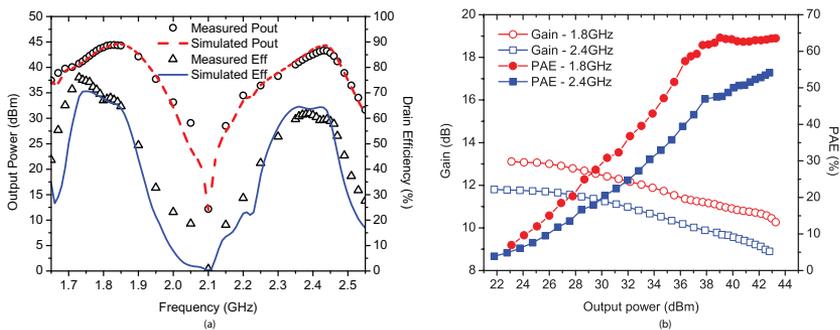


**Fig. 4.13:** Performance of the dual-band DPA (a) Measured and simulated drain efficiency and gain vs. frequency; (b) Measured PAE and gain versus output power.

drain efficiency is 69 % at 1.8 GHz, 61 % at 2.4 GHz while the output power is slightly higher than 43 dBm in the two bands. The measured power gain and PAE versus output power at the two operating bands are shown in Fig. 4.13(b). A correct Doherty behavior can be easily noticed at the two operating bands, where an almost constant high efficiency across OBO range of 6 dB is observed, in particular for the 1.8 GHz band. For the 1.8 GHz band, the measured PAE is 64 % at an output power of 43 dBm, and 60 % at an output power of 37 dBm (6 dB OBO). Similarly, for the 2.4 GHz band, 54 % PAE is measured at 43 dBm output power, and 44 % at 6 dB OBO. The gain compression in the Doherty region is limited to 1 dB for 1.8 GHz and 1.2 dB for 2.4 GHz.

### 4.2.3 Concurrent modulated measurements

Linearized concurrent dual-band modulated measurements were performed on both PAs. The linearization was performed with the 2-D-DPD presented in [89] and the memory polynomial model with nonlinear order 7 and memory depth 3 [57]. The concurrent signal used in the measurements consisted of 10 MHz LTE signal with 7 dB PAPR, and 10 MHz WiMAX signal with 8.5 dB PAPR.

In the experiment, the LTE signal is applied at 1.8 GHz band while the WiMAX signal is applied at the 2.4 GHz band. The measured output spectrum
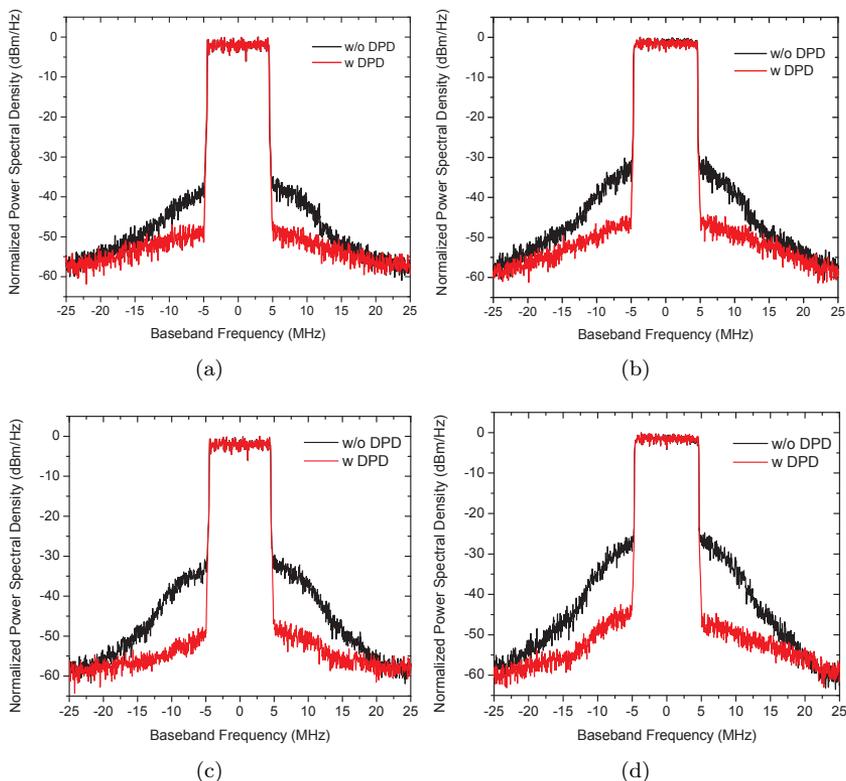


**Fig. 4.14:** Output signal spectrum in concurrent mode, without (w/o) and with (w) DPD, of (a) PA, 10MHz LTE at 1.8GHz, (b) PA, 10MHz WiMAX at 2.4GHz, (c) DPA, 10MHz LTE at 1.8GHz, (d) DPA, 10MHz WiMAX at 2.4GHz.

for both PAs at 1.8 GHz and 2.4 GHz, before and after DPD are shown in
Fig. 4.14. Average output power, PAE, and ACLR, with and without DPD,
are summarized in Table 4.4. These results are obtained for an average input
power of 19 dBm and 22 dBm for the PA and the DPA, respectively.

**Table 4.4:** Measured average output power, average PAE and minimum ACLR.

|       | Pout(dBm) | | PAE(%) | | ACLR(dBc) | |
|-------|-----------|-------|-----------|-------|-------------|-------------|
|       | w/o DPD   | w DPD | w/o DPD   | w DPD | w/o DPD     | w DPD       |
| PA    | 33.0      | 33.0  | 24.5      | 25.0  | $-34.3, -39.0$ | $-47.6, -46.5$ |
| DPA   | 33.4      | 33.2  | 34.4      | 34.1  | $-34.1, -29.0$ | $-48.6, -46.0$ |

### 4.2.4 Dual-band PA versus dual-band DPA

The advantages and the drawbacks of the DPA architecture compared to the
single-ended dual-band PA are discussed in this section. This discussion is
based on both continuous wave and modulated signal measurements performed
on both PAs. The frequency response of the two PAs in terms of output power,
gain, and PAE is compared in Fig. 4.15(a), while the performance of the two
PAs at the two operating frequencies versus output power is compared in
Fig. 4.15(b).

As expected, the output power of the DPA is higher than the one of the
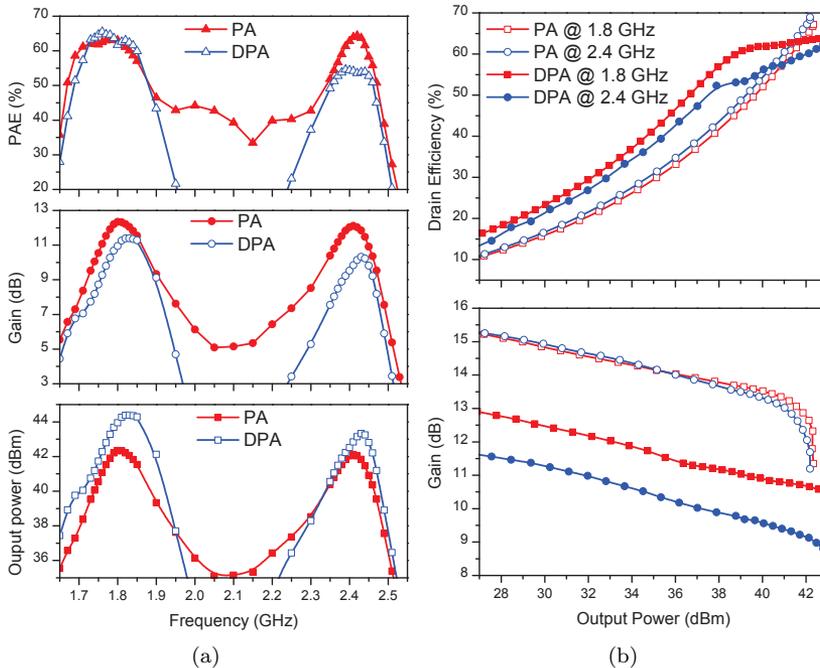


**Fig. 4.15:** Performance comparison of dual-band PA and dual-band DPA (a) Frequency sweep measurement (b) Power sweep measurement.

PA, due to the doubled active periphery. However, the gain of the DPA is lower because of the unequal division of the input power. Moreover, it can be noticed that the PA has similar performance in terms of output power and PAE at both operating bands, while the DPA presents a performance reduction at the higher band. This reduction can be attributed to the input/output combining networks of the DPA. The input/output combining networks of the DPA introduce greater complexity to the circuit and makes it more sensitive to the variations in the practical circuit realization. It is also important to note that despite that performance reduction, the bandwidth is not affected. In fact, similar levels of 1 dB gain ripple bandwidths have been registered at both bands for both PAs.

From the results summarized in Table 4.4, it can be noticed that standard DPD methods can be used to linearize the two PAs, and that the achieved linearity is independent from the architecture of the amplifier since similar ACLR levels have been registered from both PAs. However, the advantage of the DPA with respect to the PA can be noticed in terms of average PAE, where an improvement of 40% is registered for the same operating conditions.

### 4.2.5 Dual-band DPA performance comparison

Comparison between the performance of the presented DPA with recently published dual-band DPAs is summarized in Table 4.5.

**Table 4.5:** State-of-the-art dual-band DPAs. Presented values are for "Break" / "Saturation" conditions. "Break" refers to the turn-on of the Auxiliary device, and "Saturation" refers to the saturation of the DPA.

| | | First Band | | |
| Reference | Freq(GHz) | Pout(dBm) | Gain(dB) | PAE(%) |
| --- | --- | --- | --- | --- |
| 2010 [33] | 2.14 | 33/39 | 6/5 | 33/35 |
| 2011 [89] | 0.88 | 35/41 | 8/6 | 33/40 |
| 2011 [35] | 2.00 | 36/42 | 10/5 | 44/48 |
| 2011 [138] | 1.96 | 36/42 | 8/9 | 33/50 |
| 2012 [139] | 0.92 | 35/41 | 8/9 | 33/41 |
| [Paper G] | 1.80 | 37/43 | 11/10 | 60/64 |
| | | Second Band | | |
| 2010 [33] | 3.50 | — | — | — |
| 2011 [89] | 1.96 | 34/40 | 8/7 | 30/38 |
| 2011 [35] | 2.72 | 36/42 | 10/5 | 40/30 |
| 2011 [138] | 3.50 | 35/41 | 8/9 | 25/33 |
| 2012 [139] | 1.99 | 34/41 | 6/5 | 29/32 |
| [Paper G] | 2.40 | 37/43 | 10/9 | 44/54 |

The presented dual-band DPA shows state-of-the-art results since it outperforms all the other published dual-and DPAs in terms of output power, gain, and PAE. These results demonstrate the usefulness of the proposed approach to implement highly efficient multi-band/multi-mode transmitters for current and future wireless communication systems.

# Chapter 5

# Conclusions and future work

## 5.1  Conclusions

This thesis presents various design techniques that improve bandwidth and efficiency characteristics of PAs used in wireless communication systems.

The design of high peak efficiency single-ended PAs is considered by proposing a new design procedure. The procedure is based on using a bare-die technique that eliminates the parasitics associated with the package of the transistor and an in-house model optimized for high efficiency switched-mode and harmonically tuned PAs. Moreover, MC and EM simulations are performed to ensure first-pass design. This procedure has been demonstrated by designing high efficiency PAs for S-band and C-band. The excellent results obtained demonstrate the success of the selected bare-die mounting, modeling, and circuit design methodologies used.

Then, two design techniques that extend the bandwidth of high efficiency PAs are presented. The first design technique is for single-ended PAs with octave bandwidth, while the second one is for push-pull PAs with bandwidth exceeding one octave. For the single-ended PA, the approach is based on a harmonically tuned approach to ensure high efficiency performance. Moreover, unlike most published work where matching networks are designed using optimization in a non linear circuit simulator, an extensive and systematic design procedure for broadband matching networks is explained and presented. The procedure has been demonstrated by implementing a hybrid high-efficiency octave bandwidth PA covering S-band. To extend the bandwidth to more than one octave, we investigated the potential of push-pull technique and in particular, we studied the influence of the even mode second harmonic impedance of the output balun on the push-pull PA performance. A prototype push-pull PA has been implemented with a balanced output and the output balun operation has been emulated by using a novel push-pull harmonic load-pull measurement setup that allows arbitrary balanced fundamental and second harmonic loads to be presented to the push-pull PA. The study shows that the performance of the PA is very dependent on the second harmonic even mode impedance of

the output balun. The efficiency may be degraded up to 25 % if improper common mode harmonic impedances are presented by the balun. The approach presented allows the PA and balun properties to be isolated from another and is therefore an important tool for further understanding and optimization of PAs and baluns for broadband push-pull microwave PAs.

The dual-band amplification of signals with high PAPR is considered by proposing an extensive design procedure for highly efficient dual-band DPAs. In particular, the procedure concentrates on the design of the passive structures, presenting several possible topologies for the dual-band DPA. The procedure is demonstrated by implementing a state-of-the-art dual-band DPA. The proposed approach allows the design of efficient dual-band DPAs which can be very useful in future wireless transmitters.

A step towards designing multi-band DPAs has been made in this thesis by proposing a new method to design Multi-band BLCs. The complete theoretical analysis of the topology is derived, leading to a closed form equations system for its design. Three couplers are implemented for dual-, triple-, and quad-band operation to validate the methodology. The proposed couplers can be also used in any multi-band microwave and millimeter-wave applications due to their simple structure and the possibility to select arbitrary operating bands.

The proposed design techniques in this thesis provide the designers of PAs with new concepts and thus lead to build new PAs with improved performance in terms efficiency, energy consumption, and bandwidth for current and future wireless systems. Finally, it is important to note that even though the focus has been put on wireless communications, this work is very generic and can be used for many other applications where high efficiency and/or wide bandwidth is demanded.

## 5.2   Future work

The work presented in this thesis is in need of continued research. Here follows a few ideas that can be subject to further research in the future:

**High efficiency power amplifiers**     So far, the proposed approach, the mounting technique and the optimized model of the transistor are tested up to C-band. Therefore, it would be interesting to test the (frequency) limitations of these techniques by designing and implementing hybrid and integrated PAs at higher frequencies, i.e, X-band, for radar and microwave radio link applications.

**Wideband baluns**     The design of broadband baluns is a significant challenge at microwave frequencies. In [Paper D], it is shown that baluns and in particular their common mode response have big importance on the performance of push-pull PAs. Therefore, it would be interesting to investigate and design new broadband baluns with high common mode impedance to be used in broadband push-pull PAs.

**Multi-band branch-line couplers**     The theory presented in [Paper F] is valid for equal amplitude coupler for all bands. Therefore, this work can

be extended to find more generalized coupler design closed-form that allow un-equal amplitude coupling for different bands.

**Multi-band and wideband Doherty power amplifiers** [Paper G] presents a general design approach for dual-band DPAs. This work can be extended to investigate the possibilities to design multi-band DPAs. However, if the number of bands increases, beyond three, the passive networks become very complicated and the design may not be practical. Therefore, designing wideband DPAs is also very important in order to know their limitations and hence, to realize when multiband versus wideband DPAs are giving the best performance.

# Chapter 6

# Summary of appended papers

## Paper A

**A Highly Efficient 3.5 GHz Inverse Class-F GaN-HEMT Power Amplifier**

This paper presents the design of a highly efficient inverse class-F PA using bare-die GaN-HEMT device. A detailed circuit design methodology for inverse class-F PAs is presented and validated.

My contributions are: Design, simulations, implementation, measurement of the PA and writing of the paper.

## Paper B

**Highly efficient GaN-HEMT power amplifiers at 3.5 GHz and 5.5 GHz**

This paper presents the design of two highly efficient harmonically tuned PAs using bare-die GaN-HEMT devices. The first PA is designed at at 3.5 GHz while the second is designed at 5.5 GHz. This work was accomplished together with Hossein Mashad Nemati. The goal of this work was to explore the capabilities of the circuit design methodology presented in [Paper A] for high frequencies and to win the 'High Efficiency Power Amplifier Design Competition' of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).

My contributions are: Device modeling, design of the 5.5 GHz-PA, simulations, implementation, measurement of the 5.5 GHz-PA and writing of the paper.

# Paper C

### Design of a Highly Efficient 2-4 GHz Octave Bandwidth GaN-HEMT Power Amplifier

A design methodology for high-efficiency octave bandwidth PAs is presented. Moreover, a detailed method for the design of suitable broadband matching network solutions is derived analytically. The design approach is demonstrated by the design and implementation of a highly efficient 2-4 GHz octave bandwidth PA using bare-die GaN-HEMT device.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.

# Paper D

### Investigation of push-pull microwave power amplifiers using an advanced measurement setup

In this paper, we propose a push-pull harmonic load-pull measurement setup that allows the influence of the balun on push-pull PA performance to be investigated in detail under realistic operating conditions. A prototype wideband 1-3 GHz push-pull PA has been developed to investigate the influence of the balun characteristics on the overall PA characteristics.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.

# Paper E

### Concurrent Dual-Band GaN-HEMT Power Amplifier at 1.8 GHz and 2.4 GHz

The capabilities of the design methodology presented in Papers A and B are explored for dual-band PAs. This is demonstrated by the design of an efficient dual-band harmonically tuned GaN-HEMT PA at 1.8 GHz and 2.4 GHz.

This research was performed in close collaboration with the group of Prof. Paolo Colantonio at University of Rome Tor Vergata, where I spent six months during 2011.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.

# Paper F

### Design Method For Quasi-Optimal Multi-Band Branch-Line Couplers

In this paper, a closed form design approach for multi-band BLCs for arbitrary operating frequencies is presented. The circuit theory, including design equations and limitations of the approach are presented. The design approach

is validated through the practical implementation of dual-, triple-, and quad-band microstrip BLCs.

This research was performed in close collaboration with the group of Prof. Paolo Colantonio at University of Rome Tor Vergata, where I spent six months during 2011.

My contributions are: Participation in theory and circuit analysis, design, simulations, implementation, and participation in the writing of the paper.

# Paper G

## Design of a Concurrent Dual-Band 1.8 GHz-2.4 GHz GaN-HEMT Doherty Power Amplifier

In this paper, a detailed design procedure for high efficiency dual-band DPA is presented. In particular, the design procedure concentrates on the design of the passive structures, presenting several possible topologies for the dual-band DPA. This is validated by successfully state-of-the-art experimental results of a dual-band DPA operating simultaneously at 1.8 GHz and 2.4 GHz.

This research was performed in close collaboration with the group of Prof. Paolo Colantonio at University of Rome Tor Vergata, where I spent six months during 2011.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.

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