# On the nature of the interfacial layer in ultra-thin TiN/$LaLuO_3$ gate stacks

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We present a detailed investigation on the nature of the interfacial layer (IL) in ultra-thin TiN/$LaLuO_3$ (LLO) gate stacks, which is of importance to facilitate CMOS scaling. The molecular beam deposited $LaLuO_3$ films are found to be amorphous by high-resolution transmission electron microscopy. A ~9 Å thick $LaLuO_3$/interlayer transition observed by medium energy ion scattering correlates with the presence of a dual silicate/$SiO_2$-like interfacial layer derived from the analysis of photoelectron line positions and electron energy loss spectra. A theoretical model is used for the dielectric transition in a bi-layer $LaLuO_3$/IL structure, linking physical and electrical characterization data. The obtained leakage current of $10^{-3}$ A/cm$^2$ at 1.5 V and equivalent oxide thickness of 0.75 nm for TiN/$LaLuO_3$ gate stacks are adequate for scaling in the 14-12 nm node.  [http://dx.doi.org/10.1063/1.4746790]

## I. INTRODUCTION

Strategies for achieving a sub-nanometer equivalent oxide thickness (EOT) for the CMOS gate stack require an ultra-thin or zero $SiO_2$ interfacial layer (IL).[1] Recently, the IL metal-induced scavenging technique has been shown to yield an EOT of 0.42 nm for an $HfO_2$-based MOSFET high-k gate dielectric, in conjunction with IL scaling for the 16 nm technology node.[2] Research so far suggests that from the 14 nm gate length, a perovskite (like $LaLuO_3$ (LLO), $SrZrO_3$, $LaHoO_3$, $LaYO_3$) with a properly designed interlayer is likely to be needed.[3,4] The dielectric $LaLuO_3$ has sufficiently large band offsets with Si (2.1-2.2 eV),[5,6] high permittivity value (~32),[6] and high crystallization temperature (up to 1000 °C).[7–10] Critically, LLO retains a high permittivity (k) in its amorphous phase (unlike $LaAlO_3$),[11] and shows less severe hygroscopic affinity compared to $La_2O_3$.[12] Moreover, LLO shows less Fermi-level pinning,[13] lower leakage than hafnia with the same EOT,[14] and involves less electron charging than $HfO_2$.[15] High-quality amorphous LLO layers with an EOT = 0.86 nm and very low leakage (0.001-0.1 A/cm$^2$) have been reported.[16] The LLO-based stacks have been recently integrated into bulk[10] and silicon-on-insulator, fully depleted MOSFETs[17] using gate-first and replacement gate processes, respectively. Although the interfaces of LLO with metal gates and Si have been reasonably investigated,[5,10,17–19] the state-of-the-art results on the LLO-based MOSFETs[17] point to interface engineering as a key to further scaling. An $SiO_2$-like LLO/Si IL can contribute to a lower density of interface states and consequently higher channel carrier mobility,[2] but lowers the effective k-value of the gate stack. The nature of this interface currently represents the most challenging aspect of the LLO-gate stack physics and is under additional scrutiny in this paper. The physical characterization presented here is used in the construction of a semi-analytical model which correlates the structural results with electrical characterization.

## II. EXPERIMENTAL

The $LaLuO_3$ films of 3, 6, and 40 nm nominal thickness were deposited, on RCA standard cleaned 1-10 Ωcm n- and p-Si(100), by molecular beam deposition (MBD),[14] and combined with titanium nitride (TiN) metal gate (2, 25, and 50 nm, nominal) prepared by reactive sputtering and lift off. A forming gas anneal (FGA) comprising of 10% $H_2$ + 90% $N_2$ was performed only on 3 and 6 nm (nominal) LLO-based stacks at 450 °C for 30 min, for comparison with the same as-deposited stacks. In order to tune the TiN/$LaLuO_3$ barrier height, an AlN layer with thickness of 2–3 monolayers (MLs) was deposited on the LLO surface by atomic layer deposition prior to TiN deposition. Reference samples comprised of an RCA cleaned Si, sputtered Ti, La, and Lu, as well as oxidized Ti, La, and Lu foils.

The x-ray photoelectron spectra (XPS) were recorded using an ESCA300 spectrometer with monochromatised Al

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Kα x-rays of energy 1486.6 eV and electron take-off angles (TOA) of 15-90°. The spectrometer was calibrated so that the $Ag3d_{5/2}$ photoelectron line had a binding energy (BE) of 368.35 eV, and a full width at half maximum (FWHM) of 0.5 eV. The x-ray source power was 2.8 kW and the spectrometer pass energy was 150 eV with the entrance-slit width of the hemispherical analyzer set to 1.9 mm. Under these conditions, the overall spectrometer resolution was ~0.5 eV.[20] Charge compensation was achieved using a VG Scienta FG300 low energy electron flood gun with the gun settings adjusted for optimal spectral resolution. The electron BEs were then corrected by setting the C1s peak in the spectra (due to stray carbon impurities) at 284.6 eV for all samples.[21] Wide scans were recorded in the 0-1250 eV energy range to determine the elements present in the sample and to check for surface contamination. Then the O1s, N1s, Ti2p, Si2p, Si2s, Al2p, La3d, La4d, and Lu4d photoelectron lines were recorded separately. The core-level positions are defined as the FWHM and determined to within 0.05 eV by fitting a Gaussian/Lorentzian curve to the measured peaks. The angle resolved (AR)-XPS measurements were made in a separate ultra high vacuum system consisting of an Al Kα x-ray source and a PSP Vacuum Technology electron energy analyser. This spectrometer was operated with an overall resolution of about 0.8 eV. Medium energy ion scattering (MEIS) was carried out at the STFC Daresbury Laboratory, with a 100 keV $He^+$ beam and a double alignment scattering configuration with a scattering angle of 90° and 135°. Scanning transmission electron spectroscopy (STEM) and electron energy loss spectroscopy (EELS) were carried out in a Titan 80-300 equipped with a Cs-probe corrector and a gun monochromator, operated at an acceleration voltage of 200 kV. Analytical EELS profiles were recorded in angular dark field (ADF) STEM mode with a <0.2 nm diameter probe and beam current of at least 0.5 nA. Capacitance voltage (CV) and current voltage measurements were performed using an impedance analyser HP 4192 A and a semiconductor parameter analyser HP4155B, respectively.

## III. RESULTS AND DISCUSSION

### A. Thickness and elemental depth profiles obtained by MEIS

MEIS measurements were performed to assess the thickness and distribution of elements present in the ultra-thin gate stacks. The key findings are outlined in this section. The MEIS energy spectra for as-deposited 3 nm (nominal) LLO samples are shown in Fig. 1(a). A ratio of 1:1.28 and 1:1.16 for the metallic elements (Lu:La) was extracted from MEIS data before and after TiN capping, respectively. An angle-dependent XPS on these samples shows that the Lu:La ratio is constant with depth within ±2%. Both samples characterized in Fig. 1(a) exhibited a significant amount of surface carbon.[22] It is known that surface and even bulk hydration and carbonation takes place for all binary lanthanide oxides.[23] The incorporation of carbonate species in the film is likely to occur during the low temperature deposition process,[6–8,14,23] and has also been found on the surface of the TiN coatings exposed to air.[24]

An excess of oxygen is observed for both samples, before and after TiN deposition. To account for this effect, the La/Lu signal was used to calculate the amount of O corresponding to $LaLuO_3$; this amount is then subtracted from the fitted O signal to give a value for the excess oxygen, which has been assumed to be in $H_2O$ or −OH form, and from that a H-profile was calculated. The O-rich LLO layers have been reported even after post deposition annealing at 800 °C.[23] Note that even if OH− is present in the bulk, no deleterious effect was found on the electrical properties of the LLO films.[23] This is in contrast to other binary oxides, such as $La_2O_3$, $Dy_2O_3$, which reveal a high degradation due to their hygroscopic characteristics.[23,25]

The elemental depth profiles, including La/Lu, O, Si, and H are shown in the bottom part of Fig. 1(b), and reveal the structure of 2.7 nm LLO/1.4 nm IL/Si. There is no obvious sign of Si mixing with O from the MEIS energy spectra shown in Fig. 1(a), bottom. In the LLO/Si sample, the O-peak is sharp and well-defined, and appears to be of

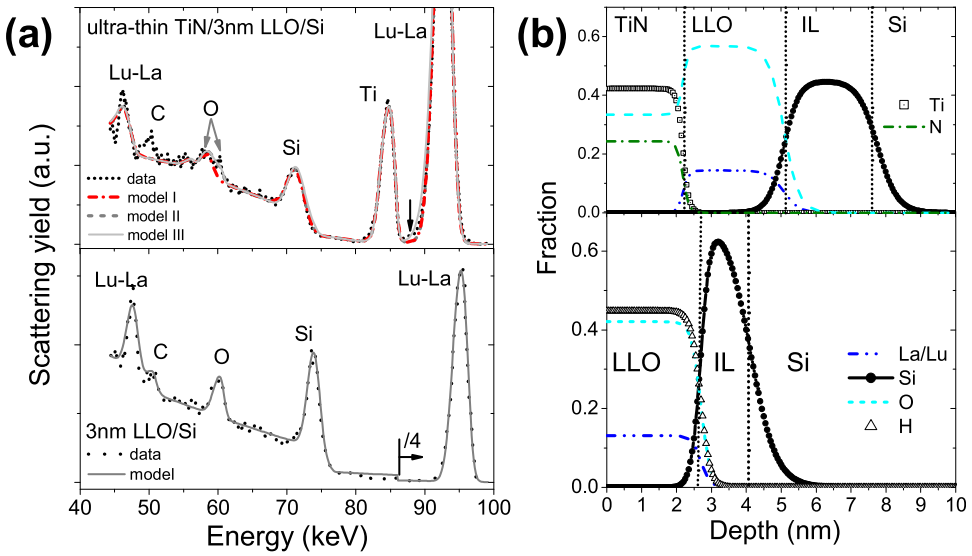


FIG. 1. (a) MEIS energy spectra, model simulations and (b) depth profiles for 3 nm LLO/Si and ultra-thin TiN/3 nm LLO/Si as-deposited gate stacks.

the same width as the La/Lu peak. This may indicate that O is predominantly mixing with La/Lu. The depth profiles in Fig. 1(b), bottom, show some La/Lu concentration into IL within a 9 Å depth from the interface and the Si-rich LLO/Si interfacial layer.

Fig. 1(a), top, shows the case of an ultra-thin TiN/LLO gate stack where an asymmetric O-peak is seen, consisting of two sub-peaks. This observation points to multiple bonding states of oxygen in the film. Several models were used to simulate experimental MEIS data. Model I assumes that oxygen is bonded locally as –O–La–O– ($La^{3+}$ radius 103 pm) within frames of polyhedrons with the smaller ions ($Lu^{3+}$ radius 86 pm) caged inside,[16] that is solely within the $LaLuO_3$ layer. This model can account for only one O sub-peak. Both O sub-peaks can be simulated by using model II, which introduces an O profile into TiN. The existence of the Ti-O bond has been found in the ultra-thin TiN layer[5] underpinning this result. Furthermore, the experimental data at the base of the Lu/La peak (at ~88 keV, Fig. 1(a), top) can be modelled accurately by including 10% of Si into the LLO and 10% La/Lu in Si (model III) pointing to the presence of a silicate type IL. Note that here, the H-depth profile is excluded for simplicity. The depth profiles of Ti, N, O, La/Lu, and Si (Fig. 1(b), top) show a gate stack of 2.2 nm TiN/2.9 nm LLO/2.5 nm IL.

### B. Structural characterization by HRTEM and STEM/EELS

In addition to MEIS, the thickness of the gate stacks was estimated using HRTEM and STEM/EELS techniques. Fig. 2(a) shows the HRTEM image of a 25 nm TiN/40 nm LLO sample. An amorphous structure for the LLO with no apparent formation of nano-crystallites within 5 nm from the Si interface is clearly seen. Figures 2(b) and 2(c) show the ADF STEM and EELS map images of two different cross-sections of the ultra-thin TiN/3 nm, nominal LLO/Si as-deposited sample. The sample was scanned with the STEM probe at a step size of 0.15 nm while recording the EELS spectrum for each point. The green rectangle shown in Figs. 2(b) and 2(c) on the left marks the area of the STEM image being mapped. The EELS color map in Fig. 2(b) shows the extent of oxygen in the structure and enabled measurement of the $LaLuO_3$ (3.5 nm) and IL (2.5 nm) thickness. The fading intensity of oxygen signal close to the interface with Si can be observed from Fig. 2(b). The titanium is mapped in Fig. 2(c) and marks the end of the oxide and the beginning of the TiN layer. The importance of EELS spectrum image shown in Fig. 2(c) is that it enabled thickness of the TiN to be extracted (2.7 nm), as this was not feasible using either TEM/STEM images due to nearly the same contrast of the high-k oxide and TiN. Note that there is a thickness variation by EELS for the metal gate and high-k oxide in comparison to MEIS data; this discrepancy is likely to be mainly due to sample preparation of the cross-sectional view for the microscopy work, which gives a tolerance bar of about ±5 Å.

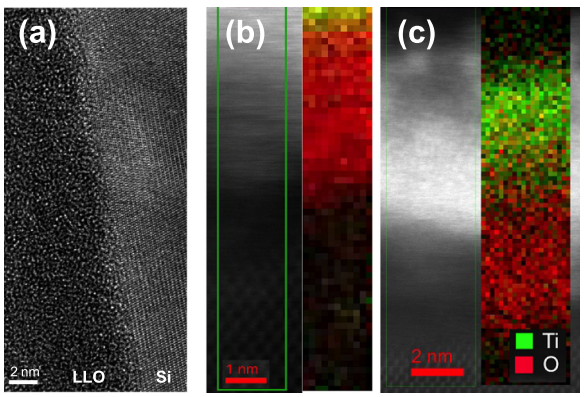


FIG. 2. (a) HRTEM image of 25 nm TiN/40 nm LLO/Si as-deposited gate stack. (b) and (c) ADF STEM images and EELS maps of Ti and O on two different cross-sections of ultra-thin TiN/3 nm LLO/Si as-deposited gate stack.

### C. XPS core level positions and nature of the interfacial layer

This section presents a detailed account of photoelectron line positions and relevant AR-XPS data for Si2s core level to reveal the nature of IL in the observed gate stacks. The XPS core levels of the main peaks (O1s, La3d, La4d, Lu4d, Si2p, Si2s, Table I) mirror closely the MEIS observations. The O1s XPS photoelectron line shown in Table I refers to the O-ions of the La-Lu oxide framework.[16] A second peak, at higher BE, earlier noticed in the data of Ref. 5, has been de-convoluted into two sub-peaks corresponding to $OH^-$ (531.3 eV) and $CO_2^-$ impurities (532.2 eV). This is in line with MEIS depth profiles model simulations of hydrogen and carbon. The following can be deduced from the positions of core-level peaks shown in Table I.

First, there appears to be significant interaction between La/Lu and Si, which may be due to charge transfer from La and Lu to Si, assuming initial state effects contributing to the observed BE shifts.[21] This argument is substantiated by (i) consistent shifts of the La and Lu peaks towards higher BE in comparison to values measured in respective $La_2O_3$ and $Lu_2O_3$,[26–28] and (ii) shifts of Si2s peaks towards lower BE, in comparison to the reference peak in $SiO_2$.[29] The BE of La and Lu peaks reduces by ~1 eV for thicker 40 nm $LaLuO_3$ films when the measureable contribution due to interaction with Si diminishes, which strengthens this argument further.

Second, for samples with TiN deposition, there is an indication of interaction between La/Lu and TiN evidenced by an increase of BE (up to 1 eV) of both O1s and Si2p core levels, suggesting a reduced interaction between La/Lu and Si in these samples. Electron charge transfer from La/Lu to Si (and to TiN for sample with TiN layer on top) seems apparently plausible based on simplistic electronegativity argument, since the electronegativity of La and Lu is about 1.2 while that of Si is 1.9 and Ti is 2.04, although we note that the BE shifts may also include more complicated final state effects.[21] There has been a recent report of no detectable diffusion of La/Lu into the TiN or the Si interface for TiN/1-5 nm LLO gate stacks deposited by pulsed laser deposition.[10] However, in that case a nitrided interlayer had been used to prevent diffusion into the interface.

TABLE I. Photoelectron line positions (in eV) for $LaLuO_3$ and reference samples derived from this work and literature. Columns labelled (1) and (2) for $La3d_{5/2}$ indicate the magnitude of spin-orbit splitting. The binding energy of the most intense peak in the La3d multiplet structure is given. $\delta$ is the energy difference between the two final states of $La3d_{5/2}$ photoelectron lines.

| | | $La3d_{5/2}$ | | | | | | Si2p | | Si2s | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | O1s | (1) | (2) | $\delta$ | $La4d_{3/2}$ | $La4d_{5/2}$ | $Lu4d_{5/2}$ | Oxide | Substrate | Oxide | Substrate | $\Delta$ |
| $La_2O_3$ | 528.6 | 834.5 | 838.2 | 3.7 | 105.3 | 102.2 | … | … | … | … | … | |
| | 529.1[a] | 833.5[a] | 837.9[a] | 4.4 | 104.1[a] | 100.9[c] | | | | | | |
| | | 833.4[c] | | | | | | | | | | |
| $Lu_2O_3$ | 528.8 | … | … | | … | … | 196.1 | … | … | … | … | |
| | 529.0[c] | | | | | | 194.7[c] | | | | | |
| 3 nm LLO, MBD | 529.0 | 835.0 | 838.6 | 3.6 | 105.7 | 102.6 | 196.7 | … | $^{1/2}$99.4, $^{3/2}$98.8 | 152.3 | 150.2 | 2.1 |
| 40 nm LLO, MBD | 528.9 | 834.4 | 838.2 | 3.8 | 105.0 | 101.6 | 196.1 | … | … | … | … | |
| 150 nm LLO, PLD[b] | … | 833.8[b] | | | | | 194.9[b] | … | … | … | … | |
| 3 nm LLO/TiN | 530.0 | 835.1 | 838.8 | 3.7 | 105.8 | 102.8 | 196.7 | … | $^{1/2}$100.1, $^{3/2}$99.6 | 153.4 | 151.0 | 2.4 |
| 40 nm LLO/TiN | 528.9 | 834.5 | 838.3 | 3.8 | 105.0 | 101.8 | 196.3 | … | … | | | |
| 3 nm LLO/TiN, FGA | 528.9 | 835.0 | 838.4 | 3.4 | 105.7 | 102.6 | 196.7 | … | $^{1/2}$99.1, $^{3/2}$98.5 | 152.9 | 149.9 | 3.0 |
| 3 nm LLO/TiN-AlN, FGA | 529.0 | 834.8 | 838.4 | 3.6 | 105.7 | 102.6 | 196.7 | … | $^{1/2}$99.2, $^{3/2}$98.6 | 152.8 | 150.0 | 2.8 |
| 1.3 nm $SiO_2$/Si | 532.3 | … | … | | … | … | … | 102.9 | $^{1/2}$99.4, $^{3/2}$98.8 | 153.9 | 150.2 | 3.7 |
| $SiO_2$/Si | 532.7[d] | … | … | | … | … | … | 103.1[d] | | | | |

[a]Reference 26.
[b]Reference 27.
[c]Reference 28.
[d]Reference 29.

Third, there is a slight shift of the Si2p substrate peak towards lower BE for stacks subjected to FGA, which implies that the top layer of Si has undergone some rearrangement after FGA. The core level positions change negligible for FGA TiN/AlN/LLO/Si gate stack (Table I). The FWHM of O1s, La3d, La4d, and Lu4d peaks is nearly the same before and after FGA, suggesting no significant change in the structure of the LLO layers after the FGA.

The Si2p core levels, which originate from the oxide cannot be measured for LLO samples due to the heavy interference with the La4d levels. Thus, the Si2s core levels were used to elucidate more closely the nature of the LLO/Si interfacial layer. The XPS spectra of Si2s core levels for 3 nm LLO-based gate stacks are shown in Fig. 3(a). The lower binding energy peak at ~150 eV originates from the emission of 2 s electrons in the Si substrate, while the higher BE peak refers to IL. The signature of an $SiO_2$-type[29] IL is the sub-peak shifted from the main Si2s peak by +3.7 eV, designated $\Delta 0$ in Fig. 3(a). It is evident from Fig. 3(a) and Table I that as-deposited stacks, with shifts of +2.1, 2.4 eV, are likely to have silicate-dominant IL, while for FGA stacks with shifts of +2.8-3 eV, a component of sub-oxide with silicate Si-O-La/Lu is expected.[17] The additional AR-XPS Si2s data for the FGA gate stack shown in Fig. 3(b) confirm this assumption as a peak at 153.4 eV is resolved with three subpeaks: two centred at 151.5 and 152.7 eV (silicate), and one at 153.8 eV from an $SiO_2$-like constituent.[17] It is worth mentioning that for thin (3.5 nm) LLO/Si gate stacks in Ref. 17,

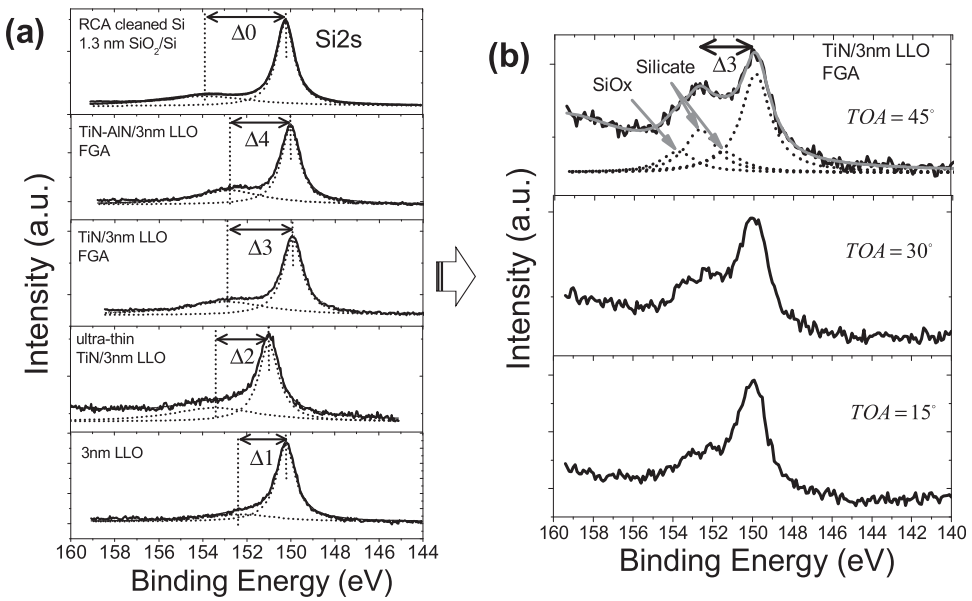


FIG. 3. XPS Si2s core levels for 3 nm $LaLuO_3$ before and after metal gate deposition (TiN or TiN-AlN) and FGA. As a reference, Si2s spectrum for 1.3 nm $SiO_2$/Si is added. (b) Si2s AR-XPS spectra for 50 nm TiN/3 nm LLO gate stack after FGA.

the evidence of a silicate IL with a small contribution of $SiO_2$ came from analysing only Si2s core level spectrum; no full account of photoelectron line positions with reference spectra have been presented or a confirmation on the nature of the interlayer from other complementary techniques discussed. However, the occurrence of silicate IL has been interpreted for thicker 10-20 nm LLO/Si stacks using secondary ion mass spectrometry,[18] as well as depth-resolved cathodoluminescence spectroscopy where the presence of 3.8 eV defect emission has been found as a signature of interfacial interdiffusion.[19]

In summary, the results from MEIS, EELS, and XPS characterization on ultra-thin gate stacks in this work reveal a feature of the $LaLuO_3$ system to form a predominantly silicon-rich interfacial layer with La/Lu depth profiles gradually changing within 9 Å. This will have a favorable effect on electrical properties, in particular for scaling the EOT. The presence of oxygen and some La/Lu at the TiN/LLO interface was observed. This needs to be controlled, as it can alter the workfunction of the gate stack.[30–32]

### D. Electrical characterization data

Electrical characterization of the gate stacks was realized using current voltage and capacitance voltage measurements. Fig. 4(a) shows data from current density measurements as a function of gate voltage for bulk MOS capacitor samples on n-type Si with nominal LLO thickness of 3 and 6 nm. Note that for both thicknesses, the FGA treated samples have larger leakage current than the as-deposited ones. At 1.5 V bias,[33] the leakage of the 3 nm as-deposited sample is in the range of $10^{-3}$ A/cm$^2$, more than one order of magnitude lower than for FGA treated sample with ~0.3 A/cm$^2$. The EOT data are derived from capacitance equivalent thickness (CET) measured using capacitance voltage technique and considering a quantum correction of 0.3 nm. The EOT data from this work on 3 and 6 nm LLO films are added to previously published data on MBD films[14] for completeness (see filled black circles in Figs. 4(b) and 4(c)). It is evident from Figs. 4(b) and 4(c) that as-deposited stacks have smaller EOTs. The effective EOT values for 3 nm nominal thicknesses LLO are ~0.75 nm for as-deposited and 1 nm for FGA treated samples. This result is in agreement with the increased shift in the flatter maximum observed in Si2s core levels in Fig. 3(a), which reflects a mixed interlayer comprising SiOx and correlates with the increase of EOT after FGA. These results point to non-optimal annealing procedure and a need for controlled oxygen environment during FGA to assist a decrease of EOT.

### E. Model of the interfacial layer

We next apply the model presented in Ref. 34 to develop a correspondence between the structural and electrical results. An outline of the model is presented below for completeness. Assume that the "k" varies linearly when the transition from LLO to IL occurs. Using a graded step-like function, $[1+\exp[(x-x_F)/x_0]]^{-1}$, with the half-value at $x_F$ and a tail determined by $x_0$, the permittivity and the conduction band edge for bi-layer dielectric LLO/IL structure can be calculated as[34]

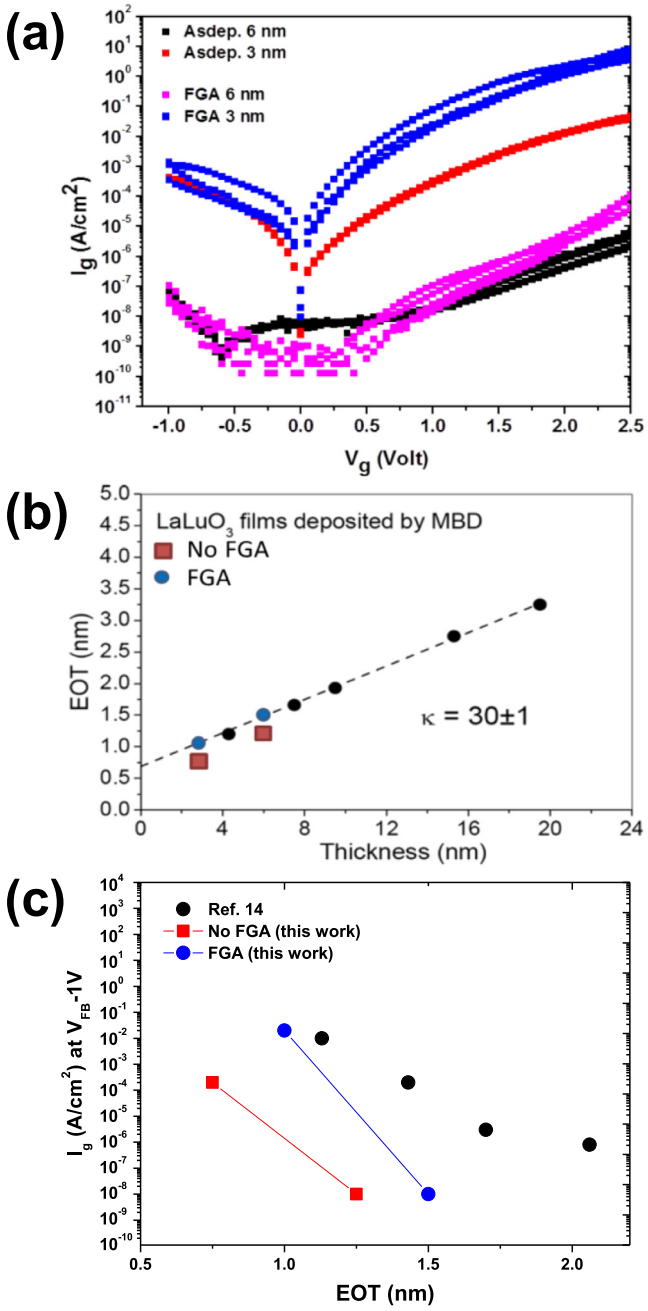


FIG. 4. (a) Current density versus voltage characteristic measured on bulk MOS capacitors with 3 and 6 nm nominal thickness of the $LaLuO_3$. (b) EOT as a function of physical high-k thickness for as-deposited samples (squares) and samples treated by FGA (filled circles). Data extrapolated to zero physical thickness give EOT values of the interlayer, which are larger after FGA. (c) Current density at flatband voltage ($V_{FB}$)–1 V vs. EOT for as-deposited and FGA-treated gate stacks. The black circles in (b) and (c) refer to data published in Ref. 14.

$$k(x) = (k_{LLO} - k_{IL})\left[1 - \left(1 + \exp\left(\frac{x - x_F}{x_0}\right)\right)^{-1}\right] + k_{IL}, \quad (1)$$

$$E_c(y) = \Delta E_{IL} - (\Delta E_{IL} - \Delta E_{LLO})\left[1 - \left(1 + \exp\left(\frac{y - x_F}{x_0}\right)\right)^{-1}\right], \quad (2)$$

where $y = d - x$, with the total oxide thickness d, varying distance from the metal interface, x; $k_{LLO}$, $k_{IL}$ are the permittivities of LLO and IL, respectively; $\Delta E_{IL}$ and $\Delta E_{LLO}$ are the conduction band offsets between the interlayer and Si, and LLO and Si, respectively. The effective permittivity of the total gate stack is given as

$$k_{eff} = d\left[\int_0^d \frac{dx}{k(x)}\right]^{-1}. \quad (3)$$

The variation in k as a function of the distance in Eq. (1) gives rise to an oxide capacitance expressed by

$$C_{ox}(x) = \left[\int_0^x \frac{du}{\varepsilon_0 k(u)}\right]^{-1}, \quad (4)$$

where $x$ and $u$ represent the length scale perpendicular to the surface of the stack. Thus, the shape of the conduction band edge as a function of depth in the oxide can be calculated.

Fig. 5 shows the dielectric transition from LLO to IL, and variation of effective k and capacitance with total oxide thickness according to Eqs. (1), (3), and (4), and assuming a dual silicate/SiOx type interfacial layer with $k \sim 7$. The k-value changes from 7 at the IL/Si to ~32 at the TiN/LLO interface. There have been recent theoretical calculations[35,36] suggesting a gradual change of dielectric transition from the $Si/SiO_2$ interface. The transition has been found to be ~4-6 Å thick and includes the full sub-oxide (SiOx) region. The local permittivity varies across the interface and has been theoretically found enhanced (see Fig. 6 in Ref. 36, where k varies from about 4 to 10 across the sub-oxide region). From the experimental data on high-k/Si gate stacks,[37,38] there is evidence of smaller capacitance equivalent thickness of the IL in comparison to physical thickness of the IL measured by HRTEM. This has been interpreted as an existence of IL with $k \sim 7$, which may be of silicate or SiOx nature. The experimental study in this paper on as-deposited LLO-stacks unambiguously point to predominant silicate formation.

The modeling for the as-deposited 3 nm LLO-based gate stack was performed so that the value of $k_{eff}$ is ~16, which was extracted using

$$CET = \frac{3.9\varepsilon_0}{C_{acc}} = \frac{3.9}{k_{eff}}d, \quad (5)$$

where CET is obtained from the measured accumulation capacitance ($C_{acc} = 3.4\ \mu F/cm^2$, as found from the CV data of the inset in Fig. 5(c)), while d is determined from the physical characterization (4.1 nm). It is evident from Fig. 5 that fitting to $k_{eff} \sim 16$ predicts a relatively abrupt dielectric transition (see dashed line in Fig. 5(a)) with the thickness of transition region of ~8 Å. This is consistent with the La/Lu MEIS depth profile gradients in Fig. 1(b), which show very low mixing of La/Lu with Si and a transition region of about 9 Å. Thus, the model serves to correlate structural parameters, such as thickness of the gate stack and sharpness of the interface, with electrical performance of the gate stack embodied in the values of CET and effective k. It may be particularly useful in evaluating properties of the gate stacks with linear dependence of metallic concentration gradients in interfacial transition regions, both on silicon or germanium.[39]

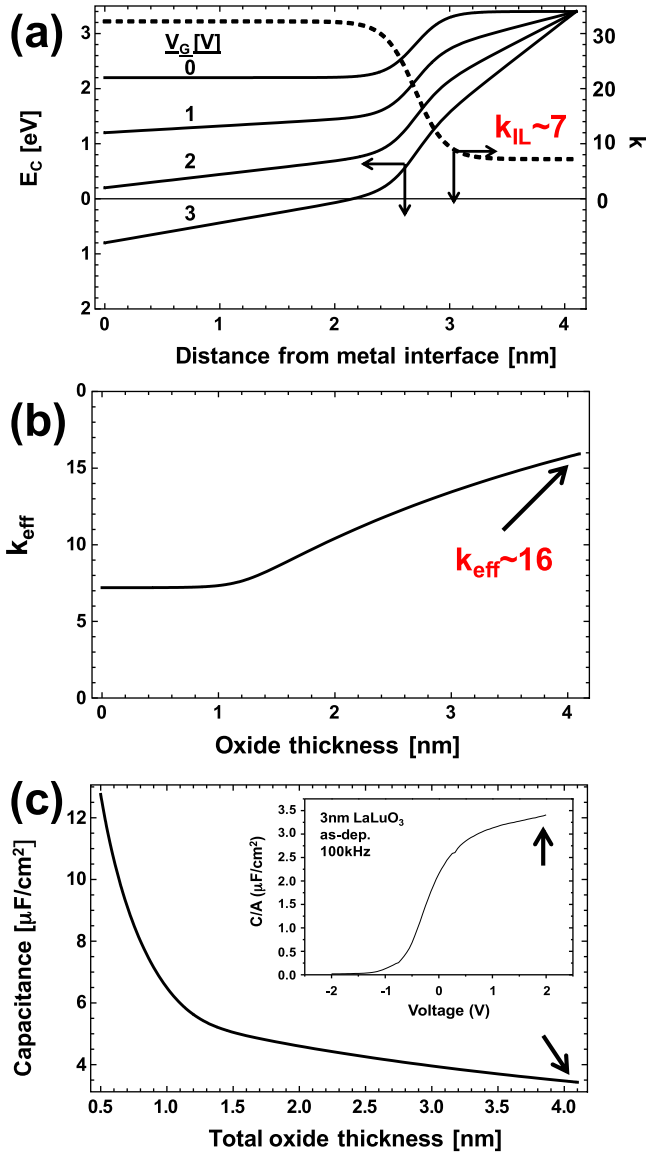


FIG. 5. (a) Theoretical prediction of the dielectric transition between $LaLuO_3$ and Si for 2.7 nm LLO/1.4 nm IL high-k gate stack and a silicate/SiOx-type interfacial layer (dashed curve). The solid curves represent conduction band edge and are calculated for oxide voltage drops of 1, 2, and 3 V. The offset values used are $\Delta E_{IL} = 3.4$ eV and $\Delta E_{LLO} = 2.2$ eV. (b) Effective k and (c) capacitance as a function of total oxide thickness of the gate stack calculated according to Eqs. (3) and (4) and fitted to $k_{eff} = 16$ to derive the interface dielectric transition profile in (a).

## IV. CONCLUSION

Detailed physical characterization of ultra-thin TiN/$LaLuO_3$ gate stacks has been conducted in this paper, and correlated with electrical characteristics using our new model. The $LaLuO_3$ layers were deposited by molecular beam deposition and found to be amorphous by HRTEM, and with no apparent formation of nano-crystallites within 5 nm from the Si interface. The elemental depth profiles of La, Lu, O, and Si have been derived from MEIS energy spectra. There is a clear indication of very low mixing of La/Lu

with Si, and the existence of a transition region of ~9 Å. A full account of the main photoelectron line positions for $LaLuO_3$ is presented. The observed chemical shifts of the main La, Lu, and Si core levels point strongly to the formation of a dual silicate/SiOx type interfacial layer. The angle-resolved photoelectron data confirmed that as-deposited gate stacks have silicate-dominant interfacial layer, while forming gas annealed stacks have a pronounced sub-oxide component. The electrical characterization of the as-deposited gate stacks shows a leakage current of $10^{-3}$ A/cm$^2$ at 1.5 V and an equivalent oxide thickness of 0.75 nm. After forming gas annealing, both the leakage and EOT were found to increase, likely to be due to modified chemistry of the interface and a more pronounced SiOx-component. A model for the dielectric transition in the LLO/IL bi-layer structure is presented, where the permittivity of the interfacial layer and abruptness of the interfacial transition can be fitted for consistency with the experimentally observed value of accumulation capacitance and effective permittivity. We show that, for the experimental data set (physical and electrical) on 2.7 nm $LaLuO_3$ gate stack, the effective k can be fitted to the observed value of ~16, by choosing k = 7, and a transition region of 8 Å. The latter values agree with findings on the silicate nature of the IL (by MEIS, XPS, and EELS) and La/Lu depth profile gradients observed by MEIS. Based on the nature of the interfacial layer and with annealing further optimized, the current study indicates that ultra-thin $LaLuO_3$-based gate stacks can be considered as high-k contenders for the 14-12 nm technology nodes.

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