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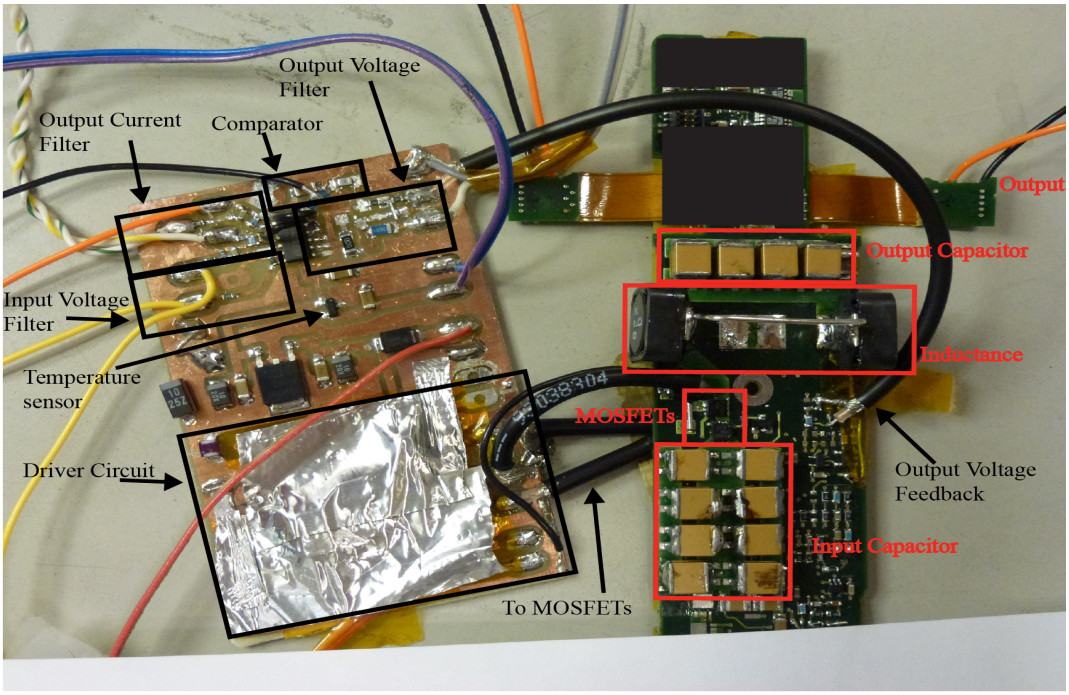

Digitally Controlled Power Supply in Radar Transmitter

Study and construction of a digitally controlled buck converter.

Master's Thesis in the Master Degree Program, Electric Power Engineering

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Gothenburg, Sweden, 2012

Abstract

In this master thesis the possibilities of digital control of DC/DC converters for airborne radar systems with their pulsating load characteristics have been investigated. An already existing buck converter was used and the analog controller was replaced with a digital controller. Different control methods were tested in order to obtain a more uniform input current to the converter. The converter was simulated in Matlab/Simulink with s-function and Simulink blocks in order to determine the control parameters used in the digital controller. Necessary interface circuits were built to handle signal measurements and switching of MOSFETs. The results indicate that digital control of DC/DC converters can increase the level of control and minimize the input current variations. When the active load step control is activated in the digital controller the RMS currents are decreased from 0.141 A to 0.087 A and from 0.248 A to 0.217 A with and without the external output filter respectively. Due to the high switching frequency, 500 kHz, of the buck converter only one converter could be controlled with the digital controller chosen. The interfacing circuitry showed pleasant performance, although future work on filtering noise and increase the speed of these circuits should be performed to further improve the overall performance.

Acknowledgements

The deepest thanks to our supervisor, Valter Nilsson at SAAB Electronic Defence Systems, for the valuable guidance and suggestions he has given us in this project. We would also like to thank SAAB Electronic Defence Systems for giving us the opportunity to carry out this master thesis in their facilities and with their help.

Johan Ringqvist

Jacob Viktorsson

Göteborg, Sweden, 2012

List of Acronyms

AC - Alternating Current

ADC - Analog to Digital Converter

AESA - Active Electronically Scanned Array

DAC - Digital to Analog Converter

DC - Direct Current

DSP - Digital Signal Processor

HB - High side Bootstrap

HI - High Input

HRPWM - High Resolution Pulse Width Modulation

HO - High Output

HS - High Side

I2C - Inter-Integrated Circuit; two-wire interface

IEEE - Institute of Electrical and Electronics Engineers

LI - Low Input

LO - Low Output

MEP - Micro Edge Positioning

MOSFET - Metal Oxide Semiconductor Field Effect Transistor

PWM - Pulse Width Modulation

RMS - Root Mean Square

SPI - Serial Peripheral Interface Bus

UART - Universal Asynchronous Receiver/Transmitter

List of Symbols

C – Capacitor

CMPA – PWM compare register

D – Diode

D_{LOAD} – Duty Cycle of Pulsating Load

f_s – Switching frequency

GND - Ground

i_C – Capacitor current

i_{in} – Input current

i_L – Inductor current

i_{LOAD} – Load current

i_{out} - Output current

K_p – Proportional constant

K_i – Integrating constant

K_d – Derivative constant

L – Inductor

OP – Operational Amplifier

R – Resistance

R_C – Equivalent series resistance of output filter capacitor

R_L – Conduction resistance of output filter inductor

R_{LOAD} – Load resistance

R_{on} – Conduction resistance of MOSFETs

R_{shunt} – Shunt Resistance

s – Laplace operator

T – Transistor

v_C – Capacitor voltage

Vd – Input voltage

V_{dd} – Supply Voltage

V_{DOWN} - Voltage decrement

V_{FB} – Feed back voltage

V_{in} – Input voltage

V_{ref} – Reference Voltage

V_{UPP} – Voltage increment

v_{out} – Output voltage

z – Discrete Laplace operator

1. Introduction

In today's modern society, power electronics can be found everywhere and the quantity is increasing day by day. This is due to their ability to control electrical energy (i.e. voltage, current and frequency) in an everyday increasing span. The power electronics family is classified by their type of input and output power and it consists of rectifiers (AC to DC), inverters (DC to AC) and converters (AC to AC or DC to DC). DC/DC converters, which is discussed in this thesis regulates an unregulated input voltage to a regulated output voltage, typically with different magnitude from the input. Compared to linear power supplies, which uses the transistors as a variable controlled resistance, switch mode DC/DC converters utilizes transistors, as the name implies, as a switch in either on or off state. This gives the switched DC/DC converter their great advantage over the linear ones i.e. they are more efficient since no excess energy has to be dissipated in the transistors to maintain the desired output voltage. The most common and fundamental DC/DC converters are the buck and the boost converters. Buck converters are a step down regulated converter whilst the boost converter is a step up.

1.1. Background

Switched power supplies often uses analog controllers, however they are today in some cases being replaced with digital controllers. With a change from analog to digital more advanced control of voltage, current, frequency as well as protective features are easier to implement. If the control of the power supply need to be modified due to aging of components or stricter requirements on e.g. output voltage ripple this can easily be done in the software rather than changing the hardware itself. There is also the possibility to enable the controller to self adapt to the converter. With a digital processor one also have the ability to control multiple converters with the same controller. The converter hardware is more or less the same regardless if it is controlled by a digital or analog controller. This leads to that one controller often can be replaced with the other. The only thing that is affected by the change of controller is the circuitry that connects the controllers to the converter. By using a digitally controlled power supply, the power supply can be used in various applications with similar demands and the only change that has to be made in order to make it work in these different applications is made in software.

Today's airborne phased array radar systems often have a distributed architecture and consist of a couple of hundred solid state transceivers and their power supplies [**1**]. Demands for improved radar performance require an increasing number of modules in the future. Probably in excess of thousands modules in a fighter radar application. If thousands of transceivers should be used they have to decrease both in size and power consumption. The same applies for their power supplies and one possible way to do this is to change from analog to digital control.

1.2.Purpose

The main aim of this thesis is to investigate and evaluate solutions for control of digital controlled power supplies for Active Electronically Scanned Array (AESA) radars with their pulsating load characteristics. The project should result in a more uniform current consumption of the radar system, an equal or better regulation performance compared to the analog controller and a more flexible power supply. By flexibility means that the system should be easily scalable to meet the future demands, such as increase of transmitters and power consumption.

The pulsating load characteristics of airborne AESA radars creates problem downstream in the power supply system i.e. generators and gearboxes will wear out faster due to rapid changes in torque. With the use of digitally controlled DC/DC converters, an increased level of control can be obtained. Greater controllability gives the possibility to get a more uniform current consumption, which will eliminate the rapid torque changes.

1.3.Scope

The electromagnetic compatibility of the converter will not be investigated in this project. There are however two areas, related to that field that will be handled, noise in measurements and the output voltage quality.

For the efficiency of the converter the existing converter hardware will not be changed except for the way it is controlled. Due to this the switching frequency of 500 kHz will be kept the same as for the analog controller.

The focus on the added circuitry surrounding the converter will be on the function and not the form factor. This is mainly due to that the converter need to be redesigned with both the converter and the controller together with the interfacing circuitry on the same board.

The software written for the processor will focus on implementing the desired functions, and this in C code. Code optimization is only done in case of shortage of processing time and will not include assembler code.

2. Theory

In the first sections of this chapter some basic background knowledge about buck converters, different control techniques and controllers are presented. The digital processor together with its peripherals are present in Chapter 2.2. In the last two chapters, signal filtering and the principles of radars are discussed.

2.1. Buck Converter

The ideal buck converter seen in Figure 1 is a step-down DC/DC converter. Controlling the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which controls the current in the inductor, regulates the output voltage. When the MOSFET is turned on the inductor current is increasing i.e. the inductor is charged from the supply. The current paths can be seen in Figure 2. In Figure 3 the current paths are depicted during the off period while the energy stored in the inductor is discharged through the load. The capacitor is used to reduce the output voltage ripple that occurs during charging and discharging of the inductor.

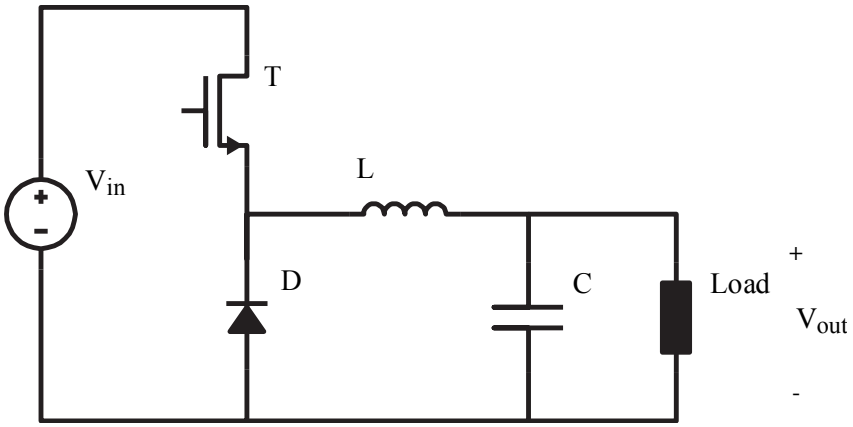

Figure 1 - Ideal buck converter

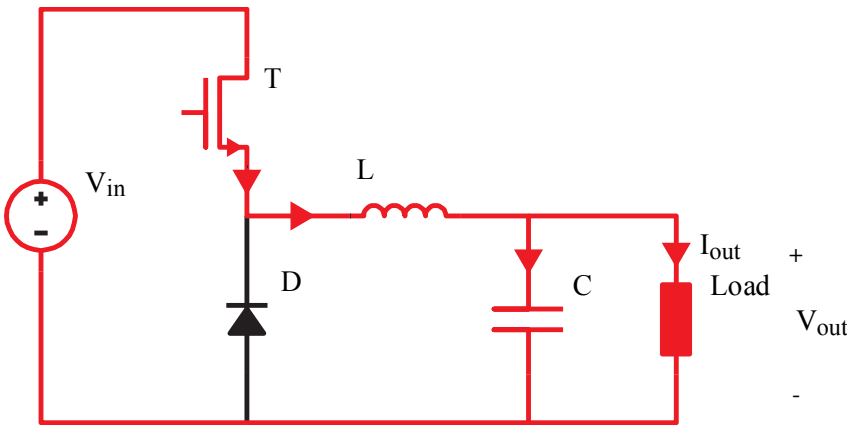

Figure 2 - MOSFET on, inductor current increasing. Red indicates the current path.

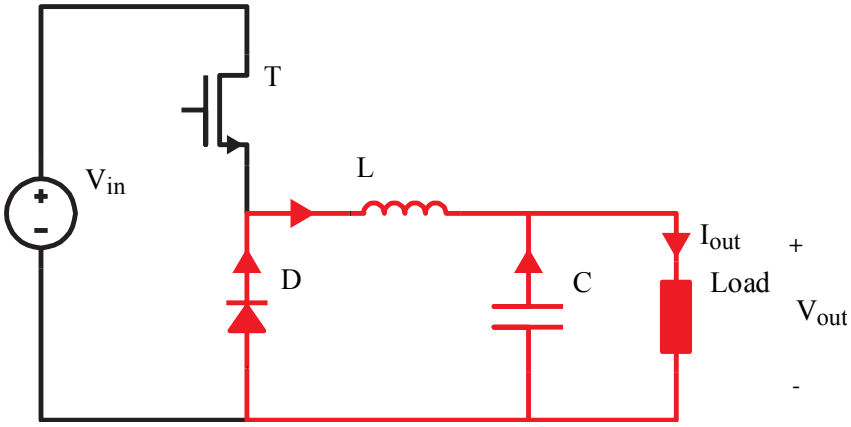

Figure 3 - MOSFET off, Inductor current decreasing.

The buck converter can be operated in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). In CCM the inductor current is continuous i.e. it never goes to zero, whilst in DCM the inductor current goes to zero before the switch is turned on again and the inductor is recharged. During the period when the inductor current is zero the load current is supplied from the capacitor, which can be seen in Figure 4.

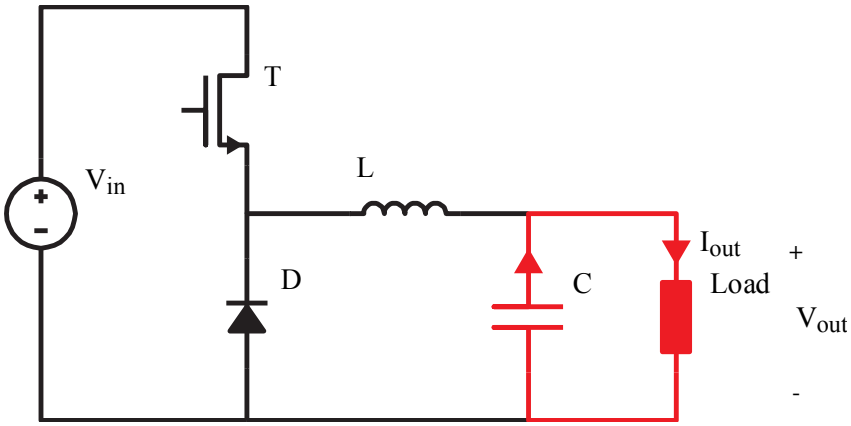

Figure 4 - MOSFET off and inductor current is zero.

Seen in Figure 5 is the buck converter where the parasitic elements of inductor, capacitor and MOSFET have been introduced. Instead of the freewheeling diode, a MOSFET have been added, this is done to lower the losses when the upper MOSFET is turned off.

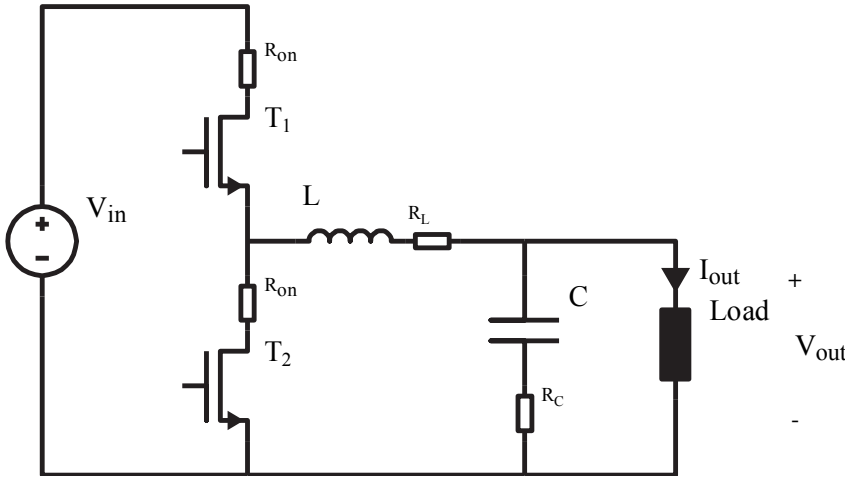

Figure 5 - Buck converter with parasitic elements and low side MOSFET.

2.1.1. State Space Model of the Buck Converter

In order to describe the buck converter mathematically it is necessary to look at the equivalent circuits when the switch is turned on, turned off and when the inductor current has decreased to zero. This is done to design the controller. The current path when the switch is turned on can be seen in Figure 2 in Chapter 2.1. The following equations describe the on state,

$$V_{IN} = L\frac{di_L}{dt} + i_L(R_{on} + R_L) + v_{OUT} \tag{2.1}$$

$$i_{OUT} = v_{OUT} / R_{LOAD} \tag{2.2}$$

$$v_{OUT} = v_C + R_C i_C \tag{2.3}$$

$$i_C = i_L - i_{OUT} \tag{2.4}$$

$$i_C = C\frac{dv_C}{dt} \tag{2.5}$$

Figure 3 depicts the current path when the switch is turned off and the inductor current is different from zero (CCM). This state is described by

$$L\frac{di_L}{dt} = -i_L(R_{on} + R_L) - v_{OUT} \tag{2.6}$$

$$v_{OUT} = v_C + R_C i_C \tag{2.7}$$

$$i_{OUT} = v_{OUT} / R_{LOAD} \tag{2.8}$$

$$i_C = i_L - i_{OUT} \tag{2.9}$$

$$i_C = C\frac{dv_C}{dt} \tag{2.10}$$

When the inductor current has decreased to zero (converter operated in DCM) the current path is shown in Figure 4 and described by

$$i_{OUT} = v_{OUT} / R_{LOAD} \tag{2.11}$$

$$i_C = -i_{OUT} \tag{2.12}$$

$$i_C = C\frac{dv_C}{dt} \tag{2.13}$$

(2.1)-(2.13) have been rearranged into state space form according to

$$\dot{x} = Ax + Bu \tag{2.14}$$

$$y = Cx \tag{2.15}$$

$$x = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{2.16}$$

$$u = V_{IN} \tag{2.17}$$

$$A_{ON} = \begin{bmatrix} -\frac{1}{L}\left(Ron + R_L + \frac{R_C R_{LOAD}}{R_C + R_{LOAD}}\right) & -\frac{1}{L}\left(\frac{R_{LOAD}}{R_{LOAD} + R_C}\right) \\ \frac{1}{C}\left(1 - \frac{R_C}{R_C + R_{LOAD}}\right) & -\frac{1}{C}\left(\frac{1}{R_C + R_{LOAD}}\right) \end{bmatrix} \tag{2.18}$$

$$A_{OFF} = \begin{bmatrix} -\frac{1}{L}\left(Ron + R_L + \frac{R_C R_{LOAD}}{R_C + R_{LOAD}}\right) & -\frac{1}{L}\left(\frac{R_{LOAD}}{R_{LOAD} + R_C}\right) \\ \frac{1}{C}\left(1 - \frac{R_C}{R_C + R_{LOAD}}\right) & -\frac{1}{C}\left(\frac{1}{R_C + R_{LOAD}}\right) \end{bmatrix} \tag{2.19}$$

$$A_{OFF,DCM} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C}\left(R_C + R_{LOAD}\right) \end{bmatrix} \tag{2.20}$$

$$B_{ON} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{2.21}$$

$$B_{OFF} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{2.22}$$

$$B_{OFF,DCM} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{2.23}$$

$$C_{ON} = \begin{bmatrix} \frac{R_C R_{LOAD}}{R_C + R_{LOAD}} & \frac{R_{LOAD}}{R_C + R_{LOAD}} \end{bmatrix} \tag{2.24}$$

$$C_{OFF} = \begin{bmatrix} \frac{R_C R_{LOAD}}{R_C + R_{LOAD}} & \frac{R_{LOAD}}{R_C + R_{LOAD}} \end{bmatrix} \tag{2.25}$$

$$C_{OFF,DCM} = \begin{bmatrix} 0 & \frac{R_{LOAD}}{R_C + R_{LOAD}} \end{bmatrix} \tag{2.26}$$

The three time instants are described by the subscript ON, OFF and OFF,DCM. This method of combining the three different time instants is called state space averaging [**2**].

In CCM state space averaging is performed as

$$A = A_{ON}D + A_{OFF}(1-D) \tag{2.27}$$

$$B = B_{ON}D + B_{OFF}(1-D) \tag{2.28}$$

$$C = C_{ON}D + C_{OFF}(1-D) \tag{2.29}$$

The ON matrix is multiplied with the duty cycle D and the OFF matrix by 1-D, which is equivalent to when the upper switch is closed. State space averaging in DCM is realized in the same manner although one extra matrix and time period is added in order to include the time when the inductor current is zero and the load is supplied from capacitor. This time is denoted (1-D-Δ_1), where Δ_1 is the time when the switch has been turned of and the inductor current is decreasing as described by

$$A = A_{ON}D + A_{OFF}\Delta_1 + A_{OFF,DCM}(1-D-\Delta_1) \tag{2.30}$$

$$B = B_{ON}D + B_{OFF}\Delta_1 + B_{OFF,DCM}(1-D-\Delta_1) \tag{2.31}$$

$$C = C_{ON}D + C_{OFF}\Delta_1 + C_{OFF,DCM}(1-D-\Delta_1) \tag{2.32}$$

2.1.2. State Space to Transfer Function and Small Signal Modeling

The state space equations derived in Chapter 2.1.1 can be transformed into a transfer function according to

$$G(s) = C[sI - A]^{-1}B + D \tag{2.33}$$

Doing so will unfortunately generate a non-linear function, which will counteract the understanding of the converter dynamics. The non-linearity is due to that the duty cycle is used when state space averaging is performed i.e. it is multiplied with the other state variables. However, by applying small signal modeling techniques (linearization) it is possible to overcome the problem with non-linearity [**2**]**.** In the following section small signal modeling will be described in short.

By introducing small ac perturbations

$$x = X + \tilde{x} \tag{2.34}$$

$$v_{OUT} = V_{OUT} + \tilde{v}_{OUT} \tag{2.35}$$

$$d = D + \tilde{d} \tag{2.36}$$

and separate the ac and dc components i.e. there is a steady state operating point and only small variations in voltage, duty cycle and current will occur.

In [**2**], which describes the procedure of transforming state space equation to a linear transfer function,

$$\frac{\tilde{v}_{OUT}(s)}{\tilde{d}(s)} = C[sI - A]^{-1}[(A_{ON} - A_{OFF})X + (B_{ON} - B_{OFF})V_{IN}] + (C_{ON} - C_{OFF})X \tag{2.37}$$

is given.

With the use of (2.37) the transfer function for the buck converter is then given as

$$G_{BUCK}(s) = \frac{b_0 s + b_1}{s^2 + a_1 s + a_2} \tag{2.38}$$

$$b_0 = \frac{1}{L}\frac{R_C R_{LOAD}}{(R_{LOAD} + R_C)}V_{IN} \tag{2.39}$$

$$b_1 = \frac{1}{LC}\frac{R_{LOAD}}{R_{LOAD} + R_C}V_{IN} \tag{2.40}$$

$$a_1 = \frac{R_C R_{LOAD} + R_C R_L + R_L R_{LOAD} + L/C}{L(R_{LOAD} + R_C)} \tag{2.41}$$

$$a_2 = \frac{1}{LC}\frac{R_{LOAD} + R_L}{R_{LOAD} + R_C} \tag{2.42}$$

2.2.Digital Processor and its Peripherals

In this section an overview on the operational principles of digital processors and its peripherals used in this thesis is presented.

2.2.1. Principle of Operation

The digital processor uses a crystal oscillator to generate a clock frequency. This frequency can then be changed by multiplication by a phase locked loop circuit to generate the system clock frequency. The system clock is used for synchronization and timing for all logics in the processor and thereby determine the speed of the processor. The digital processor is feed with digital data as input, which it processes according to instructions programmed into its memory by the user, and provides results as output. Generally today's Digital Signal Processors (DSP) and microprocessors in the mid to high end range uses either 16- or 32-bit architecture.

The main operation of a processor is based on fetch and execute, which mean that the processor first reads the instruction from the program memory. When the instruction is identified the processor executes the task specific for the instruction and then loads the next instruction from the memory. Most of the instructions are of the types of moving data between different registers or performing different logic or mathematical calculations. Beside this set of instructions there are also instructions for conditional statements and other more processor specific. A program is built up of a sequence of instructions stored in the memory. This sequence can be written by hand or be translated from some more high-level program language. The translation is done by a compiler that translates the language of the program into instructions and then into machine code, which is binary values (0, 1). To configure all functions in the processor the settings are written in the processor's registers. Also the data into or out from the processor are written or read from the registers. To process data in the processor the Arithmetic Logic Unit (ALU) is used. The ALU can perform logic operations e.g. AND, OR, NOT, XOR and XNOR together with mathematical addition, subtraction and sometimes multiplication.

Floating point and fixed point are two types of number formats. For numbers that need good resolution and a big range floating point is preferred since they can handle decimals and exponentials. A drawback is that calculations is more complex to perform and often takes longer time to execute. For fixed point a compromise between resolution and range has to be made. Most processors uses integers but decimal numbers can be scaled as multiple of two and stored as integers.

2.2.2. Peripherals

In this section the digital processors peripherals, which are being used in the project, are discussed. The main peripheral modules that are used are the Pulse Width Modulation (PWM) module and the Analog to Digital Converter (ADC) module. In the following section these modules are discussed in more detail. However, these modules all have one thing in common, they use General Purpose Input/Output (GPIO) pins. Typically, every processor that interacts with other devices utilizes GPIO pins as their connection between them. Digital processors are often equipped with numerous GPIO pins and some of these pins have preset functions whilst other can have their function programmed in software.

2.2.2.1. Analog to Digital Converter

The ADC is a device that converts an analog voltage to a digital number i.e. a continuous quantity to a digital discrete representation. The digital number is often linearly proportional to the analog voltage. The resolution of the ADC varies but are usually in between 6 and 24 bits, which gives the possibility of encoding an analog input to 64 and 16777216 levels respectively. Generally the higher the resolution the slower the analog to digital conversion becomes. The voltage resolution of the ADC is given by dividing the range of voltage that can be measured with the bit resolution. By having an input range from 0-40 V and a resolution of 12 bit=4096, the Least Significant Bits will correspond to a change of 10 mV, according to

$$\Delta V = \frac{range}{resolution} = \frac{40-0}{4096} \approx 10mV \tag{2.43}$$

To increase this the range can be changed to 20-40 V instead, which will result in 5 mV resolution but with the drawback that low voltage cannot be measured.

In practice the ADC can only measure a constant value, therefore it uses a sample and hold circuit. The sample and hold circuit uses, in most cases, a capacitor with a switch to disconnect the ADC from the input as seen in Figure 6. First, the capacitor is charged to the same value as the input then the left hand switch is opened and the right hand switch is closed and then the voltage level on the capacitor is converted to a digital representation [**3**]. This value is then stored in a register to be used. It is also important to have a low input impedance, around tens of ohms, to the ADC circuit to get sufficient current to the ADC. To achieve a low input impedance an operational amplifier is preferably used as a voltage follower in series with the input resistance. The speed of the ADC is limited mostly by the internal circuitry that converts the voltage to a digital representation but also by the RC-constant, which constitutes of input impedance plus the internal resistance and the capacitor.

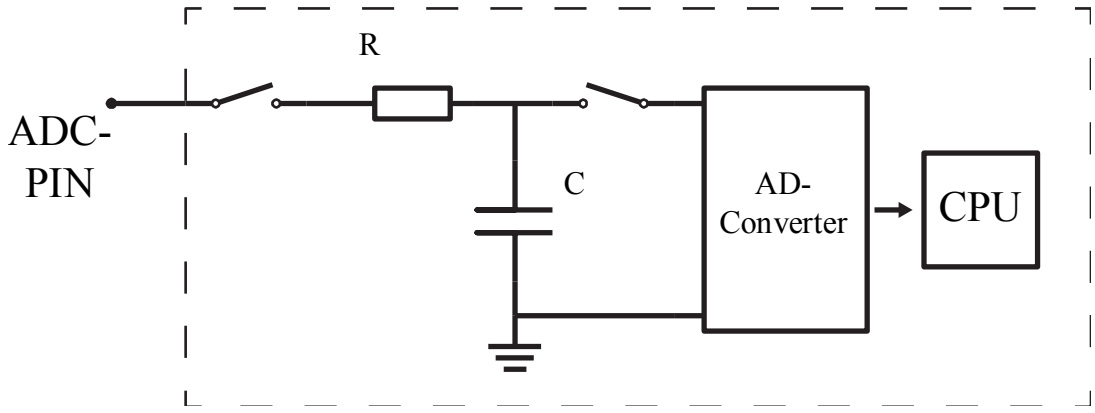

Figure 6 - Internal circuitry of an ADC.

2.2.2.2. Pulse Width Modulation

A PWM module is necessary in order to be able to control DC/DC converters. The PWM module can be seen as a Digital to Analog Converter (DAC) where a digital reference, a Duty cycle, is converted to an analog signal. The digital PWM modules used in digital processors usually utilize a counter, which is connected directly or indirectly to the system clock, that increment periodically. When the counter reaches a set reference value, the PWM output changes from high to low or vice versa, as seen in Figure 7, and at the end of each PWM period the counter is reset. A seen in Figure 7 there is a dead time in between when the high signal goes low and the low signal goes high. This dead time is used to prevent shoot through if the PWM module is used to control a converter with an upper and lower MOSFET. The dead band time can be adjusted or set to zero if it is not needed. The digital PWM resolution is decided by the system clock frequency divided by the PWM frequency desired e.g. a 150 MHz system frequency and a 500 kHz PWM gives a resolution of one third of a percent [**4**]**.**

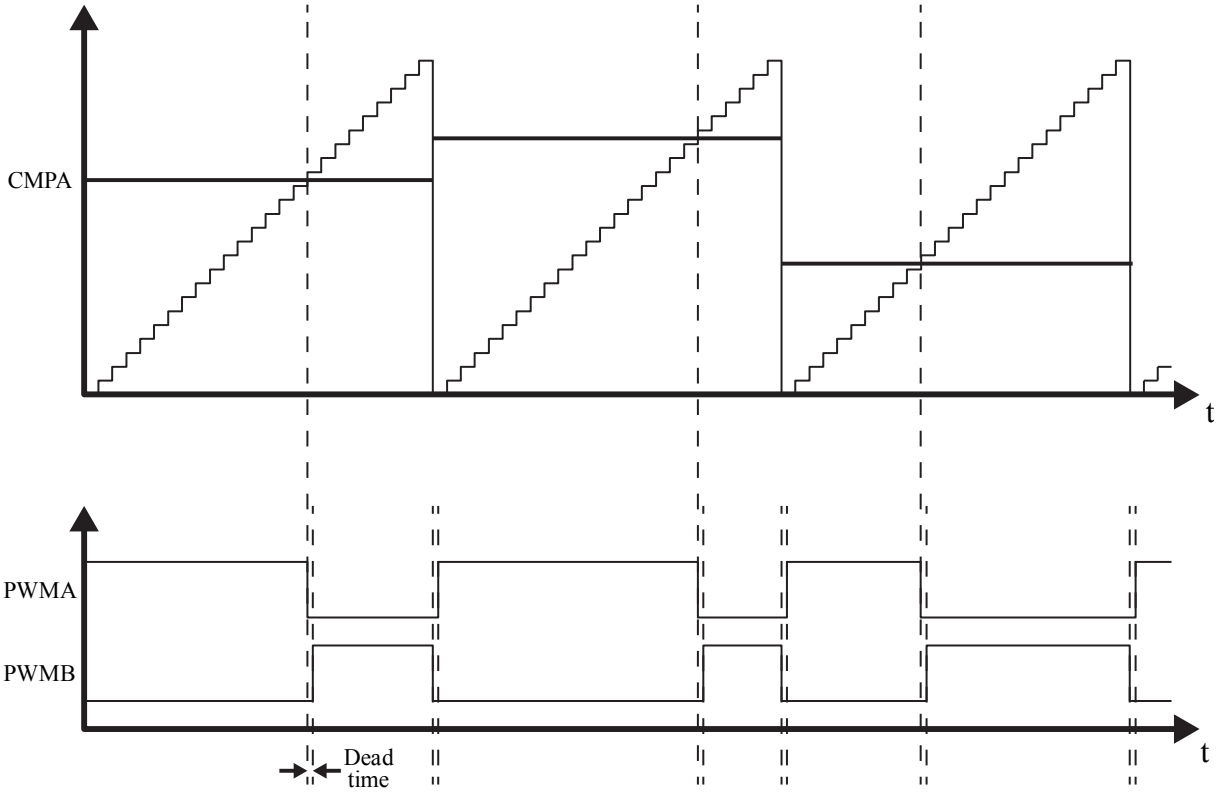

Figure 7 - PWM counter. CMPA is the set reference value. One reference drives two channels. B channel is inverted.

In some processors this resolution can be enhanced with the use of High Resolution Pulse Width Modulation (HRPWM), which utilizes the ability to control the edge of the PWM pulse very accurately [**5**]. The Micro Edge Positioning (MEP) control, which it is also called, is realized with the use of an internal delay circuit that delays the switching from e.g. high to low with the desired time. This gives that the normal PWM step can be divided into smaller steps as seen in Figure 8.

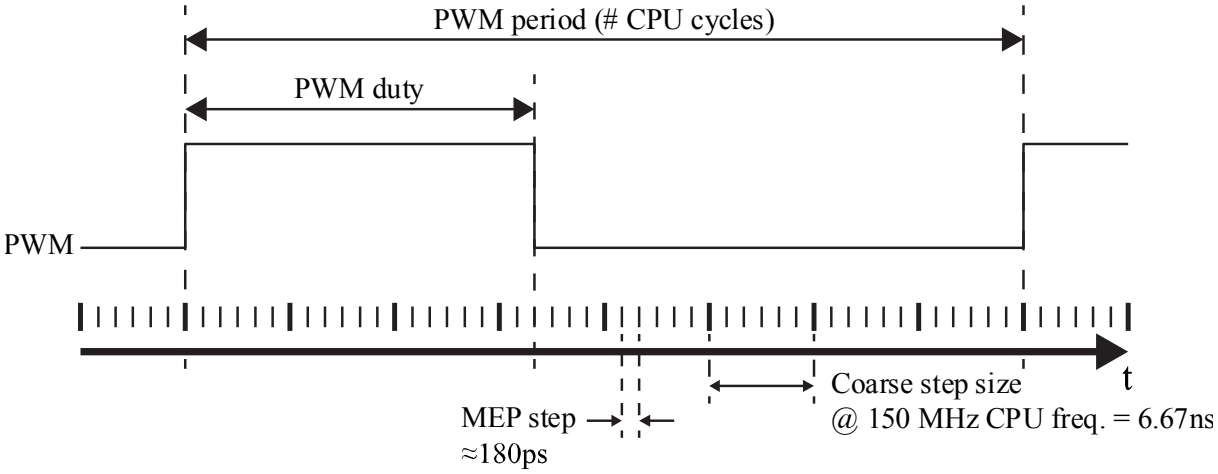

Figure 8 - Example of HRPWM with bold lines representing the normal PWM resolution.

2.2.2.3. Communication

Often a processor does not work by its one and need to control or be controlled from other sources. This is often done through different communication protocols i.e. Universal Asynchronous Receiver/Transmitter (UART), Serial Peripheral Interface Bus (SPI) or Inter-Integrated Circuit (I2C) (two-wire interface). Generally processors have modules that take care of the transmitting of data in the chosen protocol. The module in the processor often have two message boxes, one for transmitting and one for received messages. When a message is written to the transmit box the message is transmitted if the receiving device is ready. If a message is received it is stored in an inbox for later processing. An interrupt can also be generated on received message to start a sequence of operations directly.

The connection between communicating parts is a bit different for the different protocols. There is parallel and serial communication where parallel use many connections and a number is transmitted at once. For serial communication, each bit is transmitted after each other. Sometimes there are more than two devices communicating and then a bus can be used. The bus is a type of network with several units and a common connection. To control the communication, usually one device need to act as a master and it is the only device that can initiate communication. Depending on the connection between all the devices sometimes circuits are needed to power the bus or to shift levels.

2.3. Control Strategies

There are many control strategies and switching schemes that can be used to control DC/DC converters. The controller whose task is to control the output voltage can be of many different types. The most common control strategies and controllers are discussed in brief in the following chapters.

2.3.1. Current and Voltage Mode Control

There are two type of controller modes used in today's DC/DC converters, current mode or voltage mode control. In current mode the controller consists of two loops an inner and an outer loop. The inner loop monitors and controls the inductor current whilst the outer loop, which controls the current reference, monitors the output voltage and increases or decreases the current reference depending on the output voltage error. In current mode control the current is continuously monitored so that the switching is performed at the correct instant [**6**].

In voltage mode control the output voltage is monitored and the duty cycle is regulated to obtain the desired output voltage. Since the voltage is fairly constant during one switching period and since the duty cycle only can be updated at the next period it is sufficient to sample the voltage once during each period and update the duty cycle thereafter.

2.3.2. PID Controller

The controller that is used in the digital processor to control the buck converter is a PID controller and in this section a short explanation on how the controller works is presented. The proportional (P) part of the PID controller multiplies the error with a given constant Kp, the proportional gain. The higher the proportional gain is, the faster the controller responds to output deviations. However if the gain is too high the system becomes unstable. At a small proportional gain the system becomes less responsive to disturbances in the output and the error at steady state becomes larger.

A Proportional-Integrator (PI) controller, also known as a phase-lag controller, is used to increase the loop gain at low frequencies resulting in a reduction of the steady-state error. The introduction of an I term will also decrease the stability of the system. The integrating term of the PI controller is proportional to both the magnitude of the error and the time the error exists.

By introducing a derivative term a PID controller is obtained. The derivative term is introduced to increase the stability of the system, however if the error signal is noisy the derivative term will cause problems since the derivative of noise generally is very high. The transfer function of the PID controller is described as

$$G_{PID}(s) = K_p + \frac{K_i}{s} + K_d s \tag{2.44}$$

2.3.3. Synchronous and Asynchronous Switching

Since AESA radars consists of multiple radar modules and each or a couple of them have their own separate DC/DC converter. Synchronous switching of these converters can be used to gain more control of when the power is drawn from the power source. To be able to use synchronous switching an external clock or oscillator has to be used in order to synchronize the switching frequency of all converters. If all the converter switches are turned on at the same instant all the energy will transferred from the supply to the inductor and then further on to the load during the on period. During the off period no current will be taken from the load which will make the array of DC/DC converters act as a pulsating load, albeit with high frequency. Instead of turning on all switches there is a possibility to phase shift the turn on of half of the array of converters with 180 degrees or divide the array into more groups and phase shift them evenly. This will make the current taken from the power supply unit more uniform since energy transfer through the converter to the radar is conducted in more than one instant.

With asynchronous switching each converter clock frequency is set separately. Since some of the internal oscillators run slower or faster than others, the frequency will not be exactly the same for all converters. This will result in that their turn on instant will not occur at the same time. The drawback of this is that it becomes harder to manage the power drawn from the supply. However if enough converters are used it is expected that equally many are faster and slower in switching frequency, which will even out the power drawn from the supply. This is also the easiest method to implement since it doesn't require any connection between the converters. It is also more robust since all converters run separated compared to synchronous switching where a failure in the synchronizing clock will affect the control of the converters.

2.4. Filters

Only low pass filters are used in this project. Low pass filters are used to filter out high frequency disturbances. The first order active low pass filter consists of a series resistor and a capacitor connected to ground and an operational amplifier, as seen in Figure 9. The first order filter has a cut-off frequency described by

$$f_{c,1} = \frac{1}{2\pi RC} \tag{2.45}$$

$$H_1(s) = \frac{1}{1 + sRC} \tag{2.46}$$

The cut-off frequency is the frequency where the gain of the filter has decreased with 3 dB. At frequencies above the cut-off frequency the gain will decrease with 20 dB per decade.

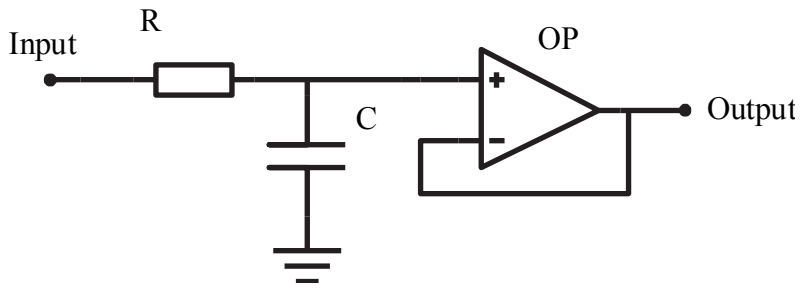

Figure 9 - First order active filter.

A common second order active low pass filter, which is seen in Figure 10, is of the type Sallen-Key. A main feature of the Sallen-Key filter is the low part count. The cut-off frequency and transfer function of the Sallen-Key filter is calculated according to

$$f_{c,2} = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{2.47}$$

$$H_2(s) = \frac{2\pi f_0}{s^2 + 2\pi\frac{f_0}{Q} + (2\pi f_0)^2} \tag{2.48}$$

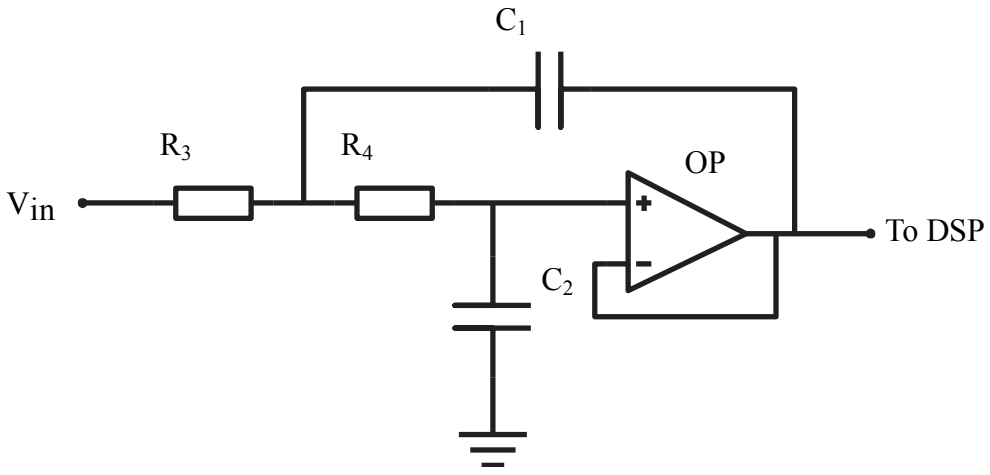

Figure 10 - Second order active filter low pass filter.

Another low pass filter is the RLC filter, depicted in Figure 11, which in this project is utilized to obtain a DC voltage and DC current at the output of DC/DC converters. In DC/DC converters and similar filter applications the resistance is equivalent to the load. The RLC filters is configured to withstand high currents and voltages, which means that the components used in these types of filter can not be of the same type as the ones used in the active filters described above.

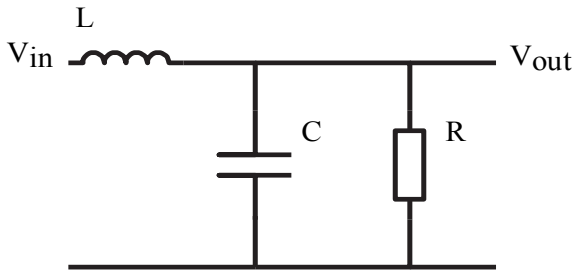

Figure 11 - RLC filter.

The transfer function of a low pass RLC filter is defined as

$$H_3 = \frac{\frac{1}{LC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \tag{2.49}$$

As seen, the filter is of the second order and will therefore reduce its gain with 40 dB per decade after the 3dB gain drop.

The cut off frequency is calculated according to

$$f_{c,3} = \frac{1}{2\pi\sqrt{LC}} \tag{2.50}$$

Another thing to note is that since it is a RLC circuit it will have a resonant frequency, which is calculated as [**7**]

$$f_{0,3} = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{(RC)^2}} \tag{2.51}$$

2.5. The Fundamentals of Radar and its Load Characteristics

The AESA radar is an electronically scanned radar and have therefore in most cases a non moving antenna [**1**]. This makes the searching direction easy and fast changeable with the possibility to jump between different targets instead of sweeping. To form the radar beam, multiple transmitters are used and they are individual delayed in time/phase. In Figure 12 an example of six modules transmitting with a set delay between them is seen. This results in superposition where waves adding and subtracting each other from the different transmitters forming a wave front.

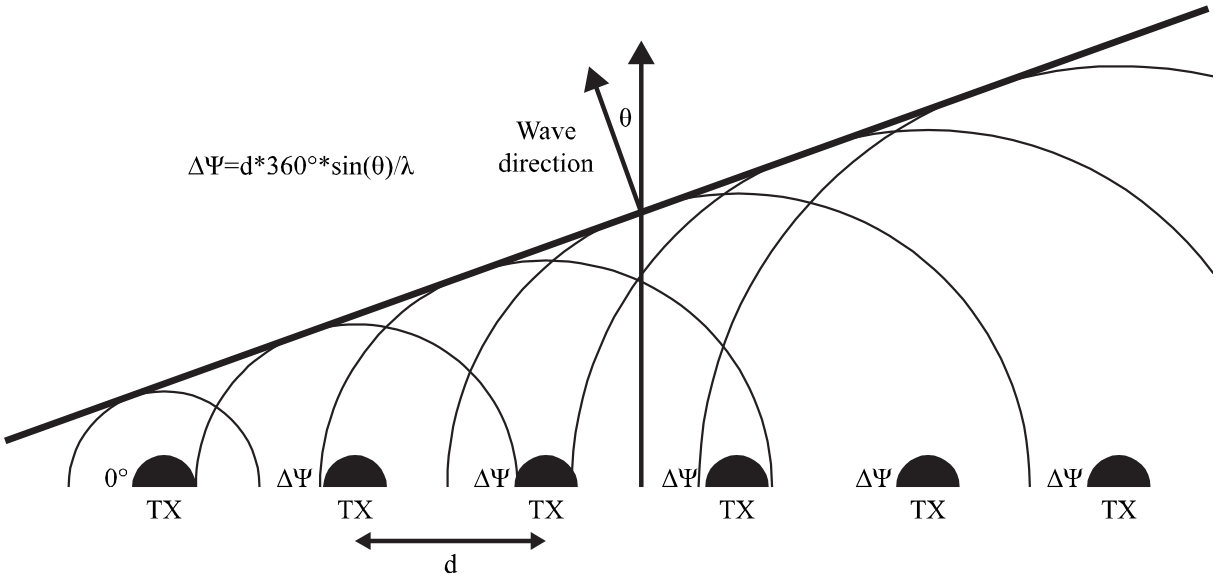

Figure 12 - AESA radar beam. The wave direction θ, with fixed distance d and fixed wavelength λ, is decided by the delay $\Delta\Psi$ between the different transmitters (TX).

The system is often module based and each module consists of transmitter, receiver, power supply and antenna. The antenna is in most cases used both for transmitting and receiving although not at the same time. All modules are connected to a central controller that activate the transmitters and sets their delay to achieve the direction. The central controller also receives the data from each receiver and analyze the content to get the data of interest i.e. range, speed and direction of target.

Since all modules transmitting at the same instant and for short periods of time, the power consumption to the radar varies much with time, as seen in Figure 13. The power supply that supplies the radar needs to handle these variations or some kind of filtering is needed to average the consumption. In these systems the power distribution system are often complex and supplying many hundreds or thousands modules. Often bulk capacitors are used to get an uniform consumption but they often occupy large volumes, which is problem since the bulk capacitors need to be close to the modules placed in the antenna array. Especially in airborne systems this is problematic due to strict safety constraints, limited weight and volume. The consumption from the receiver and all other electronics is small compared to the transmitters with its power amplifiers.

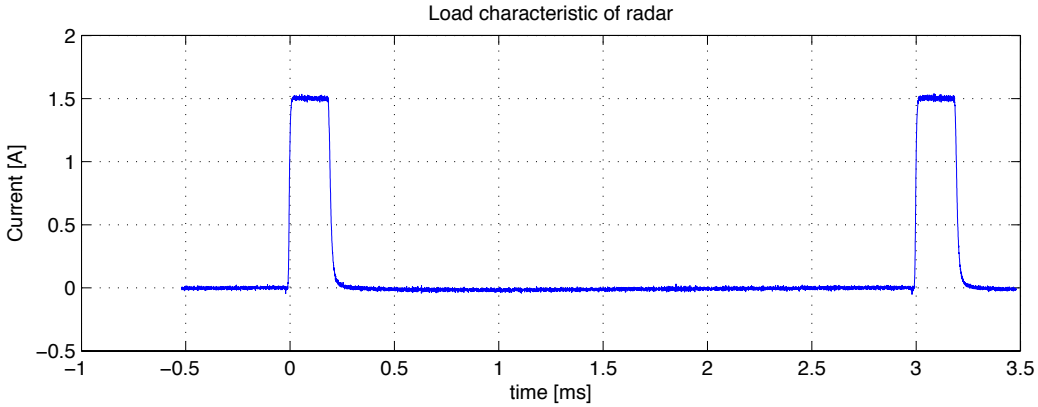

Figure 13 - Load characteristic of AESA radar.

In Figure 14 is an equivalent circuit of how the AESA radar has been modeled in this thesis. The inductor and capacitor make up an external filter on the input. The external filter is used to smoothen the current and voltage respectively so that the converter, which is connected in front of the external filter, will not experience the full load step. The load current is modeled by a dynamic load, which draws either full load current or no current as seen in Figure 13.

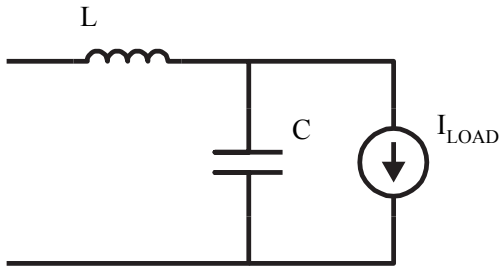

Figure 14 - Model of radar and external filter.

During sending i.e. a load step, the energy that has to be transferred from the supply to the radar is increased substantially and since DC/DC converters are not infinitely fast at reacting to these kinds of load changes the voltage will drop. If the voltage drop is not too large the radar, which is sending with constant current, can still operate normally. By knowing that the voltage drops at each transmission this can be accounted for in signal analyzing software, but only if the voltage profile is the same for each transmission so that the modulation of the sending signal also is the same each transmission.

3. Case set-up

In order to control the buck converter digitally a couple of different tasks had to be completed, how these tasks was completed are described in this chapter. The chapter starts with how the modeling and simulations was performed in Matlab/Simulink and continuous with the choice of digital processor. An interface board connecting the digital processor and the buck converter, for both outgoing and incoming signals, had to be constructed and this is described in Chapter 3.3. In Chapter 3.4 and 3.5 the program structure, how the converter is controlled and how its protective features were implemented are presented. Finally, the test setup and the evaluation strategy are described.

3.1.Modeling and Simulation

To be able to choose a suitable discrete controller, the converter has been simulated in discrete time in Matlab with Simulink. The state space model, equation (2.14)-(2.17), of the converter was put into a block in Simulink called s-function. An overview of the block diagrams used when simulating the converter can be seen in Figure 15. On the left hand side of the s-function the inputs i.e. voltage, duty cycle and load are feed into the converter, whilst on the right hand side, output voltage, inductor current and capacitor voltage are the outputs.

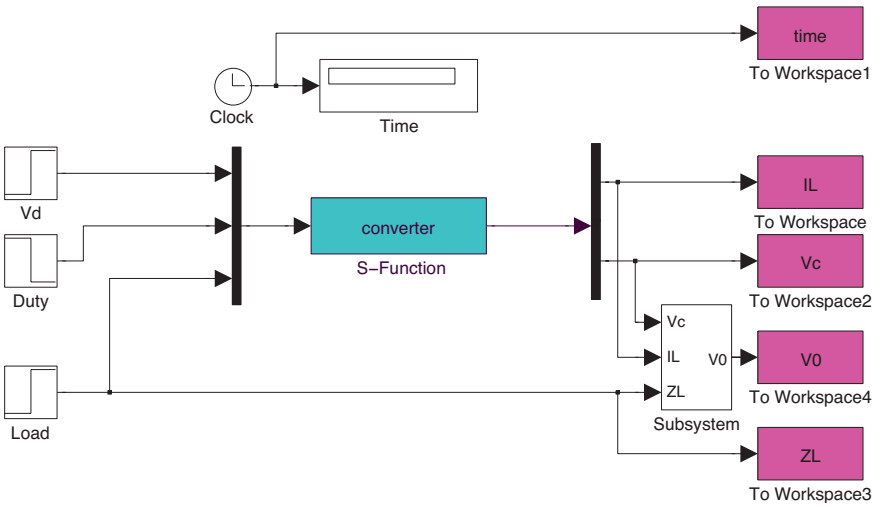

Figure 15 - S-function in Simulink with inputs and outputs

From the state space model it is possible to derive a transfer function as described in Chapter 2.1.2. However this transfer function is nonlinear and to be able to use it when designing the controller it had to be linearized. This was done with the use of Matlab according to Chapter 2.1.2. The linear transfer function can be seen in equation (2.38)-(2.42).

With the use of the Matlab toolbox called sisotool (Signal input/Signal Output) a controller with the desired phase margin and bandwidth can easily be derived. One thing that should be considered when designing controller is the time delay from sampling until the calculations have been made and the new duty cycle has been updated. This is in the best of cases one clock cycle. By having a phase margin of the closed loop system of 60 degrees the delay is accounted for. The bandwidth of the controller was set to 10kHz, which is 50 times below the

switching frequency, in order to be sure the system is not to fast and becomes unstable. The controller in continuous time is described by

$$C(s) = \frac{7.863s^2 + 2.603e5s + 4.325e9}{s^2 + 6.792e6s + 9.741e8} \tag{3.1}$$

The continuous controller was then discretized in Matlab with the bilinear transform. The discrete transfer function and the difference equation are described by

$$C(z) = \frac{1.043z^2 - 2.017z + 0.9762}{z^2 - 0.2564z - 0.7431} \tag{3.2}$$

$$D(n) = 0.2564D(n-1) + 0.7431D(n-2) + 1.043E(n) - 2.017E(n-1) + 0.9762E(n-2) \tag{3.3}$$

(3.3) was verified in Simulink and later on used in the DSP as the controller.

3.2.Choice of Digital Processor

On the market today there are a wide range of processors and manufacturers. There are some families of processors designed for different tasks, one example is the DSP, which goal usually is to measure analog signals and then process the data in an appropriate way. Every processor family has different specifications and is designed to suit different applications. The process of choosing a processor is a demanding task. One way of doing this is by setting up some requirements. Important parameters for a digital processor used in this thesis are listed below.

- Fast PWM (500kHz) with high accuracy and at least 2 for one converter, increasing with 2 per converter.
- High CPU clock to perform the necessary computations.
- Fast ADC convergence 2-4 per converter.
- Some type of communication to external equipment.
- Commonly used and available.

To be able to control one MOSFET one PWM output is required. For this thesis at least four outputs are needed since two converters are intended to be controlled. By replacing the analog controller with the digital controller the switching frequency need to be the same. Otherwise the inductor and filters on the converter needs to be changed. With high speed often resolution is sacrificed so it is a trade off between speed and resolution.

The high switching frequency, 500kHz, of the converter implies that the processor speed needs to be sufficiently fast in order for the code to be executed in the short period of time between each PWM update. Besides the regulating code, some other code for communication and monitoring need time to run. For a processor with clock speed of 150 MHz and a PWM frequency of 500 kHz, 300 operations (one cycle operations) can be executed each switching period according to

$$operations = \frac{clockspeed}{PWMfrequency} = \frac{150MHz}{500kHz} = 300 \quad (3.4)$$

The control code consists mainly of addition and multiplication operations forming a filter. Addition is a fast operation for processors to perform but multiplication is a more complex operation and the time it takes differs from processor to processor. Some processors have built in modules to speed up these complex operations. Processors are built to handle either or both fixed and floating point arithmetic's and for this thesis a processor that can handle floating point is desired since most of the calculations are of non-integer type.

The analog to digital converter is needed to get analog inputs to the processor. All ADC converters take some time to sample the measured quantities and this is desired to be as short as possible, but still with enough resolution. For this thesis many different signals need to be sampled and depending on the processor this can be performed in different ways. The best would be to sample all signal simultaneously but often this is impossible due to restrictions in the ADC modules. So instead, one or a pair of signals can be sampled and then the other in series afterwards. The accuracy of the ADC can be calculated according to equation (2.43) in Chapter 2.2.2.1.

For communication with the processor some type of protocol is needed. This communication can be handled in software or in hardware but since the processor cannot be interrupted by the communication a hardware module is needed. In Chapter 2.2.2.3 the different types of communication protocols are described more thorough.

The processor that was chosen was the Delfino F28335 floating point DSP from Texas Instruments. With its 32 bit CPU running at 150 MHz, 16 ADC channels 12 bit each and 6 PWM outputs it fulfilled all the requirements [**8**].

3.3.Interface Board

In order to connect the DSP to the DC/DC converter an interface board with driver circuit, comparator, voltage- current- and temperature measurements had to be constructed, the next sections will describe how this was performed.

3.3.1. Driver Circuit

The DSP can only sink or source a current of 8 mA so in order to be able to operate the MOSFETs quickly a driver circuit that can source enough current at the turn on and sink the gate fast enough at turn off had to be constructed. Even though the charge needed to charge/discharge the MOSFET is small the current is significant due to the short time required to switch efficient. Fast switching transistors are required for high efficiency but this will create noise that may interfere with sensitive circuit in the system. For example the feed back in the DC/DC converter or the receiver in the radar can be affected.

The gate driver IC, LM5109 from Texas Instrument, which was chosen is a driver circuit with a totem pole configuration. In order for this driver to function properly with the high and low side MOSFET configuration, a diode and bootstrap capacitor needed to be added externally as seen in Figure 16. The bootstrap capacitor is used to increase the gate voltage above the

converters supply voltage so that the upper MOSFET can be turned on when the lower one is turned off. To get this to work the capacitance needs to be large enough so that the MOSFET gate is supplied during the entire on period and was therefore chosen to be 100 nF. One thing to be aware of is that during the off period the capacitor needs to be recharged again. This results in that this configuration can not be used when the duty cycle is close to one, since the time to recharge the capacitor is insufficient. The diode needs to have a minimum blocking voltage of 48 V, which is equal to the supply voltage minus the interface boards supply voltage. The gate driver IC has the possibility to sink or source a current of 1 A [**9**]**.** Two resistors; 10 ohms each were inserted (according to Figure 16) in order to limit the gate charge currents below the specified value.

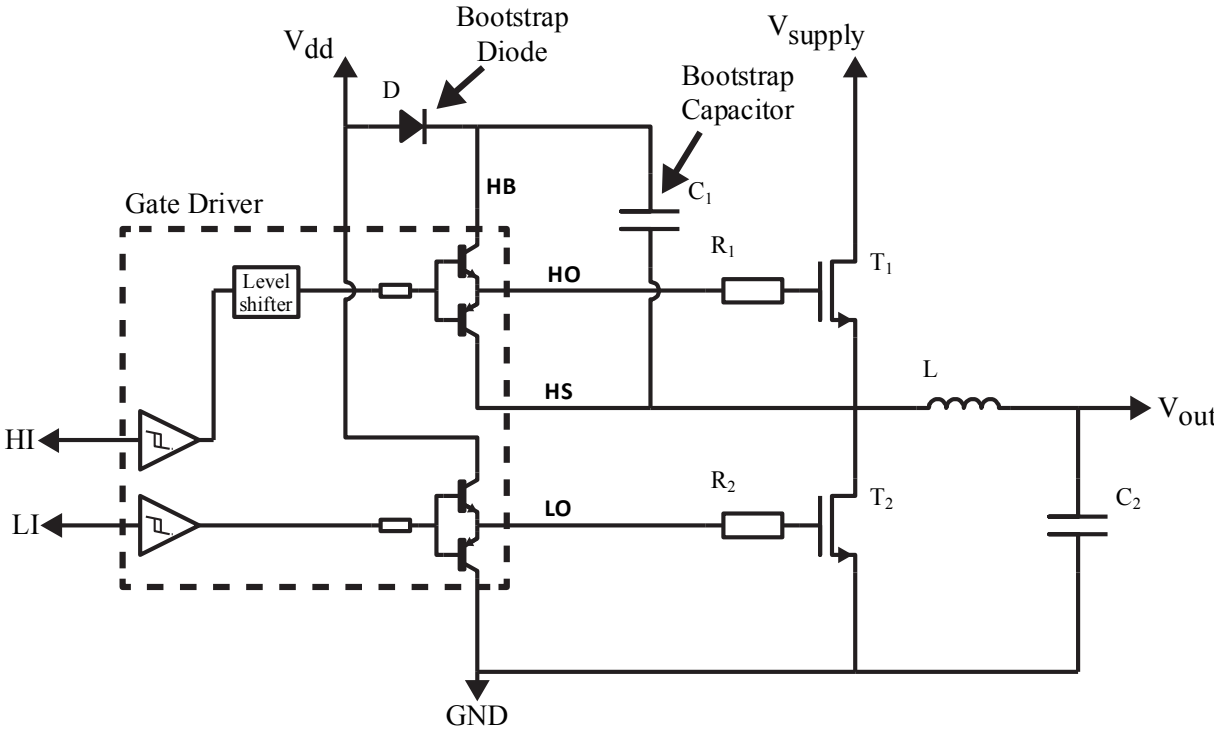

Figure 16 - Circuit diagram of the driver circuit and its connection with the converter.

3.3.2. Current Measurement

The most convenient way to measure the current out from the buck converter was to use a resistive current shunt. Therefore a precision resistor of 0.11 ohm was put in series with the converter and the voltage was measured across it. The low value is required to preserve low power loss and a minimum voltage drop. To minimize the affect the current measurement has on the existing circuit and to filter the noise in the current an operational amplifier with filter was put in between the resistor and the DSP. The bandwidth of the filter was set to 60 kHz. Since the shunt resistance is fairly small in order to minimize its losses and the voltage drop across it the gain of the operational amplifier had to be adjusted so that the voltage into the DSP would be in the 0-3 V range. At full load the drop across the resistance was 164 mV by setting the gain to around 16 times the voltage into the DSP at full load became 2.6 V. This gave enough headroom to measure currents higher than the maximum load but still enough accuracy. The final design of the current measurement circuit can be seen in Figure 17.

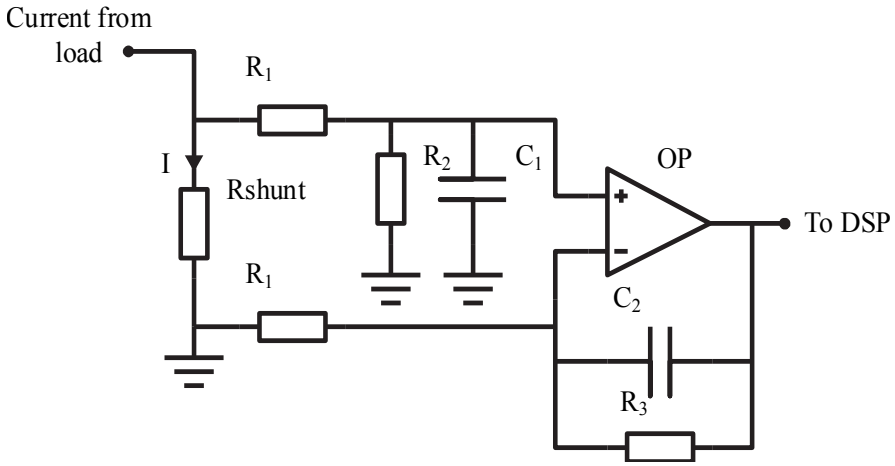

Figure 17 - Current sense resistor with differential amplifier.

3.3.3. Voltage Measurement

The ADC module on the DSP that measures the voltage on the output of the converter is connected to the existing voltage feedback of the buck converter via an active filter. The existing voltage division gives, at 32 V output, a voltage of 0.79 V into the analog controller, according to

$$V_{FB} = V_{OUT}\frac{R_2}{R_2 + R_1} = 32\frac{465}{465 + 18.3k} = 0.79V \tag{3.5}$$

Since the ADC uses 12 bit resolution (2^12=4096) in the range 0-3 V each step corresponds to 0.73 mV. This gives that the minimum voltage that could be detected on the converter output was around 30 mV. By increasing the voltage into the ADC to around 2 V, at 32 V output, it was possible to detect approximately 12 mV i.e. better resolution with enough headroom. In order to get the voltage to 2 V the resistors that constitute the voltage division had to be changed. This could be done in two ways; either increase the low voltage resistance or decrease the high voltage resistance. To increase the low voltage resistance gave the least effect on the circuit. The new resistance was calculated to 1200 ohm, according to

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{FB}} - 1} = \frac{18.3k}{\frac{32}{2} - 1} \approx 1.2k\Omega \tag{3.6}$$

The resistive voltage division is followed by an operational amplifier, which acts as a voltage follower with a second order Sallen-Key low pass filter. The filter was designed with a bandwidth of 70 kHz. The low pass filter was used to filter the high frequencies that originate from the switching of the MOSFET. By filtering these high frequencies a more accurate voltage measurement was obtained. The final design of the voltage measurement circuit can be seen in Figure 18.

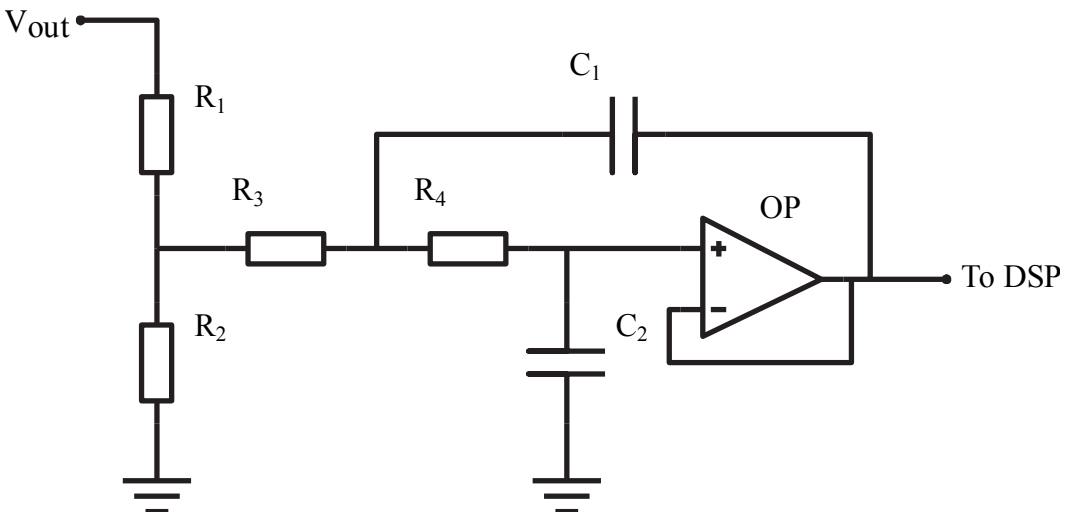

Figure 18 – Output voltage feedback and second order Sallen-Key active filter.

To measure the input voltage an operational amplifier has been used. Since the input voltage is constant and fairly free from noise only a first order filter with bandwidth of 234 kHz have been designed. By using negative feedback with a voltage divider, R2 (22 kohm) and R1 (1 kohm), the gain of the filter at DC frequency was set to -27 dB. In Figure 19 the input voltage measurement circuit can seen.

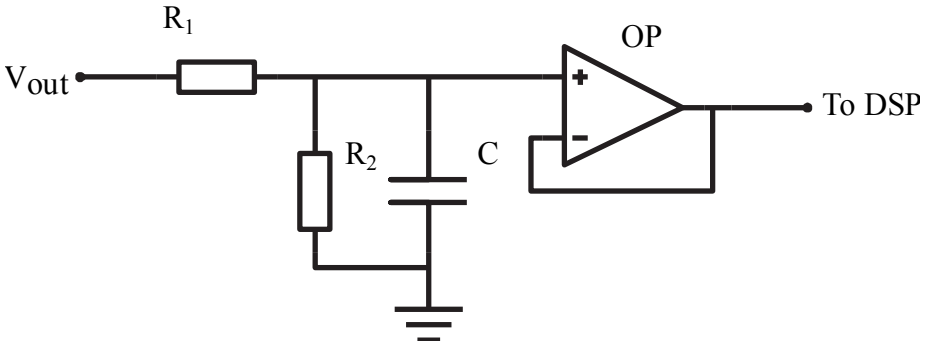

Figure 19 - Input voltage divider and filter circuit.

3.3.4. Temperature Measurement

High currents are flowing in the MOSFETs and due to their internal resistance they are subjected to power loss. This heat needs to be dissipated to not damage the transistors. If the transistors or their cooling system should fail the temperature will increase. To be able to stop the converter if a too high temperature should occur a temperature-monitoring device can be used. However since it is hard to fit the sensor to the converter the sensor is placed on the interface board and it has only been used to test the measurement and interfacing to the processor. A LM50 is used to measure temperature and the processor uses one of its ADC pins to read the voltage from the sensor and store the value in a register.

Due to that the output voltage from the sensor is dependent on a stable supply voltage a decoupling capacitors have been used to get a stable supply voltage. The output voltage was filtered with a capacitor to reduce the high frequency noise. In the processor the read value is scaled to the correct temperature using the relation

$$T = 0.01V(T) - 0.5 \tag{3.7}$$

3.3.5. Comparator

An analog comparator was constructed in order to measure the current load step in a more simplified way than what an ADC measurement is. The comparator, seen in Figure 20, uses a single operational amplifier. A reference signal of 1.65 V corresponding to 1 A was fed into the positive input of the op-amp and on the negative input the voltage signal out of the current measurement op-amp was fed in. This gave a comparator that gives a high signal on the output when the current is below 1 A and low signal when above. The output signal was then fed to one of the GPIO pins on the DSP that sensed which state, high or low, the pin was in.

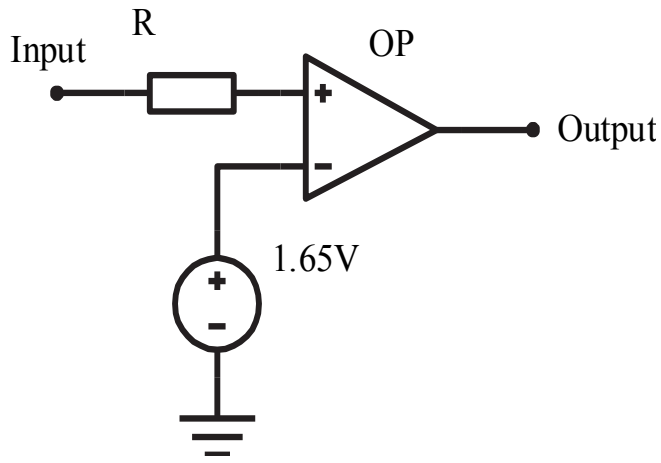

Figure 20 - Comparator

3.4.Program Structure

For the processor to perform the controlling task the sequence of execution of different tasks needs to be determined. Interrupt is used to control when different parts of the code i executed, this due to that some parts is time critical. The code responsible for the voltage measurement and voltage controller is executed during each PWM cycle to update the duty cycle for the next PWM period. The rest of the code responsible for other functions is run when there is time left. The PWM frequency is controlled by the clock frequency. It is also the PWM that initiate the ADC and when the conversions are completed the time critical code is run. After the PWM period is updated the other code is executed. This sequence is depicted in Figure 21.

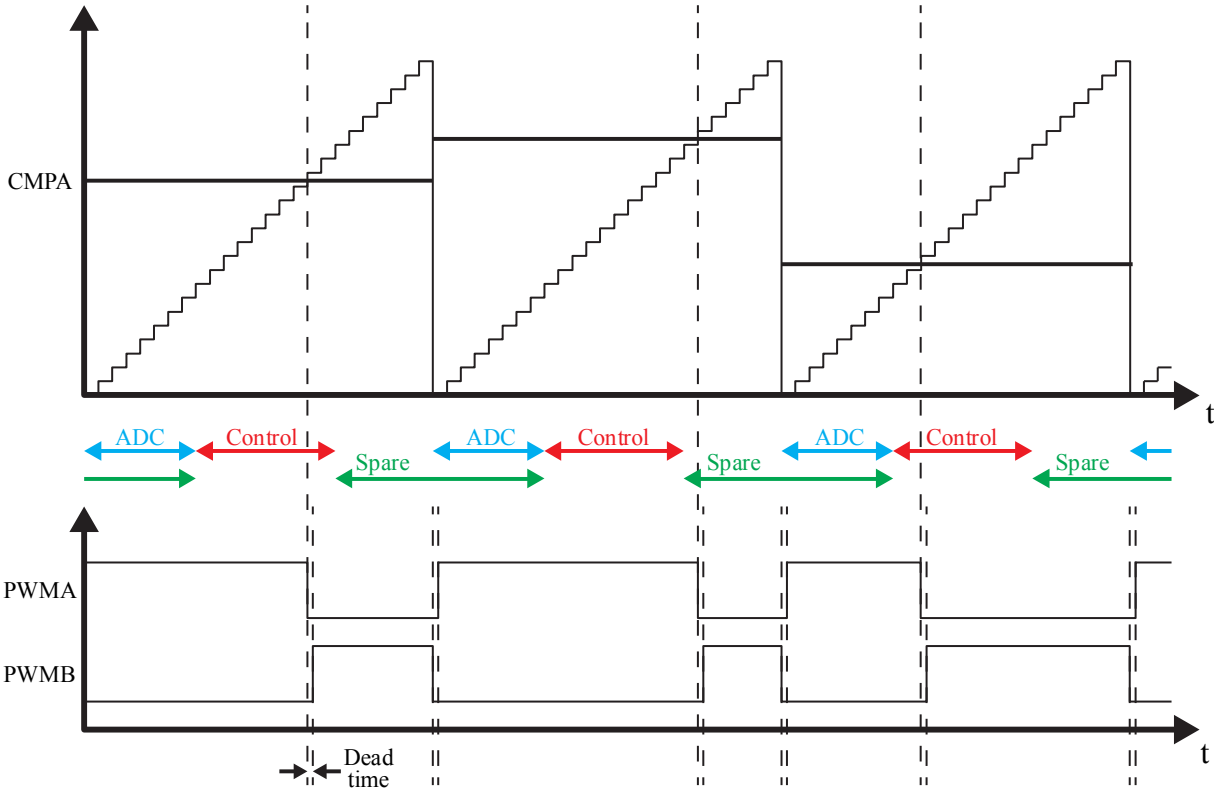

Figure 21 - Sequence of operation.

3.4.1. Soft-start

Soft-start is needed to limit the inrush current during startup. The high current is mainly due to the charging of the output filter capacitor. There are three conditions that need to be met in order to initiate soft-start. First the converter need to be enabled and then the converter should not have been in softstart before. The last condition is that the converter is connected to a power supply with the required voltage. When these conditions are met the soft-start function starts to ramp up the reference voltage until the normal operating voltage is reached. The increment of the voltage reference during soft-start is set by the user and determines the time needed to reach the final voltage. When the ramp up is done a flag is set to prevent the function from running again.

3.4.2. Active Control During Load Step

When the output current increases rapidly the voltage will drop until the controller is able to respond and increase the duty cycle in order to maintain the desired output voltage. By increasing the duty cycle more energy will be transferred from the input to the output resulting in that the load step will be mirrored, albeit delayed and with a smoother shape, from the output to the input. To limit the affect the load step has on the input current, it was possible to change how the converter was controlled during this instant. Previously in the analog controlled converter there was set an upper current limit, which was set significantly lower than the load step current. This resulted in that the output voltage dropped during a load step since the converter was not able to transfer enough energy fast enough to maintain the output voltage at the set reference. With the digitally controlled converter the output voltage was controlled during a load step instead. This method utilizes the ability to change the

voltage reference during operation i.e. decrease the voltage reference when a load step is detected and then slowly increase the voltage reference up to the converters normal operating voltage in between the load steps, as depicted in Figure 22. The equations

$$V_{DOWN} = \frac{I_{OUT,MAX}}{C}\frac{1}{f_S} \tag{3.8}$$

$$V_{UPP} = \frac{I_{OUT,MAX}}{C}\frac{D_{LOAD}}{1-D_{LOAD}}\frac{1}{f_S} \tag{3.9}$$

were used in order to calculate how fast the voltage was decremented and incremented during each switching period. f_S is the switching frequency, C is the total output capacitance and D_{LOAD} is the duty of the pulsating radar load,

The current load step was detected in two different ways, either using the ADC-module or with an external analog comparator. The ADC is used to measure the current and compare it to a reference, which is set so that when the current is above this threshold it is certain that a current load step has occurred. The analog comparator was used and a GPIO pin was set to 0 V or 3 V at higher or lower current respectively. Since the current into a capacitor is decided by the rate of change of the voltage across it, the voltage was linearly increased and decreased to get a constant current in and out of the filter capacitor.

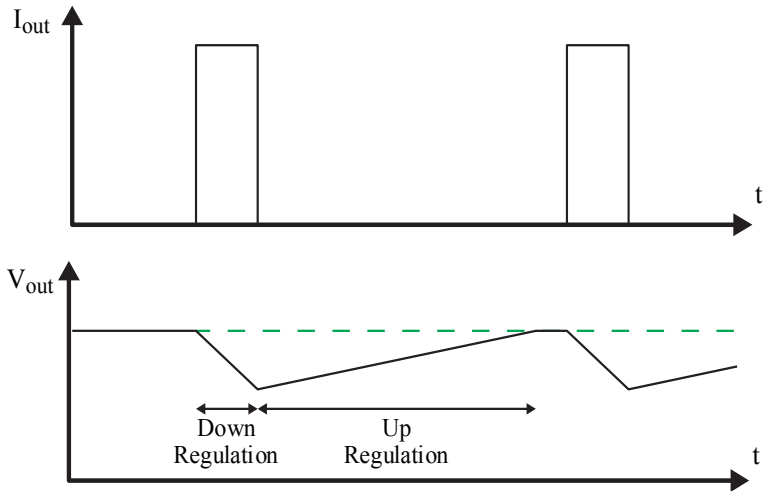

Figure 22 - Voltage and current during load step

3.5.Control

The control code consists of four different sections as seen in Figure 23, in the first section declarations of variables, functions and inclusions of additional header files are made. In the second section, which is the first part of what is called main, initialization of the PWM module, the ADC module, the GPIO pins used and enabling of interrupts are made. Section three, the second part of main, is an endless loop that runs whenever there is time left before or after the closed loop control code have been executed. In the infinite loop temperature reading, input voltage reading, soft-start mode and other non-time critical operations are executed. The last part is the interrupt code, which is the time critical code that needs to be executed at each PWM period i.e. 500000 times each second in order to maintain control of

the converter and its output voltage. This code is explained more thoroughly in Chapter 3.5.1 closed loop control, but its most important features are output voltage and output current reading, controller code, PWM register update and ADC reinitialization.

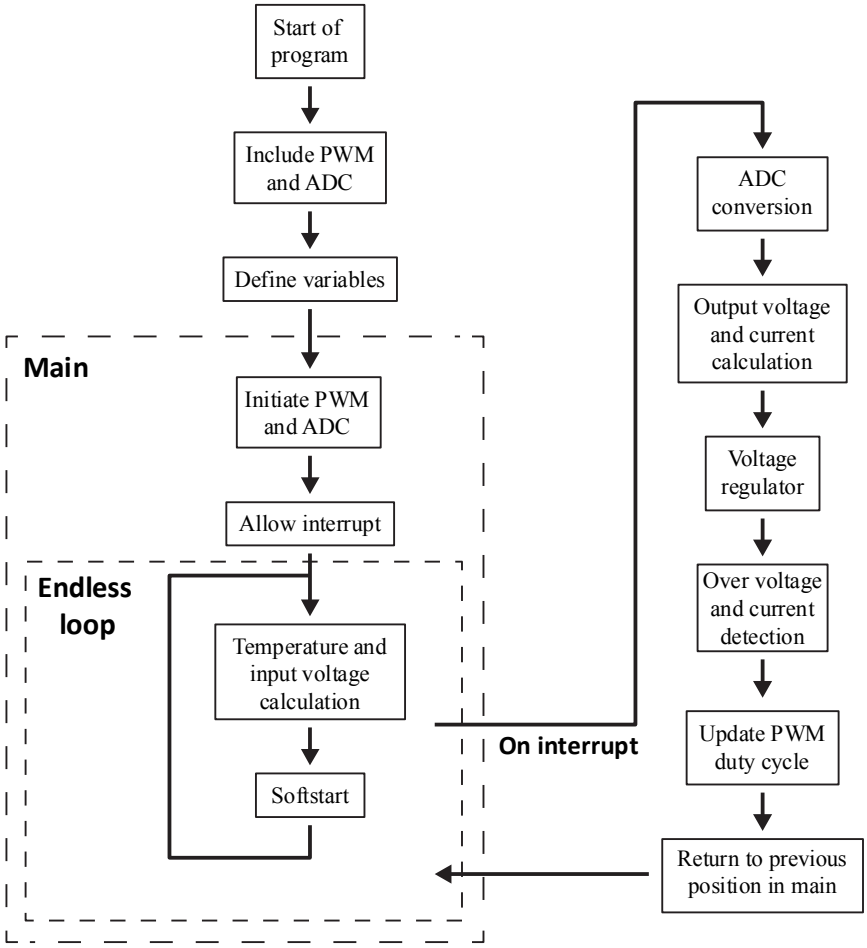

Figure 23 - Block diagram of how the control code is built up.

3.5.1. Closed Loop Control of the Buck Converter

When the PWM counter starts to increment, an interrupt is sent to the ADC module and the ADC starts the conversion. The ADC samples the signals two by two, first the input voltage and temperature are sampled and then the output voltage and current. The output voltage and current are sampled in the second stage since the first stage occurs directly after switching i.e. the output voltage and current are subject to oscillations directly after switching. When the conversion of all four inputs is finished and the values have been saved to the ADC register, another interrupt is sent. This interrupt triggers the start of the closed loop control code. The closed loop control code utilizes the difference equation (3.3) derived in Chapter 3.1 to calculate the duty cycle for the next PWM period. First in the control code the ADC registers for output voltage and output current are rescaled to match their real value instead of numbers between 0 and 4095. Since the controller is discrete and uses values from previous measurements, these values, voltage error and duty cycle, are stored for the last two samples. The stored values and the most recent voltage error are multiplied with their corresponding constants and then added up as

$$E(n-2) = E(n-1) \tag{3.10}$$

$$E(n-1) = E(n) \tag{3.11}$$

$$E(n) = Vref - v_{OUT} \tag{3.12}$$

$$D(n-2) = D(n-1) \tag{3.13}$$

$$D(n-1) = D(n) \tag{3.14}$$

$$D(n) = d1 \cdot D(n-1) + d2 \cdot D(n-2) + e0 \cdot E(n) + e1 \cdot E(n-1) + e2 \cdot E(n-2) \tag{3.15}$$

The next step after the duty cycle calculations is to verify if the voltage and current are within specified limits. This is done with a simple conditional statement. If this statement is true i.e. the voltage or current are too high the duty cycle is set to zero.

When the new duty cycle has been calculated it has to be written to the PWM registers. Since the PWM period is built up by coarse and fine steps there are two registers that have to be written to, one for coarse and one for fine steps. The normal PWM register uses an integer number between 0-300, which is the number of course steps on one PWM period and outputs a duty. A duty cycle of 0.6 corresponds to 180 i.e. 0.6*300=180. The HRPWM register with its fine step control is somewhat different since it is only activated if the duty cycle times the period is a number with a fraction i.e. 0.405*300=121.5. By subtracting the integer only the fraction is left and this is then written to the HRPWM register after it has been scaled to a number between 256-65536.

After the registers have been updated, the ADC module is initialized in order for it to be ready for the next conversion interrupt. The interrupt is also cleared and the program jumps back into the endless loop.

3.5.2. Protective Features

To protect the components in the system, a number of protection features have been implemented. These functions does not only protect the DC/DC converter but also the devices before and after from failure in the converter or the supplied devices. The first type of protective function often thought about is current limiting. This is done by monitoring the current with the ADC and compare it to a reference. If the current increase over the reference the converter is shut down. Over current protection could also be implemented with the use of the analog comparator. The reference in the comparator could be set so that it corresponded to an overcurrent in the shunt resistance. And when the voltage across the shunt resistance became larger than the reference, the output of the comparator would be grounded and the DSP would the shut down the converter.

Over and under-voltage protection was implemented in the same way i.e. monitoring the voltage with the ADC and compare it with two references and turn off the converter if the voltage was out of range. Since the output voltage is measured and used in the control loop, no extra measurement had to be made. The input voltage is also monitored to make sure that the supplying bus voltage is correct.

3.5.3. Tuning of Control Parameters

The controller obtained through modeling and simulation, which is described in Chapter 3.1, does not work perfectly with the converter. This is due to several reasons but the main reasons are that the model of the converter does have some inaccuracies in the parameter estimations and the linearization of the transfer function does not explain the system perfectly. In order to obtain a faster and more accurate controller, tuning of the control parameters had to be performed. This was done in real time during operation of the converter. The converter was run normally with the pulsating load and without the "control at load step" and the external output filter. The output voltage was captured with the oscilloscope and its behavior was observed when the control parameters in the difference equation, (3.3) in Chapter 3.1, was incremented and decremented. The controller that was found to be the fastest with the least overshoot is described as

$$D(n) = 0.2573D(n-1) + 0.7432D(n-2) + 1.0441E(n) - 2.0168E(n-1) + 0.9762E(n-2) \qquad (3.16)$$

3.6. Test Setup

Seen in Figure 24 is the setup of how the DSP, DC/DC converter, its power supply, interface board, the dynamic load and measurement equipment were connected. The DSP is mounted to an evaluation board from Texas Instruments. Between the DSP board and the DC/DC converter an interface board is connected. Some of the interconnections between the different boards are shielded. The system is supplied from two different sources, one for the interface board and the other for the converter. The interface card is supplied with 8 V and the converter with 56 V. Depending on the test performed, the filter is connected between the converter and the load. To simulate the radar transmitter current consumption a dynamic load is used. In order to program the processor it is connected to the PC via USB.

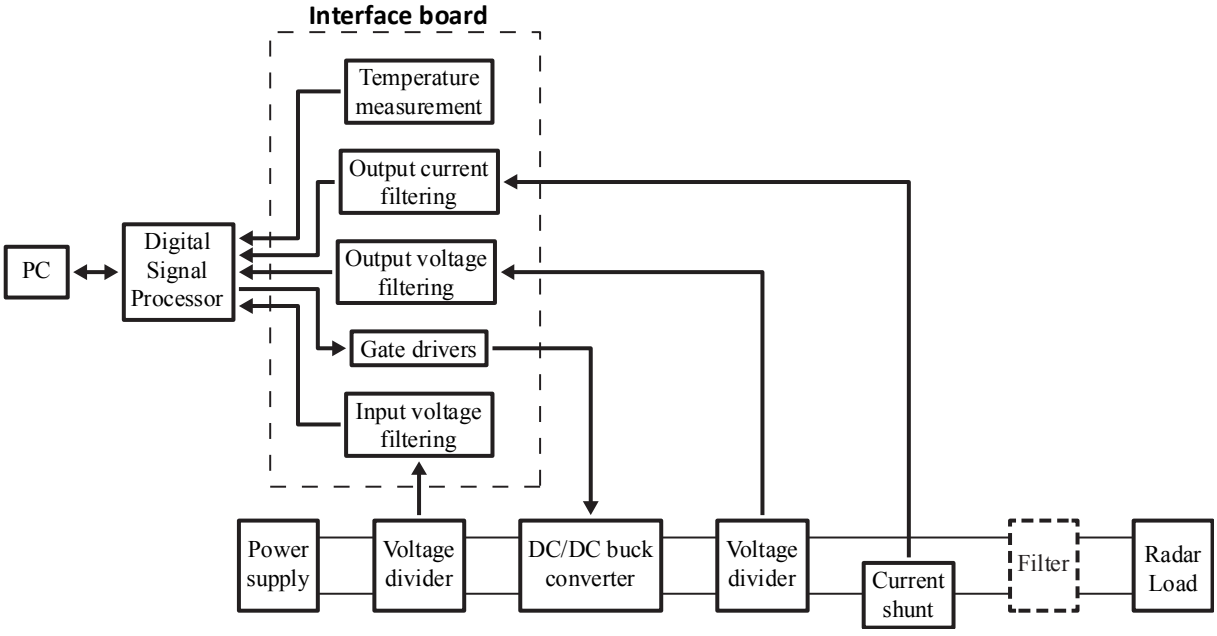

Figure 24 - Test setup.

Figure 25 depicts the buck converter and the interface board and how they are interconnected.

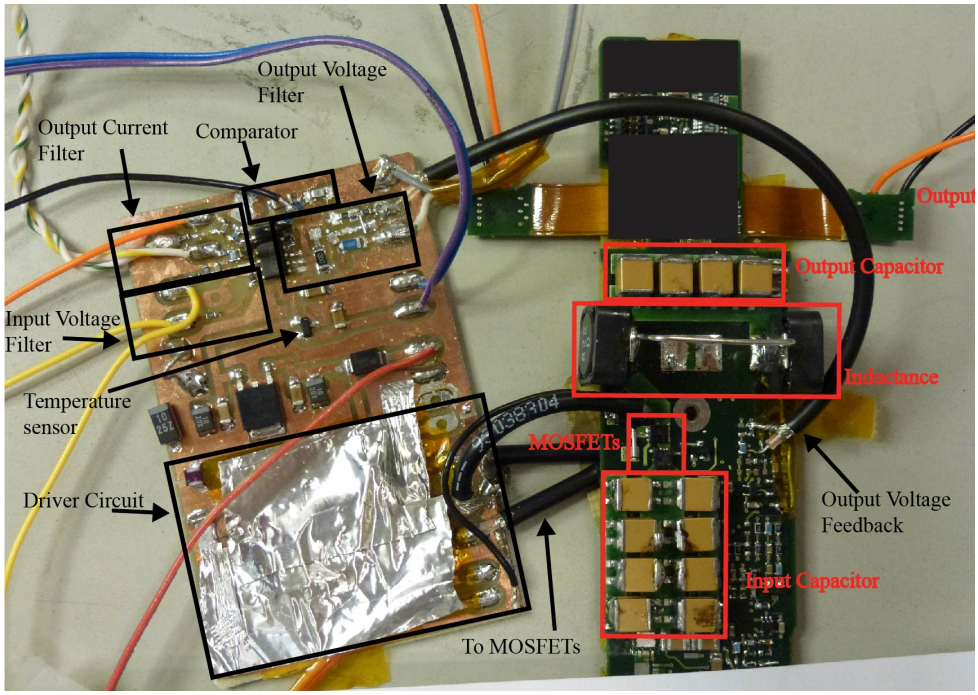

Figure 25 - Buck converter and interface board.

Seen in Figure 26 is the Delfino F28335 floating point DSP mounted on the evaluation board.

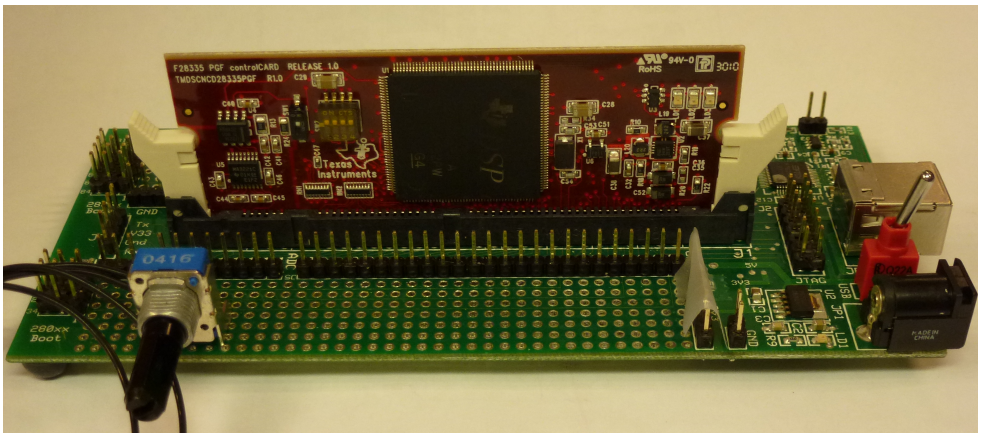

Figure 26 – Texas Instruments evaluation board with the DSP mounted.

3.7.Evaluation strategy

To evaluate the digitally controlled converter, its performance was compared with the analog controlled converter's performance. Since the analog converter have fixed output voltage the test was conducted on one voltage level only i.e. 32 V output. When running the converter at 32 V the radar load current was applied and the behavior of both converters with and without external filter was studied. The "control at load step" function was also studied and the currents and voltages were compared to when the function was not activated in the DSP. The protective features were evaluated by changing the maximum reference below normal levels during operation and by studying the effect. To test if the soft-start function worked properly, the converter was started and voltage and currents were studied.

The circuitry on the interface board i.e. driver circuit, input and output voltage filter, output current filter, comparator and temperature circuit were tested separated from the converter. The output and input filters were evaluated by applying sinusoidal signals of different frequencies on their inputs and study the amplitude of these signals on the output. The temperature sensor and its temperature response were tested by applying a heat source to the sensor and study the voltage response.

4. Results

In the results chapter the results obtained through measurements of the analog and digital controlled converter and its additional circuitry as well as the simulated results are presented and discussed.

4.1.Simulation results

The simulations done in Matlab/Simulink were performed with the same type of load and voltage level as the digitally controlled converter was intended for. In Figure 27 is the voltage and current depicted when a pulsating load has been applied. From the figure it can be seen that the controller is fast at reacting to the load step although, due to the voltage overshoot, it does not reach steady state during the load step. When the load step ends the voltage increases and then oscillates a little until it reaches steady state after around 0.28 ms after the load step has ended. The voltage deviates about 0.22 V from the reference of 32 V regardless if the load step starts or stops.

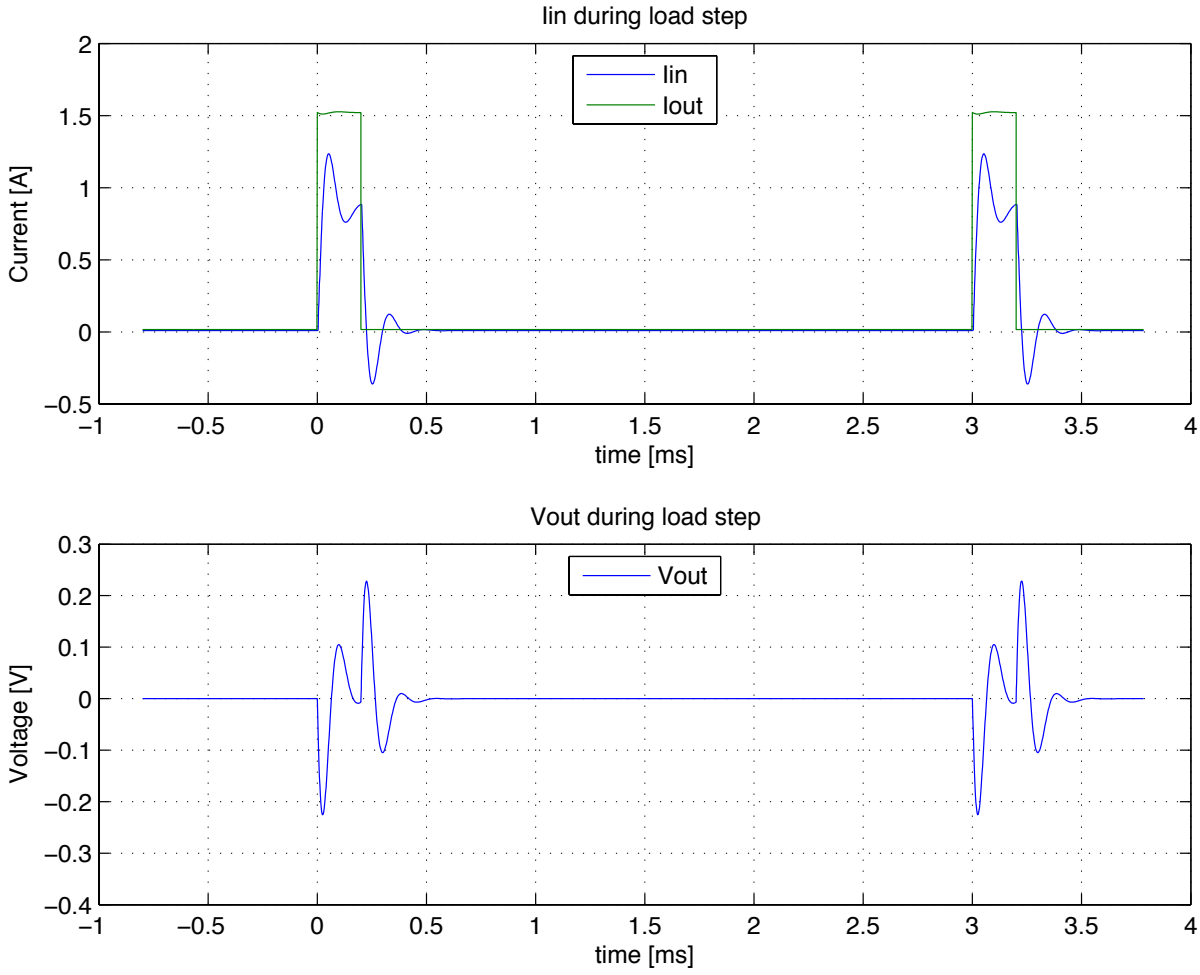

Figure 27 - Simulated output voltage and input current responses during a radar pulse.

The input current also exhibits a little bit of oscillation, which can be expected by looking at the voltage waveform. The peak value of 1.22 A is realistic since the input voltage is 1.75 times larger than the output voltage. Although this controller is not the fastest it performed well enough so that it could be used in the DSP as first starting point.

4.2.Interface Board

In this chapter the performance and function of the additional circuitry are presented. Each circuit is presented separately and the results are discussed briefly.

4.2.1. Driver Circuit

The speed of the driver circuit is sufficient for both high and low side MOSFETs as seen in Figure 28. The delay between the input and output is consistent for both channels. It is always a bit of lag from when the input changes state until the output does, for this driver it is around 50 ns. If the delay is not consistent it can cause both MOSFET transistors to be on at the same time even if dead time is used. The dead band delay was set to 100 ns in the DSP and the measured delay is around 80 ns.

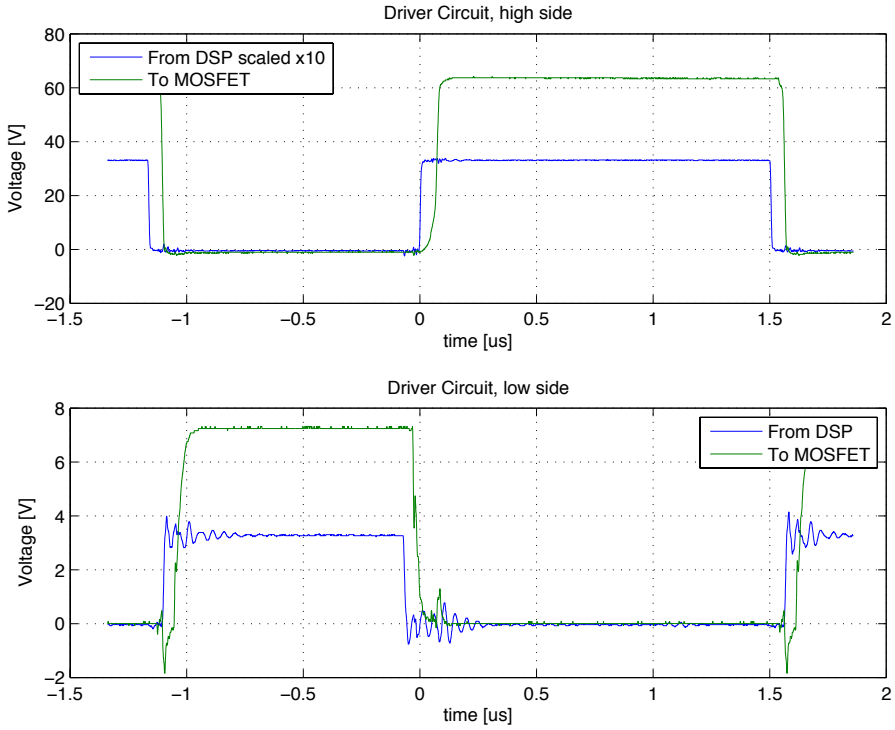

Figure 28 - Measured waveforms of signals from DSP to driver circuit and from driver to MOSFETs, high and low side.

The driver does also provide enough current to the gate in order to switch the MOSFETs fast enough to reduce the switching losses. The high derivatives of the voltages and currents of the driver and the MOSFETs generate interference. This does not affect the driver or the converter but the measurements will suffer from the noise. To suppress the noise it is important to minimize the distance between the driver circuit and the MOSFETs and to try to decouple the driver from the supply to reduce the noise. The bootstrap configuration makes it easy to drive a transistor half bridge and the limitations in the range of duty cycle do not cause any problems. This due to that the duty cycle is fairly constant around 57% in normal operation and during transients never close to 100%.

4.2.2. Current Measurement

In Figure 29 a typical load step is plotted together with the output from the current measurement circuit. As seen the measured current have a delay of 5 µs, and this due to the operational amplifier. The frequency response of the active filter is depicted in Figure 30 and from the figure it can be seen that the cut off frequency is at approximately 45 kHz and the gain is around 23.5 dB at DC frequency, which corresponds well to how the filter was designed. The filter is used to limit the interference from the switching noise and the ripple in the current. The total gain of the current measurement at DC is 4.38 dB and that is from actual current to voltage into the DSP. From Figure 30 it can be seen that the bandwidth of the current sensor is sufficient and the waveform is not too distorted. There are still some problems with noise and this affects the accuracy of the measurements.

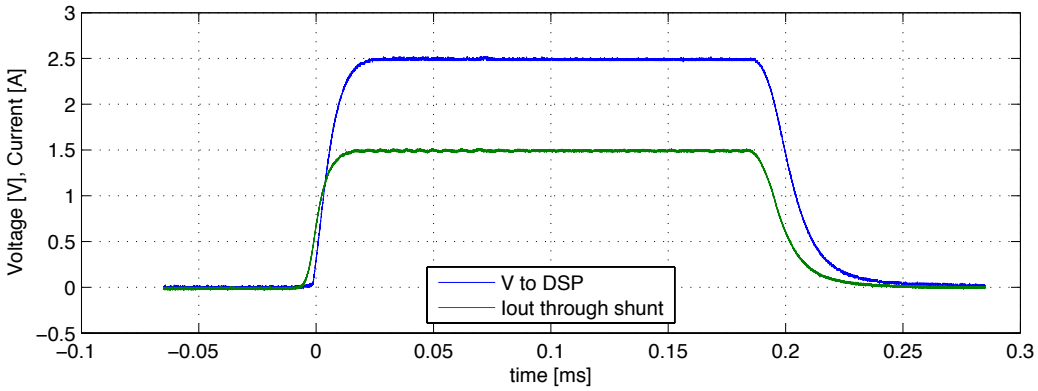

Figure 29 - Measured response of current measurement at a load step.

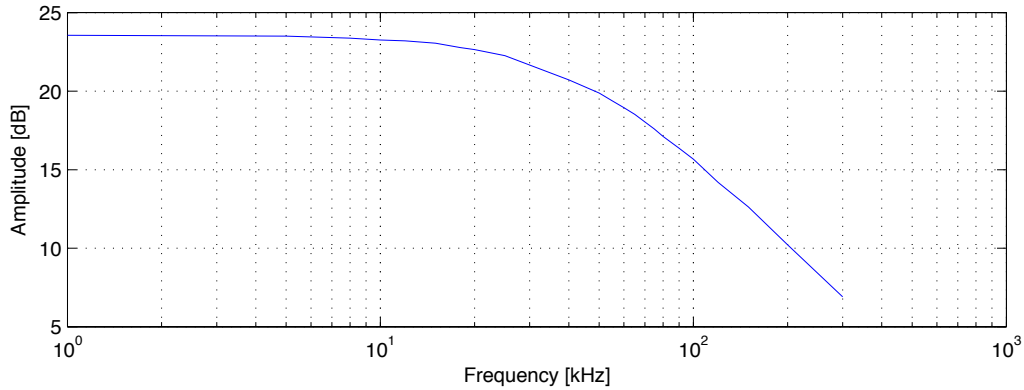

Figure 30 - Measured frequency response of current measurement circuit.

The shunt resistor will affect the output voltage measurement depending on if the shunt is placed before or after the voltage divider. If the shunt is placed after the output voltage divider the output voltage will drop with the output current. Instead of using a shunt resistor an inductive sensor can be used in order to remove this effect. An inductive sensor will also improve the suppression of noise. The efficiency will also increase since the sensor does not use a resistor to measure the current. Since the current measurement is only used to sense when the load step occurs or if there is an overcurrent the accuracy is not as important as with the voltage measurement circuit. From this reasoning it can be concluded that the circuit measurement works satisfactory although there are could be work done to minimize the delay.

4.2.3. Comparator

The comparison between the current and the threshold takes some time for the processor to perform, so instead of doing this comparison in software this can done in hardware with the comparator. If overcurrent protection were to be determined with a comparator instead of in software, as it is done at the moment, another comparator with a voltage reference corresponding to an overcurrent in the current shunt is needed.

In Figure 31 the current step together with the digital output from the comparator to the DSP is plotted. The threshold is set at 1A and as seen there is a delay of around 6 µs from when the current reaches the threshold until the output goes low. This delay is due to operational amplifier both in the comparator and the current measurement circuits. The delay is a bit problematic since this will affect when the down and up regulation of voltage starts and ends during a load step. Another thing to note is that the signal is inverted, which mean that when output is high the current is below the threshold.

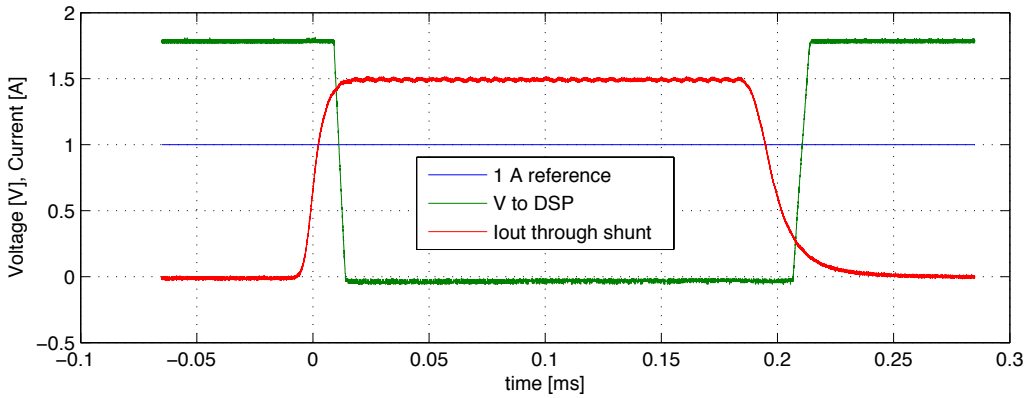

Figure 31 - Measured response of current comparator when a load step occurs.

4.2.4. Voltage Measurement

The second order Sallen-Key filter used for output voltage was designed to have a bandwidth of 70 kHz and as seen in Figure 32 the 3 dB amplitude drop occurs at around 80 kHz. Since most of the noise and disturbances comes from switching of the MOSFETs, the switching frequency (500 kHz) needs to be well suppressed so that these disturbances does not interfere with the measurement. If the curve in Figure 32 is extrapolated it can be seen that the filter has a damping of around 50 dB at 500 kHz. The overall gain of both the voltage follower and the resistive voltage divider was measured to -24.3 dB at DC, which is close to what it was designed for. If the filter was designed with a bandwidth closer to the controller's bandwidth (around 15 kHz) the filter could interfere with the control loop and make the system, in the worst of cases, unstable or at least slower.

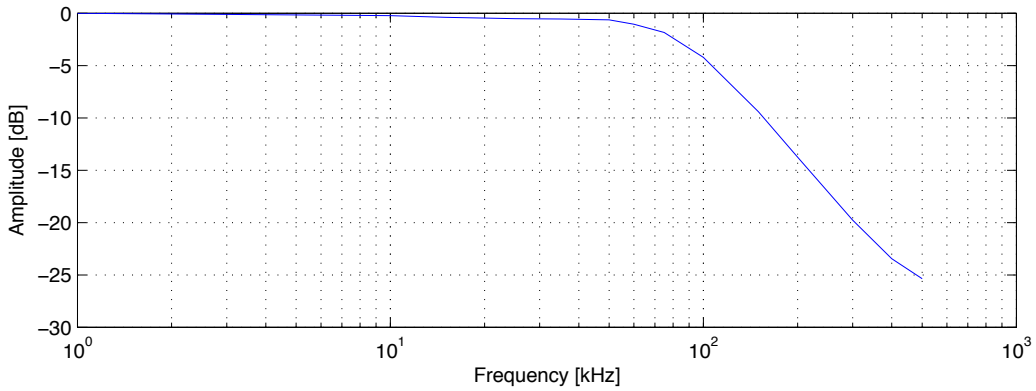

Figure 32 - Measured frequency response of the output voltage filter.

Even though a filter is used for the output voltage, some parts of the noise reached the DSP resulting in variation in the measured voltage and thereby variations in the duty cycle. This affects the stability of the system negative.

In Figure 33 the frequency response of the input voltage measurement is depicted. The filter was constructed with a gain of -27 dB and a bandwidth of 234 kHz. From Figure 33 it can be seen that the cutoff frequency is at 400 kHz and a DC gain of -27 dB. Since the input voltage is almost constant and not subject to much noise the high bandwidth of the filter does not cause any problem. The strange shape of the response is probably dependent on the operational amplifier's lack of bandwidth at these frequencies and gain.

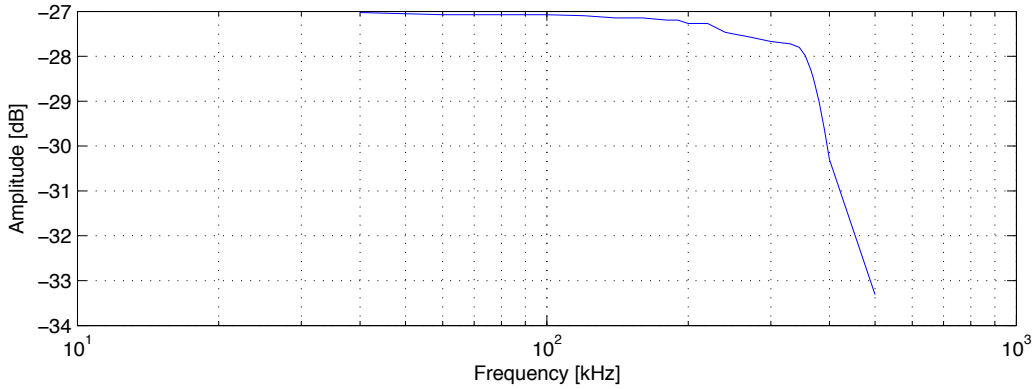

Figure 33 - Measured frequency response of the input voltage filter.

4.2.5. Temperature Measurement

In Figure 34 the temperature response is plotted, at t = 0 s the sensor is at room temperature and a heat source is added. In 7 s the output have stabilized to the new temperature, which is a response time much faster than needed. At the start of the measurement the room temperature was measured to 23˚C but the sensors output corresponded to 26˚C according to (3.7) in Chapter 3.3.4. However, due to that the temperature sensor is only used to detect abnormal operating temperatures the accuracy is not that important and a 3 degrees offset is not a problem as long as the offset is constant over the entire temperature range.

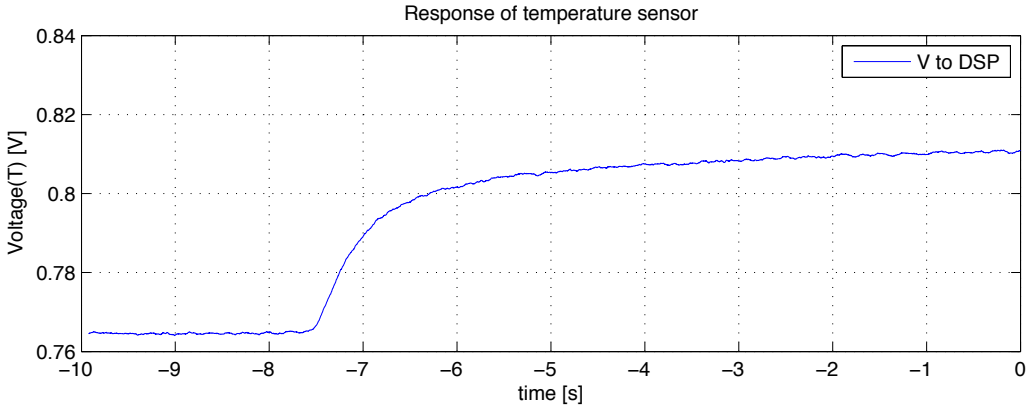

Figure 34 - Measured voltage response of the temperature sensor when a heat source is added.

4.3.Buck Converter

In this part the results of both the analog and digitally controlled converter are presented. Both converters were tested with and without the external filter. The converters performance was evaluated with either a pulsating load or a load step.

4.3.1. Regulations Speed at Load Step

In Figure 35 the speed of regulation of the converter at a load step (0 to 1 A) can be seen for both the analog and digitally controlled converter without the external filter. The digitally controlled converter has a faster voltage recovery than the analog as seen in Figure 35. It takes about 200 µs and 300 µs to reach steady state for the digital and analog controller respectively. The analog controller also has some overshoot compared to the digital that reach the reference without any overshoot. The voltage deviation is more or less the same, 0.7 V, for the digital and analog controller.

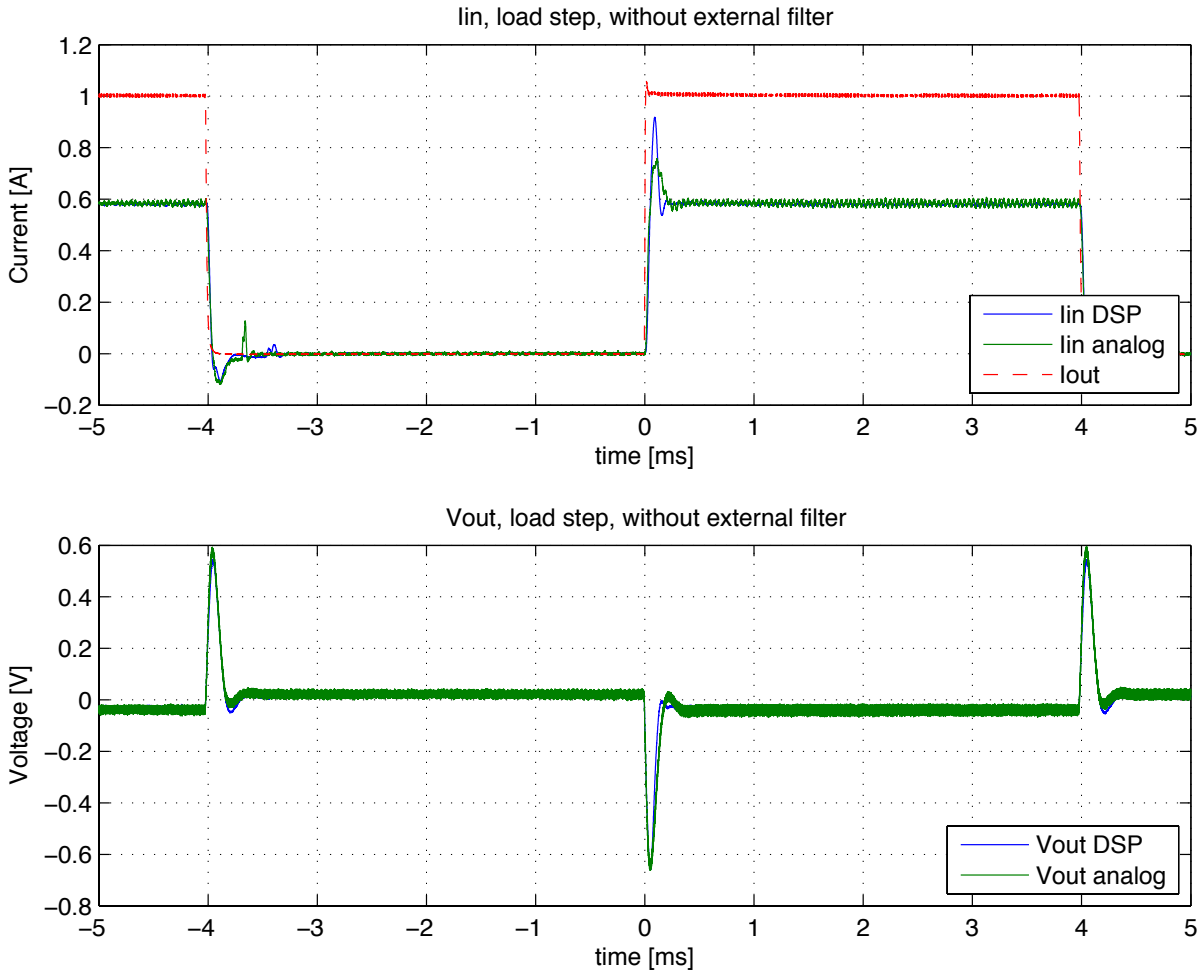

Figure 35 - Measured regulation speed at load step, without external filter.

Depicted in Figure 36 is the voltage and current waveforms during a load step when the external output filter has been connected. From Figure 36 it can be seen that the regulation speed is decreased substantially due to the external filter. The current peak is lower compared to when no filter is used, which is good for the devices supplying the converter since they do not need to handle as high current peaks as the converter.

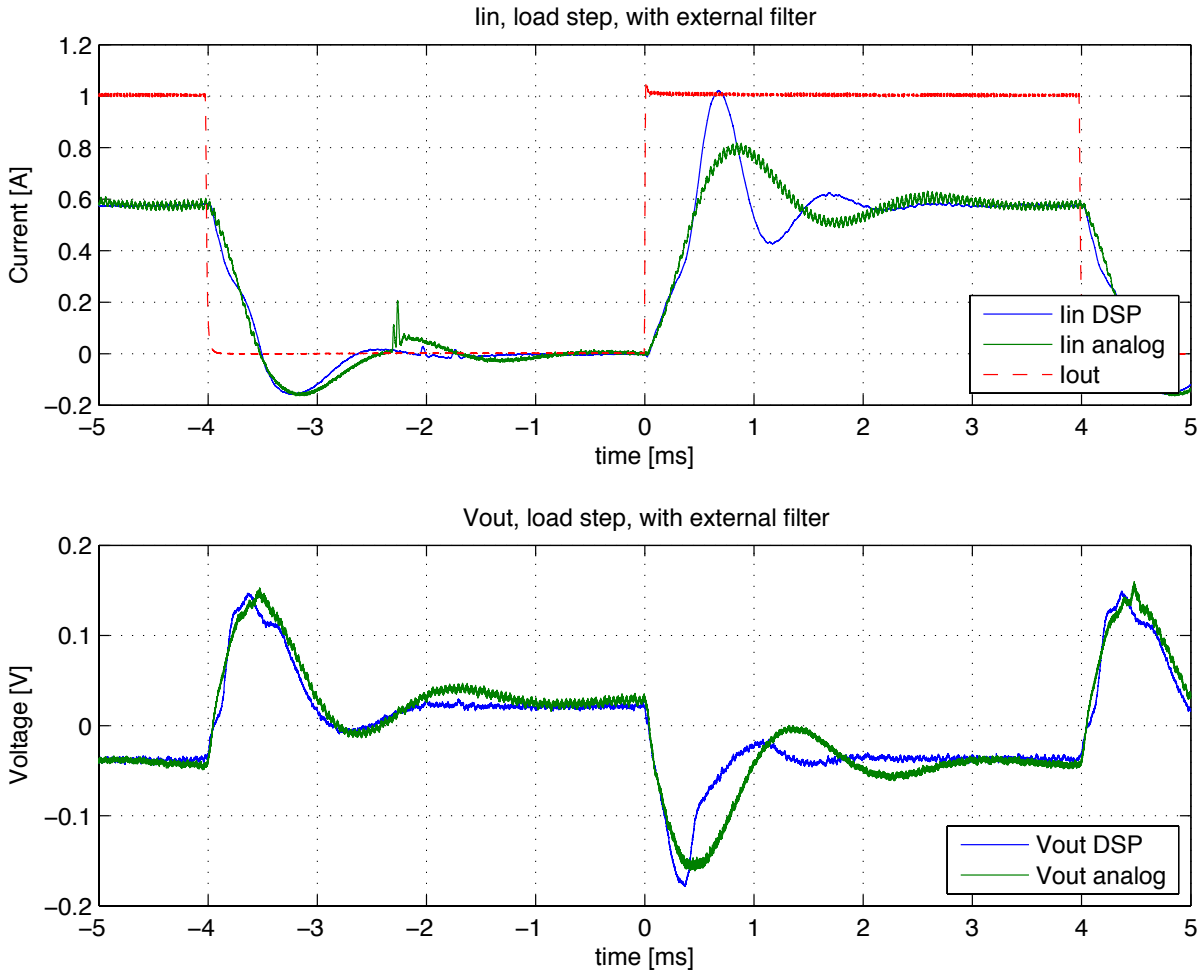

Figure 36 - Measured regulation speed at load step, with external filter.

4.3.2. Regulation Speed with Radar Load

When the converter is subject to a pulsating load i.e. a radars load characteristics, the behavior differs from the figures shown in Chapter 4.3.1. Due to that the pulse is only 200 µs long the controller of the converter is not fast enough in order for the voltage reach the reference before the step is over. This will result in an oscillation in the output voltage with a voltage under the reference during the load step and a higher voltage after the step, as seen in Figure 37. Without the external output filter the current on the input and output are quite similar in shape, although the input current is a bit distorted. This is due to the controller and the input and output filters of the converter. The peak input current is around 1.3 A.

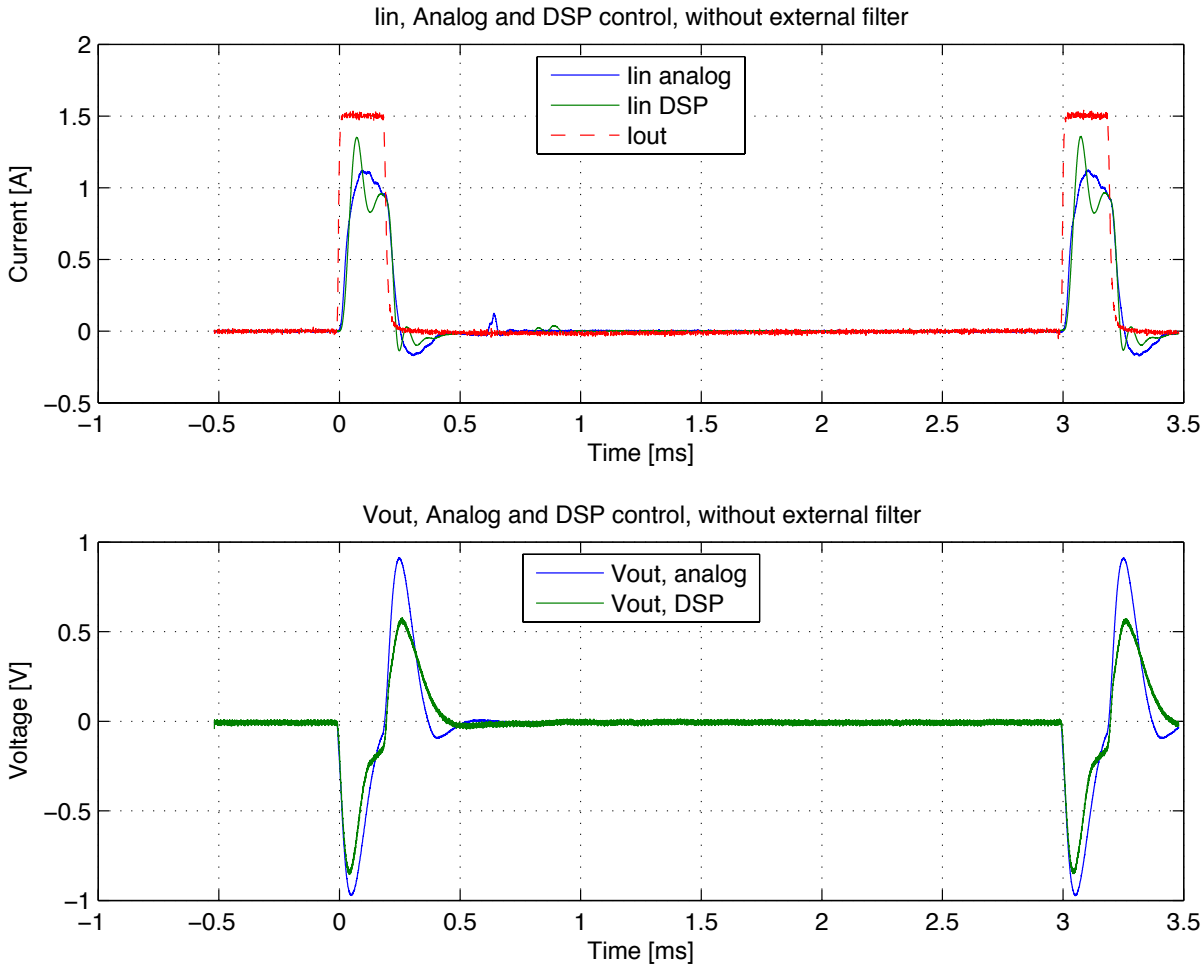

Figure 37 - Measured input current and output voltage behavior during radar load, without external filter.

When the external output filter is used the input current amplitude is decreased and the time the converter consumes current is prolonged compared to the load step length. The peak is only a fourth compared to when no external filter is used as seen in Figure 38. There is also a difference in current peak value between the analog and digital controller. This is mainly due to the overshoot in the voltage for the analog controller. The peak voltage drop from the voltage reference is only one fifth of the voltage drop that occurs without the filter. However the time duration of the disturbance is longer. Since the energy consumed for each pulse is almost the same the time and amplitude of the current is closely related to each other i.e. low current longer duration, high current short duration.

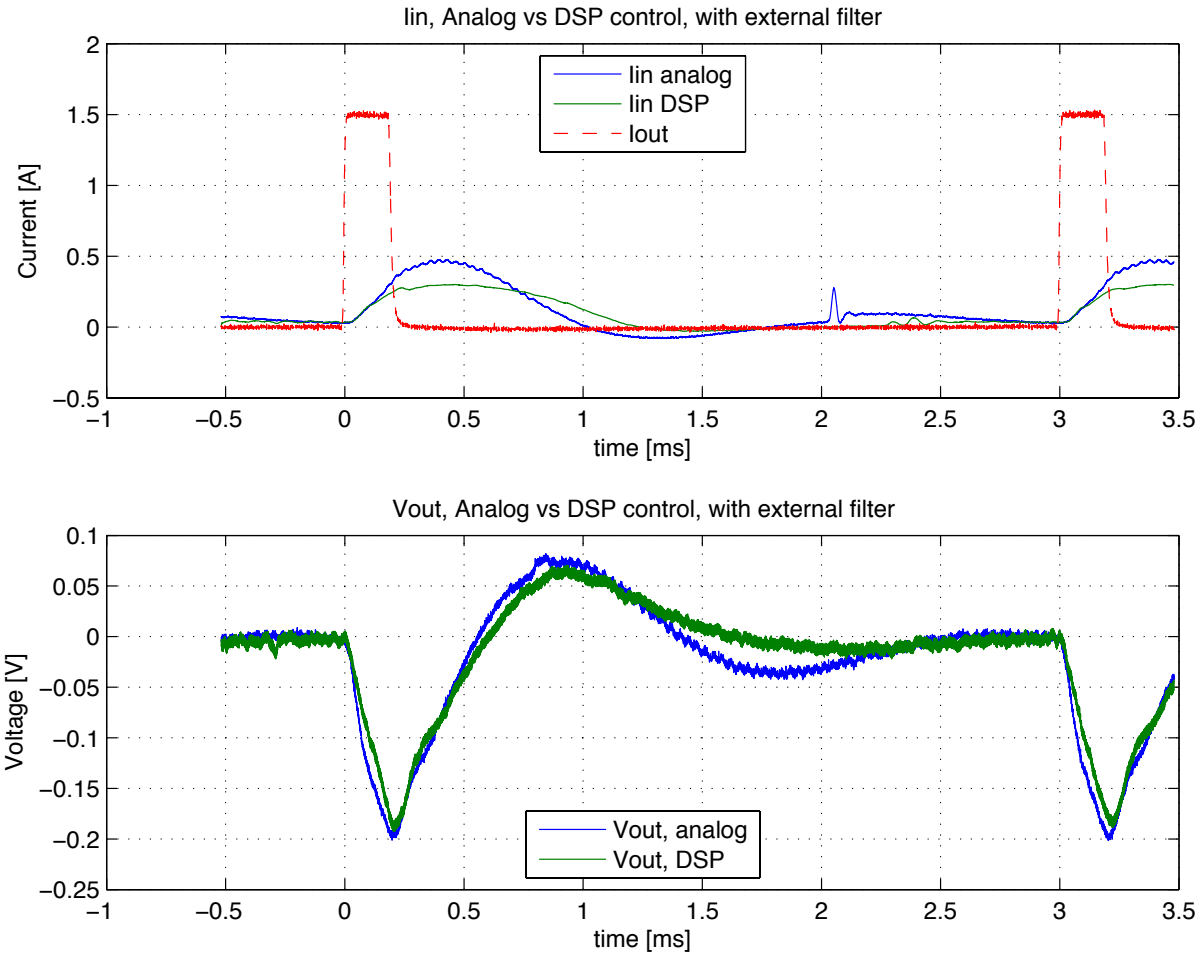

Figure 38 – Measured input current and output voltage behavior during radar load, with external filter.

The external filter improves the input Root Mean Square (RMS) current as seen in Table 1. This will decrease the requirements on the devices before the converter since they do not have to handle the big current pulses. To further improve the RMS current the external filter can be increased but this will make the filter even bulkier.

Table 1 - RMS input current during normal operation with digital and analog controller.

	Digital	Analog
With external filter	0.141 A	0.188 A
Without external filter	0.248 A	0.251 A

4.3.3. Active Control During Load Step

The voltage curve named *Iin DSP with load step control* seen in Figure 39 is the voltage during a radar load step when load step control has been activated in the DSP and the external filter is used to smoothen the voltage and current. The voltage and current curve with normal DSP control are the reference curve. At a detection of a load step, the voltage is decremented and the load is mostly supplied from the output and external filter capacitor. When the load step has passed, the voltage is slowly incremented with the rate equaling a constant current into the capacitors according to (2.5) in Chapter 2.1.1.

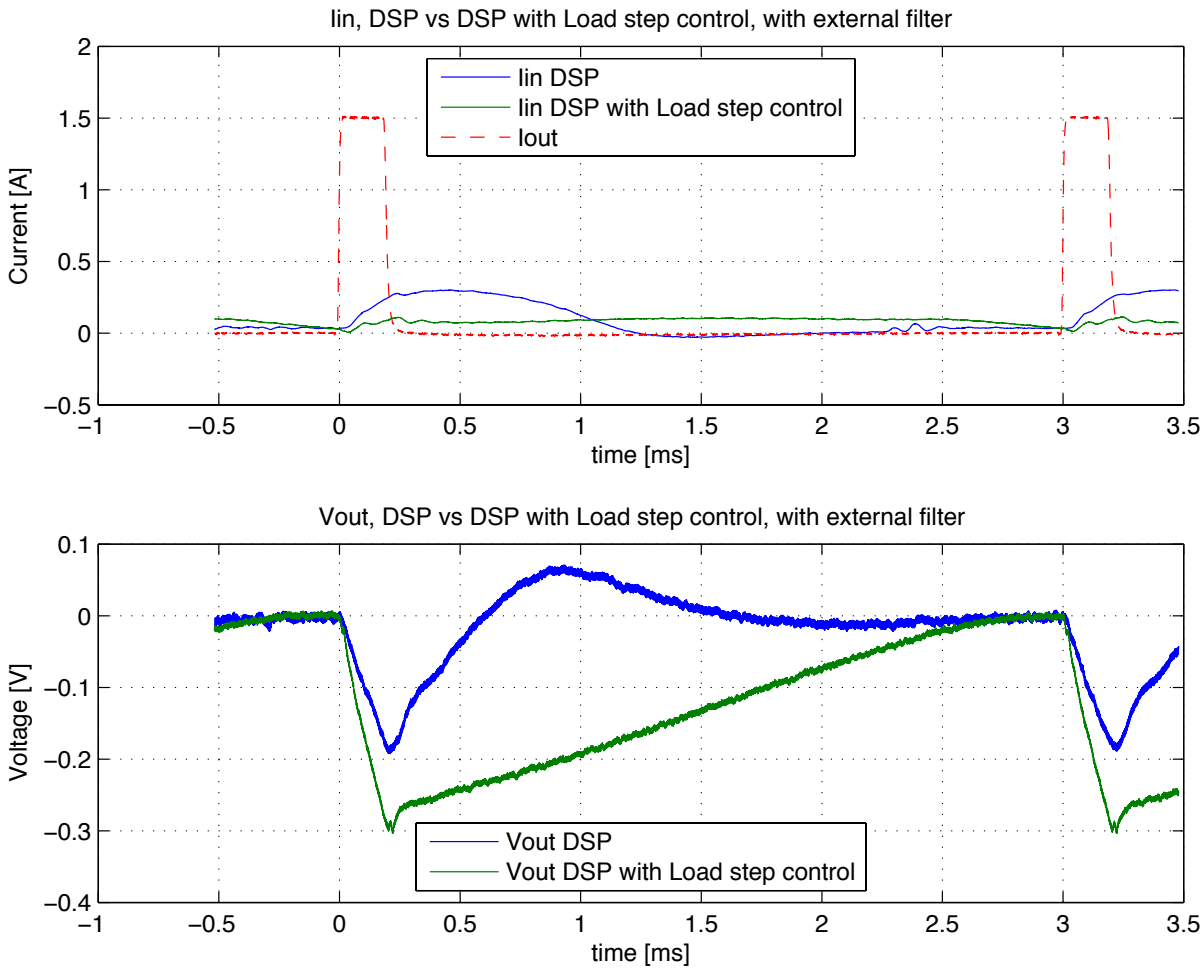

Figure 39 – Measured input current and output voltage curves during radar load with active control, with external filter.

Figure 40 depicts the output voltage together with the in and output current during a load step where active load step control has been activated and the external filter is in use. The *Vout DSP* and *Iin DSP* curve are the reference curve without load step control, which are discussed in chapter 4.2.2. When the load step occurs the voltage reference for the load step control 1 and 2 are linearly decremented from 32 V down to 31 V and 29.5 V respectively (the zero level in Figure 40 corresponds to 32 V). As soon as the load step is over the voltage is linearly increased. The same increment step have been used for both curves but since the load step control 2 curve have a lower starting voltage it will of course take longer time for the voltage to reach 32 V.

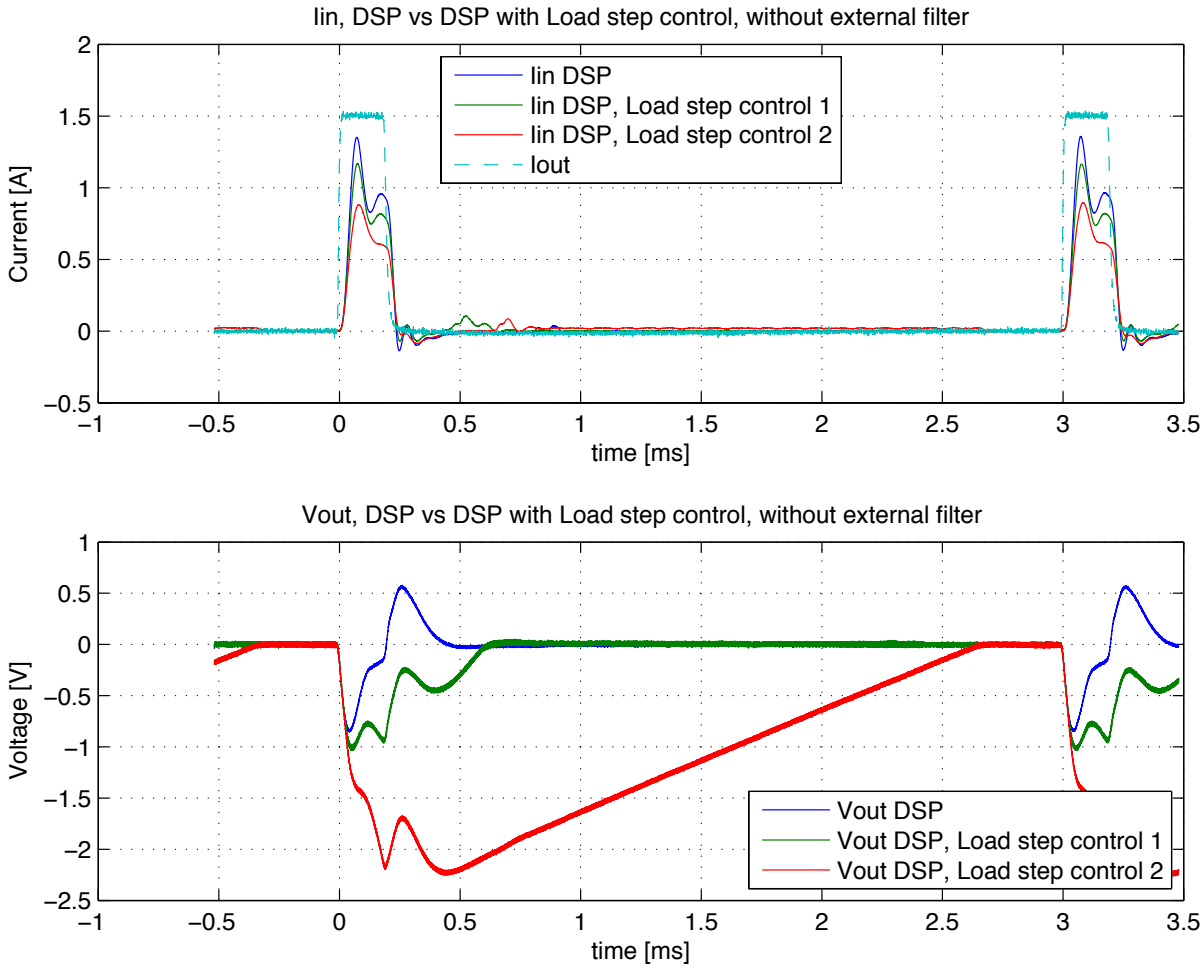

Figure 40 – Measured input current and output voltage curves during radar load with active control, without external filter.

Looking into how the input current behaves during the load step it can clearly be seen that the peak values are decreased when the load step control is activated. This is due to that the current taken by the load is partly supplied from the output capacitor, which releases its stored energy to the load when the voltage is lowered. After the load step the capacitor is slowly recharged since the voltage is increased, hence the small current into the converter. At load step control 2 the current is more or less constant at around 0.02 A until the voltage have reached the reference value for normal operation and then goes to zero. This is in line with what could have been expected.

When this control technique is used the RMS current over the period is decreased as seen in Table 2. The external filter can thereby be decreased and the same performance as for the analog controller with the filter is maintained.

Table 2 - RMS input current with digital control with and without active load step control.

	Normal control	Load step control 1	Load step control 2
With external filter	0.141 A	0.087 A	-
Without external filter	0.248 A	0.217 A	0.227 A

4.3.4. Soft-start and Protective Features

The soft-start function works as expected i.e. the voltage is slowly incremented until it reaches the normal operating voltage as seen in Figure 41. The increment step is easily adjusted in the software for a faster or slower ramp up. The important aspects of the soft-start function are how the voltage is ramped up to the reference and how the program appropriately switched to normal control mode after the completion of the soft-start.

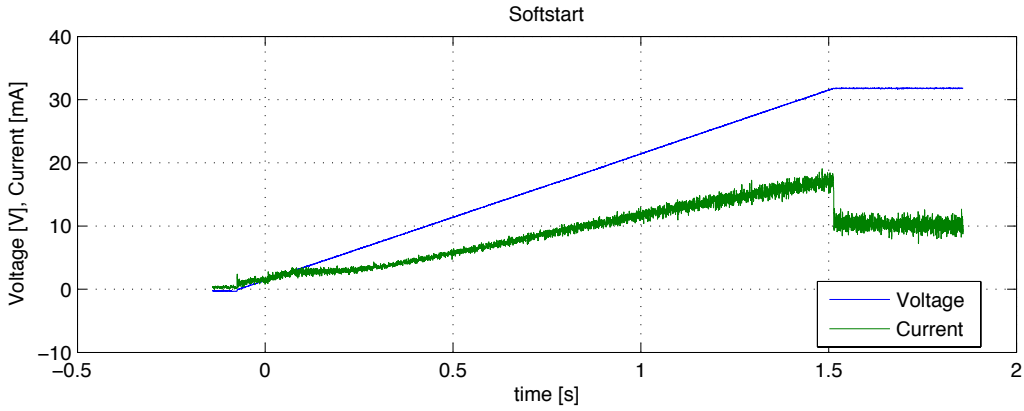

Figure 41 – Measured voltage and current waveforms during soft-start.

The functions for overvoltage and overcurrent protection perform as expected. The overvoltage and overcurrent limits were changed during operation to a value, which would trigger the functions and shut down the converter. If there was a violation of these limits the converter did shut down immediately. One change that could be made in the software is to add a memory that saves the previously measured overvoltage or overcurrent value or values and wait until next sample is made and check if the limits are still violated. With this function, the converter would become more resistant to faulty trips.

4.3.5. Efficiency and Power Consumption

The efficiency for both the analog and digitally controlled converters are measured for different constant load currents and without the external filter. In Figure 42 the highest efficiency is for the higher currents for both converters. The best efficiency for the digital is 93% and for the analog 94%. The low efficiency at low currents is mainly due to that the converter have some losses that is not dependent on the load current i.e. control circuitry, support voltages and since the converters always work in CCM. At no output current the analog and the digital controlled converter consumes roughly 1.6 W and 1.13 W respectively.

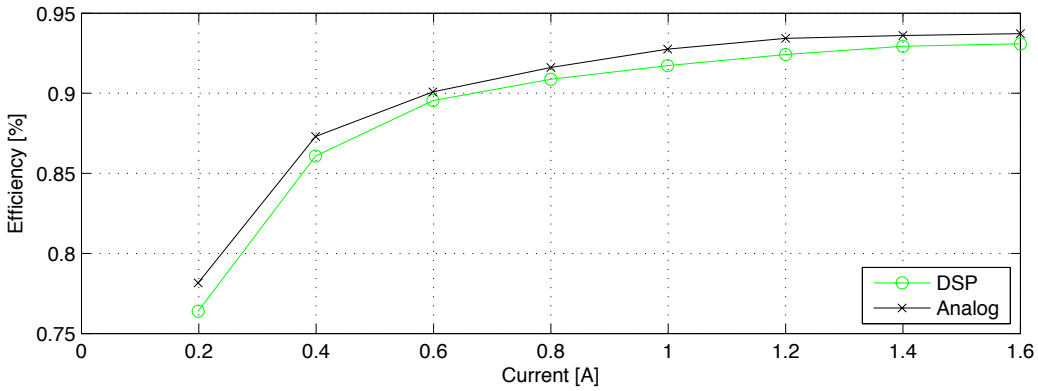

Figure 42 – Measured efficiency of both analog and digitally controlled converter.

The power consumption of the processor increase with the clock frequency and the time it takes for the code to be executed. At a clock frequency of 150 MHz the processor power consumption is typical around 850 mW [**8**]**.** For the gate driver the power consumption increase with increased switching frequency and this is due to that each switching occasion requires a small charge. For the measurement circuits, the power consumption is almost constant. The variation of load does not affect the power consumption of the processor or the measurements circuits. However due to the power consumption of the DSP is higher than the analog controller the total efficiency is lower for the digitally controlled converter. This is expected since the converters are the same and the variations are due to the losses associated with the controller and surrounding circuits.

Since the converter always operates in CCM a current is always present in one of the transistors and in the inductor. This results in higher losses compared to a converter that operates in DCM during light loads.

4.3.6. Noise

Due to the switching action in the converter a lot of noise is generated. This noise spreads to all other circuits and especially affects the measurement circuits. To handle this the driver of the MOSFETs was put as close as possible to the MOSFETs and the driver was shielded. The tighter design and the shielding reduce the noise but it is still present. Due to that this project uses an existing converter it is hard to keep the design tight. All measurements circuits are bandwidth limited to filter out some of the noise although this can potentially affect the performance of controller. The time the measurements are sampled is also of importance since the switching instants should be avoided. The switch time can also be changed to reduce the noise but with the disadvantage of decrease in the efficiency. The noise should be reduced as much a possible since it reduces the overall performance of the DC/DC converter.

5. Conclusion

During this master thesis an analog controlled buck converter has been modified to use a digital controller with great success. The results show that a digitally controlled converter, with the use of more sophisticated control methods, can obtain a more uniform input current than an analog controller. Due to the great flexibility of the processor the software can easily be modified to change the operation. The controller can be optimized to have fast response, low overshoot, voltage accuracy etc. The type of control structure can freely be chosen, however the area where most can be done is the surrounding features i.e. protective functions, voltage shaping, constant power etc.

Due to the high switching frequency, 500 kHz, of the buck converter only one converter could be controlled with the digital controller chosen. This leads to that other control strategies and methods, as discussed in Chapter 5.1, could be chosen in order to control two or more converters.

As seen in the results chapter, the regulation speed of analog and digital controller is similar. The digitally controlled converter is able to regulate the voltage to the reference and handle the load variations satisfactorily. When the active load step control is activated in the digital controller the RMS currents are decreased from 0.141 A to 0.087 A and from 0.248 A to 0.217 A with and without the external output filter respectively. By combining an external filter with active control during load step the best performance i.e. an almost a constant current can be achieved.

The interface board, which is built separated from the processor and the converter, shows pleasant performance for both the input and output measurements and for the driver circuit. As for all switched mode power supplies, noise and interference is a problem. The layout of components is one of the most important aspects of limiting this noise. A second strategy is to reduce the effect of the noise on circuitry by adding filters. The filters used for the measured signals perform satisfactorily and are vital for signal quality.

Modeling of the converter is an effective tool in order to generate the control parameters used in the digital controller. However, the control parameters obtained have to be tuned in order to achieve optimal performance due to inaccuracies in estimates of component values and signal contamination.

5.1.Future work

Even if the DC/DC converter if functional, some things can be improved. The lack of time in the processor limits the number of converters that can be controlled and also the number of auxiliary functions that can be implemented. In order to save processing time, optimization of the program code can be performed. This is preferably done using assembly code. Another way of increasing the number of converters that can be controlled is by using digital controller ICs responsible for the voltage regulation. The processor is then only programmed to take care of active control during load step, monitoring and protective features. An example of this kind of circuitry is the UCD9248 [**10**]. A system with this setup will be a bit more complex and include more communication.

The noise from the switching is hard to keep out from the measurements. Efforts on filtering the noise in the feedback signals of the system have been, but due to that noise are coming from different directions this is hard. The layout of the components and the connections need to be redesigned to minimize the interference. Also the separation between switching and the measurement circuitry could be improved.

The resistive shunt used in the current measurement could be replaced with an inductive current sensor. This could be done to reduce the losses and to insulate the measurement from the output to improve the rejection of interference.

References

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Appendix

A. Program Code

Main

```
//###########################################################################
//
// FILE:            Converter_Control.c
//
// TITLE:           Converter Control
//
//###########################################################################

#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File
#include "DSP2833x_EPwm_defines.h"                  // useful defines for initialization
#include "Converter_PWM.h"
#include "Converter_ADC.h"

interrupt void MainISR(); // Define interrupt rutine

// Initialisation
void InitAdc();
void InitSysCtrl();
void InitPieVectTable();


// Declaration of functions
//---------------------------------------------------------
struct Converter_PWM Converter_pwm = Converter_PWM_DEFAULT;
//---------------------------------------------------------

////////////////////////////////
//////// Variables ////////////
Uint32 count=0;

////////Voltages, Current and Temperature///
float Vout=0.0,Vin=0.0,Iout=0.0, Temperature=0.0;

/////PWM update Variables//////////
Uint16 pwm_period=300;
Uint16 DutyFineLR=0;
Uint16 DutyFineHR=0;
float DutyFineFrac=0.0;
Uint16 MEP_ScaleFactor=37;
Uint16 PWM_polarity=2;

/////Control Parameters////////////
//float d1=0.2564,d2=0.7431,e0=1.04301,e1=-2.01699,e2=0.9762;          // From MatLab
float d1=0.2573,d2=0.7432,e0=1.0441,e1=-2.0168,e2=0.9762;            // Tuned
float Duty=0.0,Dutyn_1=0.0,Dutyn_2=0.0;
float Error=0.0,Errorn_1=0.0,Errorn_2=0.0;
//   do not increase e0,1,2 with more then 0.0001 when tuning

/////Smart Control Variables////////
float VI_down=0.0027,VI_up=0.00023;

/////Limits & References////////////
float Vref=0,Vref_normal_op=32,Vref_Softstart=0;
float Vin_limit=50,Vout_max=35,Iout_max=1.8,Iout_load=1;

//////////Flags//////////////////
Uint16 Softstart=1;
Uint16 Normal_op=0;
Uint16 once=0;
```

```
Uint16 Start=0;
Uint16 load_step=0;
Uint16 Iout_compare=0;
Uint16 update=1;
////////////////////////////////
/////////END OF VARIABLES//////////

void main(){

                InitSysCtrl();
                InitPieVectTable();//Create a table of ISR address

                EALLOW;
                                PieVectTable.SEQ1INT=&MainISR;
                EDIS;
                PieCtrlRegs.PIEIER1.bit.INTx1=1;//Enable the ADC interrupt in PIE level
                IER |=M_INT1;//Enable the ADC interrupt in CPU level
                EDIS;
                EALLOW;
                  GpioCtrlRegs.GPBMUX1.bit.GPIO34 = 0;                  // Enable GPIO34
                  GpioCtrlRegs.GPBDIR.bit.GPIO34 = 1;                   // GPIO34 = output
                  GpioCtrlRegs.GPBMUX1.bit.GPIO32 = 0;                  // Enable GPIO32
                  GpioCtrlRegs.GPBDIR.bit.GPIO32 = 1;                   // GPIO32 = output

                  GpioCtrlRegs.GPCPUD.bit.GPIO86 = 1;  // Disable=1/ Enable=0 pullup on GPIO86
                  GpioCtrlRegs.GPCMUX2.bit.GPIO86 = 0; // GPIO86 = GPIO86
                  GpioCtrlRegs.GPCDIR.bit.GPIO86 = 0;  // GPIO86 = input
                EDIS;
                // Initialize ADC and PWM
                INITIAL_PWM(pwm_period);
                InitAdc();
                Settings_ADC();

                EINT;
                ERTM;

                // Endless Loop
                while(update==1){
                                // Read ADC register
                                Vin=(AdcMirror.ADCRESULT0*0.01685);
                                Temperature=(AdcMirror.ADCRESULT1*0.07324-50.0);

                                ////////////////////SoftStart/////////////////////////////////////
                                if(Softstart==1 && Vin>=Vin_limit && once==1 && Start==1){
                                   EPwm1Regs.DBCTL.bit.POLSEL=2;
                                                Vref_Softstart=Vref_Softstart+0.0001;
                                                Vref=Vref_Softstart;
                                                once=0;

                                                if(Vref_Softstart>=Vref_normal_op){
                                                                Softstart=0;
                                                                Vref_Softstart=0;
                                                                Vref=Vref_normal_op;
                                                }
                                }
                                ////////////////////Input voltage limit////////////////////////////////
                                if(Vin<Vin_limit){
                                                Vref=0;
                                                Duty=0;
                                                Softstart=1;
                                                Vref_Softstart=0;
                                                Start=0;
                                }
                                ////////////////////// Turn off and init Softstart mode//////////////////////
                                if(Start==0 && once==1){
                                                Vref=0;
```

```
                                        Softstart=1;
                                        Vref_Softstart=0;
                                }
                                ////////////Blink the red LED to see if the DSP is running//////////////////
                                count++;
                                  if(count==100000){

                                        GpioDataRegs.GPBTOGGLE.bit.GPIO34 = 1;
                                        count=0;
                                  }
                                ////////////////////////////////////////////////////////////////////////////
                        }
}
//////// Start of Interrupt ////////////////////////////////
interrupt void MainISR(){

                                once=1; // Do operation in main only once per interrupt

//Conversion of ADC-channels and conversion from bits values to voltages
                                Vout=(AdcMirror.ADCRESULT2*0.01191);
                                Iout=(AdcMirror.ADCRESULT3*0.0004483);

////////////////Comparator////////////////////////
                                Iout_compare=GpioDataRegs.GPCDAT.bit.GPIO86;

                                if(Iout_compare==0){
                                        GpioDataRegs.GPBSET.bit.GPIO32 = 1; // Turn on GPIO32
                                                }
                                if(Iout_compare==1){
                                        GpioDataRegs.GPBCLEAR.bit.GPIO32 = 1; // Turn off GPIO32
                                                                                                }

////////////////////////////////////////////////

////////////SMART CONTROL, during load step///////
                                if(Iout>=Iout_load){
                                        Vref=Vref-VI_down;
                                        load_step=1;
                                }

                                if(Iout<=Iout_load && load_step==1){
                                        Vref=Vref+VI_up;
                                }

                                if(load_step==1 && Vref>=Vref_normal_op){
                                        Vref=Vref_normal_op;
                                        load_step=0;
                                }
////////////////////////////////////////////

/////////Difference Equation/////////////////
        Errorn_2=Errorn_1;
        Errorn_1=Error;

        Error=Vref-Vout;

        Dutyn_2=Dutyn_1;
        Dutyn_1=Duty;
        Duty=d1*Dutyn_1+d2*Dutyn_2+e0*Error+e1*Errorn_1+e2*Errorn_2;

/////////Limit Duty to max 0.9//////////////
        if(Duty>0.9){
                        Duty=0.9;
        }

/////Voltage and Current Protection
```

```
    if(Start==0 || Vout>Vout_max || Iout>Iout_max){
                    Duty=0;
                    Start=0;
      EPwm1Regs.DBCTL.bit.POLSEL=0; // Sets PWM1A and PWM1B in phase to prevent current through MOSFETs at shutdown
                                    }

    //Duty=0.5;

//////////////////PWM Update////////////////////////
// Call the PWM-function with the updated duty cycle //
                     Converter_pwm.Duty=Duty;
                     Converter_PWM_OUTPUT(Converter_pwm);

 //***************************************************************************
 //***************************************************************************

 // Reinitialize for next ADC sequence
   AdcRegs.ADCTRL2.bit.RST_SEQ1 = 0x1;  // 1 = Immediately reset sequencer to state CONV00
   AdcRegs.ADCST.bit.INT_SEQ1_CLR=1;  //Writing a 1 to this bit clears the SEQ1 interrupt flag bit, INT_SEQ1.
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}
```

PWM

```
#ifndef Converter_PWM_H_
#define Converter_PWM_H_

#include "DSP28x_Project.h"


struct Converter_PWM
{
                    float Duty;
                    float Duty_PWM;
                    float DutyFineHR;
                    float PWM_dutyHR;
                    Uint16 PWM_dutyLR;
                    float DutyFineFrac;
                    float pwm_period;
                    Uint16 MEP_ScaleFactor;
};

#define Converter_PWM_DEFAULT \
{\
                    0.0,\
                    0.0,\
                    0.0,\
                    0.0,\
                    0.0,\
                    0.0,\
                    300,\
                    37\
}

#define INITIAL_PWM(period)\
EALLOW;\
GpioCtrlRegs.GPAMUX1.bit.GPIO0=1;\
GpioCtrlRegs.GPAMUX1.bit.GPIO1=1;\
EDIS;\
EPwm1Regs.TBCTL.bit.CLKDIV=0;                   /*Time-base Clock Prescale Bits*/\
EPwm1Regs.TBCTL.bit.HSPCLKDIV=0;                /*High Speed Time-base Clock Prescale Bits*/\
EPwm1Regs.TBCTL.bit.CTRMODE=0;                                  /*Counter Mode. 0 = Up-count mode*/\
EPwm1Regs.TBPHS.half.TBPHS=0;                                   /*These bits set time-base counter phase of the
selected ePWM*/\
EPwm1Regs.TBCTL.bit.PHSEN=0;                    /*Counter Register Load From Phase Register Enable*/\
EPwm1Regs.TBCTL.bit.PRDLD=0;                    /*Active Period Register Load From Shadow Register Select. 0 = The
period register (TBPRD) is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero.*/\
EPwm1Regs.TBCTL.bit.SYNCOSEL=1;                                 /*Synchronization Output Select. These bits select the
source of the EPWMxSYNCO signal. 1 = CTR = zero: Time-base counter equal to zero (TBCTR = 0x0000)*/\
EPwm1Regs.CMPCTL.bit.SHDWAMODE=0;               /*Counter-compare A (CMPA) Register Operating Mode. 0 = Shadow
mode. Operates as a double buffer. All writes via the CPU access the shadow register.*/\
EPwm1Regs.CMPCTL.bit.SHDWBMODE=0;               /*Counter-compare B (CMPB) Register Operating Mode 0 = Shadow
mode. Operates as a double buffer. All writes via the CPU access the shadow register.*/\
```

```
EPwm1Regs.CMPCTL.bit.LOADAMODE=0;          /*Active Counter-Compare A (CMPA) Load From Shadow Select Mode. This bit has no effect in immediate mode (CMPCTL[SHDWAMODE] = 1). 0 = Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)*/\
EPwm1Regs.CMPCTL.bit.LOADBMODE=0;          /*Active Counter-Compare B (CMPB) Load From Shadow Select Mode. This bit has no effect in immediate mode (CMPCTL[SHDWBMODE] = 1). 0 = Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)*/\
EPwm1Regs.AQCTLA.bit.CAU=2;                /*Action when the counter equals the active CMPA register and the counter is incrementing. 2 = Set: force EPWMxA output high.*/\
EPwm1Regs.AQCTLA.bit.CAD=1;                /*Action when the counter equals the active CMPA register and the counter is decrementing. 1 = Clear: force EPWMxA output low.*/\
EPwm1Regs.DBCTL.bit.OUT_MODE=3;            /*Dead-band Output Mode Control. 3 = Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by DBCTL[IN_MODE].*/\
EPwm1Regs.DBCTL.bit.POLSEL=2;              /*Polarity Select Control. 2 = Active high complementary (AHC). EPWMxB is inverted.*/\
EPwm1Regs.DBCTL.bit.IN_MODE=0;             /*Dead Band Input Mode Control. 0 = EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.*/\
EPwm1Regs.DBFED=10;                        /*Dead-Band Delay. 10 = 0.1us*/\
EPwm1Regs.DBRED=10;                        /*Dead-Band Delay. 10 = 0.1us*/\
EPwm1Regs.ETSEL.bit.SOCAEN=1;              /*Enable the ADC Start of Conversion A (EPWMxSOCA) Pulse. 1        = Enable EPWMxSOCA pulse.*/\
EPwm1Regs.ETSEL.bit.SOCASEL=1;             /*EPWMxSOCA Selection Options. These bits determine when a EPWMxSOCA pulse will be generated. 1 = Enable event time-base counter equal to zero. (TBCTR = 0x0000)*/\
EPwm1Regs.ETPS.bit.SOCAPRD=1;              /*ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Period Select. 1 = Generate the EPWMxSOCA pulse on the first event: ETPS[SOCACNT] = 0,1*/\
EPwm1Regs.TBPRD = period-1;                /*Set Period. 300 - 1 = 500 kHz*/\
EPwm1Regs.CMPA.half.CMPA = 0;              /*Set 0% fixed duty EPWM1A*/\
EPwm1Regs.CMPA.half.CMPAHR = (1 << 8);     /*These 8-bits contain the high-resolution portion (least significant 8-bits) of the counter-compare A value. CMPA:CMPAHR can be accessed in a single 32-bit read/write. Shadowing is enabled and disabled by the CMPCTL[SHDWAMODE] bit as described for the CMPA register.*/\
EPwm1Regs.CMPB = 0;                        /*Set 0% fixed duty EPWM1B*/\
EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;         /*Action when counter equals zero, EPWM1A.*/\
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;/*Action when the counter equals the period, EPWM1A.*/\
EPwm1Regs.AQCTLB.bit.ZRO = AQ_SET;         /*Action when counter equals zero, EPWM1B.*/\
EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;/*Action when the counter equals the period, EPWM1B.*/\
EALLOW;\
EPwm1Regs.HRCNFG.all = 0x0;                /*Clear all bits first*/\
EPwm1Regs.HRCNFG.bit.EDGMODE = HR_FEP;     /*Edge Mode Bits: Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: HR_FEP = MEP control of falling edge*/\
EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;     /*Control Mode Bits: Selects the register (CMP or TBPHS) that controls the MEP: HR_CMP = CMPAHR(8) Register controls the edge position ( i.e., this is duty control mode). (default on reset)*/\
EPwm1Regs.HRCNFG.bit.HRLOAD  = HR_CTR_ZERO;/*Shadow mode bit: Selects the time event that loads the CMPAHR shadow value into the active register: 0 = CTR = zero (counter equal zero)*/\
EDIS;

#define Converter_PWM_OUTPUT(p) \
                                    DutyFineLR=p.Duty*pwm_period;\
                                    DutyFineFrac=p.Duty*pwm_period-DutyFineLR;\
                                    DutyFineHR=(DutyFineFrac*MEP_ScaleFactor+1.5)*256;\
                                    EPwm1Regs.CMPA.half.CMPAHR = DutyFineHR;\
                                    EPwm1Regs.CMPA.half.CMPA = DutyFineLR;
#endif /*Converter_PWM_H_*/
```

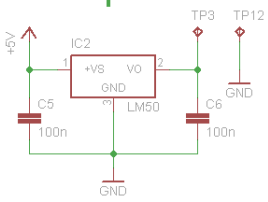
ADC

```
#ifndef CONVERTER_ADC_H_
#define CONVERTER_ADC_H_

#define Settings_ADC()\
                EALLOW;\
                AdcRegs.ADCTRL1.bit.ACQ_PS = 0;\
                AdcRegs.ADCTRL1.bit.CPS = 0;\
                AdcRegs.ADCTRL3.bit.ADCCLKPS =  1;\
                AdcRegs.ADCTRL1.bit.SEQ_CASC = 0;      /*0x0 Dual Sequencer Mode, 0x1 Cascaded Mode*/\
                AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1=1;  /*ADC triggered by PWM*/\
                AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 0x1;          /*enable the interrupt in cascaded mode*/\
                AdcRegs.ADCTRL3.bit.SMODE_SEL = 0x1;     /*Simultaneous sampling*/\
                AdcRegs.ADCTRL2.bit.RST_SEQ1 = 0x1;                /*reset the sequence*/\
                AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 1;\
```

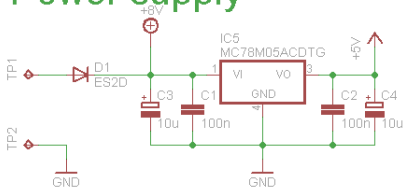
```
                AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 1;            /* ChSelect: CONV00: First Conversion ADC A1->
Vin; ADC B1-> Temp */\
                AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0;            /* ChSelect: CONV01: Second Conversion ADC A0->
Vout; ADC B0-> Iout */\
                EDIS;

#endif /* CONVERTER_ADC_H_ */
```

B. Circuit Schematics

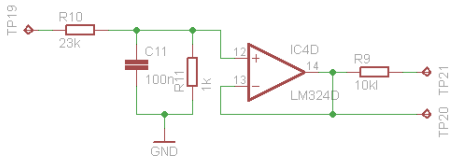
Temp meas.



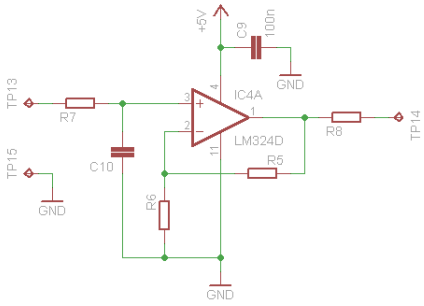
Power supply



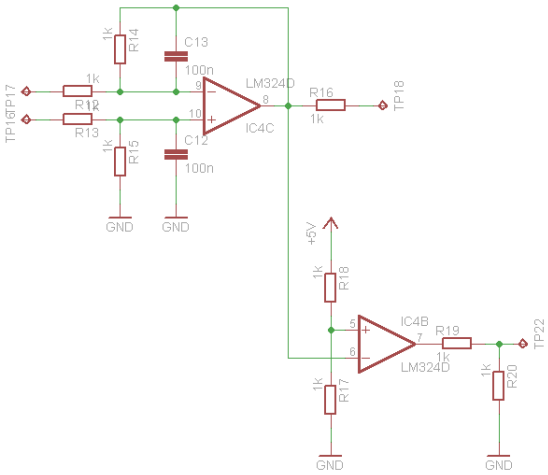
Vin meas.



Vout meas.



Currnent meas. & Current comp.



MOSFET driver