Thesis for The Degree of Licentiate of Engineering

Theory and Design of Wideband Doherty Power Amplifiers

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Göteborg, Sweden, 2012

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Abstract

The Doherty power amplifier (DPA) is one of the most popular power amplifier architectures for obtaining high average efficiency for modern communication signals with high peak-to-average power ratios (PAPR). However, the DPA suffers from often having narrowband performance which limits its capabilities in wideband and/or multi-standard microwave and radio frequency applications.

In this thesis, the theoretical and practical bandwidth limitations of the DPA are examined and it is demonstrated, by theory and measurements, how to design high performance and wideband DPAs.

A Tee-line network of transmission lines is presented that enables simple design of Doherty combining networks in many situations where traditional approaches would fail. The utility of the Tee-line network is demonstrated by implementation in a 7-8 GHz gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) DPA. Continuous wave measurements showed a power added efficiency (PAE) larger than 30 % at 9 dB output power back-off across a 6.7-7.8 GHz frequency range. The maximum output power was maintained within 35 ± 0.5 dBm from 6.6 to 8.5 GHz. Linearized modulated measurements, employing a signal with 7.8 dB (PAPR), reported average PAE larger than 35 %, with an average output power of 27.5 ± 0.2 dBm and an adjacent channel power ratio (ACPR) less than -45 dBc, across a 6.8-8.5 GHz frequency range. The results demonstrates state-of-the art performance both in terms of PAE and bandwidth.

To extend the inherent bandwidth of the DPAs a new type of power amplifier, based on the DPA topology, is presented. It is theoretically shown that the proposed amplifier can simultaneously provide high efficiency at full output power and at power back-off, as well as reconfiguration of the efficiency in power back-off without the need of tunable elements. The theoretical findings were confirmed by the fabrication and measurements of a demonstrator circuit. Measurements reported higher than 48 % drain efficiency at both full output power and at power back-off from 1.5-2.4 GHz, thereby demonstrating a unique combination of high fractional bandwidth and high back-off efficiency. The reported fractional bandwidth that was simultaneously achieved at full output power and at 6 dB output power back-off is to the author's knowledge larger than what has been reported for any power amplifier architecture.

Keywords: Broadband amplifiers, Doherty, gallium nitride, GaN, high efficiency, microwave, MMIC, power amplifier, wideband

List of Publications

Appended Publications

This thesis is based on work contained in the following papers:

[A] D. Gustafsson, J. Chani, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, "A Wideband and Compact GaN MMIC Doherty Amplifier for Microwave Link Applications," submitted to *IEEE Transactions on Microwave Theory and Techniques*, May 2012.

[B] D. Gustafsson, C. M. Andersson, and C. Fager, "Theory and Design of a Novel Wideband and Reconfigurable High Average Efficiency Power Amplifier," manuscript, May 2012.

Other Publications

The following paper has been accepted for publication but is not included in the thesis. The content partially overlaps with the appended papers or is out of the scope of this thesis.

[a] D. Gustafsson, C. M. Andersson, and C. Fager, "A Novel Wideband and Reconfigurable High Average Efficiency Power Amplifier," to be presented at the *IEEE MTT-S International Microwave Symposium*, 2012.

Contents

Chapter 1

Introduction

In 2011, the global mobile data traffic more than doubled for the fourth year in a row, showing a 2.3-fold growth, and a 18-fold growth from the year 2011 to 2016 is predicted, Fig. 1.1, [1].

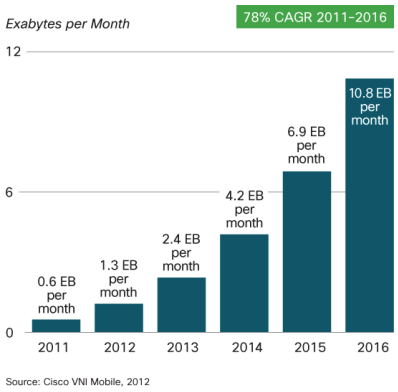


Figure 1.1: Projection of the global mobile data traffic [1].

To cope with the exploding demand for high speed wireless access, much focus is today spent on shrinking cell sizes in user dense areas [2]. To make small cell sizes a realizable investment it is of great importance that microwave transmitters, which are key building blocks of any base station and radio link equipment, can be produced and operated with low complexity and cost.

The power consumption of a microwave transmitter not only constitutes a large part of the overall mobile network operational cost but also increases the system complexity, weight and cost since active cooling equipment often is required to manage with the dissipated heat [3]. Reducing the power consumption is therefore important in order to reduce both complexity and cost of present, and future, microwave transmitters. A reduced power consumption can also, in a larger extent than today, enable passive cooling and local power sources, such as solar cells, thereby greatly reducing cost and complexity, and simplifying installation in rural areas with deficient electrical

power-infrastructure.

The core of a microwave transmitter is the power amplifier (PA), which amplifies the information carrying signal to be transmitted to its required power level. The amplification is done by transforming direct current (DC) power into radio frequency (RF) power and it is of fundamental interest to maximize this conversion efficiency. Older communications standards such as GSM, employ a modulation format with constant amplitude of the transmitted signal and the transmitter PA was therefore optimized for high efficiency at the specific output power level. However, the high order modulation schemes adopted to improve the spectral efficiency in modern communication standards results in signals with large amplitude variations. Modern PAs must therefore provide high efficiency over a large range of output power levels in order to obtain a high average efficiency.

The larger bandwidths needed to support increasing high data rates, in combination with the scarcity of available frequency spectrum, has resulted in a fragmentation of the frequency bands used for wireless communication. In order to keep complexity and cost of wide- and multi-band microwave transmitters low, it is therefore important that modern PAs also can support a diversity of signal bandwidths and frequency bands.

Many different PA-techniques for enhancing the efficiency in back-off has been proposed, such as envelope tracking, dynamic load modulation, RF-pulse width modulation, and Doherty power amplifiers [4–8]. In contrast to the former, the Doherty power amplifier (DPA), originally proposed in [9], has low complexity and do not utilize any external control circuitry. The DPA has therefore attracted lot of attention in the recent time [10–14]. A well known disadvantage of the DPA is, however, its typical bandwidth restrictions which limits its use in wide- or multi-band transmitter applications.

This thesis investigates the theoretical and practical bandwidth limitations of the DPA. In Chapter 2 the theory of the ideal DPA is reviewed and the bandwidth limiting properties are explained and analyzed. Chapter 3 thereafter discusses practical issues when designing DPAs and different output network (NW) topologies are reviewed. Chapter 3 also introduces, based on [Paper A], a new type of output network intended to overcome limitations of well established techniques. Chapter 4 reports the implementation and results of a monolithic microwave integrated circuit (MMIC) DPA, based on [Paper A], employing the output network introduced in Chapter 3.

With respect to the limited bandwidth of the DPA, Chapter 5 reports on a new type of PA, based on [Paper B], with a significantly extended bandwidth. The theory of the proposed amplifier is illustrated and the results are compared to what is reported in Chapter 2. In order to verify the theoretical findings Chapter 5 also reports on the implementation and measurements of a demonstrator circuit presented in [Paper B].

Finally, the thesis is concluded in Chapter 6 and future work is discussed.

Chapter 2

Fundamental Theory

In the pursuit of increasing the bandwidth (BW) of DPAs it is essential to understand the principle of their operation. In [15] a great introduction to DPAs is given, however, the theory only focuses on the specific configuration where the efficiency peaks at 6 dB output power back-off (OPBO), and bandwidth issues are not addressed. Paper [16] is one of few papers where an analysis of the DPA bandwidth limitations is presented. Unfortunately, due to the limited length of the paper, the analysis is only brief and, as in [15], it only focuses on the DPA configuration that yields peak efficiency at 6 dB OPBO.

The purpose of this chapter is therefore to provide a more complete theory including both different configurations of the DPA as well as its frequency response. In the first section a simple and straight forward theory for describing the DPA at the center frequency is presented and it is demonstrated that the efficiency behavior in back-off is a design parameter that determines how to chose the load impedance and driving conditions. In the the second section, the analysis is extended to also include the frequency response and it is demonstrated how the DPA-architecture limits the efficiency bandwidth in OPBO. The theory will remain very idealized though out this entire chapter. Effects from using peak amplifier class-C bias, non-ideal harmonic terminations, and limitations imposed by the input network will not be addressed. The theory to be presented will assume that the reader has a basic knowledge of power amplifier theory, if the reader wishes to learn more about PA-theory, Cripps book [15] is strongly recommended.

2.1 Center frequency analysis

Fig. 2.1 shows the basic configuration of the DPA, consisting of the main and the peak amplifier, combined via a $\lambda/4$-transmission line impedance inverter with a characteristic impedance Z_T at the output of the main amplifier, and connected to a load Z_L [17]. The input consists of a voltage divider and a $\lambda/4$-transmission line at the input of the peak amplifier that serves to give the same phase delay through the two amplifier paths. The analysis of an idealized DPA assumes that the two amplifiers are in perfect class-B operation with all harmonics short circuited. Both amplifiers are also assumed to have the same drain-source bias V_{ds} and zero knee voltage.

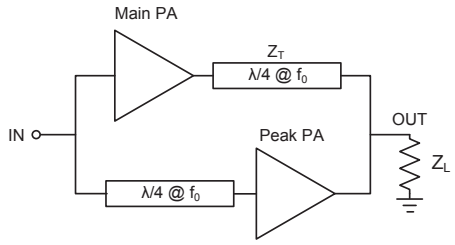


Figure 2.1: Basic configuration of a Doherty power amplifier.

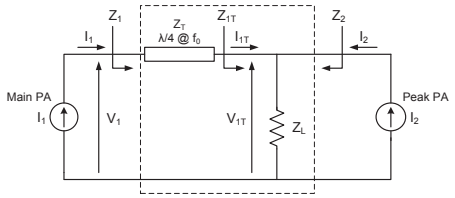


Figure 2.2: Schematic of output network for a Doherty power amplifier. The main and peak amplifiers are represented by the current sources I_1 and I_2, respectively

The output network in the DPA can be schematically illustrated as in Fig. 2.2 where the amplifiers are represented by current sources having fundamental output current phasors I_1 and I_2 that depends on the amplifier voltage drive level $0 \leq \xi \leq 1$ as,

$$I_1 = \xi \frac{I_{max1}}{2}, \tag{2.1}$$

$$I_2 = \begin{cases} 0 & 0 \leq \xi \leq \xi_b \\ \frac{I_{max1}}{2} \frac{\xi - \xi_b}{\xi_b} e^{-j\theta} & \xi_b < \xi \leq 1 \end{cases}, \tag{2.2}$$

where the variable ξ_b is the drive level at the onset of the peak amplifier and I_{max1} is the maximum current of the main amplifier. The phase difference θ is given as $\bar{f}\pi/2$ where $\bar{f} = f/f_0$ is the frequency normalized to the center frequency f_0. The amplitudes of I_1 and I_2 are illustrated versus drive level in Fig. 2.3, and as observed, the value of ξ_b determines the onset, the maximum value, and the increase rate, of the peak amplifier current.

The main and peak amplifier output voltages, V_1 and V_{1T} (Fig. 2.2) are given by,

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \tag{2.3}$$

$$V_{1T} = Z_{21} I_1 + Z_{22} I_2 \tag{2.4}$$

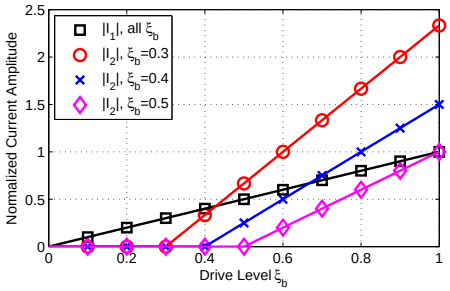


Figure 2.3: The amplitudes of the output currents I_1 and I_2, normalized to $I_{max1}/2$, versus drive level ξ for $\xi_b = 0.3$, 0.4, and 0.5.

where the impedance values are given by the impedance matrix for the dashed two-port in Fig. 2.2 [16]. Fig. 2.2 also shows that the voltage over the load Z_L is equal to the peak amplifier output voltage.

$$\mathbf{Z} = \begin{bmatrix} Z_T \frac{Z_L \cos(\theta) + jZ_T \sin(\theta)}{Z_T \cos(\theta) + jZ_L \sin(\theta)} & \frac{Z_T Z_L}{Z_T \cos(\theta) + jZ_L \sin(\theta)} \\ \frac{Z_T Z_L}{Z_T \cos(\theta) + jZ_L \sin(\theta)} & \frac{Z_T Z_L \cos(\theta)}{Z_T \cos(\theta) + jZ_L \sin(\theta)} \end{bmatrix}. \tag{2.5}$$

The values of Z_T and Z_L that optimizes the output power and efficiency at the center frequency can be derived from (2.3), (2.4) and (2.5). Starting with Z_T, we first observe from (2.4) and (2.5) that the peak amplifier output amplitude becomes $|V_{1T}| = |I_1|Z_T$ at the center frequency. The value of Z_T should therefore be set to maximize the efficiency of the peak amplifier at full output power, which is the same as saying that the amplitude $|V_{1T}|$ should equal the drain-source bias V_{ds} at full output power. Thereby, using the requirement of $|V_{1T}| = V_{ds}$ when $\xi = 1$ and $\theta = \pi/2$ gives,

$$Z_T = \frac{2V_{ds}}{I_{max1}}. \tag{2.6}$$

For drive levels where $I_2 \neq 0$, the expression for V_1 in (2.3) can at the center frequency be written as,

$$V_1 = \frac{I_{max1}}{2} Z_T \xi \left(\frac{Z_T}{Z_L} - \frac{1}{\xi_b} \right) + \frac{I_{max1}}{2} Z_T. \tag{2.7}$$

Thereby, by choosing,

$$Z_L = \xi_b Z_T. \tag{2.8}$$

the first term in (2.7) will equal zero which gives $V_1 = Z_T I_{max1}/2 = V_{ds}$, for all drive levels $\xi \geq \xi_b$. Fig. 2.4 illustrates the normalized main and peak amplifier output voltage amplitudes $|V_1|/V_{ds}$ and $|V_{1T}|/V_{ds}$ versus the drive level for different values of ξ_b when Z_T and Z_L are set according to (2.6) and (2.8) and $\bar{f} = 1$. As expected, the amplitude of the main amplifier output voltage is kept at the bias amplitude all over the high power region, that is when $\xi_b < \xi \leq 1$, thereby ensuring high efficiency operation. The linear relationship between $|V_{1T}|$ and ξ implies that the DPA provides perfectly linear gain. The fact that Z_L is a function of ξ_b implies that ξ_b most often is a fixed value since Z_L

otherwise has to be reconfigurable. This makes it important for the designer to understand at which output powers high efficiency should be prioritized in order to obtain high average efficiency.

When investigating how different modifications of the DPA affects its performance it is important to verify that $|V_1|$ and $|V_{1T}|$ do not exceed the bias level of the main and peak amplifier, respectively, since otherwise this would lead to non physical operation and a incorrect value of the calculated efficiency.

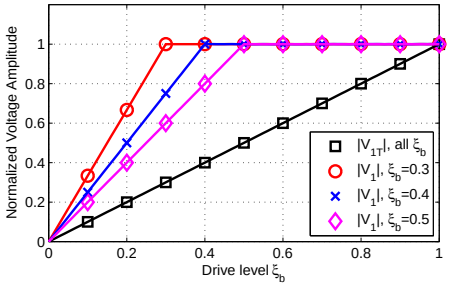


Figure 2.4: The amplitudes of the main and peak amplifier output voltages, V_1 and V_{1T}, normalized to V_{ds}, versus drive level ξ for $\xi_b = 0.3$, 0.4, and 0.5.

In order to calculate the efficiency of the amplifier, the output power and DC-power consumption are first identified to [15],

$$P_{out} = \frac{|V_{1T}|^2}{2Z_L} = \frac{Z_T|I_1|^2}{2\xi_b}, \tag{2.9}$$

$$P_{DC} = \frac{2V_{ds}\left(|I_1| + |I_2|\right)}{\pi}. \tag{2.10}$$

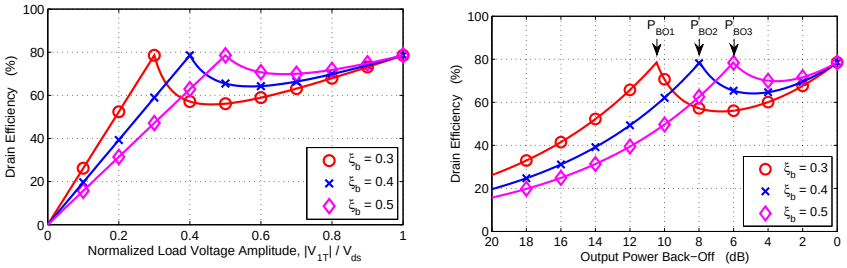
The drain efficiency (η) is thereafter given by,

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\pi R_{opt}|I_1|^2}{4V_{ds}\xi_b\left(|I_1| + |I_2|\right)}. \tag{2.11}$$

The result is illustrated in Fig. 2.5 where the drain efficiency is plotted versus (a) the normalized load voltage $|V_{1T}|/V_{ds}$, and (b) versus OPBO, for different settings of ξ_b. A smaller value of ξ_b gives a higher efficiency in back-off with a deeper efficiency-dip between the two efficiency peaks. The OPBO-level where the efficiency peaks, herein referred to P_{BO}, depends on ξ_b as $P_{BO} = -20\log(\xi_b)$, and is indicated in Fig. 2.5 for reference.

The theory presented in this section has illustrated how a simple combination of two amplifiers, together with correct driving conditions and load impedances, results in very good efficiency performance while perfect linearity is maintained. It was demonstrated how the value of ξ_b influences the efficiency curves, the driving conditions, and the choice of load impedance.

In the next section the analysis is extended to also include the frequency response of the DPA and it will be shown how the $\lambda/4$-transmission line affects the bandwidth for different values of ξ_b.



(a) (b)

Figure 2.5: The drain efficiency versus (a) normalized load voltage amplitude $|V_{1T}|/V_{ds}$, and (b) output power back-off , for $\xi_b = 0.3$, 0.4, and 0.5. $P_{BO1} = 10.5$ dB, $P_{BO2} = 8$ dB, and $P_{BO3} = 6$ dB, associated with $\xi_b = 0.3$, $\xi_b = 0.4$, $\xi_b = 0.5$, respectively, are indicated in (b)

2.2 Frequency response analysis

Using (2.5), the relation in (2.8), the current relations in (2.1) and (2.2), and the expression for the main and peak amplifier voltages in (2.3) and (2.4), the expression of V_1 and V_{1T} are derived as functions of ξ, ξ_b, and θ,

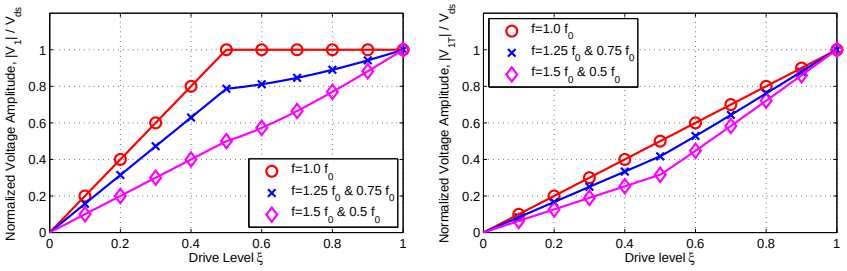
$$V_1 = \begin{cases} V_{ds}\left(\dfrac{\xi\xi_b\cos(\theta) + j\xi\sin(\theta)}{\cos(\theta) + j\xi_b\sin(\theta)}\right) & 0 \le \xi \le \xi_b \\ V_{ds}\left(\dfrac{(\xi\xi_b + \xi - \xi_b)\cos(\theta) + j\xi_b\sin(\theta)}{\cos(\theta) + j\xi_b\sin(\theta)}\right) & \xi_b < \xi \le 1 \end{cases} \tag{2.12}$$

$$V_{1T} = \begin{cases} V_{ds}\left(\dfrac{\xi\xi_b}{\cos(\theta) + j\xi_b\sin(\theta)}\right) & 0 \le \xi \le \xi_b \\ V_{ds}\left(\dfrac{\xi\xi_b + (\xi - \xi_b)\cos(\theta)(\cos(\theta) - j\sin(\theta))}{\cos(\theta) + j\xi_b\sin(\theta)}\right) & \xi_b < \xi \le 1 \end{cases}. \tag{2.13}$$

Fig. 2.6 illustrates how $|V_1|$ and $|V_{1T}|$ from (2.12) and (2.13) depends on drive level at different frequencies when $\xi_b = 0.5$. Fig. 2.6a clearly demonstrates how the large voltage swing on the output of the main amplifier cannot longer be maintained in the high power region when the frequency diverges from the center frequency. In addition, the relationship between $|V_{1T}|$ and ξ, depicted in Fig. 2.6b, is only linear at the center frequency which implies that linear gain cannot be maintained outside the center frequency.

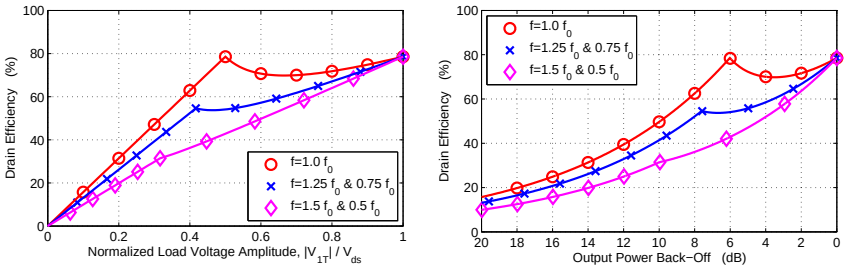
Fig. 2.7 illustrates how the reduced voltage swing on the output of the main amplifier affects the over-all efficiency. As observed, the efficiency in back-off is significantly reduced outside the center frequency. It is important to note, however, that at full output power neither efficiency, nor the gain, are affected by the frequency.

The bandwidth behavior in back-off and full output power can be qualitatively understood by the way Z_{1T} and Z_1 in Fig. 2.2 are related,



(a) (b)

Figure 2.6: The amplitudes of, (a) the main amplifier voltage $|V_1|$, and (b) the peak amplifier voltage $|V_{1T}|$, normalized to V_{ds}, versus drive level ξ for different frequencies.



(a) (b)

Figure 2.7: The drain efficiency versus, (a) normalized load voltage amplitude $|V_{1T}|/V_{ds}$, and (b) output power back-off, for different frequencies.

$$Z_1 = Z_T \frac{Z_{1T} + jZ_T \tan(\theta)}{Z_T + jZ_{1T} \tan(\theta)}. \tag{2.14}$$

At maximum output power, Z_{1T} equals Z_T, and the nominator and denominator in (2.14) becomes equal which makes Z_1, and therefore also the efficiency and gain, independent of frequency. Contrary, at low output powers where $I_2 = 0$, Z_{1T} becomes equal to Z_L, and the frequency response of Z_1 thereby becomes dependent on the ratio Z_T/Z_L.

Fig. 2.8 illustrates how the efficiency at P_{BO} depends on frequency for different settings of ξ_b. As observed the frequency range where high efficiency is obtained in back-off becomes more narrow when ξ_b is decreased. The 1 dB drain efficiency bandwidth ($BW_{\eta-1dB}$), defined as the fractional bandwidth where the drain efficiency is larger than $\max(\eta)10^{(-0.1)}$, for different ξ_b becomes as tabulated in Table 2.1.

The presented analysis has demonstrated the inherent bandwidth limitations of DPA. Fig 2.8 shows how the efficiency bandwidth in OPBO drastically decreases for small values of ξ_b and Table 2.1 showed that $BW_{\eta-1dB}$ becomes as small as 14 % for $\xi_b = 0.3$ ($P_{BO} = 10.5$ dB). The introduced frequency dependence in (2.5) is due to the electrical length of the $\lambda/4$-transmission line

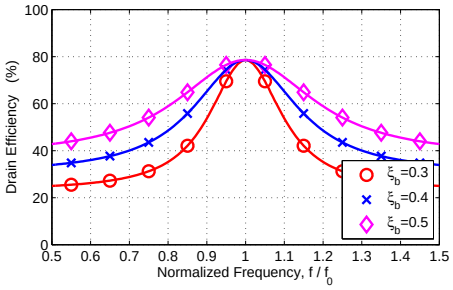


Figure 2.8: The drain efficiency versus frequency at P_{BO} for different values of ξ_b.

Table 2.1: 1 dB efficiency bandwidth

ξ_b	P_{BO}	$BW_{\eta-1dB}$
0.30	10.5 dB	14 %
0.35	9.1 dB	18 %
0.40	8.0 dB	23 %
0.45	6.9 dB	28 %
0.50	6.0 dB	34 %

impedance inverter and its dependence on frequency. It could therefore be argued that another type of impedance inverter with less frequency dependence could increase the theoretical bandwidth of the DPA. However, no such impedance inverter have been described in literature, nor has the the studies preceding this thesis indicated that such impedance inverters can be realized.

Chapter 3

Combining Networks

Fig. 3.1 illustrates a typical equivalent circuit of a high electron mobility transistor (HEMT). In contrast to the assumptions in Chapter 2, there are multiple, both linear and non-linear, elements between the drain terminal and the intrinsic current source. Hence, correct DPA functionality is not obtained by only connecting the drain terminals of the main and peak amplifier transistors with a $\lambda/4$-transmission line.

Seen from the output, the elements in Fig. 3.1 are most often dominated by C_{ds} and C_{gd} and it is therefore standard practice, in PA-theory, to use a simplified transistor model where the output is modeled with an effective capacitance C_{out}, Fig. 3.2 [15, 16, 18, 19]. The network that combines the two transistors must therefore be designed so that it, together with the output capacitances, approximates the behavior of a $\lambda/4$-transmission line impedance inverter, Fig. 3.3.

This chapter addresses how to connect the drain terminals of the main and peak transistors for realization of a practical DPA. Different alternatives are reviewed and their applicability is discussed.

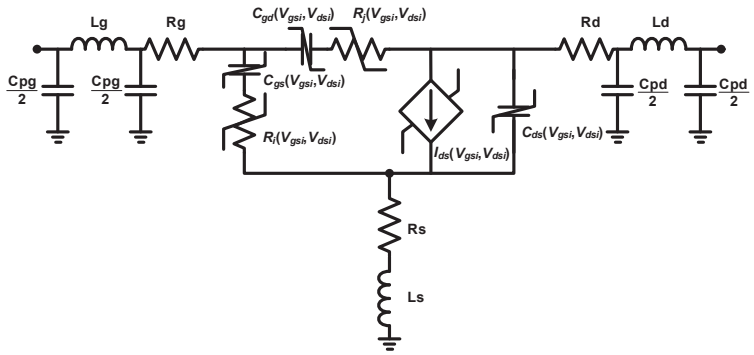


Figure 3.1: Large signal equivalent circuit of a HEMT.

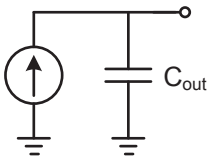


Figure 3.2: Simplified transistor model used for analyzing DPAs.

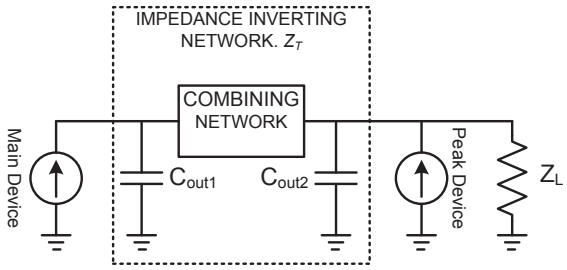


Figure 3.3: Schematic illustrating how the total network connecting the intrinsic current sources must act as an impedance inverter.

3.1 LC-resonant circuits

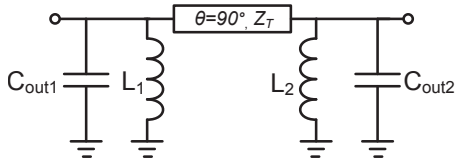


Figure 3.4: Impedance inverting network where the output capacitances are resonated by inductors.

The most straight forward method to design the combining network is to resonate the output capacitances with inductors as illustrated in Fig. 3.4 where the values of L_i (the index i refers to either 1 (main) or 2 (peak)) are,

$$L_i = \frac{1}{\omega_0^2 C_{out,i}}, \tag{3.1}$$

and ω_0 is the center frequency.

The applicability of this combining network depends on the impedance of the transmission line since high value of Z_T in practice can require non-realizable linewidths. For instance; wide bandgap technologies, such as GaN, that utilizes high drain bias voltages can in low and medium power applications require values of Z_T that is larger than 100 Ω. Such high impedance transmission lines many times violates process layout rules if being realized.

The short circuited inductors are often convenient to use for the DC bias feed. However, in implementations where inductors typically have low current handling capabilities, such as MMIC, bias feed through the inductors might not be possible due to high DC-currents.

The bandwidth of the LC-resonant circuits in Fig. 3.4 also affects the bandwidth of the DPA and [16] demonstrated that the LC-resonant circuits severely can reduce the DPA bandwidth.

3.2 Quasi-lumped network

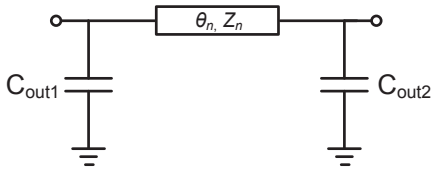


Figure 3.5: Schematic of the quasi-lumped impedance inverting network suggested in [16].

To limit the bandwidth reduction imposed by the LC-resonant circuits, [16] suggested that the output capacitances should be utilized in the impedance inverting network as illustrated in Fig. 3.5. When C_{out1} and C_{out2} are equally large, the length and impedance of the transmission line is given by,

$$\theta_n = \arccos\left(\omega_0 C_{out} Z_T\right), \tag{3.2}$$

$$Z_n = \frac{Z_T}{\sin\left(\theta_n\right)} \tag{3.3}$$

where $\omega_0 C_{out} Z_T < 1$ in order to give real values of θ_n and Z_n.

From (3.3) it can be seen that $Z_n \geq Z_T$ and the method is therefore not suitable for applications where high values of Z_n implies non-realizable linewidths. It should also be noted that the quasi lumped network requires additional bias circuitry which might degrade its performance and complicates the design procedure.

3.3 Pi-network

An impedance inverter can also be obtained by the lumped element network illustrated in Fig. 3.6 where,

$$X_i = \frac{1}{\omega_0 (C_{out,i} - C_T)}, \tag{3.4}$$

$$C_T = \frac{1}{\omega_0 Z_T}, \tag{3.5}$$

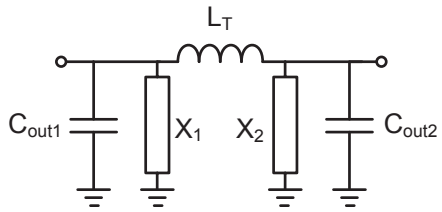


Figure 3.6: Schematic of a lumped element impedance inverting pi-network. The reactances X_1 and X_2 can be both negative and positive depend upon the values of C_{out1} and C_{out2}, respectively, see (3.4).

$$L_T = \frac{Z_T}{\omega_0}, \tag{3.6}$$

Compared to the networks in Section 3.1 and 3.2, the pi-network is not limited by non-realizable linewidths when Z_T is large. However, combinations of ω_0, Z_T and C_{outi} can result in large inductor values that are difficult to realize. In particular, it can be cumbersome to realize large inductor values in MMIC technology due to the often limited current handling capabilities, high loss, and shunt-parasitics associated with spiral inductors. The high inductor losses associated with MMIC implementations were addressed in [18, 20, 21] by implementing them off-chip using bond-wires and slab inductors on a printed circuit board whereas [22] used bond-wires alone for realizing the series inductance L_T.

3.4 Tee-line network

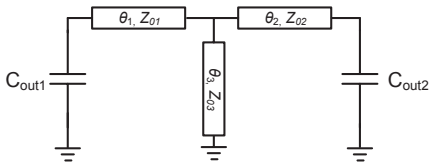
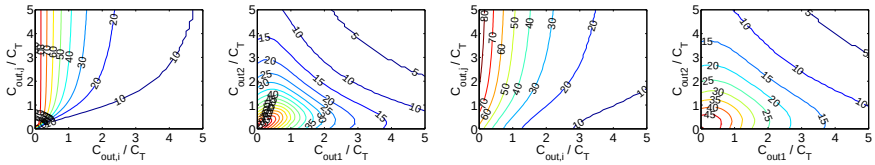


Figure 3.7: Tee-line impedance inverter. The impedances Z_{0i} can be arbitrary chosen whereafter the electrical lengths θ_i can be calculated.

With respect to the previous discussion, a combining network that is not limited by the performance of inductors, or by narrow transmission lines, is desirable. In [Paper A] we therefore proposed a "Tee-line" combining network, depicted in Fig. 3.7, consisting of three transmission lines with the electrical lengths θ_m and characteristics impedances Z_{0m} (the index m represents either one of the three transmission lines). It was shown that each characteristic impedances Z_{0m} can be pre-selected to a convenient value whereafter the electrical lengths are calculated for the given set of C_{out1} and C_{out2}. Fig. 3.8,

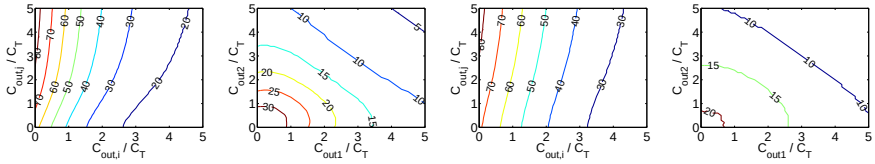


(a) θ_i for the configuration $T_1 = 1$, $T_2 = 1$, $T_3 = 1$.

(b) θ_3 for the configuration $T_1 = 1$, $T_2 = 1$, $T_3 = 1$.

(c) θ_i for the configuration $T_1 = 1.5$, $T_2 = 1.5$, $T_3 = 1.5$.

(d) θ_3 for the configuration $T_1 = 1.5$, $T_2 = 1.5$, $T_3 = 1.5$.



(e) θ_i for the configuration $T_1 = 2$, $T_2 = 2$, $T_3 = 2$.

(f) θ_3 for the configuration $T_1 = 2$, $T_2 = 2$, $T_3 = 2$.

(g) θ_i for the configuration $T_1 = 3$, $T_2 = 3$, $T_3 = 3$.

(h) θ_3 for the configuration $T_1 = 3$, $T_2 = 3$, $T_3 = 3$.

Figure 3.8: The plots shows the how the lengths θ of the transmission lines should be chosen for different capacitance ratios C_{out1}/C_T and C_{out2}/C_T and impedance ratios T_1, T_2 and T_3 in order to make the network in Fig. 3.7 to behave as an impedance inverter. Due to symmetry θ_1 is given by setting $i = 1$, $j = 2$, and θ_2 is given by setting $i = 2$, $j = 1$.

originally presented in [Paper A], shows how the electrical lengths of the transmission lines in Fig. 3.7 depend on the output capacitances for different sets of impedance ratios $T_m = Z_T/Z_{0m}$. The plot axes are normalized to C_T given by (3.5). The implications of Fig. 3.7 is that a Tee-line network with reasonable line lengths can be used as an impedance inverter for a large span of capacitance ratios C_{out1}/C_T and C_{out2}/C_T and impedance ratios T_1, T_2 and T_3 .

The main advantage/feature of the proposed network is that it realizable also for large values of Z_T and its applicability is not affected by the availability and performance of lumped inductors and capacitors. In addition, the network also offers convenient biasing through the short circuited transmission line. The Tee-line network is therefore highly suitable for DPA designs e.g. implemented in GaN MMIC techniques due to the often large values of Z_T and limited current handling capabilities of spiral inductors, as will be demonstrated in the next chapter.

Chapter 4

MMIC Doherty Power Amplifier

To demonstrate the utility of the Tee-line combining network, a Doherty power amplifier with a target frequency band of 7.0-8.0 GHz was designed in the TriQuint 3MI GaN MMIC process [23] and is reported in [Paper A].

This chapter will review some of the design considerations made when designing the MMIC-DPA, and an extended discussion regarding why the Tee-line network is more suitable compared to other topologies, is presented. The results reported in [Paper A] are thereafter revisited and compared to other DPA-MMIC designs published in the literature.

4.1 Design considerations

The selected frequency range of 7.0-8.0 GHz is selected to target microwave link applications for the mobile backhaul system. As in many other applications, microwave links utilizes modulation schemes with peak to averages power ratios (PAPR) in the order of 7-9 dB. To obtain high average efficiency it was therefore decided to implement the design with a value of $\xi_b = 0.33$, giving $P_{BO} = 9.5$ dB, and $Z_T/Z_L = 3$. The total gatewidth of the main amplifier transistor was chosen to 4×100 μm, which in combination with a drain voltage of 20 V implies that $Z_T = 150$ Ω should be chosen for high power utilization of the main amplifier transistor, as well as a convenient value of $Z_L = 50$ Ω.

With $\xi_b = 0.33$, equation (2.2) shows that the peak amplifier must be able to handle twice the current compared to the main amplifier. The size of the peak amplifier transistor was therefore chosen to 10×100 μm. With the given transistor sizes the output capacitances were found to 0.15 pF and 0.44 pF for the main and peak amplifier transistor, respectively.

The widths of the Tee-line transmission lines in Fig. 3.7 were chosen to $w_1 = w_2 = 25$ μm and $w_3 = 40$ μm, giving characteristic impedances of $Z_{01} = Z_{02} = 79$ Ω, $Z_{03} = 69$ Ω. Using the equations derived in [Paper A], the electrical lengths of the transmission lines were thereafter calculated to be $\theta_1 = 52.3°$, $\theta_2 = 18.9°$ and $\theta_3 = 17.0°$.

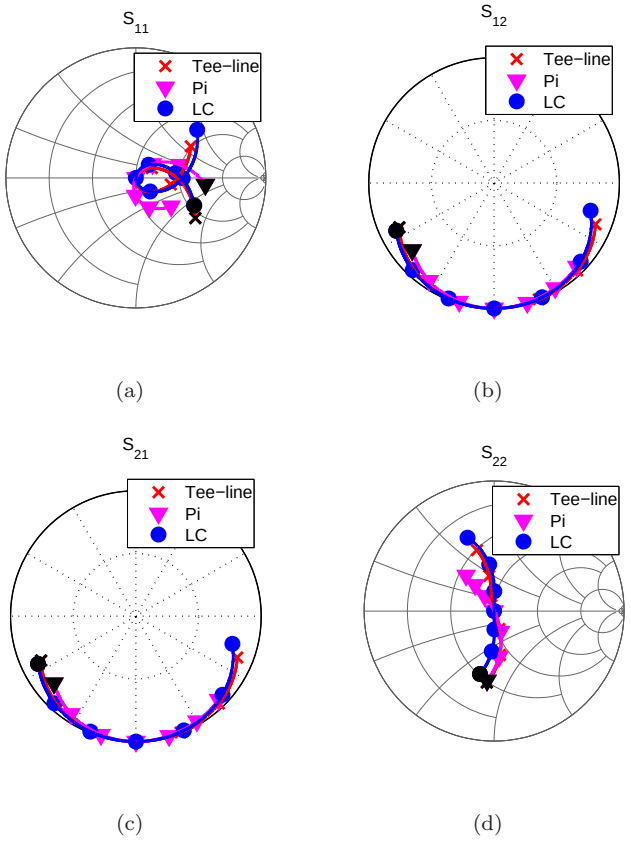


Figure 4.1: S-parameters simulated from 6.0 to 9.0 GHz with a 150 Ω system impedance for the LC-, pi-, and Tee-networks with $C_{out1} = 0.15$ pF, $C_{out2} = 0.44$ pF, and $Z_{01} = Z_{02} = 79\ \Omega$, $Z_{03} = 69\ \Omega$. The marker spacing is 0.5 GHz and the black markers indicates the highest frequency point.

For comparison, the width of a transmission line with characteristic impedance $Z_T = 150\ \Omega$ would be less than 0.5 μm which violates the process layout rules. The LC-resonant and quasi lumped combining networks in Section 3.1 and 3.2 could therefore not be used for the reported design. Simulations indicated a maximum DC-current in the order of 420 mA. Using the pi-network in Section 3.3 therefore requires spiral inductors with very large metal widths ($\approx 80\ \mu$m) to handle the expected DC-currents. Such inductors would consume a very large area and have large parasitic capacitances degrading the performance.

Even though the networks in Sections 3.1-3.3 are unpractical as discussed above, it is still of interest to investigate how their frequency response compare with the Tee-line network for the specific design in this chapter. Ideally, such an analysis should demonstrate how each combining network affects the efficiency of the DPA at different frequencies. However, calculating V_1 and V_{1T} when using the networks in Chapter 3 sometimes results in amplitudes that are larger than the bias level. As discussed in Section 2.2, such a behav-

ior is not physical, and will in practice be prevented by the limitations of the transistor. In an idealized theory it is however not obvious how to impose the voltage restriction in a physical way without losing the clarity of the analysis. The frequency responses of the networks are therefore evaluated by comparing their S-parameters. In general, a less frequency dependent combining network also allows for more wideband DPA-designs.

Fig. 4.1 shows the S-parameters of the networks in Chapter 3 for the design specifications presented above. As observed in the figure, the Tee-line network behaves very similar to the network from Section 3.1 (indicated as LC), whereas the lumped element pi-network is less frequency dependent. This can be interpreted as if the pi-network has the potential to provide more wideband DPAs compared with the Tee-line network. However, when realizing the circuits, the properties of the physical inductors will be less ideal than those for the physical transmission lines. Thus, the S-parameters for a realized pi-network will be more degraded than for a realized Tee-line network, and it therefore not obvious which network that provides the largest bandwidth in practice.

4.2 Circuit realization and results

Fig. 4.2 shows the schematic of the realized output network. Compared to the schematic in Fig. 3.7, only a RF-short capacitor has been added in the realized circuit. The lengths, widths and impedances of TL1, TL2 and TL3 are tabulated in Table 4.1

Fig. 4.3 shows a photo of the realized circuit. A compact layout was emphasized which resulted in a total chip-size of 2.1 × 1.5 mm, small enough to fit in a quad-flat no-leads (QFN) 4x4 package.

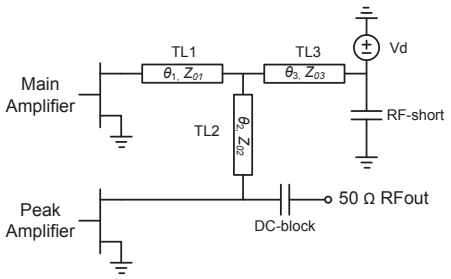


Figure 4.2: Schematic of output network.

Table 4.1: Tee-line Network Parameters

	TL1	TL2	TL3
Length	2800 μm	840 μm	750 μm
Width	25 μm	25 μm	40 μm
Impedance	79 Ω	79 Ω	69 Ω

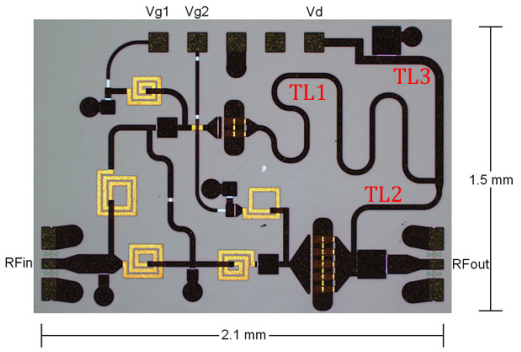


Figure 4.3: Photo of the realized circuit.

4.2.1 CW-Measurements

The results reported in [Paper A] are here summarized in Fig. 4.4. The bias setting used for the reported measurements was $V_{g1} = -3.7$ V, $V_{g2} = -5.4$ V, and $V_d = 20$ V.

Fig. 4.4a demonstrates a well pronounced enhancement of efficiency in back-off and Fig. 4.4b reports a maximum PAE at 9 dB OPBO of 37 % that occurs at 7.1 GHz. The 1 dB efficiency bandwidth, i.e. the bandwidth where the PAE is larger than 29.4 %, is 15 % at 9 dB OPBO. Section 2.2 derived a 1 dB efficiency bandwidth of 18 % at 9.1 OPBO for an ideal DPA with $\xi_b = 0.35$ (Table 2.1). Even though it is difficult to make a fair comparison between the reported 15 %, and the theoretical 18 % bandwidth, the reported bandwidth must still be regarded as an excellent result. Fig. 4.4b also demonstrates that the PAE is less frequency at high output powers which is in good agreement with the theory.

The reported gain in Fig. 4.4c and Fig. 4.4d is larger than 10 dB in the 6.5-7.5 GHz frequency range but decreases at higher frequencies. Fig. 4.4d also shows that the maximum output power is maintained at 35 $\pm$ 0.5 dBm in the 6.6 to 8.5 GHz frequency range.

4.2.2 Linearization

Linearized modulated measurements, employing a vector switched generalized memory polynomial (VS-GMP) model [24], were performed in 100 MHz intervals over a 6.5 to 8.5 GHz frequency range for a 10 MHz QAM signal with 7.8 dB PAPR.

Fig. 4.5 reports the measured average PAE versus frequency at an average output power of 27.5 $\pm$ 0.2 dBm. The figure also includes linearization performance measures such as normalize mean square error (NMSE) and adjacent channel power ratio (ACPR). As noticed, the power amplifier performance is consistent to the results obtained using CW measurements (Fig.4.4) obtaining average PAE larger than 35 % across the 6.8-8.5 GHz frequency range while maintaining NMSE and ACPR better than -35 dBc and -45 dBc, respectively, at all frequencies.

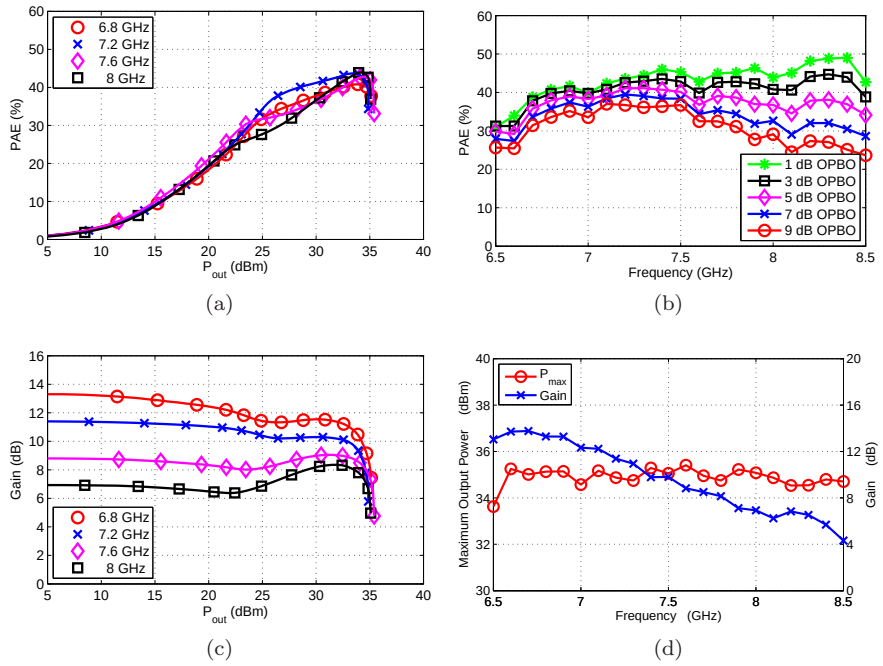


Figure 4.4: Results from CW-measurements of the realized DPA. (a) PAE versus output power, (b) PEA versus frequency at different OPBO-levels relative the maximum output power, (c) gain versus output power, (d) maximum output power and small-signal gain versus frequency.

4.2.3 Discussion

It is of interest to compare the herein reported results, based on [Paper A], with other MMIC-DPA publications in order to verify that the results are competitive. However, when doing so, one should keep in mind that comparing different DPA designs is a cumbersome task due to different implementation techniques, frequencies, modulations schemes, etc.

In [19] a 9.5 GHz GaAs MMIC-DPA was demonstrated with 34 % PAE at 6 dB OPBO and a maximum output power of 29 dBm. Considering the high frequency the results are excellent but no information was given about the bandwidth which indicates non-wideband performance.

If comparing with [18] wherein a GaAs HBT MMIC-DPA is demonstrated with more than 30% average PAE across the 1.6 to 2.1 GHz band, one can conclude that the therein reported fractional bandwidth is larger than what is reported in [Paper A]. However, the design in [18] is implemented at a lower frequency and the inductors in the output network where realized with bond-wires and off-chip components.

[22] presents a 39 dBm GaAs HBT MMIC-DPA, utilizing a bond-wire in the output network, developed for the 728 to 768 MHz band. Despite a factor 10 higher frequency the DPA in [Paper A] provides similar PAE results without the need of bond wire inductances, although at 4 dB lower output

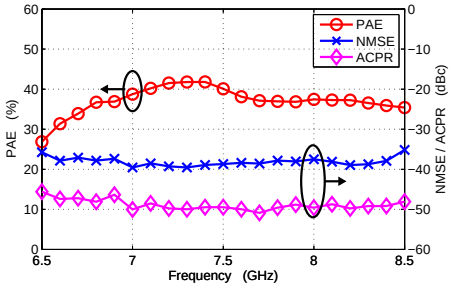


Figure 4.5: Measured average PAE, NMSE, ACPR at an average output power of 27.5 ± 0.2 dBm.

power.

The reported results in [Paper A] thereby verifies the utility of the Tee-line network by demonstrating state of the art performance both in terms of bandwidth and PAE when considering the frequency and chip-size.

Chapter 5

Doherty Power Amplifier with Extended Bandwidth

The theory presented in Chapter 2 revealed two drawbacks of the original Doherty power amplifier; The bandwidth is limited due to the transforming properties of the impedance inverter. And, P_{BO} depends on Z_L which prohibits reconfiguration of P_{BO} unless tunable elements such as varactors are introduced [REF]. These facts limits the potential of designing wideband and multi standard DPAs. In [Paper B] we therefore propose a novel power amplifier based on the DPA architecture in Fig. 2.2, but with a new set of design parameters. It is theoretically demonstrated how the proposed amplifier can provide both significantly larger bandwidth compared to what is reported for the DPA in Chapter 2, as well as simple reconfiguration of P_{BO}. [Paper B] also reports the design and measurements of a demonstrator circuit used for verifying the presented theory.

In the first section of this chapter, the presented theory in [Paper B] will be demonstrated and compared to the results in Chapter 2. The second section will thereafter review the results of the demonstrator circuit.

5.1 Theoretical Performance

5.1.1 Bandwidth

The foundation of the proposed amplifier in [Paper B] is to use the DPA-architecture in Fig. 2.2 but with $Z_T \equiv Z_L$. Thereby, when $I_2 = 0$, Z_{1T} equals Z_L, and Z_1 in equation (2.14) becomes independent of frequency which implies that the also efficiency becomes frequency independent when $I_2 = 0$. In order to obtain proper load modulation under the condition that $Z_T = Z_L$, new bias and driving conditions was derived and are here revisited in Table 5.1.

The expression for k will only assume real values when,

$$\frac{1-\xi_b^2}{1+\xi_b^2} \leq \sin\left(\pi\bar{f}/2\right), \tag{5.1}$$

and the equation in Table. 5.1 will therefore be valid for a limited set of

Table 5.1: Design Papameters

Parameter	Value
V_{ds2}	V_{ds2}
V_{ds1}	$\xi_b V_{ds2}$
Z_T	$2V_{ds2}/I_{max1}$
Z_L	$2V_{ds2}/I_{max1}$
I_1	$\xi I_{max1}/2$
I_2	$\begin{cases} 0, & 0 \le \xi \le \xi_b \\ \frac{k \cdot I_{max1}}{2} e^{-j\theta}, & \xi_b \le \xi \le 1 \end{cases}$
θ	$\arcsin\left(\frac{k\cos(\pi\bar{f}/2)}{2\xi}\right) + \frac{\pi}{2}, \quad \xi_b \le \xi \le 1$
k	$\sqrt{\xi^2 + \xi_b^2 - \sqrt{(\xi^2+\xi_b^2)^2 - \left(\frac{\xi^2-\xi_b^2}{\sin(\pi\bar{f}/2)}\right)^2}}$
$\bar{f}$	f/f_0

frequencies. Insertion of ξ_b-values in (5.1) shows that the valid frequency span for for $\xi_b = 0.5$ and $\xi_b = 0.4$ is $0.41 \le \bar{f} \le 1.59$ and $0.52 \le \bar{f} \le 1.48$, respectively. It is therefore most likely that the frequency will be constrained by other factors before the theoretical limit of k.

The equations in Table. 5.1 were derived under two conditions: First, the amplitude of the load voltage $|V_{1T}|$ was assumed to be proportional to ξ for all frequencies. Secondly, in order to ensure maximum efficiency, the amplitude of the main amplifier output voltage $|V_1|$ was assumed to $|V_1| = V_{ds1}$, for all $\xi \ge \xi_b$ and all frequencies. The main and peak amplifier voltage amplitudes in Fig. 5.1 are therefore valid for all frequencies where k is defined.

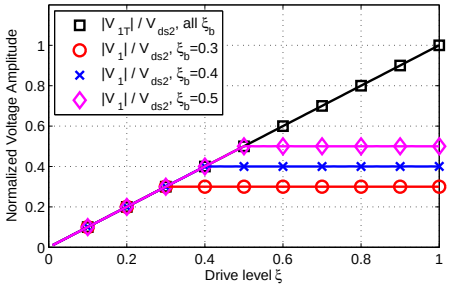
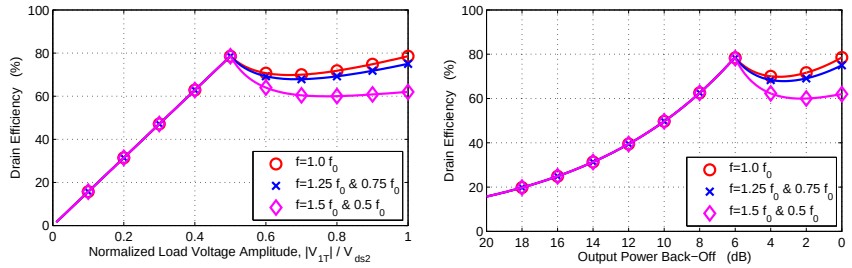


Figure 5.1: The amplitudes of the normalized main and peak amplifier output voltages versus drive level ξ for all frequencies where k is defined.

Fig. 5.2 illustrates the efficiency versus output level for $\xi_b = 0.5$. As observed, the efficiency is independent of frequency when $\xi \le \xi_b$ and has only a weak frequency dependence when $\xi > \xi_b$. When comparing with the same



(a) (b)

Figure 5.2: The drain efficiency versus, (a) normalized load voltage amplitude $|V_{1T}|/V_{ds2}$, and (b) output power back-off, for different frequencies.

Table 5.2: 1 dB efficiency bandwidth

ξ_b	P_{BO}	DPA $BW_{\eta-1dB}$	Proposed PA $BW_{\eta-1dB}$
0.30	10.5 dB	14 %	72 %
0.35	9.1 dB	18 %	80 %
0.40	8.0 dB	23 %	86 %
0.45	6.9 dB	28 %	93 %
0.50	6.0 dB	34 %	99 %

plot for the DPA , Fig. 2.7, it is obvious that the bandwidth of the proposed amplifier is significantly larger.

Fig. 5.3 reports the frequency response of the efficiency at full output power for different settings of ξ_b and should be compared with Fig. 2.8. In Table 5.2 the 1 dB efficiency bandwidth of the proposed amplifier at full output power is compared to the 1 dB efficiency bandwidth of the DPA at P_{BO}. Fig. 5.3 and Table 5.2 clearly manifests the larger bandwidth of the proposed amplifier compared to the DPA.

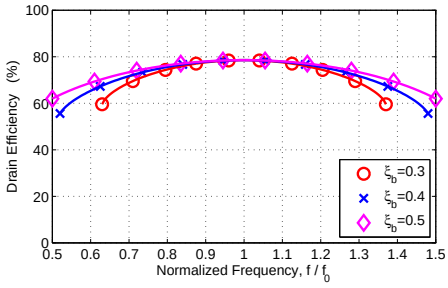
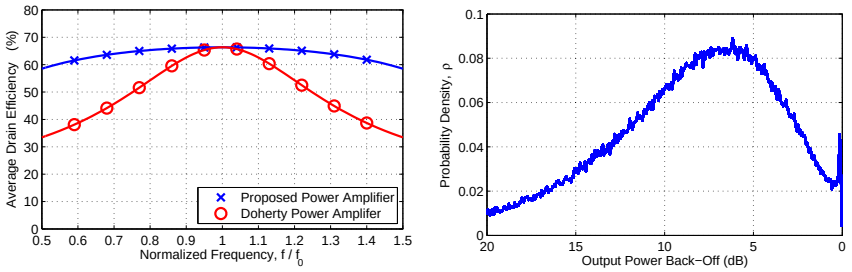


Figure 5.3: The drain efficiency versus frequency when at full output power for different values of ξ_b.

Since the intention of both the DPA and the proposed amplifier is to transmit modulated signals it is of interest to compare their average efficiency when



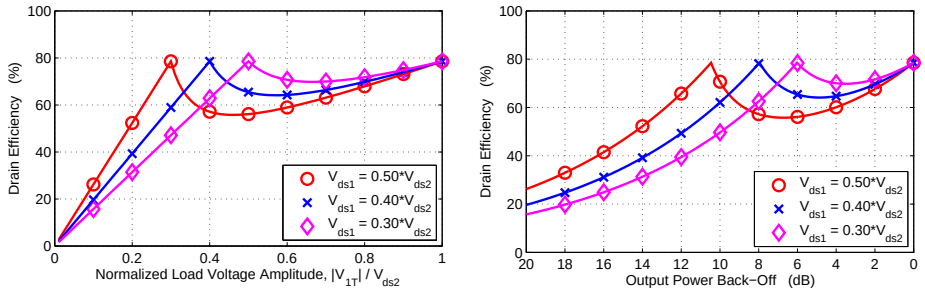
(a) (b)

Figure 5.4: (a) The average drain efficiency versus frequency for the proposed amplifier and the DPA calculated for the signal width the PDF in (b).

transmitting the same signal. Fig. 5.4a therefore illustrates the average efficiency versus frequency for both amplifiers (ξ_b=0.45) when transmitting a signal with 6.6 dB PAPR and a probability density function (PDF) as in Fig. 5.4b. The result again proves the large bandwidth of the proposed amplifier.

5.1.2 Reconfigurability

Table. 5.1 shows that the only design parameters that depends on ξ_b is the main amplifier bias V_{ds1} and the current I_2. This implies that if one has the ability to control the current I_2, e.g. with a dual RF-input configuration [11, 16], the value of ξ_b and P_{BO}, can be reconfigured by changing the main amplifier bias V_{ds1} as illustrated in Fig. 5.5. In addition, Fig. 5.1 shows that the output voltage $|V_{1T}|$, and thereby the output power, not depends on the value of ξ_b. A single amplifier can thereby, as discussed in [Paper B], be reconfigured for optimal performance for a large variety of modulation schemes with maintained large bandwidth and output power.



(a) (b)

Figure 5.5: The drain efficiency versus, (a) normalized load voltage $|V_{1T}|/V_{ds2}$, and (b) output power back-off, at the center frequency. ξ_b is set to 0.5, 0.4 and 0.3 respectively.

5.2 Demonstrator circuit results

To verify the theoretical findings, [Paper B] also presented the design and measurements of a demonstrator circuit, depicted in Fig. 5.6. The design goal was to obtain as wideband performance as possible with a 2.14 GHz center frequency. The amplifier was implemented with dual RF-inputs [11, 16] which allows for proper control of the currents I_1 and I_2 in order to obtain high bandwidth and reconfigurability of ξ_b. The combining network was implemented using the technique described in Section 3.2 and simulations indicated that the combining network allowed for high performance in the 1.7 to 2.6 GHz frequency range.

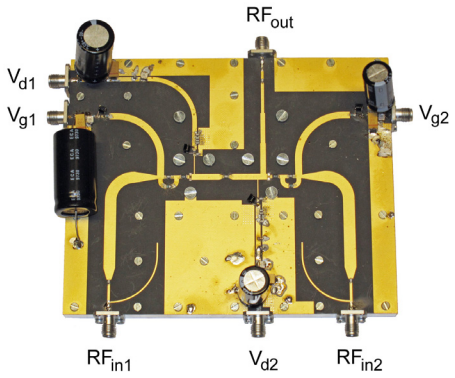


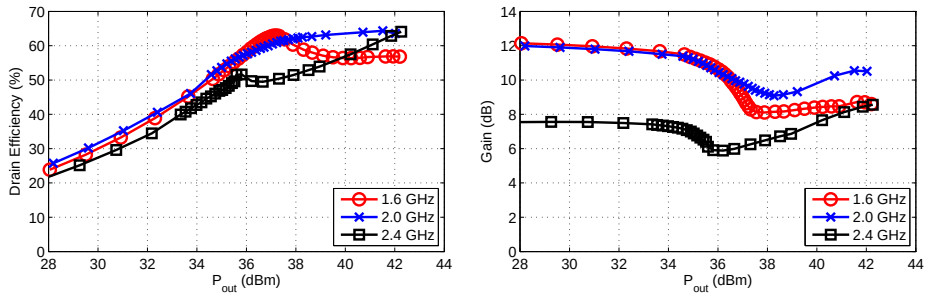
Figure 5.6: Photo of the PA demonstrator circuit.

The measured drain efficiency and gain at 1.6, 2.0 and 2.4 GHz are plotted versus output power in figure Fig. 5.7. The main and peak amplifier bias where set to 17.5 V and 30 V, respectively, which indicates $\xi_b = 0.5$ if accounting for 5 V knee-voltage. As observed, the efficiency in back-off is almost identical at all three frequencies, in good agreement with the theory.

Fig. 5.8 demonstrates the drain efficiency and PAE at full output power (42 dBm) and at 6 dB OPBO (36 dBm) versus frequency when using the same bias as for Fig. 5.7. The result demonstrates a drain efficiency that is larger than 50 % at both full output power and at 6 dB OPBO from 1.5 to 2.4 GHz. Unfortunately, the measured frequency range was not large enough to determine the 1 dB efficiency bandwidth. Fig. 5.9 shows how the gain becomes low at high frequencies while it remains larger than 8 dB from 1.6 to 2.1 GHz. The gain decrease at higher frequencies was not predicted by simulations and implies a reduced PAE as reported in Fig. 5.8b.

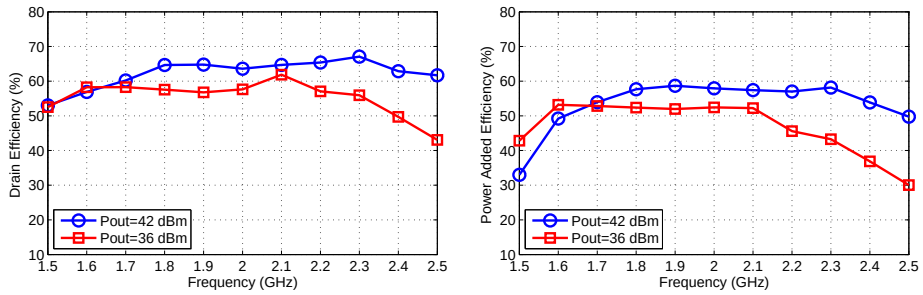
The reconfigurability of P_{BO} was verified by measuring the drain efficiency versus output power for different values of the main amplifier bias V_{ds1}. The result, reported in Fig. 5.10, demonstrates a distinct agreement with Fig. 5.2b.

The measurements thereby confirms the theoretical findings, both in terms of bandwidth and reconfigurability, and makes the presented PA an interesting candidate for realization of multi standard and efficient wireless transmitters.



(a) (b)

Figure 5.7: The measured (a) drain efficiency, and (b) gain, versus output power at different frequencies. V_{ds1} = 17.5 V, V_{ds2} = 30 V, V_{g1} = -2.8 V, V_{g2} = -4.5 V.



(a) (b)

Figure 5.8: The measured (a) drain efficiency, and (b) PAE at full output power (42 dBm) and at 6 dB output power back-off (36 dBm) versus frequency. V_{ds1} = 17.5 V, V_{ds2} = 30 V, V_{g1} = −2.8 V, V_{g2} = −4.5 V.

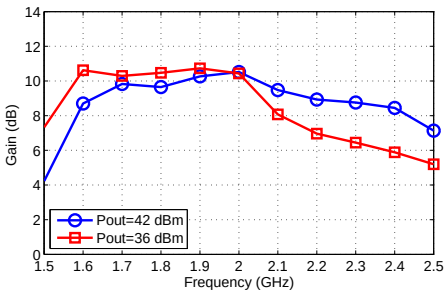


Figure 5.9: The measured gain at full output power (42 dBm) and at 6 dB output power back-off (36 dBm) versus frequency. V_{ds1} = 17.5 V, V_{ds2} = 30 V, V_{g1} = −2.8 V, V_{g2} = −4.5 V.

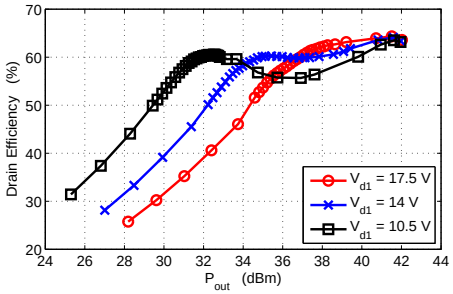


Figure 5.10: Measured drain efficiency vs. output power at 2.0 GHz for different main amplifier drain biases. V_{ds2} = 30 V, V_{g1} = −2.8 V, V_{g2} = −4.5 V.

Chapter 6

Conclusions

The work presented in this thesis has aimed to provide a more complete understanding of theoretical and practical issues related to the design of RF and microwave wideband Doherty power amplifiers.

A theoretical frequency response analysis of the ideal DPA was performed in order to understand and illustrate theoretical bandwidth limitations of the ideal DPA. The analysis showed that the bandwidth in back-off becomes more narrow when high efficiency is requested at deep back-off levels whereas the bandwidth at full output power is invariant of the frequency.

Established techniques used for designing DPA-combining networks were examined in order to understand practical limitations of DPA designs. It was concluded that the examined topologies have shortcomings when a high characteristic impedance needs to be realized, and/or when components, such as spiral inductors, has limited current handling capabilities. In [Paper A] we therefore proposed the Tee-line network of transmission lines that enables simple design of high characteristic impedance impedance inverters with realizable component dimensions. The utility of the Tee-line network was verified by the design and measurements of a 7-8 GHz DPA, implemented on GaN MMIC. The reported results showed state-of-the art performance both in terms of PAE and bandwidth.

With respect to the inherent bandwidth limitations of the DPA, a new PA, based on the DPA-topology, was presented in [Paper B]. It was theoretically demonstrated that the proposed PA can provide a significantly larger bandwidth compared to the DPA, as well as reconfigurability of the efficiency in back-off. A demonstrator circuit with individually controlled RF-inputs was designed to verify the theory. The reported results showed a drain efficiency larger than 48 % in 6 dB output power back-off in the 1.5-2.4 GHz frequency range. The reconfigurability of the efficiency in back-off was also demonstrated and showed excellent agreement with theory. The large bandwidth combined with the possibility to reconfigure the efficiency in power back-off makes the presented PA an interesting candidate for realization of multi standard and efficient wireless transmitters.

6.1 Future work

The work presented in this thesis has established a fundamental understanding of the practical and theoretical limitations of the DPA, in particular with respect to its bandwidth and frequency response.

Based on this knowledge, we will continue to explore how the performance can be further stretched e.g. by using DPD linearization techniques. In particular, we plan to investigate the linearization of the new power amplifier in [Paper B]. The dual input DPD architecture presented in [25, 26] is of particular interest for this architecture. The operation and linearization during concurrent multi-band operation is also interesting to investigate.

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Paper A

A Wideband and Compact GaN MMIC Doherty Amplifier for Microwave Link Applications

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Paper B

Theory and Design of a Novel Wideband and Reconfigurable High Average Efficiency Power Amplifier

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