

THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Class-E Power Amplifiers for Pulsed Transmitters

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Abstract

Nowadays the main driving parameters for the radio transmitter research are: energy efficiency, frequency re-configurability and integration. Pulsed transmitter architectures have attracted large interest in the recent years due to their potential to meet these demands. In pulsed transmitters, a highly efficient switch mode power amplifier (SMPA) is used in conjunction with a pulse modulator to achieve high efficiency linear amplification. Digital implementation of the modulator enables wide bandwidth for the signal generation path and improves the level integration. The bandwidth in a pulsed transmitter is however typically limited by the load matching network of the SMPA. This thesis presents two main contributions in the field of pulsed transmitter architectures.

In the first part focus is given to bandwidth improvement of class-E switch mode PAs. A continuum of novel closed-form class-E modes is derived extending the traditional class-E design space. The extended design space provides important possibilities for wide band design of the class-E load networks and for further efficiency optimization of class-E PAs. A wide band design methodology is thus developed based on the analytical design equations.

In the second part, focus is given to efficiency improvement of RF pulse width modulation (RF-PWM) based transmitters. A new SMPA topology particularly suitable for energy efficient amplification of RF-PWM signals is derived. It is analytically shown that high efficiency can be maintained over a wide power dynamic range if the imaginary part of the class-E load impedance is varied along with the pulse width. Using in-house (Chalmers University) SiC varactor diodes to implement the tunable load impedance, a 2 GHz 10 W peak output power CMOS-GaN HEMT RF-PWM transmitter demonstrator is realized. The static measurements show that a drain efficiency $> 70\%$ can be obtained over a 6.5 dB dynamic range. A digital pre-distortion based linearization scheme is proposed to enhance the linearity of the transmitter. An adjacent power ratio of -45 dBc and average drain efficiency of 67% is achieved using a realistic W-CDMA communication signal. These results clearly demonstrate the feasibility of the proposed pulsed transmitter topology for high efficiency linear amplification.

keywords

Class-E, energy efficiency, frequency agility, pulsed transmitters, RF-PWM.

List of Publications

Appended Publications

This thesis is based on the work contained in the following papers.

- [A] M. Özen, R. Jos, and C. Fager, "On the Continuity of Class-E Power Amplifier Modes", *Manuscript*.
- [B] M. Özen, R. Jos, C. M. Andersson, M. Acar, and C. Fager, "High-Efficiency RF Pulsewidth Modulation of Class-E Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol.59, no.11, pp.2931-2942, Nov. 2011
- [C] M. Özen, C. M. Andersson, Thomas Eriksson, M. Acar, R. Jos, and C. Fager, "Linearization Study of a Highly Efficient CMOS-GaN RF Pulse Width Modulation Based Transmitter", to appear in *2012 European Microwave Conference Digest*, Amsterdam, Nov. 2012

Other Publications

The following paper has been published but is not included in the thesis. The content partially overlaps with the appended papers or is out of the scope of this thesis.

- [a] M. Özen, C. M. Andersson, M. Thorsell, K. Andersson, N. Rorsman, C. Fager, M. Acar, M.P. van der Heijden, R. Jos, "High efficiency RF pulse width modulation with tunable load network class-E PA," *2011 IEEE Wireless and Microwave Technology Conference (WAMICON)*, April 2011

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Chapter 1

Introduction

1.1 Motivation

In the last decades, data rates of wireless communications systems have increased tremendously due to the large increase in the number of mobile subscribers and expanding use of mobile internet. Increasing data rates has important impacts on the design and realization of radio frequency (RF) transmitters.

Current wireless standards such as Wideband Code Division Multiple Access (W-CDMA), Worldwide Interoperability for Microwave Access (WiMAX), Long Term Evolution (LTE), use high order modulation techniques to increase the spectral efficiency and thus the capacity. This results in high peak-to-average power (PAPR) signals. The efficiency of traditional linear power amplifiers (PAs), unfortunately, decrease very quickly versus output power back-off causing low average efficiency with high PAPR signals [1]. This results in high operational costs in radio base stations and short battery life times in mobile terminals. Furthermore, the transmitter sizes becomes larger since more cooling and a larger power supply units are needed [2].

For LTE and beyond, fragmented spectrum allocations over wide frequency ranges are planned to further increase the capacity. Frequency agility of the RF transmitters is therefore very crucial for realization of the future wireless

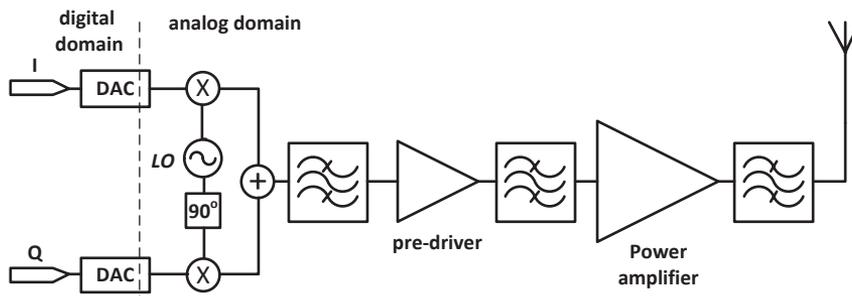


Figure 1.1: A simplified block diagram of conventional up-conversion transmitter architecture.

infrastructures. In conventional up-conversion transmitters, see Fig. 1.1, the analog components in the chain, i.e. mixers, filters and matching networks, limit the bandwidth. It is thus desired to bring the digital CMOS circuitry closer to the antenna to skip band limiting analog components for an improved frequency agility.

The vast growth of the wireless industry increased the manufacturing volumes considerably. High level of integration is therefore becoming very crucial to reduce the transmitter cost. This further stresses the digitalization and need for transmitter architectures that profit from CMOS scaling road maps.

1.2 Pulsed Transmitters

Pulsed transmitter architectures have attracted large interest in the recent years due to their high potential for realization of energy efficient, highly digitalized frequency agile transmitters [3]. In pulsed transmitters, a highly efficient switch mode power amplifier (SMPA) is used in conjunction with a pulse modulator to achieve high efficiency linear amplification, see Fig. 1.2. There are a number of coding techniques for modulation of the amplitude in pulsed transmitters. The best known techniques are $\Delta\Sigma$ modulation, carrier pulse width modulation (PWM) and RF pulse width modulation (RF-PWM). A general overview of pulse modulation techniques can be found in [4]. Advanced sub-micron silicon technologies enable pulse modulators to be realized at microwave frequencies. In [5], a 2 GHz RF pulse width modulator is implemented in 65 nm CMOS. A 2 GHz $\Delta\Sigma$ modulator is implemented in a SiGe bipolar technology in [6]. The modulated pulse train is typically pre-amplified with a chain of inverters before the final SMPA stage [7], [8]. Pulsed transmitter topologies may therefore provide wide bandwidth until the final SMPA stage and also high level of integration. The load matching network of the SMPA therefore remains as the only bandlimiting block in pulsed transmitters. Also, the overall efficiency is mainly determined by the efficiency of the SMPA.

Clearly, the design of SMPAs that are compatible with pulsed architectures is essential and determine the overall transmitter performance, both in terms of bandwidth and efficiency.

For RF SMPAs, low energy losses at the switching instances is crucial for high efficiency operation. Class-E PAs are well known for their low loss switching behavior and are therefore identified as the most suitable SMPA topology for RF frequencies [9].

1.3 Thesis Outline

In this thesis, we focus on the theory and design of energy efficient wide bandwidth class-E PAs for pulsed transmitter architectures.

The thesis is organized as follows. In Chapter 2, theory and design of class-E PAs are reviewed. Important class-E variants and their design equations are presented. In Chapter 3, a continuum of novel closed-form class-E solutions is derived. A wide band class-E design procedure is then developed that is based on the novel derivation. Chapter 4, focuses on a novel class-E topology

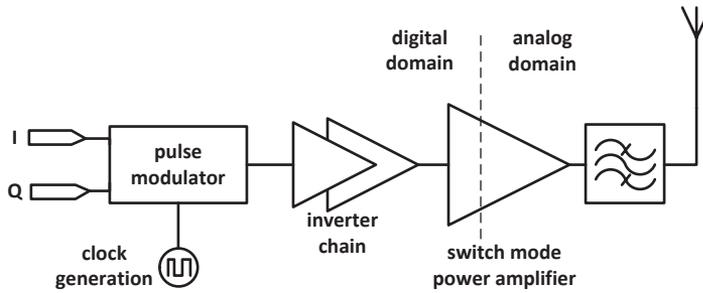


Figure 1.2: A generic block diagram of pulsed transmitters.

that is particularly suitable for efficient amplification of RF-PWM signals. A 2 GHz 10 Watt output power RF-PWM transmitter is constructed and characterized with realistic communication signals to demonstrate the feasibility of the proposed technique. Finally, conclusions are given in Chapter V.

Chapter 2

Class-E Power Amplifiers

Class-E is a single ended PA consisting of an active switching device and a load network to shape the switch waveforms, see Fig. 2.1. The load network is designed to satisfy the following switching conditions to ensure low switching losses [10]:

$$v_C \left(\frac{2\pi}{\omega_0} \right) = 0 \quad (2.1)$$

$$\left. \frac{dv_C(t)}{dt} \right|_{t=\frac{2\pi}{\omega_0}} = 0 \quad (2.2)$$

where $v_C(t)$ is the voltage across the capacitor C shown in Fig. 2.1. The condition given in (2.1) is named zero voltage switching (ZVS) which is necessary to prevent losses due to discharge of capacitor C at off-to-on switching instances. Power losses in switching circuits due to non-ZVS follow as:

$$P_C = f_o \frac{1}{2} C V_C^2 \quad (2.3)$$

where V_C is the voltage across the capacitor C at the turn on moments of the switch. The condition given in (2.2) is named zero voltage derivative switching (ZVDS). Note that, from Kirchoff's current law, current through

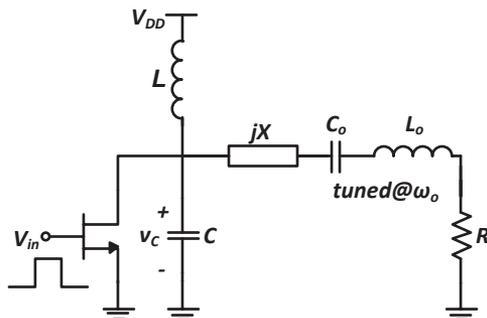


Figure 2.1: Schematic of class-E PAs.

C is transferred to the switch at the transition instances. ZVDS is therefore meant to prevent a high current flow through an unsaturated transistor during off-to-on transitions [9].

The series resonant filter in the load network, which is tuned at ω_o , is meant to suppress the harmonic currents. The reactive element X is therefore only effective for the fundamental tone because ideally there is no harmonic current through the load resistance R .

Design of class-E PAs requires $\{L, C, X, R\}$ values to be calculated to satisfy the ZVS and ZVDS switching conditions. In the original work of Sokal, it is assumed that L in Fig. 2.1 has an infinite inductance and therefore the current through L has only a DC component [10]. This assumption greatly simplifies the circuit analysis. However, later it is shown that, class-E PAs with finite feed inductance gives much better design flexibility and also better performance. In the following sections, first, design of conventional class-E PAs, so called class-E with RF-choke feed inductance, is treated. Next, design of class-E PAs with finite feed inductance is treated, following the historical development of class-E theory.

2.1 Class-E Power Amplifiers with RF-choke Feed Inductance

Analysis of class-E PAs with RF-choke feed inductance can be found in [11]. Here, only the results will be used to outline the design steps. Assumptions made for the circuit analysis are however important to mention, which follow as:

- The transistor is replaced with an ideal switch for the analysis, see Fig. 2.2. The switch has a zero on-resistance and infinite off-state resistance.
- Reactive elements are lossless and the only loss occur in the load resistance R .
- The current flowing through the load resistance is a pure sinusoid at the switching frequency. This assumption is valid only if the loaded quality factor (Q_L) of the series LC filter is infinite. Loaded quality factor is defined as $Q_L = \omega_o L_o / R$ where $\omega_o = 1/\sqrt{L_o C_o}$.

The switch duty cycle is defined as the on-duration of the switch normalized with the RF period. Class-E PAs can in principle be realized at any switch duty cycle, but a duty cycle of 50% is conventionally used for easier drive signal generation, e.g. by using a sinusoidal input signal. According to the circuit analysis, required C and X values at 50% switch duty cycle follow as:

$$C = \frac{0.1836}{\omega_o R} \tag{2.4}$$

$$X = 1.14R \tag{2.5}$$

Corresponding normalized switch waveforms are shown in Fig. 2.1.

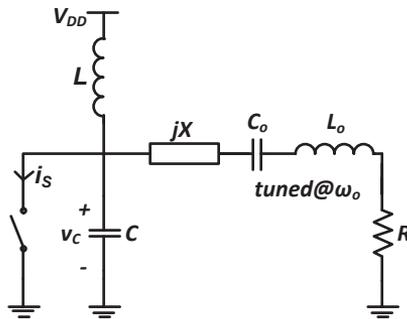
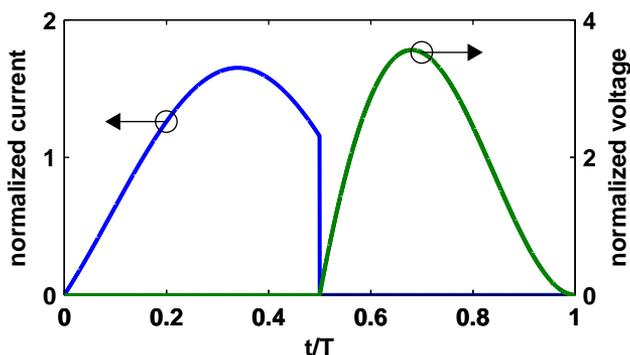


Figure 2.2: Idealized schematic of class-E PAs.

Figure 2.3: Normalized conventional class-E voltage, v_C/V_{DD} , and current, $i_S R/V_{DD}$, waveforms.

The values of V_{DD} and R should be known for a complete design. The supply voltage V_{DD} should be determined considering that the maximum value of the switch voltage (v_{Cmax}) should not exceed the breakdown voltage (V_{BR}) of the device, where

$$v_{Cmax} = 3.56V_{DD} \quad (2.6)$$

The load resistance R is dependent on output power level and V_{DD} :

$$R = 0.58 \frac{V_{DD}^2}{P_{out}} \quad (2.7)$$

It is also important to know the maximum value of the switch current (i_{Smax}) to determine the required device size. The expression for i_{Smax} is given by

$$i_{Smax} = 1.66 \frac{V_{DD}}{R} \quad (2.8)$$

It is worth to mention that the load resistance R also can be determined to maximize the output power for a given device size using (2.8).

Finally, values of L_o and C_o can be calculated using the selected Q_L value. As mentioned previously, the circuit analysis assumes that no harmonic current flows through the load resistance. Higher values of Q_L will therefore better approximate the ideal waveforms. In practice, Q_L values in the order of 10–20 already yield almost ideal waveforms [12].

The power utilization factor (U) quantifies the maximum output power for given device current and breakdown voltage, and is for an ideal RF choke feed class E PA given by:

$$U = \frac{P_{out}}{v_{Cmax} i_{Smax}} = 0.0981 \quad (2.9)$$

Class-E mode can not be realized if the required C is smaller than the device output capacitor (C_{out}). This fact sets a maximum limit for the operating frequency (f_{max}):

$$f_{max} = 0.063 \frac{I_{max}}{C_{out} V_{BR}} \quad (2.10)$$

where I_{max} is the maximum current capability of the device. Observe that, f_{max} is independent of the device size. It is therefore universal for a given device technology.

2.2 Class-E Power Amplifiers with Finite Feed Inductance

Since Sokal introduced the class-E concept [10], different variants has been proposed to improve the performance in terms of maximum operating frequency and power utilization factor. Best known variants are even harmonic resonant and parallel circuit class-E PAs. In even harmonic resonant class-E, it is assumed that the feed inductor resonate out capacitor C at an even harmonic of the carrier frequency, i.e. $2n\omega_o = 1/\sqrt{LC}$, where n is a positive integer number [13]. Values of $\{C, X, R\}$ are then calculated to satisfy the switching conditions. In parallel circuit class-E, component X is assumed to be a short circuit [14] and required values of (C, L, R) are calculated.

Design equations and performance of class-E variants, including the conventional solution, are summarized in Table 2.2. Term q in the table is equal to normalized resonant frequency of the circuit formed by parallel connection of feed inductance L and C , see Fig. 2.1:

$$q = \frac{1}{\omega_o \sqrt{LC}} \quad (2.11)$$

As seen from the table, even harmonic resonant class-E has the highest f_{max} though the lowest U . Parallel circuit class-E has the highest U and provides 1.75 times higher f_{max} than class-E with RF-choke does.

2.2.1 Generalized Class-E Design Equations

In [15], it is analytically proven that, class-E switching conditions can actually be satisfied for an arbitrary value of q . The derived design equations and the

	RF-Choke [11]	parallel circuit [14]	even harmonic [13] resonant ($n = 1$)
q	0	1.412	2
$\omega_o RC$	0.1836	0.685	0.071
X/R	1.14	0	-4.903
v_{Smax}/V_{DD}	3.56	3.65	3.78
$i_{Smax}R/V_{DD}$	1.66	3.61	0.22
RP_{out}/V_{DD}^2	0.58	1.365	0.056
f_{max}	0.063	0.11	0.191
U	0.0981	0.1036	0.066

Table 2.1: Summary of design formulas and performance figure of merits for different class-E variants. $\bar{f}_{max} = f_{max}/(\frac{I_{max}}{C_{out}V_{BR}})$

waveform expressions have the following forms:

$$C = \frac{1}{\omega_o R} K_C(d, q) \quad (2.12)$$

$$X = RK_X(d, q) \quad (2.13)$$

$$R = \frac{V_{DD}^2}{P_{out}} K_P(d, q) \quad (2.14)$$

$$v_C(t) = V_{DD}v(d, q, t) \quad (2.15)$$

$$i_S(t) = \frac{V_{DD}}{R} i(d, q, t) \quad (2.16)$$

where functions $\{K_C, K_X, K_P, v, i\}$ can be found in [15], and also in [Paper B, Section III]¹. Variable d represents the switch duty cycle, e.g. $d = 1$ corresponds to 100% duty cycle. Example normalized switch waveforms for different q values are shown in Fig. 2.4.

Free selection of q gives extra flexibility for the design, where its optimal value is dependent on the design considerations. For instance, q can be selected to maximize the power utilization factor yielding minimum possible device size for a given output power level. Power utilization factor is plotted versus q in Fig. 2.5 and is maximum at approximately $q = 1.5$. Once q is known, V_{DD} can be determined from (2.15) considering that the maximum value of v_C should not exceed switch breakdown voltage. Values of C, X, R and L are found through (2.12)-(2.14) and from (2.11), respectively.

It can also be desirable to fully absorb C by the device output capacitance C_{out} for a lower complexity of the load network. This implies $C = C_{out}$ and allows q, V_{DD} and R to be solved from (2.12),(2.14) and (2.15). Remaining circuit element values X and L are then easily calculated using found values of q and R .

It is useful to know values of f_{max} versus q for a specific technology. The

¹Equations derived in [Paper B] have an extra independent variable k to parameterize the voltage slope at off-to-on instances. It must therefore be set to zero to achieve (2.12)-(2.16)

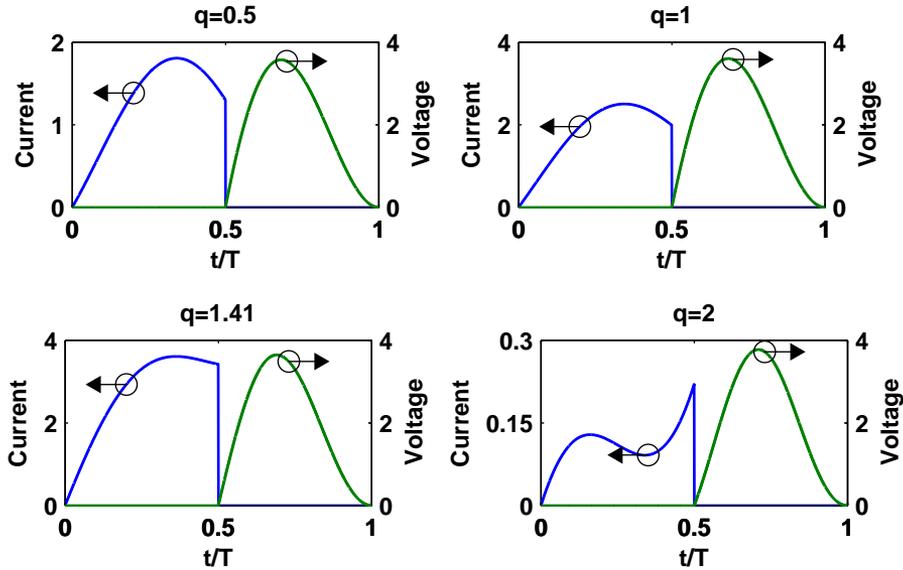


Figure 2.4: Normalized voltage and current waveforms, v_C/V_{DD} and $i_S R/V_{DD}$ respectively, for different q values.

expression of f_{max} is easily derived using (2.12)-(2.16):

$$f_{max} = \frac{K_C v_{Cmax}}{2\pi R i_{Smax}} \frac{I_{max}}{V_{BR} C_{out}} \quad (2.17)$$

Note that, the first term in the expression purely depends on q and the latter on the device technology. Normalized f_{max} is plotted versus q also in Fig. 2.5. As seen from the figure, although both f_{max} and U increases until at approximately $q = 1.5$, there is a compromise between them for higher q values.

In this chapter, theory and design of class-E PAs has been reviewed. As explained, development of the class-E theory essentially follows finding different combinations of component values $\{L, C, X, R\}$ that satisfy the switching conditions. In the next chapter, a new dimension is brought to the class-E theory and the design space is further extended. The extended design space provides important possibilities especially for wide band designs.

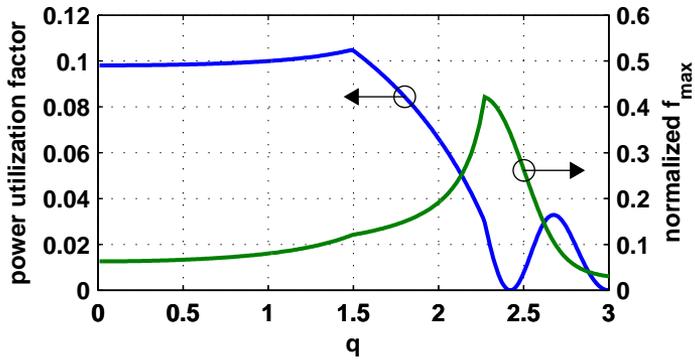


Figure 2.5: Power utilization factor and f_{max} normalized with device technology factor ($I_{max}/V_{BR}C_{out}$) versus q at 50% duty cycle.

Chapter 3

Continuous Class-E Power Amplifier Modes

Class-E PA design at a fixed operating frequency is a straight forward task as shown in the previous chapter. It is however challenging to maintain the class-E operation over a wide range of frequencies with passive only load networks [9], [16]. The limiting factors for the bandwidth can easily be understood by studying the design equations of class-E PAs, e.g. the ones for the conventional mode, which from the previous section follow as:

$$C = \frac{0.1836}{\omega_o R}$$
$$X = 1.14R$$

The first requirement is valid only for a fixed frequency if C is a fixed capacitor. Term X represent the residual reactance of the tuned filter in the load network of class-E PAs, see Fig. 2.1. The tuned filter, however, depending on the Q factor, may present a highly sensitive impedance versus the frequency. The second requirement is therefore also difficult to satisfy over a wide range of frequencies. Also note that, the requirements above are calculated assuming that the current through the load branch is a pure sinusoid at the carrier frequency. This requires that the harmonic impedances seen by the switch-capacitor combination are open circuits. At microwave frequencies, generally shunt quarter wavelength ($\lambda/4$ at $n\omega_o$) stubs are used to filter out the harmonics. The impedance trajectory of these kinds of filters are however, very sensitive to frequency, making it almost impossible to provide fixed harmonic impedances for wide bandwidth. It is important to mention that, especially the second harmonic load impedance has high impact on efficiency of class-E PAs [17].

In [Paper A], it is analytically proven that, for a certain reactive second harmonic load impedance, it is possible to find a X/R value and a $\omega_o RC$ value, that ensure ZVS and ZVDS. This knowledge provides important possibilities for wide band class-E PA synthesis. In addition, arbitrary selection of the second harmonic load impedance enables robust shaping of the switch waveforms for further performance optimization. In the next section, corresponding design equations are presented.

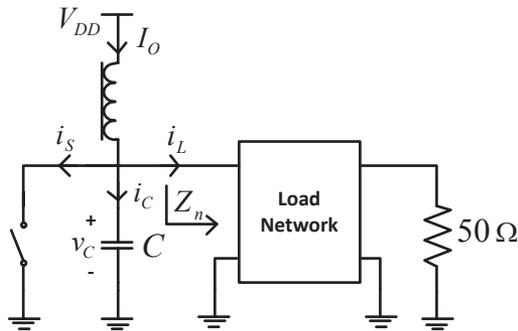


Figure 3.1: Generic single ended switch mode power amplifier schematic. Term Z_n denotes the impedance provided by the load network at $n\omega_o$, where n is the harmonic index.

3.1 Design Equations and Switch Waveforms

The analysis in [Paper A] is done referring the generic SMPA schematic shown in Fig. 3.1. The following assumptions are made for the circuit analysis:

1. The switch is on during $0 \leq t < \pi/\omega_o$ and off during $\pi/\omega_o \leq t < 2\pi/\omega_o$.
2. The switch is lossless, i.e. it has a zero on state resistance and infinite off state resistance.
3. The load matching network shown in Fig. 3.1 consists of only reactive lossless passive components.
4. The load matching network provides a fundamental impedance of $Z_1 = (1 + jx_1)R$ and second harmonic impedance of $Z_2 = jx_2R$. Higher order harmonic impedances are open circuits, $Z_n = \infty$, $n > 2$.

Note that, assumptions 1-3 are made also for the analysis of conventional class-E PAs, see Chapter 2. The novelty of the derivation is thus revealed by the last assumption.

The circuit design parameters, i.e. expression of $\{x_1, x_2, C\}$, are derived as functions of only one independent variable, ϕ_1 , which denotes phase of the fundamental tone load current. The design equations therefore reveal continuous class-E solutions, which are expressed as functions of ϕ_1 , noting that $\phi_1 = 57.5^\circ$ corresponds to conventional class-E solution. The circuit design parameters follow as:

$$x_1 = \frac{1}{12\pi} \sec(\phi_1)^2 [3\pi^2 + 16\pi \cos(\phi_1)^2 \cot(\phi_1) + 2\pi \sin(2\phi_1) - 32] \quad (3.1)$$

$$x_2 = \frac{\pi [3\pi + 4 \sin(2 \tan^{-1}(2 \cot(\phi_1)))] + 2(\cos(2 \tan^{-1}(2 \cot(\phi_1))) - 2) \tan(\phi_1)}{24 \cos(\phi_1)(\pi \cos(\phi_1) - 2 \sin(\phi_1))} \quad (3.2)$$

$$C = \frac{2}{\pi\omega_o R} \cos(\phi_1)^2 \quad (3.3)$$

The switch current and voltage expressions are also derived as functions of ϕ_1 :

$$i_S(t) = \frac{V_{DD}}{R} \frac{4}{\pi^2} \sin(\phi_1) \left[\cos(\phi_1) (\pi \cos(2\omega_o t - \tan^{-1}(2 \cot(\phi_1))) \sqrt{1 + 4 \cot(\phi_1)^2} - 4 \sin(2\omega_o t)) - \pi \cos(\omega_o t + \phi_1) + 4 \sin(\phi_1) \sin(\omega_o t)^2 \right] \quad (3.4)$$

$$v_C(t) = \frac{V_{DD}}{\pi} \tan(\phi_1) \left[4\omega_o t \tan(\phi_1) - 6\pi \tan(\phi_1) + (4\pi \cot(\phi_1) - 8) \sin(\omega_o t)^2 - 2\pi \sec(\phi_1) \sin(\omega_o t + \phi_1) + (\pi - 2 \tan(\phi_1)) \sin(2\omega_o t) \right] \quad (3.5)$$

Examples of normalized switch waveforms are shown in Fig. 3.2 for different values of ϕ_1 . As seen from the figure, by changing ϕ_1 the switch waveforms can be shaped differently for performance optimization. For instance, losses during on to off transitions might be severe due to jump in the current waveform for the conventional class-E waveforms, see the waveforms for $\phi_1 = 57.5^\circ$, especially if a slow switching device is used [18]. In [19], class- E_M concept was introduced to address this issue. The switch waveforms were in that case shaped for zero current switching (ZCS) at the turn off moments of the switch via active second harmonic current injection. Active current injection however cost extra DC power and increases circuit complexity dramatically. By proper selection of ϕ_1 , the current waveform can actually be optimized for a relatively lower switch current at the turn off moment, see the waveforms for $\phi_1 = 77^\circ$, better tolerating the switching speed. In addition to switching losses, ohmic losses due to finite on resistance of the device also has to be considered to maximize the peak efficiency. As the design equations are compact, they can easily be implemented in circuit simulators to find the best compromise between the switching and ohmic losses in a specific application.

It is important to mention that the solution given with $\phi = 90^\circ$, satisfies ZCS at the turn off moment of the switch, see Fig. 3.2. However, the peak value of the resulting voltage waveform tends to infinity for that solution yielding zero output power. In fact, this property for SMPAs was proven theoretically in [20], where it is stated that ZVS, ZVDS and ZCS can not be simultaneously satisfied at a finite output power level with a passive load network.

The RF output power is given by:

$$P_{out} = \frac{V_{DD}^2}{R} \frac{8 \sin(\phi_1)^2}{\pi^2} \quad (3.6)$$

Note that, value of V_{DD} need to be determined according to the maximum value of the voltage waveform. By inspection of Fig. 3.2, the peak voltage is well approximated by $3.6V_{DD}$ for relevant $\phi \in [45^\circ, 77^\circ]$.

The power utilization factor is plotted versus ϕ_1 in Fig. 3.3. Solutions achieved with in the $\phi_1 \in [45^\circ, 77^\circ]$ give U values comparable to the that of conventional class-E: $U = 0.0981$. This proves that the output power achieved with conventional class-E mode can be maintained over a range of solutions for the same device size.

Finally, maximum operating frequency versus ϕ_1 follow as:

$$f_{max} = \frac{\cos \phi_1^2 v_{Cmax}}{\pi^2 R i_{Smax}} \frac{I_{max}}{V_{BR} C_{out}} \quad (3.7)$$

Normalized f_{max} is plotted versus ϕ_1 also in Fig. 3.3.

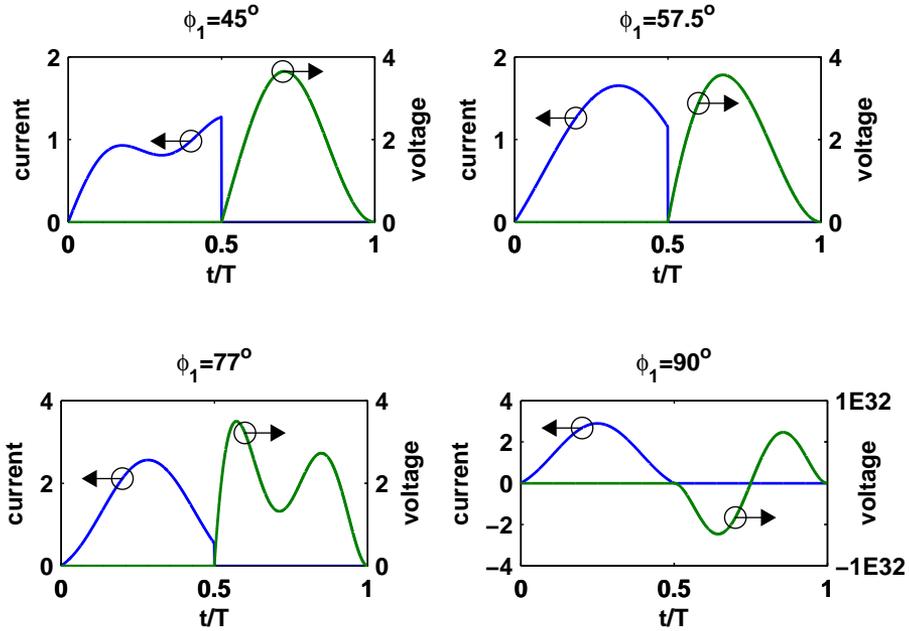


Figure 3.2: Normalized switch current, $i_S R/V_{DD}$, and voltage, v_C/V_{DD} , waveforms for different ϕ_1 values. Time is normalized with the period (T).

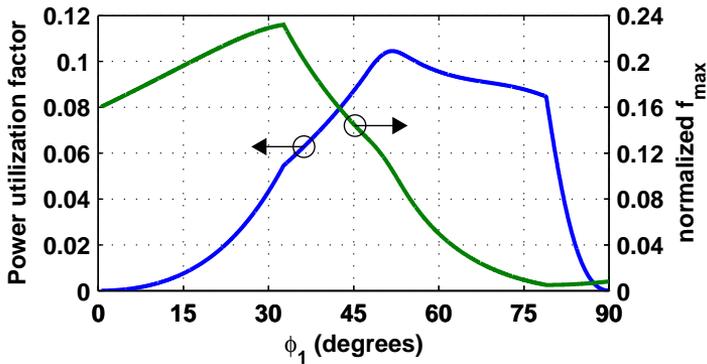


Figure 3.3: Power utilization factor and f_{max} normalized with device technology factor ($I_{max}/V_{BR}C_{out}$) versus ϕ_1 .

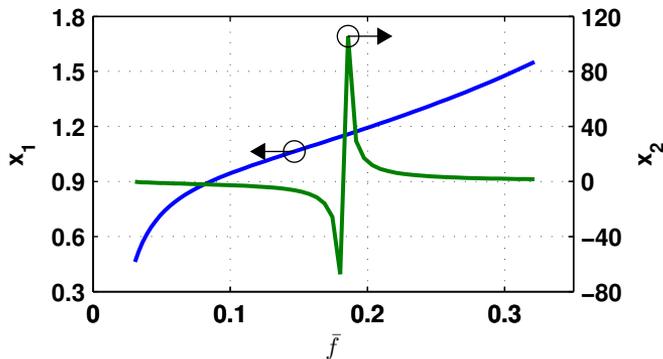


Figure 3.4: Reactive parts of the fundamental tone and second harmonic impedances normalized with fundamental resistive load impedance (R), x_1 and x_2 , respectively, versus normalized frequency, $\bar{f} = \omega_o RC$.

3.2 Wide Band Class-E Design Methodology

Using the design formulas and the waveform expressions presented in the previous sections, a wide band class-E design methodology can be outlined as follows: First, ϕ_1 and R are solved over the frequency range using (3.3) and (3.6) by assuming a constant C , e.g. $C = C_{out}$, and a constant P_{out} . If desired R may be kept constant at the cost of output power variation versus frequency according to (3.6). Thereafter, required normalized fundamental and second harmonic reactive impedances are calculated versus frequency by substituting ϕ_1 in (3.1) and (3.2), respectively.

Terms x_1 and x_2 are plotted versus normalized frequency, $\bar{f} = \omega_o RC$ in Fig. 3.4. These graphs depict the variation of the reactive load impedances versus frequency for fixed R and C values. The graphs are generated for the ϕ_1 range of $[45^\circ, 77^\circ]$ because the solutions in that range can provide output power levels comparable to conventional class-E mode operation, see Fig. 3.3.

Note that the resulting Z_1 and Z_2 values will be trajectories versus frequency rather than fixed values, see Fig. 3.5. Class E conditions may thus be preserved over a greatly improved bandwidth by mapping the inevitable frequency dependence of the load network impedance to these trajectories. The high flexibility offered by the extended class E design space is thus expected to find many applications where high efficiency and wide bandwidth are requested.

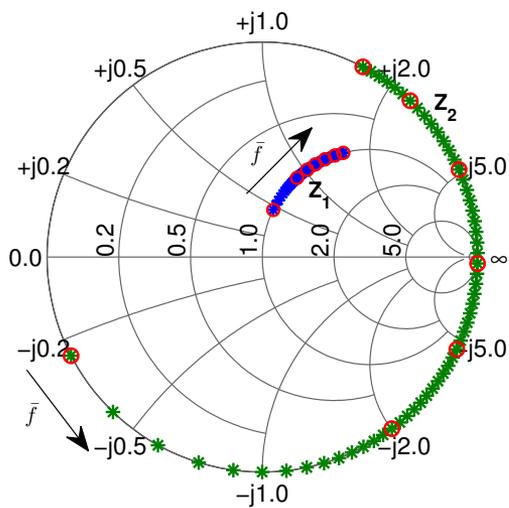


Figure 3.5: Fundamental tone and second harmonic load impedances, Z_1 and Z_2 respectively, versus normalized frequency, $\bar{f} = \omega_o RC$, for a load resistance (R) of 50Ω , which is also the reference impedance for the Smith diagram. The circle markers represent the normalized frequency points from 0.03 to 0.33 in step of 0.05.

Chapter 4

High Efficiency RF Pulse Width Modulation of Class-E PAs

RF pulse width modulation (RF-PWM) is a promising technique for amplitude modulation of SMPAs. In this chapter, a novel class-E based SMPA topology is developed particularly suitable for energy efficient amplification of RF-PWM signals. First, operation principle of RF-PWM transmitters is introduced.

4.1 RF Pulse Width Modulation Transmitters

The RF-PWM concept was first proposed by Besslich in [21] for linear amplification with highly efficient SMPAs. In RF-PWM, the pulse width of an RF square wave is varied according to the signal envelope. Phase information is conveyed by timing of the pulses. The resulting pulse train is amplified with an SMPA. Post-PA filtering is necessary to recover the signal around the carrier frequency. A block diagram of RF-PWM architectures is shown in Fig. 4.1.

The main challenge associated with the RF-PWM architecture is that conventional SMPAs work with high efficiency only for a fixed duty cycle. Variable duty cycles at the input create severe switching losses decreasing the efficiency [22], [5], [23]. Therefore, in spite of its high potential, no competitive efficiency results have been published with RF-PWM architectures so far.

In Fig. 4.2, simulated switch waveforms of a class-E PA with a non-optimal duty cycle at the input is shown to illustrate the loss mechanisms. The PA is designed to operate at 50% duty cycle, whereas 25% duty cycle is used at the input. As seen from the figure, there is a high voltage and current overlap at the switching instances due to non-ZVS. Clearly, research on novel SMPAs topologies is necessary to successfully enable the high potential of RF-PWM architectures.

In [Paper B], a class-E based novel PA topology is developed that is particularly suitable for energy efficient amplification of RF-PWM signals. It is analytically derived that a class-E PA with varying imaginary load impedance can provide ZVS operation over a wide range of duty cycles. RF-PWM of

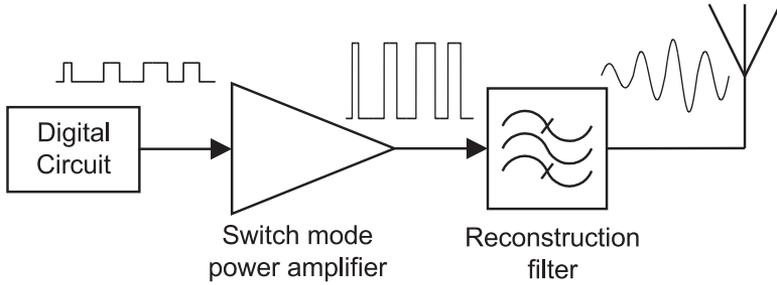


Figure 4.1: A block diagram of RF pulse width modulation based transmitter architectures.

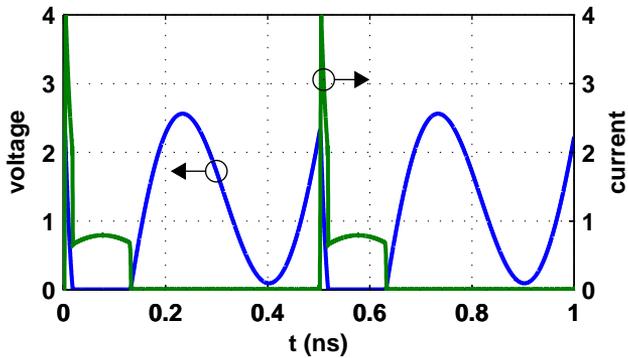


Figure 4.2: Simulated switch waveforms of class-E PA with a non-optimal duty cycle at the input.

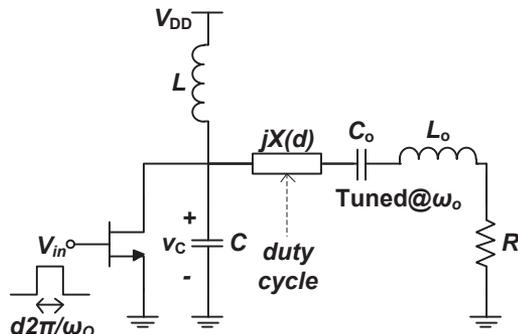


Figure 4.3: Class-E power amplifier with tunable X for high efficiency RF pulse width modulation.

such a PA will therefore not suffer from any severe switching losses and consequently provide high average efficiency with realistic, modulated signals. The operation principle of the proposed PA topology is explained in detail in the next section.

4.2 Efficient RF Pulse Width Modulated SMPA

The components of a class-E PA are optimized for a fixed duty cycle, see Chapter 2. If the duty cycle is varied from its nominal value, the switching conditions are violated and the losses increase dramatically. A possible way to preserve the switching conditions is therefore to have electronically tunable components in the load network. Singhal *et al.* [24] analytically proved that ZVS and ZVDS switching conditions can be preserved if the $\{C, R\}$ components of a parallel circuit Class-E PA are modulated along with the duty cycle. For Class-E PAs with finite feed inductance, both switching conditions can actually be preserved if two of the reactive components of the Class-E, $\{C, X\}$ or $\{L, X\}$, are re-optimized as the duty cycle is varied. This property can easily be seen by studying the design equations (2.12)-(2.14). However, it is highly desirable to have only one tunable component in the load network from a complexity point of view. Tunable inductors are not practical which excludes L , while the tuning range of C will be limited by the output capacitor of the device. Element X is therefore selected as the tunable element, see Fig. 4.3.

Tuning only one element allows only one of the switching conditions to be preserved. The literature shows that, ZVS is more important for high efficiency than ZVDS [11], [25]. It is therefore preferred to preserve ZVS, which corresponds to sub-optimal (or variable voltage slope) class-E mode. Corresponding design equations for this mode are required to calculate the X value versus the duty cycle.

Raab derived design equations for suboptimal class-E PAs with RF-choke at the supply at arbitrary duty cycle in [11]. However, as discussed in Chapter 2, class-E PAs with finite feed inductance gives much higher design flexibility. In [Paper B], design equations for suboptimal class-E PAs with finite feed inductance are therefore derived for arbitrary duty cycle.

The derivation is based on the following off-to-on switching conditions:

$$v_C \left(\frac{2\pi}{\omega_0} \right) = 0, \quad (4.1)$$

$$\left. \frac{dv_C(t)}{dt} \right|_{t=\frac{2\pi}{\omega_0}} = k\omega_0 V_{DD} \quad (4.2)$$

where k is a real number used to parameterize the voltage slope at off-to-on switching moments. The resulting design equations have the following forms:

$$C = \frac{1}{\omega_0 R} K_C(d, q, k) \quad (4.3)$$

$$X = R K_X(d, q, k) \quad (4.4)$$

$$R = \frac{V_{DD}^2}{P_{out}} K_P(d, q, k) \quad (4.5)$$

where the functions $\{K_C, K_X, K_L\}$ are found in [Paper B]. Please also note that this formulation is similar to the expressions in (2.12)-(2.14), but with k as an added degree of freedom.

In (4.3), C should be fixed. Therefore k has a relation to the duty cycle d , i.e. $k = k(d)$. The optimal X trajectory versus d then follows as $X = R K_X(d, q, k(d))$. Examples of class-E switch waveforms for variable duty cycle and X values are shown in Fig. 4.4. As seen from the figure, there is no voltage and current overlap at the switching instances yielding near 100% efficiency, but the transistor technology must be able to carry negative current.

A systematic design procedure is also developed in [Paper B]. The procedure allows practical realization of the proposed topology from circuit and component specifications.

4.3 Prototype RF-PWM Transmitter

Following the design procedure and using in-house (Chalmers University) SiC varactor diodes [26] to implement the tunable imaginary load impedance, a 2 GHz 10 W peak output power GaN HEMT (*Cree* CGH60015DE) circuit demonstrator is realized. A block diagram of the demonstrator is shown in Fig. 4.5.

RF-PWM input signals for characterization of the prototype PA is generated with a single stage inverter implemented in a 65 nm CMOS process [7]. A schematic of the inverter is shown in Fig. 4.6. Ideally, the gate bias voltages of both NMOS and PMOS transistors in an inverter should be varied to control the duty cycle. However, experiments have shown that keeping the NMOS voltage fixed does not degrade the performance significantly in terms of efficiency and output power dynamic range [Paper B]. The duty cycle is therefore controlled by only varying the gate bias voltage of the PMOS transistor, V_{gP} .

The output of the modulator is directly connected to the gate of the GaN HEMT device using very short bond wires, see Fig. 4.7. This ensures that square shaped signals across the gate of the GaN HEMT can be maintained over a wide range of frequencies. The RF input port of the CMOS chip is connected to an external RF synthesizer with no input matching network in between.

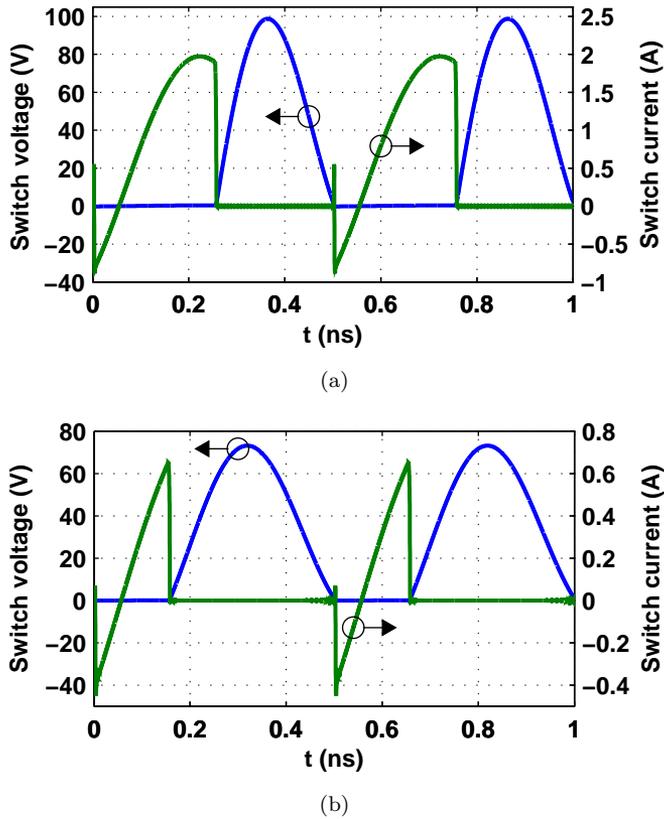


Figure 4.4: Simulated switch waveforms: (a) The duty cycle is 50% and $X = 34 \Omega$ (b) The duty cycle is 30% and $X = 101 \Omega$.

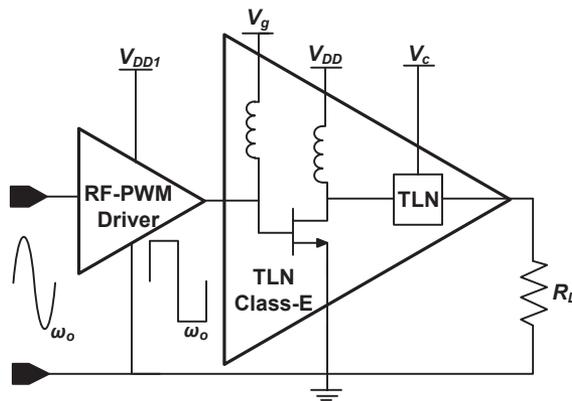


Figure 4.5: Block diagram of the RF pulse width modulated tunable load network (TLN) class-E transmitter.

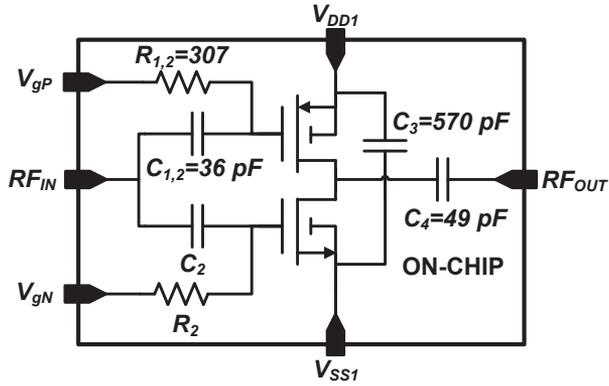


Figure 4.6: Schematic of the RF pulse width modulator used to generate the input signal to the transmitter in Fig. 4.5

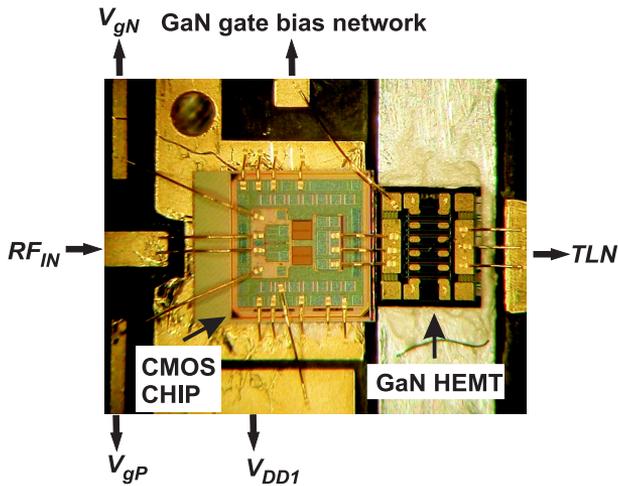


Figure 4.7: CMOS RF pulse width modulator and GaN HEMT line up. Drain terminal of the GaN HEMT is connected to a tunable load network (TLN).

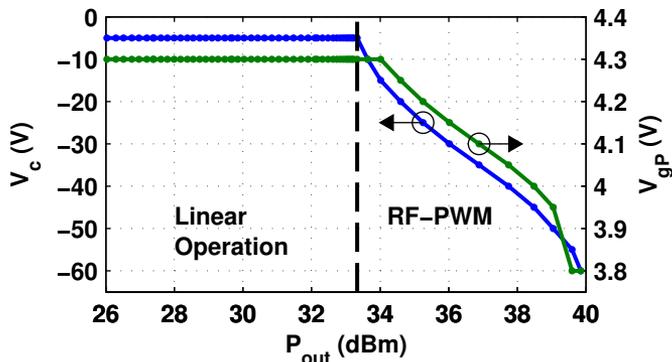


Figure 4.8: The optimal varactor and duty cycle control voltages, V_c and V_{gP} , respectively, versus the output power, P_{out} , at 2 GHz carrier frequency.

4.3.1 Static Characterization

For operation of the transmitter, the optimal combination of V_c and V_{gP} that maximizes the efficiency at every output power has to be identified. This is performed by varying V_c with a step and optimizing the V_{gP} at each step for the best transmitter efficiency based on continuous wave static measurements with a power meter. The resulting efficiency optimized control functions are shown in Fig. 4.8 and the corresponding efficiency performance is shown in Fig. 4.10. The efficiency definitions are given by

$$\eta = \frac{P_{out}}{P_{DC1}} \quad (4.6)$$

$$\eta_{tot} = \frac{P_{out}}{P_{DC1} + P_{DC2} + P_A} \quad (4.7)$$

where P_{DC1} and P_{DC2} are the DC powers drawn by the Class-E stage and the modulator stages, respectively. P_A is the available RF power from the RF synthesizer applied to the modulator input.

The output power dynamic range achieved with RF-PWM operation is around 6.5 dB as seen from Fig. 4.8. This dynamic range is clearly not enough for linear amplification of modern communication signals, e.g. W-CDMA or LTE. This limitation can, however, be circumvented by operating the transmitter in linear mode in further back-off where the output power is directly controlled by the RF input power rather than the duty cycle and varactor voltage. The resulting input-output power relation is shown in Fig. 4.9.

The efficiency results are shown in Fig. 4.10. Observe that, the efficiency of the class-E stage remains fairly constant versus output power for the RF-PWM region as expected from the theory.

4.3.2 Dynamic Characterization and Linearization

Characterization of the transmitter with modulated realistic signals require that the baseband signals are generated dynamically. A two channel arbitrary waveform generator (Tabor Electronics WW2572A) (AWG) is used to generate

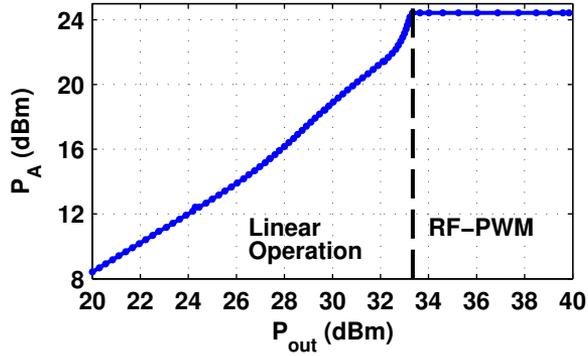


Figure 4.9: The available input power from the RF synthesizer, P_A , versus the output power, P_{out} . The carrier frequency is 2 GHz.

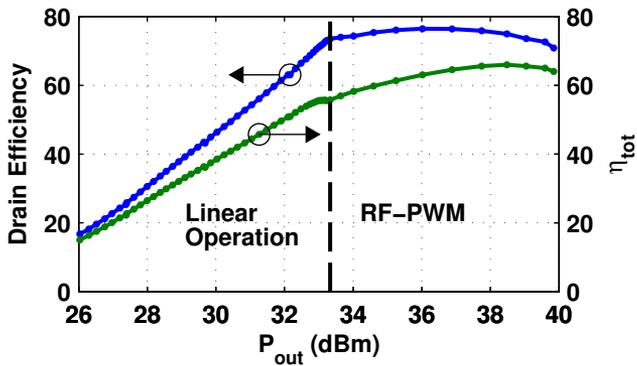


Figure 4.10: The measured drain efficiency of the Class-E stage, η , and the overall transmitter efficiency, η_{tot} , versus the output power, P_{out} , at 2 GHz carrier frequency.

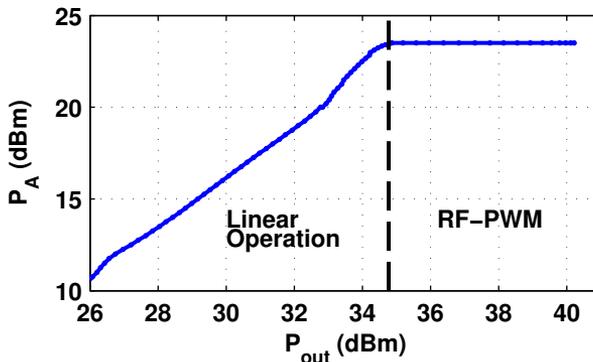


Figure 4.11: The available RF input power, P_A , versus the delivered output power, P_{out} with optimized varactor control signal for a smooth transition between linear and RF-PWM modes. The carrier frequency is 2 GHz.

the baseband signals. A high speed op-amp (MS Kennedy 600r) based feedback amplifier is used to amplify the varactor control signal to the required level, see Fig. 4.8. The duty cycle control signal V_{gP} can directly be generated with the AWG. RF input signal is generated using an evaluation board from Texas Instruments (TSW3100), consisting of two digital to analog converters (DAC) for I and Q branches and an IQ modulator. An Agilent 54845A oscilloscope is used as the measurement receiver [Paper C].

As switch mode operation requires CMOS and GaN HEMT devices to be deeply saturated, severe gain expansion is unavoidable in the transition to the linear operation region. This creates a strong discontinuity in the input-output RF power relation as seen from Fig. 4.9. The RF input signal therefore overshoots at the mode transitions creating significant distortion in the output signal. Furthermore, the linearity becomes highly sensitive to the delay mismatch between the RF-baseband signal paths due to abrupt variation of the input-output RF power relation. The varactor signal can, however, be re-optimized to obtain a smoother transition between linear and switch modes. This is done in two steps. First, input-output RF power relation is interpolated over the gain expansion region using cubic piece-wise polynomials [27] in a way that the transition is smooth. Varactor signal V_c is then optimized at each input power level to best approximate the interpolated output power levels. The resulting measured input-output power relation with optimized varactor signal for a smooth transition is shown in Fig. 4.11. Optimizing the varactor signal for the linearity over the transition region costs a slight reduction in the efficiency but greatly improves the linearity [Paper C].

A digital pre-distortion (DPD) linearization scheme is incorporated to enhance the linearity of the transmitter, see Fig. 4.12. The transmitter is considered as a single input single output system. Efficiency optimized input signals are derived from the predistorted input signal (\hat{x}) using a digital splitter constructed from the static CW measurement data, i.e. $\{V_c(\hat{x}), V_{gP}(\hat{x}), RF_{in}(\hat{x})\}$, as depicted in Fig. 4.12. The DPD model parameters are identified by comparing the measured output sample (y) and the input sample (x). A vector

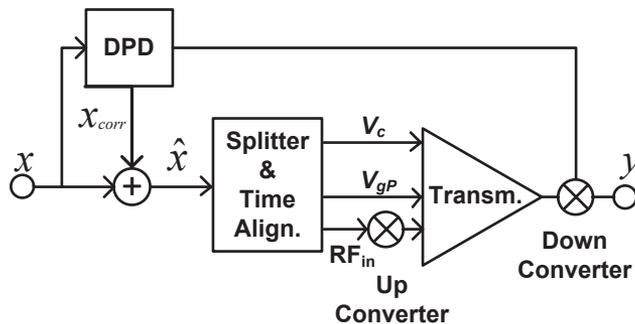


Figure 4.12: Digital pre-distortion linearization scheme.

Table 4.1: Summary of the linearization results

	NMSE (dB)	ACPR (dBc)	$P_{out-avg}$ (Watt)	η_{avg}	$\eta_{tot-avg}$
Before DPD	-13	-23	2.23	67.5%	55.5%
After DPD	-35	-45	2.18	67%	55%

switched generalized memory polynomial (VS-GMP) model is used as the behavioral model for DPD operation [28]. The VS-GMP quantize the signal according to the signal amplitude into a number of regions and model each region separately. That model is therefore very suitable for behavioral modeling of this type of transmitter which has two distinct operating regions: linear and RF-PWM, see Fig. 4.9.

A 3.84 MHz 6.7 dB PAPR W-CDMA signal is used for dynamic characterization. Normalized mean square error (NMSE) is used as the metric to measure the distortion on the output signal, defined as:

$$\text{NMSE} = \frac{\sum_n |x[n] - y[n]|^2}{\sum_n |x[n]|^2} \quad (4.8)$$

As shown in Table 4.1, NMSE is improved 22 dB with DPD without sacrificing the efficiency. Output spectra before and after linearization are shown in Fig. 4.13. The nonlinear transfer function of the transmitter causes severe spectral re-growth. The adjacent channel power ratio (ACPR) can however be suppressed down to -45 dBc by using the presented DPD.

These promising results clearly prove feasibility of the proposed transmitter architecture for efficient linear amplification of realistic communication signals.

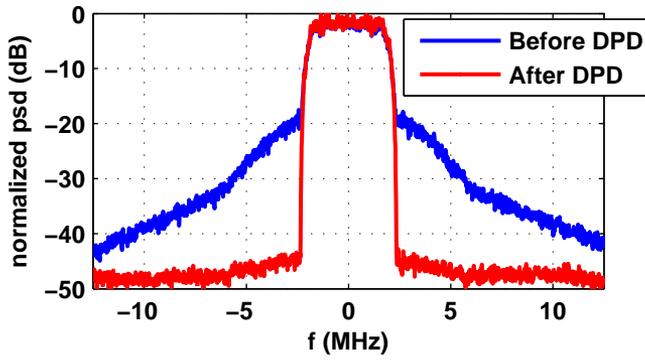


Figure 4.13: Normalized output power spectrum before and after digital pre-distortion linearization.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

Energy efficient wide bandwidth SMPAs are the key components for realization of high performance pulse modulated transmitters. In this thesis, class-E PAs are extensively studied to understand their bandwidth and efficiency potential for such applications.

In the first part of the thesis focus is given on bandwidth improvement of class-E PAs. A continuum of novel closed-form solutions is derived for class-E PAs. It is analytically proven that, for an arbitrarily selected reactive second harmonic load impedance, it is possible to find a fundamental tone impedance and a frequency normalized time constant that ensures ZVS and ZVDS. This knowledge gives important possibilities for wide band class-E synthesis. A wide band design procedure is thus outlined based on the closed form design equations derived. The high flexibility offered by the extended class-E design space is expected to find many applications where high efficiency and wide bandwidth are requested.

The possibilities of using class E PAs for realization of highly efficient pulsed transmitters was investigated in Chapter 4 where a new SMPA topology particularly suitable for RF-PWM applications was presented. The proposed class-E PA with reactive load tuning can provide ZVS operation for variable duty cycles. Thus, in contrast to the existing SMPAs, it does not suffer from switching losses as the duty cycle is varied from the nominal value. Consequently, RF-PWM of the proposed PA can provide an average efficiency that is very close to the peak efficiency for realistic, modulated signals. A prototype 2 GHz RF-PWM transmitter is manufactured for experimental verification of the theory. A very good agreement is achieved between the theory and the measurement results. The measured drain efficiency of the Class-E stage is higher than 70% and the overall transmitter efficiency is higher than 55% over a 6.5 dB of output power dynamic range proving the feasibility of the proposed PA topology for application in future wireless transmitters.

The appealing efficiency results presented and the potential shown for wide

bandwidth operation is motivating for further explorations. The results obtained have demonstrated the potential of class-E PAs for realization of energy efficient wide bandwidth pulsed transmitters.

5.2 Future Work

The research presented in this thesis has established a foundation for how to enable wide bandwidth efficient pulsed transmitters based on class-E PAs. In our future work we plan to continue these investigations.

The wide bandwidth class-E design approach that was outlined in Chapter 3 and in [Paper A] has, so far, only been demonstrated theoretically. In order to better understand its limitations and potential in real applications, it is planned to design a wide bandwidth CMOS-GaN HEMT class-E PA following the design procedure presented. Furthermore, the derivation in Chapter 3 can be generalized for arbitrary duty cycles. This may give possibilities for design of wide bandwidth tunable load network class-E PAs for efficient amplification of RF-PWM signals.

Smaller cell sizes are planned for LTE. This implies power levels will go down that may enable realization of PAs in sub-micron CMOS or BiCMOS (Bipolar-CMOS) technologies. Since these technologies allows complex highly integrated designs to be made, multi bit class-E topologies, that can be amplitude modulated with a digital control word, are interesting to investigate. It is also planned to investigate the feasibility of CMOS-GaN MMIC multi bit switch line-up for moderate and high power applications.

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Paper A

On the Continuity of Class-E Power Amplifier Modes

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Manuscript

Paper B

High-Efficiency RF Pulsewidth Modulation of Class-E Power Amplifiers

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Paper C

Linearization Study of a Highly Efficient CMOS-GaN RF Pulse Width Modulation Based Transmitter

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