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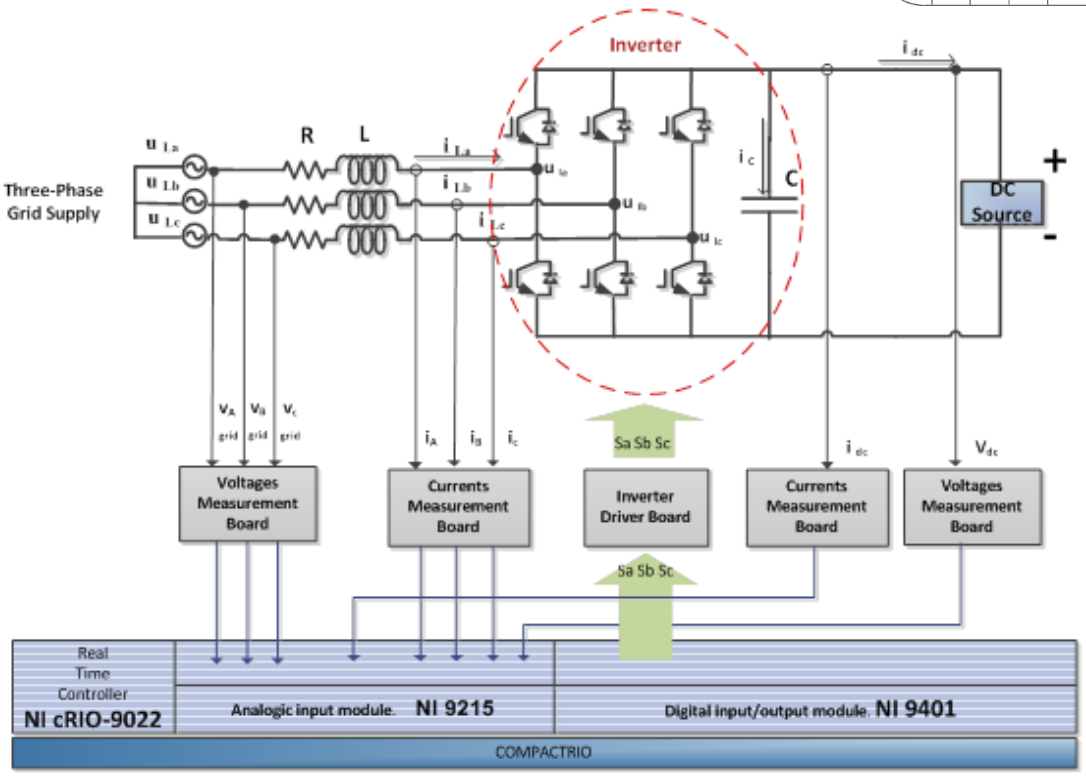

Design and Implementation of a Three-Phase Boost Battery Charger with PFC using CompactRIO Control System

Master of Science Thesis in Electric Power Engineering

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Göteborg, Sweden, 2012

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Abstract

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In a plug-in hybrid electric vehicle, the utility grid charges the vehicle battery through a battery charger. For a three-phase grid supply voltage, three-phase boost rectifiers are commonly used as chargers. Bi-directional power transfer capability and unit power factor operation become desirable features due to the increasing power quality requirements on the grid-connected converters.

The Voltage Oriented Control is one of the methods based on high performance dq-coordinate controllers which satisfies the increasing power quality requirements. The Voltage Oriented Control method for a three-phase boost rectifier has been designed, simulated and implemented. The system simulation is performed using Matlab/Simulink software as well as Labview. A feedforward decoupled current controller is designed along with a Pulse Width Modulation scheme to control the battery charging. The controller, consisting of a current controller and a DC-link voltage controller, is designed using a method called Internal Model Control.

A National Instruments CompactRIO system is used for practical implementation. The system directly runs a Labview model to execute the control. The Labview files are developed for this purpose. A brief explanation of the system configuration is provided for the experimental system.

Keywords : battery charger, decoupled controller, Internal Model Control (IMC), Pulse Width Modulation (PWM), three-phase boost PWM rectifier, Voltage Oriented Control (VOC).

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Daniel and Javier

Göteborg, Sweden

2012

List of symbols, superscripts, subscripts and abbreviations

ABBREVIATIONS	SIGNAL OR VARIABLE
$\mathbf{P_g}$	Power supplied by the grid
$\boldsymbol{P_{load}}$	Power consumed by the battery
$\boldsymbol{V_{LL(rms)}}$	Line-to-line voltage supply
$\boldsymbol{V_{DC}}$	DC Bus voltage
$\boldsymbol{V_{LN(rms)}}$	Line-to-neutral voltage supply
$\boldsymbol{R_{load}}$	Load resistance
$\boldsymbol{E_m}$	Amplitude of Line-to-Neutral voltage
R	Resistance of the line for each phase
$\boldsymbol{L}$	Inductance of the line for each phase
$\boldsymbol{\omega}$	Frequency
$\boldsymbol{id}$	Current direct axis
$\boldsymbol{iq}$	Current quadrature axis
$\mathbf{I_{Ripple}}$	Ripple current
C	Capacitance of the inverter
$\boldsymbol{V_d^*}$	d-axis component of the reference voltage
$\boldsymbol{V_q^*}$	q-axis component of the reference voltage
θ	Voltage angle
$\boldsymbol{\alpha_i}$	Current controller bandwidth
$\boldsymbol{\alpha_v}$	Voltage controller bandwidth
$\boldsymbol{K_{pv}}$	Voltage controller proportional coefficient
$\boldsymbol{K_{iv}}$	Voltage controller integrator coefficient
$\boldsymbol{K_{ii}}$	Current controller integrator coefficient
$\boldsymbol{K_{pi}}$	Current controller proportional coefficient
$\boldsymbol{\gamma_1}$	PLL integrator coefficient
$\boldsymbol{\gamma_2}$	PLL proportional coefficient
W	Vdc^2
$\boldsymbol{fsw}$	Switching frequency
Tj	Temperature in the junction
VOC	Voltage Oriented Control
PLL	Phase locked loop
IGBT	Insulated gate bipolar transistor
VFOC	Virtual Flux Oriented Control
PWM	Pulse Width Modulation
UPF	Unit Power Factor
DPC	Direct Power Control

TABLE OF CONTENTS

Chapter 1. Introduction.

In this introductory chapter, the project background, main objectives and thesis outline are described.

1.1. Background of the thesis and previous work.

Nowadays, the level of pollution and the fossil fuel availability problem has contributed to a quick evolution of the hybrid and electric vehicles.

Electric and hybrid vehicles use electric power from the grid to charge their batteries but they usually do not use the traction system during charging. Since the battery charging and traction power do not happen at the same time, both inverter and engine can be used as a charger avoiding the need of building one with a rectifier. The possibility of using a motor as a double set of inductors during the charge time allows the implementation of an integrated charger to achieve a considerable reduction of weight, volume and price [1].

According to [2], the proposed charger is an isolated high power integrated charger based in the use of half of the windings of the engine during the charge. The use of this specific engine with the charger will be a new project to in a near future.

1.2. Purpose of the thesis.

The main purpose of this thesis is to design and implement an integrated charger for an electrical or hybrid vehicle with a power requirement of 15KW and unit power factor operation as well as achieving the control of the inverter.

Firstly, the design of the different hardware is done. After this, simulations are conducted on Matlab/Simulink software [3] to check the validity of the design.

Secondly, the control system is developed by programming on LabView and implemented using a CompactRIO control device.
Finally, the experimental system is implemented in the laboratory and the results are obtained.

1.3. Outline of the thesis.

This thesis is divided into 6 chapters. After this first chapter of introduction, the modeling and the selected type of control for the rectifier are explained in chapter 2. In chapter 3, the design of the system as well as the Matlab simulations are included. After that, chapter 4 includes the simulations of all the control programmed in Labview followed by chapter 5, in which the practical implementation is included.

Finally, in chapter 6, all the results and conclusions are shown as well as the future work.

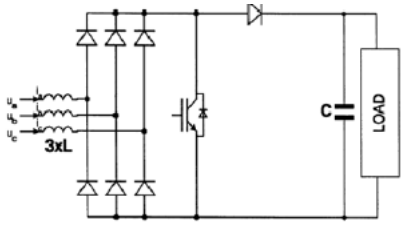
Appendices are added to this report as part of the thesis. Matlab code used in simulations, lab setup diagrams and datasheets of the lab components are shown in appendices.

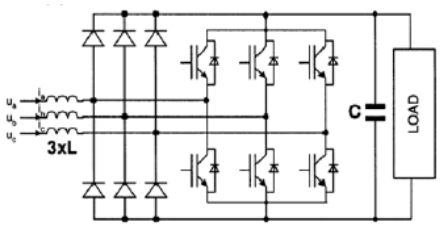
Chapter 2. Modeling and voltage oriented control of the rectifier.

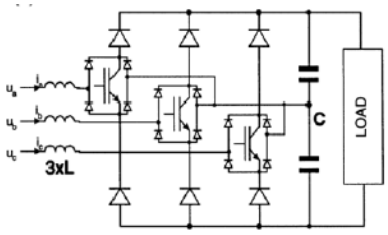
In this chapter, the rectifier topology is discussed. After that, the selected type of control (VOC) is presented as well as the mathematical model used to carry it out.

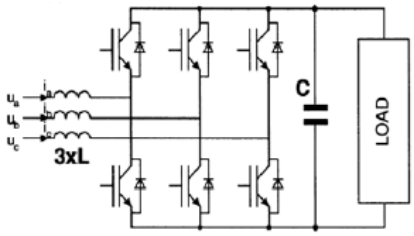
2.1. Three phase controlled rectifiers.

The aim of the thesis is to develop a three phase charger with unit power factor operation. To achieve that, several topologies have been compared and analyzed in Figure 1 in order to choose the topology which fulfills the requirements better.

<table>
<tr><th>Simple solution of the boost converter</th><th>Using PWM rectifier modules</th></tr>
<tr><td> 

High stress on the components.
Low frequency distortion on the input current.</td><td> 

Low current rating (20-25% RMS current).
Low cost potential.
Possibility of regeneration.
Possibility of active filtering.
DC regulation is more difficult.</td></tr>
<tr><th>Vienna rectifier</th><th>Universal bridge topology</th></tr>
<tr><td> 

Low switch voltage.
High power density.
Unidirectional power flow.
It can provide UPF.</td><td> 

It can provide UPF.
Bidirectional energy flow.
High switching losses.
High per unit current rating.</td></tr>
</table>

Figure 1: Comparison of topologies [4][5].

According to the specifications, the universal bridge topology is chosen and implemented using the SEMIKRON inverter.

2.2. Voltage oriented control.

Comparing several control methods, a VOC (Voltage Oriented Control) or VFOC (Virtual Field Oriented Control) can be implemented because both methods have the same advantages:

- Fixed switching frequency, which makes easier to design the input filter.
- Low sampling frequency for good performance.
- Advanced PWM is feasible with this control.
- A/D converters are cheap.

These control methods have also some disadvantages it is necessary to deal with:

- Decoupling between active and reactive power is required.
- Complex algorithm.
- Input power factor is lower than using DPC (Direct Power Control) or VF-DPC (Virtual Flux Direct Power Control).

The main advantage of the VFOC control against VOC is the better behaviour under non-linear conditions in the line voltage. In order to simplify the algorithm and due to the requirements of the system, the VOC control is implemented [3].

The Voltage Oriented Control is based on a series of transformations from a three phase stationary reference system *abc* to a synchronous rotating reference system *d-q* through a two phase stationary reference system *α-β*. With these transformations, the control voltages remain constant and become DC values, making all the control process more simple. A closed-loop current control is used. A scheme of the Voltage Oriented Control is shown in Figure 2.

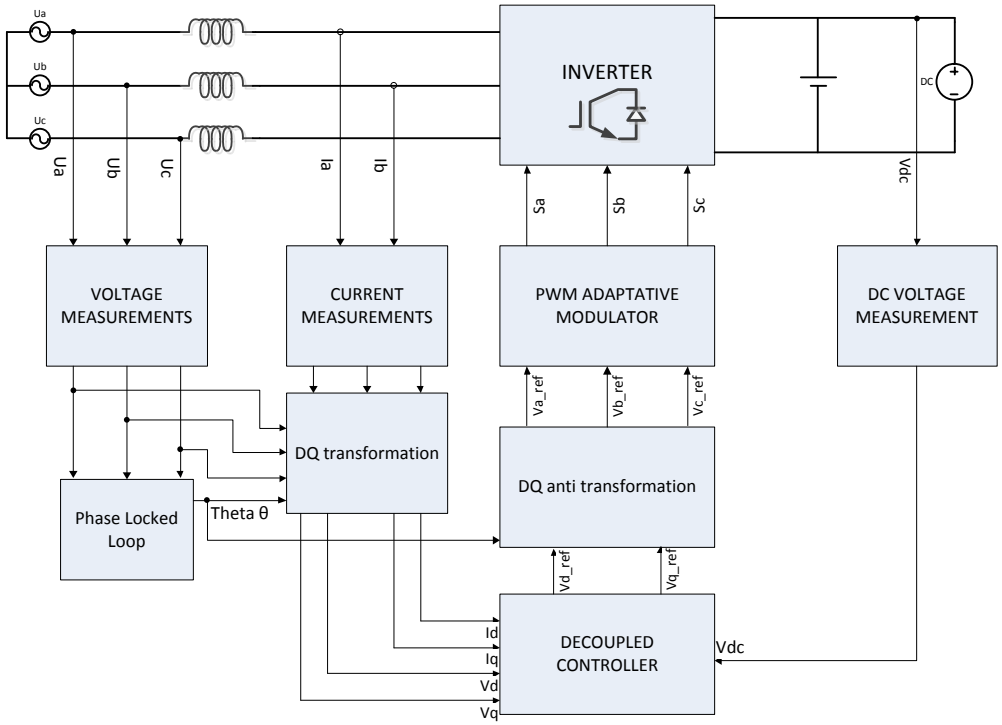


Figure 2: VOC scheme.

The mathematical model and transformations used for the control are the following:

2.2.1. Space vector definition for voltage and current.

In a three phase system, the voltages and currents are defined by the equations 2.1 and 2.2.

$$\begin{aligned} Ua &= \sqrt{2}V_{LN(rms)} \cdot \cos \omega t \\ Ub &= \sqrt{2}V_{LN(rms)} \cdot \cos(\omega t - \tfrac{2\pi}{3}) \\ Uc &= \sqrt{2}V_{LN(rms)} \cdot \cos(\omega t + \tfrac{2\pi}{3}) \end{aligned} \tag{2.1}$$

$$\begin{aligned} Ia &= Im \cdot \cos(\omega t + \varphi) \\ Ib &= Im \cdot \cos(\omega t + \varphi - \tfrac{2\pi}{3}) \\ Ic &= Im \cdot \cos(\omega t + \varphi + \tfrac{2\pi}{3}) \end{aligned} \tag{2.2}$$

These three voltages or currents can be split in only two components α and β (real and imaginary respectively) [6][7][8].

$$v^s = v_\alpha + jv_\beta = \frac{2}{3}k(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}}) \tag{2.3}$$

For the control system that is going to be developed K=1 gives an amplitude invariant which facilitates the control. In other applications another K can be interesting in order to have power invariant (k=$\sqrt{3/2}$) or RMS invariant (k=1/$\sqrt{2}$) [8].

2.2.2. From abc to α-β using Clarke transformation.

The α-β transformation can be expressed applying the matrix form of the space vector definition.

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.4}$$

After the transformation the voltage equation can be written as follows.

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = R \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} u_{S\alpha} \\ u_{S\beta} \end{bmatrix} \tag{2.5}$$

2.2.3. From α-β to d-q using Park transformation.

Physically, after the Clarke transformation, it is required to control 2 voltages (*α-β*) instead of 3 voltages (*abc*), which simplifies the control. However, u_α and u_β are still sinusoidal signals rotating physically with the angular speed of the electrical system ω. Changing again the reference axis onto new axis, which are rotating at the same angular speed ω, an amplitude invariance can be achieved. Applying Park transformation in *d-q* axis, the *α-β* axis are displaced by the angle θ, as shown in [6] [7] [8].

$$v_{dq} = v^s e^{-j\theta} \tag{2.6}$$

After applying the θ transformation.

$$u_{dq} = Ri_{dq} + L\frac{di_{dq}}{dt} + jL\omega i_{dq} + u_{Sdq} \tag{2.7}$$

After that, the real and the imaginary part are identified.

$$\begin{aligned} u_d &= Ri_d + L\frac{di_d}{dt} - \omega L i_q + u_{Sd} \\ u_q &= Ri_q + L\frac{di_q}{dt} + \omega L i_d + u_{Sq} \\ C\frac{du_{dc}}{dt} &= \frac{3}{2}\left(S_d i_d + S_q i_q\right) - i_{load} \end{aligned} \tag{2.8}$$

2.2.4. Active and reactive power.

Using the transformations shown before, an expression for the active and reactive power can be obtained [7].

$$\begin{aligned} Re\{v^s\ (i^s)^*\} &= Re\{v^{dq}\ (i^{dq})^*\} \\ v^s\ (i^s)^* &= \left(\frac{2}{3}K\right)^2 \left(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{j\frac{4\pi}{3}}\right)\left(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}}\right)^* \\ &= \left(\frac{2}{3}K\right)^2 \left[v_a i_a + v_b i_b + v_c i_c + j\frac{1}{\sqrt{3}}\left(v_a(i_c - i_b) + v_b(i_a - i_c) + v_c(i_b - i_a)\right)\right] \end{aligned} \tag{2.9}$$

From the real part, the active power is obtained.

$$P = \frac{3}{2K^2} Re\{v^s\ (i^s)^*\} = \frac{3}{2K^2} Re\{v^{dq}\ (i^{dq})^*\} = v_a i_a + v_b i_b + v_c i_c \qquad (2.10)$$

From the imaginary part, the reactive power can be calculated.

$$Q = \frac{3}{2K^2}\ Im(v^s\ (i^s)^*) = \frac{3}{2K^2} Im\{v^{dq}\ (i^{dq})^*\}$$
$$= \frac{1}{\sqrt{3}}[v_a(i_c - i_b) + v_b(i_a - i_c) + v_c(i_b - i_a)]. \qquad (2.11)$$

In this particular case, as consequence of the transformation to *d-q* axes, the *q* component of the voltage is zero. Because a charger with unit power factor is being implemented, the current will be synchronized with the voltage and therefore, the *q* component of the current will also be zero as well. This simplifies the equations of the active and reactive power to.

$$P = \frac{3}{2} E_d I_d \qquad\qquad Q = 0 \qquad (2.12)$$

Chapter 3. System design.

In this chapter, all the parameters of the components that are used in the following chapters are calculated (see Figure 3). To check the validity of these calculations, given Simulink/MATLAB files are used modifying the design parameters to satisfy the new power requirement [3].

This chapter is divided in two parts:

I. The first one contains the calculations needed to design the hardware and choose the appropriate components.

II. The second one contains the simulations in Simulink/MATLAB to verify the behavior of the system and if it follows the specifications and requirements.

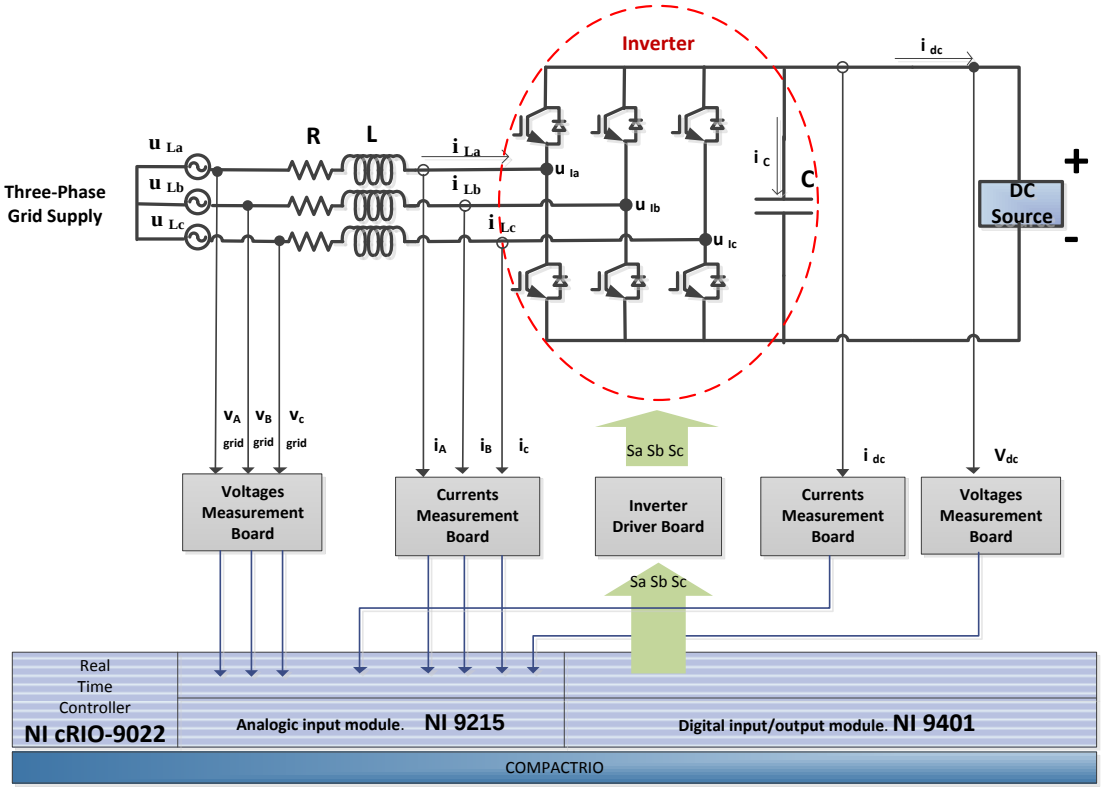


Figure 3: General view of the system scheme.

The design of the components of the charger starts from the desired power level for the system.

P_g=15 KW	$V_{LL(rms)}$= 400 V (line-to line)

3.1. Hardware design.

3.1.1. Minimum DC-link voltage.

The correct selection of the DC-link voltage needs to be done in order to assure a complete control of the inverter. The voltage should be high enough to polarize the diodes in inverse mode (Figure 4) but always taking into account the limit of the inverter, in our case the semi teach IGBT's.

Following the specifications of our inverter, the voltage should be less than 750 V [9].

$$V_{DC}<750\ \text{V} \tag{3.1}$$

To polarize a diode in inverse mode, the DC voltage has to be higher than the peak value of the diode rectifier line-to-line voltage [4].

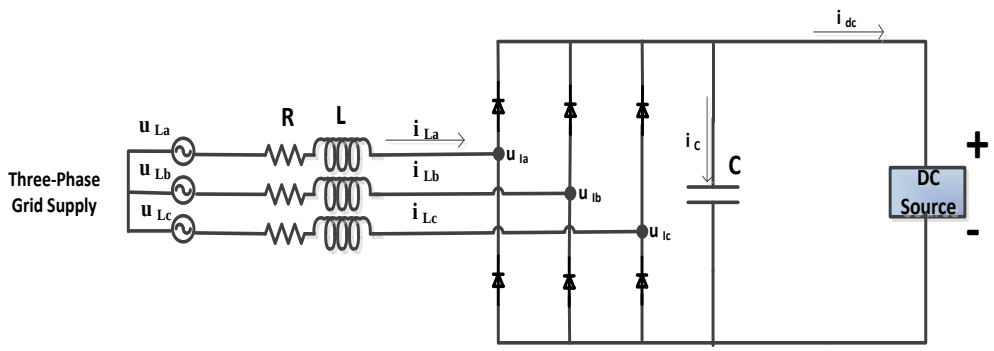


Figure 4: Three phase diode rectifier.

$$V_{DC} > \sqrt{2}V_{LL(rms)} = \sqrt{2}.\sqrt{3}.V_{LN(rms)} \tag{3.2}$$

Note that the maximum line-to-line voltage in the rectifier will depend on the control mode of the inverter, in this case sinusoidal pulse width modulation. In this control, three-phase reference voltages are compared with a triangular wave with fixed amplitude and frequency (Figure 5). Each comparator will obtain the switching pattern for each leg of the inverter.

Depending on the switching state, the positive or negative half of the V_{DC} will be applied in the inverter, this is very important to fix the lower limit for the DC bus. [10]

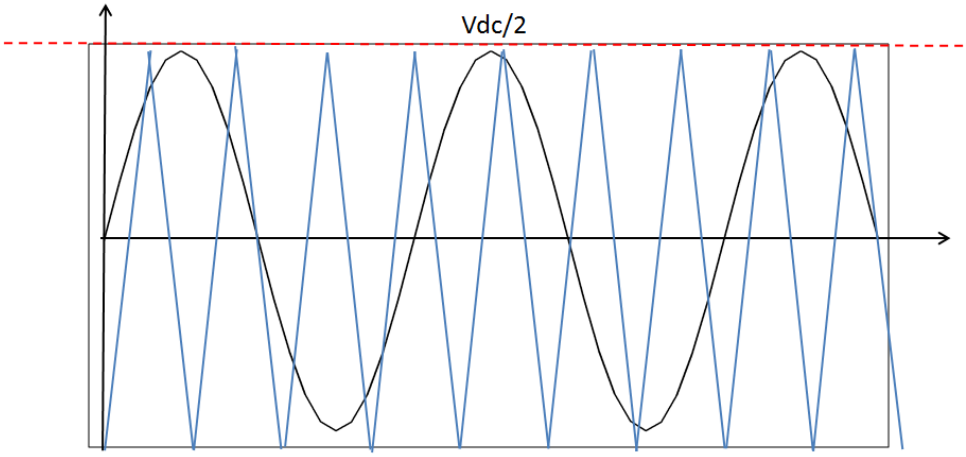


Figure 5: Maximum reference value achievable in PWM.

Using Sinusoidal pulse with modulation, the minimum DC voltage becomes the DC voltage that is provided by the diode rectifier and the maximum DC voltage is established from the limitations of the inverter as shown in Figure 6.

$$V_{LN(peak)} = \frac{V_{DC}}{2}$$
$$\frac{V_{LL(rms)}}{\sqrt{3}}\sqrt{2} = \frac{V_{DC}}{2} \tag{3.3}$$
$$V_{DCmin} > 2\,V_{LN(peak)} = \frac{2\sqrt{2}}{\sqrt{3}} V_{LL(rms)} = 653.19\,V$$

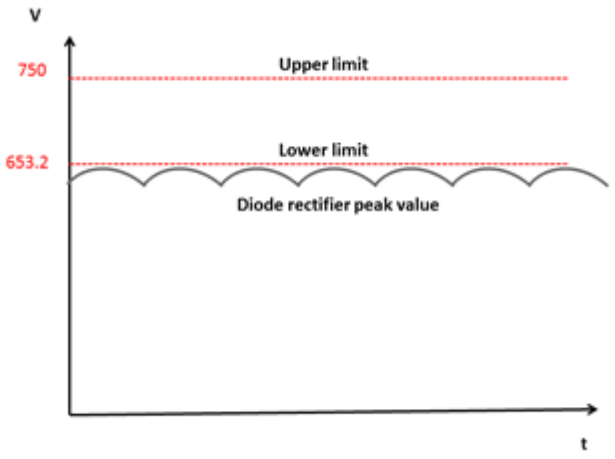


Figure 6: Range of DC bus voltage between the diode rectifier behavior and inverter limit.

V_{DC}=700 V

3.1.2. Load resistance.

For the first approximation, in this thesis a resistor is going to be used as load on the DC bus. After the implementation, a DC source is used to have a model closer to a real battery. The load resistance that is needed to fulfill the power specifications depends on the selected DC voltage. It can be calculated in two different ways.

Considering the inverter has no losses.

$$P_g = P_{load} = \frac{v_{dc}^2}{R_{load}}$$
$$R_{load} = \frac{v_{dc}^2}{P_g} = \frac{700^2}{15000} = 32.66\Omega \quad (3.4)$$

Taking into account the performance of the inverter and supposing a value of 95-98 % for performance of an auto switched inverter with IGBT technology [9].

$$P_{load} = \frac{v_{dc}^2}{R_{load}}$$
$$R_{load} = \frac{v_{dc}^2}{P_{load}} = \frac{700^2}{0.95 \cdot 15000} = 34.38\Omega \quad (3.5)$$

Finally, for simplicity, a 33Ω resistor is chosen.

3.1.3. Line inductance and ripple analysis.

Following the Chapter 11 in reference [4], a minimum value of DC voltage is defined taking into consideration the inductance. This formula is valid in our case due to the amplitude invariance transformation.

The DC bus voltage has to be high enough to compensate the voltage drop in the inductance. It can be checked that if the inductance value is zero the formula is equivalent to (3.3).

$$V_{DC} > \sqrt{4[E_m^2 + (\omega Lid)^2]}$$
$$L < \frac{\sqrt{\frac{V_{DC}^2}{4} - E_m^2}}{\omega id} \quad (3.6)$$

Based on the d-q transformations, equations for active and reactive power are obtained.

$$P = \frac{3}{2} Re\{v^{dq}(i^{dq})^*\} = \frac{3}{2}(v_d i_d + v_q i_q) = \frac{3}{2}(E_d i_d + E_q i_q)$$
$$Q = \frac{3}{2} Im\{v^{dq}(i^{dq})^*\} = \frac{3}{2}(v_q i_d - v_d i_q) = \frac{3}{2}(E_q i_d - E_d i_q) \quad (3.7)$$

In our system a unitary power factor is demanded so a decoupled current control design will be achieved to obtain $i_q = 0$. Using this control, the active and reactive power can be written as [3]:

$$P = \frac{3}{2} E_d i_d$$
$$Q = 0 \quad (3.8)$$
$$id = \frac{2}{3E_g} P_g = 30.61 \text{ A}$$

This value is confirmed in the simulations of the system.

According with the grid voltage specifications, E_g is calculated.

$$E_g = \sqrt{2}\frac{400}{\sqrt{3}} = 326.6\, V \text{ (Phase-to-Ground)} \quad (3.9)$$

Finally, in order to obtain the limit for the inductance, the initial formula is used.

$$L < \frac{\sqrt{\frac{V_{DC}^2}{4} - E_g^2}}{\omega id}$$
$$L < \frac{\sqrt{\frac{700^2}{4} - 326.6^2}}{2\pi 50 \times 30.61} \quad (3.10)$$
$$L < 13mH$$

The minimum value that can be used for the inductance depends on the maximum current ripple for the system. A series of simulations of the complete system have been carried out with different values of the inductance to analyze the current ripple.

Using 1mH, as it is a very common value for Boost converters, the current ripple is shown in the following simulation figure (Figure 7).

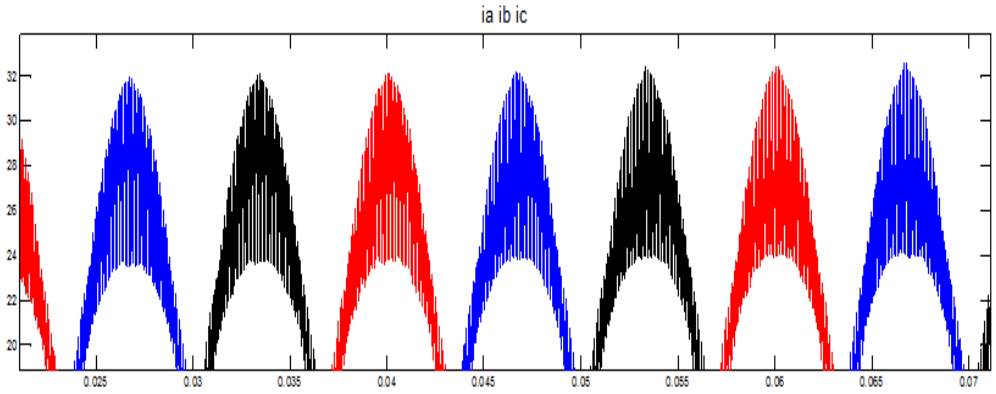


Figure 7: Current ripple with L= 1mH.

$$I_{Ripple} = 31{,}8 - 23{,}5 = 8{,}3\ A \tag{3.11}$$

Theoretically, the current ripple is calculated using the equation of the voltage drop in an inductance.

$$\Delta i_L = \frac{\frac{V_{DC}}{2} - \frac{U}{\sqrt{3}}}{Lf} \cdot D = \frac{\frac{700}{2} - \frac{400}{\sqrt{3}}}{Lf} \cdot 0{,}5 = 6A \tag{3.12}$$

Using a value for the inductance of 2mH, according to the simulation results (Figure 8) the current ripple is also calculated.

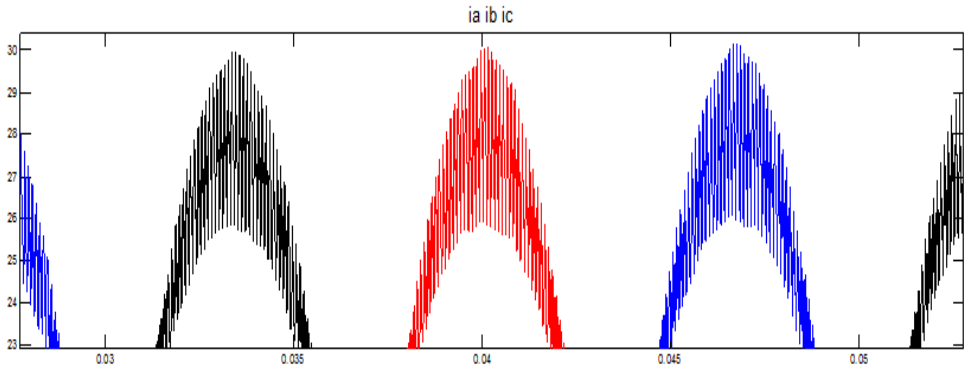


Figure 8: Current ripple with L=2mH.

$$I_{Ripple} = 29{,}7 - 25{,}4 = 4{,}3\ A \tag{3.13}$$

Theoretically, the current ripple is calculated using the equation of the voltage drop in an inductance.

$$\Delta i_L = \frac{\frac{V_{DC}}{2} - \frac{U}{\sqrt{3}}}{Lf} \cdot D = \frac{\frac{700}{2} - \frac{400}{\sqrt{3}}}{Lf} \cdot 0{,}5 = 3A \tag{3.14}$$

According to the simulation results shown in Figure 9 , the current ripple using a 3mH inductance is calculated.

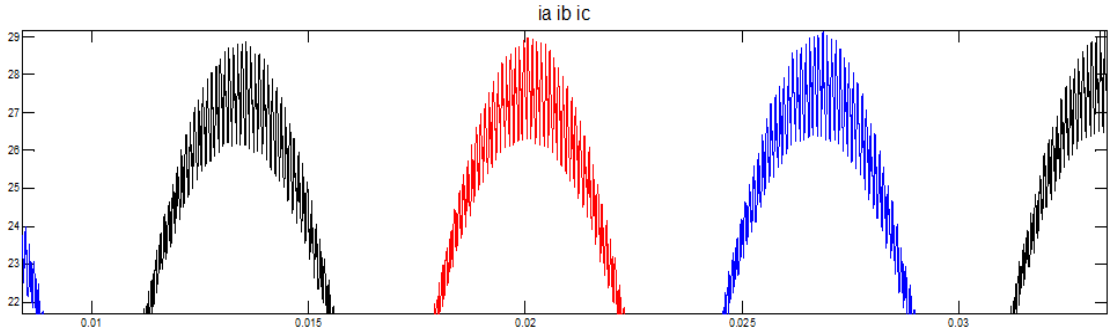


Figure 9: Current ripple with L= 3mH.

$$I_{Ripple} = 29 - 26{,}4 = 2{,}6\ A \tag{3.15}$$

Theoretically, the equation of the voltage drop in an inductance is used to calculate the current ripple.

$$\Delta i_L = \frac{\frac{V_{DC}}{2} - \frac{U}{\sqrt{3}}}{Lf} \cdot D = \frac{\frac{700}{2} - \frac{400}{\sqrt{3}}}{Lf} \cdot 0{,}5 = 1{,}98A \tag{3.16}$$

Finally, referencing to the acceptable current ripple in Boost converters applications, 3 mH has been chosen as inductance value.

3.1.4. Capacitance of the inverter.

According to the inverter specifications, the filtering capacitors are electrolytic capacitors with an individual value of 2200µF/400V, two connected in series and two in parallel.

For all the calculations the equivalent capacitance of the complete DC bus is used [11].

$$C = 1100\mu F/800V$$

3.1.5. Switching frequency used in pulse width modulation.

A fixed switching frequency is used in Voltage Oriented Control in order to have an easier design and to achieve a lower sample frequency. To minimize the effect of the harmonics on system performance, the PWM frequency should be high. But a higher frequency also means higher switching losses, so an intermediate value is used.

$$fsw = 10\ KHz$$

Resume template
P_{IN}=15 KW
$V_{LL(rms)}$= 400 V (line-to line)
V_{DC}=700 V
R_{load}=33Ω
$L = 3mH$
$C = 1100\mu F/800V$
$fsw = 10\ KHz$

Table 1: Design parameters conclusion.

3.1.6. Temperature limitation for the inverter.

It is very important to know what the temperature limit of the junction is.

The junction temperature T_{jmax} is usually 150,° but for safety reasons 125° is more appropriate value to consider. As mentioned before, an inverter using the IGBT technology has efficiency of 95-98%.

Losses have to be dissipated to maintain components in a safe range of temperatures. This is the reason why it is necessary to calculate the equivalent thermal impedance of the system and check if the temperature is lower than the maximum temperature on the junction.

The thermal impedance can be modeled as a capacitor and a resistance, as shown in Figure 10.

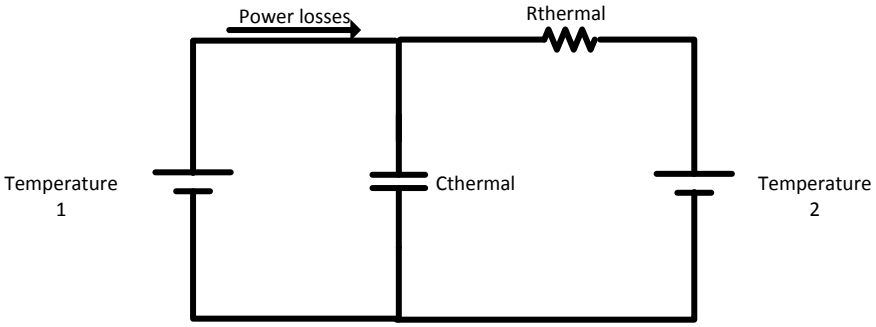


Figure 10: Equivalent thermal circuit.

Following the impedance values given in the datasheet of our inverter, it is possible to check that the value changes over time, but after 0.5 s of transient state, the capacitor value is neglected and only the resistance is taken into consideration. For nominal operation of the inverter the value of the thermal resistance is 0.4 K/W (see Figure 11).

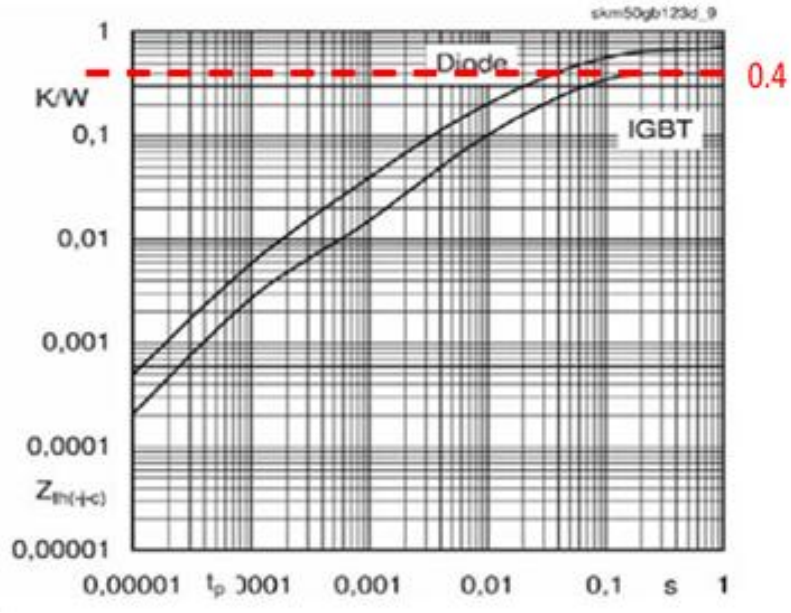


Figure 11: Thermal resistance VS time.

In the worst case scenario the inverter has efficiency of 95%, supposing steady state and that the 6 IGBT's produce the same losses, the temperature in the junction can be calculated as follows.

$$Tj=T_{ambient}+R_{th}\cdot P_{losses}$$

$$\Delta T=\frac{0.4\cdot 15000\cdot 0.05}{6}=50K \tag{3.17}$$

$$Tj=20^{o}+50^{o}=70^{o}$$

In order to have a more accurate estimation of the losses, the conduction losses and the switching losses are calculated following the expressions from datasheet [9].

The switching losses appear during the commutation due to the switching patterns.

The switching losses (on+off) for a 3 phase inverter, using the graph in Figure 12 are calculated.

$$P_{ON+OFF(IGBT)}=\frac{\sqrt{2}Irms}{\pi}\cdot fsw\cdot U\cdot K$$

$$P=fsw\cdot(Eon+Eoff)) \tag{3.18}$$

$$P=10kH(2,6+3,4)=60W$$

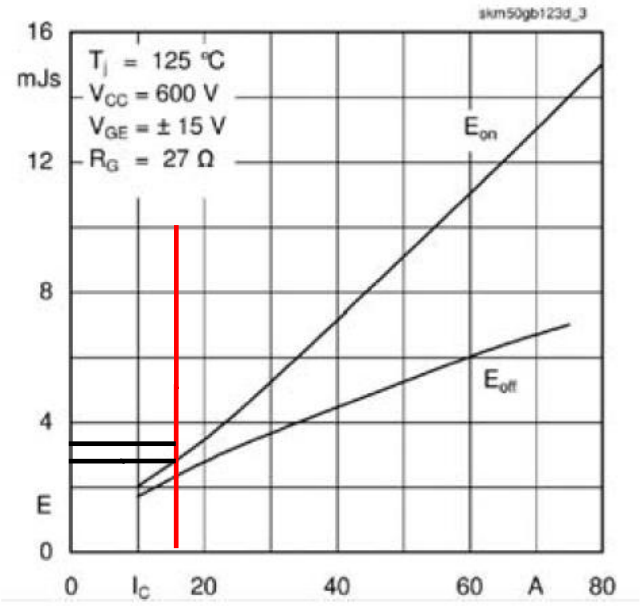


Figure 12: Switching losses from the datasheet of the inverter.

The conduction losses in an IGBT are the result of the product of the current and the voltage (collector-emitter) during the conduction period.

The conduction losses for IGBT´s in a 3 phase inverter can be estimated by.

$$P_{cond(IGBT)} = \frac{1}{2} \cdot \left(\frac{1}{\pi} \cdot Vceo + r \cdot \frac{I^2}{4} \right) + m \cdot cos\varphi \cdot (Vceo \cdot \frac{I}{8} + \frac{rI^2}{3\pi}) \quad (3.19)$$

Where *m* is a degree of modulation and V_{ce0} and *r* are determined graphically from the datasheet curves. This depends on the application, and can be calculated using the rms value of the current. The parameters for the conduction losses are calculated, using Figure 13.

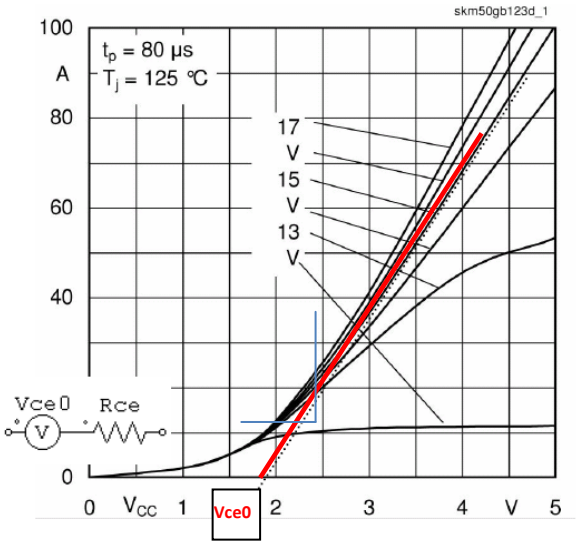


Figure 13: Conduction losses from the datasheet of the inverter

$$I_{rms}=\frac{29,7}{\sqrt{3}}=17,14A$$

$$Vce0=1,9V \quad (3.20)$$

$$r=\Delta u/\Delta I=1V/30A=0,03\Omega$$

$$m=\frac{\frac{Urms}{\sqrt{3}}}{\frac{Udc}{2}} = \frac{\frac{400}{\sqrt{3}}}{\frac{700}{2}} = 0,659$$

$$Pcond=4,703W$$

$$Plosses=64,7W \quad (3.21)$$

$$\Delta T=0.4 \cdot 64,7=25,88K$$

$$Tj=20^{o}+25,88^{o}=45,88^{o}$$

This temperature in the junction is much lower than the limit given in the data sheet. For this reason, the inverter can be used in the setup for this power level.

3.1.7. Measurement cards design.

In order to develop the control system, certain measures of voltages and currents are necessary.

3.1.7.1. Voltage measurement cards.

For this purpose, voltage transducers UMAT2 are used. They have three channels to measure three different signals with a common neutral point. The three channels of one of the voltage transducers are used to measure the three-phase voltage and only one channel of another voltage transducer is used to measure the DC voltage [1].

The transducer is an electronic device that converts energy from one form to another. In our case, the transducer UMAT2 is used as a voltage divider to give a low voltage output that our control system can manage.

The compactRIO system is an electronic system made of modules. This is very useful and can be used for different applications and purposes. In this case, the corresponding module with analog inputs has a range of ±10 V input ranges [12].

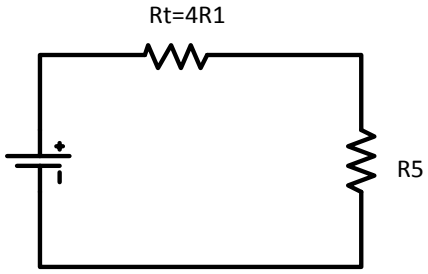


Figure 14: Voltage divider circuit.

For the transducer measuring the three-phase voltage, the maximum voltage phase-to-ground that can be measured is 327V, so the calculations are set taking into account this value.

$$U_1=\pm 400V$$

$$U_2=\pm 10V \tag{3.22}$$

$$R_t=\sum R_1+R_2+R_3+R_4=4\cdot R_1$$

Applying the voltage divider formula, the ratio between both peak values is obtained.

$$\frac{U_2}{U_1} = \frac{R_5}{R_5+R_t} = 10V/400V = 0.025 \tag{3.23}$$

Standard values for resistors are chosen.

$$\begin{gathered} R_5{=}12\text{k}\Omega \\ R_1 = R_2 = R_3 = R_4 = 120\text{k}\Omega \end{gathered} \tag{3.24}$$

With these values, the voltage ratio is obtained.

$$\frac{U_2}{U_1}{=}\frac{R_5}{R_5+R_t}{=}0.02439 \tag{3.25}$$

For the transducer measuring the DC voltage, the voltage of 750 V is chosen as a maximum because it is the maximum DC voltage that the inverter can support.

$$\begin{gathered} U_1{=}\pm 750V \\ U_2{=}\pm 10V \\ R_t{=}\sum R_1 + R_2 + R_3 + R_4{=}4{\cdot}\, R_1 \end{gathered} \tag{3.26}$$

Applying the voltage divider formula, the ratio between both peak values is obtained.

$$\frac{U_2}{U_1}{=}\frac{R_5}{R_5+R_t}{=}10V/750V{=}0.01333 \tag{3.27}$$

Standard values for resistors are chosen.

$$\begin{gathered} R_5{=}13\text{k}\Omega \\ R_1 = R_2 = R_3 = R_4 = 240\text{k}\Omega \end{gathered} \tag{3.28}$$

With these values, the voltage ratio is obtained.

(3.29)

The error between the theoretical and the calculated value is 0.23%, which is sufficiently accurate.

Using this transducer, the maximum value of the DC voltage (750V) corresponds to 10.02V, which is within the range of measurement of the compactRIO module for analogic inputs [12].

3.1.7.2. Current measurement cards.

In the same way as with the voltage, transducers are used. These transducers are four LEM LA 50-S/SP1 are going to be used. This electronic device produces a voltage drop U_{meas} in a resistance R_{meas} because of the current I_2, which is proportional to the current measured in a factor that depends on the number of turns [1].

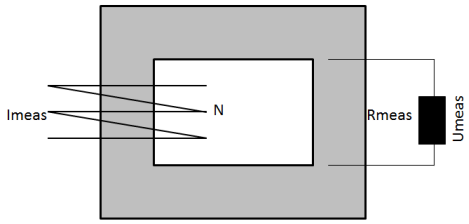


Figure 15: LEM scheme

Using an identical compactRIO module for analogical inputs with a range of ±10 V and the datasheet of the transducer, the relationship between currents is obtained.

$$\frac{I_{meas}}{I_2}=\frac{2000}{N} \tag{3.30}$$

where N is the number of turns in the LEM device. By choosing a number of turns that provides a good accuracy, it is possible to calculate the value of R_{meas}.

$$\begin{gathered} \text{N=10 turns} \\ \frac{I_{meas}}{I_2}=200 \\ I_{meas} = 200I_2 = 200\frac{U_{meas}}{R_{meas}} \\ R_{meas} = 40\Omega \end{gathered} \tag{3.31}$$

Selecting this value of R_{meas} , the relationship of the output voltage with the current measured is $\frac{1}{5}$. This is an appropriate value for our system because the maximum value of the current is ±50A, which corresponds to an output voltage of ±10 V. This is the exact range of the National Instruments analogic input module which is used [12].

3.1.8. Filter design.

Filters are very important in data acquisition systems to remove the undesirable frequencies from the signal that is being measured. To achieve this, analog filters are used before the analog to digital converter [13].

3.1.8.1. Voltage filter.

Operating with a switching frequency of 10kHz, a sample frequency of 1kHz is enough to sample the 50 Hz voltages because this is more than the double of frequency and it is sufficient to keep the desired frequency below the Nyquist limit [14].

A cut-off frequency of 1kHz in the low pass filter is enough for the voltage before the digital conversion. Taking into account the anti aliasing effect, the chosen frequency is 2kHz [15].

The design of the passive first order filter is completed using the well-known formula.

$$fc = \frac{1}{2\pi RC} \tag{3.32}$$

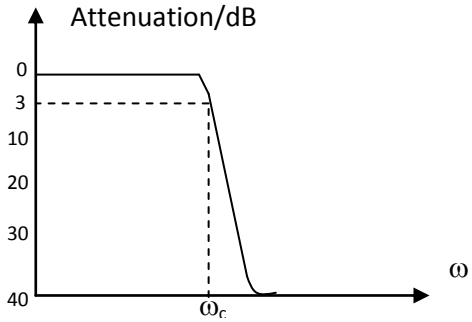


Figure 16: Attenuation scheme using a low pass filter.

Making the calculations and choosing a capacitor of C=10nF, the resistor value is calculated as R=7,95kΩ. Finally, for simplicity, R=10 kΩ is chosen.

3.1.8.2. Current filter.

Calculations are done in the same way as for the voltage filter but using a sampling frequency of 5kHz. Choosing a capacitor of C=10nF, the resistor value obtained is R=3,18 Ω . Finally, selecting a standard value, R=3,3 kΩ is chosen.

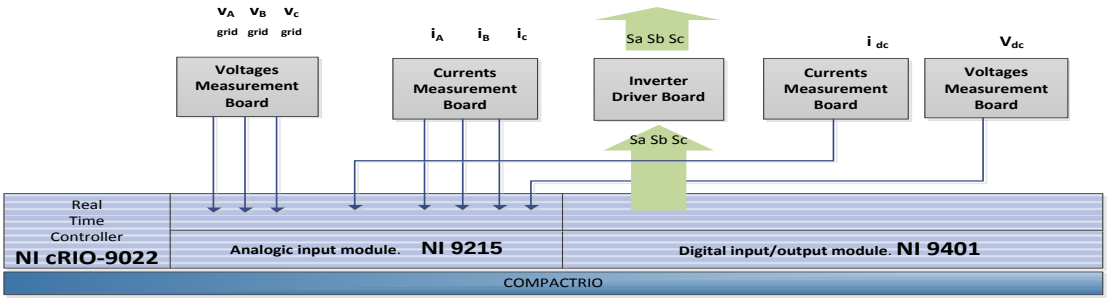


Figure 17: Data communication between CompactRIO and the system.

Signal	Measure range	Input CRIO range	Units	Sampling Frequency
Ua	± 400	± 10	V	1 kHz
Ub	± 400	± 10	V	1 kHz
Uc	± 400	± 10	V	1 kHz
Ia	± 50	± 10	V	5 kHz
Ib	± 50	± 10	V	5 kHz
Ic	± 50	± 10	V	5 kHz
Udc	750	± 10	V	1 kHz
Idc	± 50	± 10	V	5 kHz

Table 2: Range of measurements and sample rate.

Voltage measurement board		
$R5$	12	$K\Omega$
$R1=R2=R3=R4$	480	$K\Omega$
$Ratio\ of\ conversion$	0.02439	

Table 3: Voltage measurement board.

Voltage DC measurement board		
$R5$	13	$K\Omega$
$R1=R2=R3=R4$	240	$K\Omega$
$Ratio\ of\ conversion$	0.01336	

Table 4: DC voltage measurement board.

Current measurement board		
N	10	$turns$
$Rmeas$	40	Ω
$Ratio\ of\ conversion$	0.2	

Table 5: Current measurement board.

Voltage antialiasing filter		
C	10	nF
R	10	$k\Omega$
$frequency$	2	kHz

Table 6: Voltage antialiasing filter.

Current antialiasing filter		
C	10	nF
R	$3,3$	$k\Omega$
$frequency$	5	kHz

Table 7: Current antialiasing filter.

3.2. MATLAB simulations.

In order to check the validity of all the calculated parameters of the system, simulations in continuous mode and in discrete mode have been carried out.

3.2.1. Continuous simulations.

In all the simulations the behavior after a DC voltage step is checked. As shown for the currents results in Figure 18, the current values for the desired power level are around 35 A. This quantity is much lower than the limit of the inverter, which is 50A. In Figure 19, the reference voltages are shown before saturation as well as after saturation referred to d-q axis. Besides, the ABC reference voltages after anti transformation are shown in the third graph.

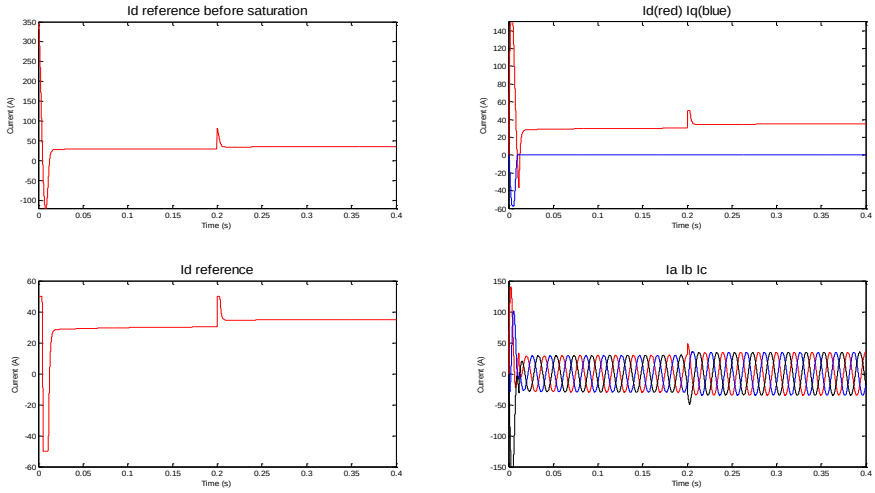


Figure 18: Currents in continuous simulation

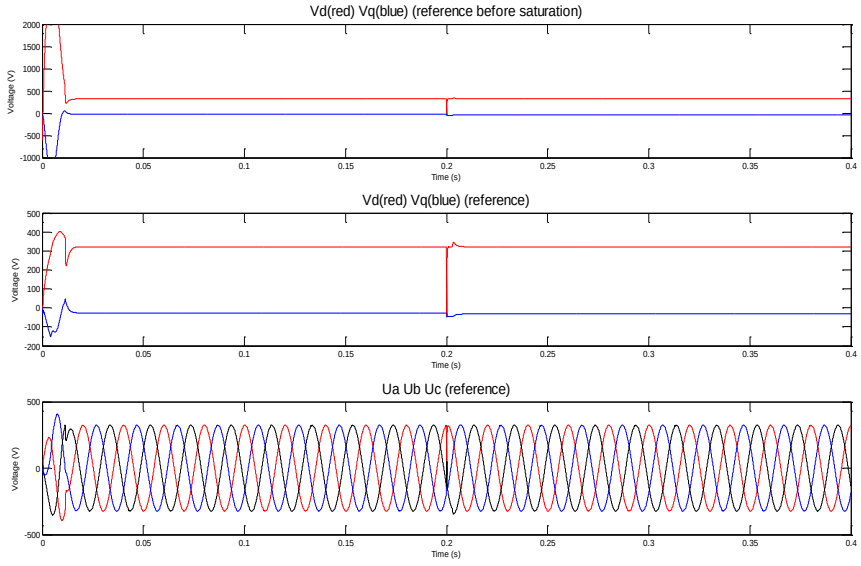


Figure 19: Voltages in continuous simulation

In order to verify the behavior of the system under a step variation in the DC voltage, the current referred to d-q axis is shown in Figure 20.

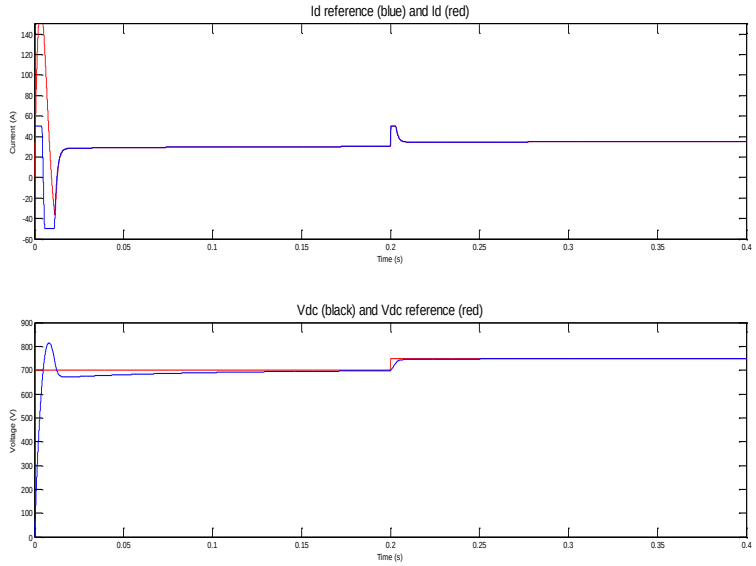


Figure 20: System behavior after DC voltage step.

3.2.2. Discrete simulations.

Carrying out an equivalent simulation with a step in the DC voltage, the current is limited to a value of 50 A during the transient state after the perturbation, as can be seen in Figure 21.

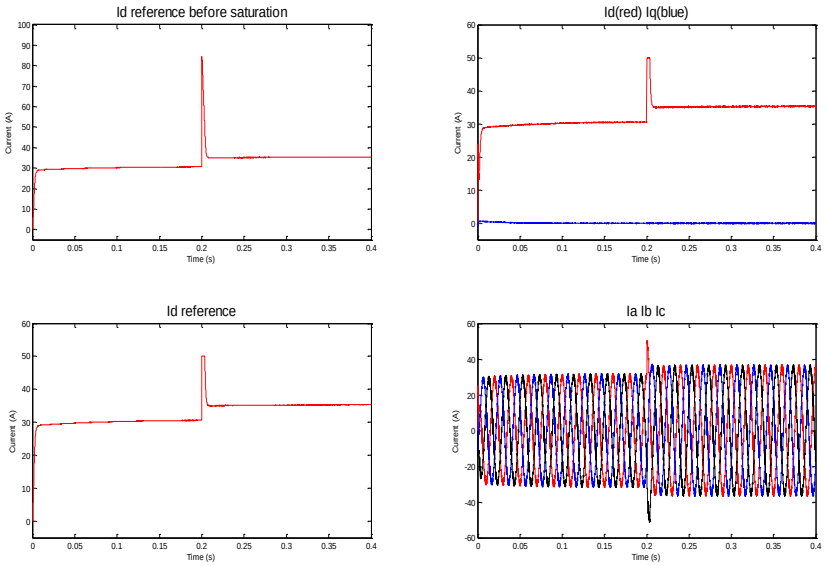


Figure 21: Currents in discrete simulation.

On Figure 22, the reference voltages after Park´s transformation are shown.

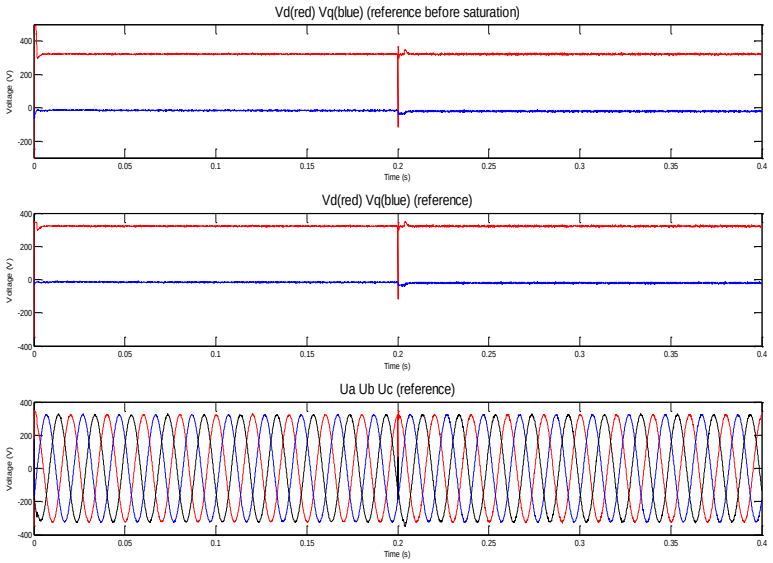


Figure 22: Voltages in discrete simulation.

The last figure of the simulations, Figure 23, shows the DC voltage and the d axis current. A good and quick response is observed because of the little integration time that was used (Ts=1*10-5s).

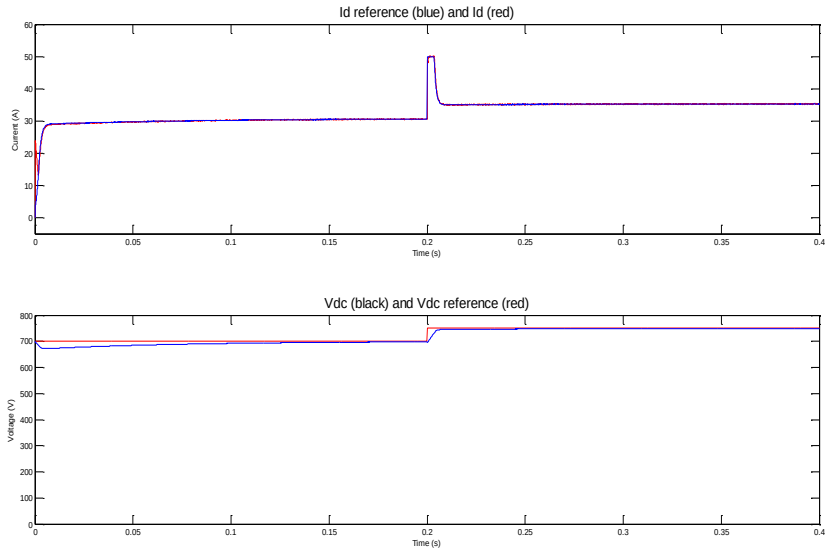


Figure 23: System behavior after DC voltage step.

Chapter 4. Software development.

In this chapter, all the simulations of the system and the control of the inverter are developed using Labview, which is the system design software created by National Instruments. In the first part, all the blocks used in the simulation are described in detail. In the second part, the running of the program is explained from the starting up to the steady state.

4.1. Complete system and description of the simulation blocks.

The complete system is shown in Figure 24, which contains all the simulation elements from the creation of the sinusoidal inputs to the rectifier model.

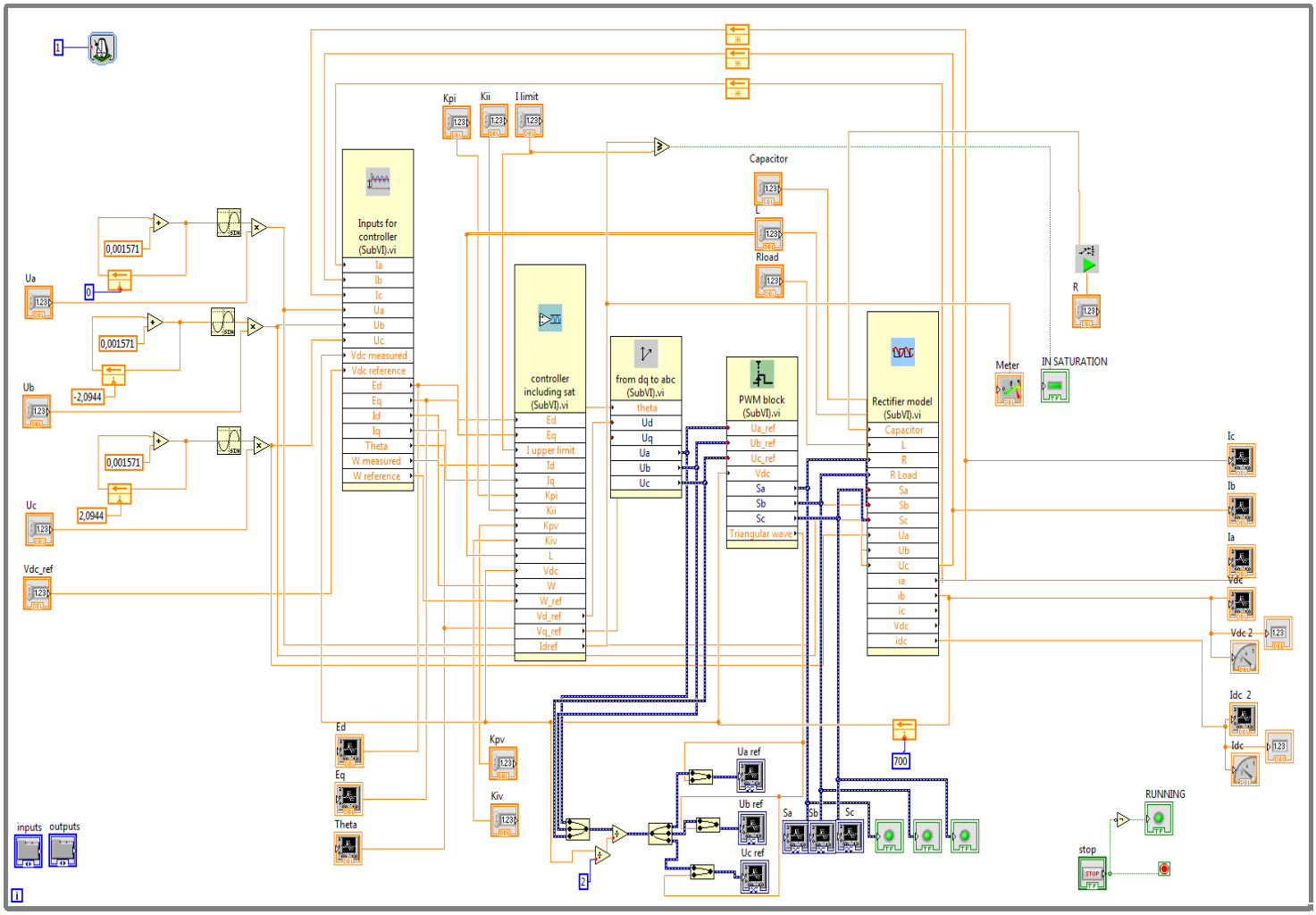
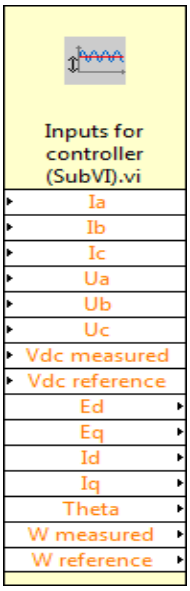


Figure 24: Overall view of all the simulation system.

4.1.1. Inputs for the controller block.



Inputs	*Outputs*
Ia	*Ed*
Ib	*Eq*
Ic	*Id*
Ua	*Iq*
Ub	*Theta*
Uc	*Wmeasured*
Vdc measured	*Wreference*
Vdc reference	-

Table 8: Inputs and outputs for Inputs for the controller subVI.

Figure 25: Inputs for controller block.

The main function of this block is to provide the appropriate inputs for the controller. For this purpose, it uses as inputs the currents and voltages of the system. The currents that are flowing through the system and the DC voltage through the load are calculated with a model of the rectifier and then used as inputs again in a loop. The three sinusoidal voltage waves have been created point by point in a discrete way (Figure 26). To do that, the phase of each wave is increased for every loop of the whole system and, by multiplying the sine of this angle by the amplitude, the sinusoidal wave is obtained. The initialization for the phase of Ub is –2,0944 radians, which is $-\frac{2\pi}{3}$, and, doing the same for Uc, the initial value of the phase is 2,0944 radians, which is $\frac{2\pi}{3}$.

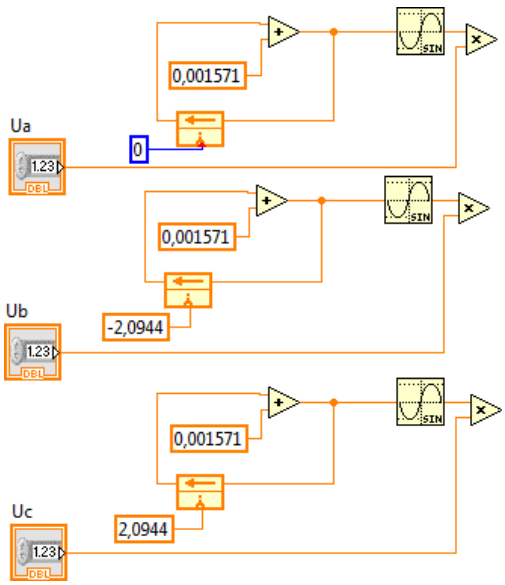


Figure 26: Generation of three sinusoidal waves of voltage.

Inside the block different operations are made. The PLL, the "W measured" and "W reference" calculations, and the DQ transformations are achieved as shown in Figure 27.

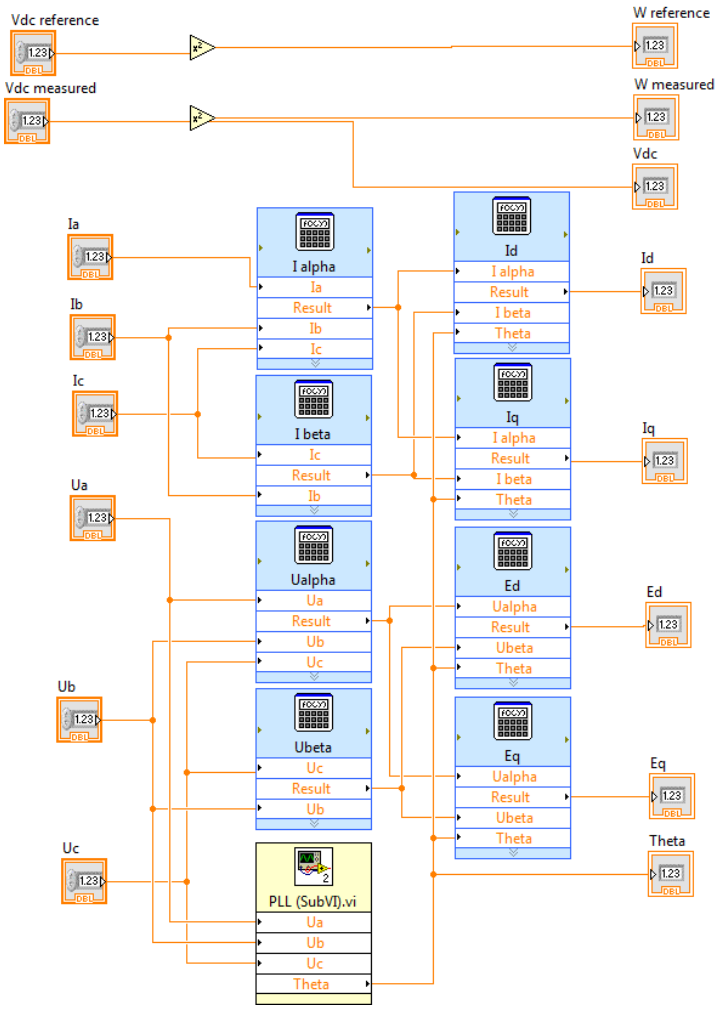


Figure 27: Inputs for the controller block, inside view.

The Phase Locked Loop (PLL) is developed as a numeric method to calculate the electric angle of the three phase system, which is necessary for the d-q transformation following the Park´s equations in chapter 2. According to [7] and [16] the PLL is designed.

$$\dot{\omega} = \gamma_1 \varepsilon$$
$$\dot{\theta} = \omega + \gamma_2 \varepsilon \tag{4.1}$$

where γ_1 and γ_2 are the gain parameters (ki and kp respectively) of the PI controller, which uses Eq as the error signal since a d-oriented control is used. In order to calculate gain parameters, the equations 4.2 are used.

$$\gamma_1 = \frac{\rho^2}{\hat{E}_g}, \qquad \gamma_2 = \frac{2\rho}{\hat{E}_g}, \qquad \hat{E}_g = \sqrt{\hat{E}_d{}^2 + \hat{E}_q{}^2} \tag{4.2}$$

where ρ is the bandwidth of the PLL in rad/s (in this case a frequency of 20 Hz is used) and $\hat{E}_g$ is the grid voltage modulus. The PLL scheme is presented in Figure 28.

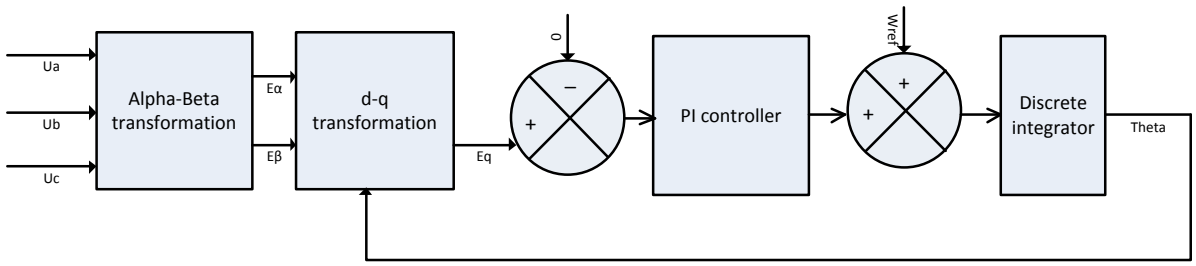


Figure 28: PLL theoretical implementation scheme.

Following the steps mentioned before, the model is implemented using two discrete integrators, one for the PI controller and the other one to obtain the electric angle from the angular speed. The integration step used in the program is 0,001s as can be checked in the Labview scheme shown in Figure 29.

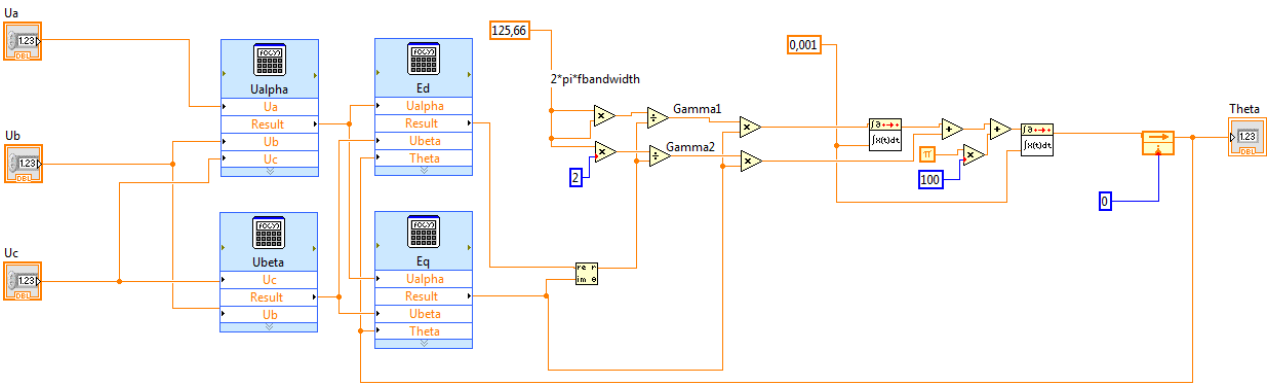


Figure 29: PLL Implementation in Labview.

4.1.2. Controller block.

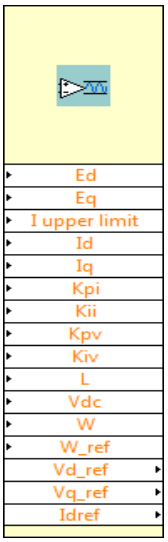


Figure 30:controller block.

Inputs	Outputs
Ed	Vd_ref
Eq	Vq_ref
I upper limit	Idref
Id	-
Iq	-
Kpi	-
Kii	-
Kpv	-
Kiv	-
L	-
Vdc	-
W	-
W_ref	-

Table 9: Inputs and outputs for the controller subVI.

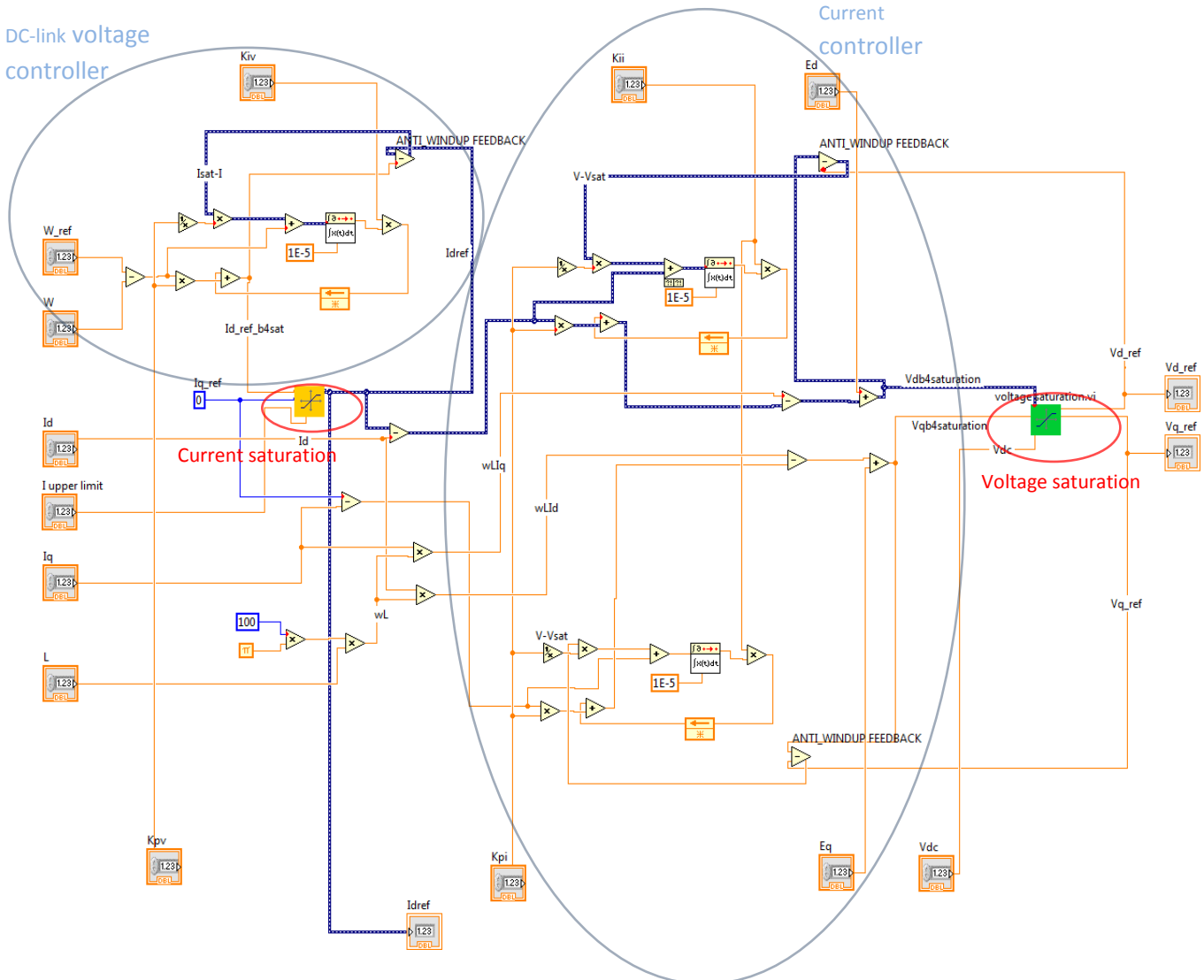


Figure 31: Inside view of the controller block.

4.1.2.1. DC-link voltage controller.

The ultimate goal of the controller is to obtain a desired voltage in the DC-link. By measuring the instantaneous voltage and comparing its square value with the square value of the reference voltage, an error that is fed to the controller is obtained.

$$\varepsilon = W_{ref} - W = V_{dc\,ref}^2 - V_{dc}^2 \tag{4.3}$$

By implementing a PI control, a reference current for the system, id^*, is calculated [3].

$$I_d{}^* = k_p\varepsilon + k_i\frac{\varepsilon}{s} \tag{4.4}$$

The PI control parameters are calculated as detailed in [2].

$$K_{pv} = \frac{\alpha_v C}{3E_m} \quad and \quad K_{iv} = 0{,}01 \tag{4.5}$$

where we choose α_v two decades smaller than the switching frequency $\alpha_v = \frac{2\pi f_{sw}}{100}$.

If there is a considerable difference between the reference DC voltage and the measured DC voltage, this results in an unacceptably high reference current calculated by the controller, which has to be limited. Therefore a saturation block is used.

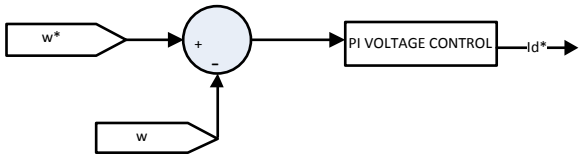


Figure 32: DC –link voltage controller

- ***Current saturation.***

In order to protect the inverter, which maximum rms current allowed is 30A, there is a need to add a limitation. The saturation control is carried out with the current Id module in such a way that the upper and the lower limit are controlled at the same time.

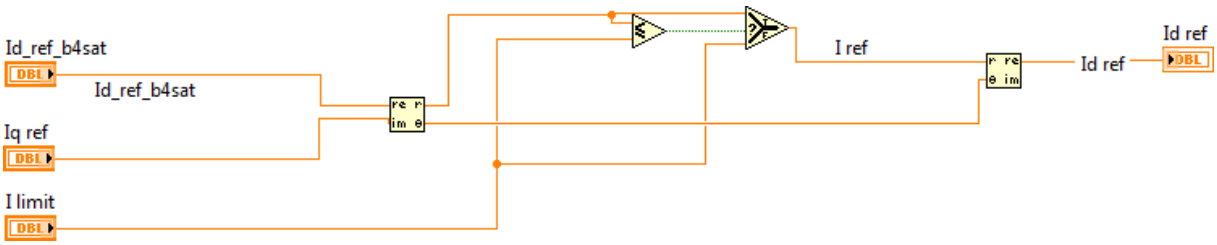


Figure 33: Implementation of the current saturation.

- ***Anti-windup Integrator.***

In practically all controllers, there are nonlinear effects that must be accounted to achieve a good and realistic control. Windup is a phenomena caused by the interactions between integral action and saturations [17]. To avoid the integrator of the control calculating a high current over the limit, the difference between the current calculated and the limit is fed back to reduce the error going inside the integral part of the controller. The new error is $\bar{\varepsilon}$ and the current calculated by the PI control is referred as $\overline{I_d^*}$. The new equations of the PI control with anti-windup loop are given below [3].

$$\bar{\varepsilon} = \varepsilon + \frac{\overline{I_d^*} - I_d^*}{k_p}$$
$$I_d{}^* = k_p\varepsilon + k_i\frac{\bar{\varepsilon}}{s} \qquad (4.6)$$

The complete scheme of the DC-link voltage controller implemented in Labview is shown in Figure 34.

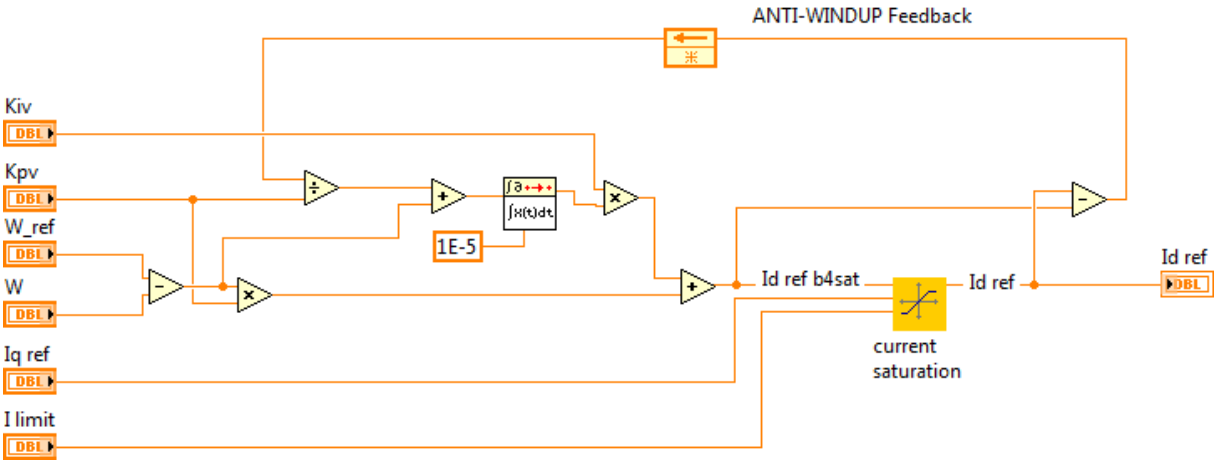


Figure 34: DC-link voltage controller.

4.1.2.2. Current controller.

Once a DC-link voltage control is established, the reference current I_d^* , which is used to control the DC voltage, is calculated. In addition, due to the unit power factor operation of the system, the q-axis reference current I_q^* is set to zero. To obtain these reference currents in the system, a current control is performed, resulting in a reference voltage which is calculated in the dq-axis system. The implementation of the controller is done in two PI control loops, one for each component of the current, I_d^* and I_q^*. The outputs of the two PI controls are $V_d{}^*$ and $V_q{}^*$ respectively. The components of this reference voltage are calculated using [3].

$$V_d{}^* = E_d - k_p\varepsilon_d - k_i\frac{\varepsilon_d}{s} + \omega L I_q \qquad \text{being} \quad \varepsilon_d = I_d{}^* - I_d$$
$$V_q{}^* = E_q - k_p\varepsilon_q - k_i\frac{\varepsilon_q}{s} - \omega L I_d \qquad \text{being} \quad \varepsilon_q = I_q{}^* - I_q \qquad (4.7)$$

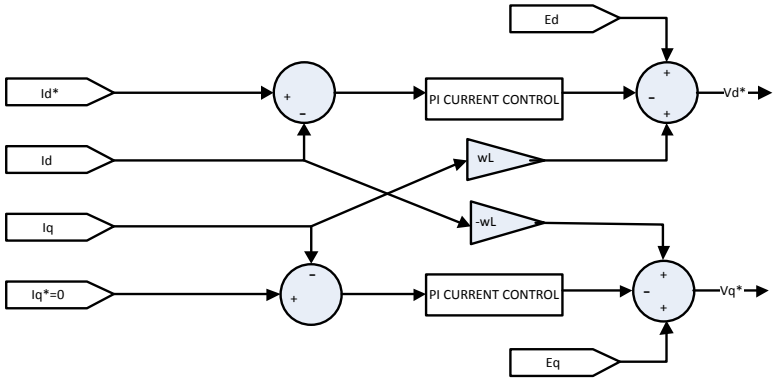


Figure 35: Current controller block diagram.

The PI control parameters are calculated as detailed in [2].

$$K_{pi} = \alpha_i L \quad and \; K_{ii} = \alpha_i R \tag{4.8}$$

where we choose α_i a decade smaller than the switching frequency $\alpha_i = \frac{2\pi f_{sw}}{10}$.

As in the case of the DC-link voltage controller, a saturation block is needed to keep the outputs in a defined range.

- ***Voltage saturation.***

As explained in the chapter 2.1., using a sinusoidal PWM, the maximum reference value that can be used is $V_{dc}/2$ [18]. Therefore, the saturation block calculates the modulus of the reference voltage and compares it with $V_{dc}/2$. In case the value of the reference voltage is higher, it is limited to $V_{dc}/2$. The components $V_d{}^*$ and $V_q{}^*$ after saturation are then recalculated using the original phase of the reference voltage, as shown in Figure 36.

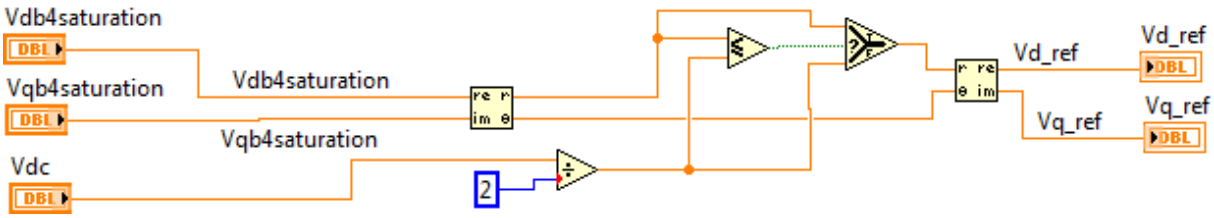


Figure 36: Voltage saturation block.

- ***Anti-windup Integrator.***

As explained for the DC-link voltage controller, there is a risk of obtaining a too high reference voltage at the output of the controller due to the action of the integrator. To avoid this uncontrollable increase of the voltage an integrator with anti-windup is used. The difference

between the voltage calculated by the Pi controller and the voltage limit is fed back to the integrator to reduce the value of the output reference voltage. The equations of the components of the reference voltage with an anti-windup integrator are obtained using equations from [3]:

$$V_d{}^* = E_d - k_p\varepsilon_d - k_i\frac{\overline{\varepsilon_d}}{s} + \omega L I_q \qquad \text{being} \quad \varepsilon_d = I_d{}^* - I_d \quad \text{and} \quad \overline{\varepsilon_d} = \varepsilon_d + \frac{V_d{}^* - \overline{V_d{}^*}}{k_p}$$
$$V_q{}^* = E_q - k_p\varepsilon_q - k_i\frac{\overline{\varepsilon_q}}{s} - \omega L I_d \qquad \text{being} \quad \varepsilon_q = I_q{}^* - I_q \quad \text{and} \quad \overline{\varepsilon_q} = \varepsilon_q + \frac{V_q{}^* - \overline{V_q{}^*}}{k_p} \qquad (4.9)$$

The complete scheme of the current controller with an anti-windup integrator implemented in Labview is presented in Figure 37.

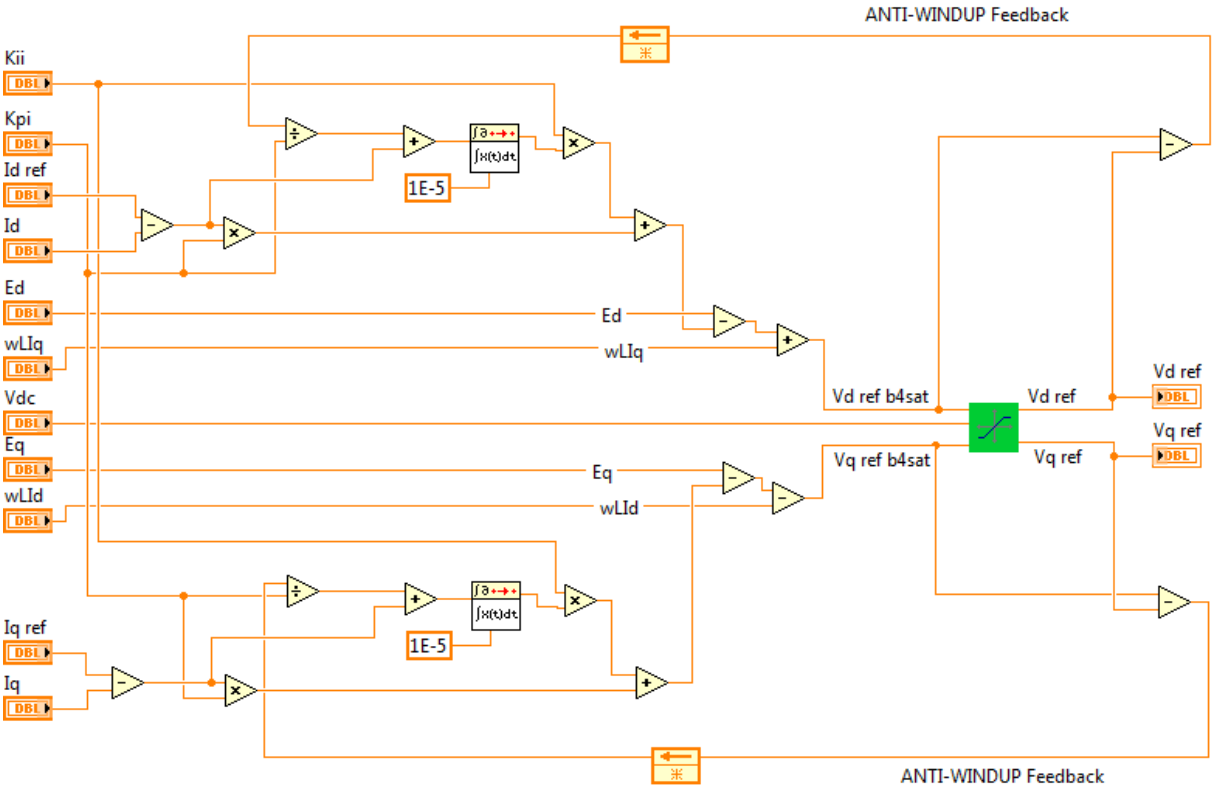
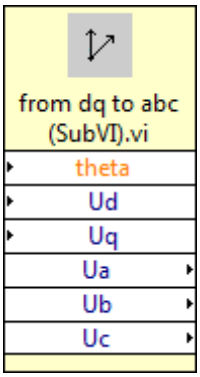


Figure 37: Current controller.

4.1.3. DQ-to-ABC transformation block.



Inputs	Outputs
theta	Ua
Ud	Ub
Uq	Uc

Table 10: Inputs and outputs of From dq to abc subVI.

Figure 38: From dq to abc block.

The output of the decoupled controller is a reference voltage whose components are expressed in dq-axes. Since the input of the PWM block is a reference voltage expressed in abc axes, a transformation block is needed. The transformation is done using the equations 4.8 and 4.9.

$$\begin{aligned} U_\alpha &= V_d \cos\theta - V_q \sin\theta \\ U_\beta &= V_d \sin\theta + V_q \cos\theta \end{aligned} \tag{4.10}$$

$$\begin{aligned} U_a &= U_\alpha \\ U_b &= -\frac{1}{2}U_\alpha + \frac{\sqrt{3}}{2}U_\beta \\ U_b &= -\frac{1}{2}U_\alpha - \frac{\sqrt{3}}{2}U_\beta \end{aligned} \tag{4.11}$$

These equations are implemented in Labview and shown in Figure 38.

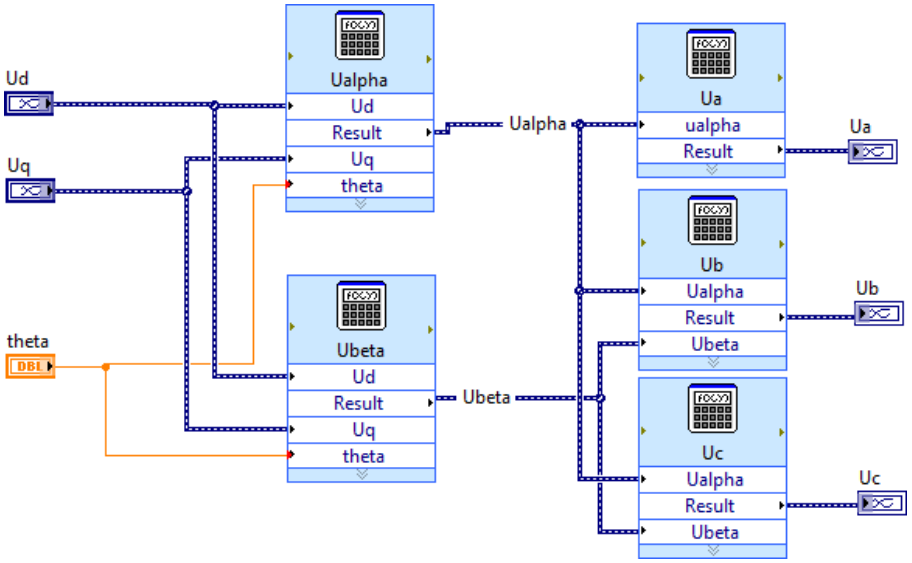
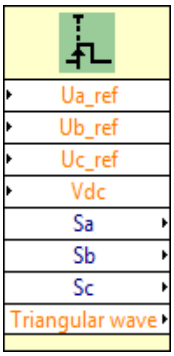


Figure 39: DQ-to-ABC transformation block.

4.1.4. Sinusoidal pulse width modulation block.



Inputs	*Outputs*
Ua_ref	*Sa*
Ub_ref	*Sb*
Uc_ref	*Sc*
Vdc	*Triangular wave*

Table 11: Inputs and outputs for SPWM subVI.

Figure 40:SPWM block.

PWM modulation is based on the comparison between the three sinusoidal reference voltage waves and a triangular carrier wave. Using this comparison, three pulse signals, Sa, Sb and Sc, are created in order to define the duty cycles of the IGBT´s.

The PWM block was created in Labview as shown in Figure 41.

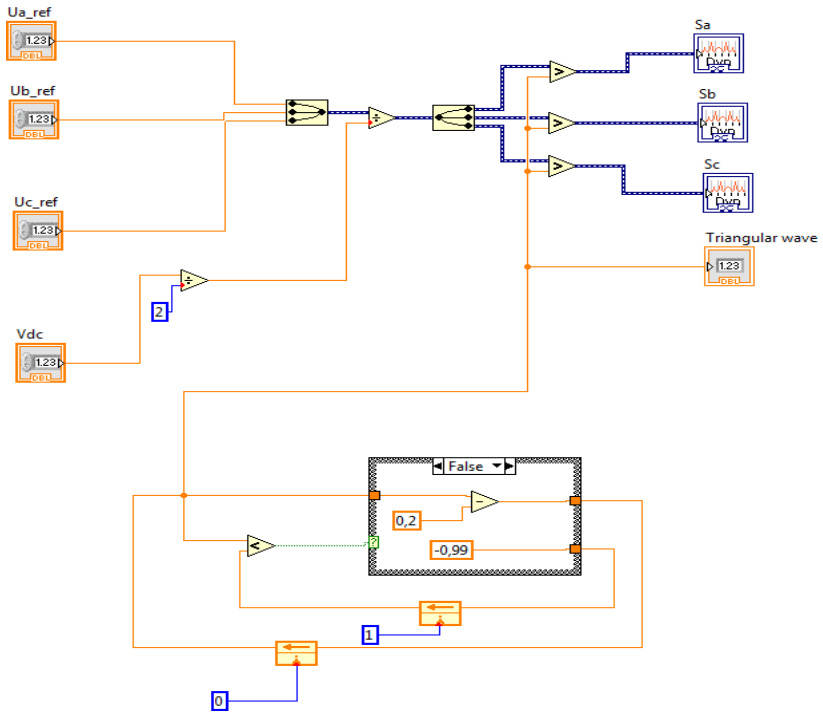


Figure 41: SPWM block, inside view.

The triangular wave is created by dividing the period of the signal according with the switching frequency into the number of discrete points that are necessary. Using the number of discrete points needed, the increment of the amplitude is calculated to achieve a triangular wave with unitary value.

The front panel of this VI shows the comparison between the triangular wave and the three sinusoidal voltages in the upper part, and the three switching patterns of Sa, Sb and Sc in the lower

part. The switching frequency is 10 kHz, and the sampling frequency used to generate the triangular wave and compare it with the control signal is 200 kHz, that is, 20 points per switching period.

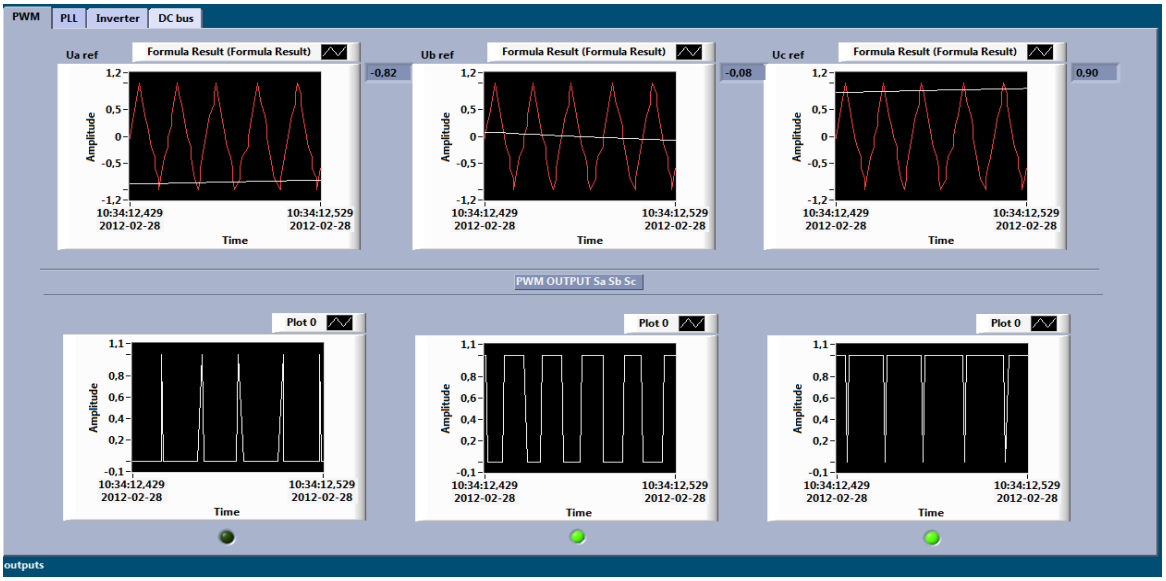


Figure 42: PWM front panel.

4.1.5. Rectifier model block.

Inputs	*Outputs*
Capacitance	*ia*
L	*ib*
R	*ic*
R Load	*Vdc*
Sa	*Idc*
Sb	-
Sc	-
Ua	-
Ub	-
Uc	-

Table 12: Inputs and outputs for the rectifier model subVI.

Figure 43: Rectifier model block.

According to [4], a rectifier model can be implemented using only three switches (Sa, Sb and Sc) by determining the voltage applied depending on the ON/OFF state of the switches. For simulations it is accepted that, in the

same leg of the inverter, one switch is always ON while the other one is OFF. However, in the implementation chapter it is explained that a dead time between commutations is used to avoid short circuits in the same leg.

$$\begin{aligned} u_{Sab} &= (Sa - Sb)\, u_{dc} \\ u_{Sbc} &= (Sb - Sc)\, u_{dc} \\ u_{Sca} &= (Sc - Sa)\, u_{dc} \end{aligned} \tag{4.12}$$

where Sa, Sb and Sc represent the state of the three top switches, one for each leg of the inverter. The value of Sa, Sb and Sc is "1" if the corresponding switch is On and "0" if the switch is OFF.

$$\begin{aligned} u_{Sa} &= f_a \,.\, u_{dc} \\ u_{Sb} &= f_b \,.\, u_{dc} \\ u_{Sc} &= f_c \,.\, u_{dc} \end{aligned} \tag{4.13}$$

where fa, fb and fc are calculated as follows.

$$\begin{aligned} f_a = S_a - S^* = \; S_a - \frac{1}{3}(S_a + S_b + S_c) &= \frac{2S_a - (S_b + S_c)}{3} \\ f_b &= \frac{2S_b - (S_a + S_c)}{3} \\ f_c &= \frac{2S_c - (S_a + S_b)}{3} \end{aligned} \tag{4.14}$$

Using the equations of a rectifier, one for each leg, the model of the rectifier is implemented for the simulations (Figure 44).

$$\begin{aligned} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} &= R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} u_{Sa} \\ u_{Sb} \\ u_{Sc} \end{bmatrix} \\ C \frac{du_{dc}}{dt} &= S_a i_a + S_b i_b + S_c i_c - i_{load} \end{aligned} \tag{4.15}$$

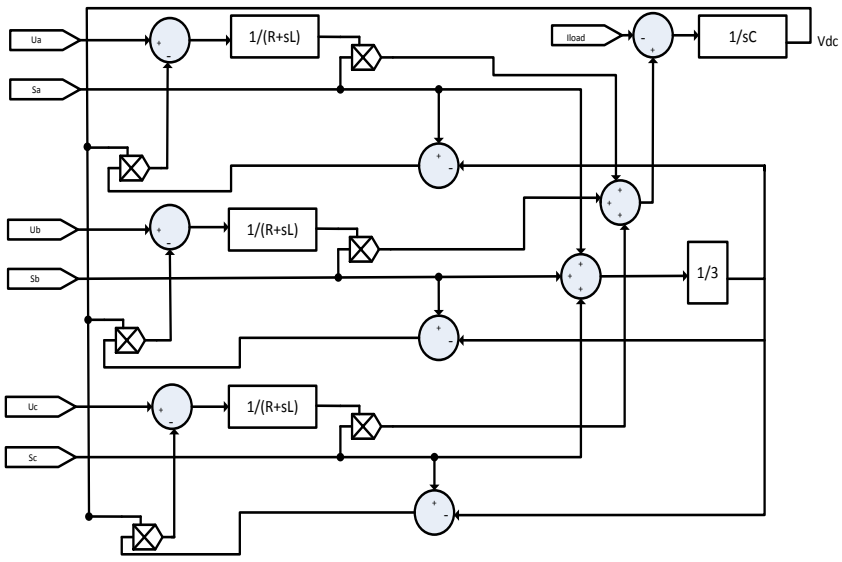


Figure 44: Rectifier theoretical scheme.

Implementing this model in Labview, the rectifier model obtained is shown in Figure 45.

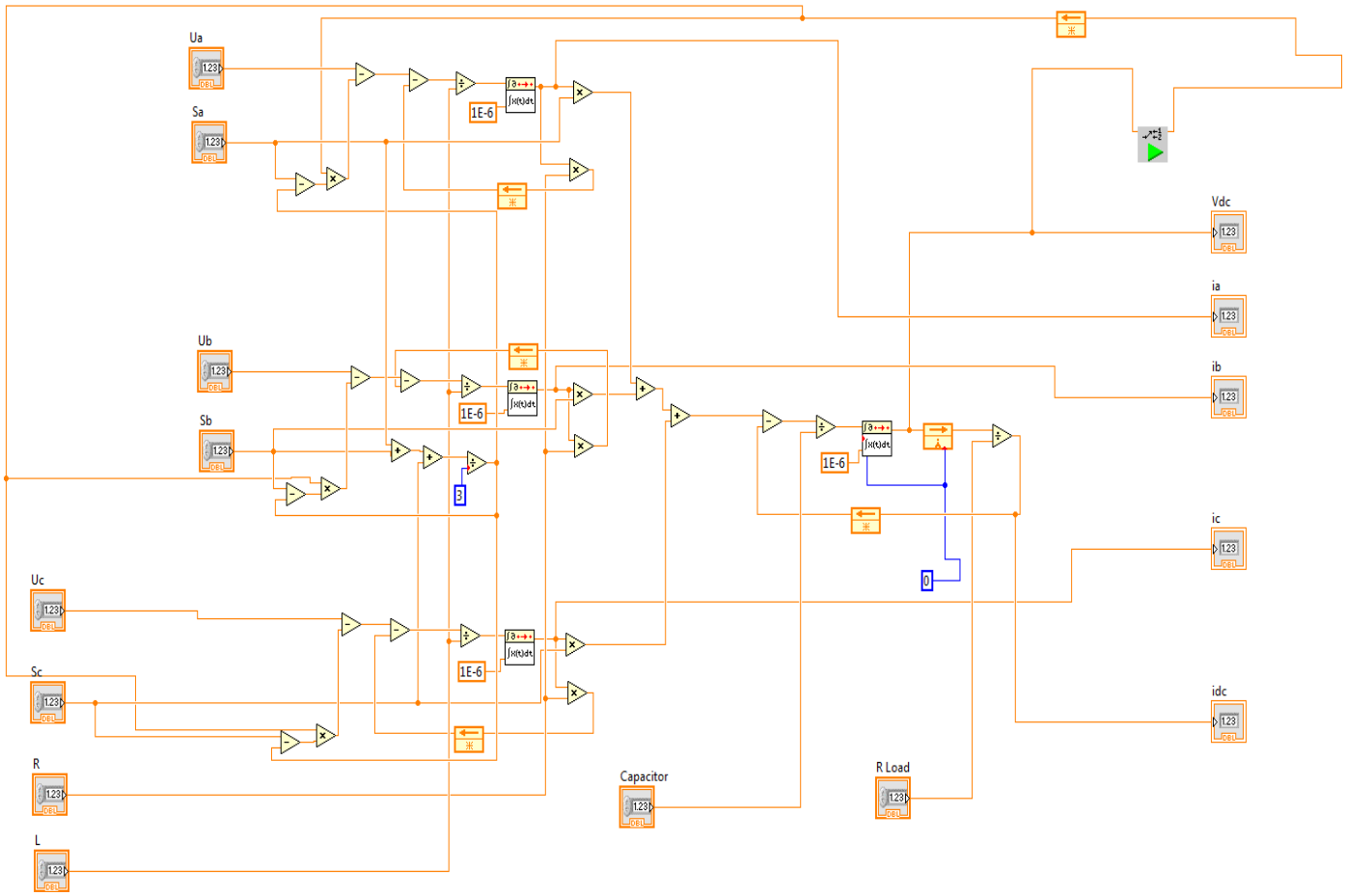


Figure 45: Rectifier Labview implementation.

4.2. Simulation procedure.

This part of the chapter includes a detailed explanation of how the simulation is developed. At the beginning all the relays and switches are off and the connection sequence is done as shown in Figure 46.

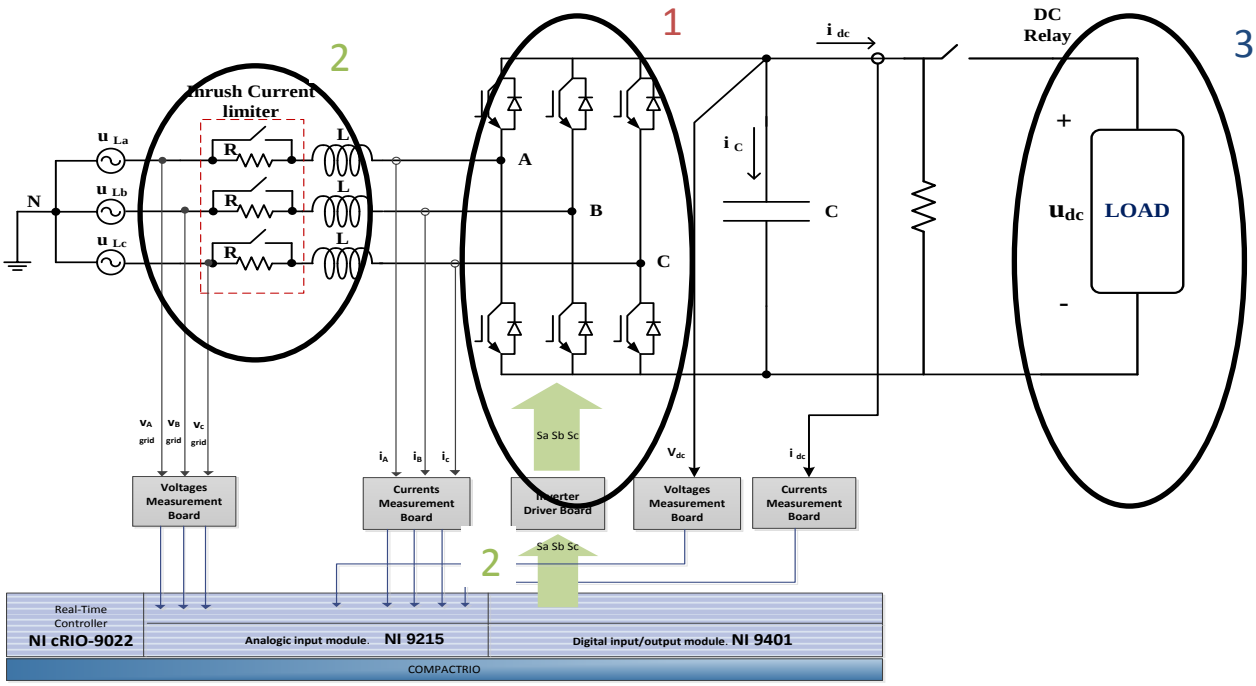


Figure 46: Start up procedure in the simulation.

1. With the relays open and the Sa, Sb and Sc switches (and the corresponding switches of the same legs) in OFF state, the system acts like a diode rectifier raising the DC voltage until it reaches the peak value of the line voltage. With a 400 V line-to-line supply, the DC voltage should reach a maximum value of 560 V minus the losses on each line, which is approximately 500V. As shown in Figure 47, the current is very low because the load is disconnected and the current is flowing through a high resistance in parallel with the load.

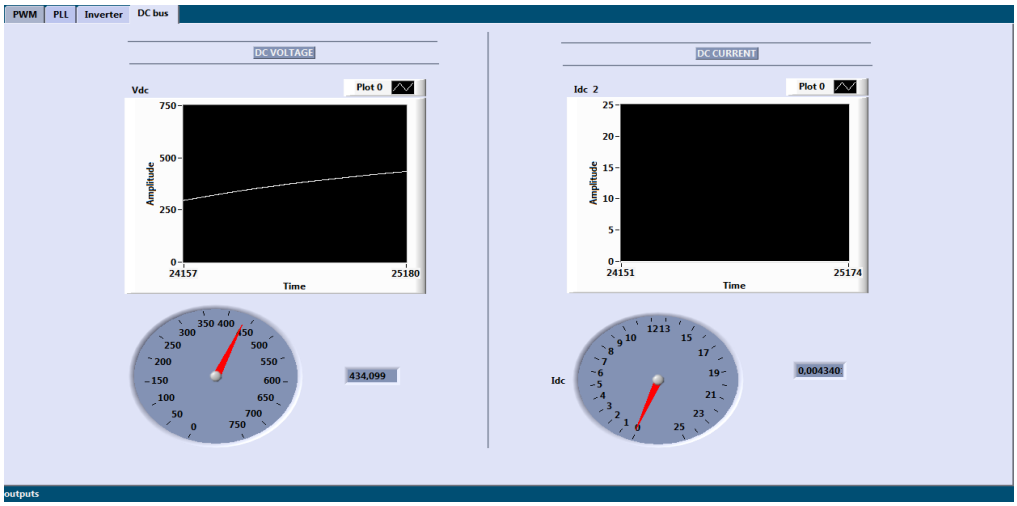


Figure 47: DC bus control with diode rectifier.

2. In the simulation, once the DC voltage reaches 500 V, the inrush current limiter is bypassed and the PWM signals start to be transmitted until the control raises the DC voltage up to the reference value. During this period of rise, the d-axis component of the reference current saturates at 30A and the AC currents are higher than in the steady state (Figure 48).

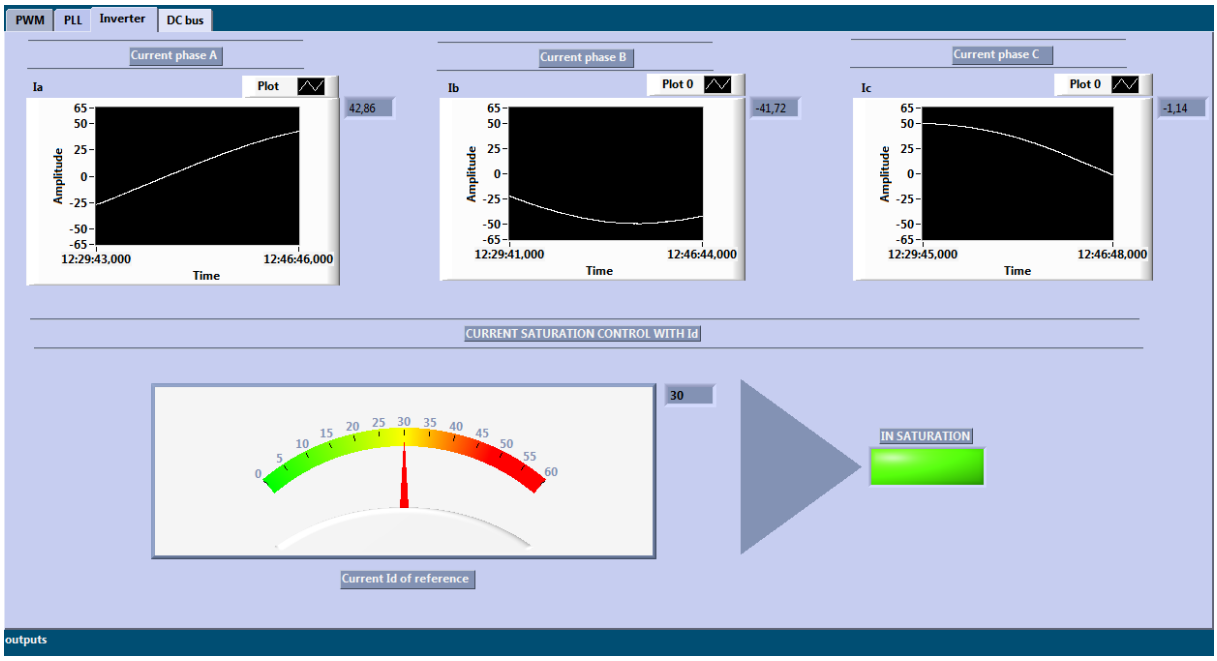


Figure 48: Inverter front panel with PWM controlling in saturation.

During this period, the load is still disconnected and consequently, the DC current is very low (see Figure 49).

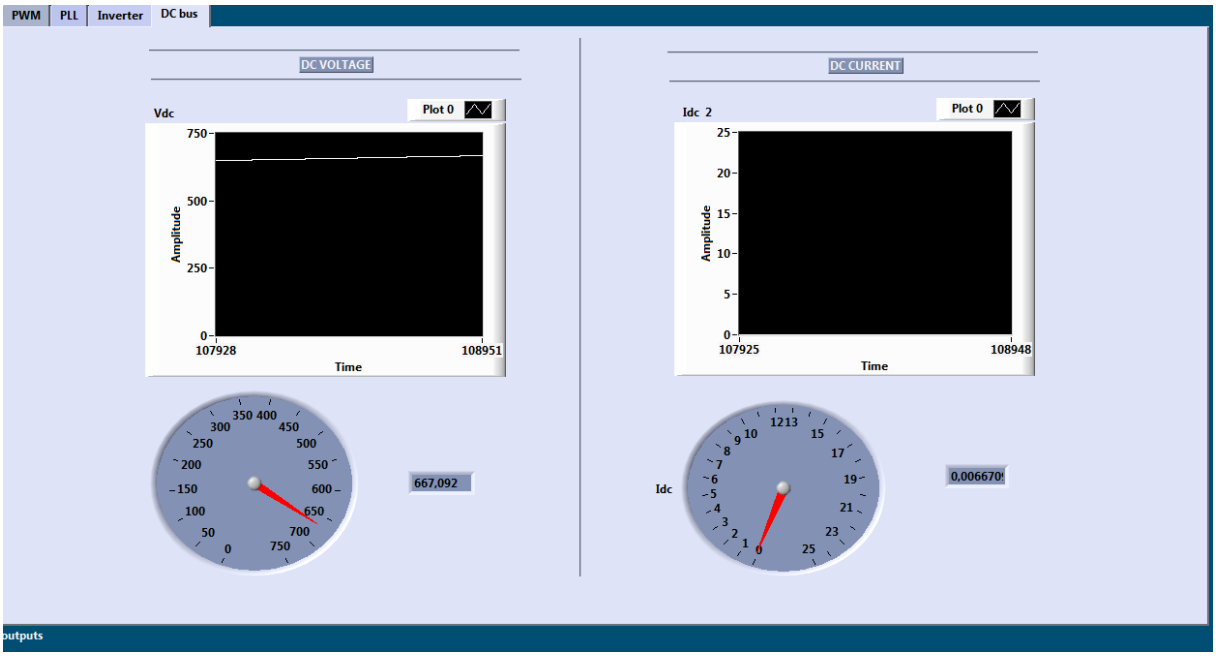


Figure 49: DC bus front panel with PWM controlling in saturation.

3. When the system is under control, after the DC voltage reaches 700V, the load is connected producing a raise of the DC current up to its steady state value, which provides the 15 kW required (see Figure 50).

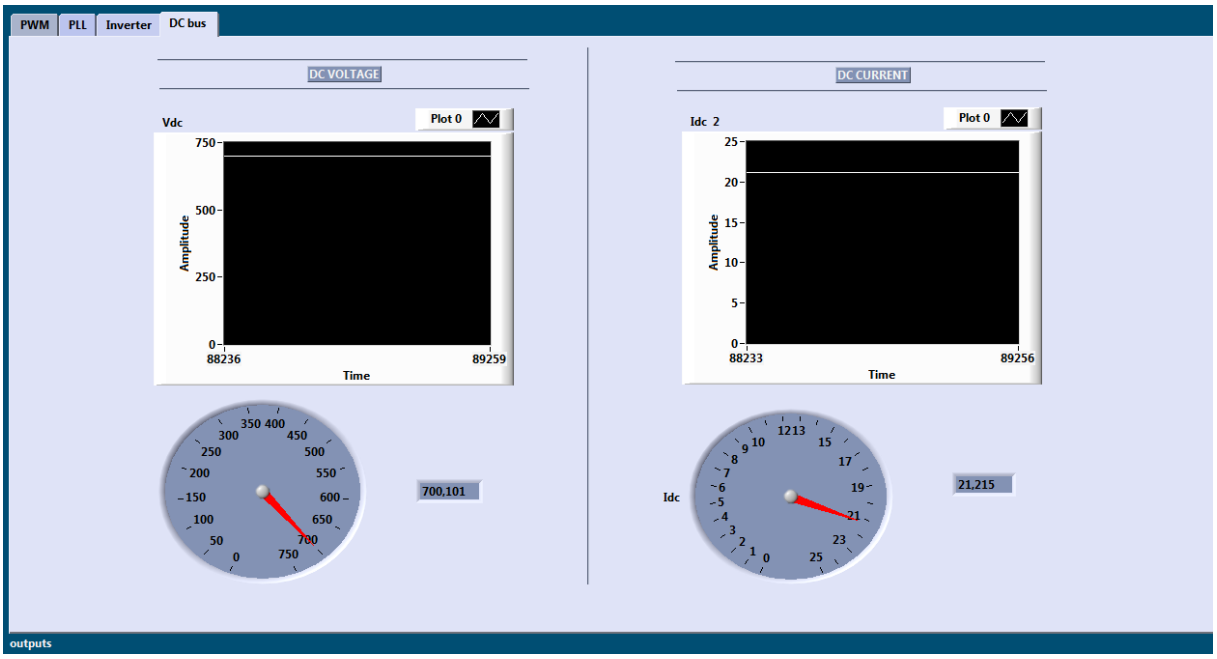


Figure 50: DC bus front panel in steady state.

During steady state, the currents are stable and the d-axis component of the reference current does not saturate anymore, as shown in Figure 51.

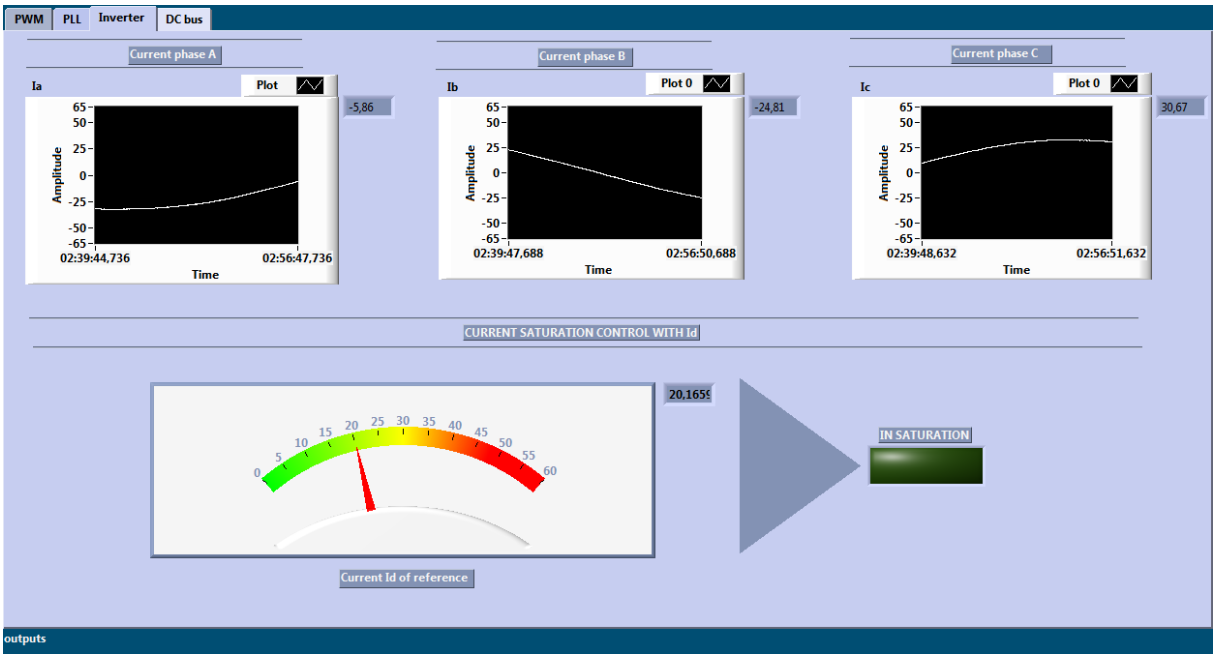


Figure 51: Inverter front panel in steady state.

Chapter 5.Hardware implementation.

In this chapter all the hardware used is explained as well as the CompactRIO programming.

5.1. System composition.

The system implemented follows the schematic shown in Figure 52.

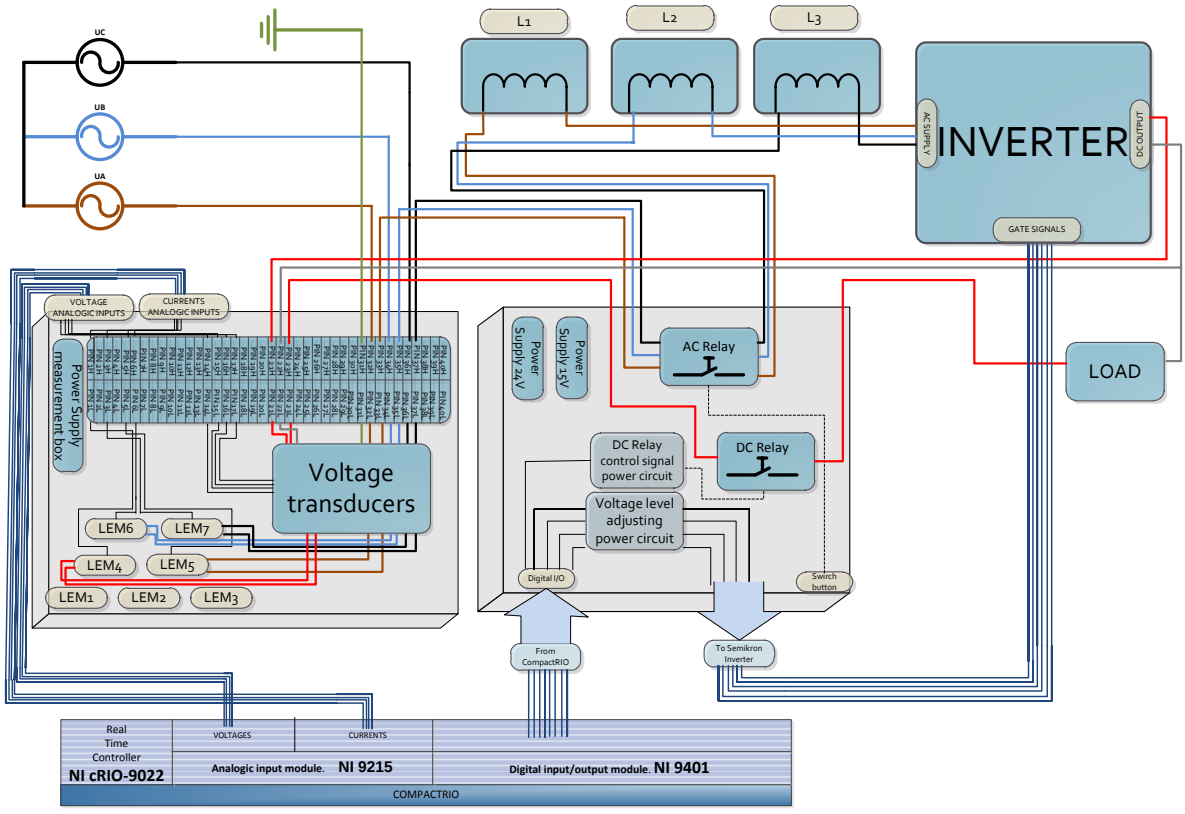


Figure 52: Complete system schematic.

This system is composed by:

- AC voltage supply.
- Three inductors of 3mH.
- The measurement box.
- The box containing the DC sources and the relays.
- The inverter with the load connected on the DC side.
- The CompactRIO device.

Figure 53: General overview of the complete system.

5.1.1. AC voltage supply.

Because of the diameter of the existent wires in the measurement box, the voltage level has to be lowered in order to be able to use the measurement box that already exists and operate within safety limits.

To provide the new voltage level, an autotransformer is placed in the lab providing the power level needed and also isolation between the set up and the grid.

Finally, the voltage level used is 20 V line-to-line.

Figure 54: View of the three-phase autotransformer.

5.1.2. Inductors.

After the calculations made in the design chapter and taking into consideration the ripple for the current and the limit needed in the voltage, the inductors were chosen with a value of 3mH.

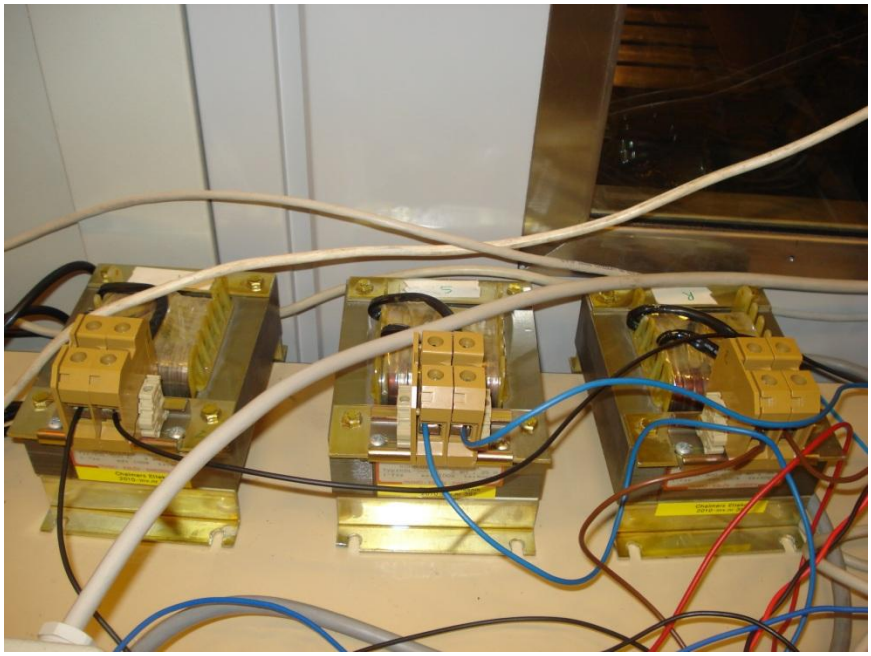


Figure 55: View of the inductors.

5.1.3. Measurement box.

The measurement box includes:

- DC voltage source of 15V in order to feed the LEMs and the UMAT2.
- Three voltage transducers UMAT2 with three channels each one.
- Seven current sensors LEM LA 50-S but only four of them in use.

The measurement box is used to measure the voltage and the currents that are needed to control the system. For this reason, 8 measures are taken, 4 for the voltages and 4 for the currents. The following Figure 56 shows where the measures are taken.

The four LEM LA 50-S/SP1 current measuring modules are used providing galvanic isolation between the primary and the secondary circuits as already explained in the design chapter. These modules are used also to measure the DC current because of a high frequency power transmission that allows the modules to measure all kinds of currents. As explained in the design chapter, the resulting current goes through a resistor to induce a voltage drop that can be read by the analogic inputs of the CompactRIO device.

The voltage measurements are taken by three voltage transducers UMAT2 but only two of them are in use. The three channels of one of them are used to measure the three AC phase voltages and only one channel of the other one is used to measure the DC voltage. In order to measure the voltages, the voltage goes through a voltage divider previously calculated in the design chapter. After that, the reduced signal goes to the AD210, which is an isolated amplifier.

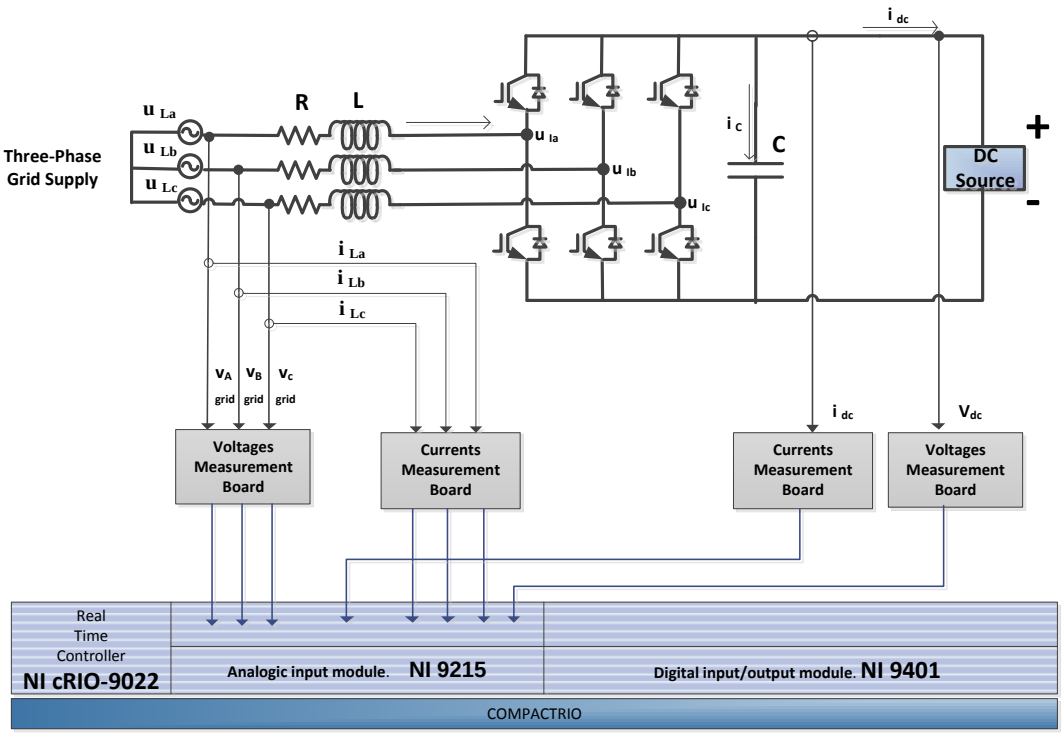


Figure 56: Definition of the points where the measures are taken.

As can be checked in the measurement box connections in Figure 57, to measure the voltage and current of each phase, the wire coming from the voltage source is connected to a pin which output is connected to the two different measurement circuits: the voltage measurement circuit connected in parallel and the current measurement circuit connected in series.

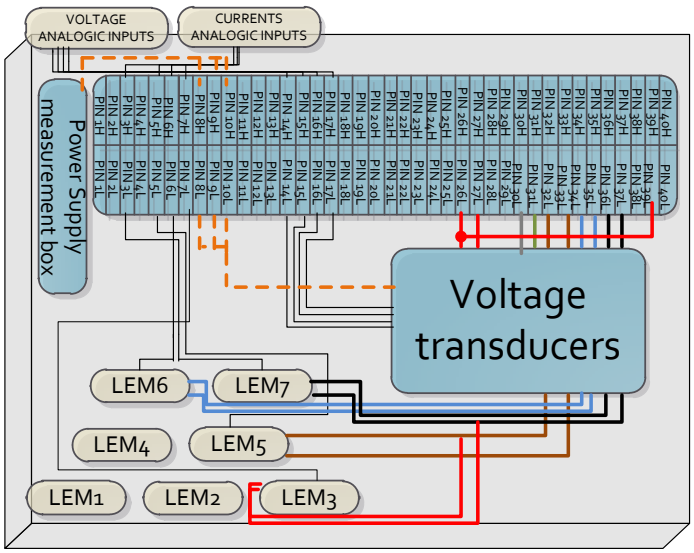


Figure 57: Measurement box schematic.

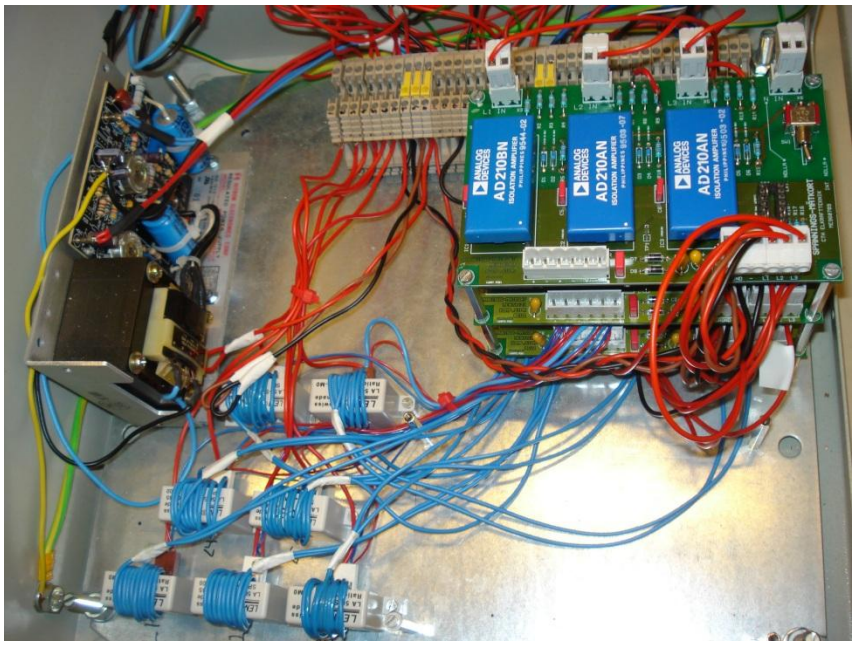


Figure 58: View of the measurement box.

The Table 13 details all the pins in use in the measurement box and which signal or wire is connected to each of them.

PIN	CONNECTED TO	PIN	CONNECTED TO	PIN	CONNECTED TO
1H	Analog output Idc	14L	Lower Volt. Trans. Output (L3)	28H	Not in use
1L	LEM 4 output	15H	Analog output Va	28L	Not in use
2H	Not in use	15L	Mid volt. Trans.outp. L1	29H	Not in use
2L	Not in use	16H	Analog output Vb	29L	Not in use
3H	Not in use	16L	Mid volt. Trans.outp. L2	30H	Vdc-
3L	Not in use	17H	Analog output Vc	30L	Low volt. Trans Input (N)
4H	Not in use	17L	Mid volt. Trans.outp. L3	31H	Not in use
4L	Not in use	18H	Not in use	31L	Not in use
5H	Analog output Ia	18L	Not in use	32H	PhasevoltageUa
5L	LEM 5 output	19H	Not in use	32L	MId volt.TransInputL1 &LEML5
6H	Analog output Ib	19L	Not in use	33H	AC Relay input phase A
6L	LEM 6 output	20H	Not in use	33L	LEM L5 return
7H	Analog output Ic	20L	Not in use	34H	PhasevoltageUb
7L	LEM 3 output	21H	Vdc+	34L	MId volt.TransInputL2 &LEML6
8H	-15V	21L	Low volt. Trans Input L3 & LEM 4	35H	AC Relay input phase B
8L	Transducerssupply	22H	Vdc-	35L	LEM L6 return
9H	0V	22L	Lower Volt. Trans. Input (N)	36H	PhasevoltageUc
9L	Transducersupply (GND)	23H	DC Relay Input	36L	Mid volt.TransInput L3
10H	+15V	23L	LEM L4return	37H	Not in use
10L	Transducerssupply	24H	Not in use	37L	Not in use
11H	Not in use	24L	Not in use	38H	Not in use
11L	Not in use	25H	Not in use	38L	Not in use
12H	Not in use	25L	Not in use	39H	Vdc+
12L	Not in use	26H	PhasevoltageUc	39L	Upper volt. Trans Input L2
13H	Not in use	26L	LEM L3	40H	Not in use
13L	Not in use	27H	AC Relay input phase C	40L	Not in use
14H	Analog output Vdc	27L	LEM L3 return	-	

Table 13: Pin terminal connections inside the measurement box.

5.1.4. The DC sources and relays box.

The DC sources and relays box includes (See Figure 59):

- A 15 Vdc voltage source that feeds the inverter and the electronic board that adjusts to an appropriate voltage level the TTL gate signals to control the inverter.
- A 24 Vdc voltage source that feeds the AC and DC relays.
- An AC relay (C3-A 30) for the connection of the system to the grid.
- A DC relay to connect the load to the rectifier.
- An electronic board to drive the DC relay.
- An electronic board to drive the AC relay.
- An electronic board to adjust the TTL gate signals voltage level to 15 V, which is the required voltage level of the gate signals in the inverter.

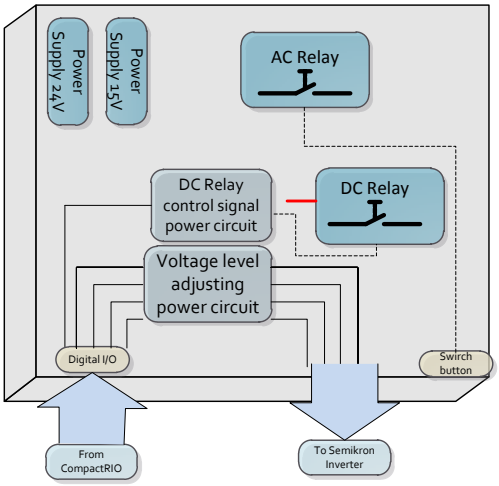


Figure 59: DC sources and relays box.

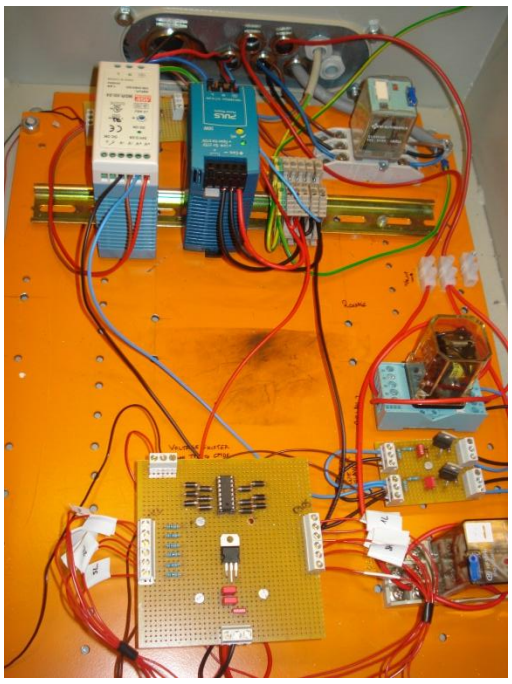


Figure 60: View of the DC sources and relays box.

5.1.5. Inverter and load.

The inverter used for this system is a Semikron inverter AN-8005. The control of the inverter switching is carried out by SPWM pulses generated by the CompactRIO device, with 10 kHz frequency. The connection between the inverter´s control circuit and CompactRIO is done by a 25-pin D type connector that transmits six PWM signals, as well as one more command signal to connect the load in the DC side.

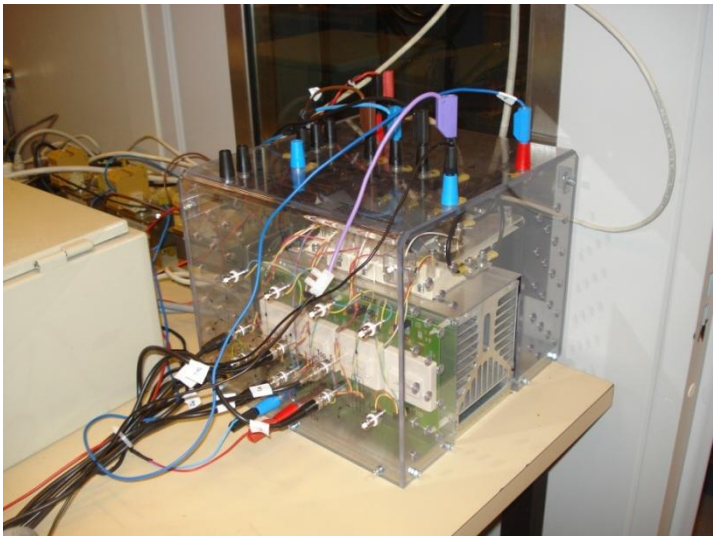


Figure 61: View of the Semikron inverter AN-8005.

The load value is 33 Ohms, as calculated in the design chapter. That way, even after changing the voltage level, the current and the voltage are reduced in the same ratio. To obtain the required load, a potentiometer of 47 Ohms is used. It is adjusted at 70% of the total resistance to achieve the 33 Ohms required for the system.

Figure 62: View of the potentiometer.

5.1.6. CompactRIO.

CompactRIO is a reconfigurable control and acquisition system. The CompactRIO system's architecture includes I/O modules, a reconfigurable FPGA chassis, and an embedded controller. The CompactRIO has been programmed with Labview graphical programming tools [8]. In this thesis the compactRIO system used is composed by the following elements:

- A real-time controller NI cRIO 9022.
- 2 analog input modules NI 9215 with BNC connectors.
- An analog output module NI 9263 (not used).
- 2 digital input/output modules NI 9401 (only one in use).

Figure 63: View of the compactRIO system.

Using the CompactRIO system, there are 3 possibilities of programming environments that can be used simultaneously; the FPGA, the microprocessor and the PC that is used for programming and monitoring. Because of the possible applications of the system, in this thesis only the FPGA and the microprocessor have been programmed in such a way that the device can be connected to control a system without the need of using a PC.

Inside the FPGA, the time critical tasks have been programmed. Mainly, these tasks are the data acquisition, the PLL calculation and the Sinusoidal PWM pulses generation. Inside the microprocessor, the rest of the programming which does not require to be as fast has been programmed, that is, the Voltage Oriented Control and the monitoring of the different signals.

5.1.6.1. FPGA Programming.

Inside the FPGA, the data acquisition, the PWM pulse generation, the PLL and the triangular wave generation have been developed, as shown in the following figures (Figure 64,Figure 66,Figure 65,Figure 68).

Firstly, the data acquisition is made (Figure 64). The sample rate is 200 microseconds for voltages and currents. The data is sent to two different locations. Firstly, it is sent to a FIFO (First In First Out) block using a “for loop”. This FIFO block is very useful to send data for monitoring in the microprocessor at high speed. The data is also stored in memory by using indicators and creating local variables to be sent to another loop inside the FPGA .

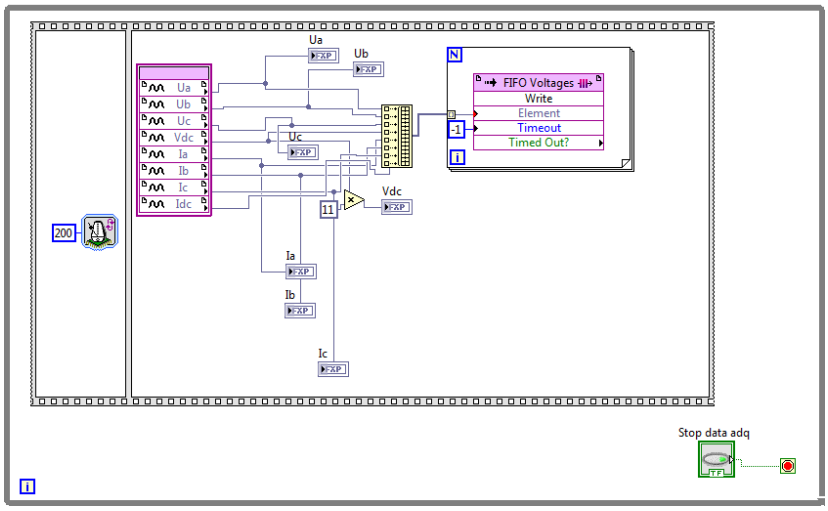


Figure 64: Data acquisition and the use of FIFO to represent the waveforms.

Secondly, the triangular wave which will be used as carrier wave for the Pulse Width Modulation is created. The triangular wave is created by adding an increment of 0.04 each loop period until the triangular wave reaches a value of 1. Then, 0.04 is subtracted from the triangular wave value until -1 is reached and so on. Since the loop time is 1 microsecond, adding this increment, a 10 kHz wave is created (Figure 65) to compare afterwards with the reference voltages in order to do the SPWM.

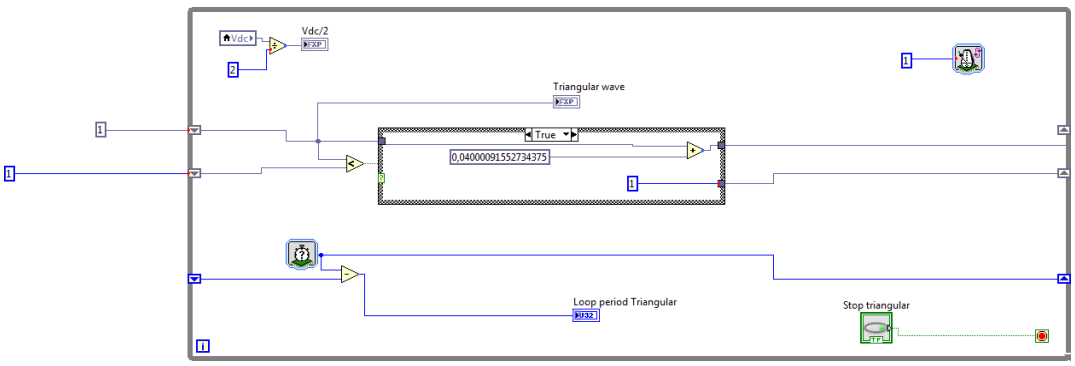


Figure 65: Triangular wave generation.

In order to develop the SPWM (Figure 66), a comparison between the reference voltage divided by half the DC voltage and the triangular wave created is made. If the reference voltage is higher than the triangular wave, the digital output will be “1” (true) and the gate signal will be sent. Otherwise it will be “0” (false) and the gate signal sent to the inverter will be zero.

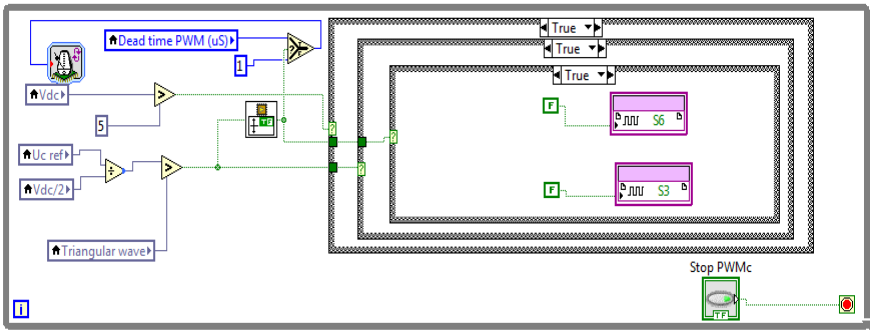


Figure 66: SPWM generation.

During the commutation between ON/OFF states, there is a risk of producing a short circuit between two IGBT´s of the same leg. This affects the output waveform of the inverter and can produce undesirable harmonics and safety issues. These effects are more significant with high switching frequency and to avoid a short circuit it is necessary to add a dead time at the switching instant. During this dead time, both IGBT’s in the same leg will be switched off [19] (Figure67).

In order to implement this dead time effect, a flank detector is placed inside the loop in such a way that when a switch is detected, the FPGA will send a 0 value to both IGBT’s of the same leg and will wait the selected dead time (in that case 5 microseconds) until the loop runs again. With this flank detector, the ON state of the 2 IGBTs in the same leg at the same time is avoided.

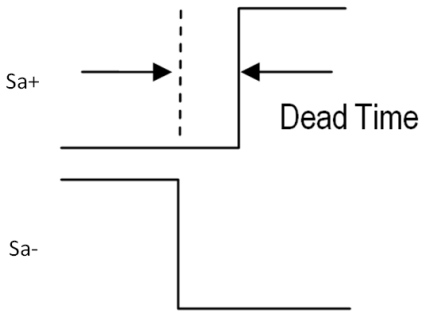


Figure67: Dead time effect.

Another key part in the FPGA program, shown in Figure 68, is the PLL block, which is an already developed VI in Labview. This PLL block gives as a result the angle of the three phase voltages for the d-q transformations that are going to be done inside the microprocessor of the CompactRIO device. In addition, in this loop al the local variables corresponding to the acquired data are bundled and sent to the microprocessor with the cluster variable "acquired data".

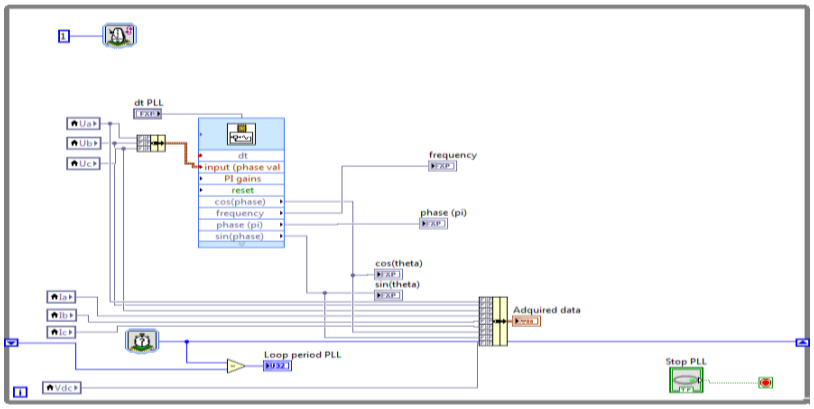


Figure 68: PLL and data sending to the processor.

Finally, the last loop in the FPGA program (Figure 69) uses the angle of the three phase voltage system calculated by the PLL block to transform the reference voltage calculated in the control loop inside the microprocessor from *dq* axis into *abc* axis.

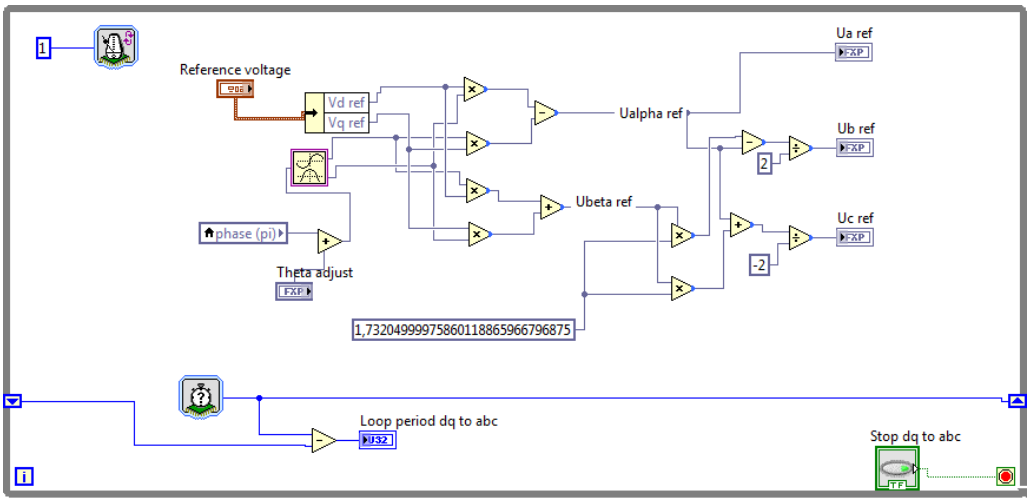


Figure 69: Reference voltage transformation from *dq* to *abc* axis.

5.1.6.2. Microprocessor programming

Inside the microprocessor, the part of the system that has been implemented includes the monitoring, the DC relay activation and the control already explained in the previous chapter. The complete programming is shown in Figure 70.

The first thing that the program in the microprocessor does is opening the FPGA program. After that, a reset is made in order to delete previous values stored in the FPGA. Once the FPGA is reset, the program runs the two loops that interchange information with the FPGA: the monitoring loop and the control loop. When the execution of both loops is stopped, the program stops all the loops in the FPGA and then closes it.

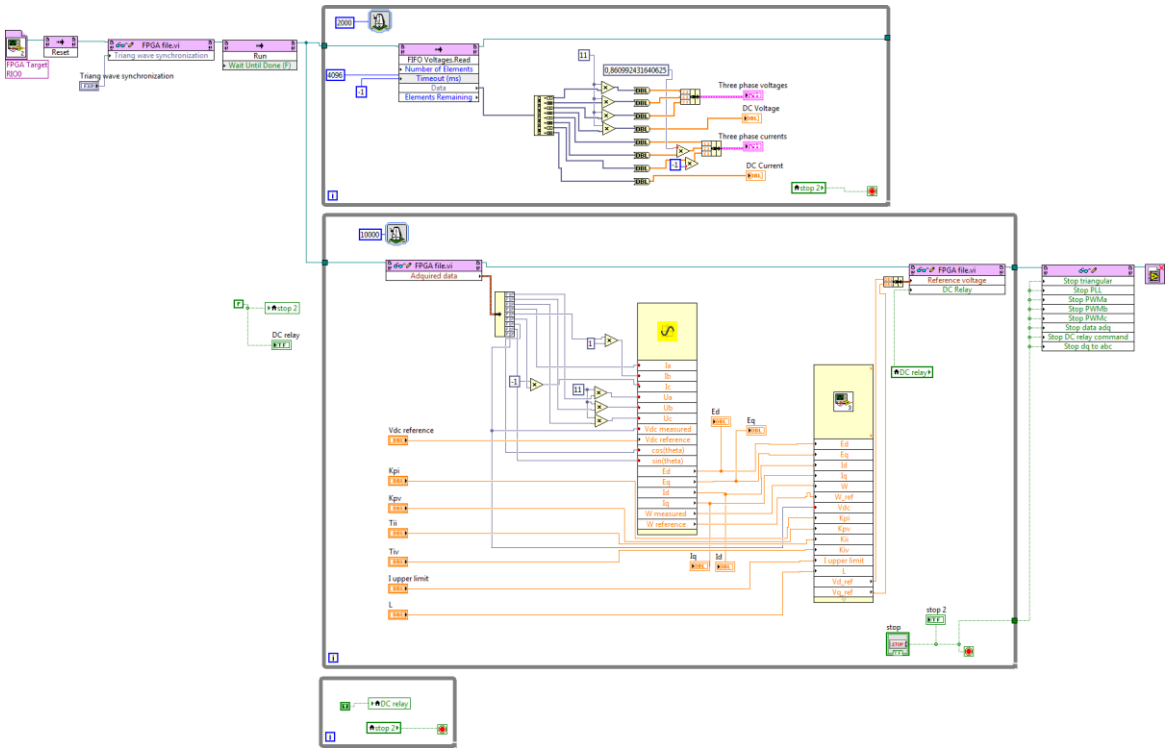


Figure 70: Complete view of the microprocessor program.

The monitoring loop (Figure 71) takes the data from the FIFO that was developed in the acquisition loop inside the FPGA, as mentioned before (Figure 64).

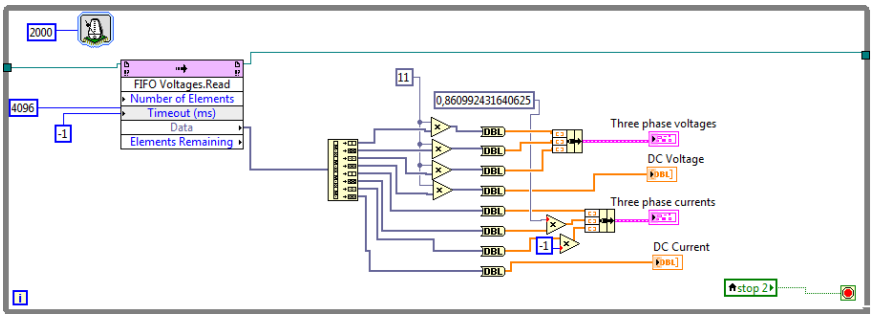


Figure 71: Monitoring loop.

The control loop (Figure 72) takes the acquired data from the FPGA by using a Read/Write block to read the cluster variable "acquired data" and then unbundles this cluster to obtain every singular variable. After that, the *dq* transformation is made for both the voltages and the currents using the angle obtained from the output of the PLL block. Once the *dq* values are obtained, the program executes the control already detailed in the previous chapter. The output of the control, which is the reference voltage in *dq* axis, is sent using again a Read/Write block to the FPGA, where it is transformed into *abc* axis three phase voltages.

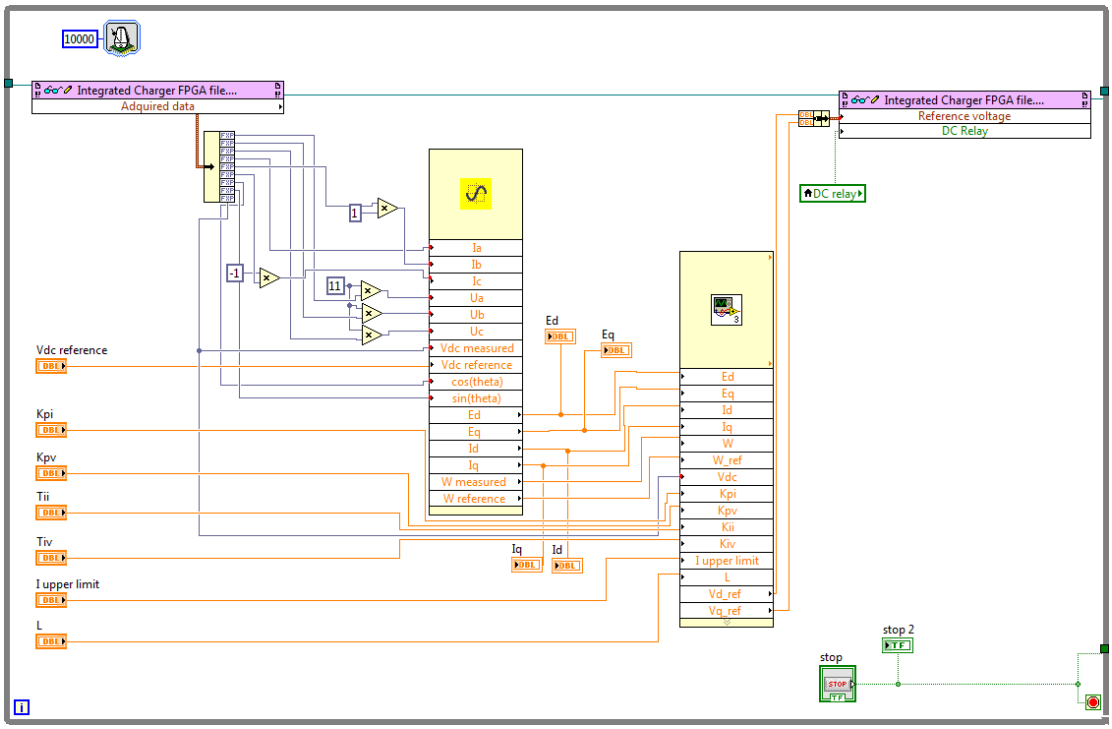


Figure 72: Control loop.

5.2. Results

After the implementation and testing of the hardware, some results are obtained through the front panel of the program running in the microprocessor.

The main duties of the control are to control the DC bus voltage and to set a power factor correction in order to have a unitary power factor.

The system was fed with a 20 V line-to-line voltage supply regulated by the auto transformer and the reference DC voltage was set to 50 V. The response of the control was also checked by changing the reference DC voltage to 60 V while the system was operating.

As shown in Figure 73, the data acquisition of the voltages and the *dq* transformation are made in the first tab of the front panel. The *dq* transformation using the output angle from the PLL block is well done since the voltage in q axis is zero.

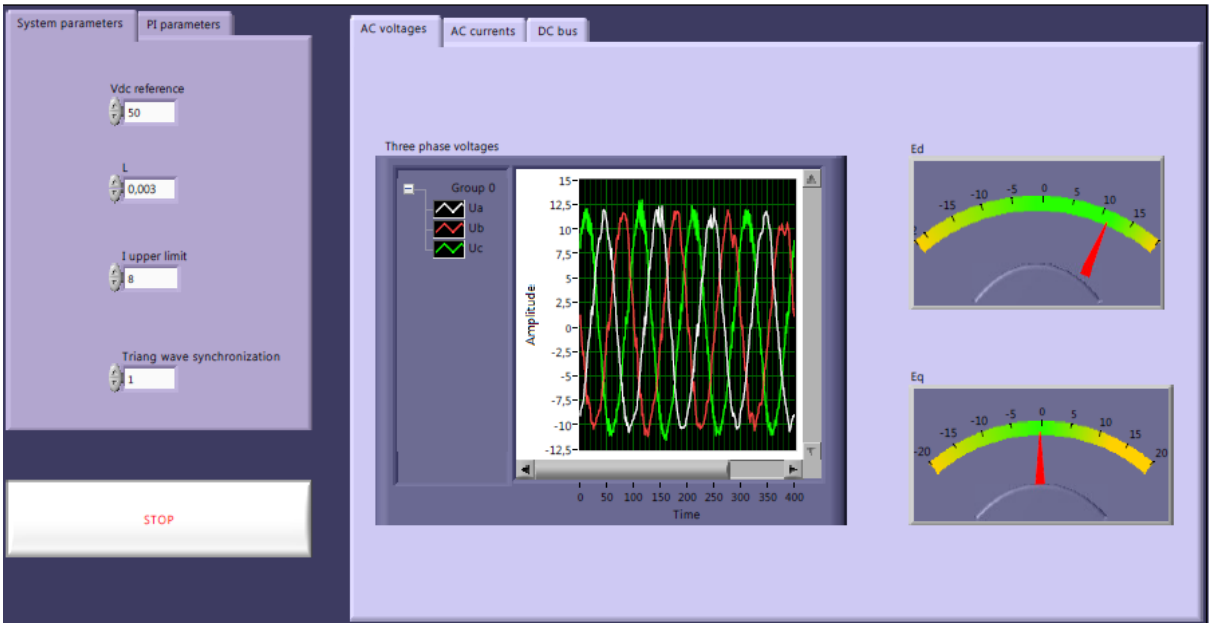


Figure 73: AC voltages and dq results transformation of voltages.

In the following tab of the front panel (Figure 74), the AC currents measured can be checked. As shown in the I_q panel, the power factor correction control is working because this component of the current is zero, achieving a unitary power factor with no reactive power flowing through the system.

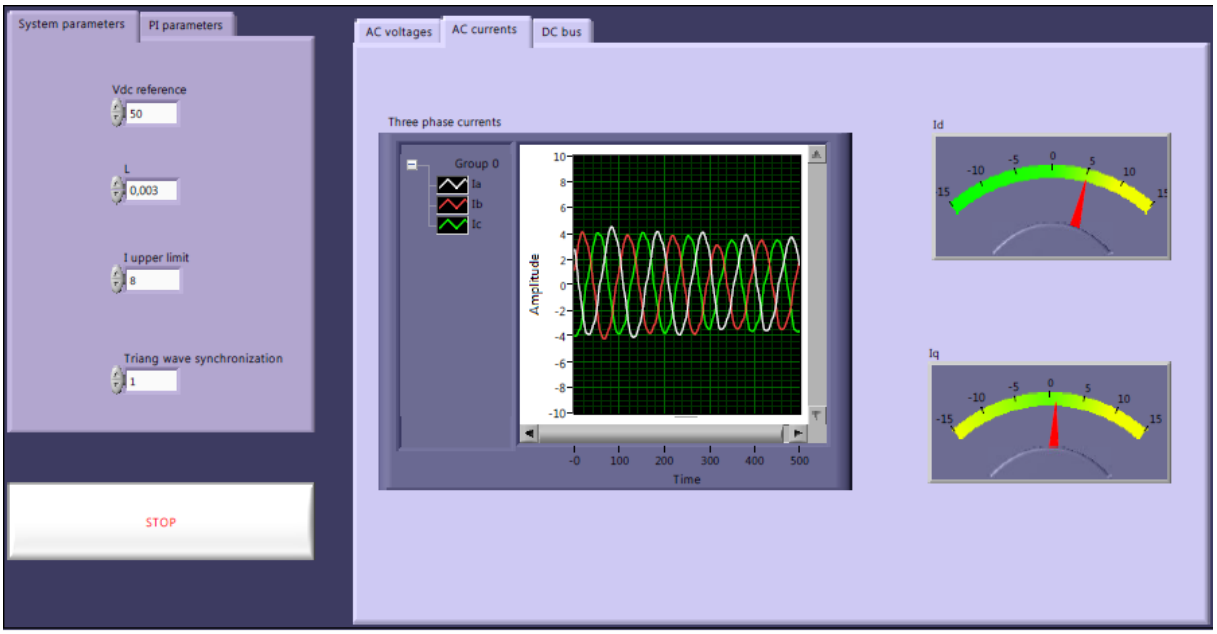


Figure 74: AC currents and dq transformation of the currents.

Finally, in the last tab of the front panel, the DC bus voltage and current are shown (Figure 75). In addition, there is a led indicating if the DC relay is activated or not, that is, if the load is connected or not.

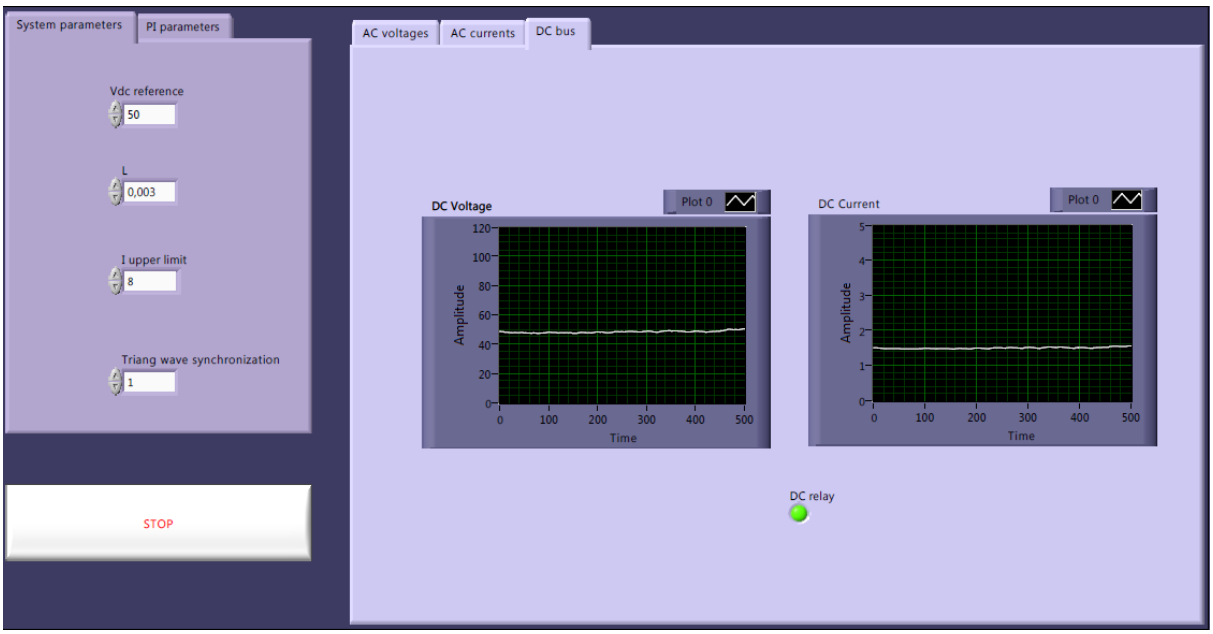


Figure 75: DC bus results.

Chapter 6. Conclusions & Future work.

6.1. Conclusions.

Voltage oriented control of a boost rectifier using a CompactRIO control system was designed, simulated and implemented in this thesis.

Firstly, a Matlab/Simulink model was used in order to carry out the design of the system. After the design, a model for the system was developed in Labview for the initial power requirement, which was 15 kW. The implemented model includes models for the PWM signal generator, inverter, controller and *dq* transformations. The simulation results showed an accurate response to DC voltage requirements.

After the simulations, a lab setup was implemented using a CompactRIO control system. Before the CompactRIO programming, the system was adjusted to a lower power requirement. The programming of the CompactRIO device was done by implementing some parts of the program in the FPGA and some other parts in the microprocessor, developing as well the required communication between them.

The results show that the system is effectively working as a boost rectifier and meets the desired DC voltage output specified as reference for the control. Furthermore, when a step in the reference DC voltage is applied, the system has a good response and meets the new reference value. There are some small oscillations in the output of the DC bus, which can be probably caused by the high switching frequency, together with the injection of a dead time between commutations. The power level that had to be used in the practical implementation also affected the results obtained, as the control needs to be more precise with low voltage levels due to a higher influence of every component of the system.

Regarding power quality, the system satisfies the requirements and accomplishes a power factor correction. The unity power factor is achieved by setting to zero the value of the reactive component of the current and synchronizing the currents in the system with the voltages.

6.2. Future work.

The current hardware is limited due to wires that only allow maximum currents of about 6 A. A possible future work could be the implementation of new hardware to achieve the initial power requirement of this thesis, which is 15 KW. For a different power level, the control with the CompactRIO device is practically identical with adjustments of some parameters.

In this thesis, the PWM modulation method was used, although the modulation method could be improved using Space Vector Modulation. SVM is a simple and effective modulation method which gives a considerable reduction in harmonics, which meets modern grid power quality requirements.

As mentioned before, a dead time of 5 microseconds was used. In order to improve the performance of the system, analysis can be done in order to minimize the dead time added during the commutations of the IGBTs.

Since the inverter used for the setup has 4 legs and one is not in use, a current control can be done through the use of this last leg working as a DC-DC converter.

In order to improve the measurement of voltages and currents a low pass filter can be added using the calculations already done in the design chapter.

References.

[1] Vindel Muñoz D., “Design, Simulation and implementation of a PMSM drive system” Master of Science Thesis in Electric Power Engineering, Chalmers University of Technology, Göteborg, 2011.

[2] Saeid Haghbin, “An Isolated Integrated Charger for Electric or Plug-in Hybrid Vehicles” thesis for the degree of licentiate of engineering. Chalmers University of Technology, department of Energy and Environment, division of Electric Power Engineering. Göteborg, Sweden, 2011.

[3] Sylvain LechatSanjuan, “Voltage Oriented Control of Three-Phase Boost PWM Converters”, Master of Science Thesis in Electric Power Engineering, Chalmers University of Technology, Göteborg, 2010.

[4] Kasmierkowski Marian P., Blaabjerg F., Krishnan R.- “Control in power electronics, selected problem”. Elsevier Science, USA. 2002. 518p. ISBN : 0-12-402772-5.

[5] Malinowski Mariusz. “Sensorless Control Strategies for Three-Phase PWM Rectifiers”. PhDThesis, Warsaw University of Technology, Faculty of Electrical Engineering, Institute of Control and Industrial Electronics. Warsaw, Poland. 2001. 128p.

[6] Lundberg Stefan. Lecture slides: ENM075 Electric Drives II. Department of Energy and Environment, Chalmers University of Technology, Göteborg, Sweden. 2009.

[7] Harnefors Lennart. “Control of Variable Speed Drives”. Applied Signal Processing and Control, Department of Electronics, Mälardalen University, Västerås, Sweden, 2002. 194p.

[8] Bueno Alexander. Universidad S. Bolivar. Industrial technology department.August, 2007

[9] SEMITEACH – IGBT SKM 50 GB 123D, Datasheet.

[10] Doriano Ciscato. PWM Rectifier with Low dc Voltage Ripple for Magnet Supply. April 1992

[11] Sargos F., IGBT Power Electronics Teaching System Principle for sizing power converters, 2008.

[12] CompacRIO analog input module. NI 9215 module for use with NI CompactDAQ and CompactRIO.

[13] S.S. Young (2001): AD instruments.
Available at: http://www.adinstruments.com/solutions/attachments/pr-signalfilters-05a.pdf

[14] Microstar Laboratories, 1994-2009.
Available at: http://www.mstarlabs.com/dsp/antialiasing/antial.html

[15] Bonnie C. Baker.Microchip Technology Inc.
Available from: http://jimfranklin.info/microchipdatasheets/00699b.pdf

[16] Ottersten Rolf. “On Control of Back-to-Back converters and Sensorless Induction Machine Drives”. PhD Thesis, Department of Electric Power Engineering, Chalmers University of Technology, Göteborg, Sweden. 2003. 165p. ISBN : 91-7291-296-0.

[17] K.J. Åström, 2002. Control system design. PID control.
Available at: http://www.cds.caltech.edu/~murray/courses/cds101/fa02/caltech/astrom-ch6.pdf

[18] Bongiorno Massimo, Sanino A. Lecture slides : ENM100 Power Electronic Solutions for Power Systems. Department of Energy and Environment, Chalmers University of Technology, Göteborg, Sweden. 2009.

[19] Seung-Gi Jeong, Min-Ho Park. “The analysis and compensation of dead-time effects in PWM inverters”. IEEE Transactions on Industrial Electronics, vol.38, no.2, 1991. Pages: 108 – 114.

[20] National Instruments webpage.
Available at: http://sine.ni.com/nips/cds/view/p/lang/en/nid/14164

Appendix A: Hardware datasheets.

CompactRIO controller.

NI cRIO-9022

Real-Time Controller with 256 MB DRAM, 2 GB Storage

- Embedded controller runs LabVIEW Real-Time for deterministic control, data logging, and analysis
- 533 MHz processor, 2 GB nonvolatile storage, 256 MB DDR2 memory
- Dual Ethernet ports with embedded Web and file servers for remote user interface
- Hi-Speed USB host port for connection to USB flash and memory devices
- RS232 serial port for connection to peripherals; dual 9 to 35 VDC supply inputs
- -20 to 55 °C operating temperature range

Product Type	Controller (Computing Device)
Form Factor	CompactRIO
Part Number	780718-01
Operating System/Target	Real-Time
LabVIEW RT Support	Yes
CE Compliance	Yes
Controller	
Controller Type	High Performance
Processor Core Type	533 MHz PowerPC
CPU Clock Frequency	533 MHz
System Memory	256 MB
Legacy Product	No
Ethernet (# of ports)	2
Serial Ports (RS232)	1
USB Ports	Yes

Chassis	
Number of Slots	0
Integrated Controller	No
Input Voltage Range	9 V , 35 V
Recommended Power Supply: Power	55
Recommended Power Supply: Voltage	24
Power Consumption	35
Physical Specifications	
Length	77.3 mm
Width	90.2 mm
Height	88.1 mm
Weight	609 gram
Minimum Operating Temperature	-20 °C
Maximum Operating Temperature	55 °C
Maximum Altitude	2000 m

CompactRIO analog input module NI 9215.

4 Ch, 100 kS/s, 16-Bit, ±10 V Simultaneous Sampling C Series Analog Input Module

NI 9215

- 4 simultaneously sampled analog inputs, 100 kS/s
- -40 to 70 °C operating range
- NIST-traceable calibration
- Hot-swappable operation

Overview

The NI 9215 module for use with NI CompactDAQ and CompactRIO chassis includes four simultaneously sampled analog input channels and successive approximation register (SAR) 16-bit analog-to-digital converters (ADCs). The NI 9215 contains NIST-traceable calibration, a channel-to-earth ground double-isolation barrier for safety and noise immunity, and high common-mode voltage range.

Specifications Summary

General	
Product Name	NI 9215
Product Family	Industrial I/O
Form Factor	CompactDAQ , CompactRIO
Part Number	779011-01
Operating System/Target	Real-Time , Windows
Measurement Type	Voltage
Isolation Type	Ch-Earth Ground Isolation
RoHS Compliant	Yes
Analog Input	
Channels	4 , 0
Single-Ended Channels	0
Differential Channels	4
Resolution	16 bits
Sample Rate	100 kS/s
Max Voltage	10 V
Maximum Voltage Range	-10 V , 10 V
Maximum Voltage Range Accuracy	0.003 V
Simultaneous Sampling	Yes

Analog Output	
Channels	0
Digital I/O	
Bidirectional Channels	0
Input-Only Channels	0
Output-Only Channels	0
Number of Channels	0
Counter/Timers	
Counters	0
Physical Specifications	
Length	9 cm
Width	2.3 cm
I/O Connector	Screw terminals , BNC connectors
Minimum Operating Temperature	-40 °C
Maximum Operating Temperature	70 °C
Minimum Storage Temperature	-40 °C
Maximum Storage Temperature	85 °C
Timing/Triggering/Synchronization	
Triggers cDAQ Chassis	No

CompactRIO digital input/output module NI 9401.

NI 9401 Measurement System

8 Ch, 5 V/TTL Bidirectional DIO for USB, Ethernet, and Wi-Fi

- Bundle includes measurement module and 1-slot NI CompactDAQ chassis
- USB, Ethernet, and 802.11 Wi-Fi connectivity
- 8-channel, 100 ns ultrahigh-speed digital I/O (DIO)
- Ability to access four general-purpose 32-bit counter/timers
- Industry-standard 25-pin D-SUB connector
- Bidirectional, configurable by nibble (4 bits)

Specifications Summary

General	
Product Name	NI 9401 Measurement Bundle
Product Family	Industrial I/O
Form Factor	USB , Wireless , CompactDAQ , Ethernet
Part Number	000000-00
Operating System/Target	Real-Time , Windows
Measurement Type	Digital
RoHS Compliant	Yes
Analog Input	
Channels	0
Single-Ended Channels	0
Differential Channels	0
Analog Output	
Channels	0
Digital I/O	
Bidirectional Channels	8
Input-Only Channels	0

Output-Only Channels	0
Number of Channels	0 , 8
Timing	Hardware
Max Clock Rate	10 MHz
Logic Levels	TTL
Supports Handshaking I/O?	Yes
Supports Pattern I/O?	Yes
Maximum Input Range	0 V , 5.25 V
Maximum Output Range	0 V , 5.25 V
Counter/Timers	
Counters	0
Physical Specifications	
Length	9 cm
Width	2.3 cm
I/O Connector	25-pin D-Sub
Minimum Operating Temperature	-40 °C
Maximum Operating Temperature	70 °C
Minimum Storage Temperature	-40 °C
Maximum Storage Temperature	85 °C
Timing/Triggering/Synchronization	
Triggering	Digital
Triggers cDAQ Chassis	Yes

Isolation amplifier for the voltage transducers.

ANALOG DEVICES

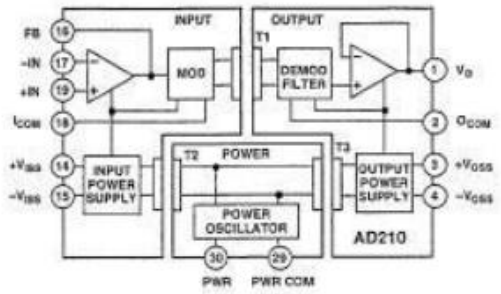
Precision, Wide Bandwidth 3-Port Isolation Amplifier

AD210*

FEATURES
High CMV Isolation: 2500 V rms Continuous
±3500 V Peak Continuous
Small Size: 1.00" × 2.10" × 0.350"
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20 kHz Full-Power (–3 dB)
Low Gain Drift: ±25 ppm/°C max
High CMR: 120 dB (G = 100 V/V)
Isolated Power: ±15 V @ ±5 mA
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD210 is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15 V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multichannel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may other vise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500 V rms (Continuous) and ± 3500 V peak (Continuous) common-mode voltage isolation between any two ports. Low input capacitance of 5 pF results in a 120 dB CMR at a gain of 100, and a low leakage current (2 µA rms max @ 240 V rms, 60 Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ±25 ppm/°C max and input offset drift of (±10 ±30/G) µV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20 kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00" × 2.10" × 0.350". The low profile DIP package allows application in 0.5" card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15 V @ 5 mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required and facilitates many alternative input functions as required by the user.

*Covered by U.S. Patent No. 4,703,285.

REV. A

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Tel: 617/329-4700 Fax: 617/326-8703

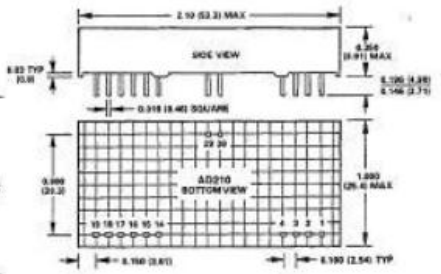
AD210–SPECIFICATIONS (typical @ +25°C, and V_S = +15 V unless otherwise noted)

Model	AD210AN	AD210BN	AD210JN
GAIN			
Range	1 V/V – 100 V/V	*	*
Error	±2% max	±1% max	*
vs. Temperature(0°C to +70°C)	+25 ppm/°C max	*	*
(–25°C to +85°C)	±50 ppm/°C max	*	*
vs. Supply Voltage	±0.002%/V	*	*
Nonlinearity[1]	±0.025% max	±0.012% max	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10 V	*	*
Maximum Safe Differential Input	±15 V	*	*
Max. CMV Input-to-Output	*		
ac, 60 Hz, Continuous	2500 V rms	*	1500 V rms
dc, Continuous	±3500 V peak	*	±2000 V peak
Common-Mode Rejection	*		
60 Hz, G = 100 V/V	*		
R_S ≤ 500 Ω Impedance Imbalance	120 dB	*	*
Leakage Current Input-to-Output	*		
@ 240 V rms, 60 Hz	2 μA rms max	*	*
INPUT IMPEDANCE			
Differential	10^{12} Ω	*	*
Common Mode	5 GΩ‖5 pF	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	30 pA typ (400 pA max)	*	*
vs. Temperature (0°C to +70°C)	10 nA max	*	*
(–25°C to +85°C)	30 nA max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	5 pA typ (200 pA max)	*	*
vs. Temperature(0°C to + 70°C)	2 nA max	*	*
(–25°C to +85°C)	10 nA max	*	*
INPUT NOISE			
Voltage (1 kHz)	18 nV/√Hz	*	*
(10 Hz to 10 kHz)	4 μV rms	*	*
Current (1 kHz)	0.01 pA/√Hz	*	*
FREQUENCY RESPONSE			
Bandwidth (–3 dB)	*		
G = 1 V/V	20 kHz	*	*
G = 100 V/V	15 kHz	*	*
Settling Time (±10 mV, 20 V Step)	*		
G = 1 V/V	150 μs	*	*
G = 100 V/V	500 μs	*	*
Slew Rate (G = 1 V/V)	1 V/μs	*	*
OFFSET VOLTAGE (RTI)[2]			
Initial, @ +25°C	±15 ±(45/G) mV max	(±5 ±(15/G) mV max	*
vs. Temperature (0°C to +70°C)	(±10 ±(50/G) μV/°C	*	*
(–25°C to +85°C)	(±10 ±(50/G) μV/°C	*	*
RATED OUTPUT[3]			
Voltage, 2 kΩ Load	±10 V min	*	*
Impedance	1 Ω max	*	*
Ripple (Bandwidth = 100 kHz)	10 mV p-p max	*	*
ISOLATED POWER OUTPUTS[4]			
Voltage, No Load	±15 V	*	*
Accuracy	±10%	*	*
Current	±5 mA	*	*
Regulation, No Load to Full Load	See Text	*	*
Ripple	See Text	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15 V dc ± 5%	*	*
Voltage, Operating	+15 V dc ± 10%	*	*
Current, Quiescent	50 mA	*	*
Current, Full Load – Full Signal	80 mA	*	*
TEMPERATURE RANGE			
Rated Performance	–25°C to +85°C	*	*
Operating	–40°C to +85°C	*	*
Storage	–40°C to +85°C	*	*
PACKAGE DIMENSIONS			
Inches	1.00 × 2.10 × 0.350	*	*
Millimeters	25.4 × 53.3 × 8.9	*	*

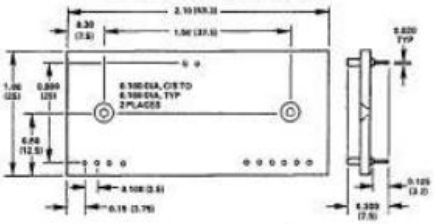
NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]RTI – Referred to Input.
[3]A reduced signal swing is recommended when both ±V_{ISS} and ±V_{OSS} supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 MATING SOCKET



AD210 PIN DESIGNATIONS

Pin	Designation	Function
1	V_O	Output
2	O_{COM}	Output Common
3	$+V_{OSS}$	+Isolated Power @ Output
4	$-V_{OSS}$	–Isolated Power @ Output
14	$+V_{ISS}$	+Isolated Power @ Input
15	$-V_{ISS}$	–Isolated Power @ Input
16	FB	Input Feedback
17	–IN	–Input
18	I_{COM}	Input Common
19	+IN	+Input
29	Pwr Com	Power Common
30	Pwr	Power Input

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD210 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

1) The input circuit of the voltage transducer card, (UMAT2), is designed in accordance to Fig 5. By omitting components and make a few steps, a circuit like Fig 2 can be achieved.

INSIDE THE AD210

The AD210 basic block diagram is illustrated in Figure 1. A +15 V supply is connected to the power port, and ±15 V isolated power is supplied to both the input and output ports via a 50 kHz carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The fullwave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A 20 kHz, three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a 2 kΩ load.

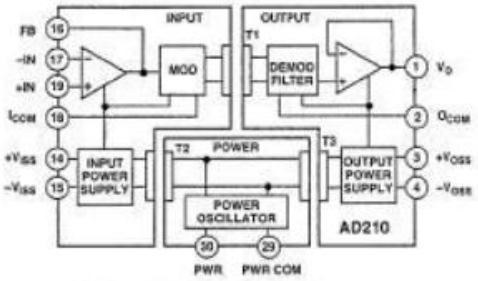


Figure 1. AD210 Block Diagram

USING THE AD210

The AD210 is very simple to apply in a wide range of applications. Powered by a single +15 V power supply, the AD210 will provide outstanding performance when used as an input or output isolator, in single and multichannel configurations.

Input Configurations: The basic unity gain configuration for signals up to ±10 V is shown in Figure 2. Additional input amplifier variations are shown in the following figures. For smaller signal levels Figure 3 shows how to obtain gain while maintaining a very high input impedance.

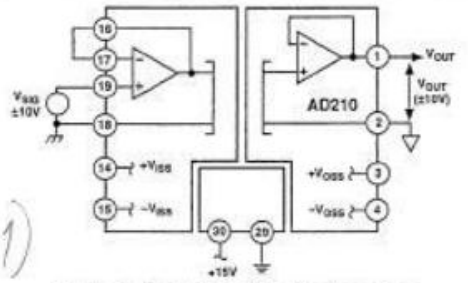


Figure 2. Basic Unity Gain Configuration

The high input impedance of the circuits in Figures 2 and 3 can be maintained in an inverting application. Since the AD210 is a three-port isolator, either the input leads or the output leads may be interchanged to create the signal inversion.

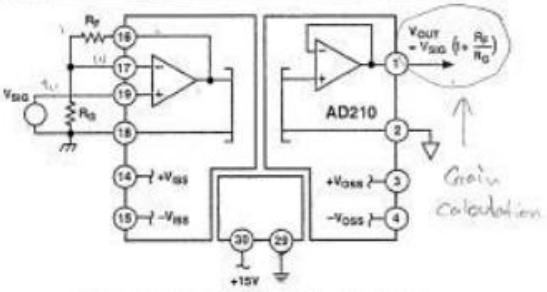


Figure 3. Input Configuration for G > 1

Figure 4 shows how to accommodate current inputs or sum currents or voltages. This circuit configuration can also be used for signals greater than ±10 V. For example, a ±100 V input span can be handled with R_F = 20 kΩ and R_{S1} = 200 kΩ.

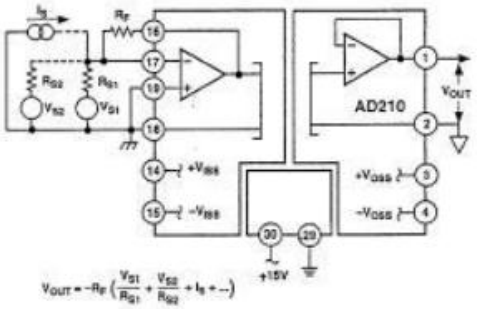


Figure 4. Summing or Current Input Configuration

Adjustments

When gain and offset adjustments are required, the actual circuit adjustment components will depend on the choice of input configuration and whether the adjustments are to be made at the isolator's input or output. Adjustments on the output side might be used when potentiometers on the input side would represent a hazard due to the presence of high common-mode voltage during adjustment. Offset adjustments are best done at the input side, as it is better to null the offset ahead of the gain.

Figure 5 shows the input adjustment circuit for use when the input amplifier is configured in the noninverting mode. This offset adjustment circuit injects a small voltage in series with the

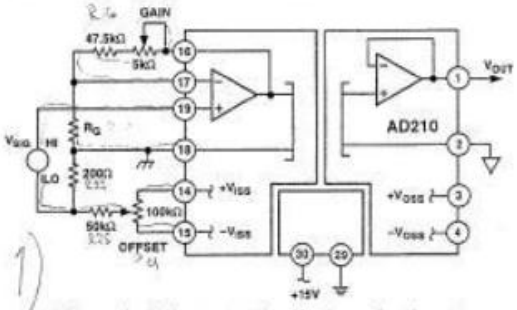


Figure 5. Adjustments for Noninverting Input

low side of the signal source. This will not work if the source has another current path to input common or if current flows in the signal source LO lead. To minimize CMR degradation, keep the resistor in series with the input LO below a few hundred ohms.

Figure 5 also shows the preferred gain adjustment circuit. The circuit shows R_P of 50 kΩ, and will work for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_P at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input impedance; it is better to adjust gain at the signal source or after the output.

Figure 6 shows the input adjustment circuit for use when the input amplifier is configured in the inverting mode. The offset adjustment nulls the voltage at the summing node. This is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is made in the feedback and will work for gains from 1 V/V to 100 V/V.

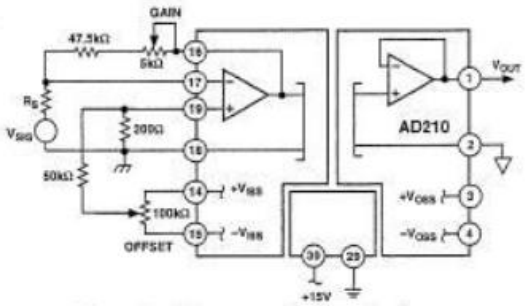


Figure 6. Adjustments for Inverting Input

Figure 7 shows how offset adjustments can be made at the output, by offsetting the floating output port. In this circuit, ±15 V would be supplied by a separate source. The AD210's output amplifier is fixed at unity, therefore, output gain must be made in a subsequent stage.

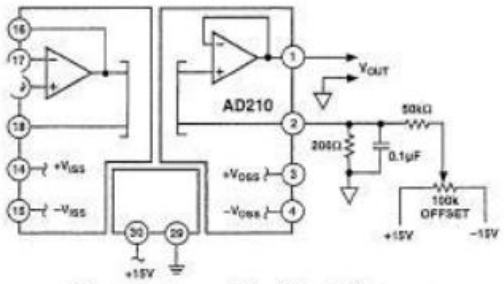


Figure 7. Output-Side Offset Adjustment

PCB Layout for Multichannel Applications: The unique pinout positioning minimizes board space constraints for multichannel applications. Figure 8 shows the recommended printed circuit board layout for a noninverting input configuration with gain.

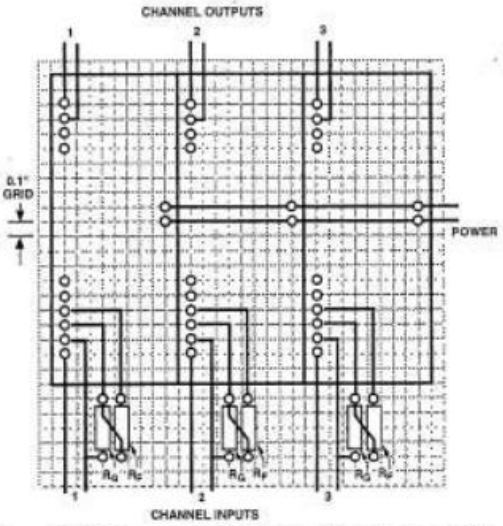


Figure 8. PCB Layout for Multichannel Applications with Gain

Synchronization: The AD210 is insensitive to the clock of an adjacent unit, eliminating the need to synchronize the clocks. However, in rare instances channel to channel pick-up may occur if input signal wires are bundled together. If this happens, shielded input cables are recommended.

PERFORMANCE CHARACTERISTICS

Common-Mode Rejection: Figure 9 shows the common-mode rejection of the AD210 versus frequency, gain and input source resistance. For maximum common-mode rejection of unwanted signals, keep the input source resistance low and carefully lay out the input, avoiding excessive stray capacitance at the input terminals.

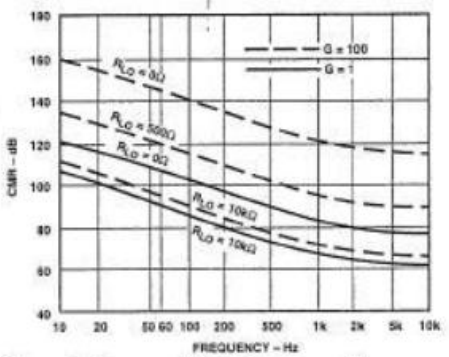


Figure 9. Common-Mode Rejection vs. Frequency

LEM Current transducer

LEM

Current Transducer LA 50-S/SP1

I_{PN} = 50 A

For the electronic measurement of currents : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

Electrical data

I_{PN}	Primary nominal r.m.s. current		50	A
I_P	Primary current, measuring range		0 .. ± 100	A
R_M	Measuring resistance		R_{Mmin} R_{Mmax}	
	with ± 15 V	@ ± 50 A_{max}	0 330	Ω
		@ ± 100 A_{max}	0 100	Ω
I_{SN}	Secondary nominal r.m.s. current		25	mA
K_N	Conversion ratio		1 : 2000	
V_C	Supply voltage (± 5 %)		± 15	V
I_C	Current consumption		10 + I_S	mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 min		3	kV

Accuracy - Dynamic performance data

X_G	Overall accuracy @ I_{PN}, T_A = 25°C		± 0.5		%
ε_L	Linearity		< 0.1		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.1	mA
I_{OT}	Thermal drift of I_O	- 10°C .. + 70°C	± 0.2	± 0.4	mA
t_r	Response time [1] @ 90 % of I_{PN}		< 1		µs
di/dt	di/dt accurately followed		> 50		A/µs
f	Frequency bandwidth (- 1 dB)		DC .. 150		kHz

General data

T_A	Ambient operating temperature	- 10 .. + 70	°C
T_S	Ambient storage temperature	- 25 .. + 85	°C
R_S	Secondary coil resistance @ T_A = 70°C	130	Ω
m	Mass	45	g
	Standards [2]	EN 50178	

Features

- Closed loop (compensated) current transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Special features

- I_P = 0 .. ± 100 A
- K_N = 1 : 2000

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

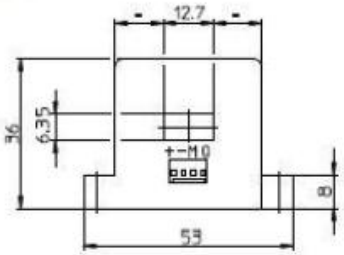
- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Notes : [1] With a di/dt of 50 A/µs
[2] A list of corresponding tests is available.

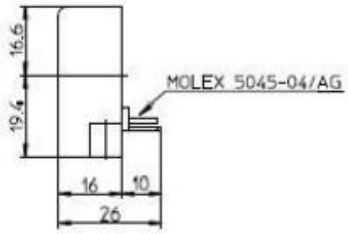
991014/5

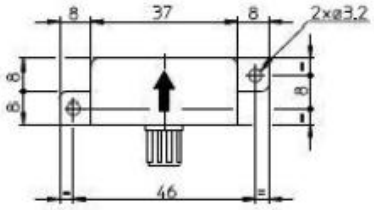
Dimensions LA 50-S/SP1 (in mm. 1 mm = 0.0394 inch)

Front view



Left view



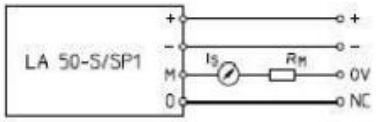


Top view

Secondary terminals

Terminal + : supply voltage + 15 V
Terminal - : supply voltage - 15 V
Terminal M : measure
Terminal 0 : NC

Connection



Mechanical characteristics

• General tolerance	± 0.2 mm
• Fastening	2 holes Ø 3.2 mm
• Primary through-hole	12.7 x 6.35 mm
• Connection of secondary	Molex 5045-04/AG

Remarks

- I_s is positive when I_p flows in the direction of the arrow.
- Temperature of the primary conductor should not exceed 100°C.
- Dynamic performances (di/dt and response time) are best with a single bar completely filling the primary hole.
- In order to achieve the best magnetic coupling, the primary windings have to be wound over the top edge of the device.
- To measure nominal currents of less than 50 A, the optimum accuracy is obtained by having several primary turns (nominal current x number of turns < 50 At).

Semistack Semikron inverter

SEMISTACK - IGBT

SEMITRANS Stack[1)]

Circuit	I_{rms} (A)	V_{ac} / V_{dcmax}	Types
B6CI	30	440 / 750	SEMITEACH - IGBT

Symbol	Conditions	Values	Units
I_{rms}	no overload	30	A
	IGBT - 4x SKM 50 GB 123D		
V_{CES}		1200	V
$V_{CE(SAT)}$	I_C= 50A, V_{GE}= 15V, chip level; T_j= 25(125)°C	2,7 (3,5)	V
V_{GES}		±20	V
I_C	T_{case}= 25 (80)°C	50 (40)	A
I_{CM}	T_{case}= 25 (80)°C; t_p= 1ms	100 (80)	A
	Rectifier - 1x SKD 51/14		
$V_{In(max)}$	without filter	3 x 480	V
	with filter	3 x 380	V
	DC Capacitor bank - Electrolytic 2x 2200µF/400V		
C_{eqvl}	total equivalent capacitance	1100 / 800	µF / V
V_{DCmax}	max. DC voltage applied to the capacitor bank	750	V
	Driver - 4x SKHI 22		
Power supply		0 / 15	V
Current consumption	max; per driver	16	mA
Thermal trip	Normally Open type (NO)	71	°C

Three-phase rectifier + inverter with brake chopper

SEMITEACH - IGBT
SKM 50 GB 123D
SKD 51
P3/250F

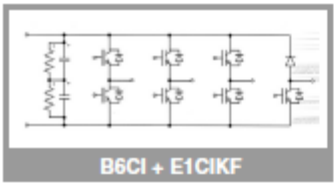
Features

- Multi-function IGBT converter
- Transparent enclosure to allow visualization of every part
- IP2x protection to minimize safety hazards
- External banana/BNC type connectors for all devices
- Integrated drive unit offering short-circuit detection/cut-off, power supply failure detection, interlock of IGBTs + galvanic isolation of the user
- Forced-air cooled heatsink

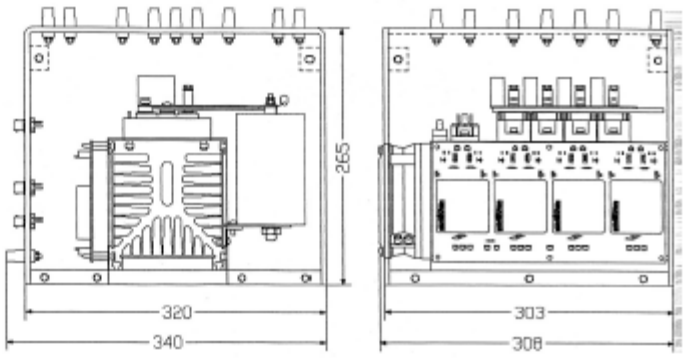
Typical Applications

- Education: One stack can simulate almost all existing industrial applications:
  - 3-phase inverter+brake chopper
  - Buck or boost converter
  - Single phase inverter
  - Single or 3-phase rectifier

[1)] Photo non-contractual



B6CI + E1CIKF



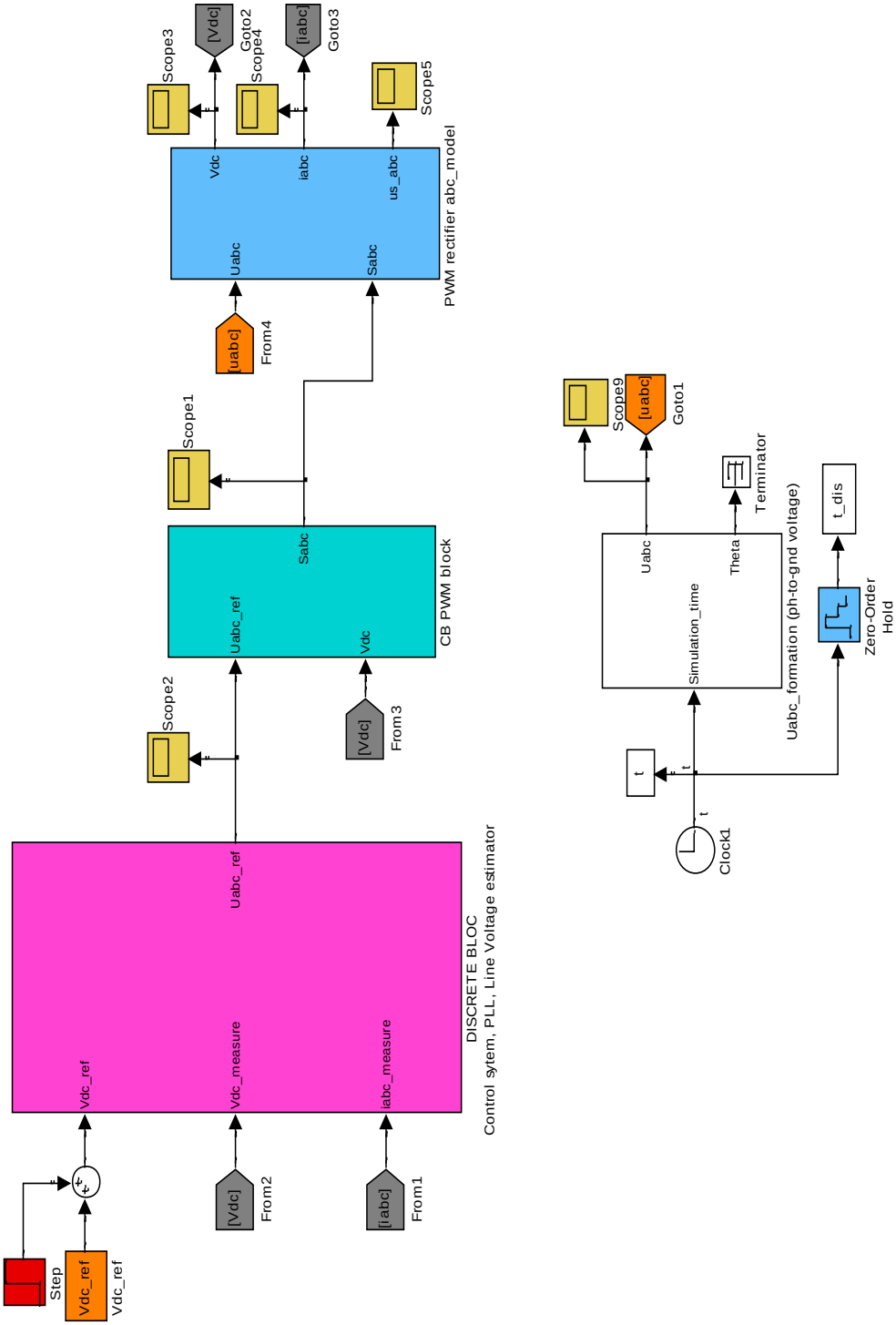
General dimensions

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.

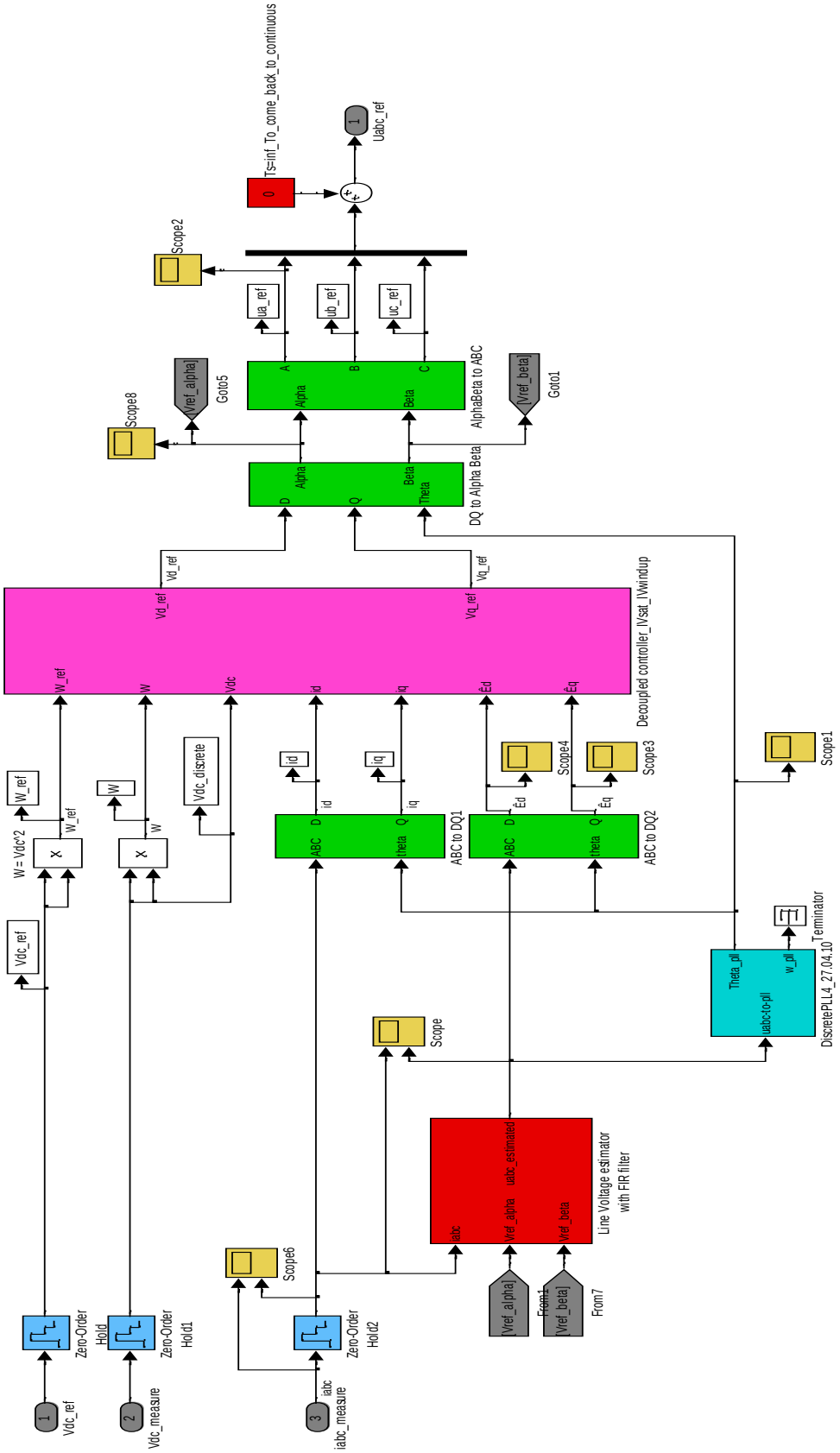
2 Power Electronic Systems – SEMISTACK 08-06-2005 © by SEMIKRON

Appendix B: Simulink simulations.

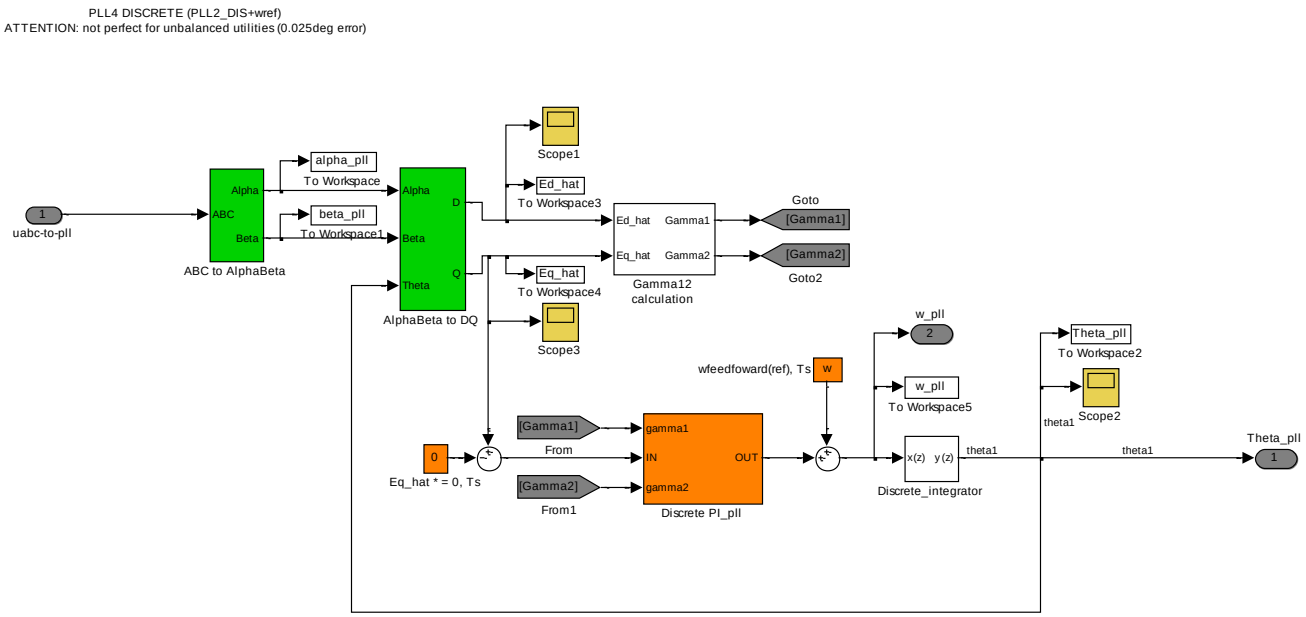
Complete simulation scheme.



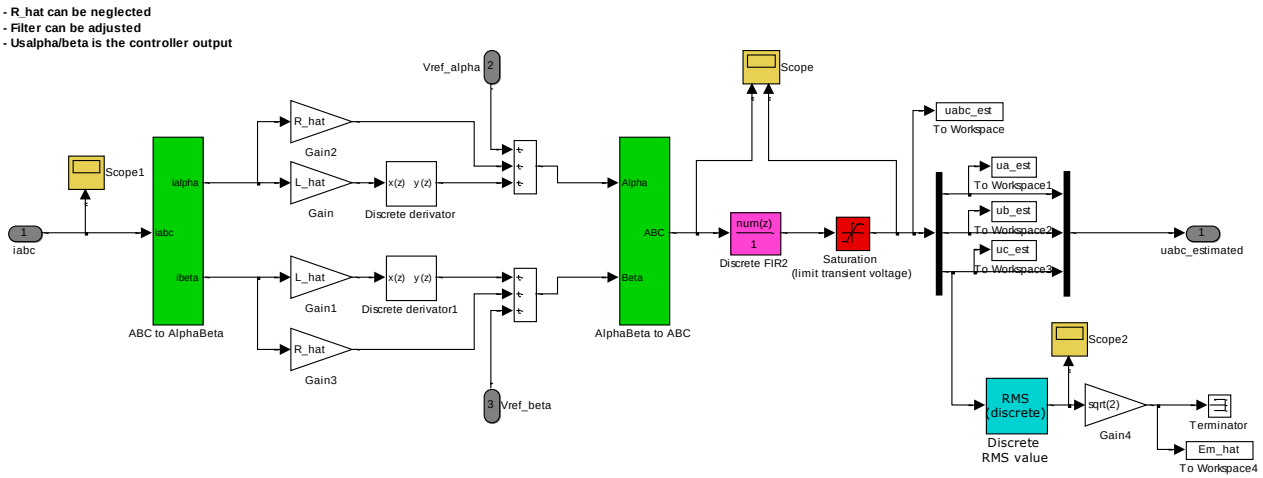
PLL, Line voltage estimator and decoupled controller.



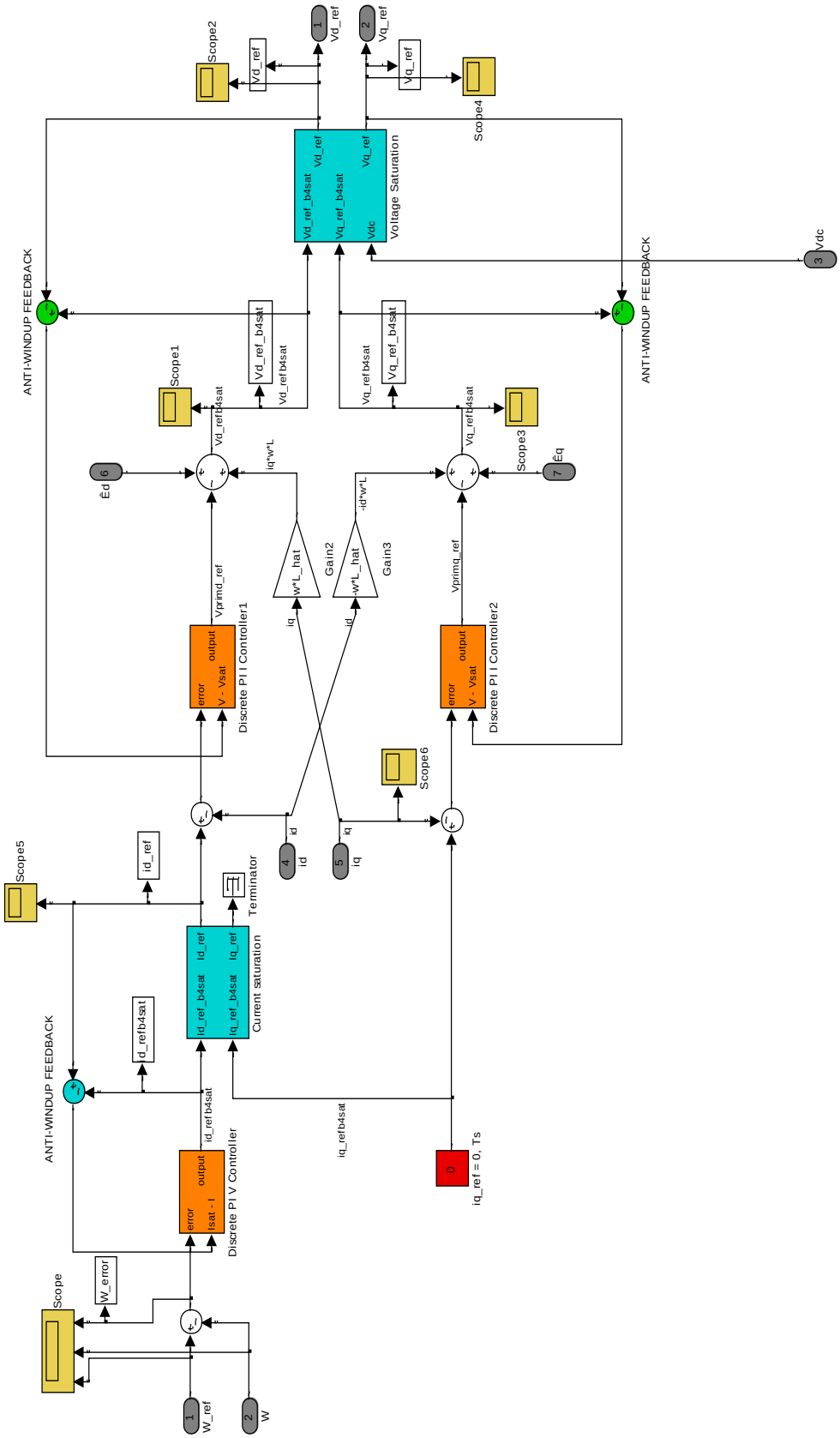
PLL discrete block.



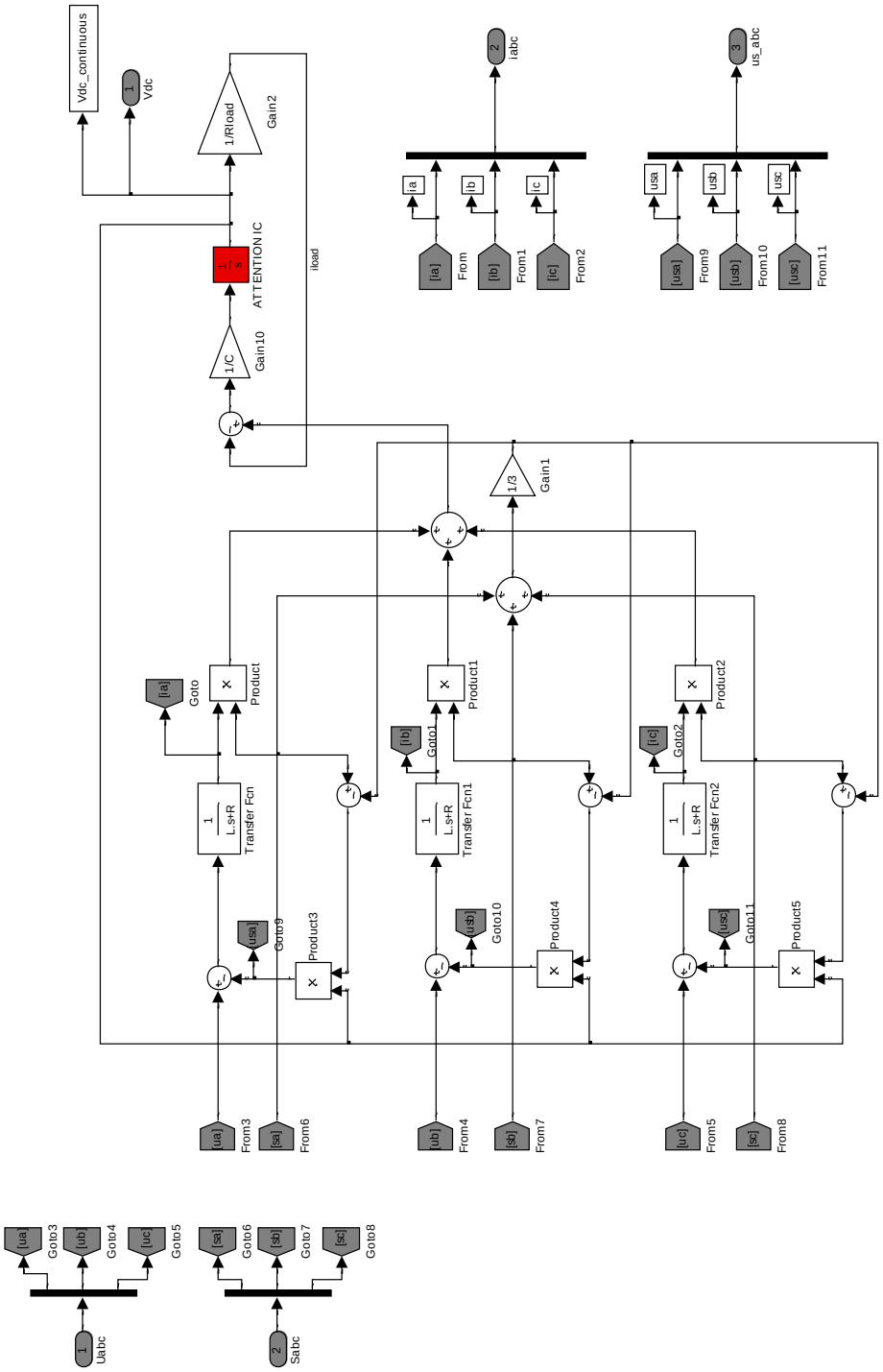
Line voltage estimator.



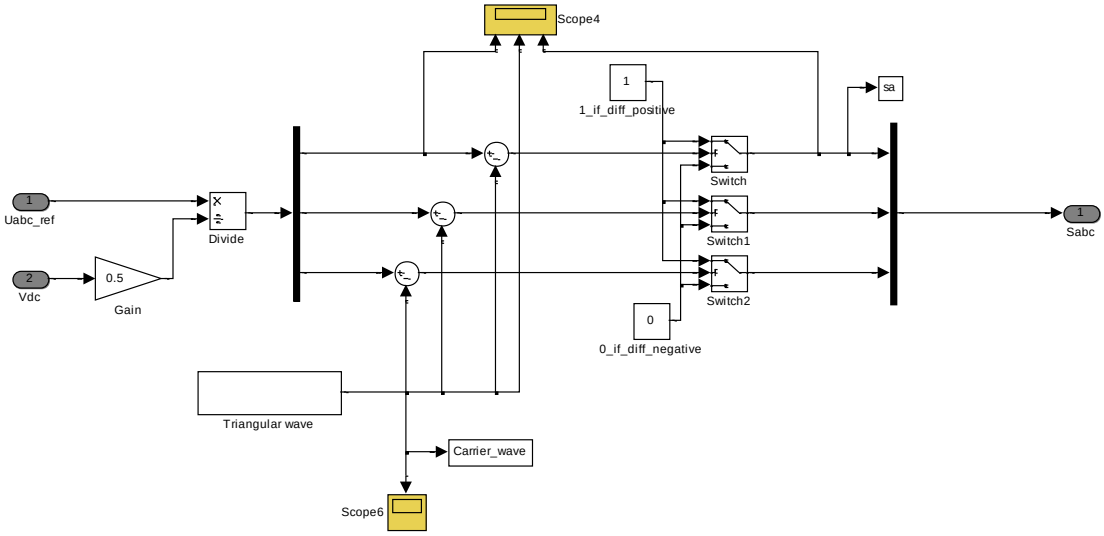
Decoupled controller.



Rectifier model.



PWM discrete block.



Matlab code.

```
%*************************************************************************
%          INITIALISATION FILE - Controller+PLL+Uest (Discrete Model)
%
%*************************************************************************
close all; clear all; clc

%*************************************************************************
% CARRIER BASED PWM PARAMETERS
%*************************************************************************
Carrier_amp = 1;    % Triangular wave Amplitude
Carrier_f = 10e3;   % Triangular wave frequency
Tc = 1/Carrier_f;   % Triangular wave period

%*************************************************************************
% CONVERTER PARAMETERS
%*************************************************************************
R = 0.1;            % Line Resistance (Kazmierkowski abc model)
L = 3e-3;           % Line inductance (Kazmierkowski abc model)
C = 1100e-6;        % DC bus capacitor
w = 2*pi*50;        % Line frequency
Em = 230*sqrt(2);   % Peak Phase voltage of the source (Kazmierkowski abc
model, need to be estimated)
Fsw = Carrier_f;    % Converter switching frequency = Triangular wave frequ.
Rload = 33;        % Output load, Pout about 800W
Vdc_ref = 700;      % Output voltage reference (5.8 3.6 ratio w Em)
initial_condition_integrator = Vdc_ref; % IC model integrator


%*************************************************************************
% PLL PARAMETERS
%*************************************************************************
%Gain gamma1&2 : calculated in simulink (we assume Ed_hat and Eq_hat can
change)
Fbandwidth_pll = 20;             %bandwidth in Hz
rho_pll = 2*pi*Fbandwidth_pll;   %bandwidth in rad/s

%*************************************************************************
% CONTROLLER PARAMETERS
%*************************************************************************
Ts = 0.5*Tc;   % Sample time, half of triangular wave period, Fs = 2*Fc

%ESTIMATED PARAMETERS
R_hat = R;
L_hat = L;
C_hat = C;     % probably, C_hat = C OK
Em_hat = Em ; % ATTENTION : will be a problem for Kpv (need to put fixed
value of do calculation in Simulink according to estimator value)

%CURRENT PI Regulator (thesis, state-variable W=Vdc^2)
alphaI = Fsw/10*2*pi;      % Bandwidth in rad/s (2000Hz)
Kpi = alphaI*L_hat
Kii = alphaI*R_hat

%VOLTAGE PI Regulator (thesis, state-variable W=Vdc^2)
alphaV = Fsw/100*2*pi;     % Bandwidth in rad/s (200Hz)
Kpv = alphaV*C_hat/(3*Em_hat)
```

```
Kiv = 0.01
%SATURATION (TO MODIFY, depends on rectifier limit)
Isaturation_upper_limit = 50; %saturation on Iref, V PI controller
Isaturation_lower_limit = -50;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% LINE VOLTAGE ESTIMATOR
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
IC_delayestimator_a = 0.1;
IC_delayestimator_b = 0;
Est_Vsaturation_upper_limit = 1.2*Em_hat; %ATTENTION : Need to put a fixed
value for implementation (or calcul in simulink)
Est_Vsaturation_lower_limit = -1.2*Em_hat;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% TESTS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%INPUT STEP
input_step_time = 0.2;
input_step_value = 50;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% SIMULATION AND DISPLAY
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
sim('Discrete_Model')

figure(1)
subplot(2,2,1); plot(t_dis, id_refb4sat,'r'); axis([0 0.4 -5 100]);
xlabel('Time (s)'); ylabel('Current (A)'); title('Id reference before
saturation', 'fontsize',16)
subplot(2,2,2); plot(t_dis,id,'r',t_dis,iq,'b'); axis([0 0.4 -5 60]);
xlabel('Time (s)'); ylabel('Current (A)'); title('Id(red) Iq(blue)',
'fontsize',16)
subplot(2,2,3); plot(t_dis, id_ref,'r');axis([0 0.4 -5 60]); xlabel('Time
(s)'); ylabel('Current (A)'); title('Id reference', 'fontsize',16)
subplot(2,2,4); plot(t,ia,'r',t,ib,'b',t,ic,'k'); axis([0 0.4 -60 60]);
xlabel('Time (s)'); ylabel('Current (A)'); title('Ia Ib Ic', 'fontsize',16)

figure(2)
subplot(3,1,1); plot(t_dis,Vd_ref_b4sat,'r',t_dis,Vq_ref_b4sat,'b');
axis([0 0.4 -300 500]); xlabel('Time (s)'); ylabel('Voltage (V)');
title('Vd(red) Vq(blue) (reference before saturation)', 'fontsize',16)
subplot(3,1,2); plot(t_dis,Vd_ref,'r',t_dis,Vq_ref,'b'); axis([0 0.4 -400
400]); xlabel('Time (s)'); ylabel('Voltage (V)'); title('Vd(red) Vq(blue)
(reference)', 'fontsize',16)
subplot(3,1,3);
plot(t_dis,ua_ref,'r',t_dis,ub_ref,'b',t_dis,uc_ref,'k');axis([0 0.4 -400
400]); xlabel('Time (s)'); ylabel('Voltage (V)'); title('Ua Ub Uc
(reference)', 'fontsize',16)

figure(3)
subplot(2,1,1); plot(t_dis,id,'r',t_dis, id_ref,'b');axis([0 0.4 -5 60]);
xlabel('Time (s)'); ylabel('Current (A)'); title('Id reference (blue) and
Id (red)', 'fontsize',16)
subplot(2,1,2);
plot(t_dis,sqrt(abs(W_ref)),'r',t_dis,sqrt(abs(W)),'b');axis([0 0.4 0
800]); xlabel('Time (s)'); ylabel('Voltage (V)'); title('Vdc (black) and
Vdc reference (red)', 'fontsize',16)
```