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Impact of photon lifetime on thermal rollover in 850-nm high-speed VCSELs

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ABSTRACT

We present an empirical thermal model for VCSELs based on extraction of temperature dependence of macroscopic VCSEL parameters from CW measurements. We apply our model to two, oxide-confined, 850-nm VCSELs, fabricated with a 9-μm inner-aperture diameter and optimized for high-speed operation. We demonstrate that for both these devices, the power dissipation due to linear heat sources dominates the total self-heating. We further show that reducing photon lifetime down to 2 ps drastically reduces absorption heating and improves device static performance by delaying the onset of thermal rollover. The new thermal model can identify the mechanisms limiting the thermal performance and help in formulating the design strategies to ameliorate them.

Keywords: vertical cavity surface emitting lasers, thermal effects, carrier leakage, photon lifetime.

1. INTRODUCTION

High-speed, vertical-cavity surface-emitting lasers (VCSELs) operating at 850 nm, with data rates as high as 40 Gb/s[1,2] are being developed for diverse applications including high-performance computing, optical interconnects, and consumer electronics.[1,3,4] The fact that commercial multimode fibers and polymer waveguides are optimized for the 850-nm wavelength band[5] has also significantly contributed to the rapid pace of their development.

Compared to their other short-wavelength counterparts (980-1100 nm),[6] pushing the data-rate of 850-nm VCSELs to beyond 40 Gbit/s has posed multiple technological challenges. Significant work had to be done to enhance the data-transmission rates and distances for devices operating in this wavelength regime.[7–13] Optimization of the active-region design for high differential gain has been achieved through the use of strained quantum wells. In the GaAs material system, compressive strain is incorporated by adding indium to the gain material. This causes a red-shift of the gain-peak, which in-turn has to be compensated by increasing the Al content in the barrier material and reducing the quantum well width.[7] However, the reduced quantum well width enhances carrier leakage[14] which further worsens progressively with increasing device temperatures. This in-turn limits the high-speed operation.[15] Reduction in K-factor has been achieved by reducing the photon-lifetime,[8] increasing differential gain,[13] and reducing the gain-compression coefficient. Reduction in gain-compression coefficient is achieved by optimizing the separate-confinement hetero-structure (SCH) region for a short carrier capture time.[9] The pad and mesa capacitances have been minimized by using low-k dielectric material such as benzo-cyclo-butene (BCB)[10] or polyimide[11,12] and by employing multiple oxide layers,[8] respectively.

Among all these techniques, the reduction of photon lifetime through a shallow surface etch in the top DBR has lead to the most dramatic improvement in both the static and dynamic performance of 850-nm VCSELs.[8,16] In this paper, using an empirical thermal model for VCSELs based on extraction of temperature dependence of macroscopic VCSEL parameters from CW measurements, we study the impact of photon lifetime reduction on thermal degradation mechanisms in 850-nm VCSELs at different ambient temperatures.

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2. EMPIRICAL THERMAL MODEL

The details of our empirical thermal model can be found in a recent paper.[17] Briefly, our model relates the power dissipated as heat to macroscopic VCSEL parameters. The temperature dependence of these parameters is extracted from a few basic CW measurements. The total power dissipated as heat can be written as

$$P_{\text{tot}} = P_{\text{QPD}} + P_{\text{LPD}},\tag{1}$$

where P_{QPD}, or quadratic power dissipation, is the power dissipated across the series resistance (R_{s}):

$$P_{\text{QPD}} = R_{\text{s}}(T_{\text{a}}, I_b)I_b^2 = \frac{dV_{\text{b}}(T_{\text{a}}, I_b)}{dI_b}I_b^2.\tag{2}$$

Here, I_{b} is the bias current, T_{a} is the ambient temperature, and R_{s} has been replaced by the differential resistance ($dV_{\text{b}}/dI_{\text{b}}$) at a given bias voltage V_{b}. We have included a direct dependence of series resistance on bias current caused by charge accumulation at the hetero-interfaces in the distributed Bragg reflectors (DBRs) as well as power dissipated through voltage drop across the diode[18]; it leads to a reduction in R_{s} with I_{b}.[17]

P_{LPD}, or linear power dissipation, is the sum total of carrier thermalization, spontaneous carrier recombination, carrier leakage, and internal optical loss. It can be written as:

$$P_{\text{LPD}} = P_{\text{therm}} + P_{\text{rec}} + P_{\text{leak}} + P_{\text{abs}} = K(T)I_b.\tag{3}$$

where P_{therm} is the power dissipation from carrier thermalization, P_{rec} corresponds to spontaneous carrier recombination, P_{leak} corresponds to carrier leakage and P_{abs} corresponds to absorption of stimulated photons in the VCSEL cavity. Below lasing threshold, it is assumed that all spontaneous recombination events produce heat[17]. $K(T)$ is the LPD coefficient whose value also depends on the device temperature T (and as a consequence on both T_{a} and I_{b}). Here, $T = T_{\text{a}} + \Delta T$ is the sum of ambient temperature T_{a} and increase in the device temperature (ΔT) induced by the bias current. Henceforth, the value of any particular device parameter corresponds to a fixed T_{a} and I_{b} (unless specified otherwise).

Above lasing threshold, where self-heating becomes significant, the LPD coefficient $K(T)$ can be expressed in terms of macroscopic VCSEL parameters as:[17]

$$K(T) = \frac{1}{q}E_B(T) - \frac{1}{q}E_L(T)\eta_i(T)[1 - \{I_{\text{th}}(T)/I_b\}] \times \left[1 - \frac{\alpha_i(T) + \alpha_m^B(T)}{\alpha_i(T) + \alpha_m^T(T) + \alpha_m^B(T)}\right],\tag{4}$$

where $E_B(T)$ and $E_L(T)$ are the temperature-dependent barrier-bandgap energy and laser-photon energy (in eV), respectively, q is the electron charge, $I_{\text{th}}(T)$ is the threshold current, $\eta_i(T)$ is the internal quantum efficiency, $\alpha_m^T(T)$ and $\alpha_m^B(T)$ are the optical losses through the top and bottom DBR, respectively, and $\alpha_i(T)$ is the internal cavity loss. The device temperature is obtained using the thermal impedance $R_{\text{th}}(T)$ which relates the change in T to the P_{tot} as[13]

$$T = T_{\text{a}} + \Delta T = T_{\text{a}} + R_{\text{th}}(T)\left[P_{\text{QPD}} + P_{\text{LPD}}\right].\tag{5}$$

Finally, the optical power emitted through the top DBR is calculated using:[18]

$$P_{\text{opt}}(T, I_b) = \frac{\eta_i(T)[I_b - I_{\text{th}}(T)]\alpha_m^T(T)}{\alpha_m^T(T) + \alpha_m^B(T) + \alpha_i(T)}\left(\frac{hc}{q\lambda(T)}\right).\tag{6}$$

where λ is the emission wavelength, c is the speed of light and h is the Planck constant. Equations (1) to (4) are used to calculate P_{tot} as a function of I_{b}. Equations (5) and (6) then provide variations in T and P_{opt} with I_{b}, respectively.

The temperature dependence of the macroscopic VCSEL parameters is found as follows: $E_{\text{B}}(T)$ is determined from the Varshini equations;[17, 19] $E_{\text{L}}(T)$ is estimated from temperature dependence of the lasing wavelength λ of the fundamental LP_{01} mode.[17] The measured value of $\Delta\lambda/\Delta T$ for all the device is around 0.06 nm/°C. This quantity is used to estimate the device temperature at various values of T_{a} and I_{b}. $I_{\text{th}}(T)$ is quantified from the measurements of the emitted optical power, voltage and emission wavelength as a function of the I_{b} over a range (15 to 100°C) of ambient temperatures.[17] The measurements are performed under CW conditions, and temperature dependence is extracted from data recorded at or just above threshold where self-heating can be assumed to be negligible ($T \approx T_{\text{a}}$).
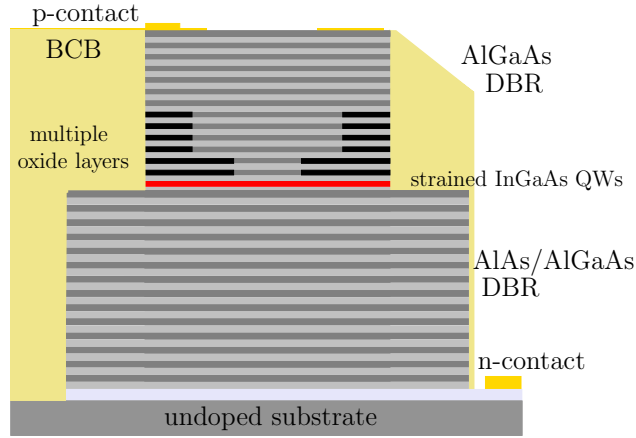
Figure 1. Schematic cross section of the high-speed 850-nm VCSELs used in the experiment. Benzo-cyclo-butene (BCB) is employed to reduce parasitic capacitance. Six layers are used for forming an oxide aperture (dark shading region).[16]

The internal optical loss, $\alpha_i(T)$, is extracted from the measured dependence of output power on bias current just above threshold for VCSELs with different top-DBR reflectivities. This reflectivity is varied by changing the thickness of the top layer (using dry etching), which controls the phase of the surface reflection.[8] By performing these measurements at different ambient temperatures, the temperature dependence of $\alpha_i(T)$ is obtained. Other methods for carrying out these measurements for any VCSEL have been previously reported.[20]

The temperature dependence of the internal quantum efficiency, $\eta_i(T)$, is also extracted from the measured P_{opt}–I_b curves. The slope efficiency (SE) is extracted from the P_{opt}–I_b curves at different ambient temperatures by averaging the slope dP_{opt}/dI_b over optical powers in the range of P_1 and P_2.[17] The choice of P_1 and P_2 is constrained such that the increase in the device temperature over this range should be negligible ($\Delta T \leq 5\,^\circ C$). Therefore, P_1 is chosen as emitted power at the lasing threshold at a particular ambient temperature and P_2 is chosen as 10% of the maximum emitted power at room temperature. The external differential quantum efficiency is then calculated using[18]

$$\eta_d(T) = \frac{q\lambda(T)}{hc}\,\text{SE}(T). \tag{7}$$

We then calculate $\eta_i(T)$ using the relation

$$\eta_d(T) = \frac{\eta_i(T)\alpha_m^T(T)}{[\alpha_m^T(T) + \alpha_m^B(T) + \alpha_i(T)]}. \tag{8}$$

Here, the temperature dependence of the transmission loss rates through the top and bottom DBRs is accurately calculated using an effective index model that takes into account the temperature dependence of the refractive index of the constituent layers of the DBRs.[8,21]

Finally, temperature dependence of the thermal impedance, $R_{th}(T)$, is estimated by measuring the change in the emission wavelength, and therefore the increase in the device temperature, with increasing dissipated power in the current range $I_b < 2I_{th}$ at different ambient temperatures.[12] This is done so that temperature increase due to bias-current induced self-heating is negligible.

3. CW MEASUREMENTS ON THE DEVICES UNDER TEST

The basic structure, common to both the VCSELs (without and with a 55-nm surface-etch in the top DBR), is shown in Fig. 1. It is grown on undoped GaAs substrates and employs an oxide-confined configuration optimized for high speed modulation.[16] The top and bottom DBRs are fabricated with graded interfaces and modulation doping to reduce their electrical resistance.[13] The bottom DBR is partly composed of AlAs to lower its thermal impedance.[8] The active region is made of five strained InGaAs quantum wells for improved differential gain[7] and is surrounded by a SCH designed for efficient carrier trapping and low gain-compression.[9,16] As indicated with dark shading in Fig. 1, six AlGaAs layers in the
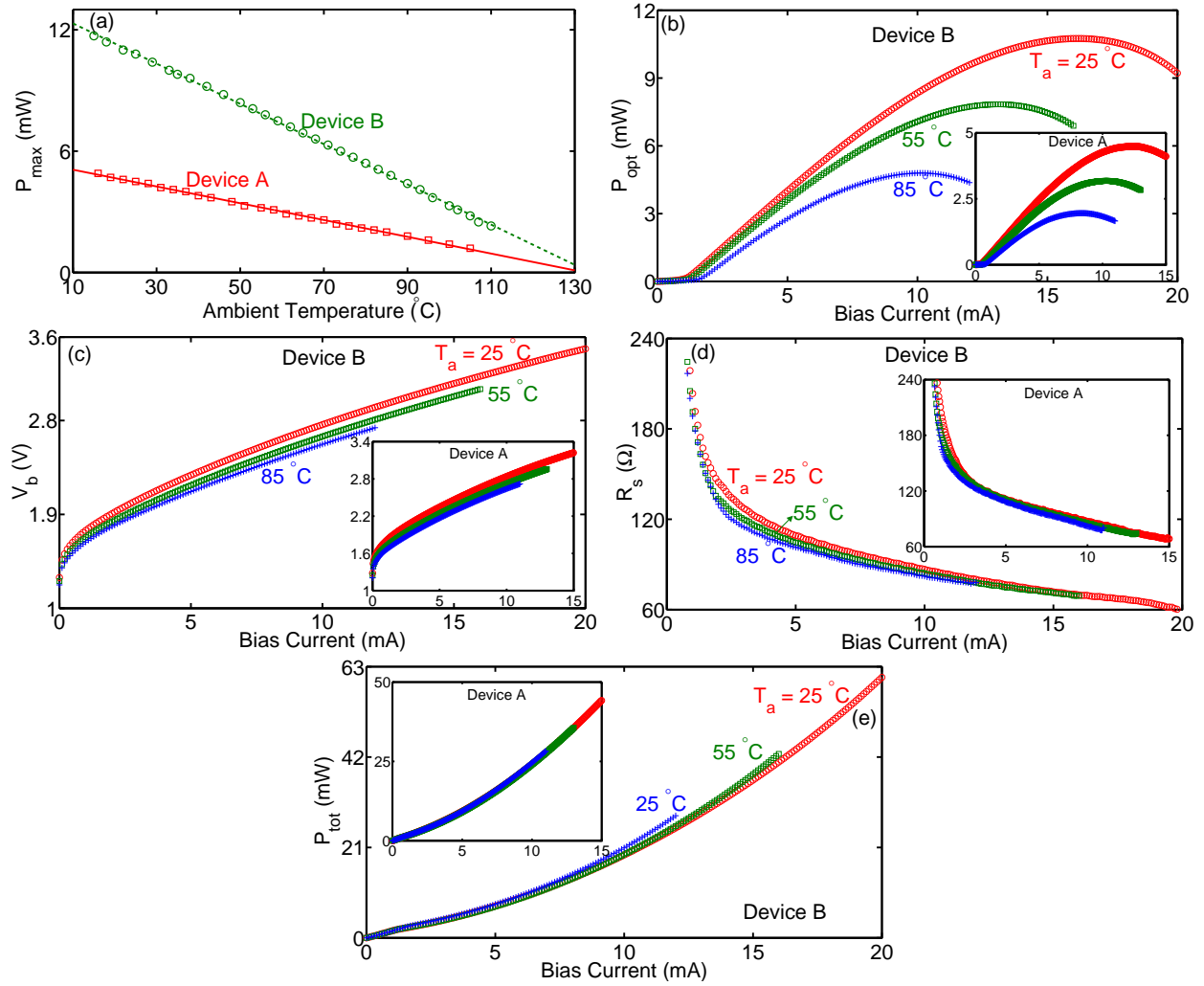
Figure 2. (a) P_{max} as a function of T_a for the two VCSELs. (b) P_{opt}, (c) V_b, (d) R_s, and (e) P_{tot} as a function of I_b at $T_a = 25, 55$, and 85 °C. For parts (b)-(e), the main figures correspond to device B (55 nm surface etch) and the inset figures correspond to device A (0 nm surface etch in the top DBR).

lower part of the top DBR are composed of high Al-content (98% for the bottom two and and 96% for the remaining four) to form a small oxide aperture for current and optical confinement and a larger oxide aperture (twice the inner aperture diameter) for reducing device capacitance.[8] In a second dry-etching process, the bottom contact layer is reached and the n-contact layers are evaporated. The etched mesas are embedded in a low-k dielectric (BCB) to further reduce the parasitic capacitances.[10, 13] After the bondpad sputtering, a shallow surface etch is made in selected VCSEL to optimize top-DBR reflectivity (and consequently the cavity photon lifetime). The two devices analyzed in this work have a 9-μm inner aperture diameter. The device with no surface etch is henceforth designated device A and the device with 55 nm surface etch is designated device B. Devices A and B correspond to photon-lifetime of 6.8 and 1.4 ps respectively at 55 °C ambient temperature.

To perform CW measurements, the two VCSELs were placed on a copper stage with active temperature control. The emitted optical power was detected by a calibrated, large-area photodiode (UDT Sensors PIN-10D) for accurate measurements. Measurements were performed over an ambient temperature range of 15-100 °C. For spectral measurements, the light was coupled into a multimode fiber that was connected to an optical spectrum analyzer. All spectral measurements were performed with 0.1 nm resolution. As a result, device temperatures deduced from the spectral data are accurate to within 1.6 °C.

Table 1. Parameter values at T_a = 55 °C for the two VCSELs

Device	λ (nm)	R_{th} (°C/mW)	α_i (ps^{-1})	α_m^T (ps^{-1})	α_m^B (ps^{-1})	T_{max} (°C)	T_{cr}
A	852.7 ± 0.33	2.07 ± 0.035	(8.3 ± 0.22) × 10^{-2}	0.0578	6.08 × 10^{-3}	133	153
B	853.9 ± 0.32	1.97 ± 0.022	(8.3 ± 0.22) × 10^{-2}	0.653	6.08 × 10^{-3}	134	145

Experimental data from CW measurements is presented in Fig. 2. Part (a) shows the maximum emitted optical power (P_{max}) as a function of T_a. A straight line can be fitted to these measurements for both these devices. At T_a corresponding to P_{max} = 0, each VCSEL stops lasing. It is important to note that the internal device temperature under such conditions is higher than T_a. Our VCSELs are projected to stop lasing in the vicinity of 130 °C. This indicates that the cut-off temperature strongly depends on VCSEL cavity design. From this point on, we present measurements and simulations corresponding to T_a = 25, 55, 85 °C. The choice of these three temperatures allows us to study the impact of photon lifetime on thermal degradation mechanisms in high-speed, 850-nm VCSELs across a broad range of ambient temperatures.

Parts (b)-(e) of Fig. 2 show P_{opt}, V_b, R_s, and P_{tot} as a function of I_b, respectively, under CW operation at the three ambient temperatures. The main figures correspond to device B and the inset figures correspond to device A. Comparing devices A and B with the same inner aperture diameter (9 μm), as the shallow surface etch in the top DBR is increased from 0 to 55 nm, the transmission-loss rate increases from 0.058 to 0.653 ps^{-1}. As shown in Fig. 2(b), this in turn causes P_{max} and I_b corresponding to P_{max} to increase. Over a broad range of ambient temperatures (15-100 °C), the increase in P_{max} is between 145 and 135% with no obvious trend, whereas the increase in I_b corresponding to P_{max} decreases in a linear fashion from 26% to 13% . This behaviour indicates that the performance enhancement from photon lifetime reduction is being countered through some other physical mechanism, particularly at higher ambient temperatures. This issue will be discussed in detail in the subsequent sections of this manuscript.

Electrically, these two devices are identical (a shallow surface etch in the top DBR has an insignificant effect on electrical properties). This leads to almost identical R_s for the two devices over the entire range of T_a and I_b, as shown in the inset of Fig. 2(d). Finally, comparing the rate of increase of P_{tot} with I_b for the two devices [Fig. 2(e)], it can be seen that power dissipated as heat in device A exceeds that in device B at any ambient temperature and bias current. In subsequent sections, the origin of this excess power dissipation will be discussed.

Tables 1 and 2 summarize the values of the parameters of the two devices at T_a = 55 °C as well as their temperature dependence deduced from the measurements. It also summarizes the errors in the corresponding measured values. It is important to understand the sources of errors in these extracted values. The uncertainty in the value of α_m^T is related to the ±2 nm uncertainty in the surface etch depth. For the analysis presented here, it is ignored.[8] Bias-current-induced increase in device temperature[17] is a prominent source of error in the parameter values. It depends on the ambient temperature T_a owing to the temperature dependence of thermal impedance [see Eq. (5)] and increasing difficulty in stabilizing high stage temperatures against room temperature. At low ambient temperatures, the error in the extracted parameter values corresponds to the resolution limit of the device thermometer which is limited by the resolution of the optical spectrum analyzer.[13,17] Assuming a worst-case value of 5 °C at T_a = 100 °C for both the devices, the corresponding worst-case errors in the parameter values are given in Tables 1 and 2.

Table 2. The linear temperature dependence ($\triangle = \frac{\partial}{\partial T}$) of VCSEL parameters.

Device	$\triangle\lambda$ (nm/°C)	$\triangle R_{th}$ (mW^{-1})	$\triangle\alpha_i$ (ps^{-1}/°C)	$\triangle\alpha_m^T$ (ps^{-1}/°C)	$\triangle\alpha_m^B$ (ps^{-1}/°C)
A	(6.077 ± 0.13) × 10^{-2}	(5.4 ± 0.4) × 10^{-3}	(4.167 ± 0.11) × 10^{-4}	−3.622 × 10^{-5}	−5.705 × 10^{-6}
B	(6.199 ± 0.14) × 10^{-2}	(3.0 ± 0.3) × 10^{-3}	(4.167 ± 0.11) × 10^{-4}	−3.643 × 10^{-4}	−5.705 × 10^{-6}

Temperature dependencies of internal quantum efficiency and threshold current (I_{th}) for the two devices were estimated from the measured P_{opt}-I_b curves.[18,22] I_{th} was calculated using a two-segment line-fit at any ambient temperature. This method is relatively insensitive to ambient-temperature induced changes in slope efficiency.[18,22] A parabolic fit to measurements is used to model the dependence of I_{th} on device temperature.[17] The maximum error in I_{th} is less than 2% for both the devices.
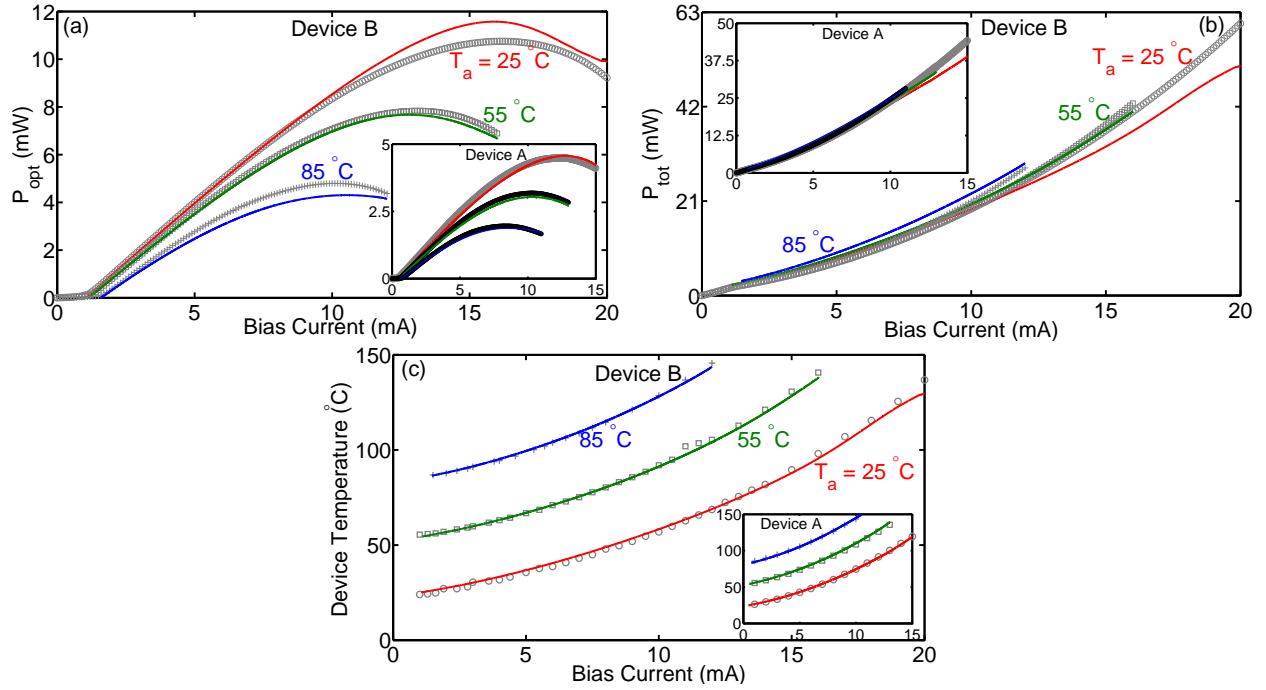
Figure 3. Comparison of predicted (colored lines) and measured values (gray symbols) of (a) P_{opt}, (b) P_{tot}, and (c) T as a function of I_b at $T_a = 25$, 55, and 85 °C. The main figures correspond to device B (55 nm surface etch) and the inset figures correspond to device A (0 nm surface etch) in the top DBR.

The temperature dependence of internal quantum efficiency is extracted using the method described in Section 2. A function of the form $\eta_i(T) = \eta_i(RT)/[1 + (T/T_{cr})^4]$ is used to numerically fit to the measurements;[17,22] $\eta_i(RT)$, where RT stands for room temperature, can be measured independently,[8,20] and T_{cr} is used as the fitting parameter. The values of T_{cr} are also summarized in Table 1. It is important to note that T_{cr} for any device is quite close to T_{max}, the temperature at which the corresponding VCSEL is projected to stop lasing [Table 1]. The maximum calculated error in the extracted value of η_i is less than 1%. Transmission losses through the top and the bottom DBR were calculated numerically using an effective index model.[17] Additional details on the methods described above, the origin of errors in their values, physical explanations behind the temperature dependence, and previously reported room temperature values can be found in.[8,13,17]

4. PREDICTIONS FROM THERMAL MODEL

In this section we use the parameter values extracted from CW measurements (see Tables 1 and 2) to study how these parameters influence the thermal rollover mechanisms. We also look at how selected VCSEL parameters evolve with increasing bias current and the influence of this evolution on thermal rollover behavior. We use the procedure outlined in section 2, together with the parameters listed in Tables 1 and 2, to simulate the basic VCSEL characteristics. Figure 3 shows the measured and predicted values of P_{opt}, P_{tot}, and T, respectively, as a function of I_b at $T_a = 25$, 55, and 85 °C for the two devices under test. The main figures correspond to device B and the inset figures correspond to device A with the same x and y axis. It can be seen in parts (a)-(c) that the quantitative agreement is not the same for two devices across the three ambient temperatures. However, the mismatch is less than 10%. We thus conclude that theoretical predictions based on Eqs. (1), (5), and (6) are in reasonable agreement with the measured data for both the devices over a broad range of ambient temperatures, across the entire range of I_b. This depicts the optical, electrical, and thermal consistency of our thermal model as well as quantifies the underlying accuracy of the derived temperature dependence of VCSEL parameters.

We next consider changes in selected VCSEL parameters with bias current to gain some insight into the origins of thermal rollover. In Fig. 4, we plot the variation of η_i and I_{th} with I_b for the two devices under test at three ambient temperatures. Figure 4 (a) corresponds to device A and part (b) corresponds to device B. Analyzing the evolution of internal quantum efficiency plotted on the left scale, it can be seen that at 25 °C ambient temperature, the value of η_i at
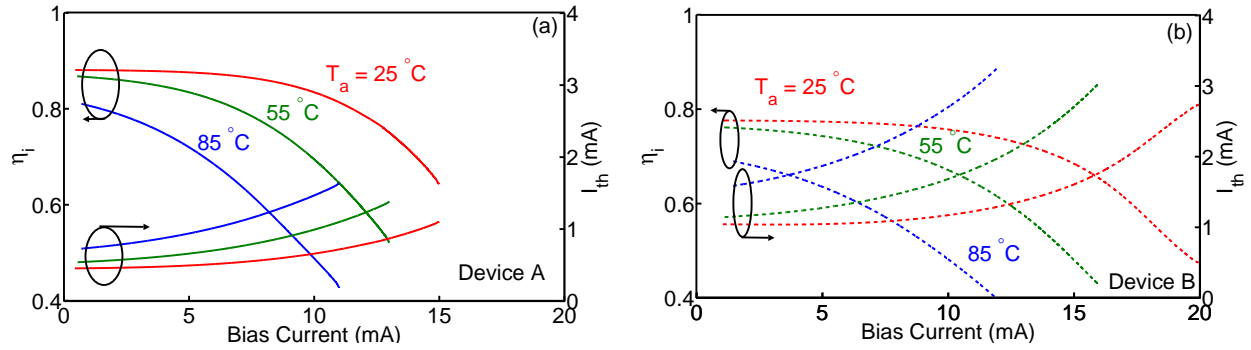
Figure 4. Changes in η_i (left scale) and I_{th} (right scale) with bias current at T_a = 25, 55, and 85 °C for the two devices under test. Part (a) corresponds to device A and part (b) corresponds to device B

low bias current for device B (about 78 %) is significantly lower than that of device A (86 %). This difference in internal quantum efficiency extends across a broad range of ambient temperature and bias currents. The physical reason behind this difference can be explained as follows: Ideally, a shallow surface etch should not drastically alter η_i. Indeed, the impact on η_i is insignificant for up to a 40-nm surface etch.[8] However, beyond 40 nm, increased cavity losses lead to an increase in the threshold carrier density, which in turn increases carrier leakage, causing a reduction in η_i. Further, it can be seen that for both the devices at any ambient temperature, there is a sharp decrease in the values of η_i at high bias currents. These high bias currents correspond to onset of thermal rollover in these devices. Therefore this rapid decrease in the value of η_i at high device temperatures is responsible for the onset of thermal rollover.

Similarly, looking at the threshold current evolution plotted on the right scale, it can be clearly seen that, at high I_b corresponding to a sharp decrease in the values of η_i, there is a corresponding increase in the values of threshold current. Since the emitted optical power is $\propto (I_b - I_{th}(T))$, an increase in the threshold current reinforces the sharp reduction in the value of η_i and hastens the output power saturation. However, the deleterious effect of threshold current can be independently mitigated by optimizing wavelength detuning between the gain peak and the cavity resonance at which the VCSEL operates.[23]
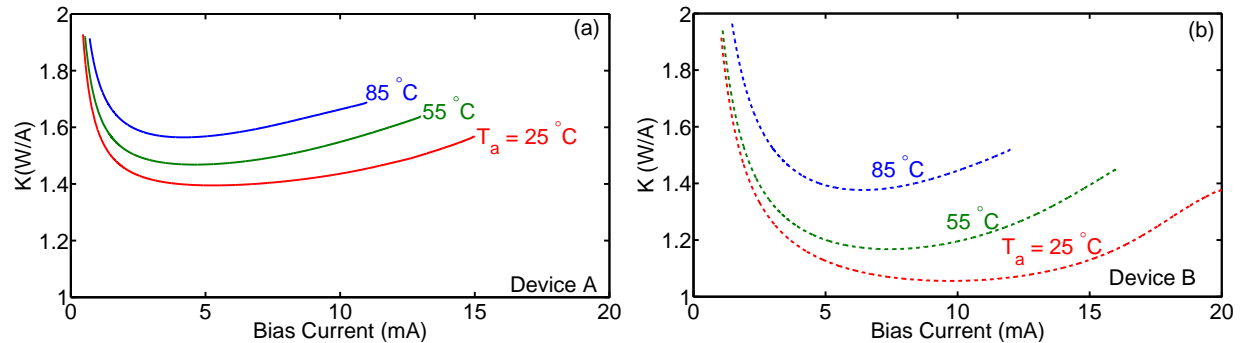

Figure 5. LPD coefficient K versus I_b at T_a = 25, 55, and 85 °C for the two devices under test. Part (a) corresponds to device A and part (b) corresponds to device B. An increase in K marks the onset of thermal rollover.

Figure 5 depicts how the LPD coefficient K [Eq. (4)] varies with I_b. Comparing the evolution of K for both the devices, it can be seen that close to I_{th}, the value of K is close to 2 W/A but it decreases quite rapidly as the drive current is increased. It takes a minimum value and begins to increase gradually on further increase in I_b. This peculiar evolution can be understood as follows:[17,22] Consider first heating due to the carrier recombination which is high below the lasing threshold. This is due to the fact that a significant percentage of the injected carriers recombine spontaneously to produce heat. It is reduced near and beyond the laser threshold because of the clamping of the carrier density. Further, the recombination heating coefficient scales with I_{th}/I_b[17].

Optical absorption (absorption of photons produced by stimulated emission in the VCSEL cavity) starts at the lasing threshold and its contribution increases with I_b due to an increase in the number of stimulated photons. The net effect of

carrier recombination and optical absorption is an initial reduction of K with increasing I_b around threshold. It is important to note that carrier thermalization and carrier leakage are low and nearly constant over these low bias currents and hence do not have a significant impact on the evolution of K.

With further increase in I_b, K in Fig. 5 for both the devices, takes its relatively low values for all ambient temperatures. For these I_b values, carrier thermalization and absorption heating are nearly constant while spontaneous recombination and carrier leakage are slowly decreasing and increasing, respectively. The net effect is a nearly constant K. With a further increase in bias current, increase in carrier leakage dominates, causing an increase of K and a corresponding super-linear increase of P_{LPD}. Further, absorption heating saturates at I_b corresponding to P_{max}, which is consistent with the saturation of the stimulated photon density in the laser cavity.

Contrasting the evolution of K for both the devices, it can be seen that at moderate bias currents corresponding to nearly constant K values, device B has significantly lower value of LPD coefficient K (nearly 40 % at 25 °C) as compared to device A. This reduction of K reduces the linear power dissipation [Eq. (3)] which in turn delays the onset of thermal roll-o;ver. A shallow surface-etch in the top-DBR therefore not only reduces the device photon lifetime but also reduces the value of K over typical operating currents which improves device static performance. The relative reduction in the value of K between the two devices is less prominent at high bias currents corresponding to thermal rollover. The same assertion is valid at high ambient temperatures ($T_a \geq 55$ °C) This can be attributed to increased carrier leakage in device B compared to device A. The physical origins of this increased carrier leakage and its impact on device performance will be discussed in the next section.

5. IMPACT OF PHOTON LIFETIME

The photon lifetime (τ_p) of a VCSEL is given by[8, 22]

$$\tau_p = \frac{1}{\alpha_i(T) + \alpha_m^T(T) + \alpha_m^B(T)}.$$ (9)

For device A (no surface etch), τ_p is 6.8 ps. This value reduces to near 1.4 ps for device B with the 55-nm surface etch. These values are calculated at 55 °C ambient temperature. It has been shown that a shorter photon lifetime improves the high-speed performance of 850-nm VCSELs.[8] Here, we look at the impact of photon lifetime on the various thermal rollover discussed in section 2.

In Fig. 6, we study the impact of photon lifetime on the LPD and QPD mechanisms by simultaneously comparing their evolution at three different ambient temperatures in the two devices under test. In parts (a,d) P_{LPD} and P_{QPD} as a function of I_b, in parts (b,e) individual LPD contributions versus I_b, and in parts (c,f) contributions of LPD and QPD mechanisms to ΔT for devices (A,B) respectively are plotted. The inset figures in parts (c-f) show the magnified version of the main figures at low bias currents for the sake of clarity. For both the devices, the solid, dashed and dotted lines correspond to 25, 55, and 85 °C ambient temperatures respectively.

Left and right columns in Fig. 6 (parts a,d) show the contributions of P_{LPD} and P_{QPD} to P_{tot} for devices A and B respectively. For both these devices, P_{LPD} exceeds P_{QPD}. This can be attributed to the fact that R_s and K in Eqs. (2) and (3) themselves depend on temperature, and therefore on I_b. Beyond a certain I_b, while K increases with I_b (Fig. 5), R_s decreases with I_b (Fig. 2d). Since similar evolution of K and R_s has been found for both the devices, it can be concluded that P_{LPD} is the dominant contributor to the self-heating effects for this class of devices. Devices A and B are electrically identical, and therefore the power dissipated across series resistance is identical for both these devices. Since P_{LPD} for device A is significantly higher than that for device B at any I_b, we can conclude that a higher P_{LPD} in device A is limiting its thermal performance. It is important to note that the comparative analysis of the thermal degradation mechanisms for the two devices is valid only upto 15 mA bias current which is the maximum bias current for device A. Lower linear power dissipation in device B means that it can be biased at currents in excess of 15 mA. At these bias currents, the power dissipation in device B will be higher than that in device A.

To understand the reason behind higher P_{LPD} for device A, we plot in Figs. 6 (b,e), the dependence of individual LPD contributions on I_b for devices (A,B) respectively at three ambient temperatures. It can immediately be seen that P_{abs} is much higher for device A as compared to device B at any ambient temperature. In fact, for device B, P_{abs} is almost negligible. This implies that a surface etch reduces the photon lifetime which not only reduces the damping[8, 18] but also significantly reduces absorption heating which delays the onset of carrier leakage, which in-turn improves the static
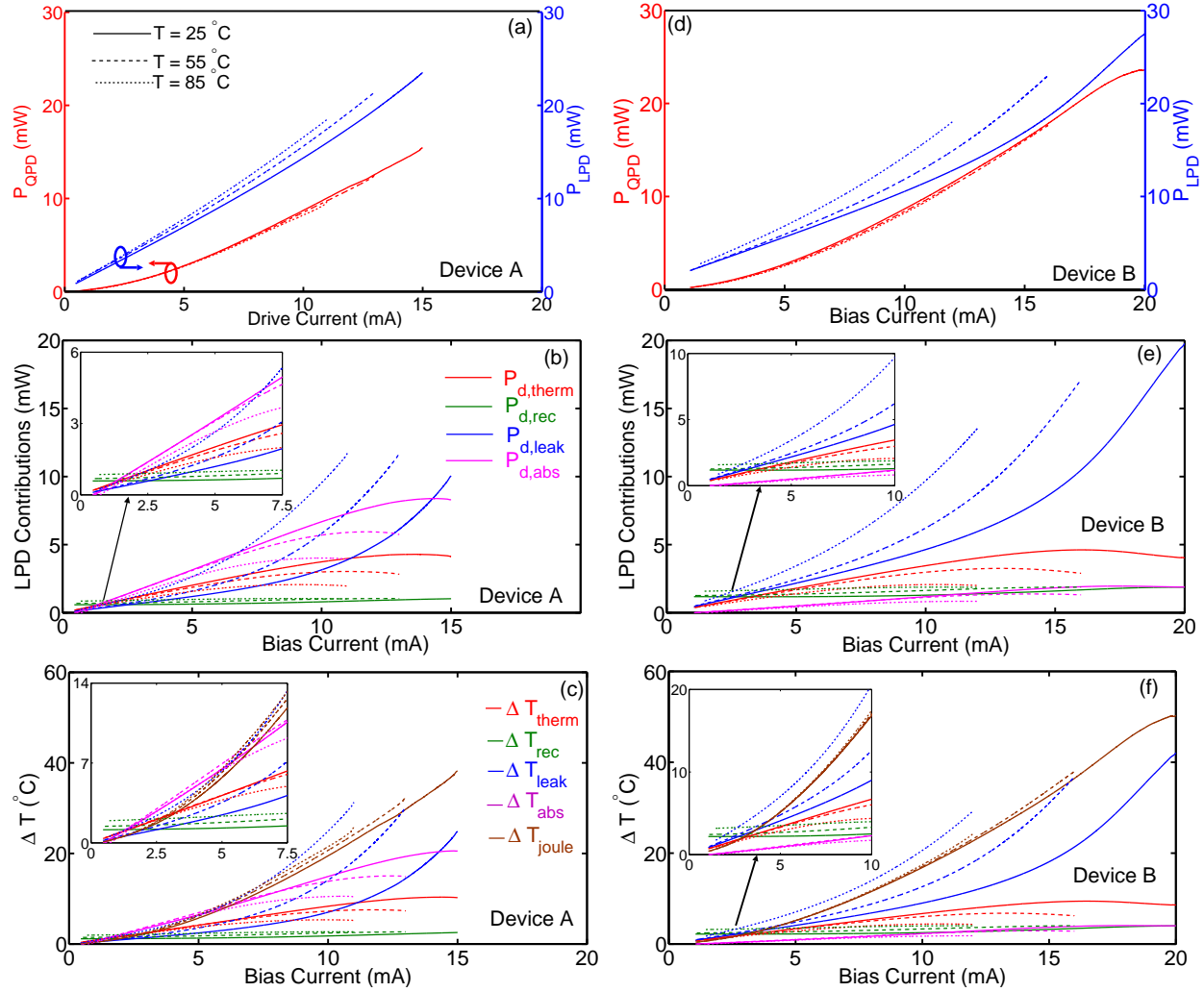
Figure 6. Impact of photon lifetime on the LPD and QPD mechanisms for the two devices under test at T_a = 25, 55, and 85 °C. Parts (a,d) P_{LPD} and P_{QPD} as a function of I_b, (b,e) individual LPD contributions versus I_b, and (c,f) contributions of LPD and QPD mechanisms to ΔT for devices (A,B) respectively. For both the devices, the solid, dashed and dotted lines correspond to 25, 55, and 85 °C ambient temperatures. For the sake of clarity, in the insets of parts (c-f), the magnified versions of the main figures at low bias currents are plotted.

performance of the device. However, it is important to note that at low bias currents, P_{leak} for device B is higher than that for device A. Therefore, a trade-off exists between absorption heating and carrier leakage in devices that control photon lifetime through a shallow surface etch in the top DBR.[22] This trade-off is different from that observed in conventional VCSELs involving absorption heating and Joule heating.[11,17] A general design guideline for this class of devices for optimizing high-speed performance is that photon lifetime should be optimized to the point where there is an insignificant increase in the threshold carrier density required for lasing. The residual carrier leakage can then be managed using other techniques such as reducing series resistance[10] and thermal impedance.[13] Indeed, devices with a 40-nm surface etch depth have been found to have superior high-speed performance.[8]

Figure 6 (c,f) shows the contribution of various power dissipation mechanisms to the total heat load for devices (A,B) respectively at three ambient temperatures. Again, the dominant contribution to increase in device temperature comes from Joule heating and carrier leakage. In device A absorption heating also contributes significantly to the total heat load. It can be seen that reduced contribution of absorption heating to the total heat load in device B implies that increase in device temperature (ΔT) in device B is less than the corresponding value in device A at any ambient temperature across a broad range of bias currents (upto 15 mA). This assertion drive home the point that reducing photon-lifetime through a shallow

surface etch in the top DBR reduces the device self-heating which in-turn has the desired effect of improving the device static performance. A careful optimization of the surface etch-depth has the additional benefit of improving the high-speed performance.

6. CONCLUSIONS

In this paper, we applied our simple empirical thermal model to study the impact of photon lifetime on the thermal performance of 850-nm VCSELs optimized for high-speed operation. We analyzed two VCSELs with different photon lifetimes (6.8 and 1.4 ps) corresponding to 0 and 55 nm surface etch in the top DBR in devices with 9-μm inner aperture diameter. Our empirical model requires temperature dependence of macroscopic VCSEL parameters such as threshold current, internal quantum efficiency, internal optical loss, series resistance and thermal impedance. Adopting a consistent procedure for both the devices, we deduce this temperature dependence through CW measurements of output power, voltage and emission wavelength as a function of bias current over an ambient temperature range of 15-100°C. It is important to note that the methods used in this work can potentially be applied to any VCSEL design. As a consequence, aside from some minor modifications in the relations for the barrier bandgap energy, lasing energy, and internal quantum efficiency, our empirical thermal model is generally applicable for a wide class of VCSELs across a broad range of ambient temperatures. We demonstrate that our thermal model can reproduce the measured VCSEL characteristics with reasonable accuracy ($< 10\%$ error), indicating that our model is consistent from the standpoint of optical, electrical, and thermal performance across a broad range of ambient temperatures. Such an agreement speaks of the underlying accuracy of the extracted temperature dependence of various VCSEL parameters. A careful analysis of changes in the threshold current and internal quantum efficiency shows that for both the devices, thermal rollover occurs because of a bias-current induced increase in the device temperature which increases the threshold current and causes a sharp reduction in the value of internal quantum efficiency.

The LPD coefficient K shows a similar behavior for both the devices across a broad range of ambient temperatures. Close to I_{th}, K is quite high because recombination heating dominates in this region. The rapid reduction of K with increasing I_{b} is due to a reduction in the recombination heating coefficient and a simultaneous increase in the absorption heating coefficient. These two effects reinforce each other. The LPD coefficient assumes a minimum value at a specific bias current and with further increase in bias current it increases gradually. This increase in the value of K is singularly dominated by carrier leakage as both absorption and carrier thermalization heating saturate and rollover at these bias currents. Contrasting the evolution of K for the two devices, it can be concluded that the onset of optical power saturation in this class of VCSELs can be delayed if the magnitude of K is reduced. For the devices analyzed in this work a reduction in K is brought about through reduction of the device photon-lifetime.

A comparative thermal analysis of devices A and B, which differ in their cavity photon lifetime, shows a trade-off between absorption heating and carrier leakage. Overcompensating for absorption heating can cause an increase in carrier leakage and vice versa. In these devices, absorption heating is reduced by a shallow surface etch in the top DBR. Beyond a certain etch-depth, cavity losses become so high that a very high carrier density is needed to achieve threshold gain which in-turn increases carrier leakage.

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