Thesis for The Degree of Licentiate of Engineering

GaN HEMT Low Noise Amplifiers for Radio Base Station Receivers

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Göteborg, Sweden 2012

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ISSN 1652-0769
Technical Report MC2-216

Printed by Chalmers Reproservice
Göteborg, Sweden, March, 2012

To My Family

Abstract

Gallium nitride (GaN) high electron mobility transistor (HEMT) has been introduced as the technology of choice for high power microwave applications due to its material properties including high saturation electron velocity and breakdown field together with excellent thermal conductivity and robustness. It is also a promising candidate for receiver front-ends in the radio base station (RBS) where low noise figure and high linearity are key issues for low noise amplifier (LNA) design.

The objective of this work has been to study the key properties of GaN HEMT LNAs in terms of linearity and noise performance, within frequency band of 1-3 GHz, for radio base station receiver front-end design. A well-designed GaN HEMT LNA technology would eventually challenge existing RBS commercial LNA platforms such as gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT).

In the first part characterization and design of a highly linear single-stage common-source GaN HEMT MMIC LNA with operational frequency of 3 GHz is presented. The main target was to investigate linearity and the trade-off between key parameters such as output third order intercept point (OIP3), noise figure (NF) and dc power consumption (P_{dc}). At 3 GHz the single-stage LNA showed a measured OIP3 of 39 dBm with $P_{dc} = 2.1$ W. The measured minimum NF was 1.5 dB which was around 1 dB higher than existing commercial GaAs pHEMTs.

The second part deals with two hybrid LNA solutions, two-stage common-source cascade LNA with operating frequencies of 1-3 GHz and single-stage cascode LNA designed for 1.5 GHz. Both hybrid designs were based on available commercial GaN HEMTs. The objective was to obtain low NF ($\leq$ 1 dB) and high OIP3 ($\geq$40 dBm) with a maximum dc power consumption of 2 W. The fabricated two-stage common-source LNA produced an OIP3 of 42 dBm with a NF equal to 0.5 dB. The dc power consumption was measured to be 1.2 W. With a OIP3/P_{dc} ratio of 13.2 the LNA may challenge present commercial GaAs pHEMT LNA solutions for RBS.

The single-stage cascode LNA exhibited minimum NF of 0.6 dB. Compared to two-stage common-source topology the single-stage cascode LNA introduced OIP3 = 35 dBm but at 50% less P_{dc}.

Keywords: radio base station receiver, high electron mobility transistor (HEMT), gallium nitride (GaN), low noise amplifier, cascode, cascade, high linearity, low noise, robustness.

List of Publications

Appended papers

This thesis is based on the following papers:

[A] P. Chehrenegar, O. Axelsson, J. Grahn, N. Rorsman, J.G. Felbinger, K. Andersson, "Design and Characterization of a Highly Linear 3 GHz HEMT Amplifier", in *IEEE Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), 2011*, pp.1-4, April 2011.

[B] P. Chehrenegar, M. Abbasi, J. Grahn, K. Andersson, "Highly Linear 1-3 GHz GaN HEMT Low-Noise Amplifier", to appear in *International Microwave Symposium*, 2012.

[C] P. Chehrenegar, M. Abbasi, J. Grahn, K. Andersson, "High Linearity GaN HEMT Low Noise Amplifiers with Low Power Consumption", *Manuscript*, 2012.

Contents

Chapter 1

Introduction

Multi-carrier receiver architecture, with wide IF-bandwidth of typically 20 MHz in combination with new standards imposes stronger requirements on the linearity of the front-end part of the receiver chain. The receiver will be more vulnerable to in/out-band spurious and interferers which affects receivers selectivity. At the same time the sensitivity of the receiver is another key parameter in determining the coverage of a wireless network. The noise performance of the first amplifier stage has a great influence on the receiver noise figure and thus its sensitivity performance. Another key design goal for the receiver front-end is robustness. As an example, in UMTS[1]-TDD[2] standard, the transmission and reception of data take place through a single antenna, utilizing a common carrier frequency. The input of the low noise amplifier (LNA) must be able to sustain high instantaneous power levels in case of antenna failure.

Commercial LNA based on GaAs pHEMT technology are today used for receiver front-end. However, to meet the challenge of high linearity, low noise, and robustness there appears to be a need for new semiconductor technology and new design techniques for LNA. Properties of AlGaN/GaN hetrostructure makes the GaN HEMT particularly suitable for high frequency and high power electronics [1]. In addition good noise properties have also been reported. The lowest noise figure was reported by K. W.Kobayashi et al. [2] to be 0.2 dB measured at -30°C within frequency range of 2-8 GHz. In Table 1.1 published works on GaN HEMT devices are listed. Compared to GaAs pHEMT, the wide bandgap corresponding to high breakdown voltage, high electron mobility, and good thermal conductivity of GaN, allow GaN HEMT to achieve comparable bandwidth, similar noise, but operate at higher voltages with significant improvements in terms of output power and linearity. A GaN HEMT LNA that offers high degree of robustness and sustains high level of input power without degradation would thus be very promising in RBS front-end design simply because it does not require input protection circuits. This will reduce the system complexity, and ultimately, the cost.

GaN HEMT is an attractive choice as a new technology source for building wide dynamic range microwave front-end components for RBS receivers. Apart from a number of studies performed on the GaN HEMT technology for trans-

[1] Universal Mobile Telecommunications System(UMTS)is a third generation mobile cellular technology for networks based on the GSM standard.

[2] UMTS-time-division duplexing (TDD) is a 3GPP standardized version of UMTS network.

Table 1.1: Published GaN HEMT based designs for LNA and power amplifier

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	BW[GHz]	Gain[dB]	Noise Figure [dB]	Linearity OIP3 [dBm]	Power Consumption [mW]
[3]	2-12	10	3.0	–	15
[4]	4-8	10.9	1.9	24	120
[5]	4-16	14.5	2.0	24	150
[6]	3-7	20	2.3	26	320
[7]	1.2-18	13.3	3.0	–	500
[8]	3-18	20	3	37.8	636
[9]	1-12	15	2.5	34.5	800
[10]	1-25	13	4.6	28.5	900
[11]	0.3-4	18	2	32	1000
[12]	3-16	20	4.0	–	2700
[13]	0.2-8	15	0.9	46.5	6000
[2]	2-8	13	0.35	43	6000
[14]	0.1-20	12.5	5.5	42.6	9000
[15]	1.7-2.3	15	2	49	16500
[16]	2.0	15	2.8	54	24192
[17]	0.5-3	15	2.0	43	–
$GaAs$ $AVAGO$[1]	0.9	17	0.4	35	280
	1.9	18	0.4	35	285
$GaAs$ $SKYWORKS$[2]	0.7-1	18	0.49	34	224
	1.7-2.0	17	0.61	34	224

[1] MGA-633P8 and MGA-634P8 from AVAGO technologies.
[2] SKY67101-396LF and SKY67100-396LF from SKYWORKS.

mitter design [3], relatively little is reported on design for the receiver. More specifically, for RBS receivers in telecommunication, it is yet not investigated in detail what GaN HEMT LNA may offer compared with existing GaAs pHEMT LNAs. At the bottom of Table 1.1 the typical electrical specifications of today's commercial solution based on GaAs pHEMT LNA are listed.

The objective of this work has been to study the key properties of GaN HEMT LNA in terms of linearity and noise performance for RBS receiver front-end designs. It is highly desirable to determine if GaN HEMT technology can act as a suitable replacement for existing commercial platforms such as GaAs pHEMT. For this matter different LNA technologies as well as topologies in GaN HEMT have been fabricated and studied in both monolithic and hybrid designs.

After a brief introduction, the design in a GaN HEMT MMIC process of a highly linear single-stage 3 GHz common-source LNA is presented in chapter 2. Chapter 3 deals with hybrid design of a two-stage common-source LNA and a single-stage cascode LNA. Both designs are based on commercial discrete GaN HEMT transistor and use surface-mount lumped components. Finally, the thesis is concluded in Chapter 4 including prospects for future work.

Chapter 2

Monolitic LNA Implementation

In this chapter the implementation of highly linear LNA based on GaN HEMT process is presented. The objective was to study the linearity of the LNA at lower frequencies, around 3 GHz, in the first place and noise in the second place. Furthermore the accuracy of the extracted model in predicting the performance of the LNA was also paid great attention. The ultimate goal was to implement a two-stage common-source LNA in a MMIC process where each stage was optimized independently with respect to noise and linearity.

2.1 GaN HEMT MMIC Process

The GaN HEMT MMIC process is based on a starting material of 25 nm $Al_{0.25}Ga_{0.75}N$ layer on top of a 2 μm undoped GaN buffer on semi-insulating SiC bulk. The process has primarily been optimized towards X-band transceiver designs and mainly for power applications [18]. The final GaN HEMT typically exhibits a power density of 5 W/mm at 10 GHz and 6 W/mm at 3 GHz. The process includes two metal layers with air bridges, thin film resistors and metal-insulator-metal capacitors. Typical parameters are listed in Table 2.1.

Table 2.1: GaN HEMT electrical parameters in the MMIC process [18]

Parameter	Value
Sheet carrier density	$10^{13} cm^{-2}$
Channel electron mobility	1200 cm^2/Vs
Gate length	0.2 μm
Gate width	4x75 μm
Source-drain spacing	3.0 μm
On-resistance	2.2 Ω mm
$I_{DSS}(V_{ds}$ = 5 V, V_{gs} = 0 V)	600-800 mA/mm
$V_{pinch-off}$	-4.0 V
Peak g_m(750-1000 mA/mm)	250 mS/mm
f_T/f_{max} (V_{ds} = 10 - 20 V, 2x75 μm)	23/52 GHz

2.2 Model Extraction

S-parameters of the device were measured in the range of 0.1-50 GHz for different bias conditions using 110 GHz power network analyzer (PNA) and an automatic probe station. The small-signal model of GaN HEMT transistor was extracted according to the method described in [19]- [20].

An ATN-NP5 noise parameter test setup was employed for measuring optimum source reflection coefficient (Γ_{opt}), minimum noise figure (F_{min}) and equivalent noise resistance (R_n) as a function of both frequency and bias. Based on the measured data the noise behavior of the device was modeled and realized with two shunt noise current sources between gate-source and drain-source according to the procedure described in [21]. The equivalent small signal model is shown in Fig. 2.1. The intrinsic parameters (bias dependent) have been placed inside the box. In paper A, the measured and modeled S-parameters are plotted.

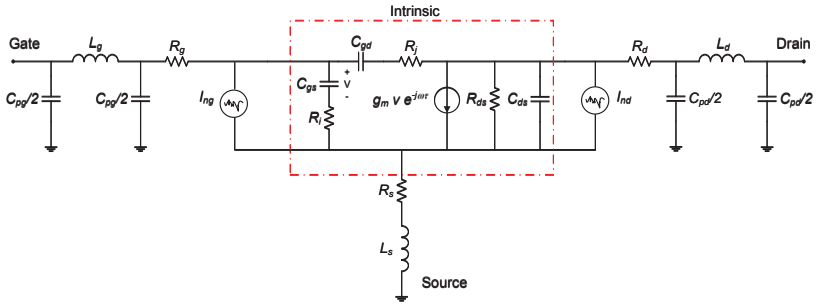


Fig. 2.1: The small signal equivalent circuit

For large signal modeling the charge based capacitance modeling method described in [22] was employed. Separate charge based expressions were derived to fit the bias dependent small-signal gate-source capacitance (C_{gs}), drain-source capacitance (C_{ds}), gate-drain capacitance (C_{gd}) and for charge conservation transcapacitance C_{dg}. The agreement between measurements and modeled in linear amplifier region (class A) was specifically addressed. The obtained capacitance models are shown in Fig. 2.2. For agreement between the large-signal model and the measured S-parameters; see paper A. Apart from S_{22}, the generated S-parameters by transistor model showed very good agreement with other S-parameters in frequency range of 0.1-50 GHz for V_{gs} = -1.6V and V_{ds} = 20V at which the transistor was intended to operate.

2.3 Circuit Design

Common-source configuration forms the core of most LNA topologies. In general the common-source stage with inductive degeneration has been widely used in LNA design due to its superior noise performance. In this thesis, two topologies, single-stage and two-stage common-source LNA, has been designed and fabricated.

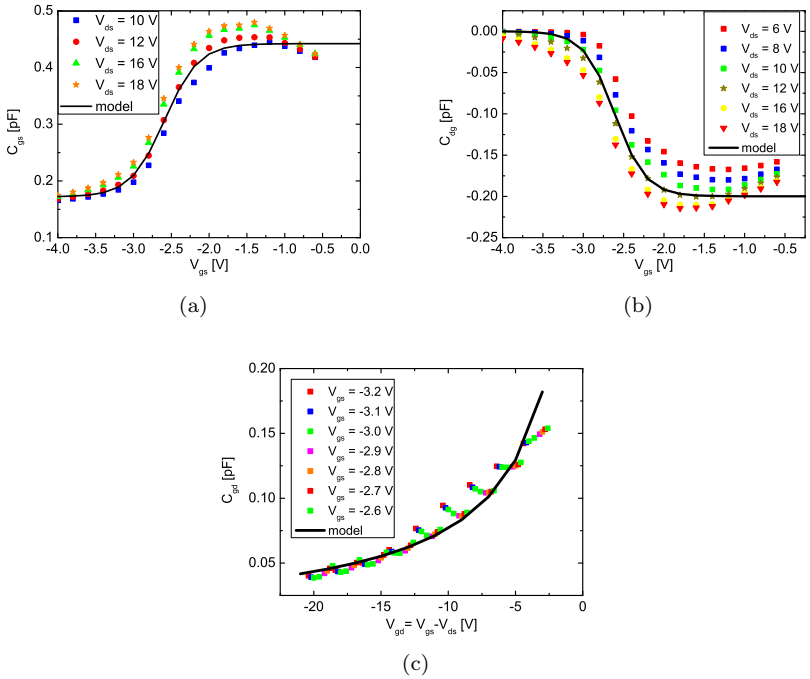


Fig. 2.2: Comparison between measured (symbols) and modeled (solid) capacitance values: (a) C_{gs} vs. V_{gs}, (b) C_{dg} vs. V_{gs}, (c) C_{gd} vs. V_{gd}.

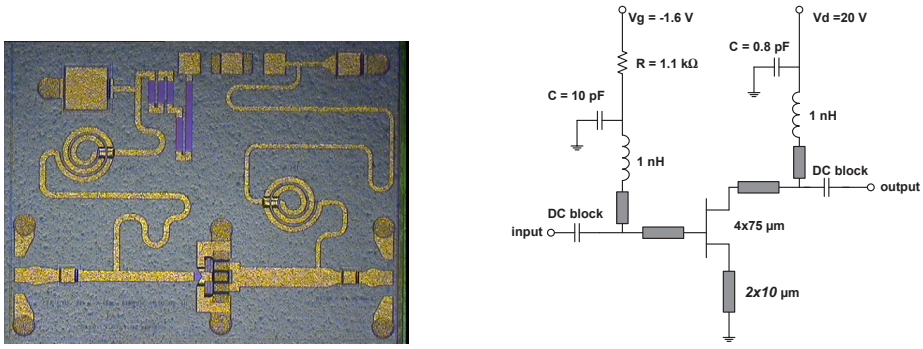
2.3.1 Single-stage common-source LNA

The single-stage common-source LNA was designed for maximum OIP3 while maintaining an input matching for reasonable noise performance and gain. A transistor with total gate width of 4x75 μm and nominal gate length of 0.2 μm built the core of the LNA. The die area was 1.82 x 1.37 mm^2. The trace length at the input was kept as short as possible to minimize its impact on noise performance. Two transmission lines, each with a length of 10 μm, connected the source to the ground. According to the simulations each transmission line gave an equivalent inductance of approximately 5 pH[1]. At 3 GHz the source resistor, R_s, provided resistive source degeneration for simultaneous low noise and impedance matching. A picture of the fabricated LNA and its corresponding circuit schematic is shown in Fig. 2.3.

2.3.2 Measurements

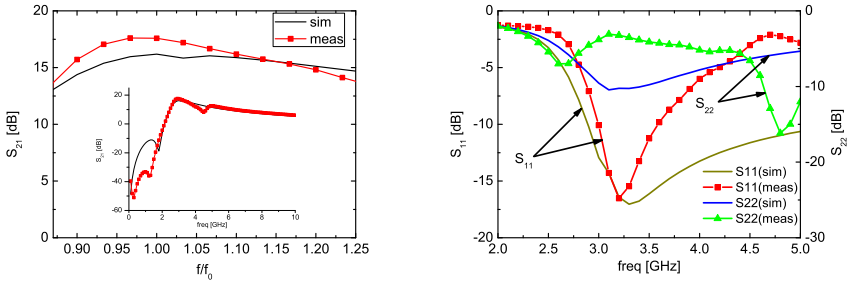
The measured S-parameters of the LNA are shown in Fig. 2.4. The measured 3 dB bandwidth was 2.7-3.6 GHz. At 3 GHz, S_{21} was equal to 18 dB while input return loss (S_{11}) and output return loss (S_{22}) were -15 dB and -3 dB, respectively. From simulation an S_{22} in the same order as S_{11} was expected. Further investigation revealed that a poor grounding of the shunt capacitor in

[1]The equivalent inductance of a via hole is about 35 pH.



(a) (b)

Fig. 2.3: 3 GHz GaN HEMT MMIC single-stage LNA, 1.82 x 1.37 mm^2: (a) micrograph of the finalized MMIC (b) Circuit schematic of the LNA.



(a) (b)

Fig. 2.4: Measured S-parameters vs. model: (a) S_{21}, (b) S_{11} and S_{22}. Inset in (a) shows S_{21} for frequency range of 0.1-10 GHz.

the drain bias network could be responsible for the degradation of S_{22}.

For OIP3 measurement, two tones with 1 MHz spacing at 3 GHz were applied at the LNA input. Each tone had a power of 0 dBm. Fig. 2.5(a) shows the obtained OIP3 with respect to I_{ds} and V_{ds}. The maximum measured value for OIP3 was about 39 dBm with I_{ds} = 105 mA and V_{ds} = 20V (V_{gs} = -1.6V) corresponding to a power consumption of 2.1 W. In the inset of fig. 2.5(a) both P_{out} and P_{IM3} are plotted to indicate the 3:1 slope relation between output power of the fundamental frequency and the third order intermodulation products. Further increasing of drain current (dc power) did not increase the OIP3 since the transistor had reached its compression point (Fig. 2.5(a)). In fact increasing the drain current would increase the noise figure (Fig. 2.5(b)). According to the simulation the device could produce higher OIP3 with its output matched to 50 Ω. Hence the degradation of S_{22} was obviously the reason higher OIP3 could not be obtained. Furthermore two-tone measurement was carried out with constant V_{gs} = -1.6V but variable V_{ds} and input power in range of -10 to 0 dBm/tone which with V_{ds} = 20 V gave an average OIP3 = 39 dBm(Fig. 2.5(c)). P_{1dB} was measured to be equal to 27 dBm using a single CW tone at 3 GHz (Fig. 2.5(d)).

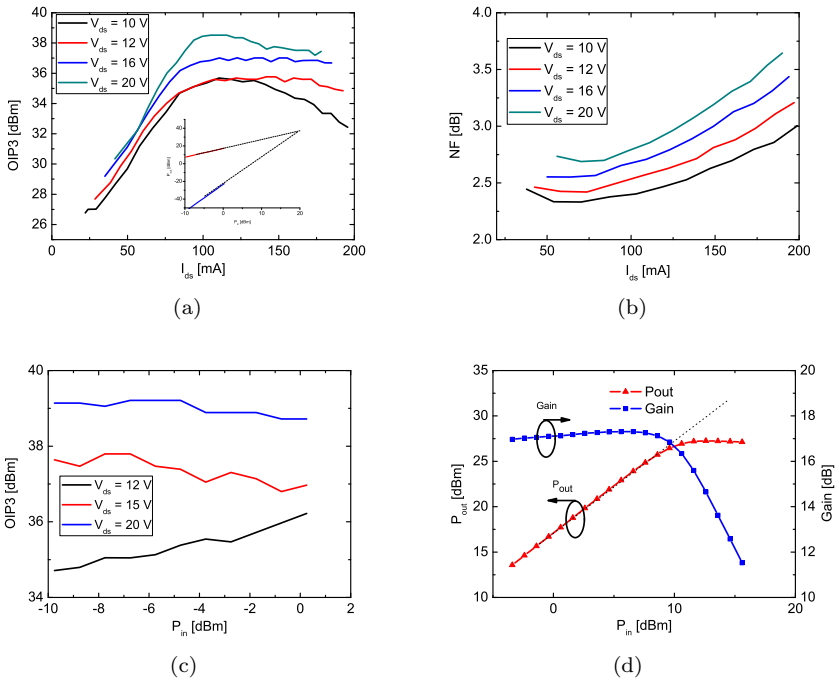


Fig. 2.5: Measured LNA characteristics of the single-stage common-source GaN HEMT MMIC LNA at 3 GHz: (a) OIP3 vs. I_{ds}, (b) NF vs. I_{ds}, (c) OIP3 vs. P_{in}, (d) P_{out} vs. P_{in}. Inset in (a) shows the 3:1 output power relation between fundamental and third order intermodulation frequency.

At 3 GHz, a NF of 2.9 dB was measured for I_{ds} = 105 mA and V_{ds} = 20V (V_{gs}= -1.6V). The minimum measured noise figure, NF_{min} of 1.5 dB occurred at 3.9 GHz. Figures 2.5(a) and 2.5(b) reveal clearly the trade-off between OIP3 and NF. With I_{ds} in the range of 100 mA to 130 mA (V_{gs} = -2V to -1.5V), a reduction of V_{ds} by 50% decreases the OIP3 by about 3 dB and NF by about 0.6 dB. See paper A for NF measurement within the frequency range of 2-5 GHz.

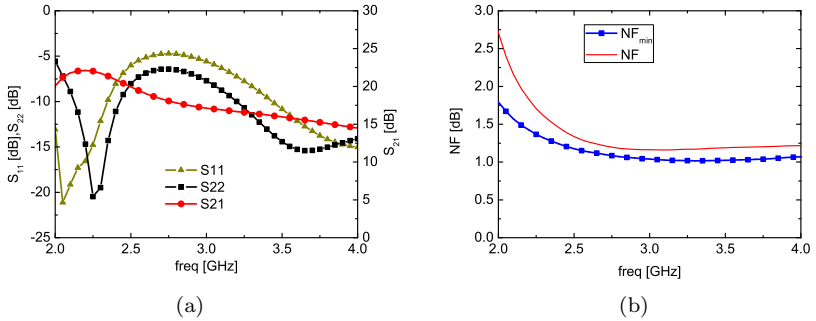
According to the measurement results in this study a single-stage GaN HEMT MMIC LNA was able to deliver high transducer gain (18 dB) and OIP3 (39 dBm). It also indicated that for proper noise match and linearity single-stage LNA design is not an optimum solution.

2.3.3 Two-stage common-source LNA

The previous single-stage common-source LNA showed the trade-off between the high linearity and low noise performance. In order to take one step further a two-stage common-source LNA is a promising solution for achieving both high linearity and low noise performance at the same time where each stage is independently optimized either with respect to noise or linearity.

A two-stage common-source LNA was designed, simulated and fabricated in the same GaN HEMT MMIC process as used for the single-stage common-source LNA. The targeted bandwidth was 3 GHz. The gate of the first stage was biased at approximately -3.5V close to pinch-off voltage (-4V) for minimal NF match while the second stage was biased close to class A (-3V). Consequently a NF of 1.2 dB could simulated for two-stage LNA with V_{ds} = 12V and total drain current of I_{ds} = 170 mA. The simulated NF was about 1.7 dB less than measured value for single-stage LNA. Obviously this was due to the fact that the first stage was indeed designed for optimum noise performance. According to the simulations the two-stage LNA gave a S_{21}=17.5 dB, S_{11}=- 6 dB and S_{22}=-8 dB. Two tones simulation gave an OIP3 of 41 dBm. See Fig. 2.6.

Unfortunately the fabricated LNA did not function properly. Since other amplifier circuits in the processed GaN HEMT MMIC batch were successful, this two-stage LNA may had some design flaw. An extensive investigation could not be pursued within the framework of this thesis thus it is still unclear if the circuit failure was related to design or process.



(a) (b)

Fig. 2.6: (a) Simulated S-parameters and (b) noise figure for two-stage common-source LNA.

2.4 Conclusion

A single-stage common source LNA had been designed on GaN HEMT for operational frequency of 3 GHz. The fabricated LNA exhibited high gain of 18 dB and OIP3 equal to 39 dBm, at a power consumption of 2.1 W. Compared to existing GaAs pHEMT technology the fabricated LNA exhibited higher OIP3 but at the cost of higher dc power consumption. A NF_{min} of 1.5 dB was measured. In other words, the single-stage fabricated GaN HEMT LNA exhibited a significantly higher NF_{min} than the existing GaAs pHEMT technology (= 0.4 dB). The single-stage solution is therefore not the optimum solution for achieving both high linearity and low noise performance without sacrificing gain. Consequently more complex topologies are required which offers more flexibility in terms of linearity and noise figure.

Chapter 3

Hybrid LNA Implementation

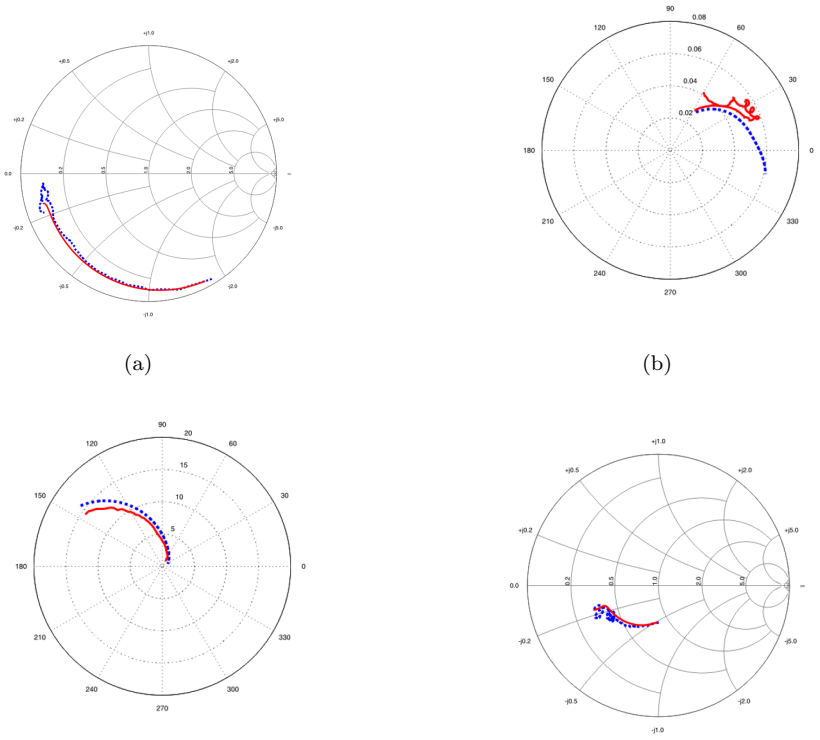
The flexibility that hybrid design offers is one of its major advantages over MMIC design. It has also considerably shorter design cycle. For these reasons the implementation of two LNA topologies with discrete transistors has been carried out. In general a single-stage common-source LNA can not provide sufficient high gain which is essential for overall noise performance. One solution is the use of multiple stages for achieving the required gain performance. Also the first stage is designed for noise while the second stage is optimized for gain. The draw back is increased power consumption, size, higher noise figure and cost. Two-stage LNA in cascade and cascode configuration had been selected for further investigation. The objective was to obtain high linearity and low noise simultaneously with reasonable power consumption in hybrid design. Both LNAs were fabricated using a commercial GaN HEMT.

3.1 GaN HEMT

Two commercial TriQuint TGF2023-01, 6 watt packaged power GaN HEMT transistors were at the core of both LNAs. This GaN HEMT is primarily intended for power amplifier applications. It is chosen because of its relatively high gain and small gate periphery compared to other devices available on the open market.

3.2 Model Extraction

The procedure described in chapter 2 had been followed for extraction of the equivalent transistor model. In order to place the reference plane of the measured data at the transistor, a dedicated calibration kit was designed and manufactured on the same substrate. The bias points were selected to cover both linear amplifier (class A) while keeping the dc power consumption below 2 W. The extracted value for drain-source resistor, R_{ds}, was 1.7 kΩ. Output return loss of the model was improved by setting R_{ds} equal to 5.5 kΩ.



(a) (b)

(c) (d)

Fig. 3.1: Measured S-parameters (dashed) vs. model (solid), 0.5-12 GHz, V_{gs}= -3.1V, V_{ds} = 10V: (a) S_{11}, (b) S_{12}, (c) S_{21}, (d) S_{22}.

Noise parameters of the device were also measured using an ATN-NP5 noise parameter test setup. The noise model was included in the small-signal model according to the procedure described in [21].

Figure 3.1 plots the agreement between the modeled and the measured S-parameters for V_{gs}= -3.1V and V_{ds} = 10V in the frequency range of 0.5-12 GHz. The accuracy of the model was evaluated by the normalized error between measured and modeled S-parameters according to Eq. (3.1) [23]. This is shown in Fig. 3.2 for -4.0 $\leqslant$ V_{gs} $\leqslant$ -2.1 V and 1 $\leqslant$ V_{ds} $\leqslant$ 32 V within frequency range of 0.5-12 GHz. It clearly shows a good agreement between modeled and measured S-parameters, particularly for -3.5 $\leqslant$ V_{gs} $\leqslant$ -2.5 V and 5 $\leqslant$ V_{ds} $\leqslant$ 15 V. For gate voltages close to pinch-off the error is significantly larger since the transistor is not able to produce enough gain. See also paper B for extraction of bias-dependent small-signal capacitances C_{gs}, C_{gd}, C_{ds} and C_{dg}.

$$\epsilon = \frac{1}{4N} \sum_{j=1}^{2} \sum_{i=1}^{2} \frac{1}{max \left| S_{ij}^{meas} \right|^2} \sum_{k=1}^{N} \left| S_{ij}^{meas}(k) - S_{ij}^{model}(k) \right|^2 \qquad (3.1)$$

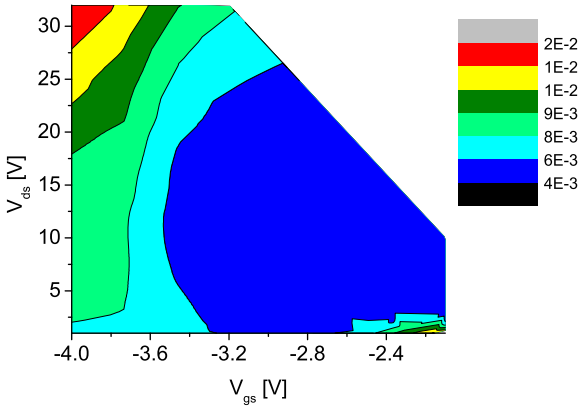
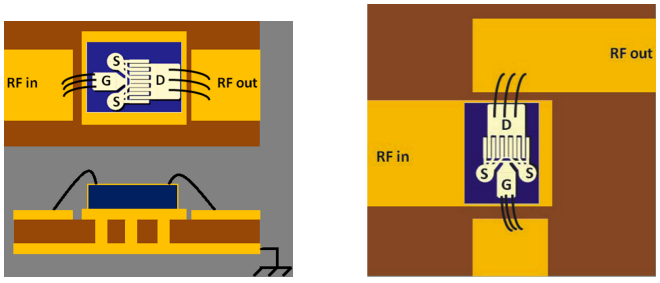


Fig. 3.2: Normalized error between measured and modeled S-parameters.



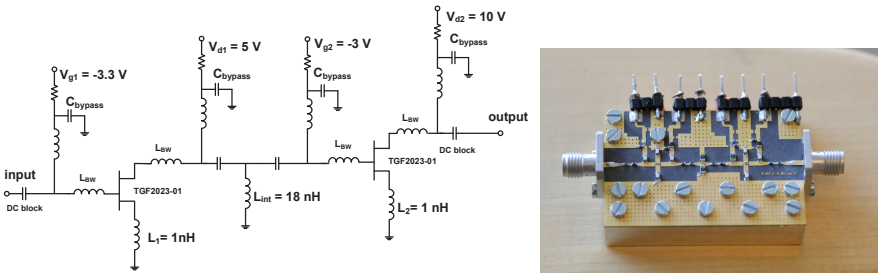
(a) (b)

Fig. 3.3: Mounting of the transistor: (a) grounded source (b) common-gate.

3.3 Circuit Design

Pad capacitances and lead inductances from the package may limit the ultimate performance that can be achieved by the help of the external circuitry. Using a transistor without any package (bare-die) where the transistor chip is wire-bonded directly to the printed boards (PCB) will help to reduce the extrinsic parasitic. The substrate is Rogers Duroid 5870 with 381 μm substrate thickness and 35 μm copper. The PCB lines are gold plated using 3-4 μm of soft gold to facilitate bonding directly to the transistor chip. The bond wires were of gold and had a diameter of 1 mil. At least three bond wires were used to connect the transistor to the PCB. The bond wires give approximately an equivalent inductance in range of 0.1-0.15 nH that was de-embedded during the model extraction of the transistor. See Fig. 3.3 which shows the mounting of the GaN HEMT in the hybrid designs.

The design used also surface-mount lumped components. Sources of the two transistors were mounted on PCB using silver epoxy while gates and drains were wire bonded to the transmission lines. Silicon-based heat sink compound



(a) (b)

Fig. 3.4: (a) Circuit schematic of the two-stage LNA, (b) Two-stage common-source LNA (46 x 30 mm^2).

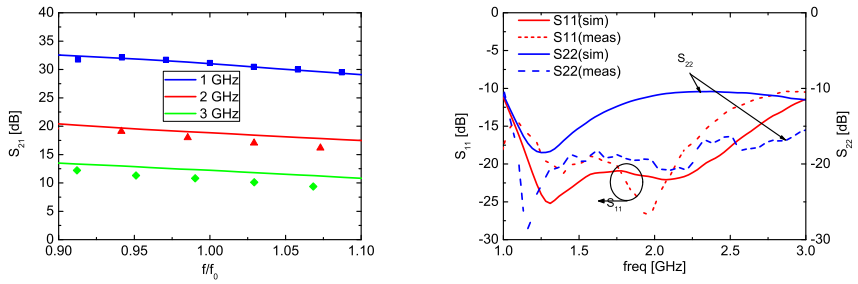
material was placed in between PCB and aluminium fixture and under each transistor for adequate heat transport. In order to move the reference plane of the measured data to the transistor, a dedicated calibration kit was designed and manufactured on the same substrate. An equivalent circuit model was however used for the inductors in which self-resonance behavior was included. Ideal component models were used for capacitors and resistors in the simulations.

3.3.1 Two-stage LNA

The circuit consisted of two common-source stages. Both stages had inductive source degradation for simultaneous low noise and impedance matching (L_1 and L_2 in Fig. 3.4(a)). In the schematic the L_{BW} represents the bondwire inductance. A picture of the fabricated LNA is shown in Fig. 3.4(b). The general design strategy was on optimizing the first stage for minimum NF and the second stage for maximum OIP3. As a first step the proper bias point had to be chosen to achieve a minimum NF while still maintaining high transducer gain. The gate and drain voltages of the first stage were selected V_{gs1} = -3.3V and V_{ds1} = 5V (I_{ds1} = 33 mA) to maintain low power consumption. With this bias point, a two-tone simulation was carried out using large signal model. It revealed that a load impedance of 50 Ω was appropriate, considering power consumption, to maximize the OIP3 of the single-stage design. The second stage was biased at higher drain voltage and current close to class A operation to maximize the linearity. The bias point for the second stage was selected to V_{gs2} = -3V and V_{ds2} = 8-10V (I_{ds2} = 97-110 mA). The inter-stage network, L_{int} and two DC block capacitors were designed to convert the input of the second stage to the required load impedance of the first stage. The amplifier was unconditionally stabilized (1-12 GHz) with 10 Ω series resistors on the drain lines.

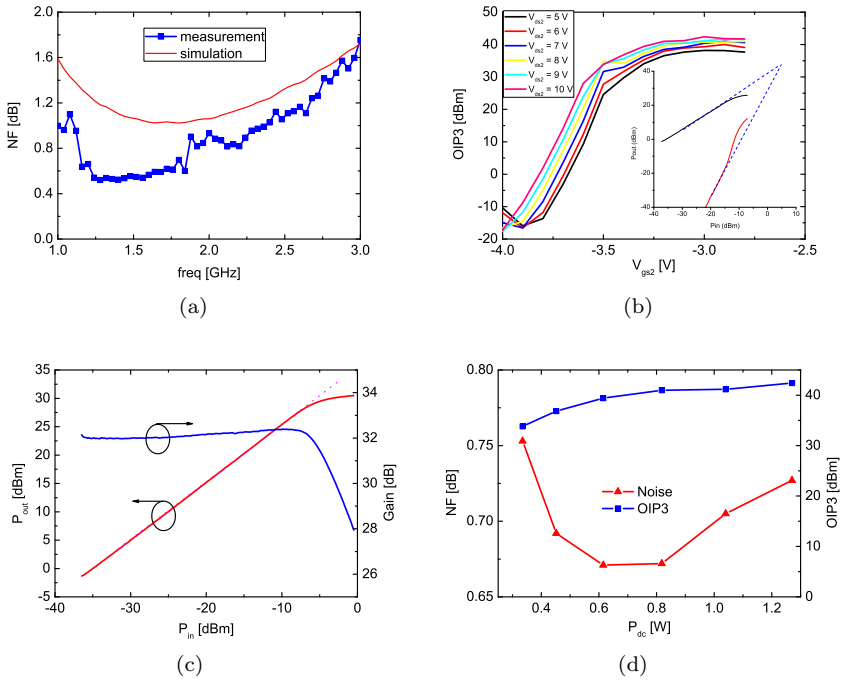
3.3.2 Measurements

The measured and simulated S-parameters of the LNA are shown in Fig. 3.5. The measured small-signal gain was 31 dB at 1 GHz, 18 dB at 2 GHz and 11 dB at 3 GHz. Figure 3.5(a) shows S_{21} with respect to 3dB bandwidth. Input and output reflection coefficients are less than -12 dB at all frequencies. A minimum



(a) (b)

Fig. 3.5: Simulated (solid) and measured (symbols, dashed) S-parameters for two-stage LNA, V_{gs1} = -3.3V, V_{ds1} = 5V, V_{gs2} = -3V, V_{ds2} =10V: (a) S_{21} vs. 3 dB bandwidth, (b) S_{11} and S_{22} vs. frequency.



(a) (b)

(c) (d)

Fig. 3.6: Measured two-stage LNA characteristics, V_{gs1} = -3.3V, V_{ds1} = 5V, V_{gs2} = -3V, V_{ds2} =10V: (a) NF vs. frequency, (b) OIP3 vs. V_{gs} and V_{ds}, (c) P_{out} and Gain vs. P_{in}, (d) NF and OIP3 vs. P_{dc}. Inset in (b) shows the 3:1 output power relation between fundamental and third order intermodulation frequency.

noise figure of 0.5 dB was measured within 1-3 GHz for V_{gs1} = -3.3V, V_{ds1} = 5V (I_{ds1} = 33 mA), V_{gs2} = -3V and V_{ds2} = 10V (I_{ds2} = 110 mA). Fig. 3.6(a) shows the simulated and measured NF of the amplifier. Noise model predicted higher NF than measured but most importantly the noise model was able to trace the

noise characteristics of the LNA. Large signal behavior of the LNA was measured for the same bias point chosen for minimum NF. As far as for the two-tone measurement, the input signals were combined by a resistive combiner. OIP3 was measured with a low input power of -20 dBm per tone but the power levels were swept to assure the 3:1 slope of the intermodulation products. Fig. 3.6(b) shows the measured OIP3 for various gate and drain voltages of second stage. The inset in Fig. 3.6(b) shows output power at fundamental and IM3 frequency vs. input power. The maximum OIP3 of 42 dBm was for V_{gs2} = -3V, V_{ds2} = 10V (I_{ds2} = 110 mA) with a total P_{dc} of 1.2 W. Further increase in the dc power could improve the linearity of the amplifier but at the expense of degradation in noise performance. Fig. 3.6(c) shows the measured P_{1dB} and gain for same bias at 1 GHz. The measured P_{1dB} was equal to 29 dBm. The trade-off between NF, OIP3 and power consumption is presented in Fig. 3.6(d). As indicated increasing the dc power consumption of the LNA beyond the measured bias points would improve OIP3 but at the cost of increased power consumption and degraded noise performance.

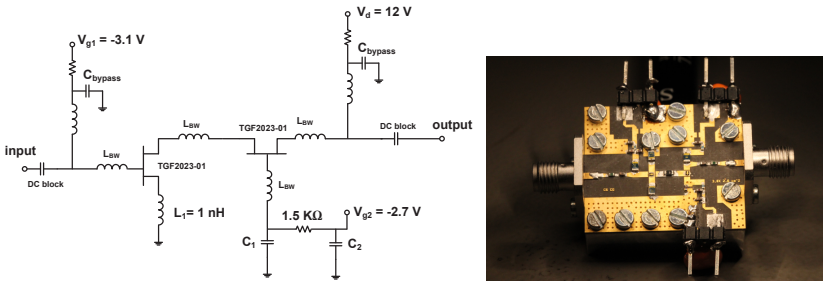
3.3.3 Single-stage cascode LNA

The cascode configuration shows some advantages against the single transistor case. The most noticeable is the suppression of the Miller effect caused by gate-to-drain capacitance of first stage. The Miller reduction improves signal gain and noise performance. In general cascode configuration offers better circuit stability and isolation between input and output. Drawbacks with respect to the simple common-source amplifier is slightly higher noise figure [24].

The circuit consisted of a single cascode stage. The common-source stage of the cascode was provided with inductive source degradation for simultaneous low-noise and impedance matching (L_1 in Fig. 3.7(a)). The source of the transistor is connected to the bottom of the chip by two via holes. As indicated in Fig. 3.3 the transistor was mounted directly on the transmission line. Due to layout consideration the second transistor was turned 90° with respect to the first transistor to give easier access to its gate-pads. From stability point of view proper ac ground was introduced to the gate of the second stage in form of two shunt capacitors, C_1 and C_2 in Fig. 3.7(a). In order to prevent oscillation at lower frequencies 15 μF capacitors were included in all three dc-feed paths. The gate voltages were selected to V_{gs1} = -3.1V and V_{gs2} = -2.7V with a common drain voltage of V_{ds} = 12V (I_{ds} = 21 mA) to obtain both minimum NF and maximum OIP3. The amplifier is unconditionally stabilized (1-12 GHz) with 10 Ω series resistor on the drain line and 1.5 kΩ at the gate. A picture of the fabricated LNA is shown in Fig. 3.7(b).

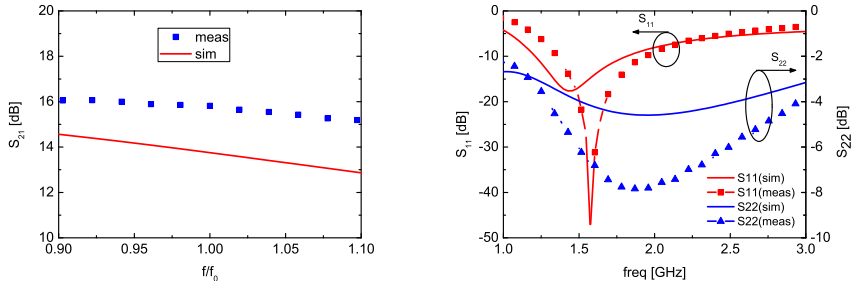
3.3.4 Measurements

Same measurement steps as for common-source LNA had been applied for measuring the common-source common-gate cascode LNA. The measured and simulated S-parameters of the LNA are shown in Fig. 3.8 for V_{gs1} = -3.1V, V_{gs2} = -2.7V, V_{ds} =12V. The measured small-signal gain is 16 dB at 1.5 GHz. Input and output return losses are less than -7 dB at all frequencies. A minimum NF of 0.65 dB was measured within 1-3 GHz for the same bias. Figure 3.9(a) shows the measured noise figure of the amplifier.



(a) (b)

Fig. 3.7: (a) Circuit schematic (b) Single-stage cascode LNA (30 x 26 mm^2).



(a) (b)

Fig. 3.8: Simulated (solid) and measured (symbols) for single-stage cascode LNA, V_{gs1} = -3.1V, V_{gs2} = -2.7V, V_{ds} =12V: (a) S_{21} vs. 3 dB BW, (b) S_{11} and S_{22} vs. frequency.

In Fig. 3.9(b) the measured OIP3 for various gate voltages of first stage and drain voltage is illustrated. The inset in Fig. 3.9(b) shows output power at fundamental and IM3 frequency vs. input power. The maximum OIP3 of 37 dBm for V_{gs1} = -3.1V, V_{gs2} = -2.7V, V_{ds} = 12V (I_{ds} = 21 mA) with a total dc power consumption of 250 mW was measured.

Interestingly further increase of the dc power consumption (up to 500 mW) did not significantly improve the linearity of the amplifier. See Fig .3.9(d). It is worth mentioning that for the two-stage common-source LNA the same amount of OIP3 obtained but with higher dc power consumption of 450 mW. Compared to GaAs pHEMT technology the cascode LNA produced higher OIP3 at lower dc power consumption. Finally in Fig. 3.9(b) the measured P_{1dB} and gain for same bias at 1.5 GHz is presented. The measured P_{1dB} is equal to 15 dBm.

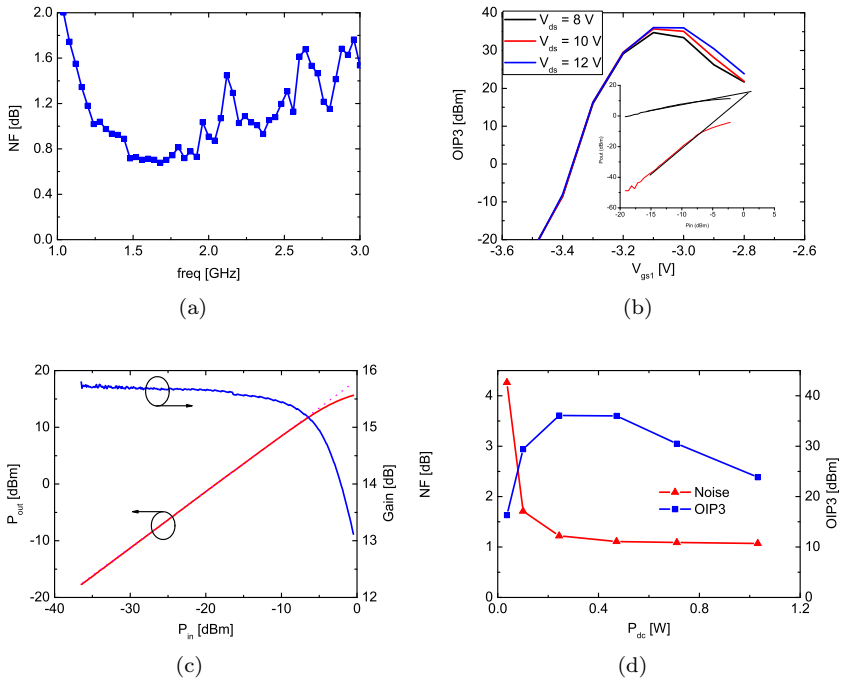


Fig. 3.9: Measured single-stage LNA characteristics, V_{gs1} = -3.1V, V_{gs2} = -2.7V, V_{ds} =12V:(a) NF vs. frequency, (b) OIP3 vs. V_{gs} and V_{ds}, (c) P_{out} and Gain vs. P_{in}, (d) NF and OIP3 vs. P_{dc}. Inset in (b) shows the 3:1 output power relation between fundamental and third order intermodulation frequency.

3.4 Conclusion

For two-stage common-source LNA a maximum small signal gain of 31 dB was measured with an OIP3 of 41±1 dBm at a power consumption of 1.2 W. The LNA exhibited low noise figure of 0.5 dB across the frequency band of interest. Considering the high linearity, low noise figure and the power consumption this amplifier showed state-of-the-art performance for GaN LNAs. Furthermore the linearity could be increased, at the cost of increased power consumption, with negligible degradation of noise performance. The GaN HEMT clearly justified its potential as a promising replacement for existing platform for RBS receiver front-end components.

The two-stage cascode LNA exhibited a maximum small signal gain of 15 dB with an OIP3 of 37 dBm at a power consumption of 0.25 W. It exhibited similar OIP3 as the cascade LNA but with 50% lower de power consumption. The cascode LNA gave a NF of 0.65 dB. This LNA could also out-perform commercial GaAs pHMET technology in terms of linearity and dc power consumption.

Chapter 4

Conclusions and Future Work

This thesis has demonstrated linearity and noise performance of GaN HEMT based LNA by studying three different LNAs topologies in both hybrid and MMIC technology.

Transistor modeling and design of single-stage common-source MMIC LNA was presented in the first part by which the trade-off between linearity and noise was discussed.

In the second part two discrete LNAs were fabricated using commercial transistors together with surface mounted lump components. A two-stage common-source cascade LNA showed outstanding state-of-art performance in terms of linearity and noise. The LNA produced an OIP3 of 42 dBm at a dc power level of 1.2 W and with 0.5 dB NF. Its performance was fully inline with commercial GaAs pHEMT LNA for RBS receiver. The LNA design also clearly showed the potential of GaN HEMT based components in robust and linear receiver front-ends. Furthermore a single-stage, cascode, LNA was fabricated. Compared to the common-source cascade GaN HEMT LNA and a commercial GaAs pHEMT LNA the same amount of OIP3 could be obtained by considerably lower level of dc power.

In Table 4.1, a comparison has been made between the results in this thesis and other published reports. The figure of merit has been defined as the ratio of $OIP3/P_{dc}$. It clearly shows the outstanding performance of the presented hybrid solutions. It justifies that GaN HEMT based LNAs are potential replacement for existing RBS receiver platforms such as GaAs pHEMT.

Further studies of GaN HEMT LNAs are required in order to be able to compete with mature RBS receiver technologies such as GaAs pHEMT components. Additional design designs are needed for 3GPP's (3rd generation partnership project) lower frequency bands, such as band 5 (850 MHz) and band 6 (800 MHz). In addition not only linearity and noise performance but also broadband topologies must be investigated. In order to take a step closer towards a commercial product the study of integrated solutions shall be put on the agenda. In this thesis mainly the circuit design (topology) has been focused on but as far as for the HEMT itself the effect of its electrical properties along with the process shall also be investigated for optimum linearity and noise. This calls for

Table 4.1: Comparison with Other Published Works

	Freq.[GHz]	NF[dB]	OIP3[dBm]	P_{dc}[W]	OIP3/P_{dc}
[16]	2-5	1.5	32	1.0	1.6
[5]	4-16	1.5	24	0.15	1.7
[2]	2-8	0.35	43	6.0	3.3
[9]	1-12	1.3	34.5	0.8	3.5
[15]	1.7-2.3	2	49	16.5	4.8
[13]	0.2-8	0.9	45	6.0	5.3
[16]	0.5-2.5	2	54	24	10
GaAs AVAGO MGA-633P8	0.9	0.4	35	0.28	11
GaAs AVAGO MGA-634P8	1.9	0.4	35	0.28	11
GaAs SKYWORKS SKY67101	0.7-1	0.49	34	0.22	11
GaAs SKYWORKS SKY67100	1.7-2.0	0.61	34	0.22	11
3 GHz MMIC LNA, Paper A	3	1.5	39	2.1	3.8
Two-stage LNA, Paper B	1-3	0.5	35	0.29	11
	1-3	0.5	42	1.2	13
Single-stage cascode LNA, Paper C	1.5	0.6	37	0.24	21

the need of noise-optimized GaN HEMT MMIC processes in the future.

Acknowledgment

I would like to express my gratitude to all who helped me during my work both at Chalmers University of Technology and Ericsson AB.

In particular I would like to express my deepest gratitude to Dr. Peter Olanders who supported me long before I started my work at Chalmers and pushing me forward with his enthusiasm. Time after time he has shown great concern about my work. I would also give my regards to my supervisors Prof. Jan Grahn and Dr. Kristoffer Andersson for their support, encouragement and guidance during this work.

I have had the opportunity of working together with a great team at Microwave Electronics Laboratory at MC2; My examinator Prof. Herbert Zirath, Dr. Christian Fager, Dr. Niklas Rorsman, Dr. Peter Linnér, Dr. Ilcho Angelov, Giuseppe Moschetti, Olle Axelsson, Mattias Thorsell, Paul Saad, Sona Carpenter are the name of a few among many others. Thank you all!

In addition I would like to thank my colleagues at Ericsson AB, among others, Göran Skoog, Magnus Molander, Zoran Drganic and Dr. Jurek Dabrowski.

I want also to express my appreciation to Dr. Morteza Abbasi for being a very good friend and source of encouragement. It was/is a great blessing to know him.

Beyond all, I am truly grateful to my family for their endless love and support.

*

This research has been carried out in GigaHertz Centre and Microwave Wide Bandgap Technology in joint projects financed by Swedish Governmental Agency of Innovation Systems (VINNOVA), Swedish Energy Agency (STEM), Chalmers University of Technology, SP Technical Research Institute of Sweden, Comheat Microwave, Saab AB, Ericsson AB, NXP Semiconductors, Infineon Technologies, Mitsubishi Electric, Furuno Electric Co., Norse Semiconductor Laboratories AB and Norstel AB.

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