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Ultra-Low Noise InP HEMTs for Cryogenic Amplification

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Abstract

InGaAs/InAlAs/InP High Electron Mobility Transistors (InP HEMTs), are today the best devices to design cryogenic low noise amplifiers. However, reported progress in reducing the noise has been slow in the last decade.

In this thesis the fabrication, optimization and characterization of 130 nm gate length InP HEMTs for cryogenic amplification at very low power dissipation is presented. By investigating device passivation, metallization, gate recess etch, and circuit integration, low-noise performance was optimized for the HEMT at low temperature around 10 K.

The effect of Al_2O_3 atomic layer deposition (ALD) for InP HEMTs was investigated. In comparison to standard plasma enhanced chemical vapor deposition passivated InP HEMTs, ALD passivated devices demonstrated much less kink effects associated with surface traps in the output drain current characteristics at room temperature.

An InP HEMT designed for ultra-low noise cryogenic amplification was fabricated. When 4x50 um devices were integrated in a 4-8 GHz 3-stage hybrid low noise amplifier (LNA), a noise temperature of 1.2 K was measured at 5.2 GHz and 10 K operating temperature. The gain of the amplifier was 44 dB across the band, consuming only 4.2 mW of DC power. The extracted minimum noise temperature of the InP HEMT was 1 K at 6 GHz. This noise temperature represents a new state-of-the-art for InP HEMT technology.

The relation between DC, S-parameter, and noise performance of the InP HEMTs has been investigated at room as well as at cryogenic temperatures. As the main noise contribution in the InP HEMT is observed to be linearly dependent on drain current I_d, excellent device performance at low I_d is a prerequisite for ultra-low noise operation. Transconductance g_m and cut-off frequency f_T of the InP HEMT at optimum low noise bias at 4 K was observed to increase with 100 % and 60 %, respectively, when cooled down from room temperature to 4 K.

To demonstrate the excellent low noise performance of the InP HEMT technology developed in this work, a 0.5-13 GHz cryogenic monolithic microwave integrated circuit (MMIC) LNA was designed and fabricated. At 15 K, the measured noise temperature within the entire band was below 7 K with a minimum of 3 K at 7 GHz. The gain was more than 38 dB and the power dissipation was 16.5 mW.

Keywords: ALD, cryogenic, InP HEMT, LNA, DC power dissipation, MMIC

List of appended papers

The thesis is based on the following papers:

[A] J. Schleeh, J. Halonen, B. Nilsson, P. Å. Nilsson, L.J. Zeng, P. Ramvall, N. Wadefalk, H. Zirath, E. Olsson and J. Grahn, "Passivation of InGaAs/InAlAs/InP HEMTs using Al_2O_3 atomic layer deposition", in *23rd IEEE International Conference on Indium Phosphide & Related Materials*, IPRM, pp. 63-66, May 2011.

[B] J. Schleeh, G. Alestig, J. Halonen, A. Malmros, B. Nilsson, P. Å. Nilsson, J. P. Starski, N. Wadefalk, H. Zirath, J. Grahn, "Ultra-low power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz", accepted for publication in *IEEE Electron Device Letters*, 2012.

[C] J. Schleeh, N. Wadefalk, P. Å. Nilsson, J. Grahn, "Characterization and Modeling of Cryogenic Ultra-Low Noise InP HEMT", Manuscript, 2012.

[D] J. Schleeh, N. Wadefalk, P. Å. Nilsson, J. P. Starski, G. Alestig, J. Halonen, B. Nilsson, A. Malmros, H. Zirath, J. Grahn, "Cryogenic 0.5-13 GHz Low Noise Amplifier with 3 K mid-band noise temperature", to be published in Proceedings of *IEEE MTT-S International Microwave Symposium*, 2012.

Contents

Chapter 1.

Introduction

Since almost two decades, the InGaAs/InAlAs/InP high electron mobility transistor (InP HEMT) has been the accepted technology for cryogenic ultra-low noise microwave amplification [1]. Record noise temperature of 1.4 K was demonstrated utilizing InP HEMTs in a 4-8 GHz low noise amplifier (LNA) around 10 K [2]. Also other competing technologies have been tested. The less expensive metamorphic InGaAs/InAlAs/GaAs HEMT has proven competitive with the InP HEMT with respect to cut-off frequency f_T and noise figure at room temperature. However, at cryogenic temperature operation, the noise is still considerable higher than the InP HEMT [3]. The more narrow bandgap InAs/AlSb HEMT, with potentially very good low noise properties at extremely low power dissipation, still suffers from high gate current and impact ionization degrading the noise performance also at cryogenic temperatures [4]. Also the SiGe heterojunction bipolar transistor (HBT) has been investigated for cryogenic low noise operation. It is suitable for applications requiring extremely stable transconductance, but with a higher noise temperature than the InP HEMT technology [5].

Reported progress in further reducing the noise figure of InP HEMTs has been absent in the last decade. There are relatively few actors in the device community able to fabricate InP HEMTs and circuits. Most focus has been made on gate scaling to realize THz InP HEMTs rather than minimizing noise to the lowest levels at cryogenic operation. InP HEMTs from the batch CRYO 3 utilized in [2] was processed at TRW/NGST more than ten years ago and has during the last decade served as a kind of standard component for ultimate cryogenic LNAs, in particular in the IF part of radio astronomy receivers. Since the CRYO3 process, no obvious progress in the field has been made because of challenges in optimizing epitaxial heterostructures, InP HEMT designs, and associated device parasitics. Also the measurement uncertainty makes evaluation of cryogenic ultra-low noise devices difficult.

In this thesis, a new state-of-the-art cryogenic ultra-low noise InP HEMTs is reported. By using an optimized epitaxial design and HEMT process, excellent device performance has been achieved for cryogenic amplification up to 10 GHz.

In Chapter 2, a description of the low-noise optimized InP HEMT technology is given. With a novel passivation method utilizing atomic layer deposition (ALD), surface traps

deteriorating device performance could be reduced. Access resistances have been minimized by developing very low resistive ohmic contacts. In Chapter 3, the optimized technology is demonstrated in a cryogenic hybrid LNA with a state of the art noise temperature. Finally, in chapter 4, a 0.5-13 GHz cryogenic monolithic microwave integrated circuit (MMIC) low noise amplifier (LNA) was designed and fabricated to demonstrate the excellent low noise performance of the InP HEMT technology.

Chapter 2.

InP HEMT Technology

The epitaxial structure nominally sets the performance of the technology with a certain electron mobility and sheet carrier concentration. The ohmic and gate contacts add parasitic resistance that needs to be minimized as far as possible. The gate recess in the InP HEMT process is crucial and easily results in defects and associated electrical traps deteriorating device performance. As a result, device passivation become essential in InP HEMT fabrication.

The InP HEMTs in this work were formed by mesa etching, ohmic contact formation, gate patterning using electron-beam lithography, followed by contact pad formation, device passivation, and air bridge formation. For more details on the device fabrication, see [6].

In this Chapter, investigations of crucial steps in the low-noise optimization of InP HEMTs, is presented. Three details in the InP HEMT have been subject to study: epitaxial structure and gate recess formation, device passivation and access resistances.

2.1 Epitaxial structure and gate recess formation

The purpose of the InP HEMT structure is to increase mobility without loss of sheet carrier concentration by separating the free electrons from their donor impurities. The epitaxial layers, grown from bottom to top on InP substrate, are buffer, channel, spacer (part of barrier), delta doping, barrier and cap. The purpose of the buffer is to overgrow dislocations and defects of the rough InP wafer and enable a crystalline base for the following epitaxial layers. The indium content of the channel should be maximized without introducing too much strain with risk for reduced mobility or even lattice dislocations. The spacer layer thickness must be carefully optimized to completely separate the delta doping from the 2-DEG without loss of sheet carrier concentration and formation of a parasitic channel. The thickness and composition of the barrier layer highly determines the gate Schottky diode, device transconductance, threshold voltage and access resistance between channel and cap layer. The cap layer should be designed with highest doping concentration for lowest possible access resistance.

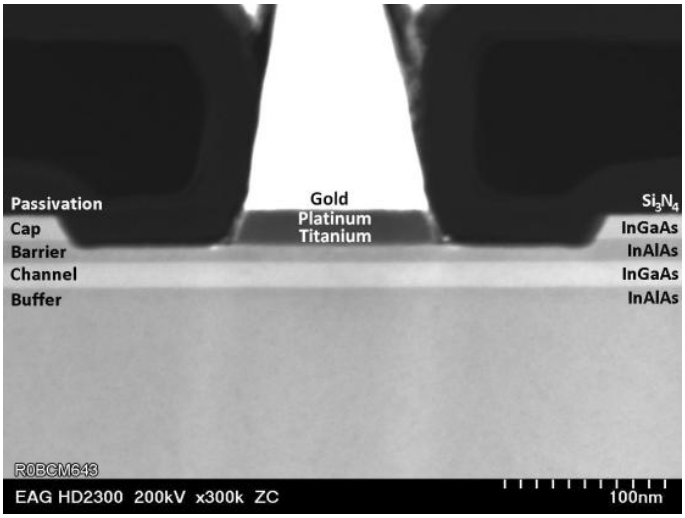

Fig. 2.1: Cross sectional STEM image of gate region in a 130 nm InP HEMT.

In general the channel is scaled toward higher indium content and reduced thickness when aiming for high frequency performance. In the same way a reduction of the barrier thickness improves high speed operation, but limits the breakdown voltage. Also the cap layer is limited in thickness as a too thick cap layer makes gate formation difficult.

The HEMT epitaxial structure used in this thesis, grown on 2" or 3" InP wafers by molecular beam epitaxy (MBE), consisted from top to bottom of 10-20 nm $In_{0.53}Ga_{0.47}As$ cap layer doped with Si to a concentration of $1x10^{19}$-$5x10^{19}$ cm^{-3}, 11 nm $In_{0.40}Al_{0.60}As$ or $In_{0.52}Al_{0.48}As$ Schottky barrier layer, $5x10^{12}$ cm^{-2} Si delta-doping layer, 3 nm $In_{0.40}Al_{0.60}As$ or $In_{0.52}Al_{0.48}As$ spacer, 15 nm $In_{0.65}Ga_{0.35}As$ channel and 500 nm $In_{0.52}Al_{0.48}As$ buffer. Hall measurements (with cap etched away) at room temperature typically demonstrated electron mobility and sheet carrier concentration of 12,000 cm^2/Vs and $2.8x10^{12}$ cm^{-2}, respectively. A STEM image of the cross section of the gate region, with marked epitaxial layers, is shown in Fig. 2.1. The micrograph confirms the thicknesses of the incoming layers of the InP heterostructure above.

Various gate recess etch procedures have been tested to minimize defects in the gate area and to have an optimum gate control over the channel. The optimization was carried out by studying drain current and dc transconductance behavior before and after device passivation. Compared to a typical CRYO3 cross-section [7], the gate recess in Fig. 2.1 is relatively flat and wide.

2.2 Device passivation

Passivation of surface-related defects during compound semiconductor processing is of large importance for the final electrical device characteristics. The standard passivation method for InP HEMTs is to deposit Si_3N_4 by plasma enhanced chemical vapor deposition (PECVD) [8, 9]. ALD is a relatively new method for compound semiconductor devices reported as gate dielectric [10]. With ALD, it would also be possible to passivate compound semiconductor surfaces in complex gate structures with superior thickness control [11]. Improved device performance has been reported for ALD Al_2O_3 passivation of AlGaN/GaN HEMTs and GaAs MESFETs [12, 13]. In this thesis ALD Al_2O_3 passivation of low-noise InP HEMTs is compared to standard PECVD Si_3N_4

passivation of InP HEMTs from the same wafer. The objective was to reduce the influence of surface charge deteriorating device performance. In this experiment the electrical measurements were only performed at room temperature conditions.

The gate length of the investigated InP HEMT was 130 nm and the gate width 2x50 µm using a source-drain distance of 2 µm. The gate area was wet-etched with a succinic-acid based solution prior to the gate metal deposition. As evidenced from transmission electron microscopy (TEM) of device cross-sections, see Fig. 2.2, a 50 nm wide recess region was formed in the cap layer adjacent to the gate. A large gate recess area helps to reduce the parasitic gate-to-drain and gate-to-source capacitance (C_{gd} and C_{gs}) but also creates surface defects which may degrade HEMT performance. Device passivation was performed either with the standard Si_3N_4 PECVD deposited at 300ºC or Al_2O_3 ALD at 250ºC with trimethylaluminium (TMA) as Al precursor and H_2O as oxygen precursor.

As seen in Fig. 2.2a, the thickness of the PECVD deposited Si_3N_4 layer was around 80 nm. The ALD passivation was performed in 300 cycles during one hour resulting in a total Al_2O_3 thickness of 33 nm, see Fig. 2.2b.

DC measurements were performed both before and after the device passivation. Small-signal microwave measurements were performed after device passivation. The microstructure of the HEMT structures were analysed by transmission electron microscopy (TEM) using a FEI Tecnai G2 S-TWIN with a LaB6 filament operated at 200 kV. Both high resolution TEM imaging and scanning TEM (STEM) with bright field and high angle annular dark field (HAADF) imaging modes were used.

I-V device characteristics before and after passivation are shown in Fig. 2.3. The unpassivated InP HEMT typically exhibited a maximum drain current density of 340 mA/mm. The gate current was around 1 µA/mm with a dip to 4 µA/mm under impact ionization, which appears for drain-to-source voltage (V_{ds}) above 0.8 V. All unpassivated devices showed the same kink phenomena in accordance with [14]. For this low bias region, this is considered to be a consequence of surface traps in the sensitive recess area adjacent to the gate, and not impact ionization. As seen in Fig. 2.4, the extrinsic transfer characteristics also suffered from this kink phenomena; the threshold voltage was ill-defined and a kink in the drain current (I_d) vs. gate-to-source voltage (V_g) characteristics was clearly present. The maximum extrinsic transconductance before passivation was measured to 0.6 S/mm at a V_{ds} of 1 V.

Irrespective of passivation method, an increase in maximum drain current density with about 20% was observed; see Fig. 2.3. The change in gate current was negligible for both passivation methods. A significant difference between PECVD and ALD passivated HEMTs was observed in the reduction of the kink in the I-V characteristics; As seen in Fig. 2.3, the kink was fully suppressed for the ALD passivated devices whereas only a minor improvement could be seen for the PECVD devices indicating that the ALD is superior to PECVD in passivation of surface traps in the InP HEMTs. One explanation for the superior ALD passivation is the dramatic reduction of Ga^{3+} and As^{3+} oxidation states after the first TMA half cycle of ALD as previously reported in Ref. [15] for $In_{0.2}Ga_{0.8}As$. Similar mechanisms may also be valid for the passivation of the $In_{0.4}Al_{0.6}As$ barrier for the InP HEMTs in this study.

Another explanation of the difference in passivation method seen in Fig. 2.2 was the superior film coverage of the ALD compared to the PECVD. This is clearly visible when comparing the TEM images of the ALD passivation shown in Fig. 2.2b with the PECVD passivation, in Fig. 2.2a. The thickness of the ALD passivation was uniform over the whole gate region whereas the thickness of the PECVD passivation varied and decreased

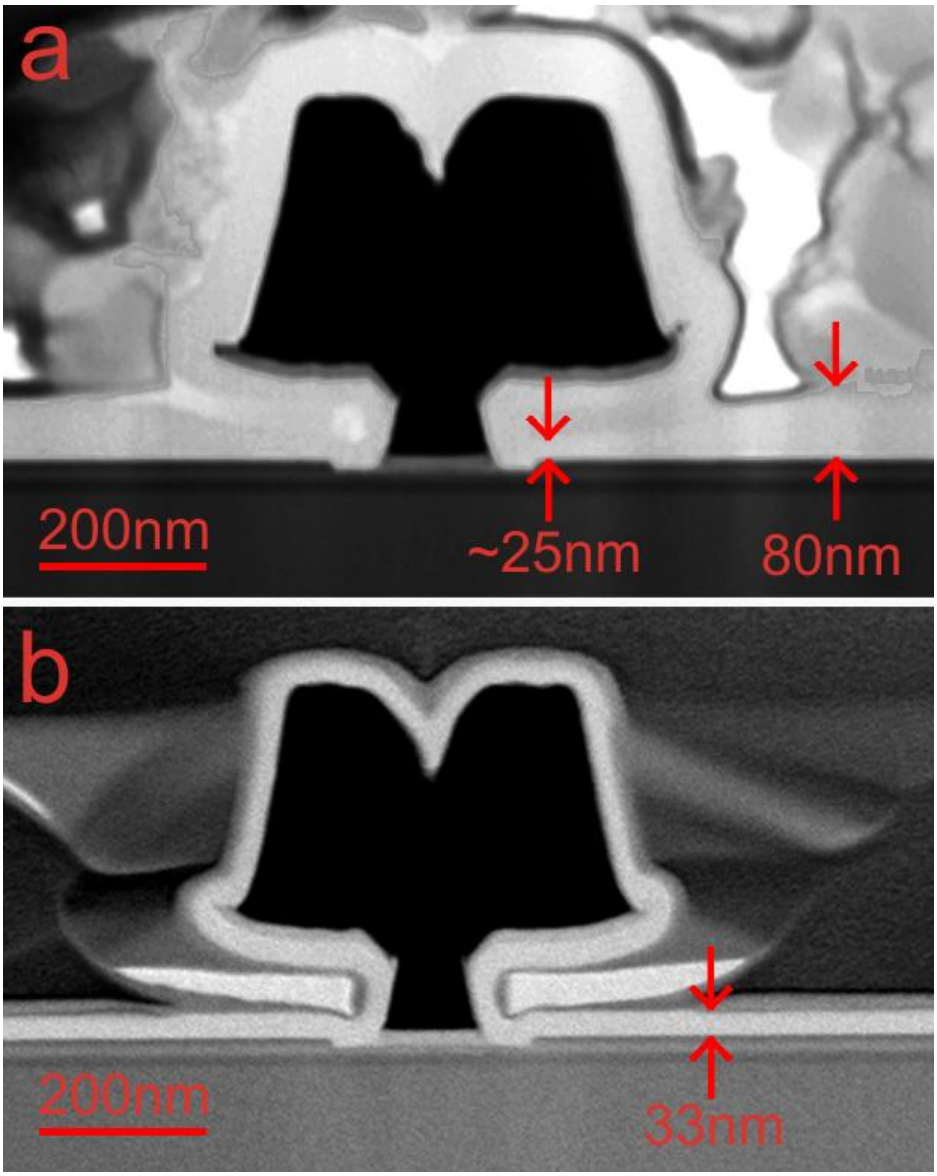

Fig. 2.2: TEM image of the gate region of a) Si_3N_4 PECVD and b) Al_2O_3 ALD passivated InP HEMT. The thickness of the passivation is marked in the figures.

under the gate hat, leaving the most important area less passivated. The thickness of the ALD passivation can probably be reduced further without loss in coverage, while a very thick PECVD passivation is needed to assure full coverage.

A further observation is the difference in atomic structure between the Al_2O_3 ALD and Si_3N_4 PECVD passivation layers. As evident from high resolution TEM images (not shown here), the PECVD passivation was fully amorphous, whereas the ALD passivation showed an atomic layered structure along the film growth direction. A high resolution TEM image of an ALD passivated device is shown in Fig. 2.5.

A reduction of the output conductance was evident after both passivation methods. As seen in Fig. 2.4, the I_{ds} vs. V_{gs} curves were smoother after both passivation methods and a well-defined threshold voltage of -0.25 V was extracted. Kinks in the extrinsic transfer characteristics were removed both with ALD and PECVD passivation. An increase in

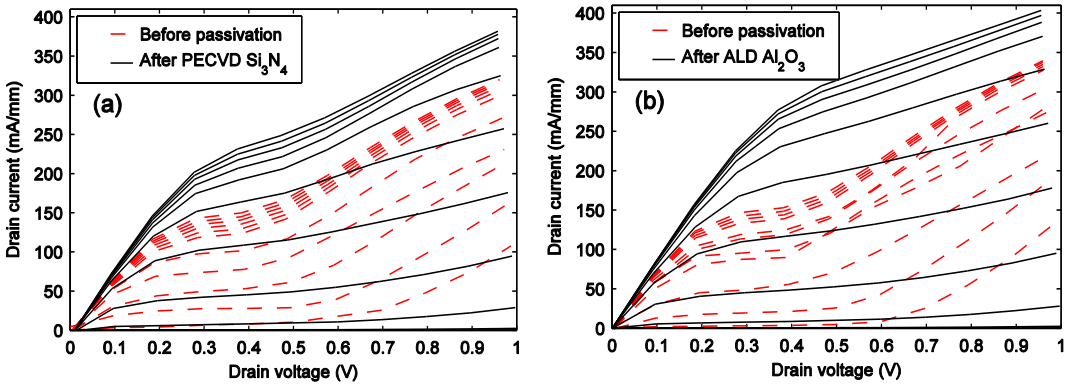

Fig. 2.3: I-V characteristics of 2x50 µm InP HEMTs before and after passivation with (a) PECVD Si3N4 and (b) ALD Al2O3. Gate voltage was swept in steps of 0.1 V from -0.4 V (lower curve) to 0.6 V (upper curve).

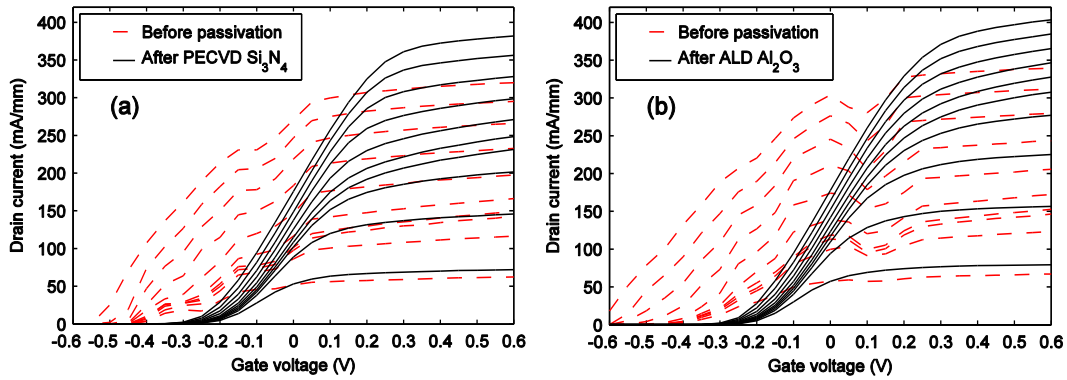

Fig. 2.4: Extrinsic transfer characteristics of 2x50 µm InP HEMTs before and after passivation with (a) PECVD Si3N4 and (b) ALD Al2O3. Drain voltage was swept in steps of 0.1 V from 0.1 V (lower curve) to 1 V (upper curve).

maximum extrinsic transconductance of about 30% was observed regardless of passivation method.

RF measurements showed extrapolated f_t and maximum oscillation frequency f_{max} of 220 GHz and 170 GHz, respectively, after both passivation methods. No obvious difference in C_{gd} (160 fF/mm) and C_{gs} (800 fF/mm) between ALD and PECVD passivated HEMTs was seen. This is explained by the higher relative permittivity of the thin ALD Al_2O_3 ($\varepsilon_r = 9.8$) passivation compared to the thicker PECVD Si_3N_4 ($\varepsilon_r = 7$), resulting in similar effective permittivity. A further reduction of the ALD Al_2O_3 thickness is expected to reduce the parasitic capacitances and enhance the device RF performance.

2.3 Parasitic access resistances

Access resistances are key parameters in the optimization of low noise HEMTs [16]. Indeed, one reason for superior performance at cryogenic temperatures is the reduction of parasitic resistances with temperature. As the electron-phonon scattering decreases with temperature, the semiconductor and metal sheet resistances decrease. However, as the

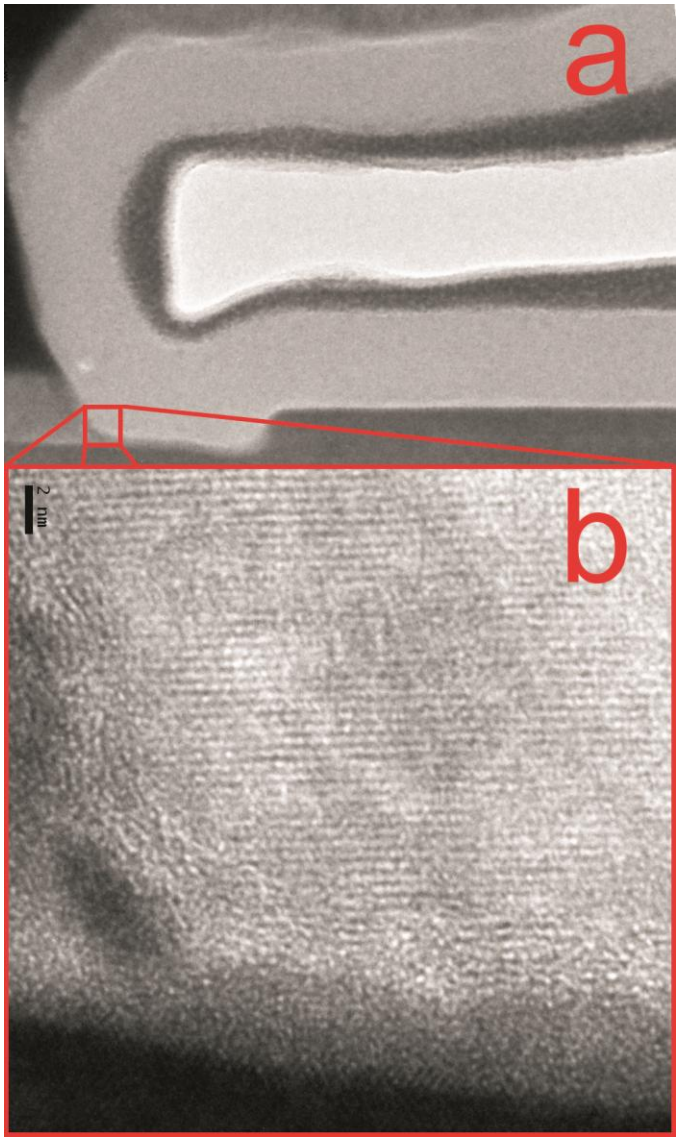

Fig. 2.5: a) TEM image of ALD passivated gate region. b) High resolution TEM image showing atomic layered structure along the film growth direction. The black bar is 2 nm long.

ohmic contact resistance R_c will likely increase with lower temperature, the total access resistance might actually increase when cooled down.

To optimize R_c and the epitaxial sheet resistances R_{sh} for the InP HEMTs the thickness and Si doping of the cap layer was increased from 10 nm and $1x10^{19}$ cm^{-3} to 20 nm and $5x10^{19}$ cm^{-3}, respectively. With a metal stack consisting of Ni/Ge/Au and an annealing temperature of 280 °C, R_c of 0.03 Ω·mm at 300 K was obtained. But most importantly as seen in Fig. 2.6, when cooled down to 4 K, R_c only increased incrementally to 0.04 Ω·mm.

The gate resistance R_g, optimized using a 130 nm T-gate technology, decreased from 320 Ω/mm at 300 K to 120 Ω/mm at 4 K. Also R_{sh} was improved from 60 Ω/□ at 300 K to 20 Ω/□ at 4 K. Notable is that R_{sh} and R_g decrease close to linearly between 300 K and 50 K, and then start to saturate. This means that at temperatures below 50 K the main limitation for the carrier mobility is not phonon scattering, but rather material impurities.

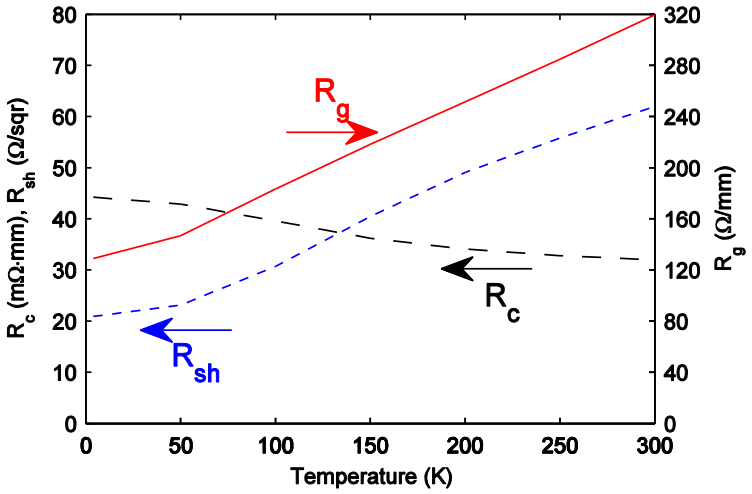

Fig. 2.6: Temperature dependence of R_g, R_{sh} and R_c.

It is observed that R_c and R_{sh} obtained in this work are 40-60 % and 50-70%, respectively, better than an optimized 100 nm gate length GaAs MHEMT technology with a very similar temperature dependence [3]. R_g is observed to be similar to [3].

The resulting source and drain resistance R_s and R_d, used in small signal modeling, was 0.13 Ω·mm and 0.14 Ω·mm at 4K, and 0.24 Ω·mm and 0.26 Ω·mm at 300 K, respectively.

Chapter 3.

InP HEMT Characterization

To optimize InP HEMTs for low noise under cryogenic conditions around 10 K is a complex task. There are several noise sources in the InP HEMT with strong dependence on both bias and temperature. As different noise sources have different optimum conditions, but only one bias and temperature of operation can be used at a time, a tradeoff is inevitable for low-noise operation. Furthermore, it is generally known that a device with excellent low-noise figure at room temperature does not automatically mean an excellent noise temperature at cryogenic temperature [16]. In addition, accurate noise measurements at cryogenic temperatures are very challenging.

This Chapter starts with a brief background to the noise contributions in InP HEMTs. The DC, microwave and noise characterization will be given for the noise-optimized HEMT described in Chapter 2. Finally, the demonstration of a state of the art InP HEMT in a hybrid 4-8 GHz cryogenic LNA is presented.

3.1 Background to noise sources in the InP HEMT

The most important physical noise sources in semiconductor devices are thermal, generation-recombination, shot, and hot-electron noise [17]. In InP HEMTs the thermal noise has its origin in the parasitic gate, source and drain resistances. As it is directly proportional to the magnitude of these resistances, optimized access resistances has been a key to low noise InP HEMTs. However, the thermal noise is also directly proportional to temperature, making its contribution at cryogenic temperatures less significant.

The generation-recombination noise in InP HEMTs is mainly generated by traps causing fluctuations of the number of free electrons and resulting conductance. Its noise contribution is minimized with an optimized epitaxial growth introducing as few traps as possible.

Shot noise is generated by gate current over the Schottky barrier. This noise source is not as straight forward to minimize. In general the thickness of the barrier layer separating the gate from the channel should be as big as possible to obtain low leakage current.

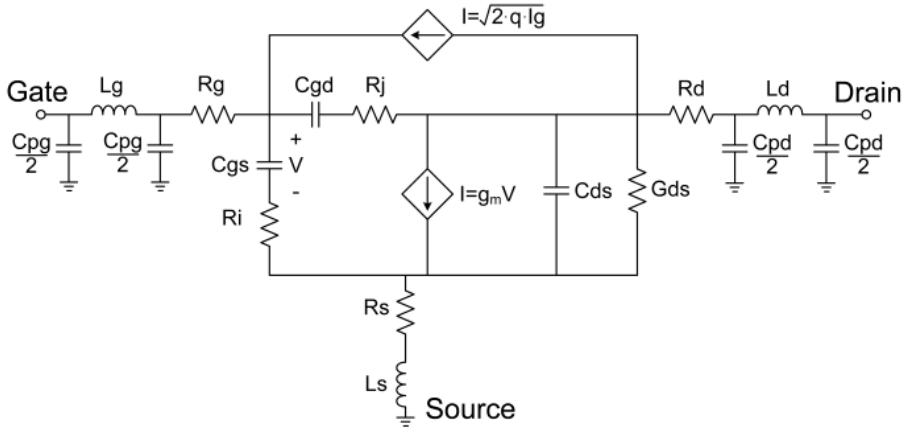

Fig. 3.1: Equivalent circuit of InP HEMT.

But the barrier thickness also strongly determines the transconductance g_m [18] which, in turn, is very important for the microwave noise.

Finally, hot-electron noise is generated by the high electric field in the channel and is the most difficult noise source to minimize. This is because a high electric field is a fundamental condition for the InP HEMT to operate at high speed. Energy relaxation, intervalley transfer, real-space-transfer and impact ionization are all examples of ultrafast kinetic processes associated with hot-electron noise [17].

To predict the noise behavior of InP HEMTs in relation to frequency, bias and ambient temperature, noise models based on small signal parameters are widely used [16, 19, 20]. In Fig. 3.1 the small signal model used for the InP HEMTs in this work is shown. For this model, omitting the gate current, an expression for the minimum noise temperature T_{min} was suggested by Pospieszalski [20]. If all resistive elements in the small signal model are equipped with temperatures and all noise sources are treated as thermal noise sources, an expression for the minimum noise temperature was obtained:

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{R_t T_g G_{ds} T_d} \tag{1}$$

where $R_t = R_s + R_g + R_i$, G_{ds} is the output conductance and T_g and T_d are the gate and drain resistance temperatures respectively. T_g is usually set to ambient temperature while the T_d should be considered as a nonphysical fitting parameter accounting for the bias dependent hot electron noise contribution. In opposite to previous models, this model takes the drain current dependent hot-electron noise into consideration

In [16] only f_T and T_d, among the parameters in (1), are considered to be strong functions of transistor bias. Hence, the optimal bias for low noise operation is obtained by minimizing the value of

$$f(V_{ds}, I_{ds}) = \frac{\sqrt{I_{ds}}}{g_m} \tag{2}$$

as T_d to a first approximation is proportional to I_d and f_T is proportional to the transconductance g_m.

To account for the shot noise generated by the gate leakage in an InP HEMT a noise current source can be added to the small signal model in Fig. 3.1. At low leakage currents the shot noise can be treated as ideal Schottky noise and its contribution be estimated as

$$i = \sqrt{2qI_g} \tag{3}$$

where q is the elementary charge and I_g is the measured gate leakage current.

3.2 DC Characterization

DC and RF characterization was performed at 4 K and 300 K in a Lakeshore model CRX-4K cryogenic probe station. Typical drain current I_d for 2x10 µm gate width devices are shown in Fig. 3.2. At 4 K, a kink is seen in the I–V characteristics at high I_d. Such behavior has been observed previously [1] when operating InP HEMTs at elevated drain currents under cryogenic conditions. Since the optimal bias of low-noise operation for the HEMT is for low I_d < 50 mA/mm, the kink phenomenon is far from the bias region of interest in this study. Maximum I_d at V_{ds} = 1 V of 1 A/mm at 4 K and 0.8 A/mm at 300 K was achieved.

A strong indicator for low noise performance in the InP HEMT is the response of DC transconductance g_m versus I_d [16]. This dependence is plotted in Fig. 3.3 which shows a very steep increase at low I_d. A g_m of more than 1 S/mm was observed for I_d of only 50 mA/mm at 4 K. Maximum DC g_m at V_{ds} = 1 V was 1.8 S/mm at 4 K and 1.4 S/mm at 300 K. At I_d of 15 mA/mm, g_m increases with 75 % to 0.6 S/mm when cooled down to 4 K. At 300 K g_m was around 0.8 S/mm at 75 mA/mm. As seen in the graph, g_m was also observed to be insensitive to V_{ds} at low drain current less than 100 mA/mm. This, in combination with the high value of g_m at this bias, enables high device performance at very low power dissipation.

As the bias region of interest for low noise operation is for low drain currents, the maximum I_d and g_m are not important. Fig. 3.4 shows measurements of the expression described in Eq. (2). The curves at 4 K exhibit a clear minimum which corresponds to the bias point I_d of 15 mA/mm. At this bias, confirmed by noise measurements, the lowest noise temperature is obtained for the InP HEMT at 4 K. At 300 K the minima does again agree with noise measurements showing a best low noise bias at I_d of 75 mA/mm. Furthermore, the minimum in Fig. 3.4 is relatively insensitive to V_{ds} pointing to low power dissipation of the HEMT under low noise operation.

At optimum low noise bias, the InP HEMT exhibited a very low gate current density I_g of 20 nA/mm at 4 K and 200 nA/mm at 300 K. The current-voltage characteristics of the gate Schottky diode at V_{ds} = 0 V is shown in Fig. 3.5. As clearly illustrated by Fig. 3.5, the gate leakage current at negative gate voltage is heavily suppressed due to the reduction of thermal emission of electrons over the Schottky barrier when cooled down to 4 K.

The fact that the gate current is low even at high V_{ds}, in combination with the high breakdown voltage (off-state defined as gate-to-drain voltage at I_d = 1 mA/mm in common source), measured to 6.5 V, shows that the HEMTs operate far from impact ionization.

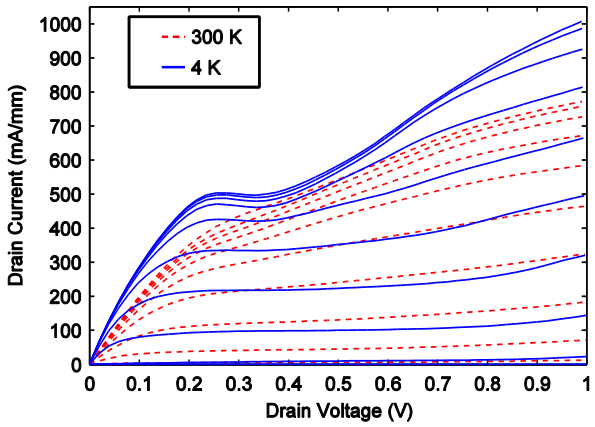

Fig. 3.2: Drain current of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{gs} measured from -0.3 V to 0.6 V in steps of 0.1 V.

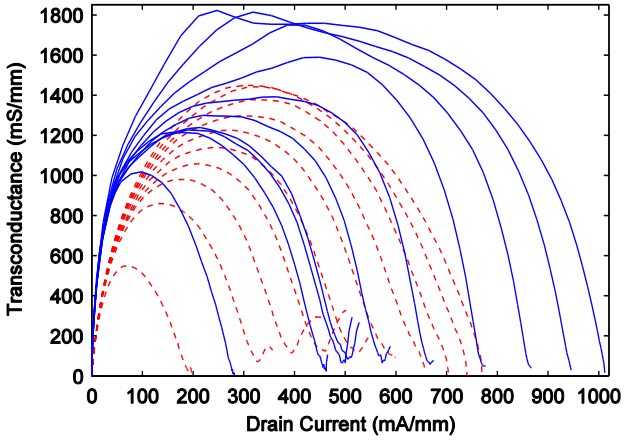

Fig. 3.3: Extrinsic g_m versus I_d of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{ds} measured from 0.1 V to 1 V in steps of 0.1 V.

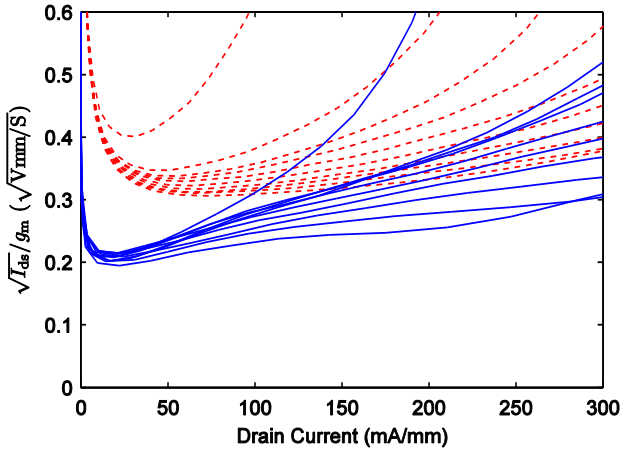

Fig. 3.4: $\sqrt{I_{ds}}/g_m$ versus I_d of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{ds} measured from 0.1 V (upper curve) to 1 V (lower curve) in steps of 0.1 V.

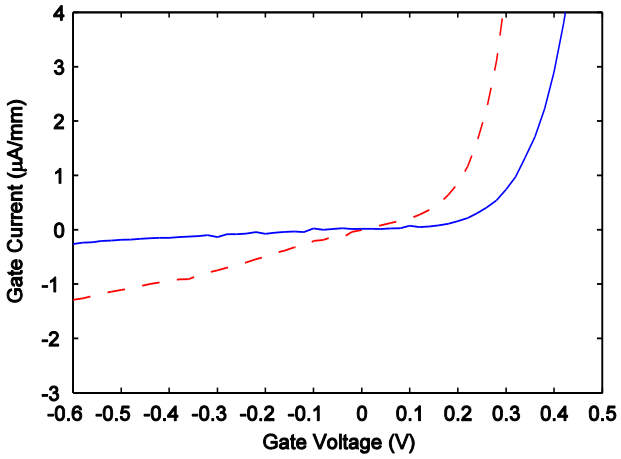

Fig. 3.5: Gate current of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{ds} = 0 V.

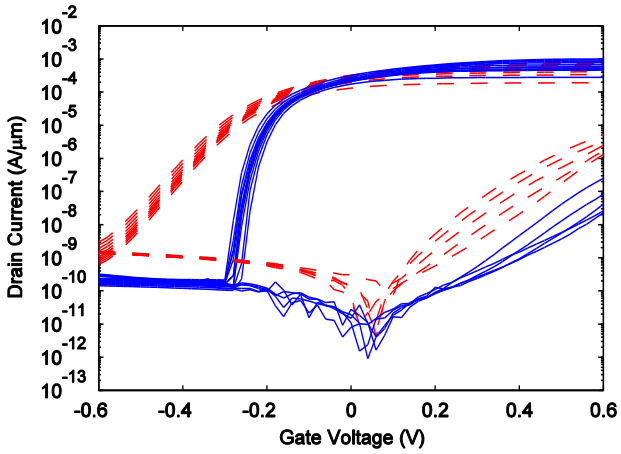

Fig. 3.6: Subthreshold and Ig characteristics of InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{ds} measured from 0.1 V to 0.5 V in steps of 0.1 V

The subthreshold characteristics are important figures-of-merit for low noise transistors operating close to pinch-off. In Fig. 3.6 the subthreshold and I_g characteristics of the InP HEMTs in this study are shown. At 4 K the subthreshold swing S was 20 mV/dec with drain induced barrier lowering DIBL of 40 mV/V. At 300 K the numbers were 72 mV/dec and 40 mV/V respectively. It is observed that the numbers at room temperature are considerable better than a 50 nm InP HEMT technology analyzed for logic applications showing S of 86 mV/dec and DIBL of 160 mV/V [21].

3.3 Microwave Characterization

S-parameter measurements were done using an Agilent 67 GHz PNA. A direct extraction method was used to obtain the small signal parameters of the model in Fig. 3.1 [22, 23]. The gate resistance R_g, which is an input parameter in the direct extraction, was obtained from DC measurements of gate through-line test structures, was 130 Ω/mm at 4 K and 300 Ω/mm at 300 K.

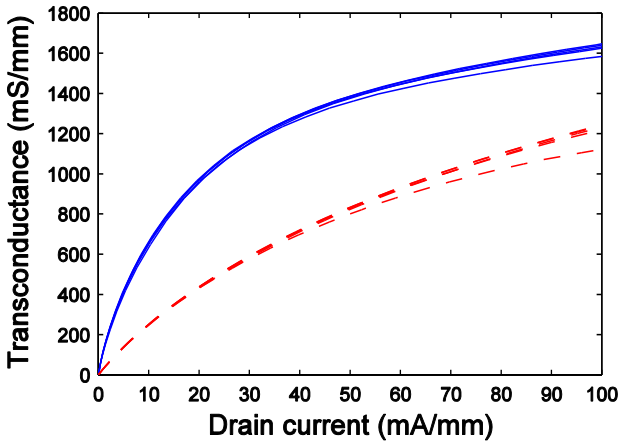

Fig. 3.7: Intrinsic g_m of a 2x100 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{ds} measured from 0.2 V (lower curve) to 1 V (upper curve) in steps of 0.2 V.

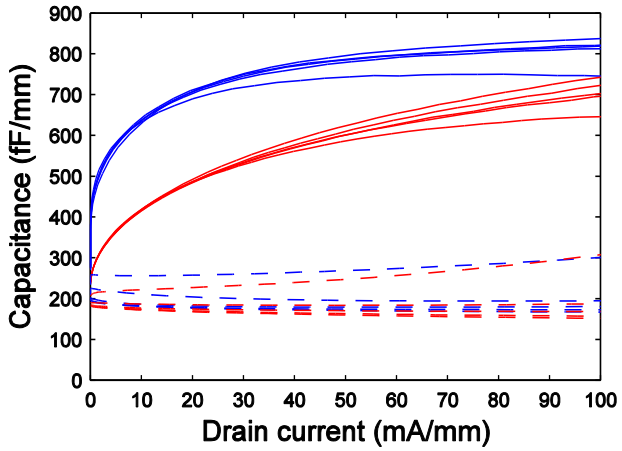

Fig. 3.8: C_{gs} (solid) and C_{gd} (dashed) of a 2x100 µm gate width and 130-nm gate length InP HEMT at 300 K (red) and 4 K (blue) ambient temperature. V_{ds} measured from 0.2 V (upper curve) to 1 V (lower curve) in steps of 0.2 V.

The only model parameters in Fig. 3.1 without bias dependence at all are the parasitic resistances R_s and R_g and their equivalent temperature T_g. At 300 K, R_s and R_g were typically 0.24 Ω·mm and 310 Ω/mm. At 4 K the values are 0.13 Ω·mm and 130 Ω/mm, respectively. Intrinsic R_i was fairly insensitive to bias but strongly dependent on temperature, and was decreased from 0.85 Ω·mm at 300 K to 0.45 Ω·mm at 4 K.

Intrinsic g_m of a 2x100 µm gate width device is shown in Fig. 3.7. g_m was observed to increase with more than 100 % at low I_d of 15 mA/mm when the InP HEMT was cooled down to 4 K. g_m was also observed to be very insensitive to V_d, indicating potentially good low power operation at both 4 K and 300 K.

C_{gs} and C_{gd}, which together with g_m determine f_T and hence are very important for low noise performance, are shown in Fig. 3.8. C_{gs} was observed to be a strong function of temperature and in opposite to [16] also a strong function of bias. At I_d of 15 mA/mm, C_{gs} was observed to increase about 30 % when cooled down to 4 K. C_{gd} was observed to be less dependent of temperature and bias. At pinch-off, when the depletion area in the channel is close to symmetric, C_{gs} and C_{gd} approach the same value of 200-250 fF/mm

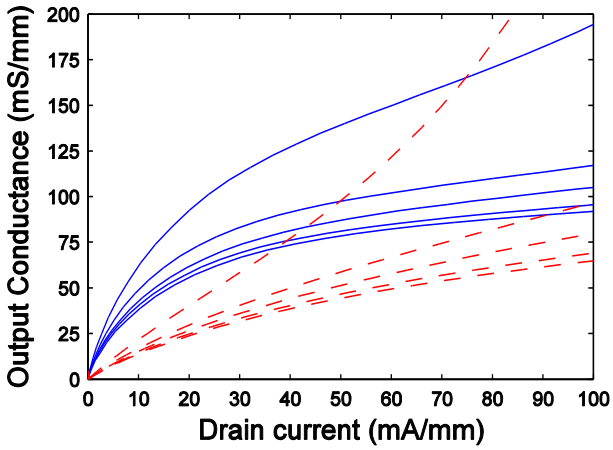

Fig. 3.9: Intrinsic G_{ds} of a 2x100 µm gate width and 130-nm gate length InP HEMT at 300 K (red dashed) and 4 K (blue solid) ambient temperature. V_{ds} measured from 0.2 V (upper curve) to 1 V (lower curve) in steps of 0.2 V.

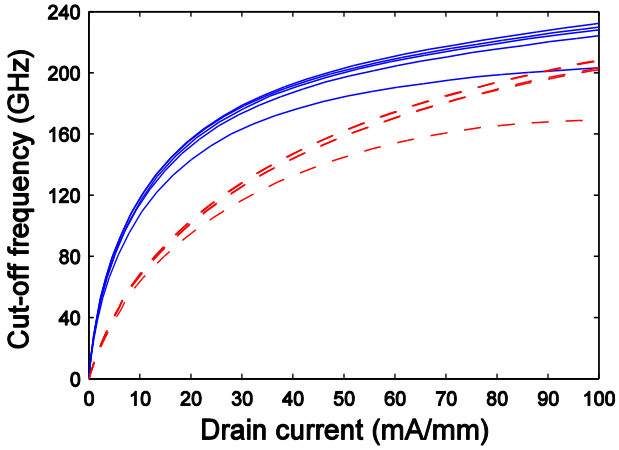

Fig. 3.10: Intrinsic f_T at 300 K (red dashed) and 4 K (blue solid) at low I_d. V_d stepped between 0.2 V (lower curve) and 1 V (upper curve) in steps of 0.2 V.

independent of temperature. In forward mode, I_d > 200 mA/mm, C_{gs} saturates at 800 fF/mm, while C_{gd} is slightly decreased to 150 fF/mm. The transition between these two boundary conditions is however strongly temperature dependent. At 4 K, as seen Fig. 3.8, C_{gs} increased very abrupt and reached the saturated value of 800 fF/mm at much lower I_d than at 300 K. In a physical perspective this requires a more confined current distribution close to the top of the channel, where the gate control is higher, when operating at 4 K compared to 300 K.

Output conductance G_{ds}, shown in Fig. 3.9, was found to increase with I_d. When cooled down a slight increase of G_{ds} was observed. As seen in Fig. 3.9, a degradation of G_{ds} was observed to for V_d < 0.2 V.

The I_d dependence of f_T is shown in Fig. 3.10. A clear improvement at low I_d was observed when cooling down the InP HEMTs. Beyond the low noise bias region, at high I_d > 200 mA/mm, f_T saturated at 250 GHz independent of temperature.

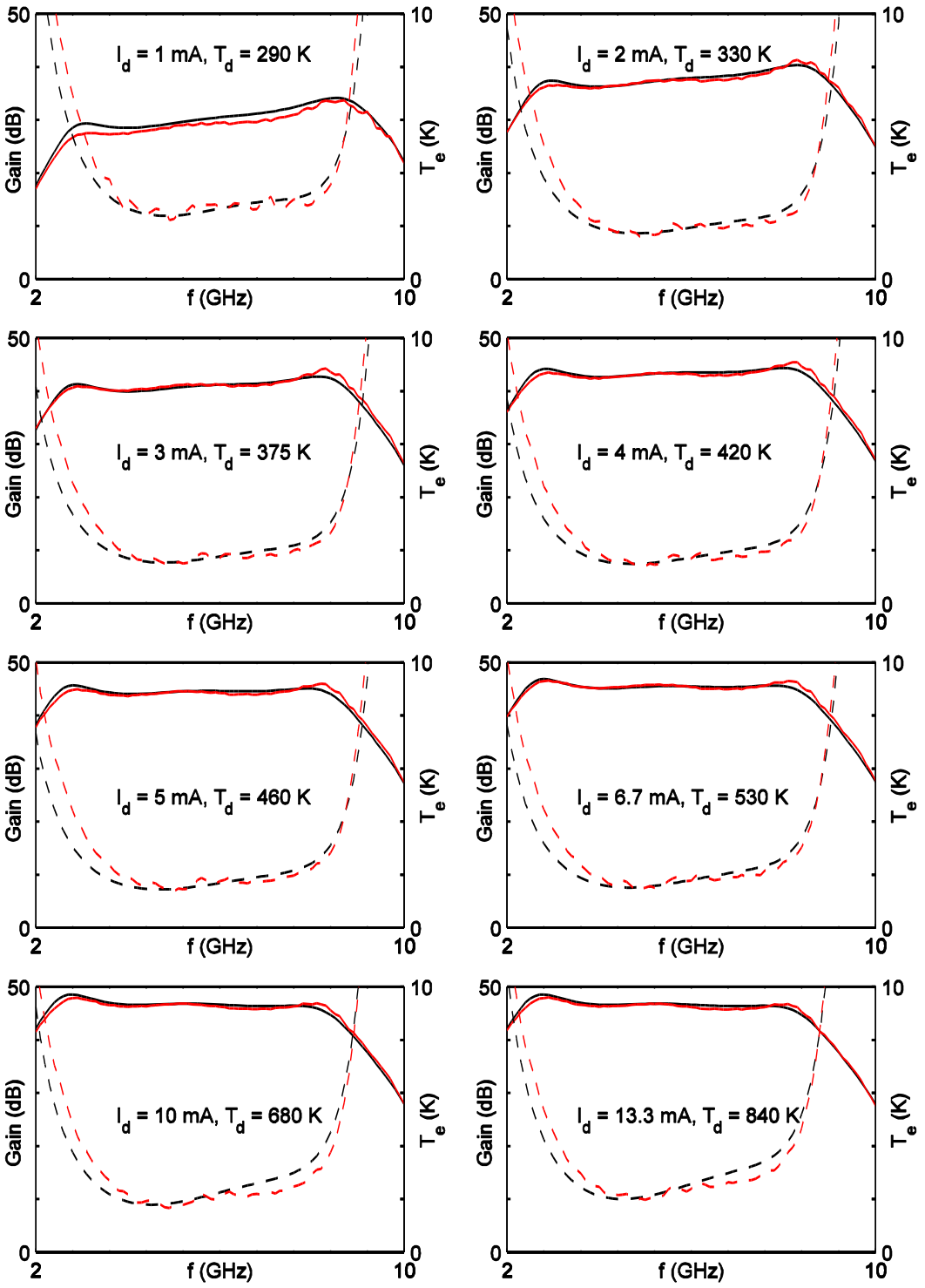

Fig. 3.11: Measured (red) and simulated (black) noise temperature (dashed) and gain (solid) at 10 K of a 3-stage hybrid 4–8 GHz LNA with 2x100 µm InP HEMTs. The 3-stage amplifier was biased so that V_{ds} over the InP HEMTs was 0.6 V in all graphs. I_d, denoting the drain current of one InP HEMT, was stepped between 1 mA (top left) and 13.3 mA (bottom right).

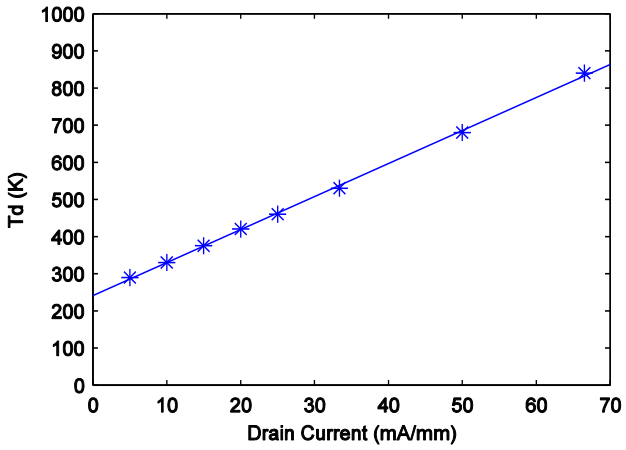

Fig. 3.12: Drain resistor temperature T_d extracted at different drain current densities from Fig. 3.11. V_d was 0.6 V for all extraction points and I_d was swept between 1 mA and 13.3 mA (5 mA/mm and 66.5 mA/mm) for each 2x100 µm InP HEMT.

3.4 Noise Characterization

Since InP HEMTs display extremely low noise at cryogenic conditions, direct noise parameter measurements are generally not possible with acceptable accuracy. Therefore an indirect method using an LNA must be used [6]. 4x50 µm InP HEMTs were integrated in a 3-stage hybrid 4-8 GHz LNA. Noise temperature for the LNA was measured at 10 K using a cold attenuator setup with a maximum uncertainty less than 1.3 K [24]. Repeatability of the measurement was better than 0.1 K.

To extract the noise parameters of the InP HEMT, a small signal model of the LNA, containing the extracted bias dependent InP HEMT model in Fig. 3.1, was used.

In Fig. 3.11 the measured and simulated noise temperature and gain of the 4-8 GHz LNA is shown for 8 different bias points. In each graph the small signal model and the noise measurement was performed at the same bias point of the InP HEMT. The value of T_d could then be extracted for the best fit between the simulation and measurement.

In Fig. 3.12 the extracted T_d is plotted against I_d. In accordance with [16], T_d was observed to be close to linearly dependent on I_d. However, T_d seems not to approach the ambient temperature as the transistor is pinched off. Instead a higher value of 230 K was obtained for very low values of I_d. The reason for this is still not fully understood.

With the extracted T_d in Fig. 3.12, the minimum noise temperature of the InP HEMT could be extracted. In Fig. 3.13 T_{min} is plotted against I_d. Without consideration of the shot noise contribution from the gate leakage current, the lowest T_{min} was less than 1.2 K (red dots in Fig. 3.13). When considering the gate current, T_{min} increased with 0.2 K.

Independent of the gate current, the optimum low noise bias was V_d = 0.6 V and I_d around 15 mA/mm. This is also in agreement with the LNA measurements in Fig. 3.11 which exhibit a lowest noise temperature of 1.4 at I_d of 15 mA/mm per stage. At 300 K the optimum low noise bias was obtained at 75 mA/mm.

To test the noise model suggested in[20], Eq. (1) was evaluated with the extracted f_T, R_t, G_{ds} and T_d and plotted in Fig. 3.13. It is seen that the expression of T_{min} agrees very well with the simulations.

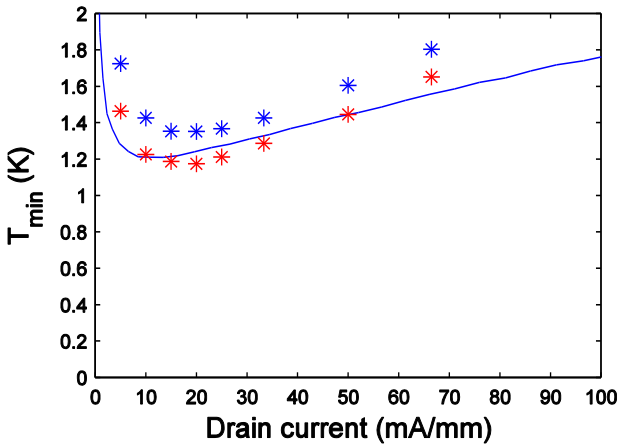

Fig. 3.13: Extracted T_{min} with (blue dots) and without (red dots) consideration of the gate current. The noise model suggested in [20] and based on extracted f_T, R_t, G_{ds} and T_d is shown by the blue curve.

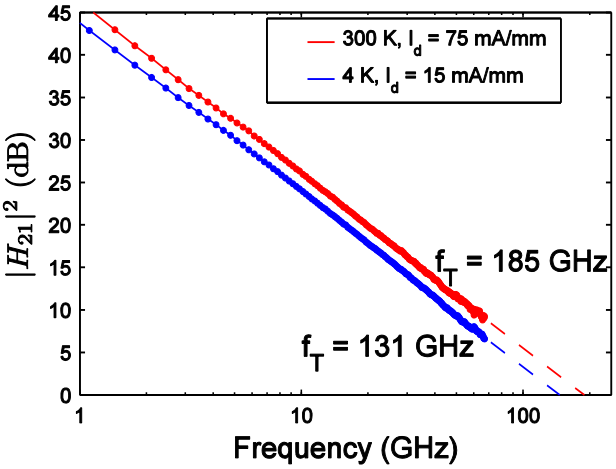

Fig. 3.14: Intrinsic current gain $|H_{21}|^2$ at optimum low noise bias of V_d = 0.6 V and Id = 15 mA/mm at 4 K and 75 mA/mm at 300 K

All extracted model parameters for optimum low noise bias at 4 K and 300 K are shown in Table 3.1. For these bias points the current gain $|H_{21}|^2$ is plotted in Fig. 3.14. The resulting f_T was 131 GHz at 4 K and I_d of 15 mA/mm and 185 GHz at 300 K and I_d of 75 mA/mm respectively.

The fact that the optimum low noise bias of the InP HEMT occurs at I_d as low as 15 mA/mm cryogenic temperatures, and not at high I_d where the small signal performance is at its optimum, makes traditional InP HEMT figure-of-merits as maximum I_d, maximum g_m and maximum f_T obsolete. Instead, the InP HEMT needs to exhibit high I_d, g_m and f_T at as low I_d as possible to minimize the tradeoff in Eq. (1).

For the InP HEMTs in this work, g_m increased with more than 100 % to 0.7 S/mm when cooled down to 4 K at the best cryogenic low noise bias of I_d = 15 mA/mm. At the optimum low noise bias at room temperature, I_d = 75 mA/mm, g_m was typically 0.8 S/mm at 300 K. At both 4 K and 300 K the numbers were far below the maximum g_m of 2 S/mm and 1.5 S/mm, respectively. Also f_T was much lower at the optimum low noise bias than at the optimum high frequency bias. At 4 K it is only about 50 % of maximum f_T and even lower than at the optimum low noise bias at 300 K.

TABLE 3.1
EXTRACTED VALUES FOR THE SMALL-SIGNAL MODEL OF 4X50 μM INP HEMT AT OPTIMUM LOW NOISE BIAS AT 300K AND 10 K

		300 K	10 K
Bias	V_{ds}	0.6	0.6
	I_d	15	3.3
	V_{gs}	-0.14	-0.18
Intrinsic	C_{gs}	132	138
	C_{gd}	34	37
	C_{ds}	52	46
	g_m	213	176
	R_i	3.9	2.2
	R_j	33	25
	G_{ds}	13	11
Parasitics	C_{pg}, C_{pd}	19	20
	L_g	35	46
	L_s	-0.8	0.4
	L_d	36	47
	R_g	5	2.2
	R_d	1.3	0.7
	R_s	1.2	0.6
Noise	T_d	2800	400

3.5 State-of-the-art ultra-low noise InP HEMTs

A new state-of-the-art result for T_{min} using ultra-low noise InP HEMTs has been demonstrated in this work. The noise temperature and gain as a function of frequency at 10 K for different bias points of a 4-8 GHz LNA equipped with InP HEMTs is shown in Fig. 3.15. At the optimum low noise bias (V_{DD} = 0.45 V, I_{DD} = 9.3 mA), a lowest noise temperature $T_{e,min}$ of 1.2 K was measured at 5.2 GHz. Across the 4-8 GHz band, the average noise temperature $T_{e,avg}$ was 1.6 K at the same bias point. Moreover, the average gain of the amplifier was 44 dB, with input and output return loss better than 15 dB, in the entire band. The total power consumption of the LNA at this bias was only 4.2 mW. The extracted T_{min} at 10 K, shown in Fig. 3.16, was 1 K at 6 GHz.

When the LNA was biased for ultra-low power consumption of 0.33 mW (V_{DD} = 0.1 V, I_{DD} = 3.3 mA), the noise temperature and gain still exhibited numbers of 2.5-4.3 K and 27-34 dB, respectively. At room temperature, the measured LNA noise temperature was typically 25-30 K with a gain of 44 dB at a power consumption of 56 mW (V_{DD} = 1.25 V, I_{DD} = 45 mA). We present in Table 3.2 our results compared to previously published state-of-the art 4x50 μm InP HEMT LNAs operating at 10-15 K ambient temperature. The 4-8 GHz LNA using the InP HEMTs in this study exhibited a significantly lower $T_{e,min}$ and $T_{e,avg}$ than previously published results. Moreover, the gain per mW dissipated power was almost a factor of two higher than [25].

TABLE 3.2
DATA FOR STATE OF THE ART 4X50 μM INP HEMT LNAS AT 10-15 K

Ref.	Freq. (GHz)	$T_{e,min}$ (K)	$T_{e,avg}$ (K)	Gain/stage (dB)	Gain/power (dB/mW)
This work	4-8	1.2	1.6	14.7	10.5
[2]	4-8	1.4	1.8	13.5	2.5
[25]	4-8	3.1	3.5	13.5	6.8
[26]	4-12	3.3	4.5	11.3	-
[27]	4-12	2.7	3.5	13.7	1.7

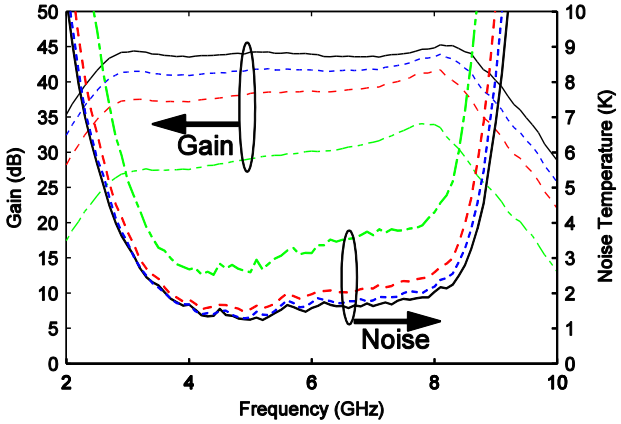

Fig. 3.15: Noise temperature and gain at 10 K of a 3-stage hybrid 4–8 GHz LNA. The 3-stage amplifier was biased at V_{DD} = 0.1 V, I_{DD} = 3.3 mA (green dash-dot); V_{DD} = 0.2 V, I_{DD} = 6 mA (red long dash); V_{DD} = 0.3 V, I_{DD} = 8 mA (blue short dash) and optimum bias V_{DD} =0.45 V, I_{DD} = 9.3 mA (black solid).

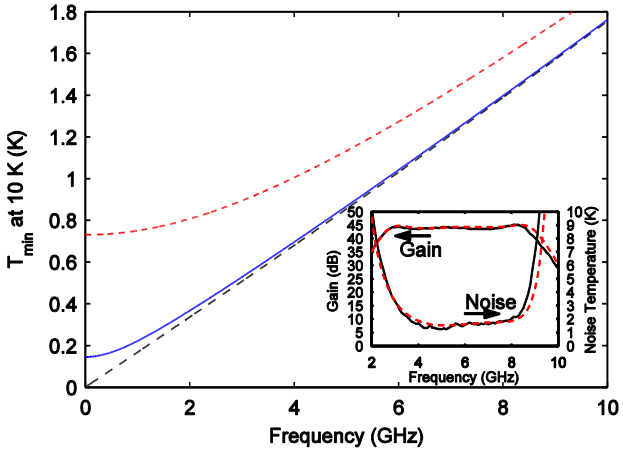

Fig. 3.16: Extracted T_{min} of a 4x50 μm InP HEMT exhibiting 20 nA/mm gate current at 10 K (blue solid) compared with the same device without gate current (black long dash) and with 0.5 μA/mm gate current (red short dash). The InP HEMT was biased at V_{ds} = 0.35 V and I_d = 3.1 mA. Inset shows a comparison between simulated (red dashed) and measured (black solid) noise temperature and gain of the 3-stage LNA in Fig. 3.15 using the extracted transistor model.

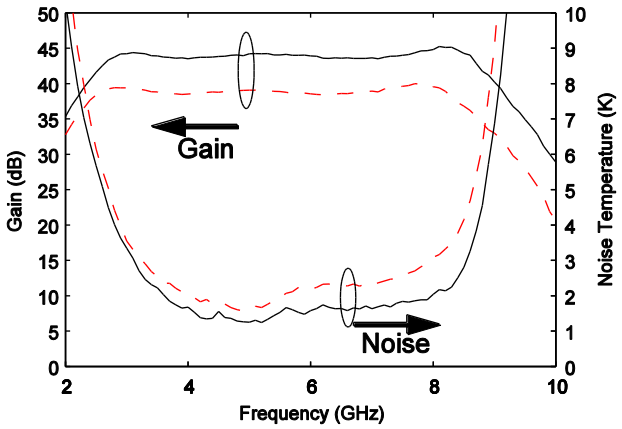

Fig. 3.17: Comparison of gain and noise temperature between 4x50 um InP HEMTs in this study (black curves) and previous state-of-the-art CRYO3 InP HEMTs [2] (red curves) measured at ambient temperature of 10 K in the same LNA in the same measurement system. The amplifier was in both cases biased at optimum low noise bias. Bias with Chalmers InP HEMTs was Vd=0.45V and Id=9.3mA. Bias with CRYO3 InP HEMTs was Vd=0.6V and Id=10mA.

The uncertainty in the noise measurement is in the same range as the measured noise. To further validate the comparison, 100 nm gate length InP HEMTs with size 4x50 µm used in [2] (CRYO3 devices) were benchmarked against the InP HEMTs in this study using the same 4-8 GHz LNA and identical measurement procedure. A graph showing gain and noise temperature of the LNA with the two different InP HEMTs at 10 K is shown in Fig. 3.17. The average noise temperature was in this case 2.2 K with an average gain of 39 dB at optimum low noise bias (V_{DD} = 0.6 V, I_{DD} = 10 mA). Hence 0.6±0.1 K better noise performance was obtained for the LNA based on the InP HEMTs in this study compared to the CRYO3 InP HEMTs used in [2].

The outstanding low noise performance of the InP HEMT is believed to be a result of the optimized epitaxial structure and gate recess resulting in high transconductance and f_T at low drain current. Also the low access resistances are a prerequisite for obtaining so low noise temperature. Finally the low gate current enables the InP HEMTs to perform well at very low frequencies where the noise normally is limited by shot noise from the gate Schottky barrier. In Fig. 3.16 the importance of low gate current is emphasized by showing two modeled InP HEMTs either with zero gate current or with a representative gate current of 0.5 µA/mm.

Chapter 4.

InP HEMT MMIC Technology

In future large telescopes for radio astronomy, the collecting area will be divided into arrays of smaller reflectors [28-30]. These telescopes will take advantage of the recent development in ultra-wideband technology which will allow them to cover decades of bandwidth with a minimum number of receivers. The proposed square kilometer array (SKA) will cover 0.1-25 GHz and the 1 km^2 collecting area will be made out of thousands of antennas each equipped with several receivers covering different frequency bands, or even with focal plane arrays. The widest band cryogenic low noise amplifiers (LNAs) reported so far usually exhibit around 100% of bandwidth. A cryogenic MMIC LNA used in the Arecibo radio telescope has a noise temperature of 3.5 K with 41 dB of gain at 4-12 GHz measured at ambient temperature of 12 K [31].

In this paper we present a broadband cryogenic MMIC LNA up to 13 GHz based on the InP HEMT technology developed in Chapter 2 and 3. To addresses the need for future large arrays either as IF-amplifier for SIS or Schottky mixer or directly connected to the feed, the LNA input impedance can be adapted to match the source.

4.1 Ultra Broadband Ultra Low Noise InP MMIC LNA

The InP HEMT process described in Chapter 2 was expanded to a full microstrip MMIC process by introducing passive components: thin film resistors (TFRs), MIM capacitors, via-hole grounding, and microstrip lines. For TFRs, NiCr with a sheet resistance of 50 Ω/□ was used. The MIM capacitors were fabricated using 150 nm thick Si_3N_4 as dielectric, giving a specific capacitance of 390 pF/mm^2. The wafer was thinned down to a thickness of 75 μm. Via-holes with a diameter of 45μm were dry etched through the substrate. Finally, the substrate backside was gold plated to allow grounding through the via-holes and to form a ground plane for the microstrip lines.

An accurate noise model of the transistor, as described in Chapter 3, is crucial for a successful LNA design. The model used for the MMIC LNA in this thesis was based on an equivalent small signal circuit of 2x100 μm InP HEMTs from a previous batch. The extracted T_{min} at ambient temperature of 15 K, shown in Fig. 4.1, was 3 K at 12 GHz.

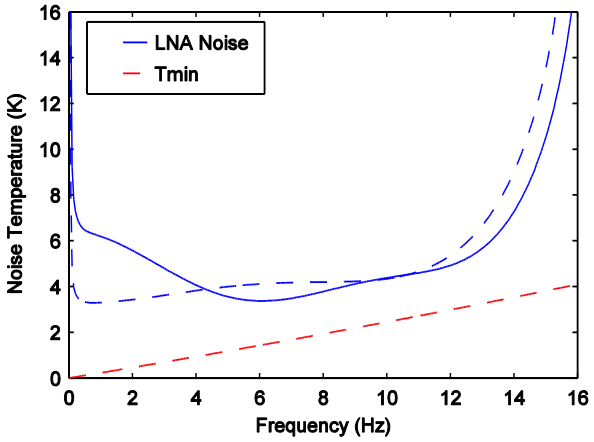

Fig. 4.1: Extracted T_{min} of a 2x100 um InP HEMT at 15 K (red dashed) compared with the simulated noise temperature of the amplifier connected to a 50 Ω source impedance (blue solid) and 100 Ω source impedance (blue dashed). The InP HEMT was biased at V_{ds} = 0.6 V.

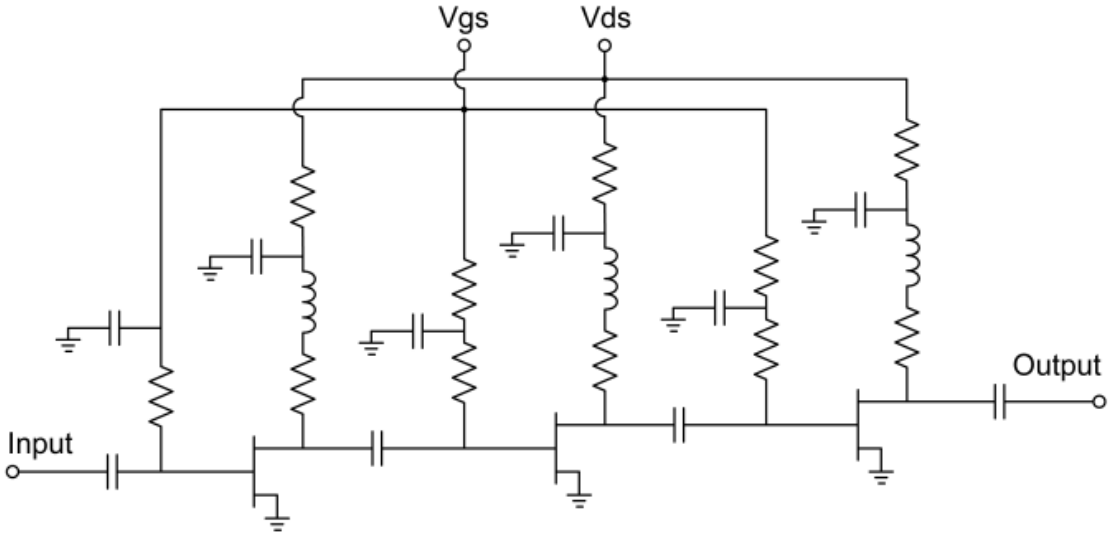

Fig. 4.2: Schematic of the 3-stage 0.5-13 GHz MMIC LNA.

Network matching was performed using MIM capacitors, TFRs, via-holes and microstrip lines. All three stages utilize 2x100 μm gate width devices with a common bias network.

In an LNA design, the matching network of the first stage ultimately sets the noise performance of the whole amplifier. To avoid substrate losses, and consequently degraded noise performance, an external input matching network on a low loss RT Duroid 6002 substrate was used. To improve stability and decrease the magnitude of S_{11}, a source inductance was introduced at the input of the first transistor using a narrow microstrip line. A schematic of the 3-stage LNA is shown in Fig. 4.2.

Since the impedance of the minimum noise figure is frequency dependent, designing a decade bandwidth LNA means a tradeoff between noise performance and bandwidth. As the minimum noise figure is close to linearly dependent on frequency as seen in Fig. 4.1, the best tradeoff regarding noise performance is to match the first transistor at the upper frequency limit and tolerate some mismatch at lower frequencies. By doing this, the noise

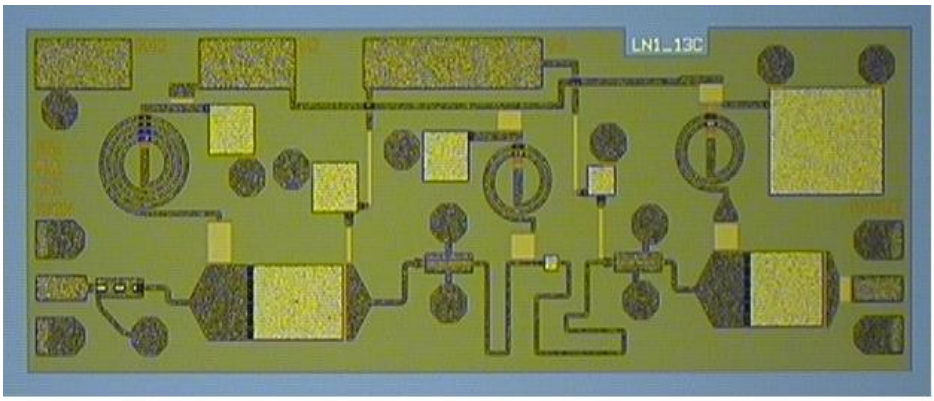

Fig. 4.3: Photograph of fabricated 3-stage 0.5-13 GHz MMIC LNA.

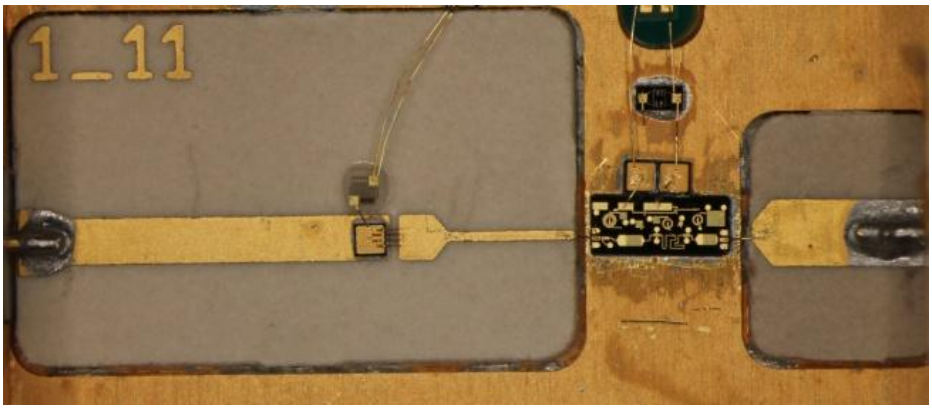

Fig. 4.4: Photograph of 3-stage MMIC mounted in housing together with the input matching network.

temperature of the amplifier could be held relatively constant with frequency and close to the minimum noise temperature at the upper frequencies; see Fig. 4.1. The second and third stages were then matched for flat gain and stability. A photograph of the 2x0.75 mm^2 MMIC can be seen in Fig. 4.3.

When used as IF-amplifier for Schottky or SIS mixers it is advantageous to omit the standard 50 Ω interface as often higher impedance is needed. Fig. 4.1 shows simulated result of the LNA using an input matching network optimized for 100 Ω source impedance. With this network, using the same RT Duroid 6002 substrate as the 50 Ω network, the bandwidth is then increased to 0.1-13 GHz.

A housing using SMA input and output connectors was designed and machined to package the MMIC LNA. A photograph of a mounted MMIC with input matching network can be seen in Fig. 4.4.

RF characterization of the mounted 3-stage LNA including the input matching network was performed at room temperature using Agilent E8361A Network Analyzer. The bias of the LNA was V_d = 2.35 V and I_d = 45 mA. As seen in Fig. 4.5, the LNA had relatively flat gain (S_{21}) between 34 dB and 40 dB in the whole 0.5-13 GHz band. Input return loss (S_{11}) has been traded off against noise performance at low frequencies but is better than 7 dB between 3 and 13 GHz. Output return loss (S_{22}) was better than 8 dB within the whole band.

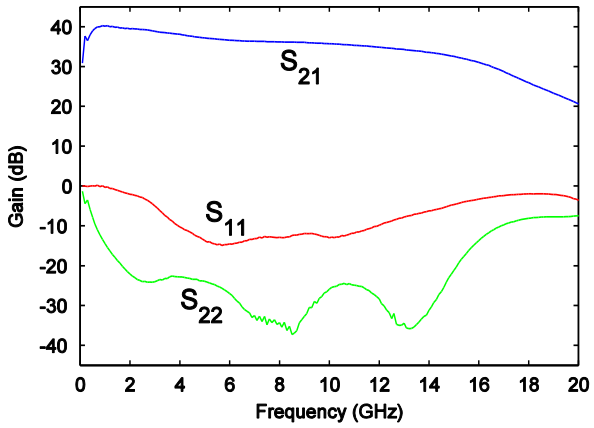

Fig. 4.5: Measured S-parameters of a 0.5-13 GHz LNA module at 300 K

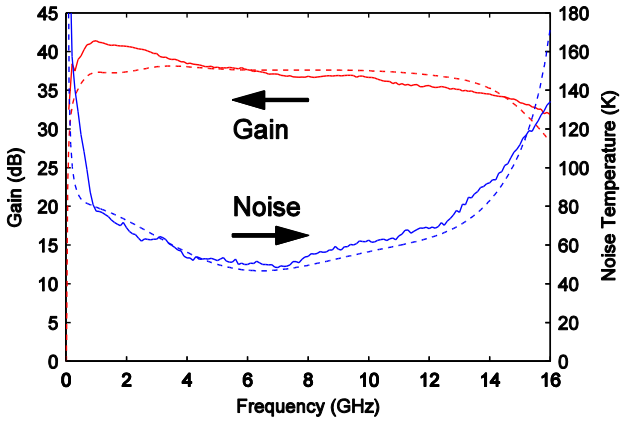

Fig. 4.6: Measured (solid) and simulated (dashed) gain and noise temperature of 0.5-13 GHz LNA module at 300 K.

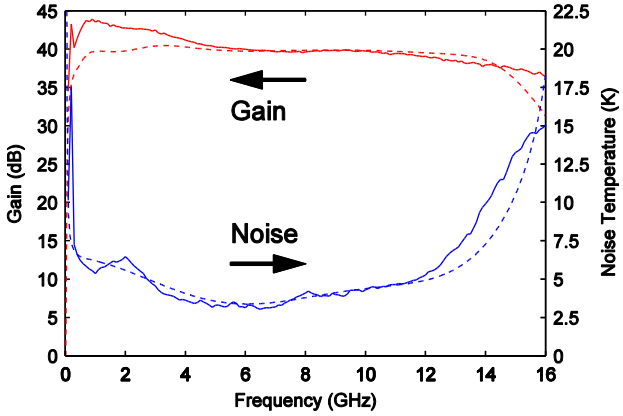

Fig. 4.7: Measured (solid) and simulated (dashed) gain and noise temperature of 0.5-13 GHz LNA module at 15 K.

Noise measurements were performed both at 300 K and 15 K using Agilent N8975A Noise Figure Analyzer. Fig. 4.6 shows the measured noise temperature and gain at room temperature. The lowest noise was 48 K and was achieved around 7 GHz. The gain, consistent with the S-parameter measurements, was above 34 dB in the whole band.

When cooled down to 15 K, the optimum low noise bias of the LNA was V_d = 1.1 V and I_d = 15 mA, resulting in a total power dissipation of 16.5 mW. As seen in Fig. 4.7, the lowest noise temperature at cryogenic condition was 3 K at 7 GHz and below 7 K in the whole 0.5-13 GHz band. The gain was slightly increased compared to room temperature and was higher than 38 dB in the whole band.

The LNA presented in this work shows very good noise performance over a very wide frequency range of 0.5-13 GHz. The measured gain however was not as flat as the simulated. This is attributed to the back thinning of the MMIC which resulted in a substrate thickness of 45 μm instead of 75 μm. Also the thin film resistors, designed to have 50 Ω/□ resistance ended up having 70 Ω/□. This unexpected process variation did however not degrade the LNA noise performance.

Chapter 5.

Conclusions and Future Outlook

This thesis has demonstrated the behavior and optimization of cryogenic ultra-low noise InP HEMTs. The performance of InP HEMTs before and after passivation with Al_2O_3 ALD and Si_3N_4 PECVD has been compared. Both passivation methods resulted in improved DC performance with a 20% increase in maximum drain current and a 30% increase in extrinsic transconductance. In contrast to PECVD passivated InP HEMTs, ALD passivated devices demonstrated a major suppression of the kink in the output I-V characteristics associated with surface traps. This is the first time Al_2O_3 ALD has been demonstrated as device passivation for InP HEMTs.

Ultra-low-noise InP HEMTs with 130 nm gate length have been designed and fabricated for cryogenic temperature operation. When integrated in a 4-8 GHz 3-stage hybrid IF LNA, a noise temperature of 1.2 K ± 1.3 K with an average gain of 44 dB and power dissipation of only 4.2 mW was measured at ambient temperature of 10 K. Extracted T_{min} of the InP HEMT was 1 K at 6 GHz. This minimum noise temperature represents a new state-of-the-art for cryogenic InP HEMT technology.

The ultra-low noise properties of the InP HEMT technology has been demonstrated by designing and processing a cryogenic 0.5-13 GHz 3-stage MMIC LNA. The noise temperature of this LNA was 3 K at the lowest point and below 7 K in the entire 0.5-13 GHz frequency band.

This thesis has pointed out that to reach future progress in cryogenic InP HEMT technology, a deeper understanding of the cryogenic properties of the InP HEMT is needed. A better understanding of the parameter T_d, used in the noise model, and its connection to device physics, HEMT design and material is absolutely necessary.

Further scaling is necessary to operate at higher frequencies beyond W-band. This will put high demands on epitaxial and process design to maintain the excellent noise properties obtained with the 130 nm gate length technology used today.

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