Thesis for The Degree of Licentiate of Engineering

Modelling of Terahertz Planar Schottky Diodes

Aik Yean Tang

Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience (MC2)
Chalmers University of Technology
Göteborg, Sweden
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AIK YEAN TANG

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Chalmers University of Technology
Department of Microtechnology and Nanoscience (MC2)
Terahertz and Millimetre Wave Laboratory
SE-412 96 Göteborg, Sweden
Phone: +46 (0) 31 772 1000

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Abstract

This thesis deals with the modelling of THz planar Schottky diodes, focusing on analyses of the geometry-dependent parasitics and the diode chip thermal management. Moving towards higher operating frequencies, the electromagnetic couplings pose significant limitations on the diode performance.

In this work, a model of the loss at high frequencies for planar diodes is developed, specifically the ohmic losses in the cathode buffer mesa is analysed. As a result, the eddy current, skin and proximity effects have been identified as important loss mechanisms in the buffer mesa. This provides an explanation to the strong frequency dependency of the series resistance, which is not explainable using conventional diode series resistance models. Due to the current crowding effect, the upper boundary of the buffer-layer thickness is approximately one skin depth at the operating frequency, whereas the lower boundary is limited by the spreading resistance at DC.

In addition to the ohmic loss, the parasitic capacitance and inductance inherently limit the power coupling to the diode junction. A model is developed to analyse this limitation, i.e by studying the diode resonance frequencies as a function of diode geometry. Analysis of the diode resonance frequencies as a function of the pad-to-pad distance is presented. Result shows that there is a trade-off between the parasitic capacitance and inductance, in optimising the power coupling to the junction.

Based on the chip layout of frequency doublers developed by Jet Propulsion Laboratory (JPL), a systematic thermal analysis of the multiplier chip is performed. Taking the temperature-dependent material thermal properties into consideration, the result shows that the thermal resistance of the 200 GHz multiplier chip is in the order of 10^3 K/W. Meanwhile, the thermal time constant is more than tens of milliseconds. The simulation result is verified through thermal imaging using infrared microscope.

Taking the thermal analysis a step further, a self-consistent electro-thermal model for the multiplier chip is proposed. The thermal model is developed using a thermal resistance matrix approach, with a linear-temperature dependency approximation of the thermal resistance. Compared to the circuit analysis without thermal model, analysis with the electro-thermal model shows a better agreement with the measured result, i.e. within 5% of the measured conversion efficiency.

Keywords: Current crowding, Electromagnetic, Electro-thermal, Frequency multipliers, Gallium Arsenide, Geometric modelling, High-power frequency multiplier, Proximity effect, Schottky diodes, Skin effect, Submillimetre wave generation and detection, S-parameter extraction.

List of publications

Appended papers

This thesis is based on the following papers:

[A] A. Y. Tang and J. Stake, "Impact of Eddy Currents and Crowding Effects on High Frequency Losses in Planar Schottky Diodes," in *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3260-3269, Oct. 2011.

[B] A. Y. Tang, E. Schlecht, G. Chattopadhyay, R. Lin, C. Lee, J. Gill, I. Mehdi, and J. Stake, "Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes," 22nd *International Symposium on Space Terahertz Technology (ISSTT)*, Tucson, AZ, USA, Apr. 2011.

[C] A. Y. Tang, E. Schlecht, R. Lin, G. Chattopadhyay, C. Lee, J. Gill, I. Mehdi, and J. Stake, "Electro-thermal model for Multi-Anode Schottky Diode Multipliers," submitted to *IEEE Transactions on Terahertz Science and Technology*, 2011.

Other papers and publications

The following publications are not included due to an overlap in contents or the contents are beyond the scope of this thesis.

[a] J. Stake, H. Zhao, P. Sobis, A. Y. Tang, and V. Drakinskiy, "Development of a Compact 557 GHz Heterodyne Receiver," 6th *ESA Workshop on Millimetre-Wave Technology and Applications*, Espoo, Finland, May, 2011.

[b] H. Zhao, A. Y. Tang, P. Sobis, T. Bryllert, K. Yhland, J. Stenarson, and J. Stake, "Submillimeter Wave S-Parameter Characterization of Integrated Membrane Circuits," in *IEEE Microwave and Wireless Components Letters*, pp. 110-112, February, 2011.

[c] H. Zhao, T. D. Thanh Ngoc, P. Sobis, A. Y. Tang, K. Yhland, J. Stenarson, and J. Stake, "Characterization of Thin-Film Resistors and Capacitors Integrated on GaAs Membranes for Submillimeter Wave Circuit Applications," 23rd *International Conference on Indium Phosphide and Related Materials (IPRM)*, Berlin, Germany, May, 2011.

[d] J. Stake, T. Bryllert, P. Sobis, A. Y. Tang, H. Zhao, J. Vukusic, A. Malko, V. Drakinskiy, A. Olsen, and A. Emrich, "Development of Integrated Submillimeter Wave Diodes for Sources and Detectors," 5th *European Microwave Integrated Circuits Conference*, September, 2010.

[e] A. Y. Tang, P. Sobis, H. Zhao, V. Drakinskiy, T. Bryllert, and J. Stake, "Analysis of the High Frequency Spreading Resistance for Surface Channel Planar Schottky Diodes," 35th *International Conference on Infrared, Millimeter and Terahertz Wave (IRMMW)*, Rome, Italy, September, 2010.

[f] A. Y. Tang, P. Sobis, V. Drakinskiy, H. Zhao, and J. Stake, "Parameter Extraction and Geometry Optimisation of Planar Schottky Diodes," 21st *International Symposium on Space Terahertz Technology (ISSTT)*, Oxford, UK, March, 2010.

[g] H. Zhao, A. Y. Tang, P. Sobis, V. Drakinskiy, T. Bryllert, and J. Stake, "Characterization of GaAs Membrane Circuits for THz Heterodyne Receiver Applications," 21st *International Symposium on Space Terahertz Technology (ISSTT)*, Oxford, UK, March, 2010.

[h] H. Zhao, A. Y. Tang, P. Sobis, T. Bryllert, K. Yhland, J. Stenarson, and J. Stake, "VNA-Calibration and S-Parameter Characterization of Submillimeter Wave Integrated Membrane Circuits," 35th *International Conference on Infrared, Millimeter and Terahertz Wave (IRMMW)*, Rome, Italy, September, 2010.

[i] H. Zhao, A. Y. Tang, P. Sobis, V. Drakinskiy, T. Bryllert, and J. Stake, "340 GHz GaAs Monolithic Membrane Supported Schottky Diode Circuits," *Gigahertz Symposium*, Lund, Sweden, March, 2010.

[j] J. Stake, O. Habibpour, A. Y. Tang, H. Zhao, V. Drakinskiy, P. Sobis, J. Vukusic, and T. Bryllert, "Schottky Receivers and Graphene for Future THz Electronics," *International Symposium on Terahertz Science and Technology between Japan and Sweden*, Göteborg, Sweden, November, 2009.

[k] A. Y. Tang, V. Drakinskiy, P. Sobis, J. Vukusic, and J. Stake, "Modeling of GaAs Schottky Diodes for Terahertz Application," 34th *International Conference on Infrared, Millimeter and Terahertz Wave (IRMMW)*, Busan, Korea, September, 2009.

[l] J. Stake, Z. Herbert, A. Y. Tang, B. Banik, V. Drakinskiy, P. Sobis, J. Vukusic, S. Cherednichenko, A. Emrich, S. Rudner, T. Bryllert, and P. H. Siegel, "Terahertz Technology and Applications," *International Symposium on Terahertz Science and Technology between Japan and Sweden*, Tokyo, Japan, May, 2008.

List of notations

c_p	Specific heat capacity
f	Frequency
k_B	Boltzmann's constant
m^*	Effective mass
q	Elementary charge
$\overrightarrow{q}$	Heat flux
w_d	Depletion width
C	Electrical capacitance
C_{th}	Thermal capacitance
I	Current
L	Inductance
L_t	Current transfer length
L_M	Mixer/Multiplier conversion loss
N_d	Doping concentration
P	Power
R	Electrical resistance
R_{th}	Thermal resistance
S	Elastance
T	Temperature
V	Voltage
Z	Electrical impedance
Z_{th}	Thermal impedance
δ_S	Skin depth
η	Diode ideality factor
κ	Thermal conductivity
$\mu_n,\ \mu_p$	Drift mobility of electrons, holes
μ_0	Permeability in vacuum
ϕ_b	Barrier height
ψ_{bi}	Semiconductor built-in potential
ρ_m	Material density
ρ_c	Specific contact resistivity
σ	Electrical conductivity
τ_{th}	Thermal time-constant
$\upsilon_{e,sat}$	Electron velocity saturation
ε	Material permittivity

List of abbreviations

ADS	Advanced Design System
CVD	Chemical Vapour Deposition
DC	Direct Current
EM	Electromagnetic
FEM	Finite Element Method
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GHz	Gigahertz (10^9 Hz)
HB	Harmonic Balance
HBV	Heterostructure Barrier Varactor
HEB	Hot Electron Bolometer
HFSS	High Frequency Structure Simulator
IMPATT	IMPact ionization Avalanche Transit-Time
IR	Infrared
LO	Local Oscillator
PEC	Perfect Electric Conductor
RF	Radio Frequency
QCL	Quantum Cascade Laser
RF	Radio Frequency
SD	Schottky Diode
SDD	Symbolically Defined Device
Si	Silicon
SiO_2	Silicon Dioxide
SI	Semi-Insulating
SIS	Superconductor-Insulator-Superconductor
THz	Terahertz (10^{12} Hz)

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Chapter 1

Introduction

Terahertz (THz) spectrum is the electromagnetic spectrum sandwiched between the microwave and optical domains, i.e. 300 GHz ($\lambda = 1\ mm$; photon energy=1.2 meV) to 3 THz ($\lambda = 100\ \mu m$; photon energy=12.4 meV). For the last few decades, there has been an increasing interest in THz applications, such as communication, biology, imaging and general sensing, radio astronomy and earth science applications [1–3]. Among these multi-discipline applications, the primary driving force for the technology advancement is the strong need for THz heterodyne receivers [4] in radio astronomy and earth science applications. The success in building such receivers depends mainly on the receiver front-end performance.

In general, THz detection and generation can be realised by solid state electronic approach, by optical means or in a combination of both. At present, the ultimate low noise heterodyne detector technology is based on cryogenic devices, such as superconductor-insulator-superconductors (SISs) [5] and hot electron bolometers (HEBs) [6]. For THz generation, high output power sources are available through vacuum-tube technology, such as gyrotons, klystrons and backward wave oscillators (BWOs). Comparatively, low power sources are available through the solid state electronic technology, e.g. transistors amplifiers [7] and two-terminal devices oscillators, such as Gunn diodes and IMPATT diodes. The oscillator output can be further 'multiplied' to higher frequencies using heterostructure barrier diodes (HBVs) [8, 9] and Schottky diodes. In the optical domain, major effort has been devoted to develop sources using quantum cascade lasers (QCLs) [10, 11].

Despite the availability of the above mentioned technologies, there are still plenty of rooms for development towards small, compact or portable, and long operating lifetime type of detectors and sources. Cryogenic devices and vacuum-tube technology are bulky, large and/or expensive. In addition, the operation lifetime is limited. Considering either space-borne or commercial imaging applications, light weight and compact instruments are desired. Due to the practical demands on the packages, the solid state electronic technology has been positioned as a prevailing solution for THz detection and generation. In particular, the Schottky diode technology has been demonstrated to be a promising solution in building THz heterodyne receiver front-ends [4, 12–14].

Several missions, such as Odin, Earth Observing System(EOS) Microwave Limb Sounder (MLS) and Herschel Space Observatory (HSO), have been de-

ploying Schottky diode technology when building detectors as well as local oscillator (LO) chains to pump the detectors. Future planetary or atmospheric missions call for receiver front-end designs with higher frequency and output power. Progressing upward in frequency, the Schottky diode technology suffers from an increase in the mixer noise temperature as well as a decrease of the power conversion efficiency for both mixers and multipliers.

This research work is devoted to develop a better understanding of the planar Schottky diode operation in the THz frequency range. The goal of this work is to model the high frequency related diode behavior towards optimising the diode performance.

1.1 Background

Schottky diodes are semiconductor diodes based on a metal-semiconductor interface system. The earliest study on metal-semiconductor system was performed by Karl Ferdinand Braun back in 1874 [15]. However, the type of semiconductor diode used today is named after a German physicist, Walter H. Schottky (1886-1976). In 1937, Schottky showed that a potential barrier arises from stable space charges in the semiconductor alone without the presence of a chemical layer [16]. The potential barrier model is known as the Schottky barrier.

Since the introduction of Schottky diodes, they have been widely utilised for microwave applications such as radio-frequency detection. Dated back in 1904, Schottky diodes were used in the detection of electrical disturbance at millimetre waves by Jagadis C. Bose [17, 18]. Today, Schottky diodes are used as nonlinear devices for frequency conversions, which are key components in THz heterodyne receiver front-ends.

For many years, Gallium Arsenide (GaAs)-based whisker-contacted Schottky diodes have been used for millimetre and submillimetre wavelength heterodyne receivers. In this diode structure, the Schottky contact is formed by mechanically contacting an anode contact with a metal whisker probe, as shown in Fig. 1.1(a). This structure is inherently simple and it enables the fabrication of a very small area device with a low junction capacitance. In addition, the parasitic shunt capacitance in this structure is extremely low. In spite of the advantages of such a simple structure, the assembly and reliability of the whisker-contacted Schottky diode are of concern. In practice, multiple anode contacts are formed on the semiconductor to increase the probability for a proper whisker-anode contact. Attributed to a close packed array of Schottky anodes, diodes with such structure are also named as honeycomb diodes.

In 1987, a planar structure diode technology, as shown in Fig. 1.1(b), was introduced by William L. Bishop at University of Virginia [20]. Compared to the whisker-contacted diodes, the planar diodes offer ease of assembly and ruggedness. The introduction of planar structure Schottky diodes open the door for circuit integration towards building compact and low cost receivers. Fig. 1.2 shows examples of an antiparallel mixer diode and a multi-anode balanced multiplier diode chip. The realisation of these diode structures and several other circuit topologies would not be possible with the whisker-contacted diode. However, the disadvantage of the planar structure is the increase of the parasitic shunt capacitance and finger inductance which affect the diode performance at high frequency.

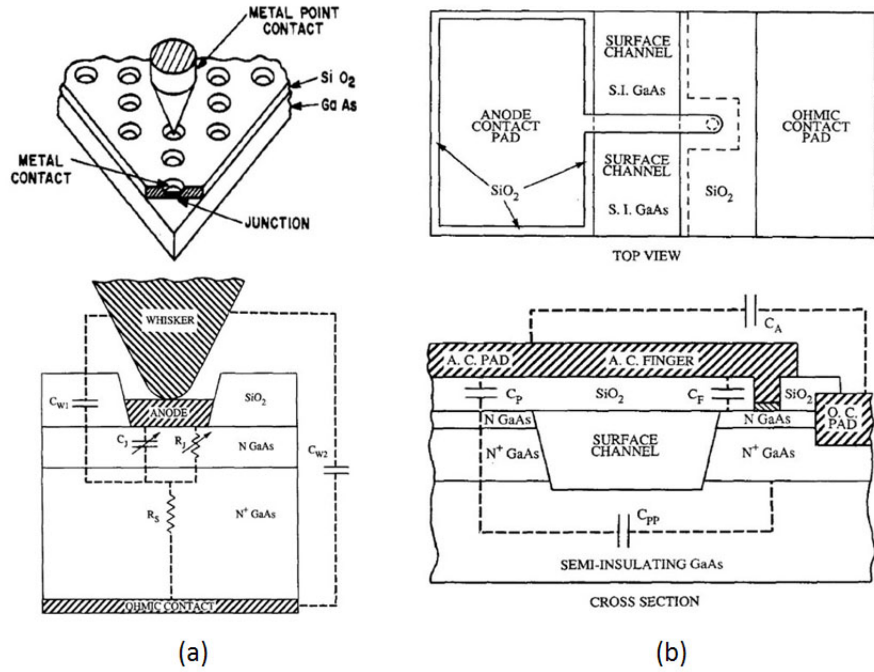

Fig. 1.1: (a)Honeycomb structure of whisker-contacted Schottky diode [19, 20]; (b) Planar Schottky diode structure [20].

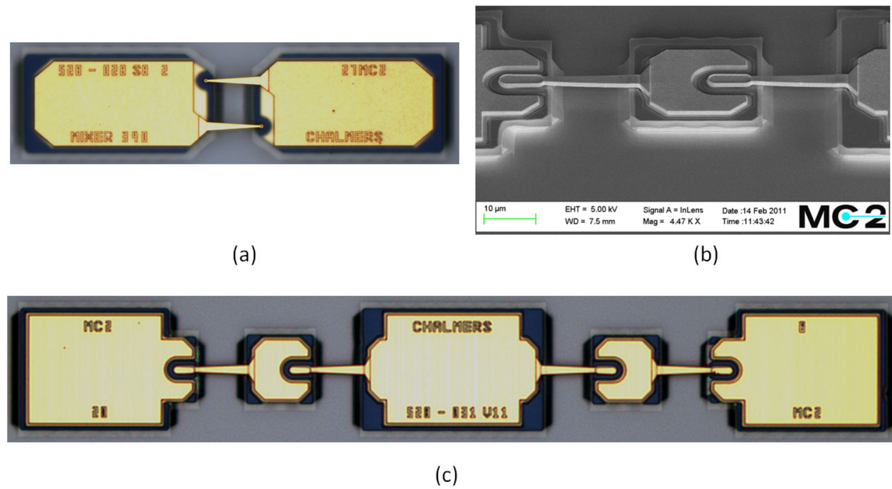

Fig. 1.2: (a) Discrete antiparallel mixer diode; (b) and (c) Multi-anode balanced frequency doubler chip.

Since the late 1990s, the planar Schottky diode technology has shown an extraordinary development. The technological development includes the diode device optimisation and diode-circuit integration. Thus, literature regarding

Schottky diode fabrication technology, device modelling and characterisation, as well as circuit integration techniques abound.

Thus far, Schottky diode based mixers and multipliers have been demonstrated up to a frequency of 2.7 THz [21–26]. A comparison of the Schottky diode performance with other technologies is shown in Fig. 1.3.

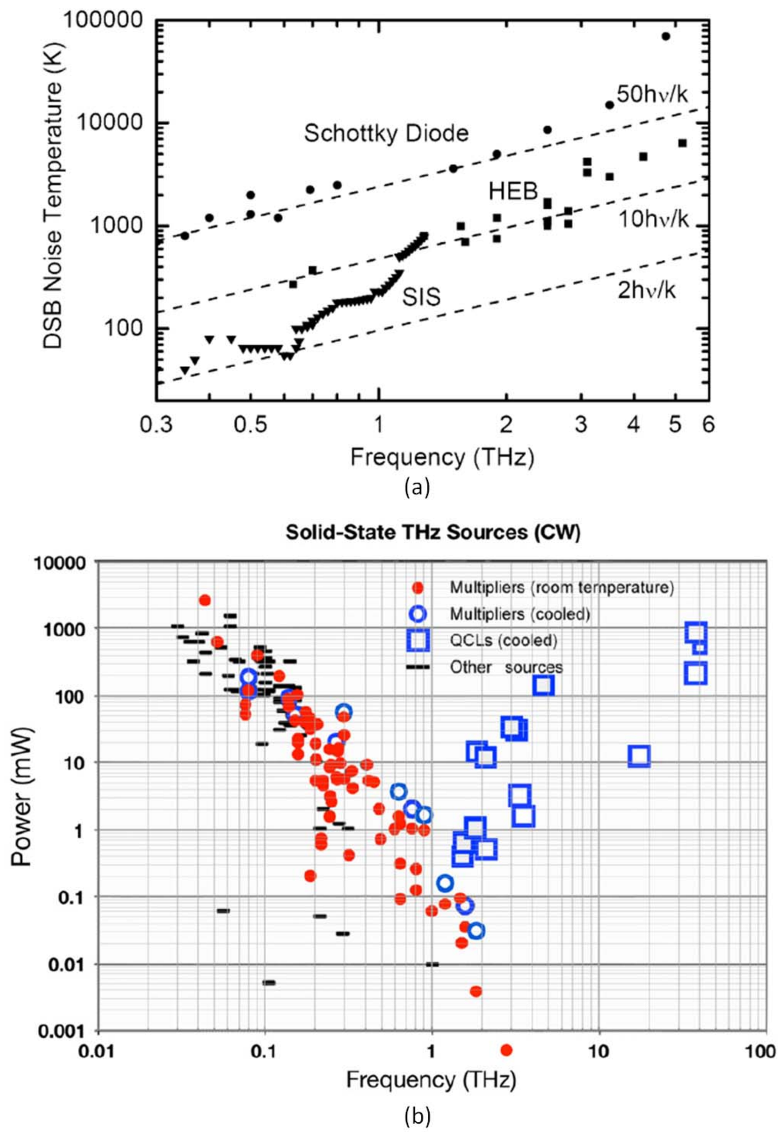

Fig. 1.3: (a) Mixer noise temperature [4] and (b) THz source output power [12] for heterodyne receivers.

1.2 Motivation and result

This research work is mainly motivated by the need for further optimisation of the diode performance in the THz frequency range. Despite the fact that the Schottky diode technology has been widely deployed in direct current (DC) and millimetre wave applications for decades, the state-of-the-art diode performance at submillimetre wave is still not fully understood. In view of this, a better understanding of the diode high frequency behavior is needed, in order to extend the current diode models and further optimise the diode performance.

In this work, the diode performance degradation due to frequency- and thermal- related phenomena are studied. The conventional lossless planar diode electromagnetic (EM) model has been extended to include the frequency-dependent losses of the series resistance. This work aids in the understanding of 'new' parasitic effect, i.e. eddy current, proximity and skin effects, influencing the high frequency losses for planar Schottky diodes (see Paper [A]).

From the thermal management perspective, a systematic analysis of the current state-of the-art multiplier thermal capability is performed. In addition, a self-consistent electro-thermal model is developed for multi-anode planar Schottky diode multipliers. This work leads to understanding of the thermal characteristic of the multiplier chip as well as opening opportunity for electrical circuit analysis to include the thermal effect (see Paper [B] and Paper [C]).

1.3 Thesis outline

This thesis presents the development work of planar Schottky diode modelling and optimisation for THz applications. In Chapter 1, the interest in THz applications and the related challenges are discussed. The background of the Schottky diode technology and the corresponding technology progress are then presented. Finally, the motivation for modelling planar Schottky diodes and the results from this work are briefly introduced.

Chapter 2 provides a general description of the planar Schottky diode for THz applications. This chapter begins with the basic diode operating principle, and further discusses the high frequency and high power related phenomena which result in diode performance degradation. Following this, issues specifically related to the planar diode structure are elaborated. Last but not least, the diode design and optimisation principles, for both mixer and multiplier applications, are presented at the end of the chapter.

Chapter 3 is concerned with the models and analysis methodologies developed/used in this work, whereas Chapter 4 presents the corresponding results. These two chapters provide a summary of the research work performed, including those presented in Paper [A] to Paper [C] and other unpublished work. Chapter 5 concludes the research work and discusses the future work.

Chapter 2

THz planar Schottky diodes

This chapter provides an overview of the Schottky diode operation, as well as the high frequency- and power- related behaviour. General physics of the metal-semiconductor interface, forming a Schottky barrier, and the corresponding diode circuit model are first presented. This is followed by a discussion focusing on the planar Schottky diode. Finally, the trade-offs between the diode geometry and the material parameters for circuit performance optimisation are discussed.

2.1 Overview of Schottky diode operation

The fundamental operation of a Schottky diode is attributed to charge transport mechanisms over a Schottky barrier, which is formed at a metal-semiconductor interface. For THz applications, n-doped GaAs is a typical semiconductor used in the metal-semiconductor system. Therefore, the foundation of Schottky diode operation in this thesis is built based on a metal and n-type GaAs semiconductor system, as shown in Fig. 2.1. The GaAs material data is listed in Table 2.1.

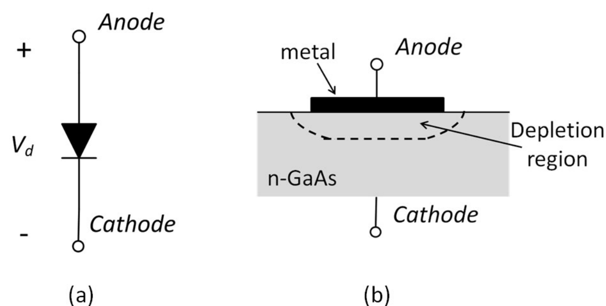

Fig. 2.1: (a) Symbol of a diode ; (b) Schematic of a metal-semiconductor interface.

Fig. 2.2 illustrates the formation of a Schottky barrier. For an ideal contact, a barrier height, ϕ_b, can be calculated as a difference between the metal work-function, ϕ_m, and the semiconductor electron-affinity, χ_s. In practice, the dependency of the barrier height on the metal work function is weak compared

Table 2.1: Material properties of Gallium Arsenide at room temperature.

Material Properties	Symbol	Value	Unit
Bandgap energy	E_g	1.42	eV
Relative dielectic constant	ε_r	12.9	-
Effective mass	(m^*/m_0)		
- electrons	m_e^*	0.063	-
- holes	m_{lh}^*	0.076	-
	m_{hh}^*	0.50	-
Drift mobilities (intrinsic)			
- electrons	μ_n	8000	$cm^2/V \cdot s$
- holes	μ_p	400	$cm^2/V \cdot s$
Saturation velocity	υ_{sat}	7×10^6	cm/s
Thermal conductivity	κ	50.6	$W/m \cdot K$
Specific heat	c_p	327	$J/kg \cdot^\circ C$
Density	ρ_m	5.317	g/cm^3

to the ideal case. Experimental characterisations showed that the metal-GaAs barrier height is approximately 0.8 eV, regardless of the metal contact work-function [27]. The nearly constant barrier height scenario is related to the imperfect metal-semiconductor interface, with the existence of the semiconductor surface states [28] and image-force lowering effect. Thus, the estimation of a practical barrier height, including the non-ideal interface phenomena, is rather complicated, as presented by Cowley and Sze [29].

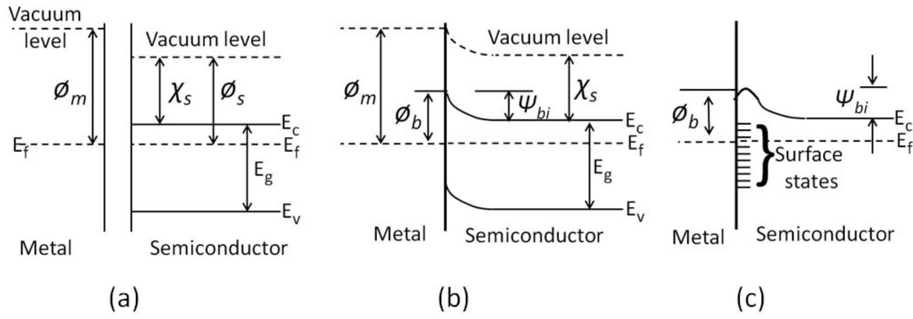

Fig. 2.2: Energy-band diagram of a metal-semiconductor system: (a)prior contact ; (b)ideal contact; (c) practical contact. E_f is the Fermi-energy level, E_g is the semiconductor bandgap energy, ϕ_s is the semiconductor work-function.

In thermal equilibrium, the semiconductor region beneath the metal contact is depleted of electrons. The electron transportation from the semiconductor to the metal contact is blocked by an energy barrier, known as the built-in potential, ψ_{bi} (see Fig. 2.2(c)). As shown in Fig. 2.3, both the depletion region and energy barrier can be modulated by altering the biasing condition.

Under a forward-biased condition, the built-in potential is lowered by a

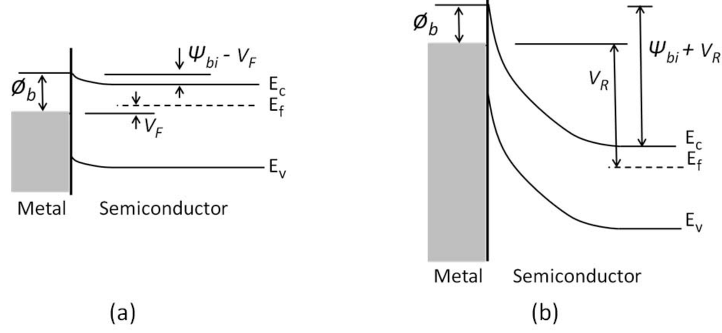

Fig. 2.3: Energy-band diagram for a metal-semiconductor system under (a) forward-biased condition ; (b) reverse-biased condition.

forward-biased voltage, V_F. In this case, the diode operates as a voltage-controlled resistor (i.e. a variable resistor or varistor). On the other hand, the depletion region, w_d, is modulated under a reverse-biased condition, where the depletion region is widened by an increase of a reverse-biased voltage, V_R. Thus, the diode operates as a voltage-controlled capacitor (i.e. a variable reactor or varactor). A typical Schottky diode circuit is modelled with a junction resistor, $R_j(V_j)$, a junction capacitor, $C_j(V_j)$, and a series resistor R_S, as shown in Fig. 2.4. The series resistor represents the total resistance from the undepleted semiconductor to the cathode ohmic-contact.

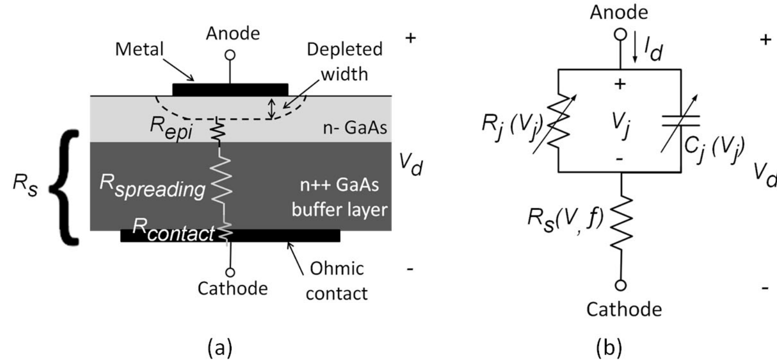

Fig. 2.4: A typical Schottky diode:(a) cross-section view; (b)equivalent circuit model.

2.1.1 Current-voltage characteristic

Under a forward-biased condition, the electron transport mechanisms across the metal-GaAs interface include the thermionic emission, recombination in the space charge region and recombination in the neutral region [30]. In addition, an electron transport mechanism in the opposite direction of the rectification process is the quantum-mechanical tunnelling. For a good metal-GaAs contact, the overall transport mechanism is dominated by the thermionic emission.

Hence, the current-voltage $(I - V)$ relation of a Schottky diode can be written as :

$$I_d(V_j, T) = I_S(e^{\frac{qV_j}{\eta k_B T}} - 1) \tag{2.1}$$

$$I_S(T) = AA^{**}T^2(e^{\frac{-q\phi_b}{k_B T}}), \tag{2.2}$$

where :
I_d = total diode current
I_S = reverse saturation current
V_j = junction voltage
q = elementary charge $(1.6 \times 10^{-19}C)$
η = ideality factor
A = junction area
A^{**} = effective Richardson constant
T = absolute temperature
ϕ_b = barrier height
k_B = Boltzmann's constant $(1.37 \times 10^{-23}J/K)$.

For a thermionic emission dominated electron transport mechanism, the ideality factor in the current-voltage relation is closed to unity. However, in practice, the ideality factor departs from unity due to the onset of the tunnelling current. The electron transport mechanism based on tunnelling is more pronounced at a lower temperature and a higher doping concentration, N_d. The effect of doping concentration and temperature on the ideality factor are formulated as (2.3) [31]:

$$\eta = (k_B T(\frac{tanh(\frac{E_{00}}{k_B T})}{E_{00}} - \frac{1}{2E_B}))^{-1} \tag{2.3}$$

$$E_{00} = 18.5 \times 10^{-12}\sqrt{\frac{N_d}{m_e^* \varepsilon_r}} \tag{2.4}$$

where E_B is the band bending $(\psi_{bi} - V_F)$, E_{00} is a material constant, m_e^* is the electron relative effective mass and ε_r is the semiconductor relative permittivity. For $k_B T >> E_{00}$, the overall electron transport mechanism is dominated by the thermionic emission.

For a reverse-biased condition, a region in the semiconductor is depleted of electrons and only occupied by the ionized donor charge. As the diode junction is further reverse-biased, the electric field across the junction is increased and the electron current conduction is decreased. Theoretically, at a limit of $V_j \to -\infty$, $I_d = -I_S$ where I_S is the saturation current.

However, in practice, a high reverse-bias voltage results in a high field across the junction, resulting in junction breakdown. The breakdown voltage, V_{bd}, can be estimated using (2.5) [32]:

$$V_{bd} = 60(\frac{E_g}{1.1eV})^{\frac{3}{2}}(\frac{N_{d,epi}}{10^{16}cm^{-3}})^{-\frac{3}{4}} \tag{2.5}$$

where $N_{d,epi}$ is the doping concentration in the epi-layer.

2.1.2 Capacitance-voltage characteristic

For a uniformly doped junction-layer, the junction charge function, $Q_j(V_j)$, and junction capacitance, $C_j(V_j)$, can be expressed as in (2.6) and (2.7), respectively.

$$Q_j(V_j) = -2C_{j0}\psi_{bi}\sqrt{1-\frac{V_j}{\psi_{bi}}} \tag{2.6}$$

$$C_j(V_j) = \frac{dQ_j(V_j)}{dV_j} = C_{j0}\sqrt{\frac{\psi_{bi}}{\psi_{bi}-V_j}} \tag{2.7}$$

where C_{j0} is the zero-biased junction capacitance.

In order to relate the junction capacitance to the diode geometry, the junction capacitance is modelled as a parallel plate capacitor. For a diode with an anode contact area of A, the junction capacitance can be calculated using (2.8). The second term in (2.8) is a first order edge fringing effect correction term for an anode contact with a diameter of D [33]. By solving (2.7) and (2.8), without considering the edge fringing correction term, the junction depletion width, $w_d(V_j)$, can be calculated as a function of the biasing voltage and doping concentration, as in (2.9).

$$C_j(V_j) = \frac{\varepsilon_s A}{w_d(V_j)} + \frac{3\varepsilon_s A}{D} \tag{2.8}$$

$$w_d(V_j) = \sqrt{\frac{2\varepsilon_s(\psi_{bi}-V_j)}{qN_{d,epi}}} \tag{2.9}$$

where ε_s is the semiconductor dielectric constant.

2.1.3 Series resistance

The diode series resistance is a non-trivial parasitic element where power is dissipated. Referring to Fig. 2.4, the series resistance of a diode is comprised of several components, as written in (2.10):

$$R_S(V_j,f) = R_{epi}(V_j,f) + R_{spreading}(f) + R_{contact}(f). \tag{2.10}$$

- *Junction epi-layer resistance, R_{epi}*

A junction epi-layer resistance, R_{epi}, is a resistance that arises due to the undepleted epi-layer. For a typical THz diode, the junction epi-layer thickness, t_{epi}, is within a range of tens to hundreds of nanometers. The electrical conductivity of this layer, σ_{epi}, is lower than that of the buffer-layer. Therefore, the current flowing through this layer is assumed to be concentrated under the anode contact. By assuming a negligible current spreading effect, the epi-layer resistance is approximated by (2.11):

$$R_{epi}(V_j) = \frac{t_{epi}-w_d(V_j)}{Aq\mu_{n,epi}N_{d,epi}} \tag{2.11}$$

where $\mu_{n,epi}$ is the electron mobility in the junction epi-layer.

For a forward-biased diode, the depletion width is assumed to be zero when calculating this resistance. On the other hand, the epi-layer can be fully depleted for a diode operating in a reverse-biased mode. Thus, a zero depletion width assumption results in an over-estimation of the epi-layer resistance, i.e. resembling the worst case scenario in term of loss. Alternately, the epi-layer resistance can be estimated using (2.12) for the reverse-biased case. In this calculation, a dynamic depletion width is considered [34].

$$R_{epi}(V_j) = R_{epi,min} + \frac{\varepsilon_s}{\sigma_{epi}}(S_{max} - S(V_j)) \tag{2.12}$$

$$S(V_j) = \frac{1}{C_j(V_j)} \tag{2.13}$$

where $R_{epi,min}$ and S_{max} are the minimum series resistance and maximum elastance, which are usually values at the breakdown voltage, respectively.

- *Buffer-layer spreading resistance,* $R_{spreading}$

A buffer-layer is a highly doped GaAs layer, i.e. with $N_{d,buf} > 10^{18}cm^{-3}$, which is used to facilitate the current flow from the epi-layer to the cathode ohmic contact. As a result of a higher buffer-layer conductivity and a larger ohmic contact area, the current is spreaded out in the buffer-layer. Due to the nature of current spreading, the calculation of the spreading resistance is inherently geometry-dependent. For a vertical diode with circular anode contact, the resistance can be estimated using (2.14) [35]:

$$R_{spreading} = \frac{1}{2Dq\mu_{n,buf}N_{d,buf}} \tag{2.14}$$

where $N_{d,buf}$ and $\mu_{n,buf}$ are the dopant concentration and electron mobility in the buffer-layer, respectively. The spreading resistance of a planar diode is more complicated due to the lateral current flow from the anode contact to the ohmic cathode contact (see Chapter 2.2.3).

- *Ohmic-contact resistance,* $R_{contact}$

A cathode ohmic-contact allows current flow between the semiconductor and the external circuit. For a vertical diode, the ohmic-contact resistance is a function of the ohmic-contact area, $A_{contact}$, and the technology-dependent specific contact resistivity, ρ_c, as in (2.15):

$$R_{contact} = \frac{\rho_c}{A_{contact}}. \tag{2.15}$$

For planar diode, the effective ohmic-contact area is characterised by the current transfer length, L_t [27]. To-date, typical ohmic-contact technologies for Schottky diodes are the Ni/Ge/Au [36] and Pd/Ge/Au [37, 38] metallisation systems. Contact technology based on these metallisation systems yields a low specific contact resistance, i.e. in the order of $10^{-6}\ \Omega \cdot cm^2$ or lower.

2.1.4 Noise properties

The noise properties of a Schottky diode are important for detection applications, where the diode operates as a varistor. As shown in Fig. 2.5, the Schottky

diode noise sources are modelled as a junction shot-noise and thermal-noises generated in the epi- and buffer-layer series resistances [35].

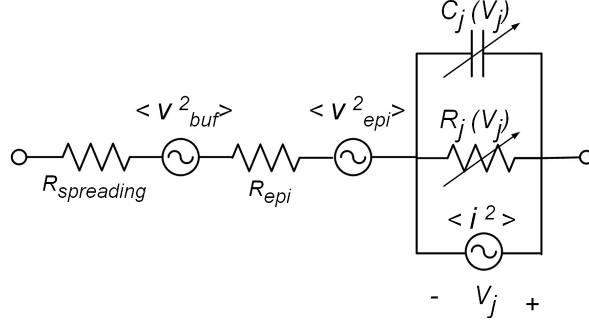

Fig. 2.5: The equivalent circuit of Schottky diode including noise sources.

For the diode noise analysis, the total diode impedance is treated as R_{total}, written as (2.16). The effect of junction capacitance is neglected since the displacement current is small compared to the conduction current. Therefore, the diode effective noise temperature, T_d, can be estimated using (2.17).

$$R_{total} = R_j + R_{epi} + R_{spreading} \tag{2.16}$$

$$T_d = \frac{\eta T}{2}(\frac{R_j}{R_{total}}) + T_{epi,eff}(\frac{R_{epi}}{R_{total}}) + T(\frac{R_{spreading}}{R_{total}}) \tag{2.17}$$

where $T_{epi,eff}$ is the effective temperature in the epi-layer.

At a low forward biased voltage, only the first term in (2.17) is important due to the high junction resistance. With an increase of the forward diode current, the thermal noise in the series resistance becomes significant. In addition, due to the high junction electric field at high biasing voltage, the electron distribution in the undepleted epi-layer is not at thermal equilibrium. Thus, the temperature of the heated electrons are approximated by an effective temperature, $T_{epi,eff}$, based upon an energy balance analysis proposed by H. Zirath [39].

2.1.5 Thermal properties

During normal diode operation, the heat generation occurs at the diode junction, elevating the local junction temperature. The generated heat is then dissipated from the top and the bottom of the junction, i.e. through the anode contact and the semiconductor, respectively. The temperature rise depends on the effectiveness of heat extraction from the junction through various cooling mechanisms, such as conduction, convection and radiation. For simplicity, it is assumed that the dominant cooling mechanism is thermal conduction, where the effect of other cooling mechanisms are assumed to be negligible. The conductive heat path is illustrated in Fig. 2.6.

By considering only the conduction cooling mechanism, the thermal problem can be analysed by solving the heat equation, expressed as (2.18):

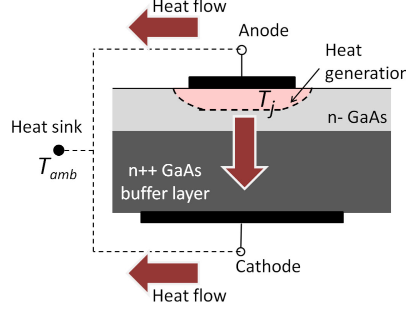

Fig. 2.6: The Schottky diode thermal conduction path.

$$\rho_m c_p(T)\frac{\partial T(x,y,z,t)}{\partial t} = \{\bigtriangledown\cdot[\kappa(T)\bigtriangledown T(x,y,z,t)]\} + g \tag{2.18}$$

where ρ_m is the material mass density, $c_p(T)$ is the material thermal capacity, $T(x,y,z,t)$ is the local temperature, $\kappa(T)$ is the material thermal conductivity and g is the heat generation rate per unit volume.

For a steady-state case, this equation is reduced to Fourier's heat law, as in (2.19):

$$\overrightarrow{q} = -\kappa(T)\overrightarrow{\bigtriangledown T} \tag{2.19}$$

where $\overrightarrow{q}$ is the heat flux, $\kappa(T)$ is the material thermal conductivity and $\overrightarrow{\bigtriangledown T}$ is the temperature gradient.

For a GaAs-based diode, the relatively poor material thermal conductivity is a concern, especially for high power diode design. The diode thermal conductivity and specific thermal capacity is a function of the temperature. The conductivity-temperature relation is approximated by (2.20) [40]:

$$\kappa_{GaAs}(T) = 50.6 \times (\frac{300}{T})^{1.28}\ [\frac{W}{mK}] \tag{2.20}$$

for $150\ K\ <\ T\ <\ 1500\ K$.

By using the interdisciplinary electrical analogy, a thermal model can be presented as a thermal network (see Fig. 2.7). The electro-thermal cross-discipline analogies are summarised in Table 2.2.

Table 2.2: Analogy between the electrical and the thermal disciplines.

Electrical current, I $[A]$	$\longleftrightarrow$	Heat rate, P $[W]$
Electrical potential, V $[V]$	$\longleftrightarrow$	Temperature, T $[K]$
Electrical resistance, R $[\Omega]$	$\longleftrightarrow$	Thermal resistance, R_{th} $[K/W]$
Electrical conductivity, σ $[S/m]$	$\longleftrightarrow$	Thermal conductivity, κ $[W/m\cdot K]$
Charge storage capacity, C $[F]$	$\longleftrightarrow$	Thermal heat capacity, C_{th} $[J/K]$

In this thermal network, the heat generation, P^{dis}, is represented as a current source. The effectiveness of the heat extraction from the junction is characterised by the thermal impedance, Z_{th}. The thermal impedance is represented

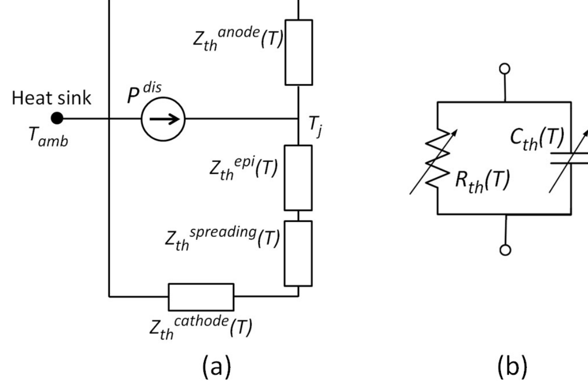

Fig. 2.7: The Schottky diode thermal model: (a) equivalent thermal network; (b) equivalent thermal impedance.

by a temperature-dependent thermal resistance, $R_{th}(T)$, and a temperature-dependent thermal capacitance, $C_{th}(T)$. The steady-state junction temperature can be calculated using (2.21):

$$T^j - T^{amb} = R_{th}(T) \times P^{dis}. \tag{2.21}$$

Similar to the electrical circuit analysis, the thermal transient response is characterised by an RC time-constant, τ_{th}.

2.1.6 High frequency and high power phenomena

The diode performance is degraded when the operating frequency or/and the operating power range is increased. To date, several phenomena resulting in the performance degradation have been identified as:

- frequency-dependent series resistance
- frequency- and/or power-dependent current saturation effect
- power-dependent diode operating temperature

- *Frequency-dependent series resistance*

For high frequency operation, the material frequency-dependent properties have significant influence on the diode performance. Studies show that an increase in the high frequency series resistance is related to the carrier-inertia, displacement current, and skin effect [41–43]. As a consequence, the low frequency series resistance model has to be expanded to a complex series impedance model, Z_S. Fig. 2.8 shows the transformation of the diode model from low to high frequency.

The high frequency series impedance can be written as (2.22) [42]:

$$Z_S = Z_{skin} + Z_{bulk} \tag{2.22}$$

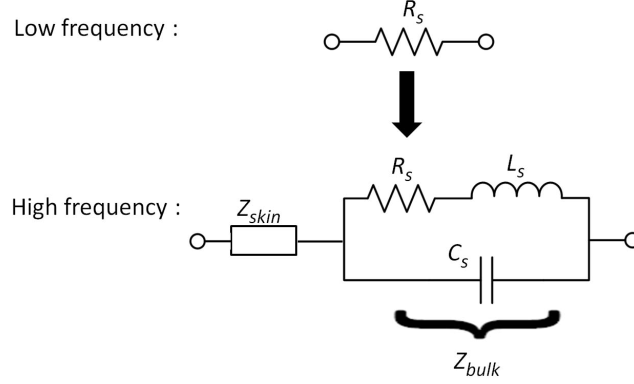

Fig. 2.8: Series resistance models for low frequency and high frequency regime.

where Z_{skin} is the skin-effect impedance and Z_{bulk} is the bulk material frequency-dependent impedance.

Referring to Fig. 2.8, the bulk series impedance comprises of a DC series resistance, an inertia inductance, L_S, and a displacement capacitance, C_S. The inertia inductance is related to the scattering frequency, f_s, whereas the displacement current is related to the dielectric relaxation frequency, f_d. These bulk material related frequencies and the classical plasma frequency, f_p, can be calculated using (2.23)-(2.25) [42].

$$f_s = \frac{1}{2\pi} \frac{q}{m_e^* \mu_n} \tag{2.23}$$

where m_e^* is the electron effective mass and μ_n is the electron mobility.

$$f_d = \frac{1}{2\pi} \frac{\sigma}{\varepsilon_s} \tag{2.24}$$

where σ is the electrical conductivity and ε_s is the semiconductor relative permittivity.

$$f_p = \sqrt{f_s f_d} \tag{2.25}$$

By using the empirical low-field mobility model by Sotoodeh et al. [44], the frequencies calculated using (2.23)-(2.25) for both the epi- and buffer-layer are summarised in Table 2.3.

Table 2.3: Calculation of bulk carrier scattering, dielectric relaxation and plasma frequency.

Layer	N_d (cm^{-3})	f_s (THz)	f_d (THz)	f_p (THz)
Epi-layer	5×10^{16} - 1×10^{18}	0.8 - 1.6	5.7 - 60	2 - 10
Buffer-layer	5×10^{18}	2.3	200	20

The skin effect arises due to the magnetic coupling within a conductor, i.e. the epi- and buffer-layer. The onset of the skin effect reduces the effective current flow cross-section to an average depth from the surface. The average

depth for current flow is known as the skin depth, δ_S. Considering an operating frequency that is far below the dielectric relaxation frequency, the skin depth can be estimated using a classical expression, as in (2.26):

$$\delta_S = \sqrt{\frac{2}{\omega \mu_0 \sigma}} \tag{2.26}$$

where μ_0 is the permeability of vacuum. For a case where significant displacement current exists, the skin depth has to be calculated from the real part of the propagation constant.

Taking these high frequency phenomena into consideration, the series impedence is inherently a complex function of device geometry, material conductivity, scattering frequency and dielectric relaxation frequency. An analytical expression of the spreading impedance for a bulk-type (vertical) diode can be found in [42].

- *Current saturation effect*

For a diode operation in varactor mode, the dominating current through the diode junction is the displacement current, $i_d(t)$. The displacement current is both frequency- and power- dependent, as written in (2.27):

$$i_d(t) = C_j(t)\frac{dV_j(t)}{dt}. \tag{2.27}$$

During normal diode operation, the displacement current in the junction must be matched to the electron conduction current, $i_e(t)$, in the undepleted epi-layer. However, the conduction current in the undepleted epi-layer is limited by the electron velocity saturation phenomena. As the displacement current is increased above the velocity saturation current, $i_{e,sat}$ as in (2.28), the limited conduction current could be modelled as an increase in the effective epi-layer series resistance [45]:

$$i_{e,sat} = AN_{d,epi}qv_{e,sat}. \tag{2.28}$$

- *Power-dependent diode operating temperature*

As a consequence of excess heat in the junction area, the diode electrical parameters, such as electron mobility, thermal voltage and thermionic emission carrier transport mechanism, are modified. The temperature-dependent electron mobility results in an increase in the series resistance, introducing additional losses. An empirical mobility model presented by Sotoodeh et. al [44] can be used to examine the temperature effect on the series resistance. The temperature dependencies of the diode thermal voltage and current are written as (2.29) and (2.30), respectively:

$$V_T(T) \propto T \tag{2.29}$$

$$I_d(T) \propto T^2\ exp(\frac{-\phi_b}{V_T})\ exp(\frac{V_j}{V_T}). \tag{2.30}$$

In addition to the performance degradation, thermal effects also influence the diode reliability as well as causing catastrophic issues, such as burn-out. Thus, the thermal management of a diode should be taken into consideration during the diode design. For instance, the maximum operating temperature should be maintained well below the failure mode temperature, e.g. 450 K.

2.2 Schottky diode with planar structure

At present, Schottky diode technology based on a planar structure has been well accepted as a promising solution for THz applications, compared to the whisker-contacted diode structure. Over the past several decades, tremendous progress has been made in bringing the diode performance using planar structures to be comparable to the performance of whisker-contacted diodes. In addition, the planar diode opens up the possibility of diode circuit integration. This enables the realisation of circuit topologies which would otherwise not be possible with the whisker-contacted diodes.

2.2.1 Physical structure of planar diodes

At the early stage of planar diode development, several possible planar configurations, i.e. mesa structure, proton bombarded diode and surface-channel diode, were investigated [20, 46]. The investigation led to a conclusion that the lowest possible parasitic capacitance can be achieved using the surface-channel type of planar diode. Therefore, the planar Schottky diode technology has been further developed and optimised based on the surface-channel planar configuration, as shown in Fig. 2.9.

The anode contact is formed by depositing a metal contact on the low-doped n-GaAs epi-layer. By etching through the epi-layer to the buffer-layer, the ohmic contact is formed at a distance of a few micrometres away from the anode contact. For diode to circuit connections, a narrow metal connection is formed across the surface-channel to route the Schottky anode path towards a large anode contact pad. This narrow metal connection is known as the air-bridge finger. The GaAs material beneath the air-bridge finger is removed in order to isolate the anode and cathode pads. The semi-insulating GaAs substrate serves as a supporting structure for the diode, whereas the silicon dioxide (SiO_2) or silicon nitride layer passivates the top semiconductor surfaces. Thus far, substantial literature on the planar diode fabrication technology is available [20, 21, 23, 24, 47–51].

2.2.2 Geometry-dependent parasitic model

The limitations on the planar diode frequency response and conversion loss are due to the power dissipation by the parasitics and the diode electromagnetic couplings. A typical diode parasitic model is shown in Fig. 2.10.

Losses due to joule heating are modelled as parasitic resistances. The parasitic series resistance of a planar diode is comprised of the air-bridge finger resistance, R_{finger}, epi-layer resistance, buffer-layer spreading resistance and the ohmic contact resistance, as stated in (2.31):

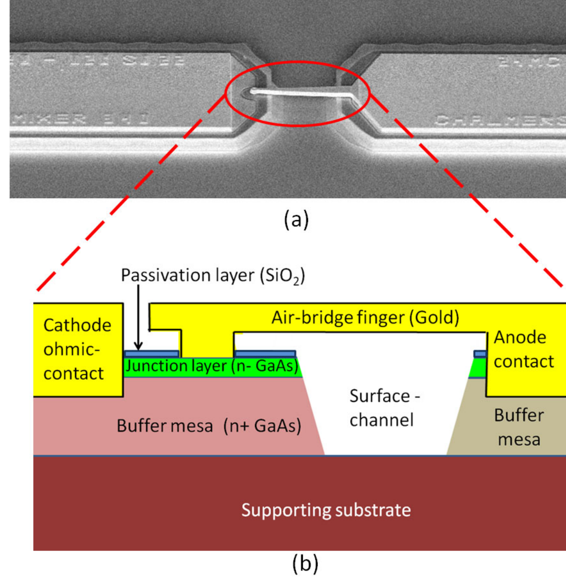

Fig. 2.9: (a) Scanning electron micrograph of a planar Schottky diode; (b) Schematic cross-section around the anode contact and surface-channel area. NB! The drawing is not to scale.

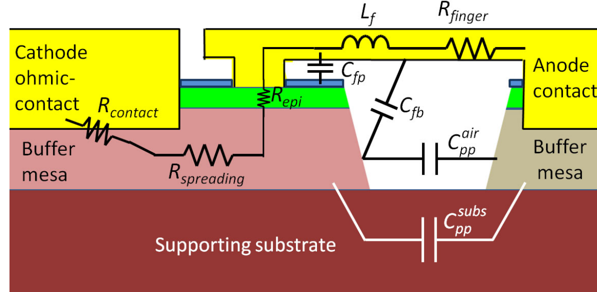

Fig. 2.10: Cross-section of planar Schottky diode indicating the diode parameters.

$$R_S(V_j, f) = R_{finger}(f) + R_{epi}(V_j, f) + R_{spreading}(f) + R_{contact}(f). \quad (2.31)$$

The electromagnetic coupling of the planar structure is modelled as capacitive and inductive parasitic elements [20, 25, 46, 52]. In general, only the parasitics at the close proximity to the air-channel and anode contact are considered in the modelling and optimisation work.

2.2.3 Lateral anode-cathode current flow

Due to the nature of the lateral current flow in a planar diode, and the less than 360 ° circumferential enclosure of the ohmic-contact around the anode

contact, the calculation of the spreading resistance in the buffer-layer is not straightforward. A 3D numerical approach is a common method for the DC spreading resistance estimation. In this method, the static form of current continuity equation, as in (2.32), is solved for the domain between the anode and cathode contacts.

$$\bigtriangledown \cdot \overrightarrow{J} = - \bigtriangledown \cdot (\sigma \bigtriangledown V) = 0 \tag{2.32}$$

where $\overrightarrow{J}$ is the current density.

The high frequency spreading resistance estimation is further complicated by the geometry-dependent current crowding effect, as addressed in Section 2.2.4.

The contact resistance of a planar diode depends on the current transfer length, ohmic contact size as well as the specific contact resistance. When progressing up in frequency, the overall diode geometry is reduced. Intuitively, the ohmic-contact resistance will increase as the contact area decreases. However, due to the skin effect at higher frequency, the current transfer length is shorter [53]. For ohmic-contact technology with a specific contact resistance of $1 \times 10^{-6}\ \Omega \cdot cm^2$ or lower, the relative increase of the contact resistance at high frequency is minimal. On the contrary, the consequence of minimising the contact area is more pronounced for contact resistance at lower frequency.

2.2.4 Current crowding effect

Current crowding phenomena, such as eddy current, skin effect and proximity effect, alter the current distribution within the conductors. At high frequency, losses due to current crowding phenomena result in an increase of the series resistance above the DC value. In general, the frequency dependency of the power losses due to skin and eddy current are stated in (2.33) and (2.34), respectively:

$$P_{loss}^{skin} \propto \sqrt{f} \tag{2.33}$$

$$P_{loss}^{eddy} \propto f^2. \tag{2.34}$$

On the other hand, a general mathematical expression to represent the high frequency proximity loss is rather complex.

Among the series resistance components in (2.31), the air-bridge finger resistance, R_{finger}, at DC is generally small and negligible due to the high electrical conductivity of gold ($\sigma_{gold} = 45.6 \times 10^6\ S/m$). At higher frequencies, the effective cross-section for current flow is reduced, resulting in an increase in the series resistance. For the air-bridge finger above the surface-channel, the skin-effect is the dominating loss mechanism, and the classical skin depth is calculated using (2.26). For example, the skin depth in the gold conductor is 0.13 μm at 340 GHz.

For the air-bridge finger at the close proximity of the mesa, the calculation of resistance is more complicated due to the onset of the proximity effect [54]. The magnetic coupling between the air-bridge finger and the buffer mesa introduces power loss due to a mixture of eddy current and proximity effect. For a typical buffer-layer thickness of planar diode, the frequency dependent resistance can be written as (2.35) [55](see Paper [A]):

$$R_{spreading}(f) = R_{DC}(1 + k(\frac{f}{f_{crit1}})^2 + k(\frac{f}{f_{crit2}})^4) \tag{2.35}$$

where k is set to 0.1.

In this resistance model, the f^2 and f^4 frequency dependencies are used to represent the loss mechanism related to eddy current and a mixture of skin and proximity effect, respectively. The f_{crit1} and f_{crit2} are the critical frequencies related to the eddy current and a mixture of skin and proximity loss mechanisms. These critical frequencies are defined as the frequencies when the corresponding loss mechanism contributes 10 %, i.e. $k = 0.1$, of the overall loss.

2.2.5 Parasitic capacitance and inductance

The parasitic capacitor and inductor representing the electromagnetic couplings are material- and geometry-dependent. The fringing field between the anode and cathode contact pad is represented by the pad-to-pad capacitor, C_{pp}, as written in(2.36):

$$C_{pp} = C_{pp}^{air} + C_{pp}^{subs}. \tag{2.36}$$

Since the pad-to-pad coupling goes through both the air-channel and substrate, the pad-to-pad capacitance is dependent on the distance between pads, height of the mesa, as well as the thickness and permittivity of the substrate.

On the other hand, the electrical coupling between the air-bridge finger to the top of the mesa is modelled as the finger-to-pad capacitance, C_{fp}, whereas the air-bridge finger to the buffer coupling is represented as the finger-to-buffer capacitance, C_{fb}. In this case, these parasitic capacitances are dependent on the gap between the air-bridge finger and the top of the mesa.

Generally, the total parasitic capacitance, C_p^{total}, of a planar diode is calculated as a sum of all the parasitic capacitance, as in (2.37):

$$C_p^{total} = C_{pp} + C_{fp} + C_{fb}. \tag{2.37}$$

From the magnetic coupling perspective, an air-bridge finger inductance, L_f, is used to model the self-inductive current in the air-bridge finger. On the other hand, there is a possibility of the onset of skin and proximity effect due to the magnetic coupling between the air-bridge finger and the buffer mesa. For anti-parallel diodes, the magnetic coupling between both air-bridge fingers are modelled as mutual inductors.

From the topology point of view, the parasitic capacitances are placed in parallel to and the parasitic inductance is placed in series with the diode junction intrinsic resistance and capacitance. Thus, at high frequency, the parasitic capacitances resembles a low impedance path between both pads, whereas the parasitic inductance resembles a high impedance path in series with the diode junction. As a result, the power coupling capability to the diode junction is reduced, degrading the overall diode performance. Thus, there is inherently a limitation of the bandwidth for power coupling to such a complex diode load [56–58].

2.3 Diode design and optimisation

The performance of mixer and multiplier circuits depends greatly on the diode device properties. Therefore, it is crucial to identify the figures of merits and possible diode parameters to be optimised. A general understanding of trade-offs between the diode parameters and the effect on the performance are essential in designing a high performance diode.

2.3.1 Mixer diode

The efficiency of a resistive mixer is characterised by the conversion loss, L_M, as defined in (2.38):

$$L_M = \frac{P_{RF,in}}{P_{IF,out}} \tag{2.38}$$

where $P_{RF,in}$ and $P_{IF,out}$ are the input power at RF frequency and output power at IF frequency, respectively.

In an ideal case, the theoretical conversion loss is 3.9 dB [59–61]. However, in practice, the conversion performance is degraded by the parasitic series resistance, return losses and losses in the matching circuit.

Another figure of merit for the mixer circuit is the receiver noise temperature, T_R. The receiver noise temperature is related directly to the diode mixer noise temperature, T_M. Moreover, the receiver noise temperature is degraded by an increase of the diode conversion loss. Thus, in order to optimise the receiver noise temperature, it is important to reduce the mixer conversion loss.

$$T_R = T_M + L_M T_{LNA} \tag{2.39}$$

The diode cut-off frequency, f_c, is a figure of merit describing the upper limit of the diode frequency response. As written in (2.40), this figure of merit is related to the parasitic series resistance, R_S, and total capacitance, C_{tot}. The diode cut-off frequency is usually calculated from DC or low-frequency measurements of the diode's characteristic. As a rule of thumb for a mixer diode design, the mixer cut-off frequency should be at least 10 times higher than the operating frequency [62].

$$f_c = \frac{1}{2\pi R_S C_{tot}} \tag{2.40}$$

$$C_{tot} = C_{j0} + C_p^{total} \tag{2.41}$$

Due to a trade-off between the junction capacitance and series resistance, the choice of anode area is difficult. In general, the capacitance range is chosen with circuit matching limitations.

Instead of adjusting the anode contact size, minimisation of the series resistance can also be accomplished by increasing the epi-layer doping concentration. However, a higher doping concentration in the epi-layer results in a higher tunnelling current, i.e. an increase in the diode ideality factor. The relationship between ideality factor and the doping concentration is stated as (2.3).

For a typical mixer diode design, the ideality factor of 1.2 or lower is desired. A high ideality factor increases the conversion loss, as well as the diode shot

noise. On the contrary, an increase in the doping concentration mitigates the hot-electron noise [63].

Finally, the epi-layer thickness is then calculated as the zero-biased depleted width for a desired doping concentration, using (2.9).

2.3.2 Multiplier diode

In frequency multiplication applications, the diode can be used as either a varactor(reactance) multiplier [34, 64] or a varistor(resistive) multiplier [64, 65]. The conversion loss of a multiplier circuit is calculated as (2.42):

$$L_M = \frac{P_{RF,in}}{P_{n\times RF,out}}. \tag{2.42}$$

where $P_{RF,in}$ and $P_{n\times RF,out}$ are the input power and output power, respectively.

According to Manley-Rowe equations [66], an ideal reactance multiplier is capable of achieving a 100% conversion efficiency. In reality, varactor multiplier performance is still far below the theoretical limits. This is attributed to the onset of resistive multiplication in a reactance multiplier circuit, where the diode is forward-biased for a fraction of the operation cycle. For an nth order resistive multiplier, the best achievable conversion efficiency is $1/n^2$ [65]. Thus, the varactor multiplier performance is further degraded by the losses in partial resistive mixing during frequency conversion. In addition, the conversion performance degradation of a varactor multiplier is also caused by the similar loss factors as in the mixer circuit.

The electron velocity saturation phenomena, as discussed in Chapter 2.1.6, is also an important limiting factor for the conversion loss. Thus, for a specific operating frequency, there is a maximum epi-layer thickness, $t_{epi,max}$. Analytical expression of the maximum epi-layer thickness is formulated as (2.43) [67] or (2.44) [68]:

$$t_{epi,max} \approx \frac{\upsilon_{sat}}{2f_{out}} \tag{2.43}$$

$$t_{epi,max} \approx \frac{\upsilon_{sat}}{2\pi f_p}. \tag{2.44}$$

where υ_{sat} is the estimated electron saturation velocity, f_{out} is the output frequency and f_p is the pumping RF frequency.

Another boundary condition in the diode design is the doping concentration dependent breakdown voltage, as described in (2.5). For a highly doped epi-layer, it is possible that an avalanche breakdown occurs prior to a full depletion of the epi-layer, reducing the dynamic cut-off frequency. Thus, for a desired epi-layer thickness and breakdown voltage, the doping concentration range can be estimated using (2.45):

$$t_{epi,bd} = \sqrt{\frac{2\varepsilon_{s,epi}}{qN_{d,epi}}(\psi_{bi} + V_{bd})}. \tag{2.45}$$

The frequency response of a multiplier is characterised by the dynamic cut-off frequency, f_{cd}. Contrary to the mixer diode, the capacitance swing from C_{min}

to C_{max} instead of the total capacitance is taken into consideration for the cut-off frequency estimation. The possible capacitance swing region is dependent on the diode breakdown voltage.

$$f_{cd} = \frac{1}{2\pi R_S}(S_{max} - S_{min}) \tag{2.46}$$

Therefore, for multiplier circuit optimsation, a diode with a high breakdown voltage, low series resistance and low parasitic capacitance is desired.

Chapter 3

Modelling and analysis methodology

This chapter is concerned with the models and analysis approach for optimisations of planar Schottky diodes. Models developed to study the high frequency and high power phenomena in diode operation are described. The analysis results are discussed in Chapter 4.

3.1 Geometry-dependent parasitic model

For practical diode-circuit operation, diodes are connected to external circuitries. This further limits the diode performance due to the parasitics, especially at a higher operating frequency. The parasitics will result in power loss and affect the input power coupling to the non-linear diode junction for power conversion. The objective of this parasitic analysis model is to investigate influences of the electromagnetic couplings on planar diode performance. In view of this, only the linear behaviours of the diode are taken into account, while the non-linear diode junction properties are disregarded. For high frequency power loss analysis, the epi-layer is not included in the EM analysis. Meanwhile, the diode junction is modelled as a 50 Ω lumped-port for the parasitic capacitance and inductance analysis.

3.1.1 High frequency power loss

The high frequency geometry-dependent parasitics model developed is based on a combination of 3D full wave EM analysis and lumped-equivalent circuit parameter extraction approach. In this work, the High Frequency Structure Simulator (HFSS) [69] is used for EM analysis, whereas the Agilent Advanced Design System (ADS) [70] is used for the parasitic element extraction. The frequency range investigated using this setup is 150 GHz to 600 GHz.

In the EM simulator, the diode structure of interest is placed in an air-channel, as shown in Fig. 3.1. In this setup, the two ends of the diode pads are extended towards two wave-ports. Coaxial modes are excited at both wave-ports where the outer wall of the air-channel acts as a ground plane. Due to the geometrical symmetry property, only half of the diode structure is simulated,

where a magnetic wall is inserted at the symmetry plane. Within the air-channel, the 3D full wave equation, as in (3.1), is solved using the finite-element-method (FEM).

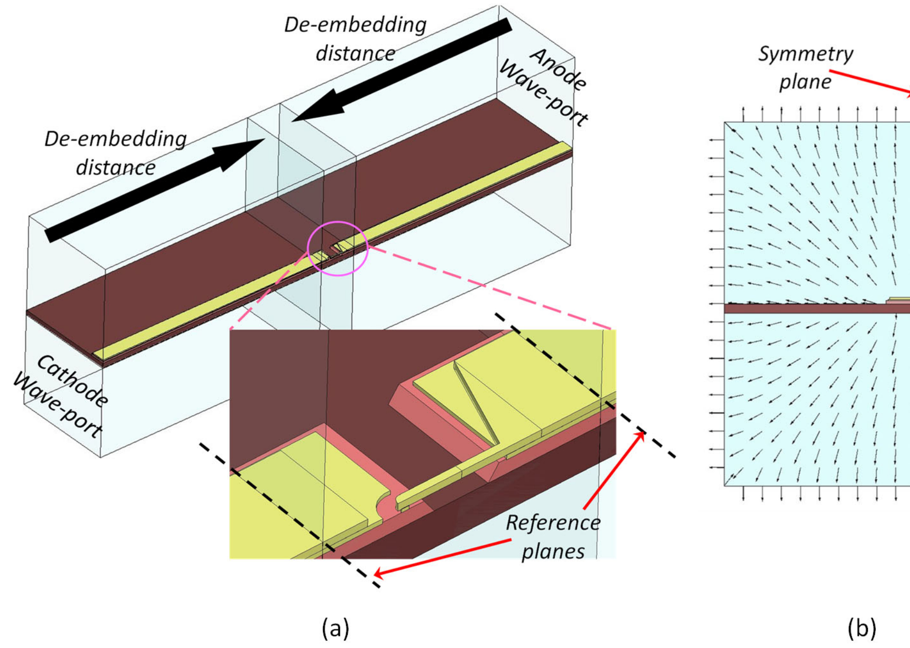

Fig. 3.1: (a) EM simulation setup; (b) Coaxial excitation mode at the wave-port.

$$\triangledown \times \left(\frac{-1}{j\omega\mu_0} \triangledown \times \overrightarrow{E}\right) = (\sigma + j\omega\varepsilon)\overrightarrow{E} \tag{3.1}$$

The EM solution, de-embedded from both the wave-ports up until the diode surface-channel reference planes, is then extracted in a measure of scattering parameters (S-parameters). The S-parameters are then transferred to a microwave circuit simulator for parasitic element extraction.

For this analysis, a total of 3 cases are simulated for each geometry variation, i.e. lossless open-circuited diode, lossless short-circuited diode and lossy cathode buffer mesa for short-circuited diode. For lossless analysis, all the electric conductors, i.e. air-bridge finger, ohmic-contact mesas, and ohmic pads, are assumed to be perfect electric conductors (PECs) in the EM simulation. On the other hand, for the lossy case, conductive loss in the cathode buffer mesa is included in the EM simulation.

The short-circuited and open-circuited diode for lossless case are used to extract the parasitic capacitance and inductance. The parasitic elements are extracted via a combination of direct extaction and least square error fitting. The extracted parasitic elements are then entered to the lumped-equivalent circuit in the lossy case, where the spreading resistance is extracted via the least square error fit method. The simulated diode configurations and the corresponding lumped-equivalent circuits are shown in Fig. 3.2.

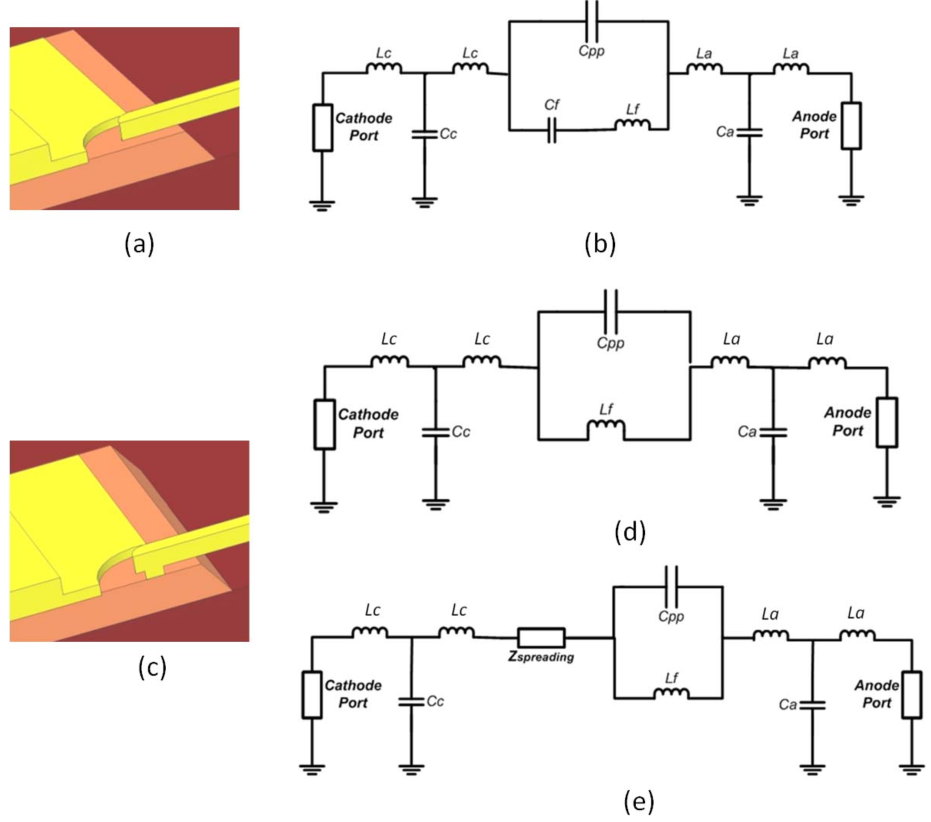

Fig. 3.2: Open-circuited diode case: (a) EM simulation structure; (b) Lumped-equivalent circuit. Short-circuited diode case: (c) EM simulation structure; (d) Lumped-equivalent circuit for lossless analysis; (e) Lumped-equivalent circuit for lossy analysis (Paper [A]) [55].

Details of the geometry variations, EM simulation setup and the parasitic parameter extraction procedure are explained in Paper [A].

3.1.2 Parasitic capacitance and inductance

For the parasitic capacitance and inductance analysis, a similar approach as in the high frequency loss analysis (see Section 3.1.1) is used. However, for this analysis, all the conductors are assumed to be perfect electric conductor, i.e. without conductive losses.

In the EM simulation, the non-linear diode junction can be modelled as a coaxial port [52] or a lossy capacitor [71]. In this thesis, the diode junction is modelled as a 50 Ω electrical lumped port. The lumped equivalent circuit, including the diode junction port, is shown in Fig. 3.3.

The relationship of the parasitic elements with the distance of cathode and anode buffer mesas, d_{pp}, is studied, by fitting the extracted result to equations (3.2) and (3.3):

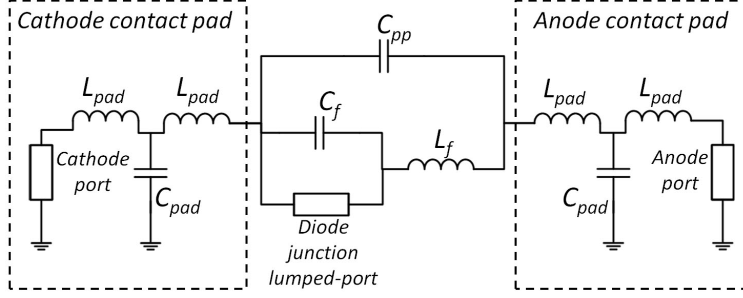

Fig. 3.3: The lumped equivalent circuit for a planar diode.

$$L_f(d_{pp}) = L_{fd}\ d_{pp} + L_{f0} \tag{3.2}$$

where L_{fd} and L_{f0} are the coefficients for curve-fittings,

$$C_{pp}(d_{pp}) = C_{ppd}\ d_{pp}^{n} \tag{3.3}$$

where C_{ppd} and n are the coefficients for curve-fittings.

The influence of the parasitic elements on diode performance are further analysed by evaluating the resonance frequencies of diode input impedance. The equivalent circuit of a single diode loaded with parasitics is shown in Fig. 3.4. The diode impedance, Z_{in}, is calculated using (3.4).

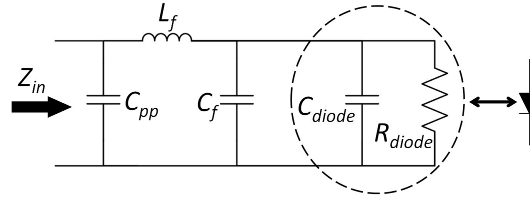

Fig. 3.4: Equivalent circuit used to define the input impedance.

$$Z_{in} = \frac{s^2(L_f C_f^d R_{diode}) + sL_f + R_{diode}}{s^3(L_f C_f^d C_{pp} R_{diode}) + s^2(C_{pp} L_f) + s(R_{diode}(C_f^d + C_{pp})) + 1} \tag{3.4}$$

$$C_f^d = C_f + C_{diode} \tag{3.5}$$

$$s = j2\pi f \tag{3.6}$$

3.2 Multiplier chip thermal analysis

The effect of diode thermal properties on the diode electrical performance is crucial for high power applications. Thus, in this work, a systematic thermal

analysis is performed on a 6-anode 200 GHz multiplier chip. In the analysis, the transient and steady-state thermal solutions are acquired through 3D FEM calculations using Ansys Mechanical Thermal Simulator [72]. The top view of the 200 GHz multiplier chip and the corresponding simulation domains are illustrated in Fig. 3.5.

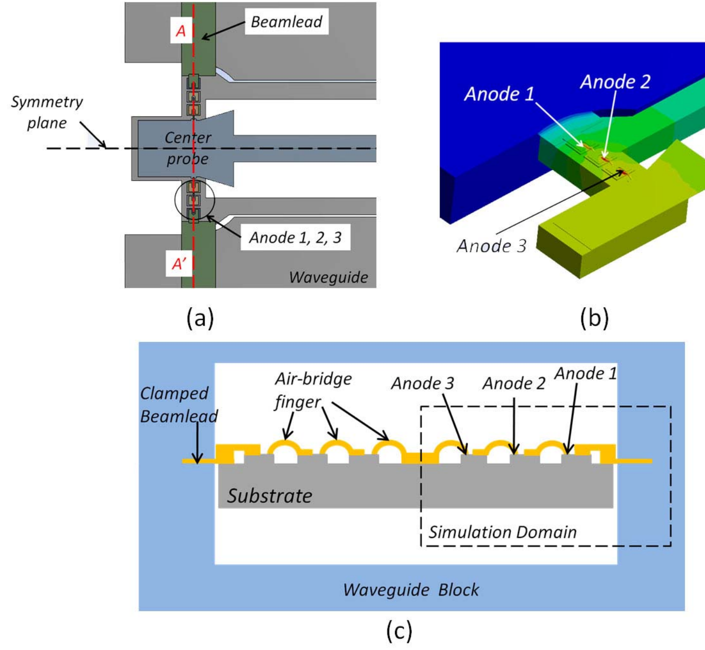

Fig. 3.5: Schematic of a frequency doubler chip: (a) top view; (b) simulated 3D geometry; (c) A-A' cross-section view (Paper [B]).

The heat extraction mechanism considered in this numerical analysis is heat conduction. Other mechanisms such as radiation and convection, are assumed to be negligible. In addition, the potential uneven heat flux distribution within the geometry due to high frequency current crowding effects are not taken into consideration. Thus, the effective heat path is equivalent to the physical geometry of the chip.

Since the objective of this work is to optimise the diode operation at room temperature, the temperature of interest is limited within a range of 300 K to 500 K . Other temperature ranges can be analysed using this approach, provided the material thermal properties are available for the specific temperature range. The transient and steady-state temperature profile of the chip is solved using (2.18) and (2.19), respectively.

Within the temperature range of interest, the temperature-dependency of the specific thermal capacity for GaAs is weak, i.e. from 327 $mJ/g \cdot K$ at 300 K to 343 $mJ/g \cdot K$ at 500 K [73]. On the other hand, the thermal conductivities for GaAs, GaN and Si exhibit a stronger temperature dependencies, as stated in the (2.20), (3.7) and (3.8) [40], respectively:

$$\kappa_{GaN}(T) = 157 \times (\frac{300}{T})^{1.9} \; [\frac{W}{mK}], \tag{3.7}$$

for 120 $K < T < 320$ K.

$$\kappa_{Si}(T) = 160 \times (\frac{300}{T})^{1.5} \; [\frac{W}{mK}] \tag{3.8}$$

for 30 $K < T < 800$ K.

Hot spots and thermal constraints in the multiplier chip are identified and the power capability of the current multiplier chip is studied. Several possible approaches to improve the chip thermal management, such as attaching heat spreading and changing chip geometries, have been investigated. In addition to the conventional GaAs material, thermal performance of a multiplier based on GaN diodes and silicon substrate have also been investigated for the same circuit topology. The simulated result has been verified through experimental measurement, using a QFI infrared microscope (InfrasScope^{TM}) [74].

Details of the simulation and measurement setup are provided in Paper [B].

3.3 Self-consistent electro-thermal model

In order to provide quantitative estimates of the trade-offs between thermal and electrical design, a self-consistent electro-thermal diode model is developed. For electro-thermal coupling, the instantaneous electrical power, i.e. $I(t)V(t)$, serves as a heat source for calculating the junction temperature in the thermal model. The diode junction temperature and the corresponding temperature-dependent electrical parameters are updated consistently. A schematic of the electro-thermal coupling is shown in Fig. 3.6.

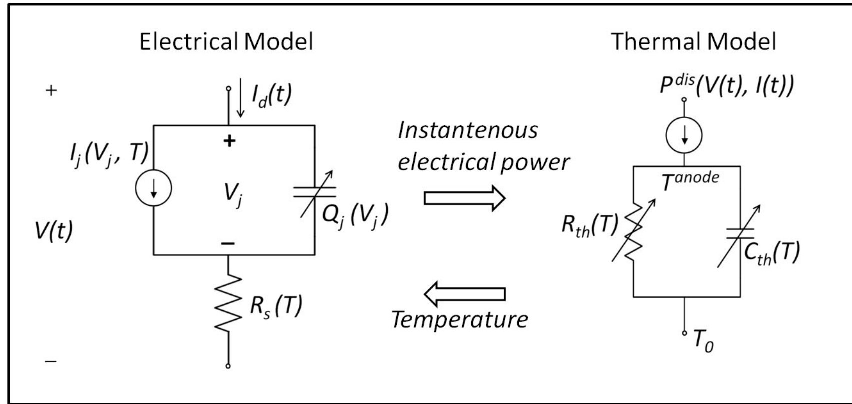

Fig. 3.6: Schematic of the self-consistent electro-thermal model.

For this study, the electrical model is built based on the full diode model, with capacitance and resistance, provided in Agilent ADS Symbolically Defined Device (SDD) [70]. In this diode model, The diode current-voltage characteristic is modelled as in (2.1). The reverse-biased junction charge and capacitance are calculated using (2.6) and (2.7). The forward-biased junction capacitance is modelled as a linear extension of the reverse biased capacitance. This linearly extended forward-biased capacitance has a slope of reverse junction capacitance at $V = \alpha\psi_{bi}$, where α is known as the forward-biased depletion coefficient.

The thermal model is developed using the electrical analogy approach, as described in Chapter 2.1.5. For the multi-anode multiplier chip, the diode junction temperatures are calculated using a thermal resistance matrix approach, which is similar to the approach used for the multi-finger transistor thermal analysis [75]. In addition, the temperature-dependent material thermal conductivity is taken into consideration, by using linear temperature approximation of thermal resistance [75, 76]. The thermal resistance matrix is extracted from 3D FEM thermal simulations.

Details of the model formulation are described in Paper [C].

Chapter 4

Results and discussions

This chapter discusses the results of the THz planar diode optimisation using the models and analysis methods presented in Chapter 3.

4.1 Diode surface-channel geometry optimisation

In order to optimise the diode performance, the diode parasitics have to be minimised. Thus, influences of the diode geometry on the parasitic resistance and reactance are investigated.

4.1.1 Effect of current crowding phenomena on power loss

By using the high frequency power loss model described in Chapter 3.1.1, the frequency-dependent losses in the ohmic-contact buffer mesa are investigated. In this analysis, the parasitic spreading resistance in the ohmic-contact buffer mesa is studied as a function of the buffer-layer thickness, b_z, and shapes of the mesa isolation wall. The analysed geometry parameters are listed in Table 4.1 and the shapes of mesa isolation wall are illustrated in Fig. 4.1.

Table 4.1: List of the analysed diode geometry.

Geometry parameter	Symbol	Variation
Buffer-layer thickness	b_z	0.5, 1, 2, 4 & 6 μm
Shape of mesa isolation wall		slanted, straight

Fig. 4.2 shows the extracted spreading resistance for diodes with slanted mesa wall. The analysis shows that the diode spreading resistance increases dramatically above DC resistance values as the operating frequency increases.

In conventional diode resistance model, the only frequency-dependent loss mechanism considered in the ohmic contact mesa is the skin effect. However, the extracted spreading resistances do not exhibit a square-root frequency dependency. According to the classical skin depth calculation, the skin depth for a highly doped buffer-layer is approximately 1.8 μm at 600 GHz. For a typical buffer-layer thickness of 0.5 *to* 2 μm, the physical thickness of the buffer-layer

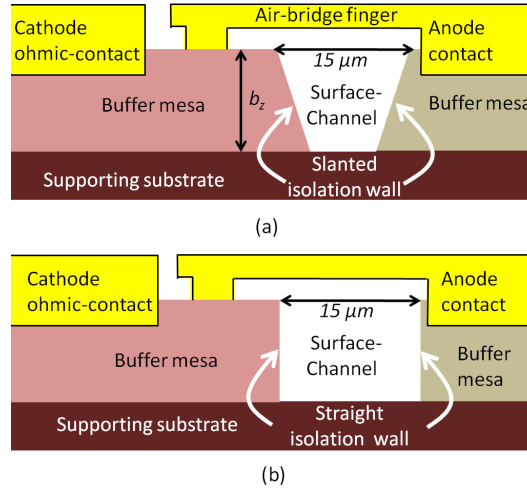

Fig. 4.1: Shape of the mesa isolation wall: (a) Slanted; (b) Straight.

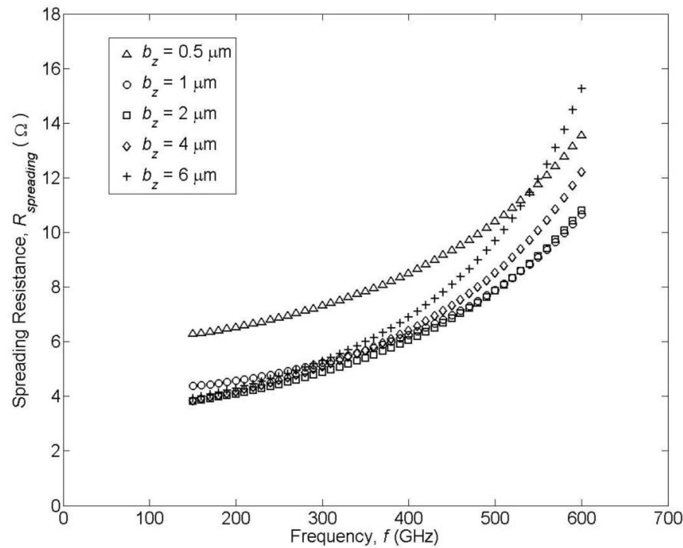

Fig. 4.2: Extracted effective spreading resistance as a function of frequency for slanted mesa wall diodes.

is less than or approximately one skin depth up to a frequency of 600 GHz. In this case, the skin effect is not the dominating loss mechanism.

By further analysing the EM field within and surrounding the buffer mesa, it is found that the high frequency losses are attributed to eddy current and current crowding effect. The time-varying electrical current in the air-bridge finger induces a time-varying magnetic field within and surrounding the air-bridge finger. The generated magnetic field is then coupled to the buffer mesa, which is located in a close proximity to the air-bridge finger. As a consequence,

eddy current is generated within the buffer mesa. The generation of eddy current can be explained by Faraday's Law, as stated in (4.1):

$$\nabla \times \overrightarrow{E} = -\frac{\partial \overrightarrow{B}}{\partial t} \tag{4.1}$$

where $\overrightarrow{B}$ is the magnetic flux density.

Due to the close proximity between the air-bridge finger and the buffer mesa, the eddy current, skin and proximity effect are the important loss mechanisms within the buffer mesa. The effective spreading resistance is then formulated as (2.35). In this equation, the first term refers to the DC resistance. The second and third terms are related to losses due to eddy current and a mixture of skin- and proximity- effects, respectively. Fig. 4.3 shows a comparison of the spreading resistance at DC and a frequency of 600 GHz as a function of the buffer-layer thickness.

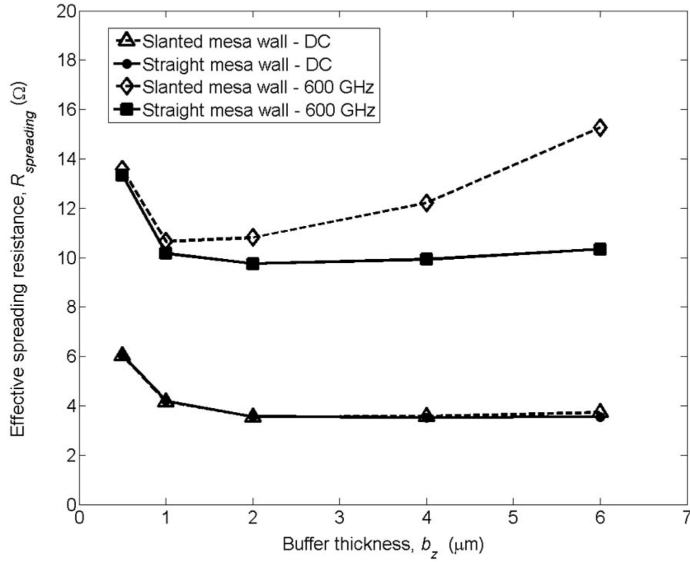

Fig. 4.3: A comparison of the spreading resistance as a function of buffer-layer thickness for both slanted and straight mesa wall diodes.

The analysis reveals advantages of the straight mesa wall diodes compared to the slanted mesa wall diodes. For the ohmic contact mesa optimisation, the lower boundary of the buffer-layer thickness is limited by the DC resistance. Meanwhile, the upper limit of a ohmic contact thickness is approximately one-skin depth at the operating frequency.

Details of the result and discussion are presented in Paper [A].

4.1.2 Effect of parasitic reactance on power coupling

The objective of this analysis is to study the influences of the diode surface-channel geometry on the diode parasitic capacitance and inductance. Fig. 4.4

illustrates the surface channel parameters analysed using the model presented in Chapter 3.1.2. The geometry parameters analysed in this work are summarised in Table 4.2.

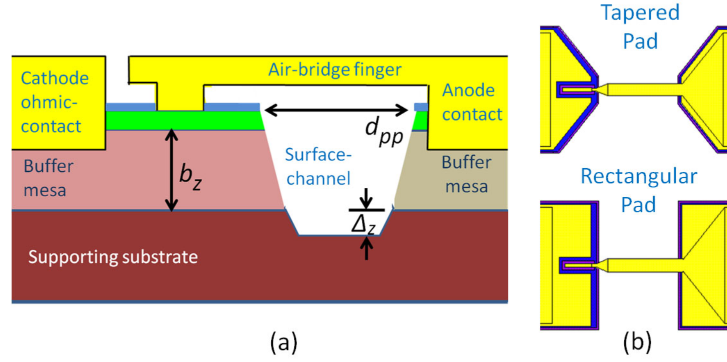

Fig. 4.4: Planar diode surface channel parameters: (a) cross-section view; (b) top view.

Table 4.2: List of the surface channel geometry parameter variation.

Geometry parameter	Symbol	Variation
Length	d_{pp}	$8 - 20$ [a], $40\ \mu m$
Depth	b_z	$2,\ 4\ \mu m$
	Δ_z	$0.5 - 3.5$ [b] μm
Shape of the contact mesa pads		rectangular, tapered

[a] interval of 2 μm.
[b] interval of 0.5 μm.

Fig. 4.5 shows the result of parameter extraction for both rectangular and tapered pads. In general, a lower pad-to-pad capacitance could be achieved with the tapered pads for a similar distance, especially for short distances. This is due to a reduction of the fringing field at the side of both mesas.

A reduction of the parasitic capacitance is possible to achieve by etching deeper into the supporting substrate during mesa isolation, i.e. creating a deeper surface channel. Meanwhile, increasing the depth of a surface channel by increasing the buffer-layer thickness is not favourable, since it increases the parasitic capacitance. In addition, a thicker buffer-layer increases the high frequency losses due to current crowding (see Section 4.1.1).

Referring to Fig. 4.5, the parasitic capacitance can also be reduced by increasing the distance between the pads. However, the finger inductance increases linearly as a function of the pad-to-pad distance. In order to investigate the effect of parasitics on the power coupling capability to the diode junction, the diode resonance frequencies are analysed.

Referring to the diode equivalent circuit in Fig. 3.4, the diode input impedance can be formulated as (3.4). By using (3.2) and (3.3), the diode resonance frequencies can be calculated analytically, by finding the roots of the nominator and denominator of (3.4), as a function of the pad-to-pad distance. In this

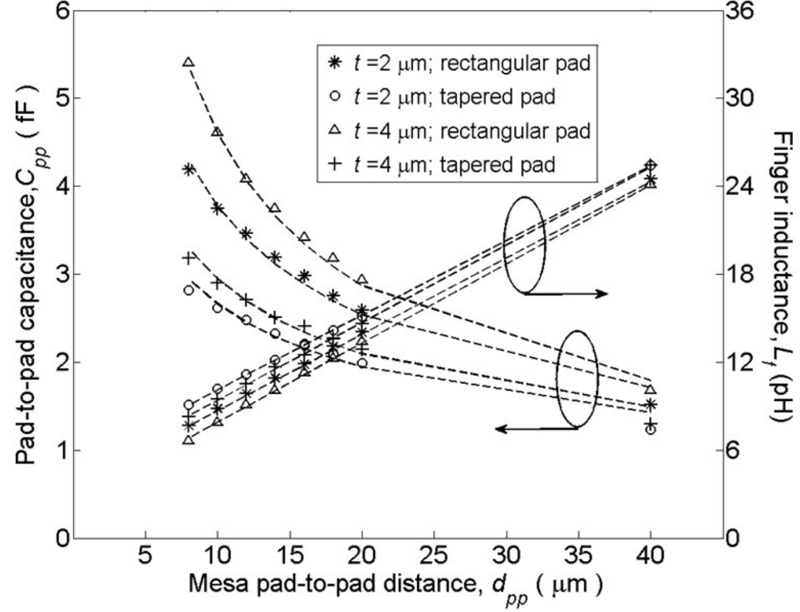

Fig. 4.5: (a)The parasitic capacitance, C_{pp}, and inductance, L_f as a function of the surface channel length, d_{pp} for both rectangular and tapered pads (Markers: extracted data; dashed-lines: fitted-curve).

analysis, a finger-to-pad capacitance of 0.5 fF is extracted from the EM simulation. The optimum mixer diode intrinsic resistance, R_{diode}, and average diode capacitance, C_{diode}, are approximated to be 100 Ω and 4 fF, respectively [58].

Fig. 4.6 shows a contour plot of the diode resonance frequencies. For a pad-to-pad distance longer than 5 μm, both the series and parallel resonance frequencies decrease as the distance is increased. This indicates that the finger inductance plays a more significant role in defining the diode resonance frequencies. For a pad-to-pad distance of less than 5 μm, the parasitic capacitance starts to dominate the diode resonance behaviour. Thus, a further decrease in the distance results in a decrease of the diode parallel resonance frequency.

Generally, an optimum design of the diode can be achieved by tapering the pads and thin buffer-layer, provided the spreading resistance at DC is acceptable. The optimisation of the pad-to-pad distance includes a consideration of the trade-off between the pad-to-pad capacitance and the finger inductance. It is important to optimise the diode geometry which enables the diode to operate within a frequency range much lower than the resonance frequencies.

4.2 Multiplier chip thermal optimisation

The 6-anode multiplier chip is designed in a way so that the chip is secured in the waveguide channel by clamping the beam leads between the two waveguide split blocks. In this system, the waveguide acts as the heat sink. The excessive heat in the chip is dissipated laterally towards the heat sink via the beam leads.

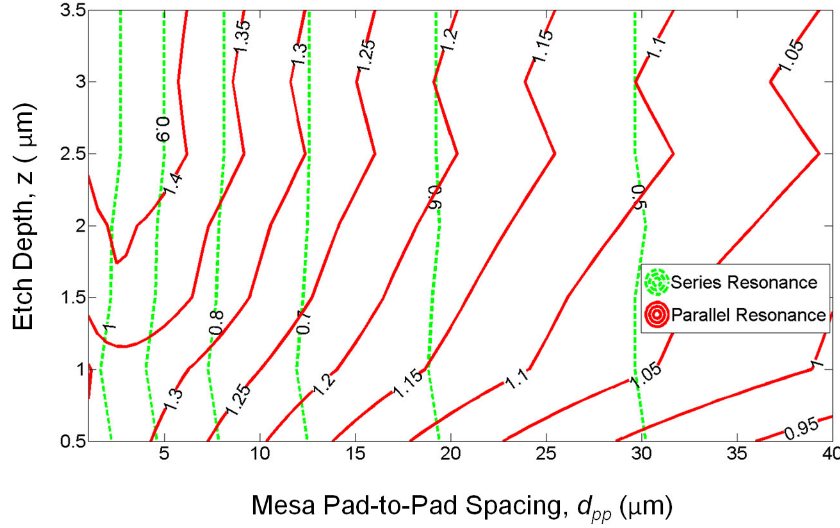

Fig. 4.6: A contour plot of the series and parallel resonance frequencies (THz) as a function of etch depths and pad-to-pad distance for a tapered pad with 2 μm thick buffer-layer.

Fig. 4.7 shows an example of the temperature distribution within the chip and the anode junction temperatures. It is observed that the hot spots are at both the anodes located closest to the centre of the chip. High thermal gradient occurs in the beam lead region, which bridges the multiplier chip to the waveguide. In addition, the temperature profile also indicates thermal constraints at the regions close to the anode contacts. The relatively high thermal resistances in these regions are due to the small diode mesa areas and narrow air-bridge fingers.

Electrical optimisation for high frequency operation favours a thinner chip substrate, where the dielectric loss is reduced. However, this deteriorates the chip thermal management. Due to the lateral heat flow, a thinner supporting substrate reduces the effective heat flow cross-section area. Furthermore, the temperature-dependent thermal conductivity of the GaAs further degrades the chip thermal capability. Thus, the electrical performance is limited by the thermal capability of the chip for high power applications.

Attaching a heat spreader, e.g. CVD diamond, under a thin substrate has been investigated and demonstrated as a solution for multipliers with thin substrate [77]. However, the advantage of the high thermally conductive CVD diamond is not fully exploited due to the high thermal resistance of the bonding agent, which is used to attach the heat spreader. At present, technology for the deposition of a CVD diamond layer on the substrate is available commercially. This provides another potential solution for future high power multiplier design. Without the thermal limitation from the bonding agent, the analysis shows that the temperature rise is approximately 100 K lower than that using a bonding agent and 50 K lower than that of a thick substrate (at a power dissipation of 30 mW per anode).

As mentioned previously, one of the thermal limitations of the multiplier chip

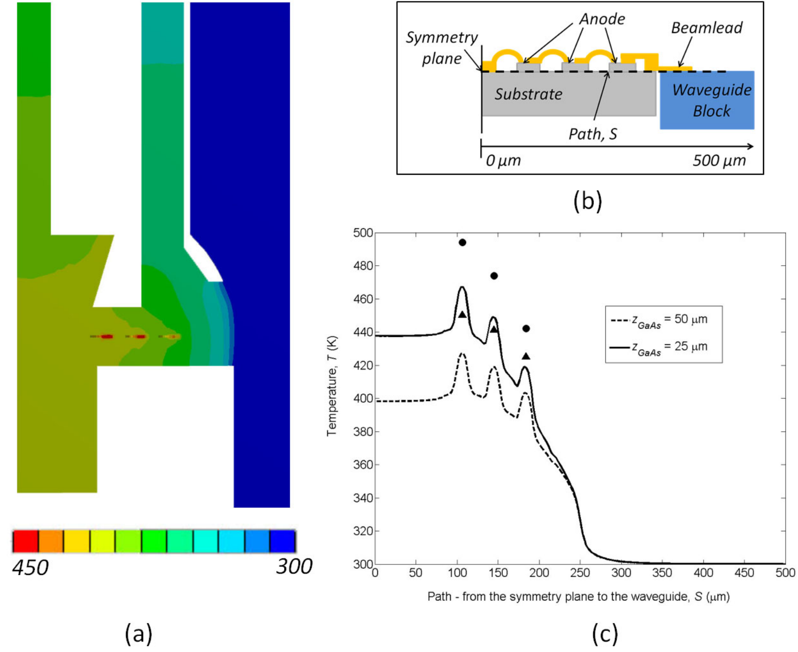

Fig. 4.7: (a) Top view of the temperature distribution throughout a multiplier chip with 50 μm thick substrate; (b) Physical location of the path S for the temperature profile plot; (c) Temperature profile along the substrate (Markers indicating the temperature at the anode junctions).

is the relatively poor thermal conductivity of GaAs. Thus, instead of attaching a heat spreader, another optimisation approach is to change to another material system for the diode and substrate. One of the potential materials under consideration is the GaN-based diode on a Si supporting substrate. Thermal analysis show that the GaN diode on silicon substrate multiplier is capable of sustaining higher power level, since both materials possess three to four times better thermal conductivity compared to GaAs. In view of the difference in the electrical properties of GaN and GaAs, e.g. the electron mobility, the multiplier performance may not be as efficient at lower power. However, beyond a certain input power level, it is possible that the output power of the GaN-based multiplier chips surpasses those of GaAs-based multipliers due to GaAs inherent thermal limitation.

Fig. 4.8 shows a comparison of the temperature profile between a GaAs with CVD diamond and a GaN multiplier chip. For a thin substrate, the result shows that the temperature gradient at the anode junction area is less significant in the GaN multiplier compared to the GaAs multiplier. This is due to a better thermal conductivity of the GaN material. However, the conduction heat bottle neck in the GaN material is more pronounced at the beam lead, which is thermally connecting the chip and the waveguide.

At the region close to the anode junction, the transient thermal behaviour shows several thermal time constants, τ_{th}. This is due to the distributed thermal mass and the thermal coupling between adjacent anodes. Nevertheless, the

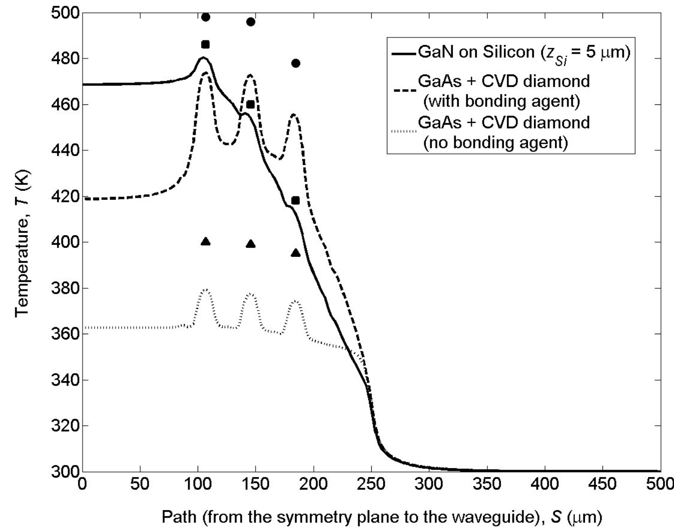

Fig. 4.8: A comparison of the temperature profile for a GaN diode on silicon substrate multiplier and a GaAs multiplier on a 10 μm thick CVD diamond (Markers show the corresponding temperature at the anode junctions).

final thermal settling time is more than 10 ms. Considering the electrical RF operation cycle which is tens of femto seconds or less, the transient thermal behaviour is considered not important for the multiplier operation. However, the thermal transient behaviour is important for applications with time-constants comparable to or lower than the thermal time constant. From a diode DC characterisation perspective, this analysis provides an estimate of the IV pulse settings required for the diode current-voltage characterisation without the influence of heating.

For both steady state and transient analyses, the simulation results are verified using the infrared microscope. The measurement is performed on a chip mounted on a half waveguide split block, heated up to a temperature of 80 $^\circ C$. In these measurements, the DC equivalent power is deposited by forward biasing the diodes. Thus, the measurement can only be performed at a relatively low power level.

Details on the result and discussion are presented in Paper [B].

4.3 Effect of excess heat on multiplier performance

Two multiplier chips with different substrate thickness are evaluated using the electro-thermal model and the results are compared to the measured efficiency. The multiplier chips evaluated are based on the ‘substrateless’ and the membrane technology developed by JPL. The supporting substrate beneath the diode is 50 μm and 5 μm thick for the substrateless and membrane multiplier, respectively.

The simulation shows that the thermal resistance at the hot spot is approximately two times higher for the membrane multiplier compared to the substrateless multiplier. An example of the temperature distribution plot for both chips are shown in Fig. 4.9.

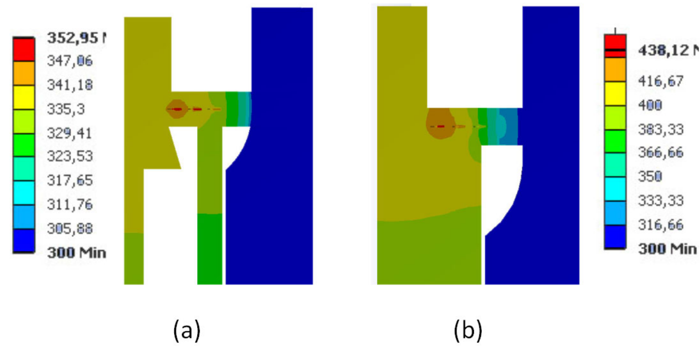

Fig. 4.9: A comparison of the temperature distribution in the multiplier chips at a dissipation power of 10 mW per anode: (a) substrateless; (b) membrane.

Benchmarking the simulation result by comparing the simulation result with and without a thermal model, the electrical performance for the membrane multiplier is expected to be better than the substrateless multiplier in the absence of thermal effect. However, due to a higher thermal resistance in the membrane multiplier, the multiplier performance is degraded. The peak conversion efficiency for the membrane multiplier is 23 % at a RF input power of 90 mW, compared to 24 % at a RF input power 120 mW for the substrateless multiplier.

In addition to the thermal effect, the multiplier eficiency is also limited by the current saturation phenomena. The current saturation level of the multiplier can be estimated using (2.28). As in a conventional electrical simulation (without the electro-thermal simulation), the electro-thermal model is also capable of providing the current-voltage information, which is useful to verify if the current saturation limit is reached. Thus, the multiplier efficiency degradation factors, either due to the current saturation or thermal effects, can be identified from the circuit simulation using the developed model.

In view of this, the developed model is useful for providing a first estimation of the trade-offs between the electrical and thermal design of the chip, either in varying the chip geometry, or exploring other materials. In addition, the temperature information is accessible via simulation, providing essential information for device reliablity studies.

Details on the result and discussion are presented in Paper [C].

Chapter 5

Conclusions and future work

The main objective of this research work is to study and understand the planar Schottky diode operation in the THz regime. The work presented in this thesis includes the investigation of the high frequency power loss and power coupling phenomena, as well as thermal effects on diode performance.

Regarding diode operation at THz frequencies, the diode parasitics have a significant impact on the diode performance due to the electromagnetic coupling. Conversion of the electromagnetic energy into heat results in power loss, which is known as the ohmic loss. High frequency loss analysis performed in this work shows that the strong frequency dependent series resistance is attributed to the onset of eddy current, skin and proximity effects (Paper [A]). From a high frequency perspective, it is beneficial that the volume of the semiconductors in close proximity to the metal conductors is minimised, e.g. minimising the highly-doped buffer material underneath of the air-bridge finger. In addition, the eddy current generation, skin and proximity effects have to be taken into account in optimising the distance between the metal conductors and semiconductor material.

The power coupling to the diode junction is limited by the geometry-dependent parasitic capacitance and inductance. In order to maximise the power coupling capability, it is important to minimise the parasitics. At present, numerical electromagnetic analysis is a common method used to analyse the parasitics as a function of diode geometry. However, experimental high frequency diode characterisation is also essential in evaluating the geometry-dependent parasitics.

Due to the inherently complex electromagnetic coupling within the planar diode structure, the diode characterisation work has to be divided into several sub-modules. This includes evaluating the planar structure parasitics on dummy diodes, i.e. diodes without air-bridge finger or diodes without anode contacts, at different frequency bands. Today, submillimetre wave characterisation methods are being actively developed by several key players in the THz field. This includes the development of waveguide embedded membrane circuit characterisation method in the WR-3 frequency band (220 – 325 GHz) at Chalmers University of Technology (see Paper [b,c]). Therefore, further work in this research area includes the high frequency characterisation of Schottky

diodes, especially at the application driven frequency band of interest.

For high power applications, the thermal capabilities of current multiplier design are limited by the relatively poor GaAs thermal properties and the restricted heat conduction path to the heat sink. Several thermal optimisation solutions are explored and analysed in this work. These solutions includes attaching a heat spreader under the chip, improving the heat spreading at the regions of thermal constraint and designing high power multiplier based on material with better thermal conductivity (Paper [B]).

Albeit by having the thermal optimisation options available, a quantitative estimation of the effect that the thermal solution has on the electrical performance is not straightforward. Thus, a self-consistent electro-thermal model is developed, where the trade-offs between the electrical and thermal design can be evaluated. This model serves as an important tool in optimsing the multiplier design, aimed at for instance increasing the multiplier output power (Paper [C]). Moreover, this model can also be implemented to investigate the mixer chip thermal behaviour, as well as a tool for device reliability studies.

In short, a better understanding of the diode operation at submillimetre wave is acquired through the research work presented in this thesis. With this, further optimisation of diode performance, e.g. pushing limits of the diode conversion loss and output power, in the submillimetre wave region hopefully be foreseen.

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Paper A

Impact of Eddy Currents and Crowding Effects on High Frequency Losses in Planar Schottky Diodes

A. Y. Tang and J. Stake

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Paper B

Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes

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Paper C

Electro-thermal Model for Multi-Anode Schottky Diode Multipliers

A. Y. Tang, E. Schlecht, R. Lin, G. Chattopadhyay, C. Lee, J. Gill, I. Mehdi, and J. Stake

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