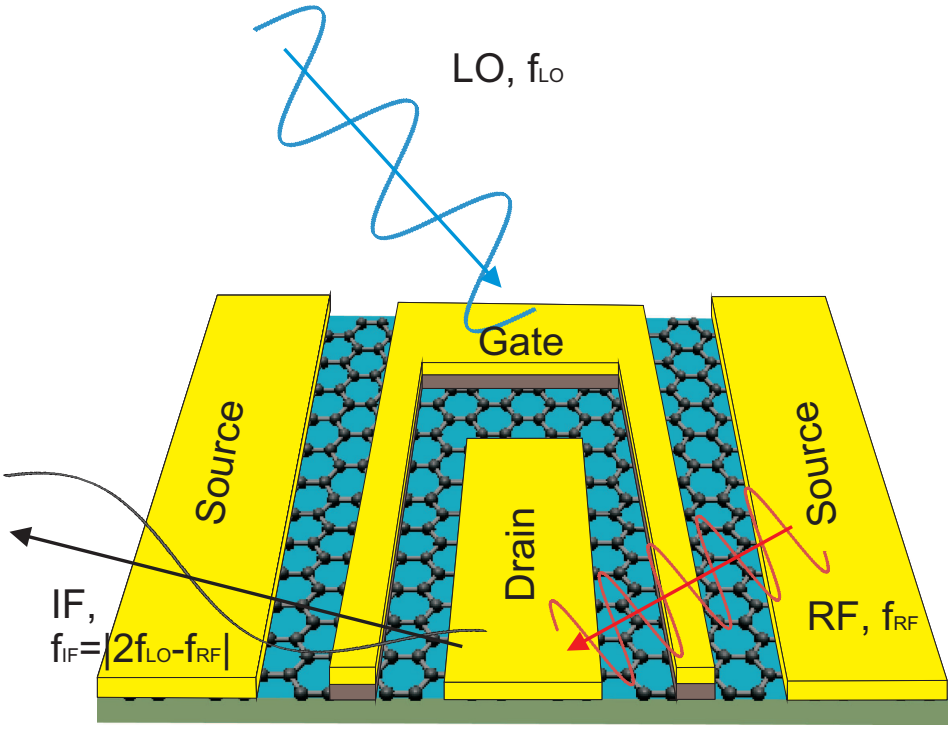

Fabrication, Characterisation and Modelling of Subharmonic Graphene FET Mixers

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CHALMERS UNIVERSITY OF TECHNOLOGY
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Thesis for the degree of Licentiate of Engineering

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by

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COVER: A graphene-FET with a two-finger gate operates as a subharmonic mixer. The LO and RF signals are applied to the gate and drain respectively and the IF signal is extracted from the drain.

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To Sara

Abstract

Graphene has exceptional carrier transport properties which makes it a promising material for future nanoelectronics. The high carrier mobility along with the ability to switch between n- and p-channel in a graphene field effect transistor (G-FET) truly distinguishes it from other types of FET technologies and enables completely new high frequency devices.

In this thesis, a novel subharmonic resistive G-FET mixer is presented. The mixer operation is based on the G-FET's symmetrical transfer characteristic. Due to this property, the mixer operates with a single transistor and unlike the conventional subharmonic resistive FET mixers, it does not need any balun at the local oscillator (LO) port. This makes the mixer circuit more compact. The mixer conversion loss (CL) is measured with f_{RF}=2 GHz, f_{LO}=1.01 GHz and f_{IF}=20 MHz in a 50 Ω impedance system, and for a G-FET with an on-off ratio of 3, a CL of 24 dB is obtained. In addition, the mixer performance is analysed based on the G-FET parameters, the LO power and the embedding impedances. It is predicted that by having a G-FET with an on-off ratio of 10 and selecting proper embedding impedances, a CL of 17 dB is attainable. Also, by further improvement of the G-FET on-off ratio, the CL is optimised to about 14.2 dB.

Moreover, a process technology for 1 μm gate-length G-FETs based on exfoliated graphene has been developed. A contact resistance as low as 500-600 $\Omega.\mu m$ is obtained, which is close to the lowest reported value. In addition, different gate dielectric materials have been investigated. A plasma enhanced chemical vapour deposition (PECVD) process for deposition of a silicon nitride film as a gate dielectric is developed. The process maintains the carrier mobility of the graphene film largely intact after deposition. Also, to form Al_2O_3 gate dielectric films, a protective layer of naturally oxidised Al is used prior to e-gun evaporation of Al_2O_3. This layer prevents further degradation of the carrier mobility.

Finally, a novel closed-form large-signal model for G-FETs is developed. The model is semiempirical and can be utilised in standard Electronic Design Automation (EDA) tools for designing and analysing G-FET circuits. The model is implemented in Agilent's Advanced Design System (ADS) software and experimentally verified for a G-FET under both DC and RF operation. The DC results agree with the model. The RF verification includes S-parameters and power spectrum measurements. The S-parameters measurements essentially coincide with the model and the power spectrum analysis shows good agreement up to the 4th order. Moreover, the model is used to simulate the G-FET mixer CL and the results follow the measurements.

Keywords : Graphene, microwave FETs, subharmonic resistive mixers, device modelling, gate dielectric, harmonic balance analysis.

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I would like to express my gratitude to all people who helped me during this thesis. In particular I would like to sincerely thank my examiner and supervisor Prof. Jan Stake for his support, guidance and advices during this work. I would also like to thank my co-supervisor Dr. Josip Vukusic for his advisory role and helpful hints. A special thank to Prof. Olof Engström for fruitful discussions regarding gate dielectric processing and for his support and encouragement. I would like to thank Prof. Erik Kollberg for his valuable discussions and comments on my papers and this work. Thanks to Dr. Sergey Cherednichenko for his support and help during this thesis. In addition, a thank you to Prof. Mikael Fogelström for all his supports. Thank you Klas Yhland for the discussions on the resistive mixers and your comments on the papers. Thank you Michael Andersson for your assistance with measurements and proof reading. I would like to sincerely thank Nanofabrication Laboratory staff especially Henrik Frederiksen, Mats Hagberg, Bengt Nilsson and Mahdad Sadeghi for help in the cleanroom.

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List of appended papers

Paper A
O. Habibpour, J. Vukusic and J. Stake, "A Large Signal Graphene FET Model," submitted to *IEEE Transactions on Electron Devices*, 2011.

Paper B
O. Habibpour, S. Cherednichenko, J. Vukusic, K. Yhland and J. Stake, "A subharmonic graphene FET mixer," *IEEE Electron Device Letters*, vol. 33, no. 1, 2012.

Paper C
O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Mobility improvement and microwave characterization of a graphene field effect transistor with silicon nitride gate dielectrics," *IEEE Electron Device Letters*, vol. 32, no. 7, pp. 871-873, 2011.

Other papers

The following papers are not included in this thesis due to an overlap in content or a content going beyond the scope of this thesis.

1. J. Stake, O. Habibpour, J. Vukusic and O. Engström, S. Cherednichenko, "Graphene Millimeter Wave Electronics," invited paper presented at *6th ESA Workshop on Millimetre-Wave Technology and Applications and 4th Global Symposium on Millimeter Waves*, Espoo, Finland, 2011.

2. O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Investigation of harmonic generation in a suspended graphene," *GigaHertz Symposium*, Lund, Sweden, 2010.

3. O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Odd harmonic generation in a suspended graphene at microwave frequency," *Proc. of the 34th WOCSDICE*, Seeheim/Darmstadt, Germany, 2010.

4. O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Characterisation of Exfoliated Graphene," *Proc. of the 33 rd WOCSDICE*, Malaga, Spain, 2009.

Contents

Abbreviations and acronyms

ADS	Advanced Design System
ALD	Atomic Layer Deposition
CVD	Chemical Vapour Deposition
CL	Conversion Loss
DOS	Density of state
EDA	Electronic Design Automation
FET	Field Effect Transistor
f_T	Cutoff Frequency
f_{MAX}	Maximum frequency of oscillation
G-FET	Graphene Field Effect Transistor
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
IF	Intermediate Frequency
LO	Local Oscilator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapour Deposition
RF	Radio Frequency
THz	Terahertz (10^{12} Hz)

Chapter 1

Introduction

Graphene is a two-dimensional sheet of carbon atoms densely packed in a honeycomb lattice through sp2 bonding. The first demonstration of graphene was achieved by mechanical exfoliation of graphite in 2004 [1]. Since then, graphene has been the subject of extensive research theoretically and experimentally. Graphene has exceptional electrical and mechanical properties making it a new material for several fields including, stronger/stiffer components [2], low cost display screens in mobile devices [3], storing hydrogen for fuel cells [4], biosensors [5], ultracapacitors [6], photonics and optoelectronics [7], plasmonics [8, 9] and high frequency electronics [10]. Realisation of these applications needs a low cost large-scale graphene production method. Up to now, large-scale graphene films are produced by the sublimation of silicon carbide [11] and chemical vapour deposition (CVD) process [12]. The quality of the graphene produced by these two methods is sufficient enough for some applications like display screens, however, for some applications like high frequency electronics, these processes should be improved in order to reach the quality level of the exfoliated graphene.

The unique transport properties of graphene given by its lattice structure, opens new niches for electronics, optoelectronics and plasmonics applications. New graphene based components including graphene field effect transistors (G-FET) [13], photodetectors [14] and plasmon resonators [15] have been introduced. For nanoscale high speed electronics, graphene can offer many advantages over other existing technologies due to its superior intrinsic properties. First, due to the massless nature of carriers, electron and hole mobilities in graphene exceed 200,000 cm^2/Vs at a few Kelvin [16] and exceed 100,000 cm^2/Vs at near-room temperature (T = 240 K) [17]. These values of Hall mobility, are the highest reported for any material and therefore graphene has potential for room-temperature operation in the THz frequency range. In addition, carriers in graphene exhibit very high drift velocities ($4 \times 10^7 cm/s$) at high fields [18, 19]. Also, graphene is a zero-bandgap semiconductor with bands intersecting at the Dirac points. The density of states is zero at the Dirac point and rises linearly for higher and lower energies. This allows field-effect control of the charge density. Finally, graphene has an excellent thermal conductivity of 5000 W/mK [20] and a high critical current density of 2×10^8 A/cm^2 [21]. These prop-

erties suggest that graphene has potential for high power density operation.

Potential applications for graphene-based high speed electronics are limited to RF applications rather than logic circuits. Since the bandgap of graphene is zero, G-FETs with a large-area-graphene channel cannot be switched off and they consume power even in the off state. Hence, G-FETs with this type of channel are not suitable for logic applications. To open a bandgap needed for logic circuits, very narrow well-defined nanoribbons are needed [22]. However, reducing the width of the nanoribbons results in a parabolic bandstructure which increases the effective carrier mass and thereby decreases the carrier mobility [23].

To realise graphene based electronics for RF systems, various types of active components including amplifiers, fundamental/subharmonic frequency mixers, frequency multipliers and oscillators are required. Since transistors are fundamental building blocks for above components, having high performance G-FETs is a significant step towards graphene based RF circuits. This purpose requires overcoming several challenges. To begin with, the gate-dielectric formation process degrades the carrier mobility severely [13]. Although several methods have been developed to decrease this effect [24, 25], the carrier mobility of graphene in G-FETs is still far from its potential. Secondly, high contact and access resistances due to the high sheet resistivity of graphene can degrade the RF performance of G-FETs. The access resistance can be reduced by a self-aligned structure [26] and a contact resistance as low as 500 $\Omega.\mu m$ at room temperature has been achieved [27]. However, this value should be reduced an order of magnitude in order to have high performance G-FETs. Finally, the transfer characteristic of G-FETs exhibits hysteresis. The hysteresis originates from charge traps at the graphene/dielectric interface [28, 29]. Hence, reducing interfacial charges is a significant step forward to reduce the hysteresis in the transfer characteristic.

Already huge efforts have been undertaken to mitigate above challenges and improve G-FET performance. As a result, waferscale G-FETs with intrinsic f_T more than 100 GHz [30, 31] and a G-FET from exfoliated graphene with intrinsic f_T more than 300 GHz [32] have been presented. However, due to high parasitic elements, especially contact resistances, the demonstrated transistors have too low transconductance and f_{MAX} for use in amplifiers. Fig. 1.1 shows the frequency performance of G-FETs compared to that of competing RF FETs (HEMT, Si MOSFET) [33]. It is seen that the frequency performance of G-FETs is far below the other technologies.

Recently, nonlinear components based on G-FETs including frequency doublers [34, 35] and fundamental mixers [36, 37] have been presented. The reported conversion loss (CL) of the frequency doublers and mixers are high ($\simeq$ 30 dB). This is due to the low on-off ratio of short gate length G-FETs. Consequently, reducing contact resistances as well as developing short gate length G-FETs with a high on-off ratio are imperative for achieving high performance graphene based RF circuits in the future.

In addition to having access to graphene based components, a G-FET model for simulating graphene based circuits is necessary. General small signal FET models [38, 39] can be used for the small signal analysis. However, for large signal applica-

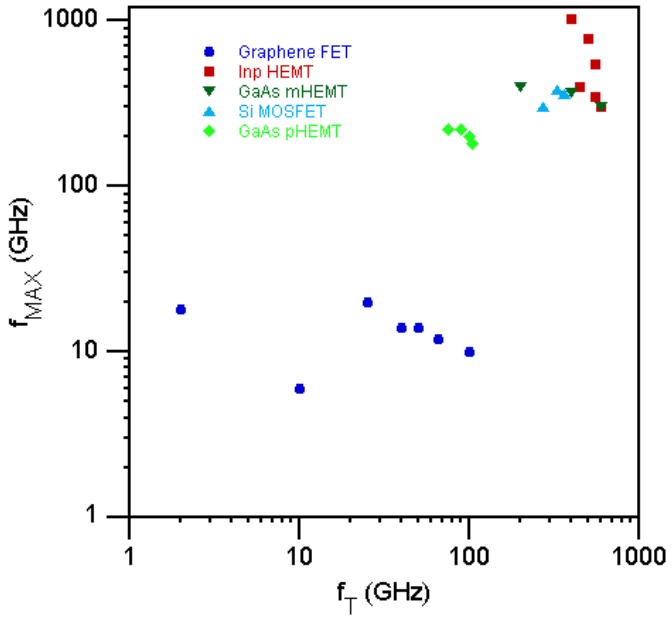

Figure 1.1: f_{MAX} vs f_T for G-FETs and competing RF FETs [33].

tions, a large signal G-FET model is required. Several physical models for predicting the charge density and the conduction of G-FETs have been proposed [40, 41, 42]. However, these models are too intricate for circuit modelling, i.e. they are not fast enough to be used in Electronic Design Automation (EDA) tools. As a result, an empirical/semiempirical model (preferably closed form) is required. There are some reported semiempirical models for G-FETs [43, 44]. These models allow the calculations of I-V characteristics, but they do not provide a closed form expression for the drain current which makes them difficult to implement in a standard circuit simulator softwares. Moreover, the models use the same carrier mobility for both electrons and holes which is not valid in many cases [30]. Up to now, all proposed models are only validated by DC measurements and no RF verification is reported.

In this thesis, a semiempirical closed form model for G-FETs is presented in paper A. The model can take into account the bipolar operation of G-FETs. It contains a small set of fitting parameters which can be extracted by a novel method. This new extraction method gives a more accurate estimation of the drain and source contact resistances than previously reported methods. The model is validated by comparing measured and simulated data at DC and RF. Furthermore, a novel subharmonic ($\times 2$) resistive mixer based on a G-FET has been fabricated and demonstrated at microwave frequencies [paper B]. The mixer utilises the symmetrical channel resistance versus gate voltage and it is implemented using only one transistor. Therefore, no balun is needed which makes the mixer circuit more compact. Finally a plasma enhanced chemical vapour deposition (PECVD) process for deposition a silicon nitride film as a gate dielectric is described in paper C. The process is modified in a way that the carrier mobility in graphene films remains largely the same as before the deposition.

Chapter 2

Graphene electronic properties

This chapter provides a brief background to the electronic properties of graphene with focus on the bandstructure, charge density, carrier mobility and velocity saturation.

2.1 Bandstructure

Graphene is a single two-dimensional layer of carbon atoms forming a dense honeycomb crystal lattice as shown in Fig. 2.1. Using a tight-binding Hamiltonian

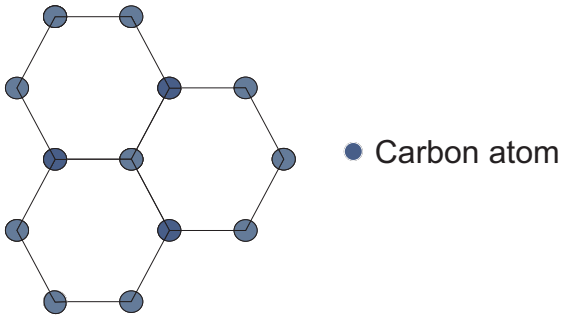

Figure 2.1: Graphene lattice structure.

to model graphene electrons, thereby assuming that electrons can only hop to the nearest neighbour atoms, the energy band can be derived as [45].

$$E_{\pm}(\mathbf{k}) = \pm t\sqrt{3 + 2cos(\sqrt{3}k_y a) + 4cos(\frac{\sqrt{3}}{2}k_y a)cos(\frac{3}{2}k_x a)} \tag{2.1}$$

where t (2.8 eV) and a (1.42 Å) are the nearest neighbor hopping energy and the carbon-carbon distance respectively. In the above expression, the plus and minus signs are applied to the upper (π) and lower (π^*) bands respectively. Figure 2.2 shows the full band structure of graphene. As can be seen, the conduction and valence bands touch each other at singular points called, Dirac points, in the Brioullin zone.

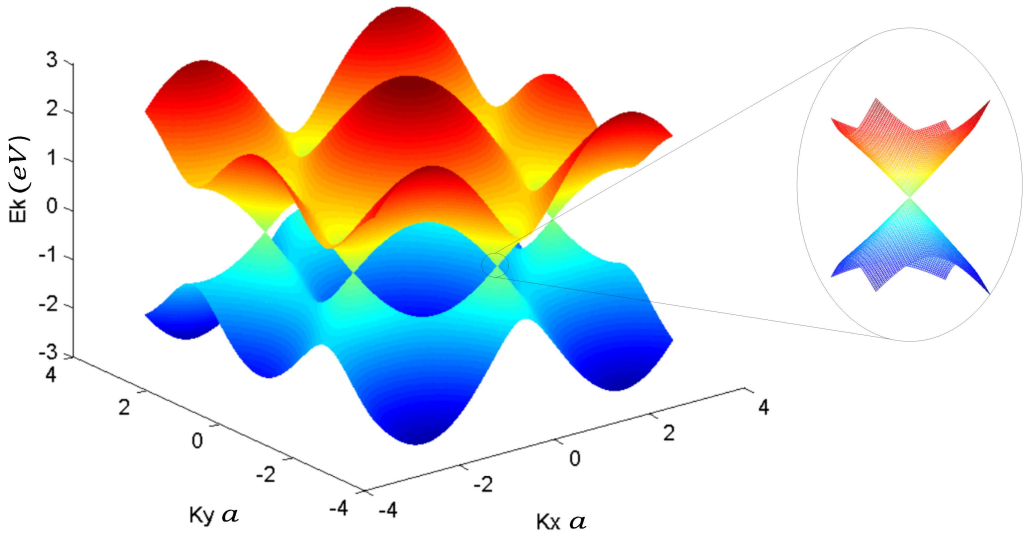

Figure 2.2: Left: Electronic dispersion in the honeycomb lattice, Right: lattice zoom in of the energy bands close to one of the Dirac points.

Thus graphene is a zero band-gap semiconductor (semi-metal). A zoom-in of the band structure close to the Dirac point is also shown in Fig. 2.2. In that range the dispersion is obtained as

$$E_{\pm}(\mathbf{q}) = \pm v_F|\mathbf{q}| \tag{2.2}$$

where $\boldsymbol{q}$ is the momentum measured relatively to the Dirac points and v_F is the Fermi velocity given by $v_F = 3ta/2\hbar \simeq 10^6$ m/s (1/300 of the speed of light). The positive sign in Eq. 2.2 represents energies in the conduction band, and the negative sign leads to energies in the valence band. The linear energy-momentum relationship

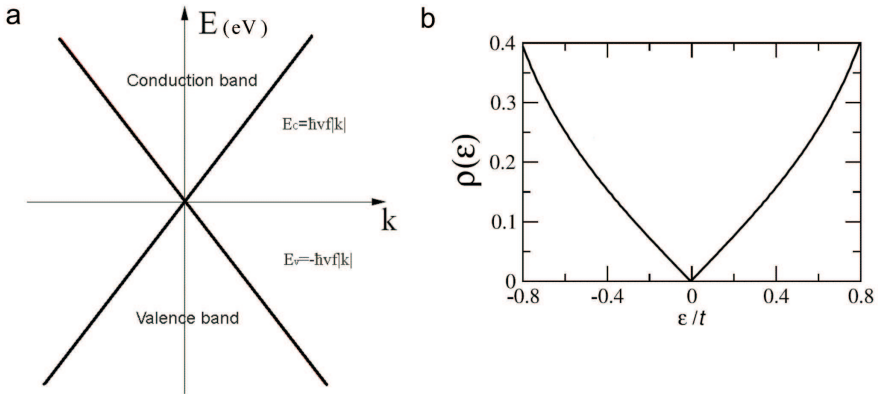

Figure 2.3: a) Energy dispersion model, b) Density of states versus energy [45].

is a very important aspect of the energy dispersion of graphene. Due to the linear

energy band diagram, electrons and holes behave like relativistic particles described by the Dirac equation. Consequently, graphene exhibits electronic properties that are unique for a 2D gas of particles. Moreover, the interaction between electrons and the lattice causes the electrons to behave as if they don't experience mass [46].

The energy dispersion model and the density of states of graphene close to the Dirac point are depicted in Fig. 2.3. The density of states linearly depends on $|E|$ around the Dirac point and can be given by [45]

$$\rho(E) = \frac{2A_c}{\pi}\frac{|E|}{v_F^2} \tag{2.3}$$

where $A_c = 3\sqrt{3}a^2/2$ is the unit cell area.

2.2 Carrier transport

Carrier mobility and velocity saturation are two important properties of materials used for high frequency electronics. The carrier mobility characterises how quickly a carrier can move, when a low to moderate electric field is applied and the saturation velocity is the maximum velocity a charge carrier attains in the presence of high electric fields. Materials with high carrier mobility and velocity saturation are suitable for high speed electronics.

It is experimentally [16] and theoretically [47] shown that free standing graphene has the highest carrier mobility among all semiconductors. This is due to the very low effective mass (table 2.1). In suspended mode (Fig. 2.4), the carrier mobility is mainly limited by the acoustic phonon scattering of the graphene lattice [47] and it is referred to as the intrinsic carrier mobility. Due to the dependency of the carrier scattering to the acoustic phonons, the carrier mobility decreases linearly with increasing temperature. Nevertheless, near-room temperature (T = 240 K) it is still more than 100,000 cm^2/Vs [17]. Also, when graphene is put in contact with/sandwiched between materials (e.g. substrate and gate dielectric) its intrinsic mobility severely degrades. This is due to scattering caused by either impurities located at graphene interfaces and in adjacent materials [48, 42] or by surface phonons of the adjacent materials [49, 50]. At low temperatures (T < 300 K), the impurity scattering is dominant and therefore the carrier mobility is constant. However, at high temperatures the surface phonon becomes dominant and the carrier mobility decays with increasing temperature [50]. The extrinsic carrier mobility of graphene varies from few thousands [51, 24] to tens of thousands cm^2/Vs [52, 53].

Table 2.1: Properties of graphene compared with conventional semiconductors

	Si	*GaN*	*GaAs*	*InAs*	*InSb*	*Graphene*
Electron effective mass (m^*/m_e)	1.09	0.19	0.067	0.023	0.013	0
$\mu_e(cm^2/Vs)$ at low doping (T = 300 K)	1200	1600	10000	33000	77000	100000
Bandgap (eV)	1.11	3.4	1.43	0.36	0.18	0
Velocity saturation ($10^7 cm/s$)	1	1.1	1.2	3.5	5	4

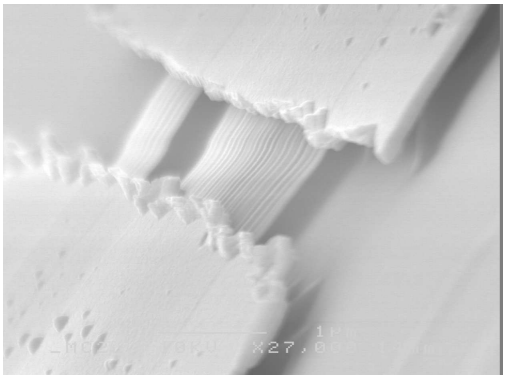

Figure 2.4: A SEM image of a suspended graphene film (85^0 tilted) [54].

Moreover, unlike the conventional semiconductors, the electron and hole mobilities in graphene are very close to each other. In suspended graphene they are the same [16] and in unsuspended graphene, due to the different type of impurities, they are within the same orders [51, 24].

The mobility is used for determining the carrier velocity in low electric fields. However, in submicron gate length FETs, the very high electric fields in the channel reduces the relevance of mobility. Instead, at high fields, the saturation velocity becomes an important measure of the carrier transport. Figure 2.5 depicts the electron velocity versus the electric field for conventional semiconductors and simulated plots for large-area graphene [19]. In graphene, the saturation velocity is mainly limited by the optical phonon scattering of the substrate, and it has been shown that within sufficient accuracy this scattering phenomenon can be described by a single phonon energy ($\hbar\omega_{OP}$) [18]. Therefore, the saturation velocity depends on temperature as $1/(N_{OP}+1)$, where $N_{op} = 1/(exp(\hbar\omega_{OP}/k_BT)-1)$ is the phonon occupation [55].

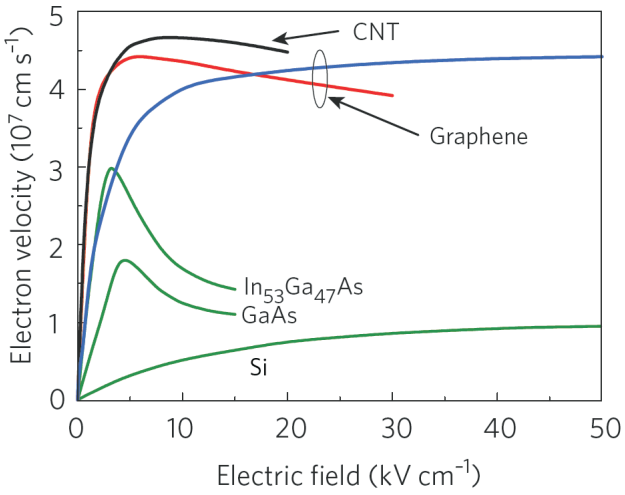

Figure 2.5: Electron drift velocity versus electric field [19].

2.2.1 Two-dimensional electron system in graphene

A 2-D system does not necessarily require a thin film and the possibility of the electronic wave function extending into the third direction should be considered. A 2-D system is defined quantum mechanically as when its electronic wave function is a plane-wave in 2-D while being a single quantised state in 3-D. In other words, a system is considered 2D if

$$\lambda_F = \frac{2\pi}{k_F} > w \tag{2.4}$$

where λ_F is the Fermi wavelength and w could be a potential well creating the film, as in 2D semiconductors, or just its thickness, as in graphene. For graphene, we have $\lambda_F \approx 35/\sqrt{\bar{n}}$ nm, where $\bar{n} = n/(10^{12} cm^{-2})$ [45], and since $w \approx 0.3$ nm (monolayer) the above condition is always satisfied, even for unphysically large $n = 10^{14} cm^{-2}$. Therefore, graphene in a strict sense is a 2D system with all carrier dynamics limited to the plane of the single layer carbon lattice. Note that in thin metal films it is impossible to have 2D electronic systems due to very high electron density of metals ($\lambda_F \approx 0.1$ nm).

2.3 Charge modulation and ability to switch between n- and p-channel

The electron and hole densities in a graphene sheet are given by the following expressions

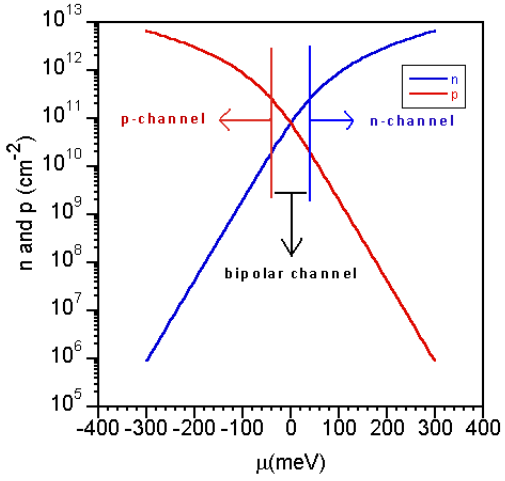

Figure 2.6: Electron concentration (n) and hole concentration (p) versus chemical potential at room temperature (-300 meV to 300 meV is the realistic range).

$$n = 4 \int \int f(E_+(q) - \mu) \frac{dq_x dq_y}{(2\pi\hbar)^2} \tag{2.5}$$

$$p = 4 \int \int [1 - f(E_-(q) - \mu)] \frac{dq_x dq_y}{(2\pi\hbar)^2} \tag{2.6}$$

where $q = |\mathbf{q}| = \sqrt{q_x^2 + q_y^2}$, μ is the Fermi energy and $f(E)$ is the Fermi-Dirac distribution function. The factor of 4 in the front accounts for spin degeneracy and the two valleys in the first Brillouin zone of graphene [56]. Fig. 2.6 shows the electron, n, and hole, p, concentration dependence on the Fermi level at room temperature. It can be seen that both electrons and holes contribute to the sheet charge density and depending on the Fermi level, the charge density of graphene can be dominated by electrons or holes. The Fermi level can be set by the field effect in a FET structure. Therefore a G-FET has the ability to switch between n- and p-channel, as opposed to conventional FET transistors that can operate with only a single carrier type (electron or hole) [57, 58, 59]. This unique property can be utilised to realise new nonlinear devices which are described in chapter 4. Fig. 2.7 demonstrates the layer structure of the G-FETs.

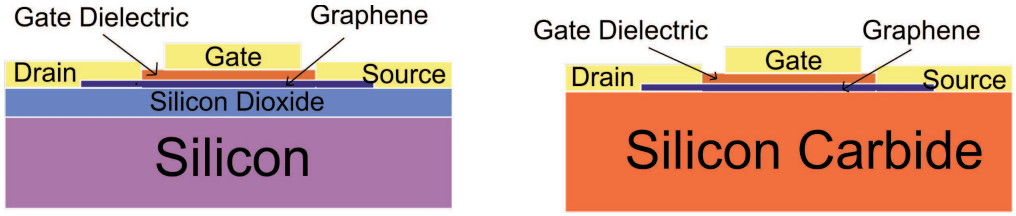

Figure 2.7: The layer structure of G-FETs based on, exfoliated graphene (left), and sublimation of SiC (right).

Chapter 3

G-FET fabrication, characterisation and modelling

The first part of this chapter includes G-FET fabrication process and characterisation. Then, large signal G-FET models are presented.

3.1 Device fabrication and characterisation

Graphene can be produced by the micromechanical exfoliation of natural graphite [1], sublimation of silicon carbide substrates [11] or CVD processes [12]. In this work, G-FETs are based on exfoliated graphene yielding high quality films. The single-layer character of the graphene sheets can be verified with Raman spectroscopy [60]. For graphene on a 300 nm silicon oxide film, however, it can also be confirmed by measuring the changes in the reflectance of green light [61] and in this work this method is used.

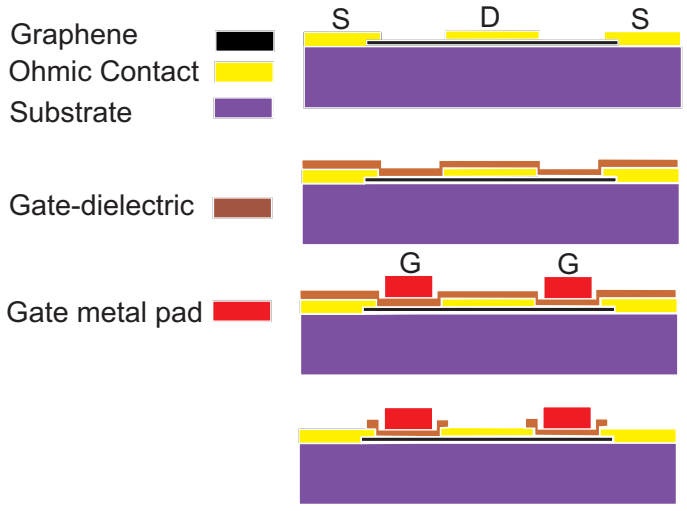

Figure 3.1: Fabrication process sequence for a G-FET device.

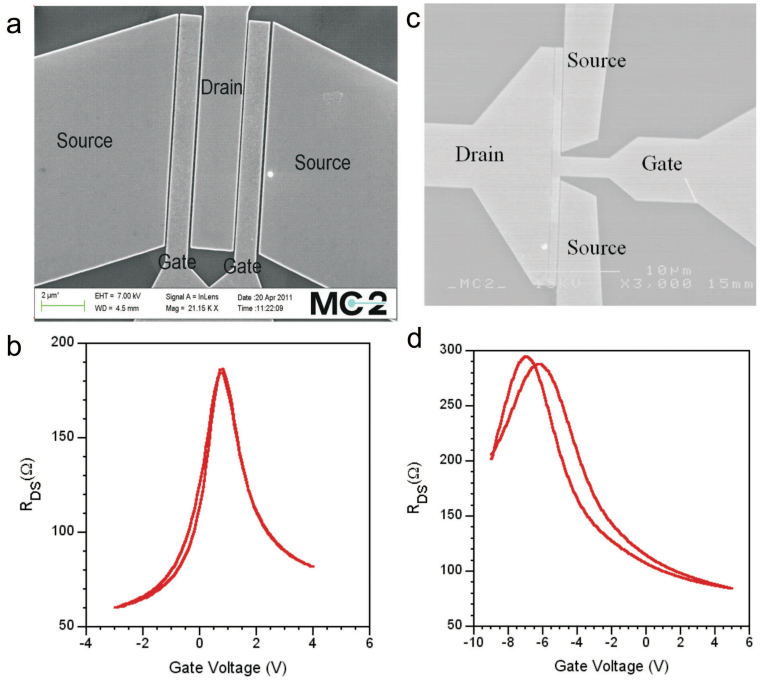

Figure 3.2: a) G-FET with 25 nm Al_2O_3 as a gate dielectric ($L_g = 1$ μm, $W_g = 20$ μm), b) Drain to Source resistance of the G-FET in a , c) G-FET with 40 nm silicon nitride as a gate dielectric ($L_g = 1$ μm, $W_g = 15$ μm) and d) Drain to Source resistance of the G-FET in c.

For microwave applications an insulating substrate is needed and for that reason, a high resistive silicon ($\rho \geq 10$ kΩ.cm) is used. The fabrication process steps are schematically illustrated in Fig. 3.1. The electron-beam lithography is used for all lithography steps. The fabrication sequence includes ohmic contact formation, gate dielectric deposition, gate pad formation and finally dielectric etching for defining the drain and source pads.

Due to the high sheet resistivity of graphene, carriers are injected into the channel at the edge of the graphene-metal contact. Therefore the contact resistance can not be reduced by having a large area graphene film beneath the ohmic contacts. In other words, the contact resistance is only depend on the channel width rather than the contact area [27]. Moreover, the choice of metal for the contacts affects not only the contact resistance, it also influences the transfer characteristic of G-FETs. In [27], it has been shown that Ni contact results in a lower contact resistance (500 $\Omega.\mu m$) than Cr/Au or Ti/Au contacts (> 1k $\Omega.\mu m$). In addition, Cr/Au contact leads to a symmetric transfer characteristic around the gate voltage of the minimum conductivity, V_{Dirac}, while the Ti/Au contact causes an asymmetric transfer function. A symmetric transfer characteristic is necessary for applications requiring the same level of conductivity for both n- and p-channel [34], [paper B]. In this work the ohmic contact metallisation is Ti(1 nm)/Pd(30 nm)/Au(60 nm). This metallisation stack gives a contact resistance of (500-600 $\Omega.\mu m$) and a fairly symmetric transfer function around V_{Dirac}. The contact and access resistances in G-FETs are about an

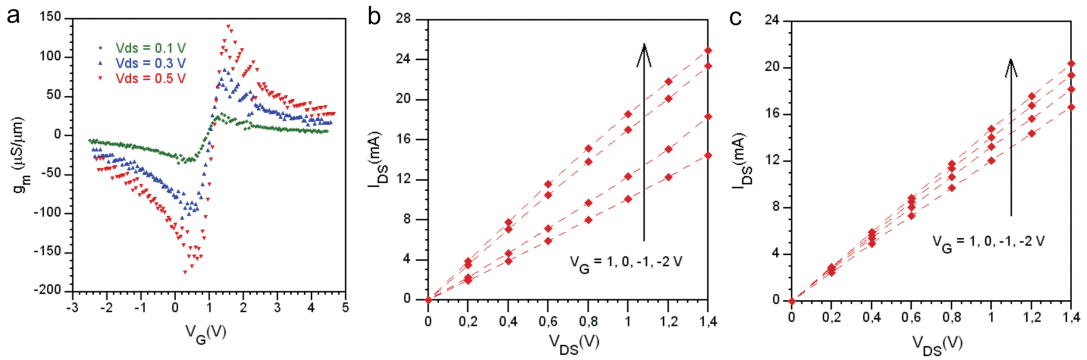

Figure 3.3: a) g_m of the G-FET in Fig. 3.2a at V_{ds} = 0.1, 0.3 and 0.5 V, b) Pulsed I-V characterisation at V_g = 1, 0, -1 and -2 V, c) DC I-V characterisation at V_g = 1, 0, -1 and -2 V.

order of magnitude higher than those of conventional FETs [27]. In order to reduce the access resistance a self-aligned structure is required [51]. However, the reduction of the contact resistance still remains a big challenge.

The gate dielectric formation process can severely degrade the transport properties of graphene [13]. Different methods have been reported to overcome this problem. One approach is to use atomic layer deposition (ALD) of high-k oxides which is performed at low temperature. However, surface pretreatments is necessary to avoid discontinuous film growth, e.g. a polymer buffer layer is used as a seed layer for the ALD of HfO_2 [62]. This method preserves the transport properties of graphene. However, from a technological point of view it is preferred to avoid the liquid processing needed for the polymer deposition. Moreover, the polymer has a problem of thermal stability. A new method for direct deposition of silicon nitride has been developed in paper C. This method preserves the transport properties of graphene. However, with this method the graphene will be unintentionally charged (doped) with electrons and V_{Dirac} appears at high negative voltages (3.2d). Therefore for large signal applications like frequency doublers and subharmonic mixers ([34], [paper B]) in which the gate voltage is needed to be biased at V_{Dirac}, this method of gate dielectric deposition is not suitable. Another method is to use a 2 nm oxidised Al as a seed or protection layer [24]. In this method a thin 1-2 nm Al is deposited on the graphene surface and oxidised naturally. Then a thicker dielectric is deposited using ALD or evaporation onto the thin oxidised layer. This method not only preserves the graphene carrier mobility, but also keeps V_{Dirac} close to the zero gate voltage. Fig 3.2 shows the fabricated G-FETs with Al_2O_3 and silicon nitride gate dielectric ($L_g = 1$ μm). It is seen that both devices have a hysteresis in the transfer characteristics but in the G-FET with Al_2O_3 gate dielectric the effect is lower.

The DC characterisation of the G-FET with Al_2O_3 gate dielectric is depicted in Fig. 3.3. It can be seen that the device transconductance, g_m is about an order of magnitude lower than that of typical HEMTs [63]. This is due to the low on off ratio in G-FETs. Consequently, up to now, G-FETs have a low f_{max} [33]. Moreover,

the pulsed I-V and DC I-V charactersations are shown in Fig. 3.3 b,c. Due to the effect of self-heating different characteristics have been observed. In [64], it is shown that with a power density of 1-2 $mW/\mu m^2$, the temperature can increase more than hundred degrees. This power density also can generate more defects in the gate dielectric.

3.2 Device modelling

Device models can be divided in two major groups: physical models and empirical models. Physical models are imperative in the early stages of the device development and they can be used for process optimisation. Moreover, they give a better understanding of the physics behind the device behavior. Several physical models for predicting the behavior of G-FETs have been proposed [40, 41, 42]. However, they are usually too complex for circuit modelling, i.e. they are neither fast nor easily implemented in EDA tools. Consequently, an empirical (semiempirical) model for G-FETs is preferred for circuit simulation. Several semiempirical models for G-FETs havr been reported. For instance, a model based on the semiempirical square-root charge-voltage relation is presented in [18, 65]. The model, however, uses the same carrier mobility for the electrons and holes which is not valid in many cases [30]. In addition to that, it cannot predict the asymmetric channel resistance for electrons and holes [66]. Another semiempirical G-FET model, based on a short-channel Si MOSFET model has been proposed [44] which allows the calculation of I-V characteristics. However, this model also uses the same carrier mobility for both electrons and holes. Up to now, the proposed models do not have a closed form and are only validated by DC measurements.

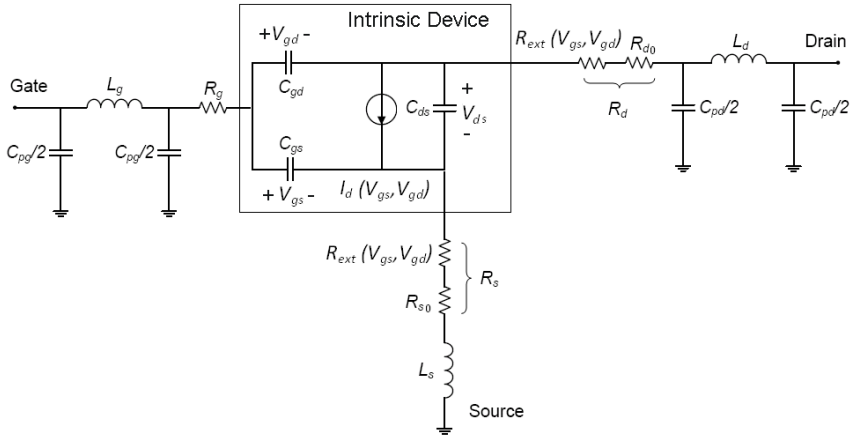

Figure 3.4: Equivalent circuit of a G-FET device.

In paper A, a novel closed form model for G-FETs which is similar to the model developed for HEMT/MOSFET [67] is presented. The model can also take into account the asymmetrical channel resistance of the G-FETs and accepts different carrier mobilities for electrons and holes. The proposed large signal G-FET model

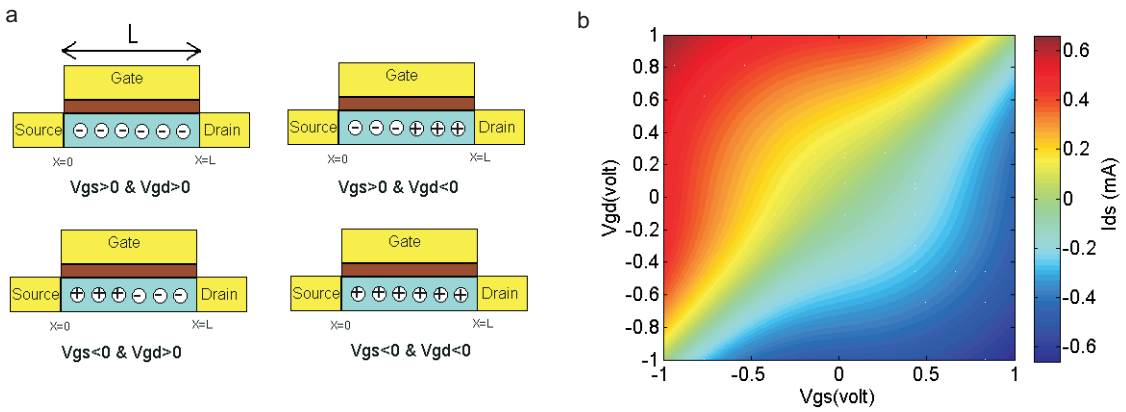

Figure 3.5: a) Carrier type in a G-FET channel at 4 different V_{gs}- V_{gd} plane quadrants, b) Contour plot of drain current ($I_{dss}(mA/\mu m)$) of a G-FET based on intrinsic V_{gs} and V_{gd}.

is based on an equivalent circuit shown in Fig. 3.4. The model is divided into two parts. The intrinsic device is defined as the part of the G-FET where the gate and channel overlap, while the rest includes parasitic elements.

In this model, the drain current is determined by the intrinsic V_{gs} and V_{gd} voltages and the type of majority carriers is determined depending on in which quadrant of the $V_{gs} - V_{gd}$ plane the device bias is (Fig. 3.5). In order to model the asymmetrical transfer function of G-FETs, a variable term is added to the drain and source resistances. This new term depends on the intrinsic V_{gs} and V_{gd}, and introduces an extra resistance when the channel majority carriers changes from holes to electrons.

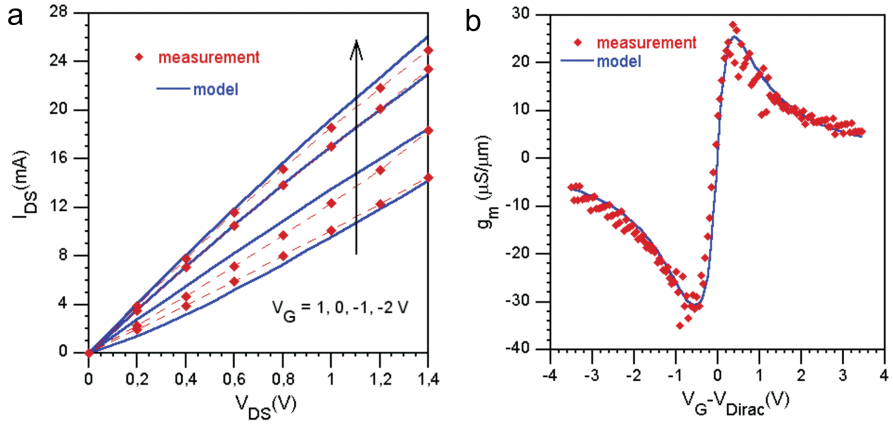

Figure 3.6: a) Model versus measured data for $I_d - V_{ds}$ characteristic curves at V_G= 1, 0, -1 and -2 V (from the bottom to the top), b) Model (solid line) versus measured data for the g_m ($V_{DS} = 0.1$ V) .

For the accurate extraction of parasitic elements, S-parameters of the open and short structures are needed [39, 68]. In conventional FETs, the open and short structures are obtained by biasing the device under the forward-biased gate and

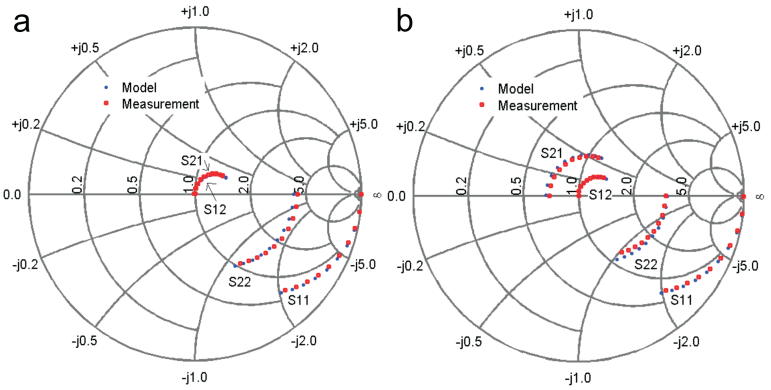

Figure 3.7: The modeled and the measured S-parameters of a G-FET, a) $V_g = 1.5$ V , $V_{DS} = 0.5$ V and b) $V_g = 1.75$, $V_{DS} = 0.5$ V.

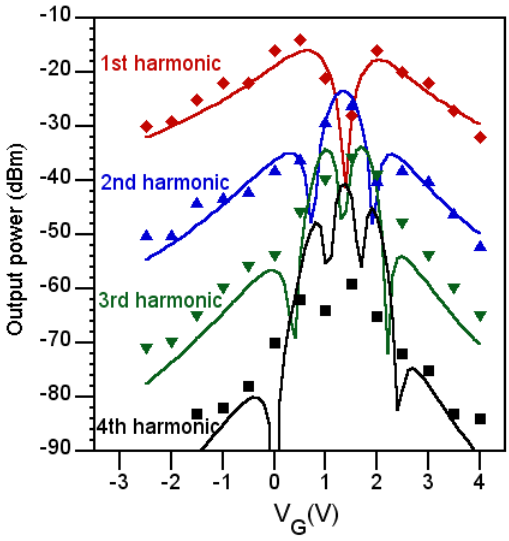

Figure 3.8: Measured and modeled power spectrum, $f_{in} = 10$ MHz, $P_{in} = 0$ dBm, $V_{DS} = 0.5$ V .

pinched off respectively ($V_{ds} = 0$). However, since G-FETs can not be pinched off, a modified method is needed for the parasitic element extraction. In [32], open and short structures with identical layouts, excluding the graphene channel, are used to deembed the parasitic elements and calculate the intrinsic elements by $Y_{intrinsic} = ((Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}$. However, since the open and short structures do not have a graphene layer, the parasitic drain and source resistances resulting from this method do not include the contact and access resistances which are the main parasitic resistances. As a result, this method underestimates the contact resistances. A new parameter extraction method is proposed in paper A which is based on both S-parameter and DC measurements. This method extracts both parasitic and channel parameters simultaneously.

The model is implemented in a circuit simulation software (ADS) and is exper-

imentally verified for a G-FET under both DC and RF operation. The g_m and $I_d - V_{ds}$ curves are depicted in Fig. 3.6 and as can be seen the model agrees with the measurements. The RF verification includes S-parameter and power spectrum measurements. In Fig. 3.7 the modeled and measured S-parameters of a G-FET are depicted for $V_g = V_{Dirac}$ ($g_m = 0$) and for $g_{m,max}$. The model is in good agreement with the measurements. Finally, a power spectrum measurement is performed to evaluate harmonic generation in the G-FET. A good global agreement between measured and modeled harmonic content is observed (Fig. 3.8).

Chapter 4

G-FET circuits

In this chapter circuits based on G-FETs are discussed with focus on a novel subharmonic resistive mixer. Up to now, the demonstrated G-FET circuits are limited to frequency multipliers and frequency mixers. This is due to the low extrinsic transconductance, g_{mex}, and high extrinsic drain conductance, g_{dex}, in G-FETs, which prevent the realisation of G-FET amplifiers. A low g_{mex} is caused by high contact resistances as well as a low on-off ratio, and a high g_{dex} is caused by having no saturation in the drain current. At low frequencies, the gain of a transistor can be approximated by $|S_{21}|^2 = 4Z_0^2 g_{mex}^2/(Z_0 g_{dex}+1)^2$, where Z_0 is the system impedance [69]. Fig. 4.1 shows the transistor gain versus g_{mex} and g_{dex} and the current status of the G-FETs. It is seen that a higher g_{mex} is needed in order to realise a G-FET amplifier.

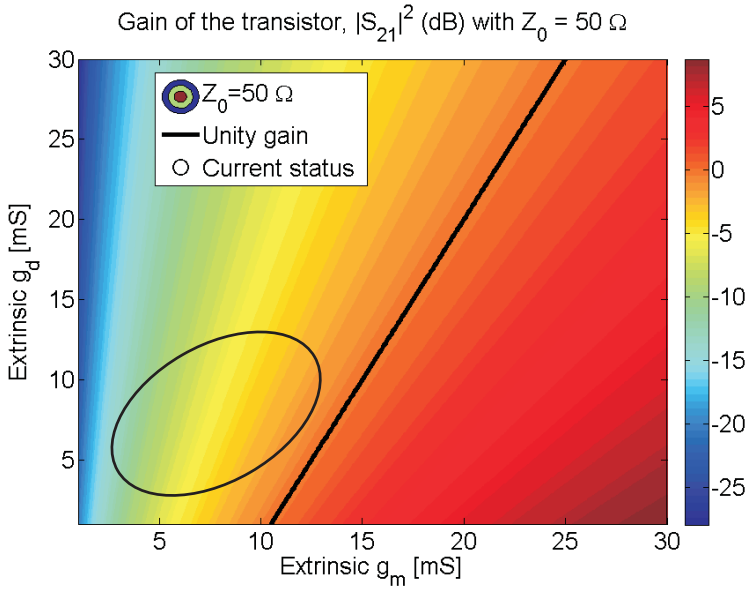

Figure 4.1: Contour plot of the transistor gain at low frequencies versus g_{mex} and g_{dex}.

4.1 Basics of frequency multipliers and mixers

A harmonic frequency multiplier generates a signal whose output frequency is an integer multiple of its input frequency. It is used to generate a high frequency signal from a lower frequency signal. Frequency multipliers are important especially at millimetre and submillimetre wavelengths where there is a lack of compact sources providing sufficient power [70]. The frequency multiplier conversion loss is the ratio of the input power at f_p and the output power at the frequency harmonic of interest, i.e. $CL_f(\text{dB})=P_{f_p}/P_{n\times f_p}$, where n is the order of the frequency multiplier. Frequency multiplication can be achieved from nonlinear two-terminal devices such as diodes [71] and varactors [72] or from transistors [73].

A frequency mixer converts power from one frequency to another frequency while keeping the signal information mostly intact. For a down-converting mixer the input high frequency RF signal is down-converted to a low frequency IF signal. The mixer conversion loss is the ratio of input RF and output IF power: $CL_m(\text{dB})=P_{RF}/P_{LO}$. Nonlinear two-terminal devices such as diodes [74] as well as transistors (active mode or resistive mode) [75, 76] can be used for frequency mixing.

An embedding impedance is the impedance that a device sees from the surrounding at a specific frequency. By selecting proper embedding impedances, the performance of frequency multipliers and mixers can be optimised. This can be performed with load-pull analysis [77], [paper A].

4.2 Frequency doublers

The power spectrum measurement shows a G-FET's ability to generate high order harmonics. From Fig. 3.8 it is seen that by biasing at $V_g = V_{Dirac}$, the second harmonic reaches its peak value while the other harmonics decay severely. Consequently, the drain current mainly contains the second harmonic term [34]. Moreover, as opposed to the conventional single FET frequency doublers [78], the fundamental mode is substantially attenuated at the maximum power of the second harmonic. Therefore high spectral purity can be achieved without any filtering element. The circuit structure of a G-FET based frequency doubler is depicted in Fig. 4.2. Up to now, a CL of 30 dB at 1.4 GHz has been reported [35]. The CL can be decreased by improving the on-off ratio of the G-FETs.

4.3 Fundamental mixers

Figure 4.3 shows a diagram of a single-device fundamental G-FET mixer. The mixer has RF, LO, and IF matching and filtering circuits, which in addition provide port-to-port isolation. It is seen that both RF and LO signals are applied to the gate and the IF signal is extracted from the drain of the G-FET. The mixer operates as follows. The LO signal generates a time-varying transconductance, $g_m(t)$, and the RF signal is applied to the $g_m(t)$. Therefore the mixing terms including the IF

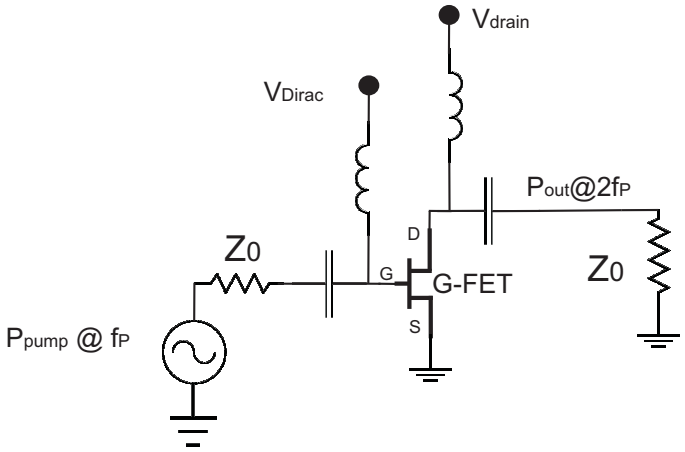

Figure 4.2: Circuit structure of a G-FET frequency doubler.

signal is generated in the drain current and is extracted by a lowpass filter.

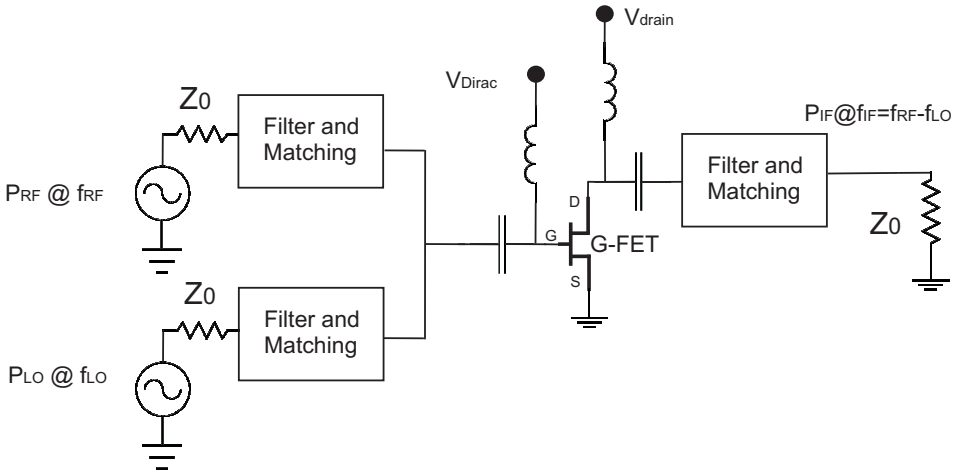

Figure 4.3: a G-FET fundamental mixer.

Since $g_m(t)$ is the primary contributor to mixing, it is important to maximise the range of variation [77]. As can be seen in Fig. 3.6, by biasing at $V_g = V_{Dirac}$, the variation range of $g_m(t)$ is maximised. Moreover, due to the symmetrical transfer characteristic around the V_{Dirac}, intermodulation distortions are significantly suppressed and a high input third-order intercept (IP3) point can be obtained. In [36] an IP3 of 13 dBm and a conversion loss of 35-40 dB at a frequency of 10 MHz is reported. The CL can be decreased by improving the transconductance of G-FETs.

4.4 Subharmonic (×2) mixers

In this section, a novel subharmonically pumped resistive mixer based on a G-FET is introduced [paper B]. The circuit topology of the proposed mixer is depicted in Fig. 4.4. In this configuration the RF signal is applied to the drain of the G-

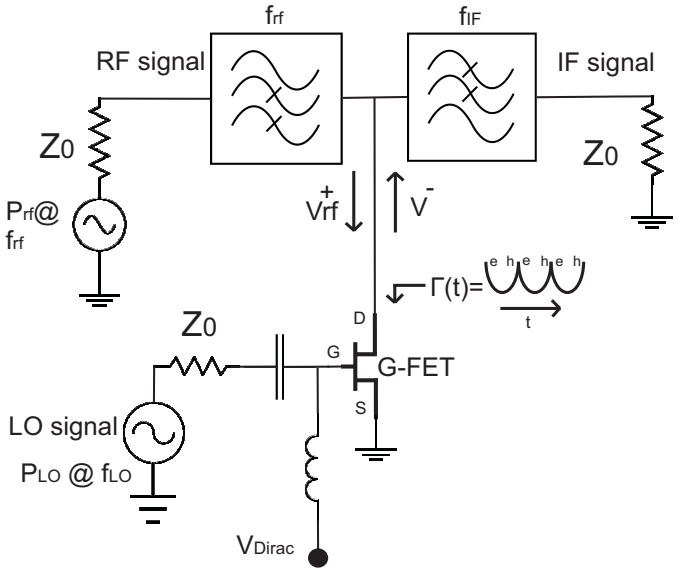

Figure 4.4: The circuit structure of the subharmonic resistive G-FET mixer.

FET. Consequently, from an RF point of view, the G-FET behaves like a variable resistance described by

$$R_{DS} = R_{min} + \frac{R_{max} - R_{min}}{\sqrt{1 + \beta_0 (V_g - V_{Dirac})^2}}, \tag{4.1}$$

with $\beta_0 = (C/qn_0)^2$ where C, n_0 and q are the gate capacitance per area, residual carrier density [24] and the electron charge respectively. The mixer operates as follows. A time-varying channel resistance ($R_{DS}(t)$) is generated by superimposing the LO signal with the gate voltage (V_{Dirac}) (Fig. 4.4a). Due to the symmetric transfer characteristic of G-FETs, the frequency of $R_{DS}(t)$, becomes twice the f_{LO}. The corresponding time-varying reflection coefficient $\Gamma(t) = (R_{DS}(t) - Z_o)/(R_{DS}(t) + Z_o)$, seen into the drain of the G-FET is depicted in Fig. 4.5b, where Z_0 is the

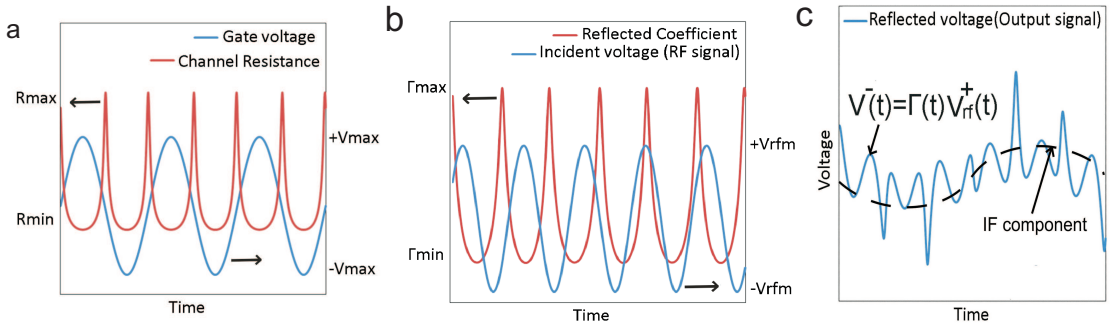

Figure 4.5: (a) Time-varying gate voltage (LO signal) and the corresponding channel resistance. (b) Time-varying reflection coefficient and the incident voltage (RF). (c) Reflected voltage (mixing signal).

system impedance. By applying the RF signal, $V^+_{RF}(t)$, through a highpass filter, a reflected signal $V^-(t) = \Gamma(t)V^+_{RF}(t)$ is generated [79]. The reflected voltage has frequency components at $|f_{RF} \pm 2n \times f_{LO}|$ and the IF component (Fig. 4.5c) ($f_{IF} = |f_{RF} - 2 \times f_{LO}|$, $f_{RF} \approx f_{LO}/2$) is extracted via a lowpass filter.

Since the conventional subharmonic resistive mixers are based on two FETs in a parallel configuration, a balun is needed in order to apply two out of phase signals to the gate of the transistors [80, 81]. Instead, the G-FET subharmonic resistive mixer is implemented using only one transistor and the mixer circuit becomes more compact.

4.4.1 Analysis of the mixer conversion efficiency

In this section the conversion efficiency of the mixer is investigated. The gate swing voltage and the incident RF voltage are assumed to be $V_{g,swing} = V_0 cos(\omega_{LO} t)$ and $V^+_{RF} = cos((2\omega_{LO} + \omega_{IF})t)$. Thus

$$R_{DS}(t) = R_{min} + \frac{R_{max} - R_{min}}{\sqrt{1 + \beta(cos(\omega_{LO} t))^2}} \tag{4.2}$$

$$V^-(t) = \Gamma(R_{DS}(t)) cos((2\omega + \omega_{IF})t) \tag{4.3}$$

where $\beta = \beta_0 V_0^2 = (CV_0/qn_0)^2$. This parameter contains device properties as well as the LO swing voltage and it can be used as a figure of merit for the mixer performance. Based on the practical values for the device parameters β can be as high as 100. Fig. 4.6 shows the conversion efficiency versus R_{max}/R_{min} (on-off ratio) for fixed $k = R_{min}/Z_0$ for $\beta = 30$ and 100.

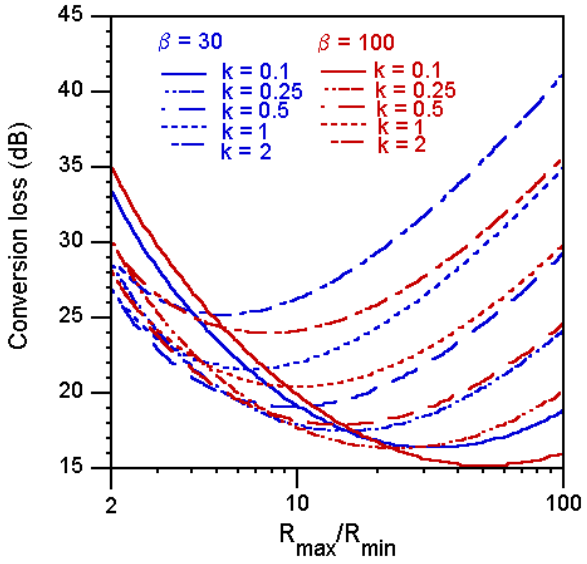

Figure 4.6: CL versus R_{max}/R_{min} for fixed $k = R_{min}/Z_0$ for $\beta = 30$ and 100. All mixing terms generated in the mixer are terminated with the same impedance, Z_0.

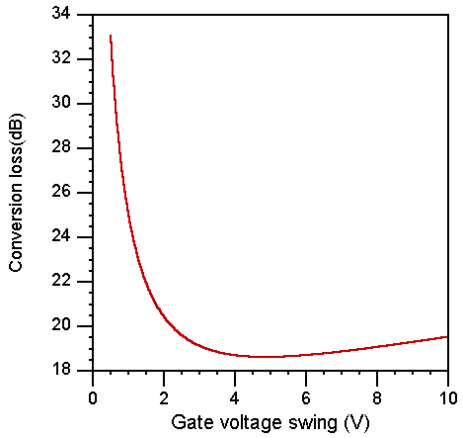

Figure 4.7: CL versus gate voltage swing for $C = 0.22\mu F/cm^2$, $n_0 = 4 \times 10^{11}/cm^2$, $R_{max}/R_{min} = 8$ and $k = R_{min}/Z_0 = 0.5$. All mixing terms generated in the mixer are terminated with the same impedance, Z_0.

As can be seen, for a given $k = R_{min}/Z_0$ and β there is an optimum value for R_{max}/R_{min} in order to obtain minimum CL. Moreover, a higher β gives a lower CL, and the lowest CL can be achieved for simultaneously high R_{max}/R_{min} and low k. For example, in order to reach a CL of 17 dB, $R_{max}/R_{min} \simeq 10$ and $k \simeq 0.3$ are required. In [82], it has been shown that by using graphene nanoribbons, an on-off ratio of 10 at room temperature is achievable. Further simulation shows that by increasing β and R_{max}/R_{min} as well as selecting proper embedding impedances, the CL decreases and saturates to about 14.2 dB. For this type of mixer, the lowest expected conversion loss is about 8 dB higher than the conventional subharmonic resistive FET mixers [80] and this is due to the difference in the waveform of the $\Gamma(t)$. In conventional resistive FET mixers, the $\Gamma(t)$ has a square waveform which gives a sharp transition between Γ_{max} and Γ_{min} and both on and off states have the same time interval. In contrast, a G-FET subharmonic resistive mixer has a smooth transition between Γ_{max} and Γ_{min} and the off state time is shorter than the on state (Fig. 4.5b).

Moreover, in the G-FET resistive subharmonic mixer there is an optimum value for the gate voltage swing, beyond which the CL increases (Fig. 4.7). This is due to the fact that higher gate voltage swing in G-FETs makes the duration of the on and off states more uneven.

The fabricated subharmonic mixer in paper B and the corresponding performance are presented in Fig. 4.8. The simulated CL in Fig. 4.8b is obtained by implementing the developed model in the ADS and applying a harmonic balance analysis. The discrepancy between the measurement and the simulation is attributed to the losses in filters (0.7+0.2 dB), cables and probes (0.2 dB). The experimental spectrum data of the $V^-(t)$ waveform is also depicted in Fig. 4.9. In this mixer $\beta \approx 25$, $R_{min}/Z_0 \approx 1$ and $R_{max}/R_{min} \approx 3$. In order to improve the CL a device with a higher on-off ratio and a higher β as well as a lower R_{min}/Z_0 is required. Lowering n_0 simultaneously increases the on-off ratio and β and by selecting a higher system

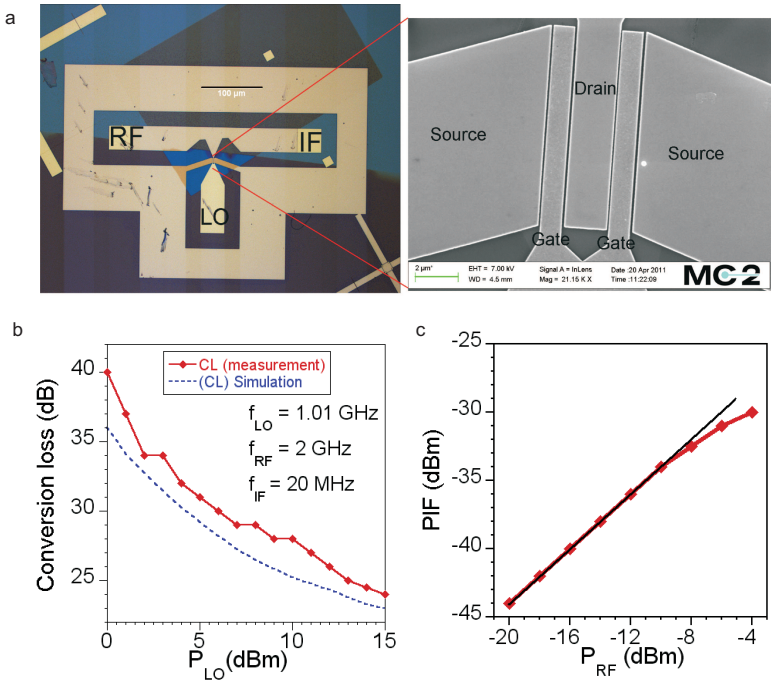

Figure 4.8: a) The fabricated mixer, b) CL versus input LO power and c) CL versus input RF power (IP_3 = -6 dBm).

impedance, R_{min}/Z_0 can be reduced. The required LO power can be reduced by reducing the gate dielectric thickness and optimising the LO source impedance.

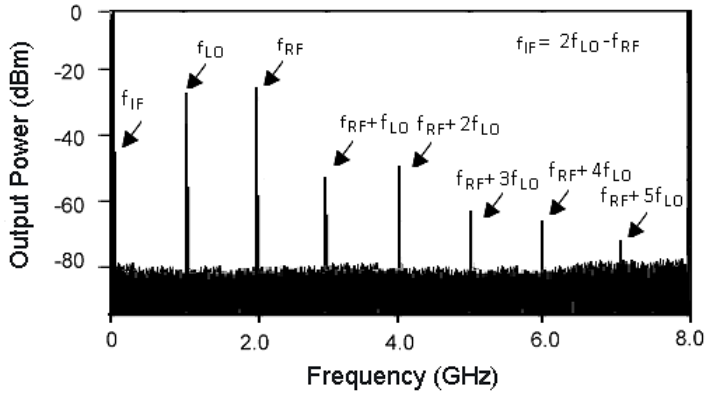

Figure 4.9: Spectrum of the reflected signal, $V^-(t)$ and the LO leakage (P_{LO} = 15 dBm, P_{RF} = -20 dBm, f_{RF} = 2 GHz, f_{LO} = 1.01 GHz).

4.5 Circuits based on unipolar G-FETs

The graphene production method can affect the transfer characteristic of a G-FET by unintentional charging (doping). In some cases such as SiC based graphene, the

unintentional doping is so high that the V_{Dirac} of the fabricated G-FET becomes unreachable [30]. In other words, the G-FET behaves like it is biased far away from the V_{Dirac} (Fig. 4.10). This type of G-FET is called a unipolar G-FET.

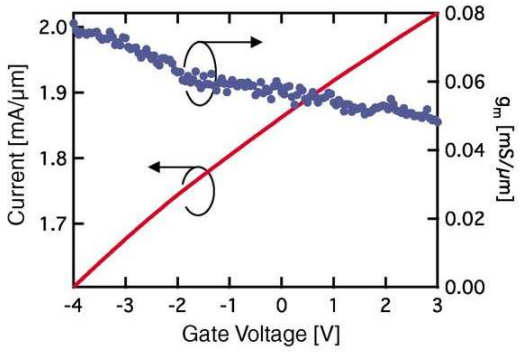

Figure 4.10: Transfer characteristic of a unipolar G-FET, $V_D = 1.6V$ [37].

It can be seen in Fig. 3.8 that by biasing away from the V_{Dirac}, all harmonics quickly decay. Therefore with a unipolar G-FET, a frequency doubler can not be achieved. Moreover, the variation range of the G-FET transconductance decreases substantially when it is biased away from V_{Dirac} (Fig. 3.3). Consequently, a fundamental mixer based on the structure in Fig.4.3 is not achievable. However, a fundamental mixer based on the topology in Fig. 4.4 can be obtained. Since the G-FET is biased away from the V_{Dirac}, by modulating the gate voltage, the drain-source resistance varies with the same frequency as f_{LO}. Consequently, unipolar G-FETs with this topology behave like a fundamental resistive mixer. In [37] such a mixer with 27 dB conversion loss at 4 GHz has been demonstrated.

Chapter 5

Conclusions and future work

In this thesis the goal has been to develop a novel subharmonically pumped resistive mixer based on a single G-FET. This has involved various aspects of device fabrication, modelling and circuit characterisation. Since the performance of the mixer essentially depends on its transistor properties, the G-FET fabrication process has played a key role in this work. Several processing steps have been taken for the mixer realisation, including achievement of a gate dielectric formation process without degradation of the carrier mobility, and development of a low contact resistance as well as a symmetrical transfer characteristic.

The mixer CL has been measured at 2 GHz RF frequency. Further theoretical studies of the mixer performance have shown that by increasing the on-off ratio of the G-FET as well as optimising the embedding impedances, the CL can be improved considerably. Although the ultimate performance of the mixer is lower than that of conventional subharmonic resistive FET mixers, this type of mixer does not need any balun at the LO port allowing it to be more compact. For example, the mixer can be used for the development of compact detector arrays for two dimensional imaging.

Moreover, for analysis and design of G-FET circuits, a large signal G-FET model has been proposed. Different verification methods including DC, S-parameter and power spectrum measurements have been performed to evaluate the model. The model can easily be implemented in standard EDA tools for fast simulations.

Further development of G-FETs is required in order to compete with the mature technology of FETs (HEMT, Si MOSFET). Reducing the contact resistance and creating a bandgap in the G-FET channel are two major steps to realise a G-FET amplifier as well as high performance mixers and frequency doublers. Also, the mobility degradation caused by the substrate indicates the importance of substrate choice for graphene devices. Although by using a single crystal hexagonal boron nitride (h-BN) as a substrate the effect of the substrate can be reduced [53], a wafer-scale single crystal h-BN is still not available. Moreover, the noise performance of G-FETs has not been reported yet. By knowing the noise figure of G-FETs, a more complete characterisation and prediction of G-FETs performance can be provided. Finally, measuring the equivalent input noise of the mixer gives a better assessment

of the mixer performance.

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