EMI from Switched Converters – Simulation Methods and Reduction Techniques

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To those who believed...

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Abstract

In this thesis, the conducted EMI from switched power converters has been analyzed using various existing models, own-derived models as well as measurements. The ingoing passive components in a switching converter have been modeled with respect to their high frequency behavior and the static and dynamic behavior of the active semiconductors has been analyzed. To understand the origin of EMI, the sources of EMI within a switching converter are investigated and measures how to reduce conducted emissions are analyzed. Once the background theory is known, all models of the ingoing components are verified as standalone units; i.e. the high frequency behavior of resistors, inductors, capacitors, printed circuit boards and relevant semiconductors are presented. The verified components are then put together to complete converters from which the emission levels are analyzed. As a measure to reduce EMI directly at the source, a new method of reducing EMI referred to as active gate control is investigated. The principle aims at reducing the high frequency content in the otherwise sharp voltage and current transitions by controlling the gate voltage during a switching event.

It has been found that many component models are insufficient for the purpose of EMI simulations; e.g. is the diode model in the widespread electric simulator SPICE unsuitable due to snappy reverse recovery behavior. Other simulation languages such as Simplorer and SABER® have solved this by incorporating more advanced diode models with adequate reverse recovery behavior that can be adapted to different diodes by more or less advanced parameter extraction procedures. Regarding MOSFET models, the black-box models provided by manufacturers have shown to exhibit good static and dynamic performance which in general makes them suitable for analysis of switching applications. Most analyzed IGBT models showed incorrect switching times and the most suitable model found in this thesis is the Simplorer model that requires more than 100 hand-tuned elements to show sufficient switching performance.

When a complete converter is to be simulated, it is concluded that it is essential to include parasitic elements (e.g. stray inductances and capacitances in the PCB and in the components) in the simulations to obtain correct switching behavior. By such a consideration by e.g. Ansoft Q3d that determine the parasitic elements within a PCB, the often unwanted oscillations in the circuit can be determined to a large extent. However, the conducted emission levels are not just determined by

stray elements and it has been has been shown both experimentally and in simulations that the levels are strongly determined by the mutual couplings in the input filter. The need for a diode model with correct reverse recovery behavior was shown to be important since the reverse recovery event affects the conducted EMI in the frequency region of $5 - 30MHz$. The connection between reverse recovery current and emission levels has been verified in simulations and measurements for two different types of converter topologies.

The derived strategy of active gate control was verified both theoretically and by measurements that establish the operation principle. The method was shown to give a reduction in the conducted EMI of a MOSFET switching circuit and the most suitable unit to control was found to be the drain current. Finally, a reduced-order MOSFET model was shown to be sufficiently accurate to model static as well as switching applications due to its thorough characterization of the gate-drain capacitance as a function of applied voltages.

Index Terms: Semiconductor device measurements, semiconductor device modeling, diode modeling, diode reverse recovery, EMI, conducted emissions, DC/DC converters, state space methods.

Acknowledgements

Contents

Chapter 1

Introduction

1.1   Problem Background

Power electronic converters can be found wherever there is a need to modify the properties of electrical energy, i.e. voltages, currents or frequencies. The area of application ranges over a wide span such as point-of-load supplies on computer motherboards, traction control for electric drives and connection of windpower plants to the grid. One trend in the automotive industry is that objects that originally were mechanically operated are being replaced by electronically controlled ones. These electrical loads often demand variable power at a varying voltage level; hence DC/DC converters and AC/DC inverters are employed. The trend of employing multiple switched converters can also be applied to the server and telecom industry, not due to the plentiful occurrence of mechanical loads, but rather to the high demand of multiple voltages that supplies processors and other consumers. Another aspect that emphasizes the importance of reduced electromagnetic interference from switched converters is the aspect of area and volume. In e.g. the automotive industry, all locations where electronic equipment can be placed are often strictly predetermined due to the restricted volume that all components have to coexist within. Since a switched converter often carry high currents and utilizes large magnetic and inductive components, it may act as a source of disturbance to sensitive equipment located nearby. Due to the aspect of limited volume, the work in this has been focused on methods and means to reduce EMI from a switched converter without adding extra filtering or shielding. Hence, a new method to reduce EMI directly at the source is proposed by directly attacking the high derivatives that occur in a converter.

The perhaps most important incitement for the increased concern of EMI is the relatively new EMC Directive, 2004/108/EC, that is valid from July 2007 within the entire EU. It is by some considered as one of the most comprehensive standards ever to originate from the European Commission and consists of directives that govern both the electromagnetic emission and immunity of a

device. The levels are governed by standards (CISPR and IEC) and cover several different areas e.g. CISPR 25 (Vehicles, boats and internal combustion engines - Radio disturbance characteristics) which is directly used by several large automotive companies. In addition to ensure equipment functionality, the EC directive 2004/40/EC aims at protecting workers from adverse health effects resulting from exposure to non ionizing electromagnetic fields. The directive contains minimum requirements concerning electromagnetic fields that an employer must fulfill; this certainly affects the automotive industry and gives another incentive to keep electromagnetic disturbances as low as possible. All in all, these new directives in combination with the growing electrification and increase of converter power density are the major reason for investigating new methods that can minimize EMI from switched DC/DC converters.

To facilitate the design process of a new product it is often of paramount importance to be able to simulate the design before it is being tested as a prototype. This has not been the case for the prediction of the electromagnetic emissions from a device and the reasons for omission have often been numerous; lack of knowledge how to simulate EMI, insufficiency in the electric simulator tools and a least but not last the complex nature of a switched converter. In order to be able to simulate a more adequate EMI signature, a multi domain simulation tool is needed where different simulators, e.g. electric circuits and FEM calculations can be connected together. This feature has been developed during the last year and as a new emerging technology it gives new possibilities, in this thesis multi domain simulation tools have been applied on switched converters to form a more covering scope of how to predict EMI issues.

1.2   Literature overview

The first topic that needs to be considered when the EMI from a switched converter is investigated is the point of generation. The major sources of EMI from a switched converter are well known and an extensive study is presented in [1]. To be able to quantify how much each of these sources contribute to the total EMI and to facilitate the design process, proper simulation tools are needed and numerous studies of how to simulate EMI from a switched converter have previously been performed. The first category of simulations is the electrical circuit simulators that are based on analytical approximations of the parasitic element [2-5]. In general, these models shows discrepancies between simulation results and measurements for higher frequencies and the versatility is drastically reduced due to difficulties in determining the parasitic capacitances in the circuit. A more general approach for simulating EMI is proposed in [6, 7] where an EMI prediction tool based on approximating the switching event is implemented. By finding the correct current and voltage derivatives during the switching event, the EMI noise can be reconstructed. The major deficit is that it only can be quantified

once the switching event is known in detail. Regarding field simulations, full 3D models based on the finite difference time-domain (FDTD) have been investigated in [8] but with lack of the converter that generate EMI and in [9] that investigate FDTD co-simulations with SPICE aimed for low power electronics and radiated fields. 3D-simulations with the Partial Element Equivalent Circuit (PEEC) method have also been investigated in [10] but with lacking integration of electric circuit models. Other methods simulating the electric fields have also been proposed in e.g. [11] where the stray parameters are extracted from a PEEC-program and [12] where a completely new programs has been developed. These methods are often based on several simplifications and do not show any good possibilities to be reused for different applications which make their versatility limited. A comprehensive study of how parasitics with a converter can be modeled is presented in [13] where both circuit simulations are supplemented with PEEC-simulations, but without the advantage to co-simulate both environments.

The effect of electric and magnetic fields from a converter and component placement has been investigated in e.g. [14] that analyzed where the highest electric fields are located but without any quantification on how it impacts EMI performance. The work regarding mutual couplings can be divided into to two major branches where the first branch focuses on letting the mutual couplings interact in a positive way so that they improve filter performance. The analysis have either been lacking a system aspect [15-17] or been based on numerical approximations of the parasitic elements [18, 19]. The second field of investigation is how mutual couplings affect conducted emissions and filter performance directly [20, 21] but without analyzing a total system performance. Perhaps the most extensive and thorough investigation is found in [22] where the influence of mutual couplings on conducted emissions has been investigated with good results. The analysis have however been focused on low power devices and no quantification of the different mutual couplings has been made which motivate the analysis performed in this thesis.

Several different approaches to reduce the EMI by controlling the gate signal have been studied but none have been aimed at controlling the entire transition. Methods of gate driving have been studied where an intermediate gate voltage slightly over the threshold voltage is applied to the gate terminal during the switching event. The technique require simple control and claims to lower EMI due to reduced dv/dt and also reduce the switching losses [23, 24]. A similar approach is to apply different sizes of gate resistors during different phases of the turn-on and turn-off process respectively which reduces the di/dt [25]. The closest technique that resembles the proposed technique with active gate control is the two-stage method [26, 27] where the di/dt of the transistor current is controlled by an external current generator. Developments of this method with more advanced control strategies have been presented in [28] and [29].

Several other measures of EMI reduction techniques can also be used like snubbers [30], random switching [31] and interleaving of converters [32]. However, a well designed converter can to some extent reduce the need of these additional measures which the main goal with this thesis. This aim has become even more relevant during the last year when a new possibility has opened for electric simulators to in an elementary way co-simulate the functionality of an electric circuit with other domains such as electric field calculations and even take temperature effects into account.

1.3   Purpose of the Thesis

As stated above, various areas of EMI from switched converters have been a target for investigation under a long time. The general objectives of this thesis can be divided into two major parts; to analyze a new strategy of how EMI can be reduced directly at the source and to analyze, simulate and validate the mechanisms of low frequency EMI generation in a switched converter both on component and system level. The purpose can be summarized as follows:

- Analyze ways to reduce the EMI from a switched converter by attacking the cause of harmonics directly at the source. The proposed way to do this in this thesis is to control the voltage and current derivatives in an advantageous way so that the harmonic content is reduced. By doing this, use of additional components such as extra filtering, shielding and snubber circuits is reduced.

- Establish suitable models for the ingoing components in a switched converter. The models shall be valid for all operation points and account for both correct high frequency behavior and temperature effects where found necessary. Most important of all shall the model be easy to parameterize which shall make the results reproducible and widely applicable to different types on converters.

- Quantify which types of components and design methods that can be used in order to enhance the EMI performance of a drive system. All ingoing components and are analyzed with respect to EMI performance and a quantification is made where different components are favorable to use.

- Make comparative studies of how different parameters affect the EMI performance on a switched converter. Once the most suitable components are selected, the parasitic properties still contribute to the total EMI signature, but with a quantification of how the different parameters affect the total EMI signature, even more enhancements can be made.

- Analyze the temperature behavior of the ingoing components and ensure that the developed models correspond well to the simulations. Once the temperature behavior is established, the effect of the changes in the characteristics is analyzed with respect both to switching behavior and EMI signature.

1.4 Contributions with Present Work

Due to the wide range of topics in this thesis, most contributions relate to comparative studies that quantify differences between the components that are used in a modern switched converter and how these differences can be used to reduce EMI levels. To the best knowledge of the author the contributions are summarized as follows.

- A strongly reduced MOSFET model in the state-space form intended for usage in the derivation process of active gate control has been developed. The static (e.g. output characteristics) and dynamic behavior (e.g. switching characteristics) of the model has been verified against measurements and a detailed SPICE model of the same component provided by the same manufacturer.

- Quantification of the changes in gate-drain capacitance in a MOSFET during a switching event both by measurements and simulations. Also, the importance of the gate-drain capacitance magnitude to obtain a correct switching event is determined.

- Experimental and theoretical implementation of active gate control to reduce the emissions in a switched converter. Both the drain-source voltage and the drain current of a MOSFET were analyzed and controlled and where the drain current was found to be more straightforward to control via a current feedback loop. The controller parameters for the implementation were found using the previously derived MOSFET state-space model.

- The reverse recovery behavior of different diodes has been investigated and verified against both simulations and measurements with good agreement. To obtain this, many different diode models have been analyzed where the one found in Simplorer has the most comprehensive coverage of the recovery phenomenon.

- Quantification of the importance of diode reverse recovery with respect to conducted emissions. Different diodes with different recovery behavior have been simulated where it is found that the reverse recovery event

affects the conducted emissions. The models were verified by analyzing the conducted emissions from two different converters (step-down and flyback) which verified the connection between reverse recovery and increased emission levels.

- Demonstrating the dynamic behavior and performing an accurate analysis of the ingoing components in a switching converter. Passive components such as resistors and capacitors have been analyzed and their high frequency behavior has been modeled and simulated. Many semiconductor models available on the market have been analyzed and both advantages and deficiencies have been pointed out for the different models.

- The importance of using an adequate PCB model when predicting the conducted emissions in a switched converter has been demonstrated. This was done by implementing a 60W step down converter into Ansoft Q3D and co-simulating with an electric circuit software to obtain correct quantification of the ingoing parasitic elements.

- Determination and analysis of the mutual couplings for the ingoing components in a switching converter. The mutual coupling have been identified and implemented as a part of the complete converter modeling and the result points out that the mutual couplings must be taken into account if correct EMI levels are needed.

- Complete converter modeling (converter including input filter) with multi domain simulation software. The previous work regarding converter modeling that has been identified by the author has either been aimed at electric circuit simulations, FEM-calculations, the input and output filter, or a small part of a converter. This thesis aims to quantify the importance of including parasitic elements as well as mutual couplings in the input filter when the conducted emission levels are to be simulated.

1.5   Outline of Thesis

The thesis starts with a background investigation of how all ingoing components in a switching converter can be modeled with respect to high frequency behavior and EMI. After that, a literature study of present work within both the field of switched converter modeling and the field of how to predict correct EMI behavior is presented. Also, a short overview of the causes of EMI within a switching converter and measures how to reduce disturbances is presented. Once the background theory is known, all models of the ingoing components are verified as standalone units; i.e. verifications of the high frequency behavior of resistors, inductors, capacitors, PCB traces and relevant semiconductors are presented. A

new method of reducing EMI from a switched converter referred to as active gate control is investigated with both relevant background theory and measurements that verify the operation principle. The last chapter summarizes the previous analysis and of single components and investigate principles of how components interact, e.g. mutual couplings and how it affects filter performance. Furthermore, different complete converters act as a base to verify the previously stated theories.

1.6   Publications

The publications originating from this thesis can be found in Appendix A and are summarized below.

I J. Paixão, A. Karvonen, J. Åström, T. Tuveson, and T. Thiringer, "EMI Reduction Using Symmetrical Switching and Capacitor Control" published at 2008 Asia-Pacific Symposium on Electromagnetic Compatibility in conjunction with the 19th Intern. Zurich Symposium on Electromagnetic Compatibility, Singapore, 2008.

II A. Karvonen, H. Holst, T. Tuveson, T. Thiringer, and P. Futane, "Reduction of EMI in SwitchedMode Converters by Shaped Pulse Transitions" published at SAEWorld Conference 2007. Detroit, Michigan, USA. Copyright SAE International, 2007.

A. Karvonen, "MOSFET Modeling Aimed at Minimizing EMI in Switched DC/DC Converters Using Active Gate Control," Institutionen för energi och miljö, Elteknik, Chalmers tekniska högskola, 2009.

A. Karvonen and T. Thiringer, "MOSFET Modeling Adapted for Switched Applications Using a State-Space Approach and Internal Capacitance Characterization " in PEDS 2009 - The Eighth International Conference on Power Electronics and Drive Systems, Taipei, Taiwan, R.O.C, 2009.

A. Karvonen and T. Thiringer, "On Dynamic Diode Characteristics and EMI Performance of an Inverter with Undeland Snubber," presented at: The 9th International Power and Energy Conference, Singapore, 2010.

A. Karvonen and J. Åström, "Simulating the EMI Characteristics of Step-Down DC/DC Converters," presented at the VPPC'2011, Chicago, IL, USA, 2011.

A. Karvonen and T. Thiringer, "Simulating the EMI Characteristics of Flyback DC/DC Converters," presented at the Intelec 2011, Amsterdam, Netherlands, 2011.

Chapter 1 - Introduction

Chapter 2

Converter Components and Behavioral Models

2.1 Passive Components

2.1.1 Wires and PCB Tracks

The conductors of a system are frequently overlooked being a part of a system since they often are assumed to be ideal connectors. If a wire carrying a high frequency current is considered, the current tends to crowd closer to the outer periphery, a phenomena known as skin effect. When the skin depth (δ) is less than the radius of a wire, it can be calculated as

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \tag{2.1}$$

where μ_0 is the permeability and σ is the conductivity of the conductor ($5.96 \cdot 10^7 \text{S/m}$ for copper). For a circular copper wire excited with a 100 kHz current, the skin depth becomes 0.21mm which means that a high frequency current can only utilize a small fraction of the available conductor. If the wire is operating in the skin-effect region, the resistance can be calculated as

$$R_{(HF)} = \frac{1}{\sqrt{2r}} \sqrt{\frac{\mu_0}{\pi \sigma}} \sqrt{f} \tag{2.2}$$

where r is the radius of the wire and f is the excited frequency. For a rectangular PCB-trace it is shown that when the skin depth (δ) becomes significant at $\delta \cong h/2$, the current crowds uniformly round the edges of the track [33] which gives that (2.2) can be simplified to

$$R_{\text{HF}} = \frac{1}{2\sigma\delta(w + h)} \tag{2.3}$$

where σ is the conductivity of the conductor and w and h is the width and height of the PCB trace respectively.

For frequencies that concern EMI, the inductance of a conductor is often considerably more important than the resistance. The inductance of a wire can be divided into two parts; a frequency dependent internal inductance (50nH/m for low frequencies without influence from the skin effect [33]) due to storage of magnetic energy within the conductor and an external inductance due to the external flux created by the current in the conductor. As for the resistance, the internal inductance of a wire due to magnetic flux within the conductor becomes frequency dependent because of the skin effect. The current crowds towards the surface of the wire and hence the magnetic flux internally in the wire decreases toward zero as the frequency increases. The internal inductance is often relatively small compared with the external partial and mutual inductance which makes it reasonable to neglect in most cases [34].

The external inductance of a wire that comes from external magnetic fields is usually referred to as the partial inductance and can in turn be divided into two parts; self and mutual inductance. The partial self inductance comes from one segment of a wire due to external fields and for a straight length of a round section wire at high frequencies is can be expressed as

$$L_{\text{p(self)}} = \frac{\mu_0}{2\pi} l \left[\ln\left(\frac{2l}{r}\right) - 1 \right] \ \ [\text{H/m}] \qquad (2.4)$$

where l is the length of the wire and r is the radius [35]. The self inductance of a normal connecting wire can be said to be 10nH/cm [33, 36] since the diameter of the wire affects the inductance only marginally. The mutual inductance arise due to interaction with the return current and if it needs to be considered, the geometry becomes important and the equations significantly more complex. An extensive explanation of the partial inductance concept can be found in [33].

The same reasoning regarding internal and external inductance can also be applied for PCB-tracks. The calculation of internal inductance becomes significantly more difficult for a rectangular cross section, but since it once again is very small compared to the partial inductance it usually can be neglected. The external DC inductance of a PCB-track depends on the return path of the current; for a microstrip it can be calculated as

$$L = 0.2l \left[\ln\left(\frac{2l}{w+h}\right) + 0.2235\left(\frac{w+h}{l}\right) + 0.5 \right] \ \ [\text{nH}] \qquad (2.5)$$

where l is the length of the microstrip, w is the width and h is the height over the ground plane [37]. As the equation tells, the inductance decreases as the width

increases and is almost directly proportional to the length of the strip.

If a conductor carries a sufficiently high frequency signal, it can no longer be treated as a simple conductor but must instead be treated as a transmission line; a rule of thumb states that when the wavelength of the highest frequency carried is less than ten times its physical length ($L > \lambda/10$), transmission line theory must be considered. For a printed circuit board, the signal integrity is often discussed in terms of transmission lines where the conduction path usually consists of a microstrip or stripline. For a 30MHz signal traveling on a FR4 substrate, an inner layer conductor longer than 40cm needs to be considered as a transmission line. Transmission line theory is more aimed at high speed digital design and therefore not so applicable to the switching circuits investigated in this thesis. The interested reader can find an extensive explanation of how transmission line theory affects PCB design in [33, 35, 38].

In addition to PCB-parasitics, the package parasitics of a component also needs to be taken into account. Semiconductor manufacturers often state a well measured value for the lead inductance and resistance in their datasheets that works well for EMI-simulations, but the influence of skin-effect is often neglected in the given values. The package resistance has been shown to increase significantly with frequency and the package inductance will decrease due to the skin effect phenomenon. This phenomenon becomes even more significant for packages that attach the die with wire bonds (e.g. TO-220) where the package resistance can vary as much as 100% for a frequency increase from 500kHz to 4MHz [39]. The best way to reduce package inductance is to use flip-chip technology which connects semiconductor chips to external circuitry with solder bumps deposited directly onto the chip pads instead of traditional bond wires.

Even vias needs to be considered if correct high-frequency behavior of a PCB is needed. A significant amount of current can flow through via holes, especially high frequency currents from bypass capacitors, which give that parasitic effects may affect the behavior. The parasitic inductance of a via is based on its length and diameter and can be calculated as

$$L_{\text{via}} = 0.129h \left[\ln\left(\frac{4h}{d}\right) + 1 \right] \; [\text{nH}] \tag{2.6}$$

where h is the height of the via and d is the diameter of the via in meters. The parasitic capacitance of a via is based on its length and the diameter of the pad surrounding the via and can be calculated as

$$C_{\text{via}} = \frac{55.5\varepsilon_{\text{r}}hd_{\text{p}}}{d_{\text{c}} - d_{\text{p}}} \; [\text{pF}] \tag{2.7}$$

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where h is the height of the via, ε_r is the dielectric constant of the surrounding material, d_p is the diameter of the pad surrounding the holes and d_c is the diameter of the clearance hole. For EMI-modeling purposes, it can be sufficient to only consider the series inductance of the via, but if the via is carrying a high speed digital signal, a π-model with a series inductance and capacitors to ground on either side gives a more correct representation [40].

2.1.2 Resistive Components

The ideal frequency response of a resistor has a magnitude equal to the value of the resistor and a phase angle of 0º for all frequencies. However, for an actual resistor the impedance will vary with frequency mainly due to the physical properties of the resistor. The origin of parasitics mainly lie in the construction of the resistor; a through-hole mount component shows both inductance and capacitance due to the leads attached to the component, see Figure 2.1 for an equivalent circuit and bode plot. For a 0.125W through-hole mounted resistor with 2cm lead length and 5mm lead spacing, the lead inductance is typically $L_{lead} \approx 15nH$ and the lead capacitance is $C_{lead} \approx 1pF$. The bridging capacitance from end-to-end due to charge leakage around the resistor body is usually larger than the capacitive coupling between the leads, a reasonable estimation is that the total parasitic capacitance lies in the magnitude of $1pF$ which makes it reasonable to neglect in many cases [33].
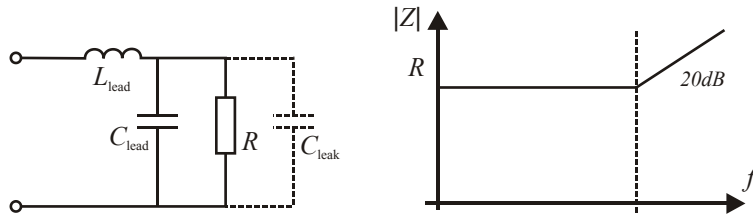
Fig. 2.1:   The nonideal resistor including effects of the leads.

Even for a surface mounted component with infinitesimally small contact electrodes, a parasitic capacitance within the resistive layer remains due to the potential drop and the field lines in the surrounding air. The parasitic self-capacitance and inductance for surface mounted resistors (size 2512 and smaller) are relatively small and lies in the range of hundreds of femtofarads [41, 42] and may therefore be neglected for the EMI simulation purposes in this thesis.

2.1.3 Capacitive components

There are many types of capacitors available on the market today, but in general are tantalum electrolytic and ceramic capacitors used for EMI suppression and aluminum electrolytes used for energy storage in low voltage applications. Ceramic capacitors have traditionally been modeled as a series RLC network

where the capacitor is described in terms of its capacitance, equivalent series resistance (ESR) and equivalent series inductance (ESL). This model works well for low frequency cases since the resistive element changes moderately with frequency and usually shows a minimum near the self-resonant point. The capacitance and ESL change is also very small at frequencies below self-resonance [43]. These assumptions work well for moderately high ESR capacitors with a low Q and when a capacitor is mounted on pads that dominate the ESL. But as the frequency goes up, the inductance associated with the height of the capacitor causes current to closer to the connectors, i.e. lower down in the capacitor. A smaller part of the capacitor carries most of the current which results in higher ESR. The current stays closer to the return current in PCB power planes leading to lower inductance. The Q of the capacitor and the anti–resonant peak is reduced at high frequencies by this effect. A distributed circuit SPICE model, captures this effect [44] and variants of this model is used by manufacturers such as Kemet and Murata, see Figure 2.2 for the Kemet SPICE model.
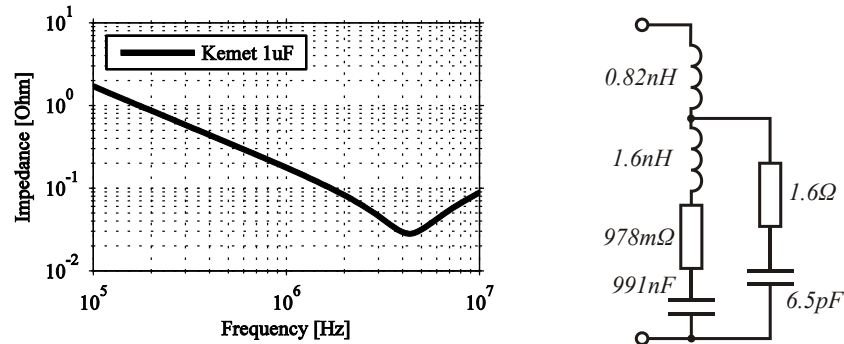
Fig. 2.2: A nonideal ceramic capacitor model with corresponding impedance as function of frequency for Kemet C1210C105K3RAC.

The capacitance of a tantalum capacitor usually shows a large frequency variation; a decay of 20% of decade per frequency is common. The electrode that penetrates the tantalum block within the capacitor have limited width but must yet penetrate to the center of the capacitor to electrically connect the deepest capacitive elements. The deeper the penetration, the higher becomes the resistance of that path. As frequency increases, the period for each capacitor element to respond and contribute to the total capacitance decreases; starting at the center and working out towards the surface, more and more capacitive elements are unable to make any contribution to the total capacitance. This electrical presentation of this phenomenon can be seen in Figure 2.3 where the capacitance increases with increasing resistance. The capacitance available to the circuit at higher frequency is all located near the outer surface of the anode [43]. A similar approach where the capacitance roll-off is implemented by exponentially decreasing the capacitance together with a constant resistance value seems to work well also for aluminum electrolytic capacitors [45].
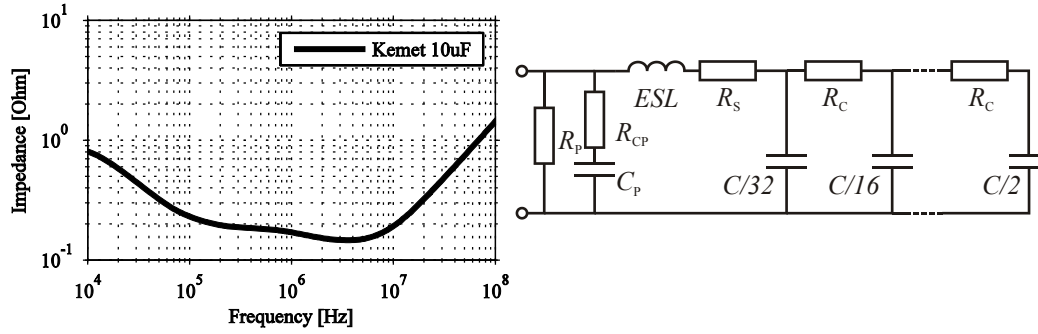
Fig. 2.3: A nonideal tantalum capacitor model with corresponding impedance as function of frequency for Kemet T494D106M035AT [43].

2.1.4 Inductive components

The parasitic components of an inductor are more complex than the ones for a capacitor due to its relatively complex design with many parasitic elements. Inductors are generally made by winding a wire around a magnetically permeable material and it is the performance of the magnetic material, along with the DC-resistance of the wire and the stray capacitance caused by the winding technique that determines the overall performance of the component. A simplified equivalent circuit of the inductor can be seen in Figure 2.4.
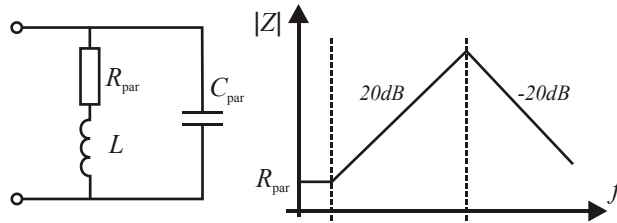
Fig. 2.4: A simplified equivalent circuit of an inductor.

Several studies of different inductor modeling aspects have been performed, e.g. has the frequency dependent losses been analyzed with a Jiles-Atherton model in [46, 47], the leakage inductance in [48] and the self capacitance of the windings in [49, 50]. From an EMI point of view, the most interesting work is performed in [51, 52] which in combination with a Jiles-Atherton model gives a comprehensive coverage of all aspects of a magnetic component.

Tihanyi [53] states that for a switched converter with a transformer, one of the primary sources of harmonics in the output are the stray component in a transformer; an equivalent circuit is shown in Figure 2.5. The interwinding capacitance, C_W, can cause common mode emissions and can be decreased by applying a faraday shield between the windings, see Figure 2.5. The intrawinding capacitances, C_P and C_S, are small and can in some cases be neglected. The last

parameter that needs to be accounted for is the leakage inductance of the primary and secondary winding, $L_{\lambda P}$ and $L_{\lambda S}$, respectively, which create a magnetic field between the windings. While some of this field is captured by the core, the rest acts as a magnetic dipole radiating out into surrounding space and may induce disturbances on nearby components. Examples of techniques for reducing the leakage inductance is interleaving the windings or by applying a conductive flux strap that provides a path for the eddy currents that result from the leakage inductance.
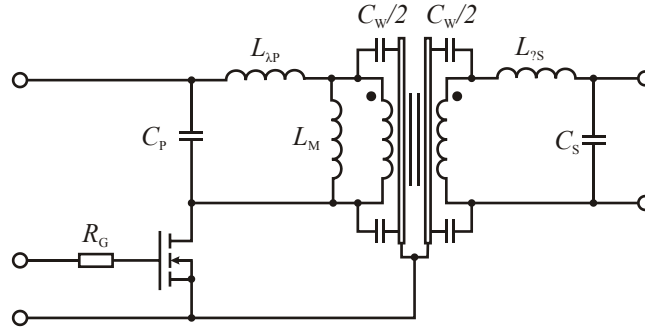
Fig. 2.5:   Equivalent circuit of a transformer.

Another parameter that in some cases must be accounted for is ferrite core stray capacitance that for lower frequencies can become a significant part of total stray capacitance. Hence, the winding arrangement may not play a significant part in low frequency common mode current generation but it may rather originate from the ferrite core stray capacitance [54].

In many modern converters, the use of planar transformers becomes more and more common due to three reasons; the possibility of achieving high power density, repeatable parameters from a production point of view and lowered leakage inductances. The leakage inductances are reduced by interleaving the primary and secondary layers so that the stray magnetic flux induced by the eddy currents is canceled [55]. However, a planar transformer has the disadvantage of increased intrawinding parasitic capacitances and increased interwinding capacitance. The increase of these capacitances gives rise to higher differential mode and common mode noise magnitude, respectively, as shown in [56].In addition to this, planar technology gives the possibility of integrating a complete EMI-filter into one component [57].

2.1.5   Mutual Coupling between Components

The last part that needs to be taken into account in order to obtain a correct EMI-signature is the electromagnetic coupling between the components in the converter. These effects especially raise influence, when parts of a circuit carry high interference levels while parts close by carry low level signals. In case of

filter circuits this condition is valid and magnetic coupling coefficients between components as low as 0.1% already dominates circuit behavior [22].

The electromagnetic coupling between two electrical circuits can be said to originate from either an inductive or a capacitive coupling between the circuits. The effect of induction fields can be minimized by usage of proper spacing and coupling angle between wires; the degree of magnetic coupling diminishes rapidly with distance and the angle between the conductors approach a right angle. In the same way, the strength of the capacitive coupling depends on the geometry between the victim and the source; it is indirectly proportional to the distance between the source and the victim, the geometry of the objects and to the permeability and permittivity of the material between the circuits.

Figure 2.6 illustrates the difference between the two coupling mechanisms applied to two transmission wires, but due to the complex geometries of most real life problems, it is in general hard to determine which coupling mechanism that dominate [33]. However, for some cases it can be obvious which mechanism that dominate, e.g. two large PCB-planes separated by a small distance with a high permittivity dielectric material will give rise to a large parasitic capacitance.
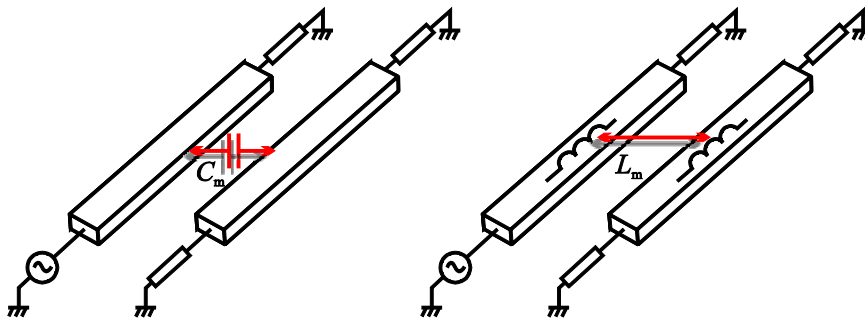
Fig. 2.6: Different forms of cross-talk between wires.

The effect of magnetic and electric field coupling can more accurately be calculated using FEM-calculation software, in this thesis are Maxwell and Q3D from Ansoft used as the primary tools. Figure 2.7 shows an example of a magnetostatic solution of two neighboring DC-excited coils; due to the closeness of the coils, the B-fields will interact with each other. Figure 2.8 shows a similar case but for an electrostatic solution of two DC-excited capacitors. Note that for practical applications, capacitors and conductors can generally be said to be the same from a mutual coupling point of view. Both components often carry high frequency AC-currents which generate a high magnetic field that couples to surrounding components. The external electric fields that are generated by capacitors are generally relatively low and capacitive coupling due to electric fields are more likely to occur between closely located neighboring structures such as PCB planes or heat sinks.
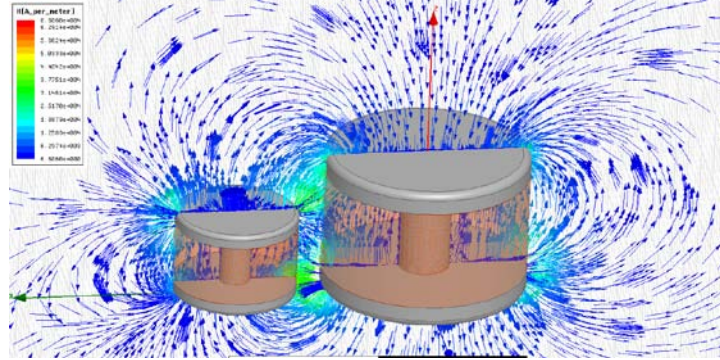
Fig. 2.7:   FEM-visualization of mutual *H*-field coupling between two inductors.
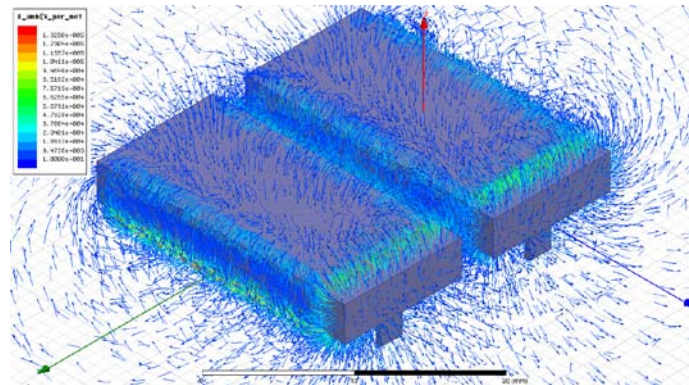
Fig. 2.8:   FEM-visualization of mutual *E*-field coupling between two capacitors.

In order to account for mutual couplings in electric circuit simulation software, it requires on one hand the calculation of the electromagnetic fields within a circuit, and on the other hand circuit simulation based on these values. Since mutual couplings can affect the properties of components, e.g. the inductance of a filter inductor, these effects also needs to be taken into account in the circuit simulation.

2.2   Semiconductors and Materials

Most modern semiconductors are at the point of writing this thesis still manufactured by silicon that has a non-negligible deficit when large powers are to be handled; a considerable wafer thickness is needed to achieve sufficient voltage handling capability. Since the thickness of the semiconducting material is the most important factor that contributes to the overall losses in the device, the possibility to use a thin wafer would strongly evolve power semiconductors even further. Recent research has showed that new materials such as silicon carbide (SiC) and gallium nitride (GaN) has substantially improved material properties in relation to silicon. Recent development has recently made silicon carbide Schottky diodes available on the market and prototypes of both bipolar transistors and field effect transistors have been presented. But due to the relatively early

stage in the development of these materials, several problems must still be mastered before other components can be produced in larger volumes [58].

2.3 The Diode

The simplest form of diode is formed when a p-doped material and an n-doped material is brought together to a pn-junction. Since electrons are moved within the crystal lattice both due to the influence of the applied electric field and due to the charge that is stored in the diode when it is forward biased, the diode can also be seen as a capacitor. The total diode capacitance, C_D, consists of two terms; the depletion capacitance (C_j) and the diffusion capacitance (C_d). The depletion capacitance originates from the accumulation of charges in the space charge region and its varying width and the diffusion capacitance is the capacitance due to transport of charge carriers through the pn-junction when the component is forward biased. [58].

2.3.1 The PiN-Diode

A regular pn-diode is often made of a highly p-doped material and an n-type epitaxial substrate. A highly p-doped material needs lower ionization energy before avalanche breakdown occurs which makes p^+n-junctions more suitable for higher currents since the power losses in the material approximately increases with the square of the device thickness. To overcome the problem with high contact resistance between metallic contacts and lowly doped n-layers, a highly doped n^+-region is added to the structure. When such a device is forward biased, the middle region (n^-) is driven into high injection, i.e. the n^--region becomes flooded with a quasi-neutral mixture of charged particles, a so called plasma; hence the acronym PiN (where i stands for intrinsic).

For a regular pn-junction diode, the voltage drop is equal to the junction voltage which can be regarded as a constant voltage. However, in high power PiN-diodes, this approximation will seriously underestimate the losses since it does not comprise the power dissipation in the drift region. This power dissipation is minimized by conductivity modulation caused by injection of minority carriers in the drift region that lowers the conduction losses. By making the carrier lifetime large enough, the on-state losses can be reduced. However, a long carrier lifetime reduces the switching speed due to the stored charges in the drift region; the characteristics of a PiN-diode are often an optimization between switching speed and on-state losses.

When a PiN -diode is turned on, the forward current starts to increase from zero with a rate of di_F/dt, see Figure 2.9. The current flow causes excess carriers to be injected into the intrinsic region from the n^+n- and p^+n- junctions where they

eventually diffuse into the middle. Initially, the ohmic losses in the intrinsic region are rather large due to the lack of injected excess carriers but as the diffusion process continues, the resistivity diminishes and approaches the value for the steady state current. This increased resistance causes an overshoot in the forward diode voltage usually referred to as forward recovery. Note that the maximum overshoot is dependent on the rate of current increase, di_F/dt; a higher derivative gives a larger overshoot both due to parasitic inductances in the package and to the resistive drop [59].
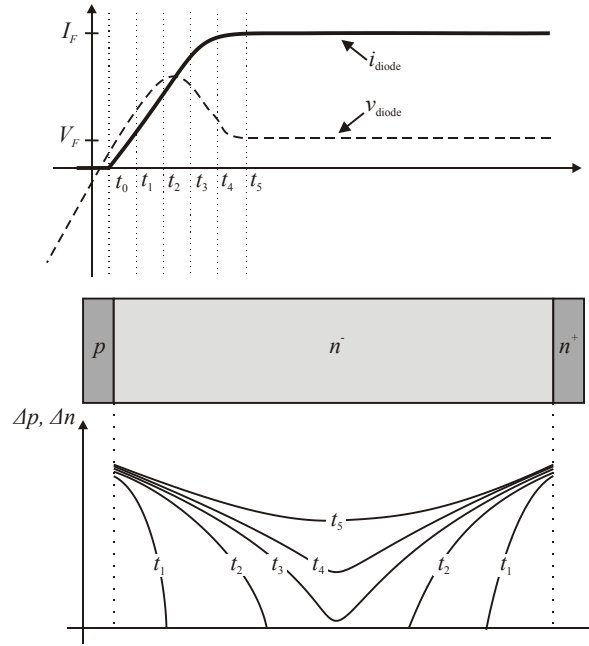
Fig. 2.9:   Turn on-process for a *PiN*-diode.

The transient process during turn-off for a *PiN*-diode that is hard switched (i.e. the diode is used as a freewheeling diode where the current momentarily is switched from the load to the diode) is shown in Figure 2.10. At $t = t_0$, the voltage over the diode changes polarity from forward to negative bias momentarily. During phase 1 (t_0 to t_1) the drop in diode current is very fast which gives that this phase is very short compared with the recombination lifetime. Therefore, as phase 1 is completed and the current crosses zero, the plasma concentration in the intrinsic region is still high.

During phase 2 (t_1 to t_2) the excess carrier concentration in the intrinsic region keeps the diode conducting. The diode current derivative remains constant which gives a small voltage drop over the diode. The reverse current in the diode is supported by sweepout of excess carriers from the intrinsic region. Electrons are swept out via the cathode contact and holes exit via the anode contact which gives a rapid decrease in carrier concentration close to the edges in the n^--region.
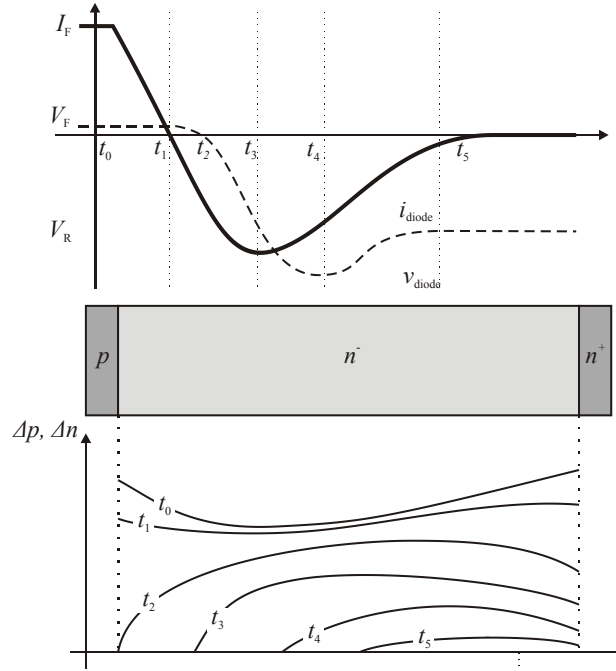
Fig. 2.10: Turn off-process for a *PiN*-diode.

During phase 3 (t_2 to t_3) the plasma concentration falls to zero at the pn^--junction due to the fact that the initial plasma concentration is much lower at the anode than at the cathode. As the plasma concentration falls to zero, a depletion layer starts to form which also supports a voltage. At $t = t_3$, the voltage across the diode reaches V_R and the current derivative reaches zero.

During phase 4 (t_3 to t_4) the plasma concentration continues to decrease. The excess charge carrier concentration at the edges of the space charge region that supports the entire voltage in the diode must consequently also continue to decrease. As a consequence, the reverse current starts to decrease after $t = t_3$. As a reaction to the negative di/dt, the stray inductances in the circuit builds up an electromotive force that results in a voltage overshoot over the diode.

During phase 5 (t_4 to t_5) the depleting plasma in the intrinsic region gives a continued current drop towards zero [58].

2.3.2 The Schottky Diode

The Schottky diode is manufactured by joining a metal and a semiconducting material together, see Figure 2.11. This gives rise to a dipole charge on the surface of the junction and the interface will show a similar behavior as a pn-junction. A Schottky diode is a majority-carrier device since only majority-carriers (most commonly electrons) are used when it conducts. This is a major difference

compared with a regular *pn*-diode since the *pn*-diode uses both majority and minority carriers for the basic function.

A Schottky diode is commonly made by evaporating a suitable metal onto the surface of an nn^+-epitaxial structure. Figure 2.11 shows the physical structure of a Schottky diode with a guard ring that increases the blocking voltage capability. The main purpose of the guard ring is to reduce the curvature of the depletion layer from the metal-semiconductor interface and to widen the space charge region at the semiconductor surface.
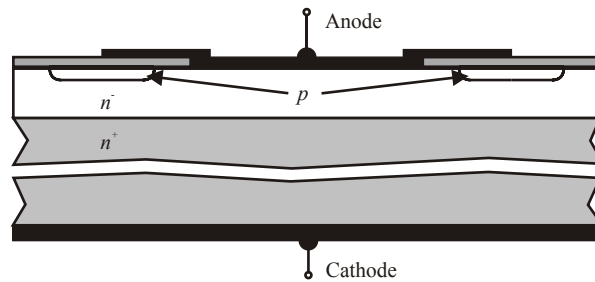
Fig. 2.11: Schematic structure of a Schottky diode with guard ring for higher blocking voltage ability.

The main advantages of power Schottky diode is low forward voltage drop, temperature and good switching characteristics. However, due to material properties of the Schottky structure, the reverse blocking voltage of silicon Schottky diodes are somewhat limited. With proper material selection and field terminations (a *p*-region surrounding the metallic contact) the blocking voltage can reach up to 250V. Also, the reverse leakage current is higher for a silicon Schottky diode compared to a *pn*-diode with the same physical structure [59]. Schottky diodes made of silicon carbide have recently been introduced on the market and several manufacturers now offer SiC Schottky diodes with blocking voltages up to 1200V. The SiC Schottky diode offer good switching characteristics and low thermal influence on its switching characteristics which makes it worth considering in e.g. high temperature applications.

2.3.3 Diode Modeling

The simplest semiconductor modeled in SPICE is the *pn*-junction diode. Originally, it is based on the well known Shockley equation

$$I_{\text{diode}} = I_S \left[exp \left(\frac{V_D}{N \cdot V_t} \right) - 1 \right] \tag{2.8}$$

that describes the current through an ideal diode. In (2.8), I_S is the saturation current, V_D is the applied voltage over the diode and V_t is the thermal voltage. For

adaptation to SPICE, an emission coefficient, N, is introduced to model the ideality of the pn-junction; a high value indicates on a higher rate of recombination of carriers in the depletion layer.

In addition to the description of the current characteristics, a series resistance (RS) is often added. The purpose of the resistance is to model the resistance in the connecting wires, the ohmic contact resistances and the ohmic drop in the quasi neutral regions. In order to obtain a better dynamic model, the diode capacitance is added to the model, see Figure 2.12 for a circuit representation.
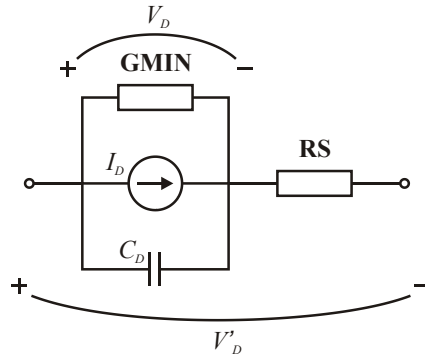
Fig. 2.12: SPICE Diode large signal model with dynamic effects.

As the physical interpretation of the diode capacitance suggests, the total diode capacitance, C_D, can be divided in two parts; the diffusion capacitance, C_d, and the depletion capacitance, C_j. SPICE interprets the depletion capacitance as

$$C_j = \frac{C_j(0)}{\sqrt{1 - \dfrac{v_{applied}}{V_{bi}}}} \tag{2.9}$$

where $V_{applied}$ is the applied junction voltage, $C_j(0)$ is the junction capacitance at zero applied bias and V_{bi} is the built-in voltage which equals the potential difference between the p-material and the n-material at zero bias. The diffusion capacitance is according to Massobrio [60] modeled as

$$C_d = \frac{dQ_d}{dV} = \frac{TT \cdot I_S \cdot e^{\frac{v_{applied}}{N V_T}}}{N \cdot V_T} \tag{2.10}$$

where N is the diode ideality coefficient found in (2.8) and TT is a SPICE parameter that describes the transit time for the carriers. If these two capacitances are plotted for the SPICE model for the diode 32CTQ030, the results in Figure 2.13 is obtained. When the applied voltage becomes positive and approaches the defined value for the diode ($V_{bi} = 1.5V$), the space charge region becomes very

thin which enables a current flow. The applied voltage at which the current starts to flow coincide with the specified forward voltage drop at rated current, $V_F = 0.4V$ @ $I_F = 15A$ according to the manufacturer datasheet. Consequently, the depletion capacitance will be the dominating part under forward bias.
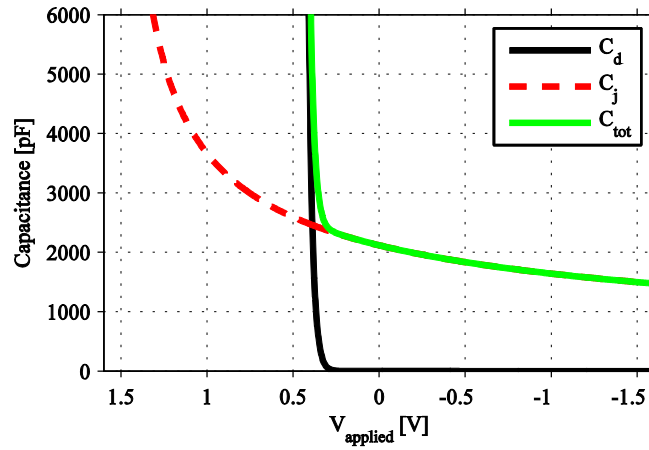
Fig. 2.13:   Internal capacitances as a function of applied voltage for 32CTQ030.

It has been shown in [61] that the excess carrier distribution profile in the vicinity of the pn-junction as the diode is being turned-off depends on the rate of change of the stored charge. If a low dQ/dt is present in the diode, the quasi-static charge equation is adequate since the stored charge in the depletion region also becomes approximately zero as the charge in the node at the interface becomes zero. However, if a high dQ/dt is present, a substantial amount of stored charge still remains in the depletion region even though the charge concentration at the interface has decreased to zero. It is this excess charge that causes the behavior of the reverse recovery current.

Charge storage in the depletion layer is not modeled by SPICE, hence the sudden increase and snappy behavior of the diode current at the moment when the charge node at the interface becomes depleted, see Figure 2.14 for a comparison between SPICE and real turn off behavior.

To summarize, the basic SPICE model provides a good modeling of the static diode behavior but it has two major deficits; it does not take high level injection into consideration and it does not include dynamic effects such as forward and reverse recovery. Numerous more advanced models that take high injection into consideration have been developed, see e.g. [60, 62, 63].
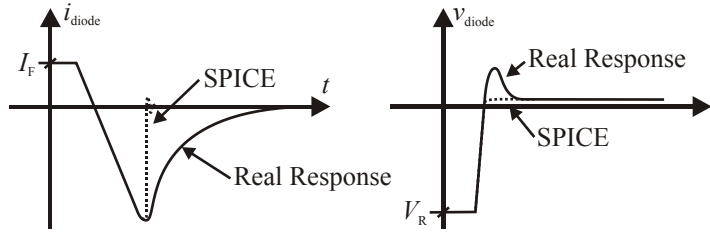
Fig. 2.14: Comparison of typical reverse recovery waveforms from SPICE and a real diode.

Regarding *PiN*-diode modeling, the SPICE diode model becomes even more inadequate due to the intrinsic region. For this reason, several modeling techniques have been proposed over the years, an extensive summary is presented in [64]. As described by Lauritzen and Ma, a model of the *PiN*-diode can be derived using the lumped charge technique [65-67]. In a *PiN*-diode driven into high injection, reverse recovery is caused by diffusion of charge from the *i*-region which can be modeled by additional charge storage nodes. The main deficits with the lumped charge model presented by Lauritzen are the parameter extraction procedure and the possibility of implementation in a circuit simulator.

To overcome this, some of the major simulation software manufacturers, e.g. Synopsys and Ansoft, have developed their own models that incorporate more correct switching characteristics. The diode model incorporated in SABER by Synopsys is presented in [68] and referred to as the unified diode model. The detailed implementation is intellectual property of Synopsys Inc. and not free to distribute, but a complete description of the validation procedures can be found in [69] and for the end user the Power Diode Tool® within the software SABER® Sketch is used for graphical parameter extraction. The last diode model investigated in this thesis is the model in Simplorer. The forward characteristics of the diode is modeled by the Shockley equation and in addition to the static behavior, junction and diffusion capacitance are also taken into account together with an additional current source that accounts for the reverse recovery, see Figure 2.15. The shape of the reverse recovery current is determined by several user defined form factor-parameters [70].

Fig. 2.15: Equivalent diode model in Simplorer.

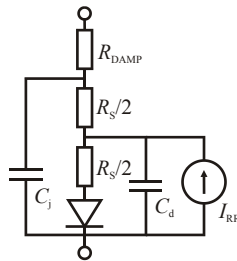### 2.3.4   Modeling of the Schottky Diode

The current through a Schottky diode can in a similar way as the regular pn-diode be modeled with (2.8). The main difference is that the saturation current I_S is not dependent on doping levels and diffusion length as for the pn-diode, but rather on the Schottky barrier voltage. As far as the large-signal model is concerned, the charge storage effects are almost entirely dominated by the depletion capacitance, C_j, see (2.9). The fact that the forward current is characterized by electron emission from the n-type semiconductor into the metal rather than hole injection into the semiconductor results in negligible minority carrier effects, hence can the diffusion capacitance, C_d, be neglected [60].

Even though a model for the Schottky diode is not implemented explicitly in SPICE, it can be simulated sufficiently good with the regular pn-diode model by adjusting the saturation current, IS, and setting $TT = 0$, see (2.8) and (2.10).

2.4   The MOSFET

For switching power electronic applications, the vertically diffused double MOSFET (VDMOS) transistor is exclusively used, see Figure 2.16 that show a n-channel VDMOS device. The geometry lowers the on-state resistance $R_{DS(on)}$, reduces the lateral size of the component and gives the possibility to parallel several elements on the same wafer which lowers the conduction losses even further [58].
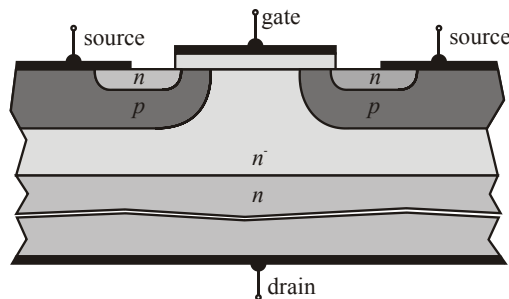
Fig. 2.16:   Schematic structure of a vertically diffused MOSFET

An unwanted feature of the most common MOSFET structure is the presence of a body diode. To reduce the risk of turning on the parasitic BJT-transistor, the metallic source electrode that covers the n^+-region is lengthened to also cover the body region in order to obtain a short-circuited base connector on the BJT. The performance of the body diode is relatively slow compared with the MOSFET and if used in a switched converter it can cause high peak currents during diode turn off [71]. Several measures can be taken in order to improve the performance of the diode and to make it more suitable for switched applications [58, 72, 73].

As the gate-source voltage reaches above the threshold voltage, a strong inversion layer starts to form in the *p*-material which gives a free path for the current to flow from drain to source. The created inversion channel acts like a resistor, i.e. the drain current is proportional to the applied drain voltage. The MOSFET is said to be operating in the linear region; i.e. the drain current is proportional to the applied gate-source voltage. Figure 2.17 shows the current voltage characteristics for an ideal VDMOS transistor.
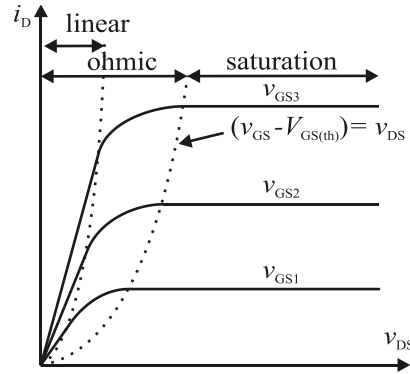
Fig. 2.17:   Output Characteristics of a vertically diffused MOSFET

If the drain-source voltage is increased from a low value, the potential at the drain is no longer negligible compared to the gate voltage. Along the formed channel the voltage potential is successively decreasing. The new reduced potential at the drain end of the channel gives a decreased inversion charge and consequently also a reduced channel width. This reduction in channel width produces the concave curvature in the ohmic region in Figure 2.17.

When the applied voltage at the drain is so large that the inversion layer at the drain end becomes zero ($V_{DS} = V_{GS} - V_{th}$), the so called pinch-off point has been reached. The electron concentration at the drain end of the channel area becomes very low since only a depletion region will exist. Note that the existence of only a depletion region is no barrier to electron flow; the electric field pulls electrons into the drain. If $V_{DS} = V_{GS} - V_{th}$, the MOSFET is operating at the onset of saturation and if the drain-source voltage is increased even further, the MOSFET will operate in the saturated region [74].

2.4.1   Internal Capacitances of the MOSFET

The switching behavior of a power MOSFET is strongly determined by the internal parasitic capacitances that are formed due to internal build-up of charges. The main parasitic capacitors are shown in Figure 2.18 whose values vary strongly with the applied voltages. They depend on different physical properties and can be divided into three major parts.

The gate-source capacitance (C_{GS}) mainly constitutes of two parts. The first part is formed by the capacitive coupling between the gate electrode and the source electrode (C_{PP}). This capacitance is geometry dependent and does not vary with the applied voltages. The second part is voltage dependent and can in turn be divided into three separate subdivisions. The first subdivision is the major contributor and consists of the gate oxide capacitance in the channel region ($C_{channel}$). The second subdivision is the diffusion capacitance in the n^+-region which originates from the gradient in the carrier concentration and depends on the applied voltage. If a change in the junction current is desired, the stored minority carriers close to the space charge region must be removed, hence the name diffusion capacitance. The third subdivision is the spread of the space charge region in the drift region. All constituents are connected in parallel which results in an internal capacitance that does not only vary with the applied gate-source voltage but also with the resulting drain-source voltage.
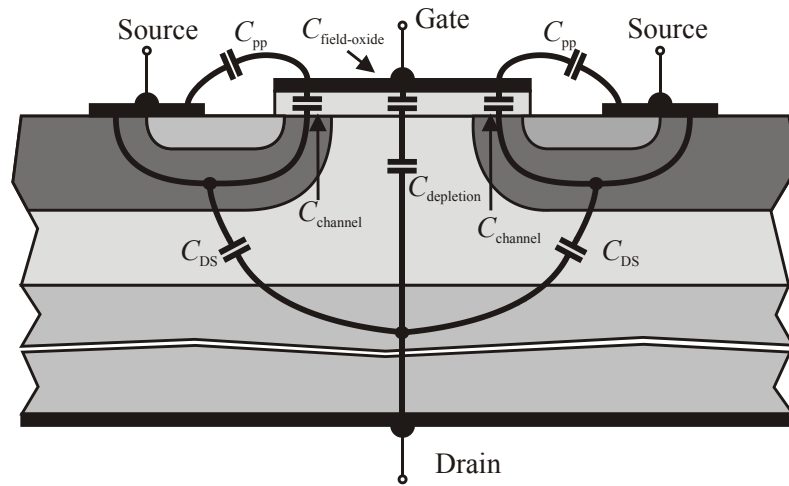
Fig. 2.18:   Internal capacitances in a vertically diffused MOSFET.

The drain-source capacitance (C_{DS}) is independent of the gate voltage, but is dependent on the applied drain-source voltage. It originates from the depletion layer capacitance in the drain-source pn-junction and can be divided into two parts; the depletion capacitance (C_j) and the diffusion capacitance (C_d). However, in the internal MOSFET pn-junction, the diffusion capacitance (C_d) is negligible; hence the drain source capacitance is manly made up of the depletion capacitance (C_j) [75].

The gate-drain capacitance (C_{GD}) is perhaps the most important parameter that determines the switching characteristics of a MOSFET. Simplified, it can be seen as the field oxide capacitance ($C_{field-oxide}$) connected in series with the depletion capacitance ($C_{depletion}$) in the drift region. The depletion capacitance shows a

strong voltage dependence since the drain-gate voltage varies strongly. As long as the MOSFET is turned off, the voltage across gate-drain is high which gives a large depletion layer and consequently a low gate-drain capacitance ($C_{GD} \approx C_{depletion}$). As the MOSFET is turned on and operating in the linear region, the voltage across it is low, an accumulation layer is present under the gate electrode. The gate-drain capacitance is then dominated by the field oxide capacitance ($C_{GD} \approx C_{field\text{-}oxide}$) [58].

2.4.2 Turn-On Behavior of the MOSFET

A common application for a MOSFET is when it switches an inductive load with a freewheeling diode. A typical schematic where a pulsed voltage (v_G) is applied to the gate terminal can be seen in Figure 2.19 together with the turn-on characteristics.
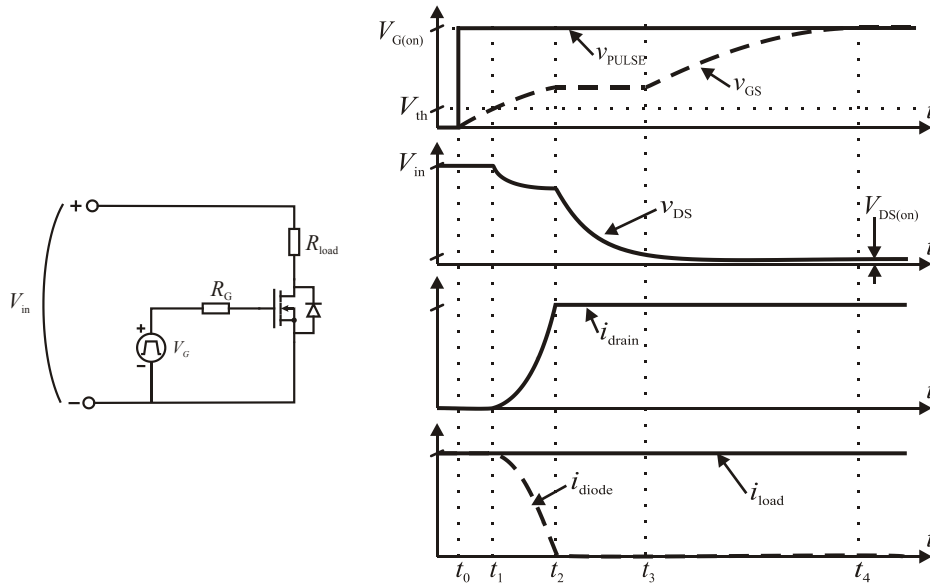
Fig. 2.19: Turn-on diagram of a MOSFET.

At $t = 0$, a positive voltage is applied to the gate terminal. The charging of the internal gate capacitances starts and the gate voltage increase during the interval $t_0 < t < t_1$ can be described according to

$$v_{GS}(t) = V_{GS(on)}\left(1 - exp\left(\frac{-t}{R_G(C_{GS} + C_{GD})}\right)\right) \qquad (2.11)$$

where $v_{G(on)}$ is the applied voltage, R_G is the total gate resistance, and C_{GS} and

28

C_{GD} are the lumped gate-source and gate-drain capacitances respectively.

At $t = t_1$, the gate voltage reaches the threshold level and a drain-source current is starting to build up in the MOSFET. As long as the entire current has not commutated to the diode, it will remain forward biased and carry a current. The commutation will not be over until the current through the MOSFET reaches the inductor current and the diode will become reverse biased. The voltage over the MOSFET will be equal to the sum of the DC resistance voltage and the voltage drop over the stray inductance in the MOSFET. As long as the voltage over drain source is relatively high, the gate-drain capacitance (C_{GD}) will be much smaller than the gate source capacitance (C_{GS}). This means that the voltage over the drain source will not have a significant effect on the gate voltage.

At $t = t_2$, the commutation process is completed and the MOSFET is carrying the total inductor current which results in a plateau on the gate source voltage. The inductor is assumed to be so large that the total current during the turn on process is constant and the diode is assumed to be ideal, i.e. it does not produce any reverse current peak during turn off. The drain current does not increase any further which gives a plateau in the gate-source voltage. This plateau also forces the gate current to only charge the gate drain capacitance. Since the C_{GD} increases with decreasing voltage; the derivative of v_{DS} decays with time, i.e. the voltage softly drops towards its steady state value.

At $t = t_3$, the drain source voltage has fallen to such a level that the MOSFET no longer is operating in the saturated region. In order to still support the current, the gate voltage is being increased. The drain source voltage is now at such a low voltage level that the change in gate capacitance (C_{GS} and C_{GD}) will only be determined by the change in gate potential. Hence, a small value of the total gate capacitance (C_{GS} and C_{GD}) will result in a faster decrease of the drain source voltage. When the gate voltage reaches the final value ($V_{G(on)}$), the turn on process is completed.

2.4.3 Turn-Off Behavior of the MOSFET

With the circuit shown in Figure 2.19, the turn-off process of the MOSFET can also be analyzed. When the MOSFET is turned on and carrying the full inductor current, a turn off process can be started in order to commutate the current to the diode, see Figure 2.20.

Before $t = 0$, a positive voltage is applied to the gate terminal and the device is fully conducting. At $t = 0$, the gate voltage is momentarily decreased to $0V$. The discharge of the internal gate capacitances starts and the gate voltage decrease during the interval $t_0 < t < t_1$ can be described as

$$v_{\text{GS}}(t) = V_{\text{GS(on)}} \left(1 - exp \left(\frac{-t}{R_{\text{G}}(C_{\text{GS}} + C_{\text{GD}})} \right) \right) \qquad (2.12)$$

where $v_{\text{G(on)}}$ is the applied voltage, R_{G} is the gate external and internal resistance, and C_{GS} and C_{GD} are the lumped gate-source and gate-drain capacitances respectively. Note the obvious similarity to (2.11) with a significant difference in the time constants found in the denominator which is caused by the voltage dependency of C_{GD}. As long as the MOSFET is turned on, the gate drain voltage is low which results in a large value of C_{GD}. The gate drain capacitance can during this time interval be assumed to be constant since the change in gate drain voltage is relatively small.
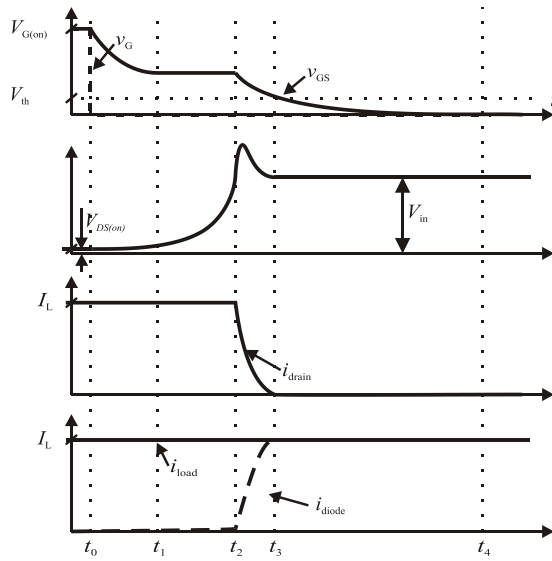
Fig. 2.20: Turn-off diagram of a MOSFET.

At $t = t_1$, the MOSFET leaves the ohmic region and enters the saturated region. As long as the drain source voltage is below the DC-voltage level, the diode will be reverse biased, hence no commutation process between the diode and the MOSFET can start. The gate voltage can no longer decrease which gives a plateau in the gate voltage. Due to the constant gate-source voltage, the entire gate current is discharging the gate drain capacitance. As the gate-drain voltage continues to increase, the gate-drain capacitance also shows a sudden decrease which gives an increasing voltage derivative as the time approaches $t = t_2$.

At $t = t_2$, the voltage over the MOSFET becomes equal to the DC-voltage which gives a possibility for the diode to start to conduct. The drain source current is no longer constrained to the full inductor current, hence can the decrease in gate source voltage continue. The sudden decrease in gate voltage is reflected in the

drain current, the inductor also sees this current drop and sets up a reverse voltage that makes the diode forward biased. If stray inductances are added, a reverse voltage is set up when the drain current is reduced. This voltage is added on top of the drain source voltage and its maximum value occurs when the change in drain current is at largest, i.e. right after $t = t_3$.

At $t = t_3$, the commutation process is completed and the gate voltage drops below the threshold voltage.

2.4.4   Modeling of the MOSFET

The original MOSFET model in SPICE is based on physical properties of the device and was originally used for describing the behavior of a low voltage metal-oxide interface. In the linear region, I_{DS} is described by

$$I_{DS(linear)} = \frac{\mu W_{eff} C_{ox}}{L_{eff}} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS}) \qquad (2.13)$$

where W_{eff} and L_{eff} is the effective channel width and length, respectively, C_{ox} is the gate oxide capacitance and μ is the carrier mobility. λ is an empiric channel length modulation parameter that corrects for the conductance in the saturation region. The drain current in the linear region is based on external applied voltages such as V_{GS} and V_{DS} and on the model geometry. If the MOSFET is being operated in the saturated region, the drain current is described by

$$I_{DS(saturation)} = \frac{\mu W_{eff} C_{ox}}{2 L_{eff}} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \qquad (2.14)$$

with the same parameters as in (2.13). The difference is that the drain-source current is no longer dependent on the drain-source voltage (except for the channel modulation parameter) since the inversion channel under the gate is pinched off.

In SPICE is the charge storage represented by the internal capacitances; C_{GS}, C_{GD} and $C_{gate-bulk}$. The SPICE gate-source and gate-drain capacitances are expressed as functions of applied voltages, channel width and operating region which make them inadequate for power MOSFET simulations since the functions are not adapted for vertically diffused structures [60, 76]. However, the *iv*-characteristics are still well represented by the SPICE model which makes it useable for static performance. The most common VDMOS representation is to use SPICE MOSFET for static performance and add extra elements to that represent the different features of a VDMOS; e.g. variable gate-drain capacitance and internal body diode. The most common approach is seen in Figure 2.21 where the equivalent circuit accounting for C_{GS}, C_{GD} and the internal body-diode D_{body} [30].
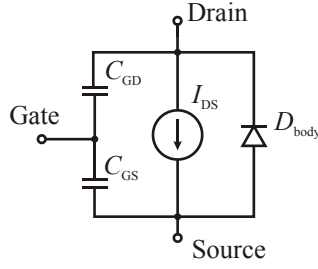
Fig. 2.21: Structure of the IGBT and equivalent circuit.

A more advanced example of this methodology is presented in [77] where the additional parameters added are a representative body diode, terminal inductances, terminal resistances and a variable gate-drain capacitance in series with a variable voltage source. A common way of modeling the voltage dependent gate-drain capacitor is by describing the current as

$$i_{GD}(t) = C_{GD} \frac{dv_{c(GD)}(t)}{dt} \qquad (2.15)$$

where $v_{c(GD)}$ is the voltage over the capacitor and C_{GD} is the capacitance. By measuring the change in gate drain voltage and multiply it with a constant, an analogous capacitor current can be achieved. Model parameters are often extracted from device measurements to minimize the error of the model.

Many semiconductor manufacturing companies have some kind of black-box MOSFET model in which a standard FET-model is adapted for VDMOS structures by adding external components that fit the model to datasheet values. See [78] for a description of Infineon SIMPOS models for switching applications and [79] for SPICE models provided by Fairchild Semiconductors.

2.5 The IGBT

The IGBT is a spin off from power MOSFET technology which clearly can be seen when the physical structure is analyzed, see Figure 2.22. The operating principle of the IGBT is the employment of a MOS structure that ignites a bipolar junction transistor which handles the majority of the current flowing through the device. As the gate voltage exceeds the threshold voltage, an inversion channel forms under the MOS interface in the p-base region. This inversion field enables the flow of electrons from the cathode to the n^--region that acts as a base current to the pnp-transistor T_1 in Figure 2.22. The IGBT anode starts to inject holes in the n-base region and enables it to carry a current. If a negative collector-emitter voltage is applied, the pn-junction at the collector becomes reverse biased and makes it possible for the device to support large negative voltages.
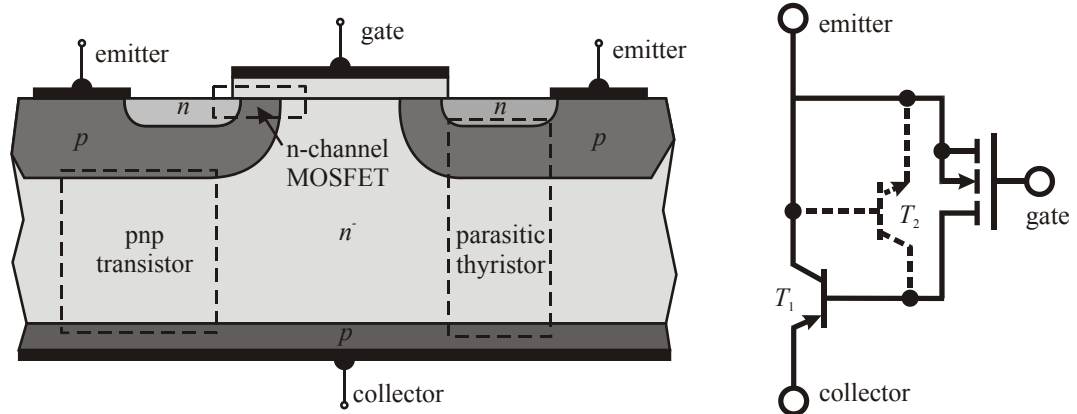
Fig. 2.22: Structure of the IGBT and equivalent circuit.

As for the power MOSFET, three different operating regions can be distinguished for the IBGT, see Figure 2.23. If a low V_{CE} is applied, the IGBT starts to operate in the saturation region. Unlike for a power MOSFET, the IGBT demand a minimum forward voltage before it starts to conduct that originates from the *pn*-junction close to the collector. When the IGBT is operating in the saturation region, the total current flowing through the IGBT collector consists of a MOS current (I_{MOS}) that depends on the applied gate voltage and a bipolar current (I_{pnp}). The bipolar transistor operates in the active mode and its base is driven by the injection of electrons from the MOS channel region. However, the large base width of an IGBT results in a low current amplification factor which gives that the main conduction path of an IGBT often is through the MOS part of the transistor.
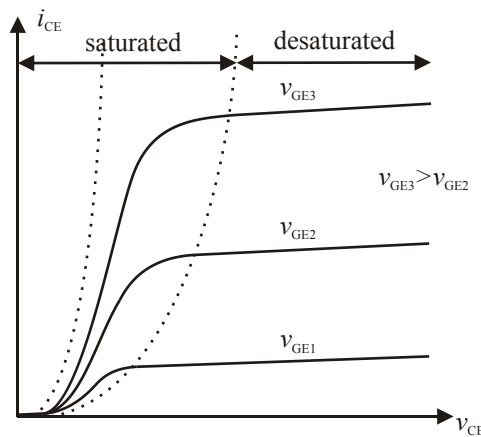

Fig. 2.23: Ideal output characteristics of an ideal IGBT.

Due to the low doping level in the n^--base region, a low injection of holes from the collector *pn*-junction drives the n^--base region into high injection and forms a type of plasma. In the region between the cells a *pin*-diode is formed via the MOS channel that injects electrons into the base region. This plasma

concentration causes a tail current when the IGBT turns off as the charges first needs to be swept out.

When v_{CE} is increased, the IGBT will eventually enter the active-saturation mode which is caused by two physical mechanisms; as the v_{CE} increases, the depletion layer at the emitter of the device also increases on expense of the internal *PiN*-region. At a certain voltage, the depletion layer of neighboring cells will be joined together which totally makes the *PiN*-region disappear. The second effect also originates from the expansion of the depletion region; as it expands into the *p*-base under the gate electrode, it gives rise to a potential increase at the end of the MOS channel. At a certain voltage, the channel will no longer be in strong inversion which results in pinch off and saturation of the MOS region. Note that the output characteristics will show a small slope in active transistor mode which originates from the Early effect in the *n*-base of the *pnp*-transistor [58].

2.5.1 Internal Capacitances of the IGBT

The internal capacitances in the IGBT are quite similar to the ones found within the MOSFET and can be seen in Figure 2.24.
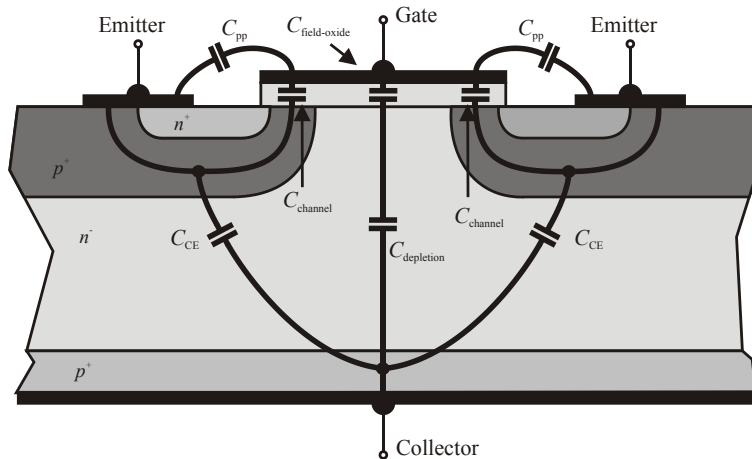
Fig. 2.24: Internal capacitances of an IGBT [80].

The dominant component of C_{GE} originates from the MOSFET region due to the gate oxide capacitance of the source overlap C_{PP}. The gate-collector capacitance (C_{GC}) consists of two different parts and the greatest contributor depends on the applied voltages. When the IGBT is operating in the linear region and the applied voltage over it is low, the gate oxide capacitance of the collector overlap ($C_{field-oxide}$) dominates. When V_{CE} is high, C_{GC} is a series combination of the gate-drain overlap oxide capacitance ($C_{field-oxide}$) and the gate-drain overlap depletion capacitance ($C_{depletion}$) [80].

As for a MOSFET, it should be taken into account that the values provided in the datasheets are mostly given for a zero gate voltage. As stated in e.g. [81-83] the value of these capacitances will differentiate substantially from the datasheet values when the IGBT is active. Another aspect that is not usually included in IGBT models but also has significant effects on the transient gate voltage waveforms is the large input capacitance variation for negative gate bias. However, models using a conventional representation can be fundamentally correct, as long as the gate voltage remains positive [84].

2.5.2   Turn-On Behavior of the IGBT

For the very common application where the IGBT is switching an inductive load with a freewheeling diode, the turn-on characteristics can be seen in Figure 2.25. The example assumes that a PiN-diode with its belonging recovery characteristics is used as a freewheeling diode.
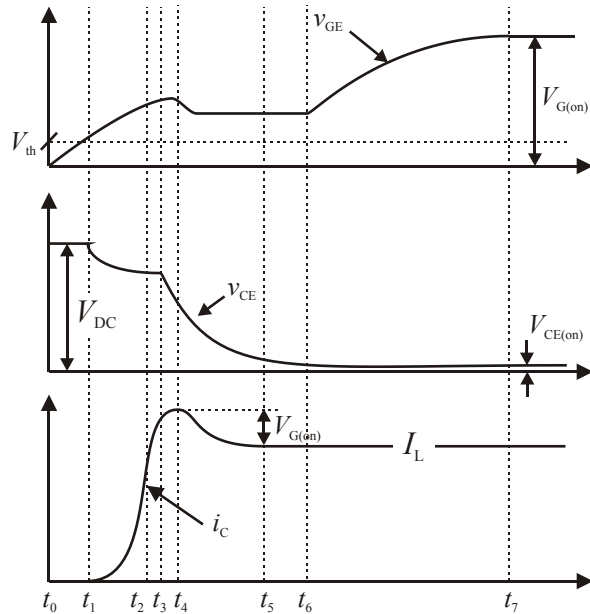
Fig. 2.25:   Turn-on diagram of a IGBT.

At $t = t_0$, a positive gate voltage is applied to the gate terminal with the amplitude $V_{G(on)}$. During the interval $t_0 < t \leq t_1$, no injection of electron will occur from the MOS interface into the IGBT since the threshold voltage still not is reached. The applied gate voltage will charge both input capacitances (C_{GE} and C_{GC}) via the gate resistor.

At $t = t_1$, the threshold voltage is reached which gives an injection of electrons into the n-base of the pnp-transistor from the newly formed inversion area under the MOS interface. As a reaction to the base current, the anode will start to inject

holes into the n-base which gives rise to the flow of a collector current (i_C). The buildup of the collector current after t_1 can be approximated to the rise of a current in the MOS transistor part of the IGBT since the low current base amplification of the internal pnp-transistor forces the majority of the current to pass through the MOS interface. v_{CE} will show a small drop during this phase due to the negative voltage build up over the parasitic inductances in the circuit.

At $t = t_2$, the collector current reaches the steady state inductor current I_L. The current through the diode drops to zero and commutation can start. If the freewheeling diode is a PiN-diode, its reverse recovery current results in a continued increase of the IGBT collector current.

At $t = t_3$ (the interval $t_3 < t \leq t_4$), all plasma at the diode pn-junction is swept out and the diode can start to support a reverse voltage. This results in a decreasing collector emitter voltage over the IGBT and a discharge of the gate-collector capacitance C_{GC}. In this phase, the gate-emitter capacitance charging current often becomes negative with a resulting decrease of the gate-emitter voltage. The current through the IGBT is then limited which results in the delayed peak in the reverse recovery current at $t = t_4$.

During the interval $t_4 < t \leq t_6$, the reverse recovery current in the diode is starting to decrease. The decreasing collector current results in a small drop on the gate voltage. As the recovery current is completed, v_{GE} settles at a level that makes the IGBT able to support the full inductor current. Eventually, as v_{CE} decreases even further, the IGBT enters the saturation region at $t = t_6$.

After $t = t_6$ has v_{CE} dropped to such a level that the IGBT goes from active transistor mode to the saturation region. In order to sustain the entire load current, the gate-emitter voltage must increase. Both gate capacitances, C_{GE} and C_{GC}, are now charged, hence the slower increase in gate voltage.

2.5.3   Turn-Off Behavior of the IGBT

As for the turn on-process, a PiN-diode is assumed to be used as a freewheeling device, see Figure 2.26 for curve forms. Before $t = t_0$, a positive voltage is applied to the gate terminal and the device is fully conducting.

At $t = t_0$, the gate voltage is suddenly decreased to 0V which causes the injection of electrons into the n-base layer to diminish. But due to the inductive load that still forces a current flow through the device, the collector current must be supported increasingly by the outflow of excess holes and electrons from the n-base; the plasma concentration starts to decrease.
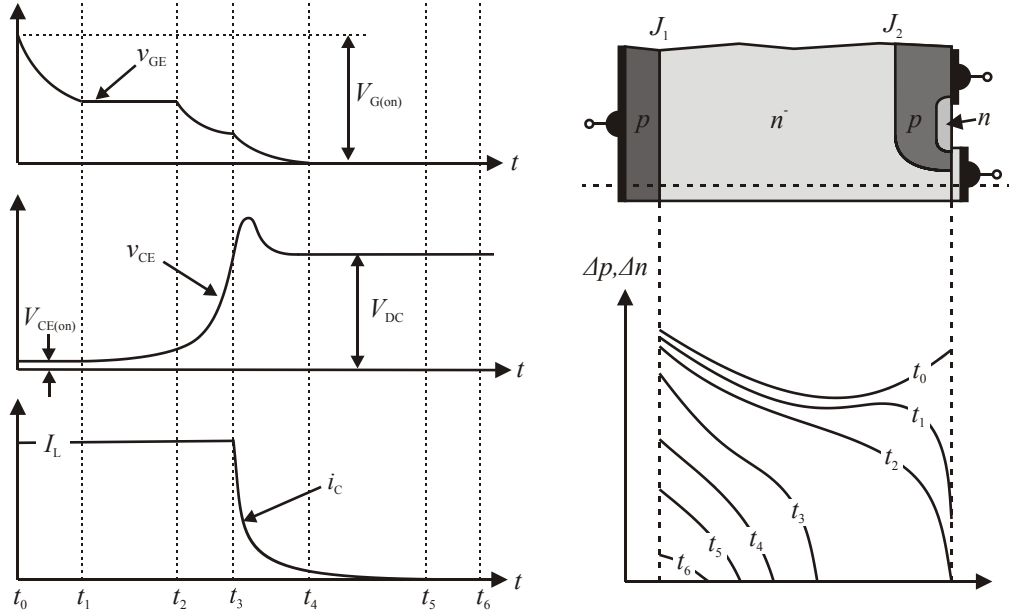
Fig. 2.26: Turn-on diagram of a MOSFET.

At $t = t_1$, the excess carrier concentration at junction J_2 has dropped to zero and a depletion layer is starting to form. This depletion layer makes it possible for the IGBT to support voltage. During this phase, the gate voltage is constant with a level that depends on the gate resistance.

At $t = t_2$ has the depletion layer increased in width and the device starts to support voltage, hence the collector-emitter voltage rises. The maximum rate at which it rises is determined by how fast the gate-collector capacitance is charged. However, the maximum rate can only be achieved if the plasma sweep-out provides the depletion layer around J_2 with enough room to expand at the required rate. The limitation of the collector-emitter voltage rise can be seen if the gate voltage is studied. If there is a limitation in gate current and C_{GC} does not consume the entire gate current, C_{GE} will also discharge and give rise to the decrease in the gate-emitter voltage.

At $t = t_3$, the collector-emitter voltage has reached the DC-level and the space charge region no longer expands. In the beginning of this period, the PiN-diode region of the IGBT conducts together with the bipolar part, hence the collector current drops rapidly and commutates to the freewheeling diode. As the PiN-region eventually shuts down due to the increased space charge region, the pnp-region has to carry the entire collector current. Since there is no way for the plasma to be swept out, the carriers have to recombine inside the n^--region. Due to the long carrier lifetime in the n^--region, the time it takes for the carriers to recombine will be correspondingly long which results in a relatively long tail in

the collector current. Also note that the high derivative in the current in combination with the stray inductances results in a voltage overshoot on v_{CE}.

2.5.4 Modeling of the IGBT

As previously explained, the IGBT operates as a bipolar transistor that is supplied with a base current by an internal MOSFET. This basic equivalent circuit of the IGBT is shown in Figure 2.27 in which the inner parasitic capacitors (C_{GE}, C_{GC} and C_{CE}) are considered [85].
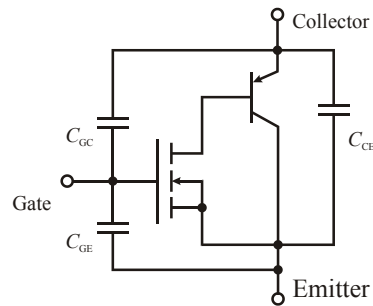

Fig. 2.27: Standard IGBT equivalent circuit [86].

No model of the IGBT is implemented in the original SPICE language but a de facto standard has been implemented PSPICE is based on the work performed in [87] and is modeled as an intrinsic device with help of current sources and charge components. According to the validation in [88], the suggested PSPICE model performs well, but for high voltage components the assumed linear carrier distribution in the n^--base region becomes unrealistic which results in inadequate iv-characteristics and switching behavior [89]. For the voltage range investigated in this thesis (600-1200V), some manufacturers (e.g. Fairchild Inc.) also have built up a complete model by implementing discrete components, e.g. MOSFETs and BJTs to form a complete IGBT model.

When dealing with SPICE models, the main problem for a hardware engineer is that the model is built on physical parameters that often are unknown for the end user. Ansoft has approached this problem by implementing a model parameter extractor in Simplorer. The IGBT model is a combination of a BJT and a MOSFET with the possibility to add an internal freewheeling diode. The complexity of the model can be defined in different levels; the most detailed model accounts for correct switching behavior. Charging and discharging of junction and diffusion capacitances are taken into account by defining the parasitic capacitances. The tail current is modeled for by an internal current source that takes both junction temperature and the applied collector-emitter voltage into account [90].

Chapter 3

Test Circuits and Experimental Setup

To be able to characterize all ingoing components, several different test circuits and simulation tools needs to be used. This chapter summarizes the different test circuits used in this thesis to obtain a full covering validation of the component models.

3.1   Computer Tools

In this thesis, the background description of the electric circuits are mainly analyzed with SPICE equations due to that it is a facto standard when simulating electric circuits, an extensive explanation of the background theory is available and that manufacturer models often are available in the SPICE language. Since it is not originally intended as a simulator for power electronics, different variants of the original SPICE adapted for switching applications have emerged on the market, e.g. LTspice IV from Linear Technology. But since the configurability of these programs have been somewhat limited, there features have not been investigated further in this thesis. In addition to SPICE, there are other simulation languages more adapted to switching circuits that also integrate the basic functionalities in SPICE together with a multi-domain simulation possibility such as SABER and Simplorer. Simplorer was chosen as the main tool in this thesis because of its IGBT model, diode model, parameter extraction tool and multi domain co-simulation capability and the possibility to import SPICE models that can be used within the program. Simplorer can also model analog, digital, mixed signal in the same simulation and be used as a top level program that controls other Ansoft software, such as finite element analysis. In many cases, a circuit analysis (e.g. AC-sweep of a capacitor model) can be performed in all electric circuit simulation software's and if not stated explicitly for a certain test, the simulation tool used is considered to be of minor importance.

For FEM calculations and to determine the parasitic elements, the electric field

solvers within the Ansoft suite were used. Maxwell is a low-frequency electromagnetic FEM calculator intended for inductor and machine design that can be used to solve static, frequency-domain and time-varying electromagnetic and electric fields. Q3D Extractor is a parasitic extraction software tool that uses both Method of Moments (integral equations) and FEM-calculations to compute capacitive, conductance, inductance, and resistance matrices. Q3D Extractor is originally intended to use for high speed digital design, but in this thesis it has been combined with Simplorer and Maxwell to form a complete coverage of the EMI performance in a switched converter.

3.2   Ramp Test Circuit

To verify e.g. the iv-characteristics of a diode a ramping circuit with high current handling capacity is needed. To obtain this, the test circuit presented in Figure 3.1 was constructed. The circuit generates a voltage ramp on the device under test and if a three terminal device is analyzed, the circuit has a possibility to connect an external voltage source. The voltage ramp is generated by a hot-swap circuit (LT1641 from Linear Technology Corporation) in combination with a single pulse generator. The test circuit generates a sufficiently slow voltage ramp so that dynamical phenomena can be neglected, but sufficiently fast so that the energy dissipated in the component does not exceed the maximum allowed safe operating area of the DUT. A typical rise time of the voltage ramp is e.g. $0-5V$ in approximately $1ms$ which is sufficiently fast so that internal heating can be neglected. For measurements of component characteristics at other temperatures than room temperature, the DUT was mounted on a heated object with large thermal capacity. The temperature was carefully monitored during the test with IR-thermometers and an IR-camera to ensure that the temperature was kept constant throughout the measurements. The test circuit is used to test the output characteristics for both MOSFETs and IGBTs as well as to obtain the iv-characteristics for diodes.
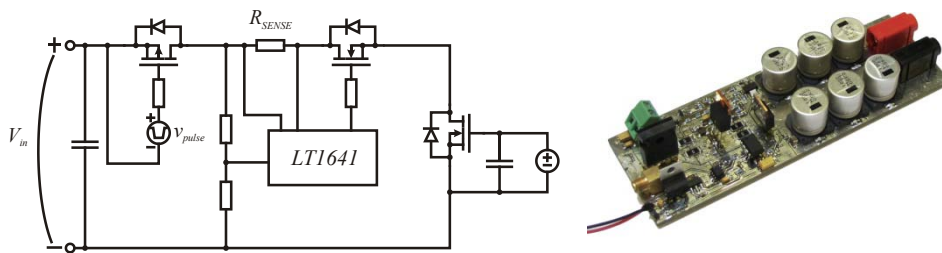

Fig. 3.1:   Test circuit for determining output characteristics

3.3   Inductive Test Circuit

The inductive test circuit is a standard test circuit found in most component

datasheets; see Figure 3.2 for schematic overview and actual circuit. The operation principle is that when the switch is turned on, the DUT is reverse biased and the current in the inductor starts to increase linearly. After a certain time, the switch is turned off again so that the inductive current forces the DUT to become forward biased. When the switch is turned on again, the DUT becomes reverse biased once again and as the current commutates from the DUT to the switch, a reverse recovery event occur. The operation of the switch is so fast so that only the parasitic inductance in the diode commutation loop will determine the current derivative during the reverse recovery event. The circuit is controlled by a microprocessor that generates the required pulses whose duration can be carefully controlled. As for the ramp test circuit, the DUT was mounted on a heated object with large thermal capacity when measurements of component characteristics at other temperatures than room temperature were performed. The temperature was once again carefully monitored during the test with IR-thermometers and an IR-camera to ensure that the temperature was kept constant.
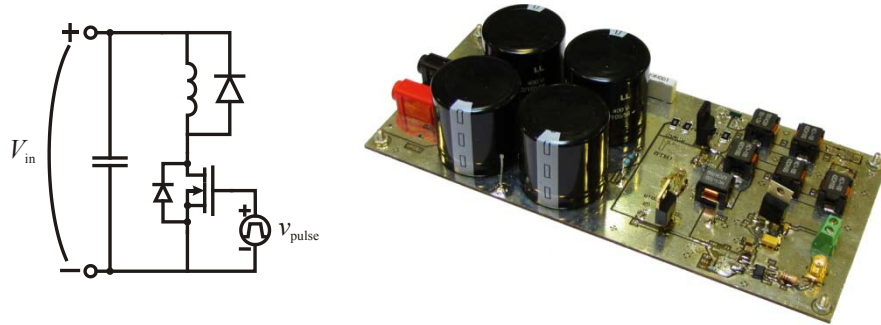

Fig. 3.2:   Inductive test circuit for determining dynamic characteristics

3.4   Switching Circuit with Resistive Load

To verify the dynamic behavior of the semiconductor models, the best way is to create a test circuit that is as simple as possible. The simplicity is needed to make sure that no other components influence the investigated component and to reduce the impact of parasitic components. The switching circuit consists of a switching element, IGBT or MOSFET, a low inductive resistive load and a drive circuit. The operational principle of the test circuit is seen in Figure 3.3 together with a photo of the real circuit. The value and power handling capability of the resistor differs depending on which type of component that is investigated.

3.5   Capacitance Test Circuit

The method for determining diode capacitances is based on a constant current charger described in [91]. The principle of the circuit is to charge the DUT with a constant current and measure the voltage. Due to the constant current, the total
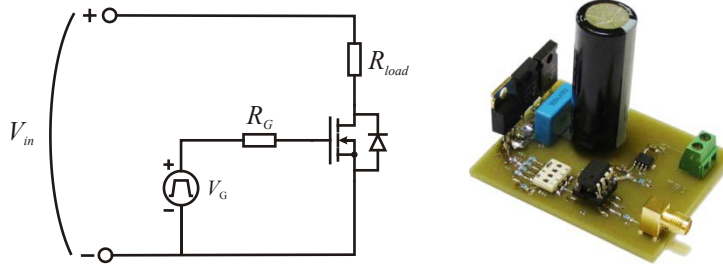
Fig. 3.3:   IGBT switching circuit with purely resistive load.

capacitance of the measurement object is

$$C_{\text{tot}} = \frac{i_{\text{tot}}}{dv_{\text{DUT}}/dt} \qquad (3.1)$$

where C_{tot} is the total device capacitance and v_{DUT} is the measured voltage. Since the inherent probe capacitance can have the same magnitude as the device that is analyzed, the probe capacitance needs to be taken into account. Figure 3.4 show a principal schematic of the constant current charger where the small constant current is generated by a constant current generator LM334 and the switch event is initiated by a mechanical switch.
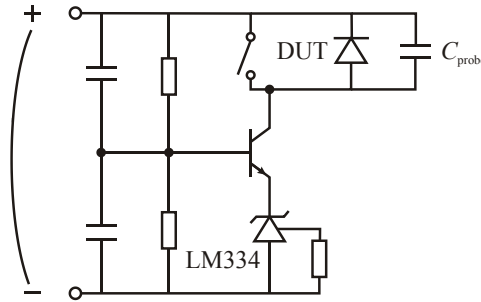

Fig. 3.4:   Circuit diagram of a constant current charger

The voltage over the probe is measured and together with the known value of the inherent capacitor (specified by probe manufacturer), the current into the probe can be calculated. The capacitance of the DUT can then be calculated since both capacitors are connected in parallel and will have the same voltage applied over them. This test method together with the measurement setup described in Section 3.6 serves as a base of all capacitance measurements on diodes.

3.6   Impedance Test Set-up

The impedance of all objects in this thesis is measured with an impedance analyzer or vector network analyzer where found most suitable. In all cases has the instrument been thoroughly calibrated with well defined impedances to

minimize measurement errors and component leads has been kept as short as possible to make sure that only the actual test object is analyzed.

All physically small components such as resistors and capacitors have been measured with an Agilent E5061B vector network analyzer (VNA) with low frequency and impedance analysis functions. The analyzer has been calibrated with the supplemented calibration kit and the components have been mounted on a test fixture (e.g. Agilent 16192A). The Agilent E5061B has also been used to measure capacitances as a function of applied voltages (built in DC-bias source up to 40V) and to measure S11 reflection parameters for PCB analysis. Filter properties and mutual couplings have been analyzed with an Anritsu MS4630B network analyzer together with a reflection bridge. The instrument has built in filter analysis functions and impedance calculation functions which make it suitable for filter analysis and mutual couplings.

3.6.1 Inductive components

A common practice is to construct an inductive components consist of a magnetic core, and in order to obtain both correct losses and to determine the correct high frequency characteristics of the inductive component, the BH-loop of the material needs to be modeled in an adequate way. The BH-loop of the material can be determined by measuring the current on the primary side to obtain the H-field and integrating the voltage on the secondary side to obtain the B-field [92], see Figure 3.5.

$$H_{\text{tot}} = \frac{0.4\pi i_{\text{prim}}}{l_{\text{e}}} \frac{1000}{4\pi} \tag{3.2}$$

The flux density in the core is determined by integrating the secondary voltage using the RC-circuit according to

$$B = \frac{R_2 C V_{\text{sec}} 10^4}{n_{\text{s}} A_{\text{e}}} \tag{3.3}$$

where R_2 is the integrating resistance, and C is the integrating capacitor.
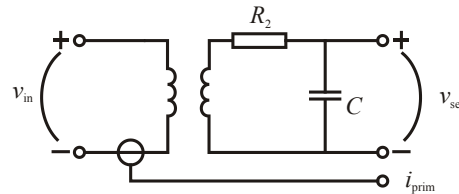

Fig. 3.5:   Electric circuit for determination of BH-loop [92].

3.6.2 PCB Impedance Test Board

A common way to obtain the total impedance of an unknown network as a function of frequency is to measure the S11 reflection parameter with a VNA and then transform it from the 50Ω -environment to obtain the total impedance. To analyze PCB properties and verify the simulations, a testboard was built that consists of several different trace lengths ($41mm, 82mm, 122mm$) and widths ($0.5mm, 2mm, 4mm$) on $1.6mm$ FR4 laminate with SMA-connectors on each end that give the possibility to connect an impedance analyzer on one end and terminate the other end with a RF-terminator, see Figure 3.6, left picture. The observant reader might also notice that the test board gives the possibility to evaluate different return paths; however, this feature was considered out of scope and therefore not evaluated in this thesis.
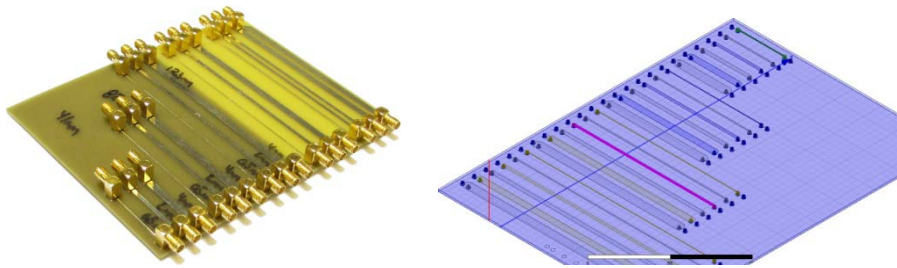

Fig. 3.6:   Left: Circuit   board   for   PCB-track   impedance measurements. Right: Q3D Extractor simulation model.

A similar test board was also implemented in Q3D Extractor, see Figure 3.6, right picture. Since it is difficult to verify the simulated capacitance, inductance and resistance with direct measurements of each component, a similar impedance as obtained with the measured S11 parameter must be calculated.

All parasitic components will interact and vary with frequency and by co-simulating Q3D Extractor with Simplorer, frequency dependent state-space parameters can be obtained of the analyzed test board. This makes it possible to perform a frequency sweep in Simplorer and in that way obtain the impedance as a function of the applied frequency.

3.6.3 Circuits for Mutual Coupling

The effect of component placement for capacitors was investigated with the testboard in Figure 3.7. One layout has short trace length but high mutual couplings which mean that the components are located parallel to each other with short trace lengths. The second layout has longer trace lengths and longer distances to grounding vias, but lower mutual couplings since the capacitors are located perpendicular to each other and are separated a relatively long distance.
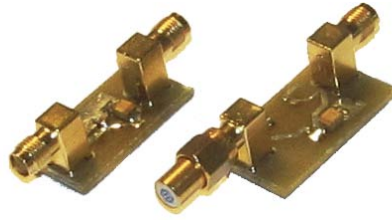
Fig. 3.7:   Test circuits for parallel connection of capacitors. Left: short traces but higher mutual coupling. Right: longer traces but lower mutual coupling. Including 50Ω SMA terminator.

3.7   Complete Converters

3.7.1   Flyback DC/DC Converter

The analyzed Flyback converter is a commercial converter PKR4211ASI from Ericsson Power Modules ($v_{in} = 36 - 75V$, $v_{out} = 5V$, $i_{out(max)} = 3A$). The converter is mounted on an additional 2-layer PCB to facilitate the interconnections, see Figure 3.8.
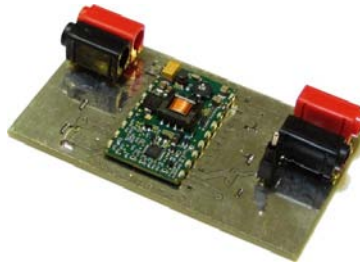

Fig. 3.8:   Analyzed Flyback converter mounted on a test PCB.

3.7.2   Synchronous Step-Down Converter

The step-down converter was made as a part of [93] and can be used both with diode and synchronous rectification, see Figure 3.9.

Fig. 3.9:   Synchronous step-down converter.

Chapter 3 - Test Circuits and Experimental Setup

Chapter 4

Modeling and Measurements of Components in Switched Converters

In order to simplify the construction process of applications that include semiconductors it is of great importance that the design can be simulated, both for a single component and as a complete system. This chapter verifies the most relevant properties of single components by measurements and simulations. Also, a more extensive analysis of MOSFET and IGBT modeling is presented; including the introduction of a new MOSFET model.

4.1   Passive Components

4.1.1   Parasitic Properties of PCB Traces

From the previously given equation (2.3), it can be seen that the skin effect will start to influence a PCB track with $35\mu m$ thickness when the frequency reaches approximately 10MHz. The increase in resistance due to skin effect becomes more significant for a trace with small cross section area, see Figure 4.1 where the analytical resistance from (2.3) is plotted as a function of the width and thickness.

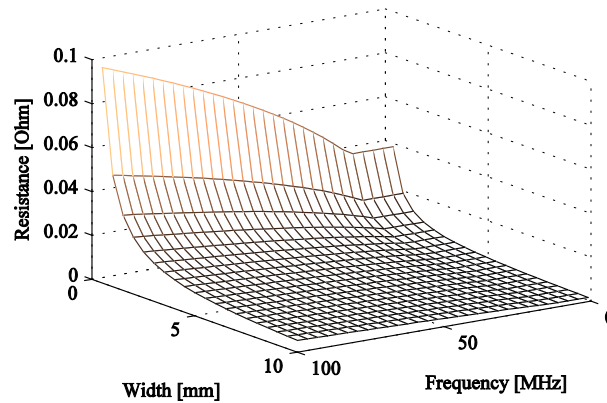*Fig. 4.1:*   Calculated analytical resistance with (2.3) for a PCB-track as a function of width and frequency ($h = 35\mu m,\ l = 40mm$).

But since (2.3) is an approximation, the behavior of a real microstrip will differ due to e.g. the proximity effect; the best way to predict the correct HF-resistance

is by FEM-calculations. The simulation results of the resistive analysis of a microstrip implemented in Q3D Extractor are presented in Figure 4.2 and 4.3. The simulations show the same trends as the analytical results, but the resistance becomes significantly higher for frequencies above 10MHz than suggested by (2.3). Note that the extracted resistance from the simulations also include effects in the via holes on the PCB. If the DC resistance is considered for a track with 3mm width, the analytical expression gives $7m\Omega$ plus approximately $1m\Omega$ per via hole with 0.6mm diameter, and the simulations gives $10m\Omega$ which verifies the validity of the DC-resistance calculations.
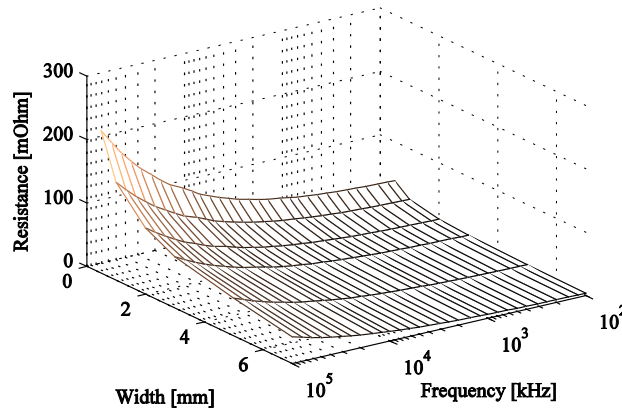
Fig. 4.2:   Simulated resistance from Q3D Extractor for a PCB-track as a function of width and frequency ($h = 35\mu m, \; l = 40mm$).

Fig. 4.3:   Simulated resistance from Q3D Extractor for a PCB-track as a function of length and frequency ($h = 35\mu m, \; w = 1mm$).

The external inductance of a PCB-track depends on the return path of the current and for a microstrip it can be calculated with (2.5). The inductance decreases as the width increases and is almost directly proportional to the length of the strip, see Figure 4.4 that shows a comparison of the DC-inductance calculated by (2.5) compared with simulation results from Q3D Extractor.

Fig. 4.4:   Simulated and calculated DC-inductance for a microstrip. Solid line: Simulation with Q3D Extractor. Circle: Analytical calculation with (2.5).

But as for the resistance, the inductance is also affected by the skin effect. The current will crowd to the edges of the conductor which results in an inductance that decreases as the frequency increases. Figure 4.5 and Figure 4.6 shows the simulation results from Q3D Extractor of the inductance as a function of frequency, width and length of a microstrip. The LF-inductance approaches values suggested by (2.5), but the results point out the importance to account for crowding due to skin effect when simulating the HF-behavior of a PCB trace. The inductance is almost proportional to the length of the track as suggested by (2.5).

*Fig. 4.5:*   Simulated inductance with Q3D Extractor for a PCB-track as a function of width and frequency ($h = 35\mu m, \; l = 40mm$)

In addition to the inductive effects, the tracks also form parallel plate capacitors between the track and the surrounding ground planes. The capacitive effects as a function of length and width are presented in Figure 4.7. Note that the frequency dependence of the capacitive is very small and negligible. The total permittivity of the dielectric is assumed to be constant since the complex part related to energy

dissipation within the medium shows almost no frequency behavior and the change of the real part, related to the energy stored within the medium, is very small [94].

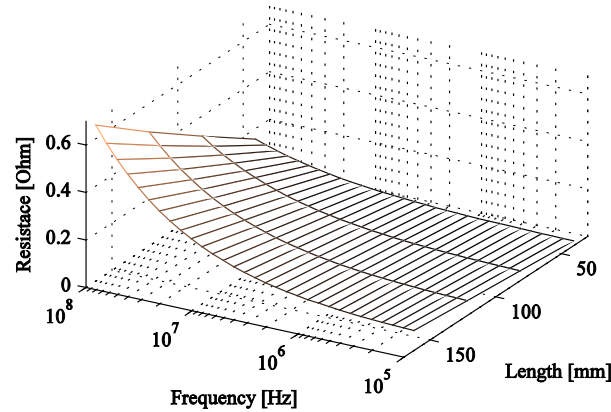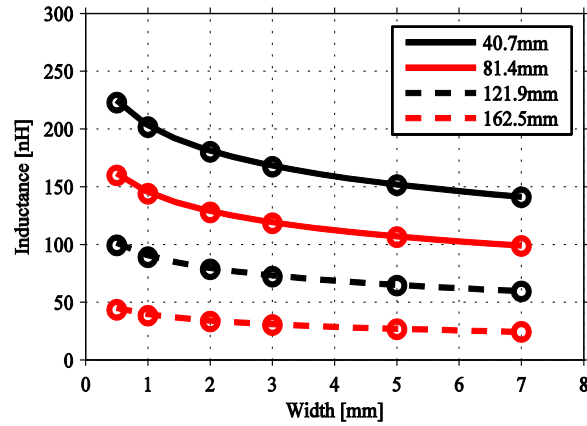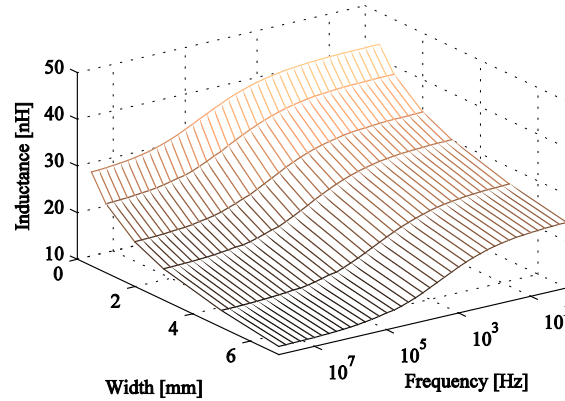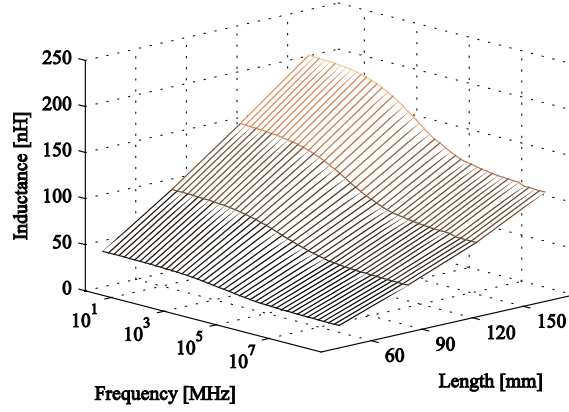*Fig. 4.6:*   Simulated inductance with Q3D Extractor for a PCB-track as a function of length and frequency ($h = 35\mu m,\ w = 1mm$)
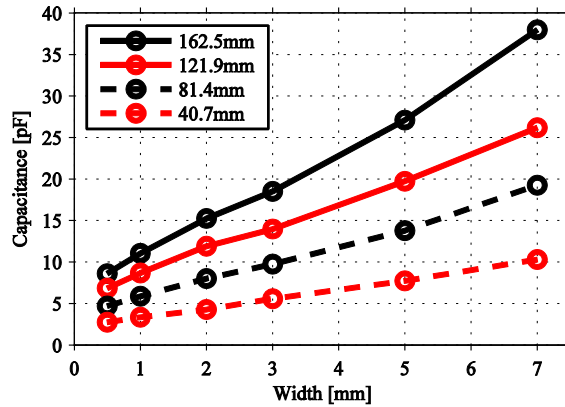
Fig. 4.7:   Capacitance for a microstrip as a function of length and width ($h = 35\mu m$). Simulation results from Q3D Extractor.

An analysis of the correspondence between simulations and measurements were performed for different track lengths and widths with the experimental setup and testboard described in Section 3.6.2. The accuracy was found satisfactory for all comparisons which verify that it is possible to simulate PCB parasitics with Q3D Extractor. Figure 4.8 shows a comparison of measurements and simulations from Q3D Extractor for three different microstrip lengths where the simulation results correspond well to the measurements. It can however be noted that since the simulation model only consisted of a PCB, the best accuracy was obtained if the simulation model was compensated with simple approximations of the parasitic capacitances in the SMA connectors.
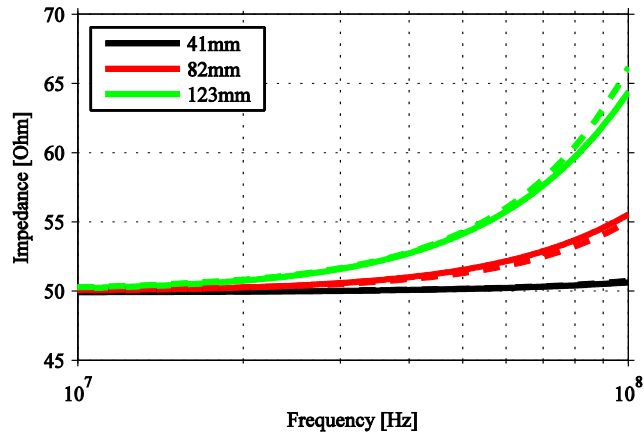
Fig. 4.8:   Impedance as a function of frequency for three different trace lengths ($w = 0.5mm$). Dashed line: Simulations from Q3D Extractor. Solid line: Measurements.

If Figure 4.8 is analyzed, it is seen that all three traces ($w = 0.5mm$) are inductive for higher frequencies and that the inductance increases as the length of the track increases. As theory tells, the inductance dominates for a long and wide trace, but when the trace becomes sufficiently wide, capacitive effects will become dominant and the impedance will decrease as the frequency increases. Capacitive effects in PCB-planes can be of interest in switching power supplies since they often utilize wide traces and planes that can handle high currents. Simulations in Q3D Extractor and measurements on the testboard described in Section 3.6.2 have verified that a trace becomes capacitive as the width increases. To illustrate this, additional simulations of traces with different lengths and widths were performed and the total impedance at $100MHz$ was calculated. The results are presented in Figure 4.9 that shows the impedance as a function of the trace area for four different trace lengths.

Fig. 4.9:   Simulated Impedance at $100MHz$ as a function of trace area for four different trace lengths ($h = 35\mu m$).

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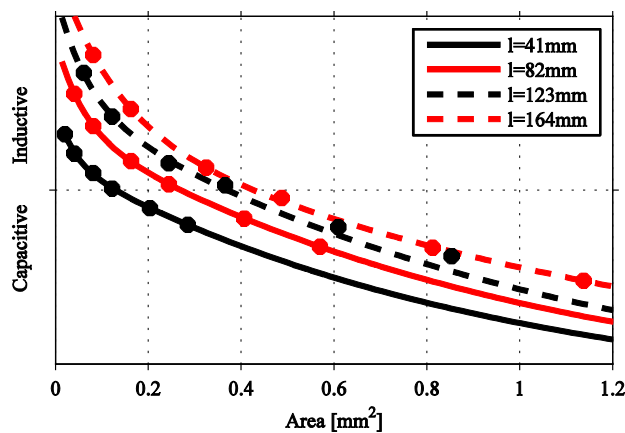The capacitive effects in the analyzed traces become dominant as the trace area increases and a long trace can be slightly narrower before the capacitive effect is noticed. As an example, the analyzed trace with length $41mm$ will become capacitive when the area exceeds approximately $0.12mm^2$ which corresponds to a width of approximately $3.2mm$. On the other hand, a trace with length $123mm$ will become capacitive when the area exceeds approximately $0.38mm^2$ which corresponds to a width of approximately $2.8mm$. Note that the analysis is only valid for the specified PCB stackup which is a microstrip with $35\mu m$ thickness, located $1.6mm$ from a ground plane on a FR4-dielectric. Different mechanisms will contribute to the changes which make the impedance necessary to simulate. A decreased dielectric thickness will result in greater capacitive effects but the trace inductance will also be affected due to the proximity effect.

4.1.2 Parasitic Properties for Different PCB Stackups

Since it is proven that Q3D Extractor gives satisfactory results for the PCB parasitics both for DC-analysis and the high frequency properties, it is of interest to expand the analysis to more realistic structures found on actual PCB's. The previous investigation has been aimed at a single microstrip, but it a more complexly structured PCB is used, the inductive and properties of the track will be significantly changed. Two additional PCB structures were analyzed in Q3D Extractor; a microstrip with a surrounding ground plane on the top layer and a stripline (a conductor sandwiched between two ground planes in a dielectric material). The aim of this investigation is to point out that not only surrounding planes on different layers separated by a dielectric material affects the high frequency behavior of the PCB trace, but also the distance to surrounding planes located on the same layer, see Figure 4.10 for illustrations of PCB stackup for the two investigated structures. The isolation distance of the surrounding ground plane is 0.3mm and the dielectric thickness is 1.6mm, i.e. the distance to the surrounding plane on the same layer is significantly shorter than to surrounding layers.
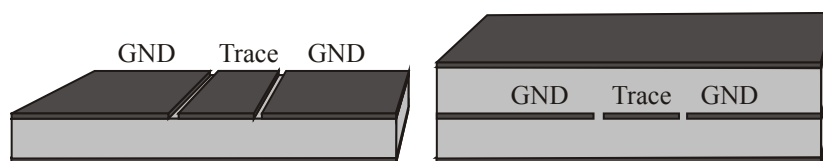

Fig. 4.10: Investigated PCB stackups. Left: Microstrip with surrounding ground plane. Right: Stripline with surrounding ground plane.

It concluded that the resistance is significantly increased by adding a ground plane on the same layer as the trace compared with a PCB structure with no surrounding ground plane on the same layer as the trace. Figure 4.11, left picture, shows the

resistance as a function of frequency and trace width for a microstrip with surrounding ground plane on the same layer and can be compared with Figure 4.2 that shows the simulated resistance for a simple microstrip. The increase is caused by the proximity effect and makes the AC-resistance significantly higher than what you would expect from skin effect alone. The magnetic fields distribute the current around the perimeter of the conductor in a non-uniform manner depending on the closeness to another conducting material [95]. In this case, the proximity effect is caused by a crowding of the current towards the side of the trace that faces the reference plane on the same layer. A narrow trace makes the proximity effect even more significant since the current crowding on the edges of the trace contributes more to the total resistance. The proximity effect also concentrate the returning signal current on the reference plane, forming it into a narrow band that flows on the plane, staying mostly underneath the signal trace. This effect is not accounted for in Figure 4.11 but must be considered if correct loop resistance is needed. The difference in resistance for the PCB structure with another ground layer separated by a dielectric becomes rather small; see Figure 4.11, right picture. These simulations verify that the distance to the closest reference layer determines the high frequency resistance of the conductor.

The inductance of the PCB trace show a behavior similar to the resistance since it also is affected by the current crowding due to proximity effect, Figure 4.12 that shows the inductance as a function of width for both structures with reference planes on the same layer. If Figure 4.12 is compared with Figure 4.5, the inductance is lowered for higher frequencies if a ground plane is added on the same layer. The proximity effect is, as the resistance also shows, more significant for a narrow trace compared with a wide trace.
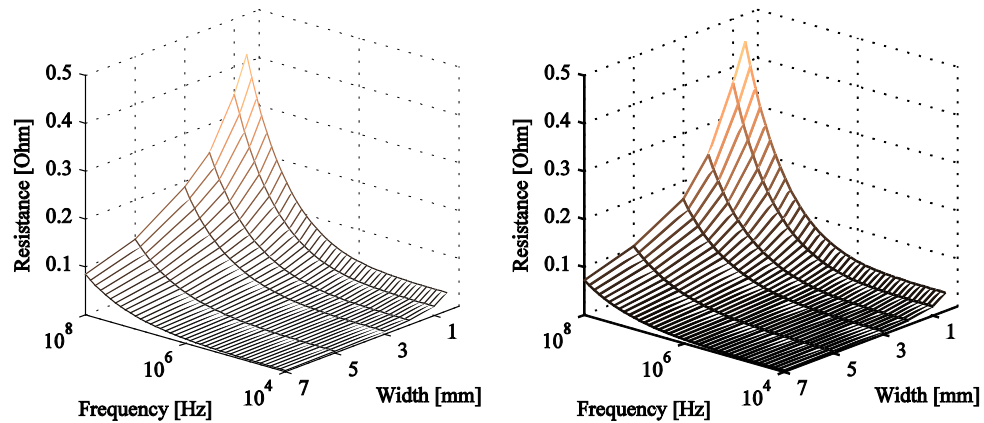

Fig. 4.11:   Simulated resistance with Q3D Extractor for a PCB-track as a function of width ($h = 35\mu m, l = 40mm$). Left: Microstrip with surrounding ground plane. Right: Stripline with surrounding ground plane.
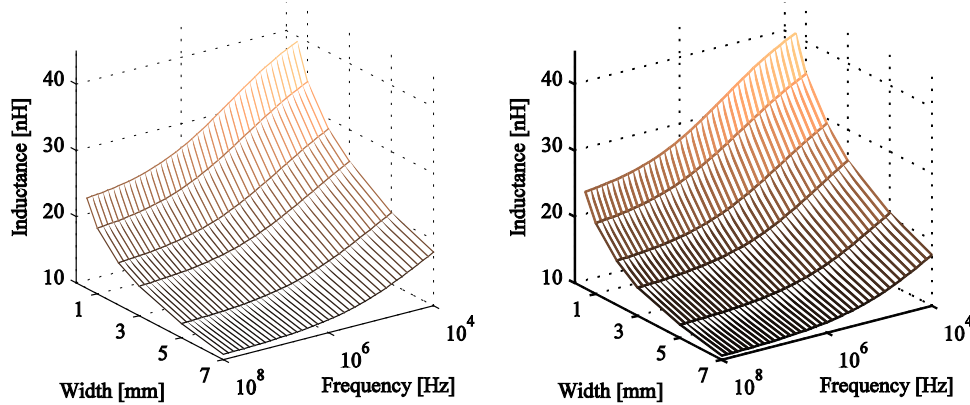
Fig. 4.12: Simulated inductance with Q3D Extractor for a PCB-track as a function of width ($h = 35\mu m, l = 40mm$). Left: Microstrip with surrounding ground plane. Right: Stripline with surrounding ground plane.

From the simulations is can be seen that by adding a ground plane on the top layer of the PCB, almost no change in capacitive effects can be noted, see Figure 4.13, left picture, which can be compared to Figure 4.7 that shows the same plot for a microstrip. If another ground plane is added to form a stripline, the situation becomes significantly different since the surrounding ground planes form two parallel connected plate capacitors. The capacitance is increased with approximately a factor 2; see Figure 4.13, right picture.
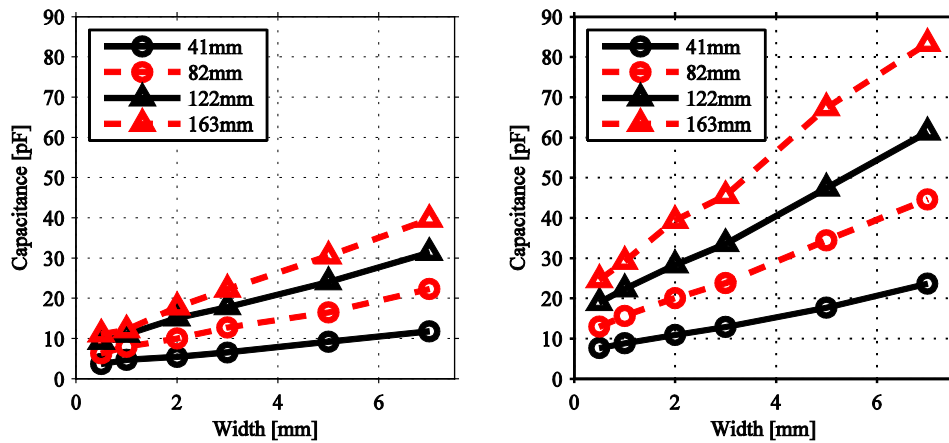
Fig. 4.13: Simulated capacitance with Q3D Extractor for a PCB-track as a function of length and width ($h = 35\mu m$). Left: Microstrip with surrounding ground plane. Right: Stripline with surrounding ground plane.

The concluding remark from the PCB-simulations is that Q3D Extractor calculates the AC-resistance and inductance by taking both the skin and proximity effect into account. If a good model of the inverter PCB can be created, this

vouches for a satisfactory behavior of the parasitic couplings that must be considered if correct EMI performance is desired in the simulations.

4.1.3 Resistive Components

As mentioned in Section 2.1.2, the high frequency characteristics of a resistor needs to be taken into account when correct high frequency EMI characteristics are needed. To characterize the resistive components correctly, the measurement procedure in Section 3.6 was used. The measurements showed that small surface mounted components (0805 and smaller) have low inductive effects at high frequencies. However, for physically larger surface mounted components (e.g. size 2512), the inductive effects becomes more significant even at frequencies below 100MHz, see Figure 4.14 that compare measurements of resistors in different packages. Within the scope of this thesis, the parasitic effects of all surface mounted resistors can be neglected and regarded as ideal components since the main scope is to identify lower frequency emission levels. However, if e.g. radiated emissions or other aspects such as high speed digital design within a converter need to be analyzed, the parasitic effects of surface mounted resistors might be necessary to include.
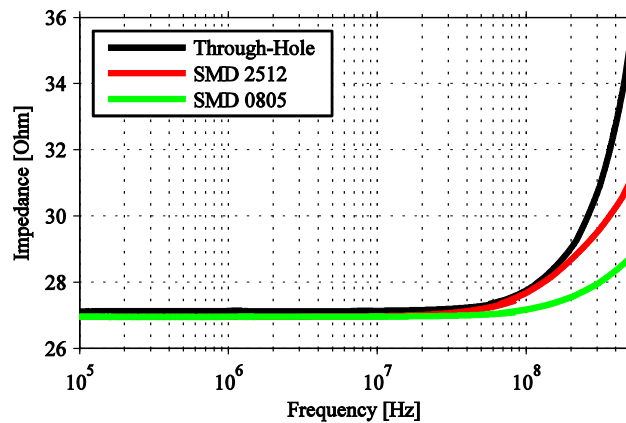
Fig. 4.14:   Measured impedance of 27Ω resistors in different packages.

Care needs to be taken if a wire-wound resistor needs to be used in a DC/DC converter that need low emission levels. The internal capacitance of the windings creates a large oscillatory circuit even at relatively low frequencies, see Figure 4.15 that shows the measured impedance for two different types of 100Ω resistors. It is also worth noting that when the measured component has high impedance, it becomes more difficult to characterize due to limitations in the impedance measurement procedure. This effect is taken into account for all components analyzed within this thesis. All resistive elements implemented furthermore in this thesis are implemented with correct high-frequency behavior, i.e. capacitive and resistive effects are taken into account where found necessary.
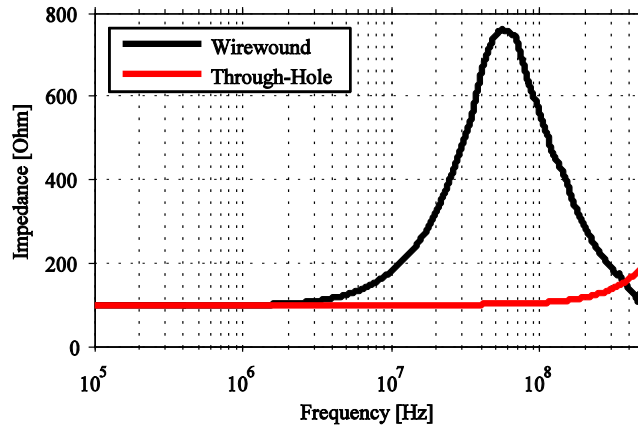
Fig. 4.15:   Measured impedance of 100Ω resistors of different types.

4.1.4   **Capacitive Components**

The high frequency characteristics for different capacitor types differ significantly from each other which make it necessary to characterize all components individually according to the measurement procedure in Section 3.6. Figure 4.16 shows a comparative study of different types of capacitors with equally large capacitance but with different types of high frequency behavior. The ceramic and plastic types show significantly lower resonant peaks compared to the tantalum type. Also, the conformity in impedance between the simulation models provided by the manufacturers (see Figures 2.2 and 2.3 for model description) and the measurements is fairly good but divergences can be noted especially for the resonant peaks.

Fig. 4.16:   Impedance   comparison   of   100nF   capacitors.   Solid   line:
            Measurements. Circled Line: Circuit model from manufacturer.

Regarding tantalum capacitors, the ESR of the capacitor is strongly frequency dependent and cannot be represented with a single resistor; see Figure 4.17, left

picture, where simulations and measurements are compared with a *RL*-circuit with constant ESR for a $1.5\mu F/35V/6032$ tantalum capacitor. The manufacturer model (see Figure 2.3) accounts for this and gives satisfactory results. Also, the package and type of dielectric strongly determines the im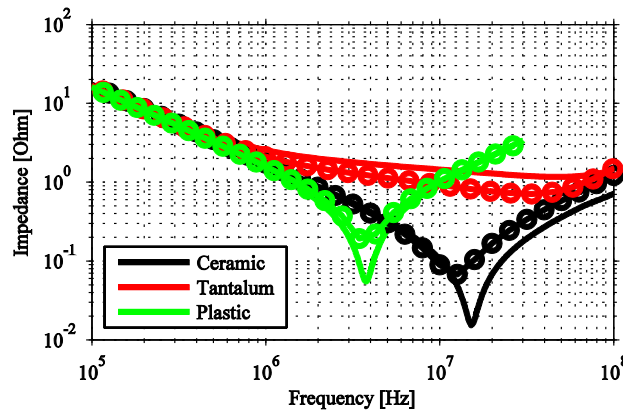pedance characteristics; see Figure 4.17, right picture, where different sizes of equally large capacitors are compared. The most noteworthy conclusion is that even though a physically larger component is most likely to have greater inductance due to the physical size, is may still be better in a mid frequency range since the ESR is lower.
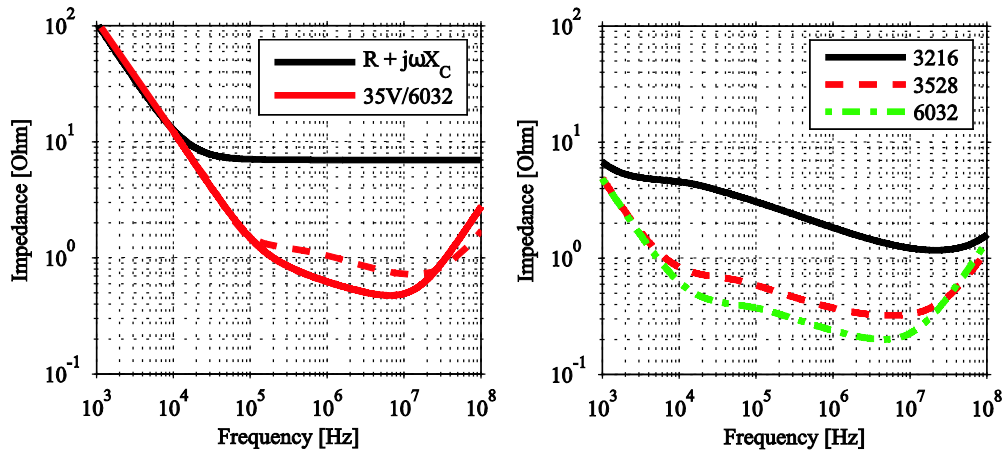

Fig. 4.17:   Left: Measurements (solid), simulated (dashed) and RL-circuit with constant ESR of $1.5\mu F/35V/6032$ tantalum capacitor. Right: Simulations of $330\mu F/10V$ capacitors in different packages with Kemet model.

The reasoning about how the material properties and size affects the impedance is of course also valid for different types of capacitors. The dielectric material in a ceramic capacitor will not only determine the capacitance due to its permittivity, but also cause different resonant peaks, see Figure 4.18, left picture. The main difference between a ceramic capacitor and a tantalum capacitor is the low ESR which gives a high Q-value. This becomes especially significant for a low-loss material such as NP0 that gives a very sharp resonance peak. The resonant peak is significantly dampened if X7R is used that has higher losses and higher dielectric constant but also a greater temperature drift. The difference in material does not influence the behavior so much if two different polypropylene capacitors are studied, instead gives the different voltage ratings rise to different package sizes which in turn increases the package inductances, see Figure 4.18, right picture. Note that since no simulation model is provided by the manufacturer for the analyzed capacitor in Figure 4.18, right picture. The analyzed model is based on Figure 2.2 with tuned parameters to fit the measured impedance curve.

A common practice is to connect a smaller ceramic capacitor in parallel with a larger electrolytic capacitor to increase the high frequency performance of the

capacitors. The size of the smaller capacitor is often chosen to 100nF which has proven to be a good balance between high frequency performance and impedance supplementation to an electrolytic capacitor. If a smaller capacitor than 100nF is chosen, its impedance will not affect the electrolytic capacitance above 10MHz, see Figure 4.19 for simulated impedance plots of tantalum (35V, 7473 package) capacitors, different ceramic capacitors (50V, 0805 package) and two capacitors connected in parallel.
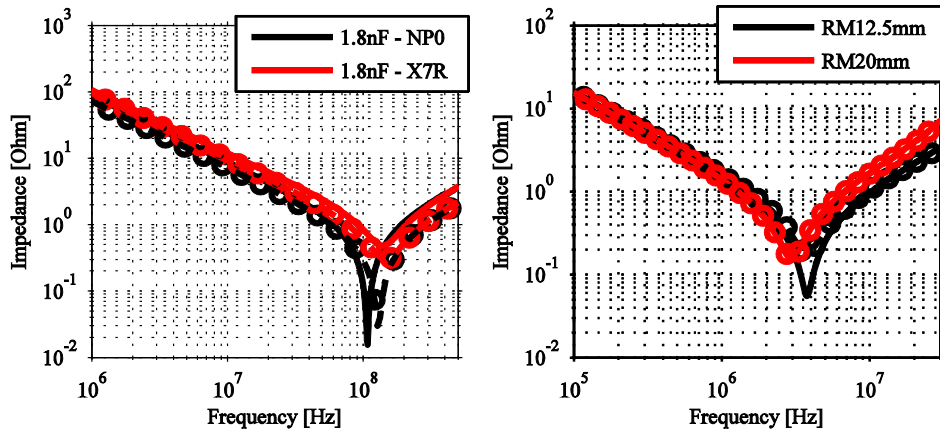
Fig. 4.18: Left: Impedance comparison of ceramic 1.8*nF* capacitors. Measurements (solid) and Kemet simulation model (circled). Right: Impedance comparison of TM polypropylene film 100*nF* capacitors. Measurements (solid) and tuned simulation model in Figure 2.2 (circled).
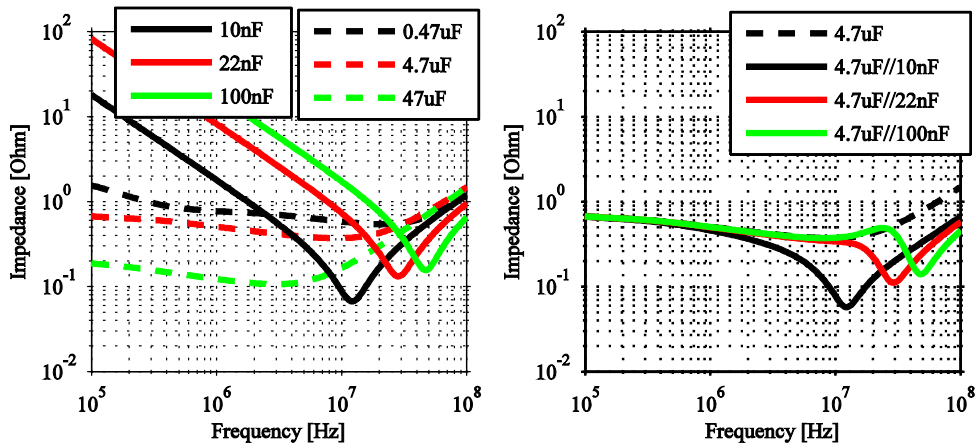
Fig. 4.19: Simulated impedance comparison of different capacitors from Kemet. Left: Size comparison of different ceramic and tantalum capacitors. Right: Parallel connection of different ceramic and parallel capacitors.

When a 100*nF* capacitor is selected, there are still many remaining issues that

needs to be dealt with; e.g. package and layout. The packaging of the capacitor affects the simulation results since a larger capacitor has a larger inherent series inductance. Figure 4.20 shows a comparison of different capacitor sizes, their impedance plots and the effect of parallelization with a tantalum capacitor; a physically smaller capacitor is more advantageous since the inherent capacitance is kept as low as possible ($< 1nH$).

Fig. 4.20: Simulated impedance comparison of different Kemet capacitors. Left: Comparison of 100nF ceramic capacitors with different packages. Right: Parallel connection of 100nF 1206 ceramic capacitor 4.7uF 7473 tantalum capacitor.

The previous simulations are based on SPICE simulation models provided by Kemet, but they still neglect several important aspects namely the influence of the PCB and mutual couplings. The analyzed capacitors were of tantalum and cer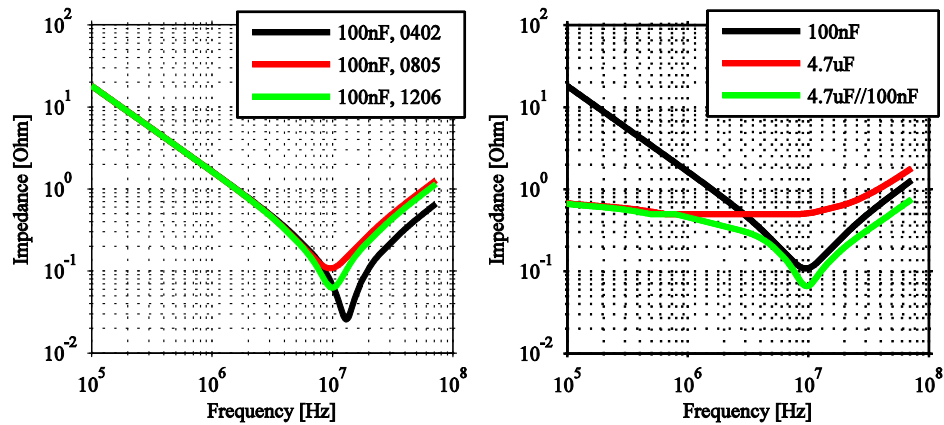amic type to achieve a compact layout as possible, but even a short distance between the two capacitors gives rise to trace inductance that must be taken into account if correct high frequency behavior is needed. If the capacitors are mounted on a PCB, see Section 3.6.2, it is found with measurements and simulations that the influence of the PCB can not be neglected even though the trace distance between the two capacitors are relatively small ($\approx 5mm$). By simulating the simple PCB in Q3D Extractor, it is found that the trace inductance lies in the range of $7nF$ for frequencies over $4MHz$ and that the capacitive effect is negligible since the trace is very short and narrow. The frequency dependence of the trace is neglected and a simple approximation is made that the trace consists of a single L with constant frequency. By adding such a short trace in the SPICE simulations, the capacitors will start to behave inductively already at $4MHz$ which is well below the resonant frequency anticipated by only the simulation model ($\sim 10MHz$). This is also seen in Figure 4.21 that shows a comparison between measurements of the capacitors mounted on a PCB and that the layout and trace is important to take into account for correct high frequency behavior.
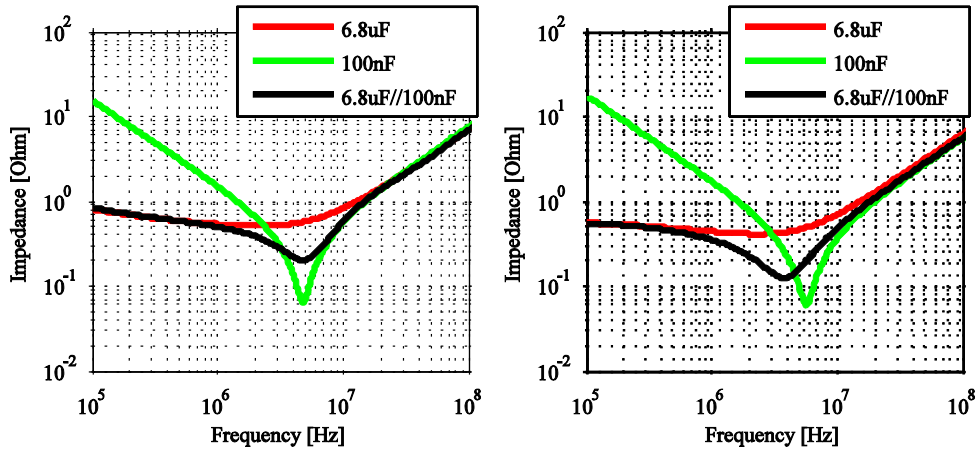
Fig. 4.21: Left: Measurement of 100nF 0805 ceramic capacitor, 6.8uF/25, 3528 tantalum capacitor and these two connected in parallel. PCB included. Right: Simulation of 100nF 0805 ceramic capacitor, 6.8uF 3528 tantalum capacitor and these two connected in parallel including PCB inductance ($L_{PCB} = 7nF$).

It is very difficult to determine the composition of the parameters that determine the parasitic behavior of the PCB; in some cases can the mutual couplings be more significant than the trace parasitics itself and vice versa. The way to investigate this is presented in Section 3.6.2 where two different component placements are described. One layout has short trace length but high mutual couplings and the other has longer trace lengths but lower mutual couplings, it can be expected that the impedance as a function of frequency is the same for the both objects since the PCB model in this case is approximately equal. However, measurements show that it is the mutual coupling that determines the high frequency behavior rather than the actual inductance due to the trace length. see Figure 4.22 where equally large capacitors are compared the different PCB's with different component placements. More results regarding the mutual couplings can be found in Chapter 6.2.

4.1.5 Inductive Components

The inductive components in the circuit are the most complicated to model since they are complex structures that consist of both a core material with magnetic properties and conductive wires to carry the current. The investigation performed in this thesis has therefore been divided in two parts; *BH*-loop modeling and impedance analysis. The two parts have then been joined in Simplorer together to form an extensive coverage of how to simulate magnetic components.
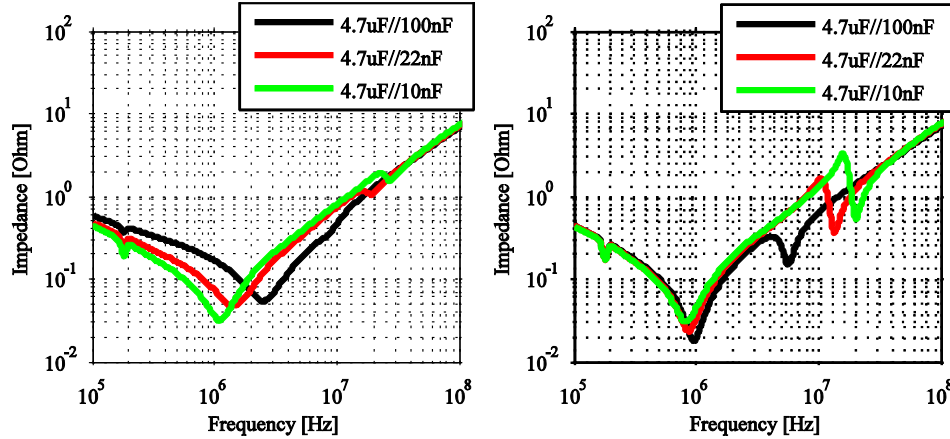
Fig. 4.22: Measured frequency response of different ceramic capacitors connected in parallel with a tantalum capacitor (6.8uF/25V 3528). Left: PCB with shorter traces and higher mutual couplings. Right: PCB with longer traces and lower mutual couplings.

One of most important parts that determine the frequency behavior of an inductor is its core and the magnetic properties of the material. For switched applications, different types of ferrite materials are most commonly used. To model this, the ferrite material with its associated *BH*-loop is implemented in Simplorer with the Jiles-Atherton model as described in Section 3.6.1. The proposed model accounts for hysteresis losses and the inductance is calculated with a reluctance term. It is concluded that the Jiles-Atherton model accounts for the hysteresis losses in an adequate way, see Figure 4.25, left picture that shows a comparison measurements and Simplorer simulations for the Ferroxcube ferrite toroid TN13/7.5/5-3F4. Note that the hysteresis loop needs to be matched to a certain frequency since the model does not account for the frequency dependent hysteresis losses [96] as seen in Figure 4.25, left picture.

Fig. 4.23: Comparison of measured and simulated *BH*-loops for Ferroxcube TN13/7.5/5-3F4 at different frequencies. Left 10kHz. Right: 100kHz.

The losses in a ferrite material with its associated BH-loop can, as previously shown, be modeled with the Jiles-Atherton model in Simplorer. The importance of correct hysteresis modeling is important since e.g. equally sized ferrite toroidal cores with different ferrite materials will show significantly different frequ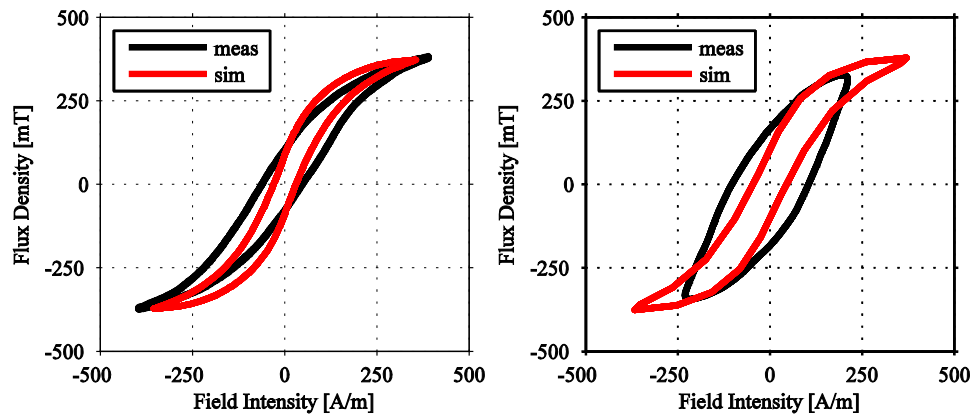ency behavior, see Figure 4.25 left picture. By combining the Jiles-Atherton model with resistances to represent copper losses and an intrawinding capacitor with associated damping resistor, see Figure 4.24, a good frequency response can be obtained for the inductor model. The model is found to be versatile and easy to parameterize which is demonstrated in Figure 4.25, right picture, where the measured frequency response is compared with a Simplorer simulation for a Ferroxcube TN13/7.5/5-3F3 inductor with 20 turns.

$$L_\lambda = 30nH \qquad C_w = 3.7pF$$
$$R_w = 10m\Omega \qquad R_m = 1e5$$
$$R_1 = 1600\Omega \qquad l_e = 30.1mm$$
$$R_2 = 50\Omega \qquad A_e = 12.2mm^2$$
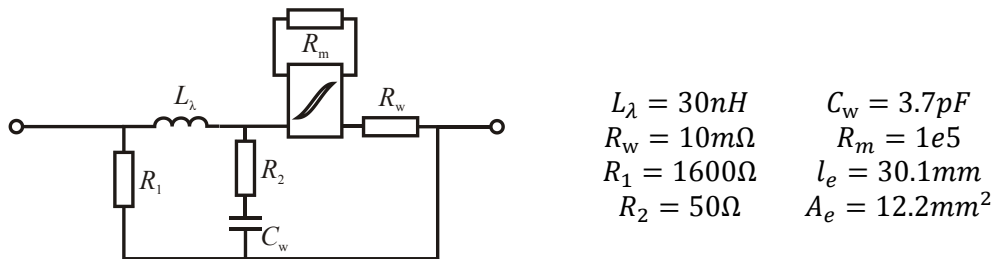
Fig. 4.24: Schematic of the investigated inductor model with associated parameters for Ferroxcube TN13/7.5/5-3F3 inductor with 20 turns.
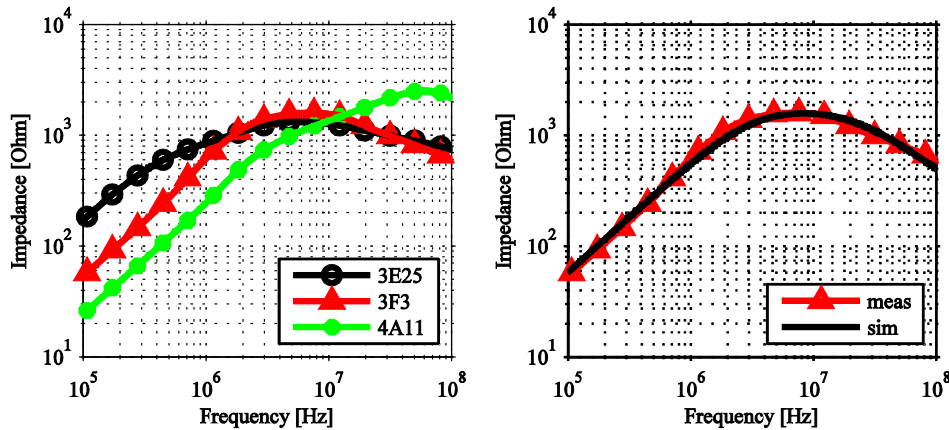
Fig. 4.25: Left: Measured impedance of similarly sized ($\emptyset d = 13mm$, $h = 5.4mm$, $n = 20$) inductors with different ferrites. Right: Comparison of measurements and Simplorer simulations for Ferroxcube TN13/7.5/5-3F3, $n = 20$.

The second important aspect that determines the high frequency performance of an inductor is the winding technique of the core. Many parameters such as distance between the windings, the number of windings and the winding

technique will affect the interwinding capacitance of the inductor. Modeling of the different wire techniques can be accounted for by different size of C_W (see Figure 4.24 for illustration) in the Simplorer model. The topic of how to reduce interwinding capacitances is very wide and will not be covered in detail in this thesis. However, an illustration of the winding importance is given in Figure 4.26 where the same inductor core is wound with three different winding techniques; round wire, planar windings and Litz wire. As described in Section 2.1.4, planar windings are often used in high power applications since it gives a possibility to utilized windings with high current handling capability. The winding type affects the impedance of the inductor at higher frequencies and must be considered if correct high frequency properties are needed for an inductor.
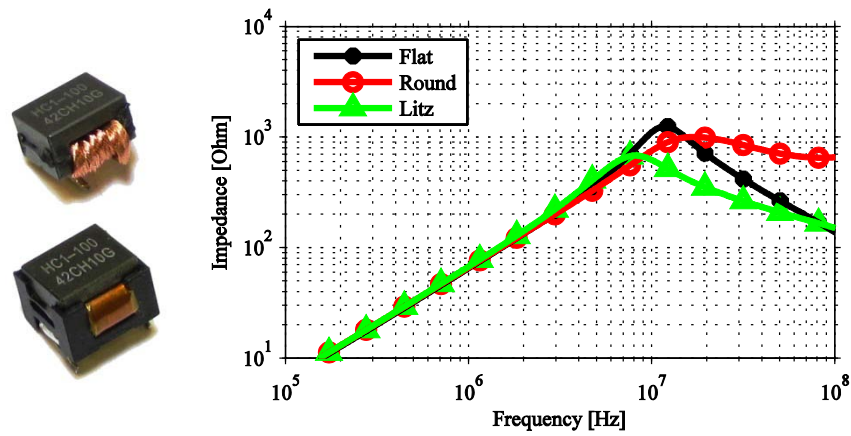
Fig. 4.26:   Measured impedances of similar ferrite cores with different winding techniques.

Not only toroidal inductors are of interest when a switched converter is investigated, the previously derived inductor model can also be applied on transformers. To determine the total frequency characteristics of a transformer, four different measurements are needed; measurements on the primary with the secondary side open, the secondary side shorted and vice versa, i.e. both sides are measured on. This gives an extensive coverage of all parasitic elements; e.g. is the leakage inductance in parallel with the interwinding capacitance obtained by shorting the secondary side. These measurements were performed on a ferrite core (EFD12/6/3.5-3F3 with 160um air gap, $N_1 = 21$, $N_2 = 6$) to illustrate the versatility and adaptability of the model in Figure 4.24. By adding a secondary winding to the model, a comprehensive simulation model of a transformer that accounts for parasitic effects up to well over 100MHz is obtained, see Figure 4.27 for comparison between Simplorer simulations and measurements.
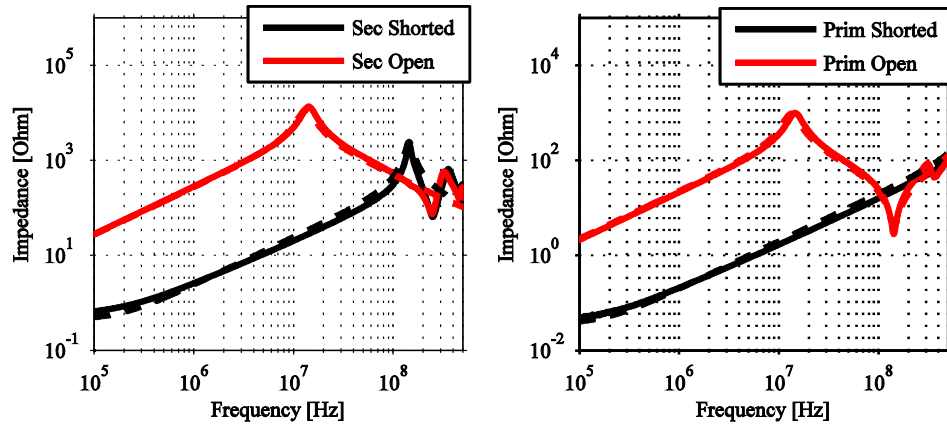
Fig. 4.27: Measured (solid line) and simulated (dashed line) frequency characteristics of transformer EFD12/6/3.5-3F3. Left: measurement from primary to secondary side. Right: measurement from secondary to primary side.

4.1.6 Temperature Effects in Ferrites

Another aspect that needs to be taken into account for full coverage of all sources of EMI is the temperature dependence in the ferrite material. As the temperature increases, the saturation flux density and the field strength in the material reduces almost linearly for a soft ferrite material [97]. These statements have been verified in the measurements where a higher temperature needs a lower flux density to saturate the material, see Figure 4.28 where the BH-loop is measured for a toroidal ferrite core from Ferroxcube (TN13/7.5/5-3F4) at two different temperatures. As the temperature increases, the decreased area of the hysteresis loop gives rise to lowered losses and the decreased permeability gives rise to a slightly lowered inductance. Note that temperature effects are not included in the earlier discussed Simplorer hysteresis model; this might be a source of error worth considering if correct EMI properties at high temperatures are needed.
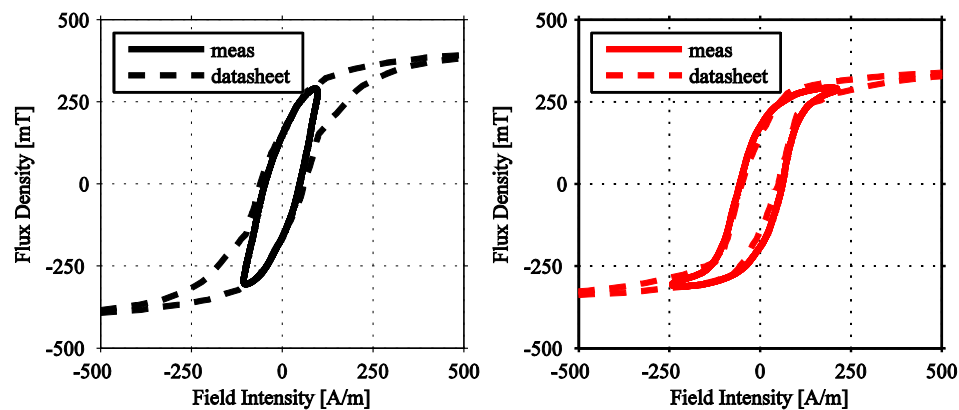
Fig. 4.28: Comparison of measured *BH*-loops for Ferroxcube TN13/7.5/5-3F4 at different temperatures. Left 25°C. Right: 100°C.

4.2 Diodes

4.2.1 Static Performance

The static behavior of a diode is rather simple to describe with the Standard Shockley equation as implemented in most simulation software's such as Ansoft Simplorer and SPICE. Manufacturers often provide SPICE models for their devices which model the static behavior in a good way, see Figure 4.29 that shows a comparison of SPICE simulations of the manufacturer model with measurements and datasheet values for the soft recovery diode 20ETF10 ($20A, 1000V$) from International Rectifier. All measurements of diode iv-characteristics are made with the ramp circuit described in Section 3.2. The diode is intended for rectifier applications where the forward voltage drop is of more importance than the switching characteristics. Since the diode has a high blocking voltage, the intrinsic layer causes a resistive voltage drop within the diode which this accounted for by the term RS in SPICE model. This resistive voltage drop is seen in the iv-characteristics as a linear increase in current as the forward voltage drop increases.
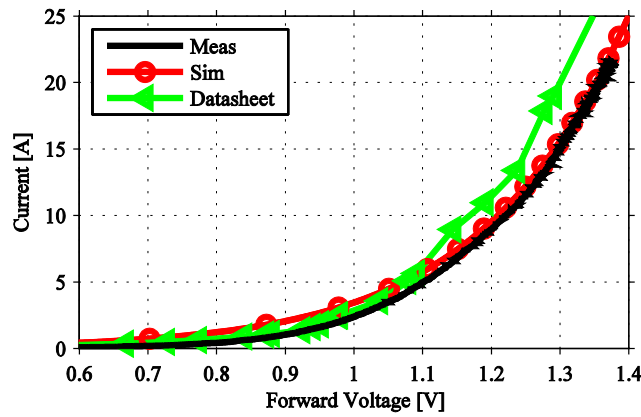
Fig. 4.29: Forward voltage vs. current for 20ETF10. Comparison of SPICE model, measurements and datasheet values.

The static behavior is often described by the standard Shockley equation which makes curve fitting easy to perform for a diode where no manufacturer SPICE model is available [98]. The iv-characteristics for the diode FFPF10UP60S can be expressed as

$$I_F = I_S \left[exp\left(\frac{V_D - I_F \cdot RS}{N \cdot V_t}\right) - 1 \right] \tag{4.1}$$

where the fitted parameters are $I_S = 2 \cdot 10^{-4}$, $N = 5$ and $RS = 0.65$, see

Figure 4.30 that show a comparison of the measured iv-characteristics, datasheet values and a curve fitted model according to (4.1). The investigated diode FFPF10UP60S is a 600V/10A general purpose switching diode with ultrafast soft reverse recovery ($58ns@I_F = 10A$) well suited for freewheeling applications.
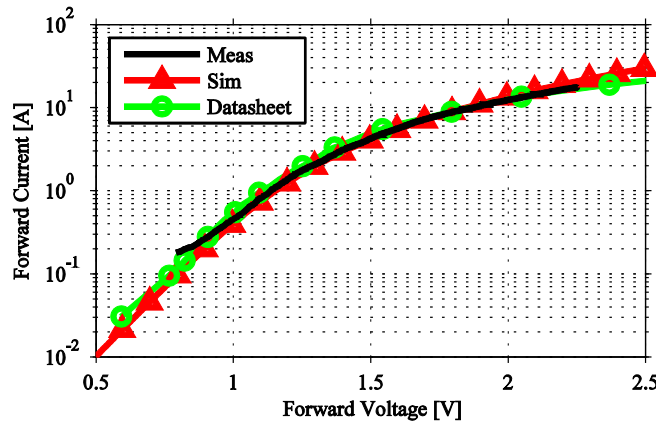
Fig. 4.30: Forward voltage vs. current for FFPF10UP60S. Comparison of curve fitted Simplorer model, measurements and datasheet values.

The Shockley equation and curve fitting procedure is not only valid for medium voltage switching diodes, but can also be applied to low voltage switching diodes and Schottky diodes, see Figure 4.31 that shows the iv-characteristics for the Schottky diode 43CTQ100 ($20A, 100V$). Note that since a Schottky diode shows a rather steep iv-characteristic curve which gives a more inadequate curve fit for the Shockley equation for lower currents. As the current through the device increases, the Shockley equation is rather well adapted to the measured iv-characteristics.
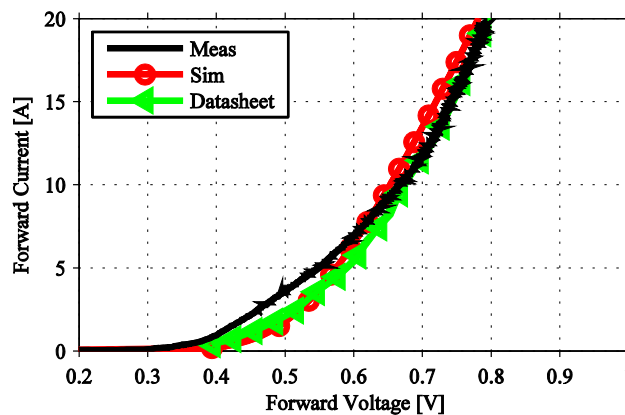

Fig. 4.31: Forward voltage vs. current for 43CTQ100 Schottky diode. Comparison of curve fitted Simplorer model, measurements and datasheet values

From these measurements it is concluded that the static diode performance can be simulated in a satisfactory way for most types of diodes that can be found in a low and medium power switched converter. The *iv*-characteristics are well represented whether a manufacturer model or manual curve fitting with the standard Shockley equation is used.

4.2.2 Determining the Junction Capacitance

From the measurements preformed with the test circuit described in 3.5, it can be concluded that the diode capacitance in SPICE described by (2.10) and (2.9) represent the capacitance adequately for many types of diodes. An example is shown in Figure 4.32 where measurements on a varactor (ZC836) with a well defined capacitance are compared with SPICE simulations with good agreement.

Fig. 4.32: Analysis of the junction capacitance in the ZC836 varactor. Left: Measured voltage with the test circuit in Section 3.5. Right: comparison of the measured and simulated capacitance.

According to Lucia [99], the total junction capacitance shows a frequency dependence that becomes apparent when the diode is forward biased. This dependence originates from the diffusion capacitance that dominates the total junction capacitance when the diode is forward biased; for low frequencies, the minority carriers that constitute the physical meaning of the capacitor will follow the applied AC-signal. However, since this thesis deals with diodes used in switching applications, the effect of small signal variations in the diffusion capacitance becomes comparably small and therefore neglected. When the diode is reverse biased, the capacitance can be considered independent of the measurement frequency [99-101]. Hence is the test frequency is selected to 1MHz in accordance with the de facto standard given in most data sheets.

The depletion capacitance is often well represented by the manufacturer models,

but some deviations have been found. Figure 4.33 shows a comparison of measured and simulated junction capacitance for the fast recovery diode UF4004; a rather large discrepancy can be seen between the SPICE simulations and the measurements. One explanation of this deviance in capacitance between measurements and the SPICE model comes from the fact that the junction capacitance and the transient behavior sometimes is seen as a not so important parameter in the diode model; in a rectifying circuit, the static behavior (conduction losses and forward voltage drop) is of greater importance.
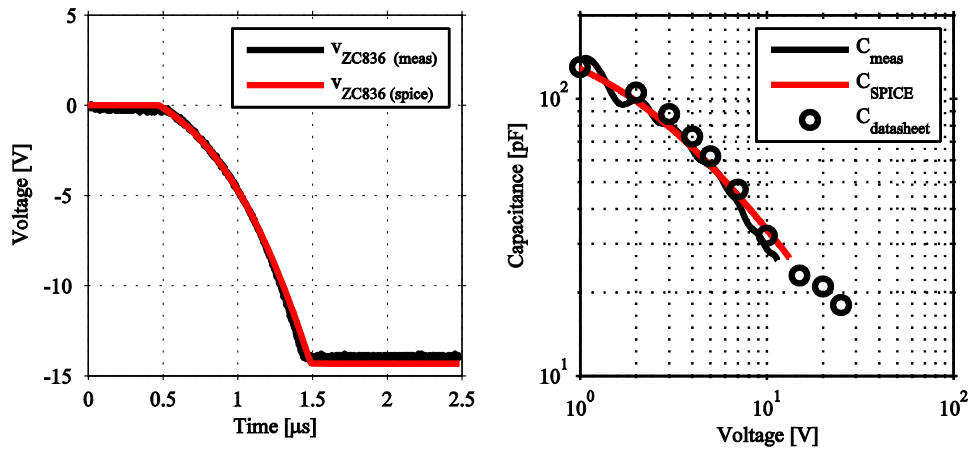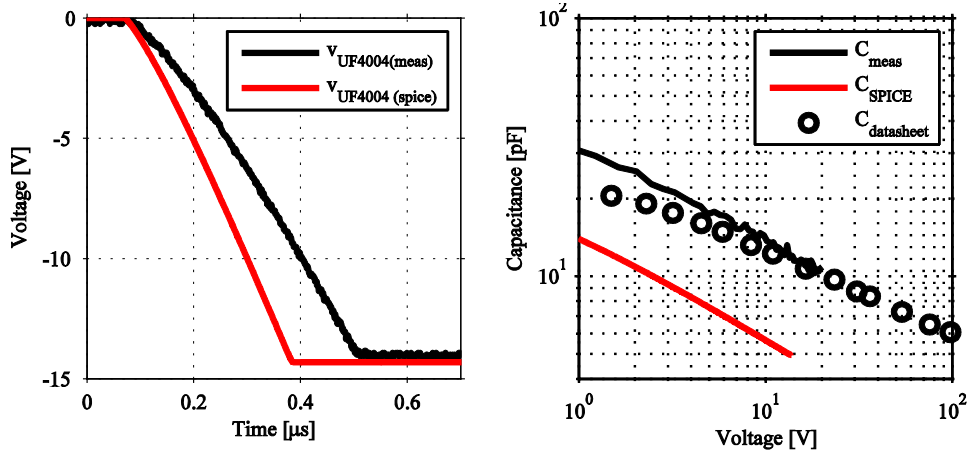

Fig. 4.33: Analysis of the junction capacitance in diode UF4004. Left: Measured voltage with the test circuit in Section 3.5. Right: comparison of the measured and simulated capacitance.

If a manufacturer model is not available, the equation that governs the junction capacitance can either be fitted to the SPICE equation (2.7) or to the Simplorer equation according to

$$C_j = C_j(0) \left[\delta_j \frac{1 - \delta_j}{\left(1 - \frac{v_{\text{applied}}}{V_{\text{bi}}}\right)^{\alpha_j}} \right]. \tag{4.2}$$

The validity of the fitting is illustrated for the previously analyzed diode FFPF10UP60, see Figure 4.34, left picture, where datasheet values are compared with the fitted parameters in (4.2) and measurements. The fitted terms are $V_{\text{bi}} = 0.6V$, $C_j(0) = 51.4\text{pF}$, $\delta_j = 0.1$ and $\alpha_j = 0.6$ and if they are correctly fitted, the Simplorer equation represent the junction capacitance well.

The SPICE and Simplorer capacitance equations are also valid for Schottky diodes as seen in Figure 4.34, right picture, where a low-voltage high-speed Schottky diode (32CTQ030) is analyzed. The difference in capacitance between a

pn-diode and Schottky diode is the lack of minority carriers which contribute to the diffusion capacitance when the diode is forward biased. This difference is not apparent as long as the diode is reverse biased, hence is good agreement obtained between simulations and measurements.
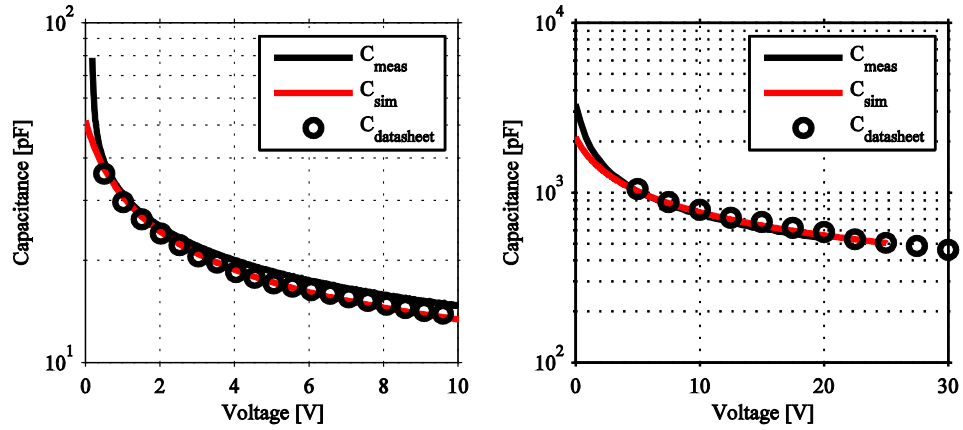
Fig. 4.34:   Analysis of the junction capacitance in different diodes. Left: *pn*-diode FFPF10UP60 with datasheet values, fitted parameters in (4.2) and measurements. Right: Schottky diode 32CTQ030. Comparison of datasheet values, SPICE model and measurements

The main conclusion that can be drawn is that the diode capacitance is well described by the general SPICE and Simplorer equations as long as the diode is reverse biased. The validity of the equations that determine the diffusion capacitance when the diode is forward biased is not verified in this thesis.

4.2.3   Validation of the Reverse Recovery

The recovery current is however not trivial to model due to its complex shape and its dependence on both operating conditions and semiconductor properties. The most significant factors that determine the shape of the reverse recovery current are the forward current, the current derivative during the recovery phase and the carrier lifetime (τ) within the diode. The time integral of the reverse recovery current (Q_{RR}) is dependent on the amount of charges that needs to be swept out; a high forward current will therefore result in a high amount of accumulated charges and consequently a greater recovery peak. This is illustrated in Figure 4.35, right picture, where the measured (see Section 3.3 for measurement setup) reverse recovery currents and voltages are presented for different forward currents. The current derivative during the recovery phase mostly affects the recovery peak; a higher derivative mainly gives a higher recovery peak when the internal charges are swept out. The semiconductor properties determine the shape of the tailing recovery current; the carrier distribution and doping levels within the diode can be modified so that soft or snappy tailing currents can be obtained.

The recovery current also shows an indirect dependence on the reverse voltage over the diode, see Figure 4.35, right picture. This dependence does not originate from the voltage applied over the diode directly but rather the current derivative. By assuming that the switching action is much faster than the diode, the current derivative during the commutation is determined by

$$\frac{di_F}{dt} = -\frac{V_R}{L_\sigma} \tag{4.3}$$

where V_R is the applied reverse voltage and L_σ is the stray inductance. A higher reverse voltage will consequently give a higher current derivative which in turn will increase the recovery peak. The shape of the current during the recovery phase is determined by the type of diode and in Figure 4.35 is a standard recovery rectifier diode (20ETS12) used to illustrate the relationships.
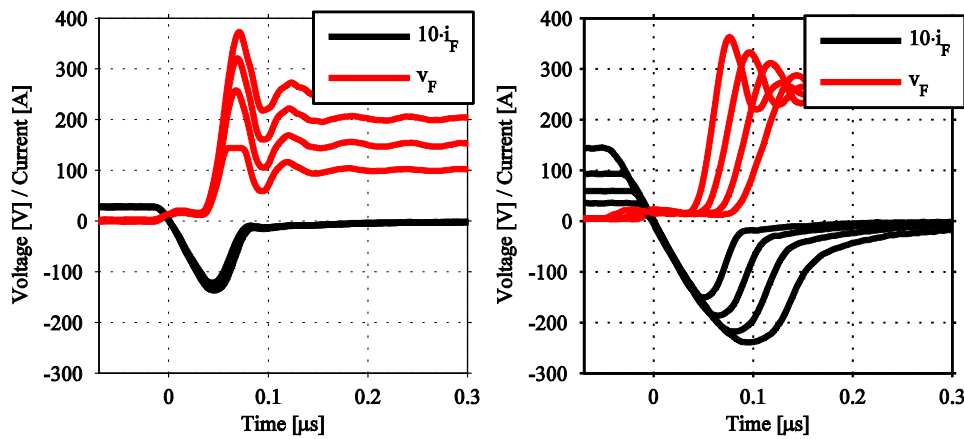
Fig. 4.35: Measured reverse recovery current as a function of the operating conditions. Left: Constant current, varying reverse voltage ($I_{forward} = 6A$, $V_{reverse} = 100V, 150V, 200V, 250V$). Right: Constant voltage, varying forward current ($I_{forward} = 3.3A, 5.7A, 9.3A, 14A$, $V_{reverse} = 250V$).

As previously described, the reverse recovery behavior is inadequately simulated in SPICE due to the fact that charge storage in the depletion layer is not included. This is illustrated in Figure 4.36 where measurements are compared with SPICE simulations for the previously analyzed rectifier diode 20ETS12. From the simulations and measurements it can be seen that the switching behavior of a *pn*-diode is not sufficiently well described in SPICE [93]. Hence, a different diode model is needed if it is to be used as a part of a switched application. However, the SPICE model might still be useful for other applications e.g. static calculations where only the forward voltage drop is considered.

The most suitable diode model for switching applications is found to be the diode

model in Ansoft Simplorer due to its extensive description of the recovery current with mathematical expressions and time constants. To illustrate the eligibility of the Simplorer model, the previously fitted diode FFPF10UP60S described in (4.1) and (4.2) are expanded with reverse recovery features. Several parameters needs to be fitted to the model by analyzing measurements at different operating conditions and the result is a diode model that adapts well to different operating conditions. Previous reasoning stated that the reverse recovery current is strongly determined by the forward current which is taken into account in the model by making the lifetime dependent on the current, see Figure 4.37 where two different forward currents are analyzed for the same diode model (FFPF10UP60S) in Simplorer. Theoretically is the peak reverse recovery current linearly dependent on the forward current but for high forward currents, the peak reverse current can be saturated due to emitter injection.
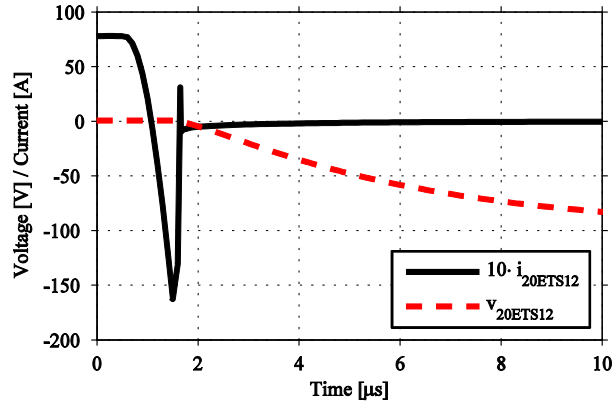

Fig. 4.36: Reverse recovery current for 20ETS12 from SPICE simulations. $I_F = 0.7A$, $V_{reverse} = 100V$
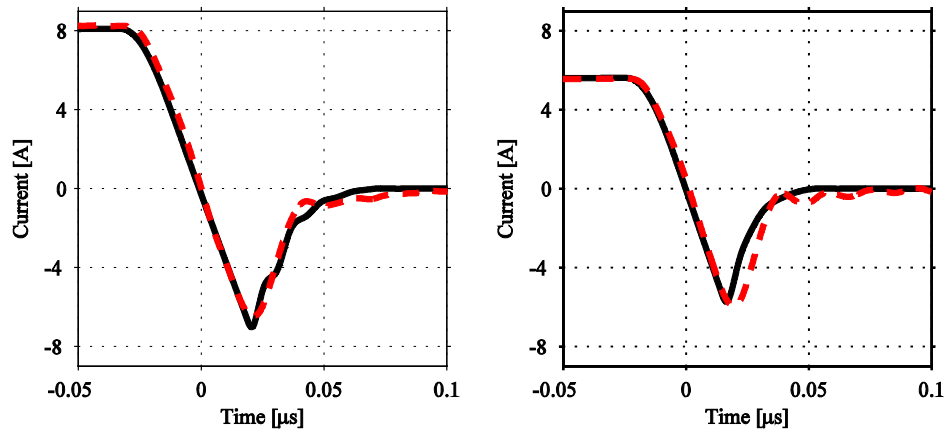

Fig. 4.37: Comparison of Simplorer simulations (dashed line) and measurements (solid line) of the reverse recovery current as a function of I_F for diode FFPF10UP60S. Left: $I_F = 8.0A$. Right: $I_F = 5.5A$.

The second criterion that determines the reverse recovery current is the current derivative during turn off. If a given charge (Q_{RR}) is to be swept out of the intrinsic region, an increase in di/dt will result in an increased reverse current peak. In Figure 4.38, left picture, is the current derivative varied by changing the turn off speed of the switch which in turn results in peak reverse current variations. The Simplorer model takes variations of the reverse recovery due to current derivative variations into account which makes it suitable for switching applications.
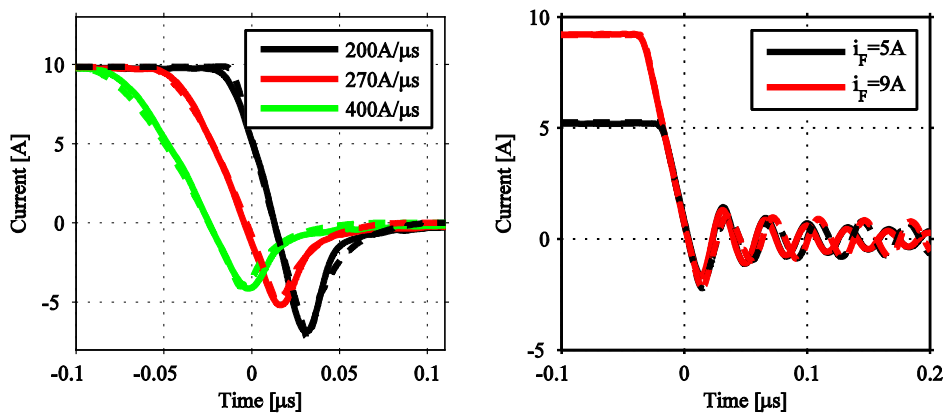
Fig. 4.38: Left: Reverse recovery current in FFPF10UP60S as a function of the current derivative during turn off ($I_F = 10A$, $V_{\text{reverse}} = 200V$). Comparison of measurements (solid) and Simplorer simulations (dashed). Right: Reverse recovery current for Schottky diode 43CTQ100, comparison between SPICE (dashed) and measurements (solid).

If a Schottky diode is analyzed, it shows none or very small reverse recovery current since it is a majority-carrier device. The relatively large capacitance can however give a recovery current similar to the one found in a *pn*-diode; see Figure 4.38, right picture, that shows the recovery event for SPICE simulations and measurements. The small difference is seen in the resonance frequency determined by the parasitic elements in the circuit. Since previous measurements have shown that the SPICE representation of the Schottky capacitance is correct, the discrepancy in resonance frequency most likely lie originate from inadequately represented parasitic inductances and capacitances within the PCB.

4.2.4   Temperature Effects of Diode Performance

The temperature of the diode is affecting both the static and dynamic performance of the component since the semiconductor parameters show strong temperature dependence, see Table 4.1 that present the most common textbook equations of how the temperature affects the semiconductor properties [102]. These parameter

variations are taken into account in the Simplorer diode model by implementation of both linear and exponential temperature coefficients.

Table 4.1   Equations describing temperature dependence of various semiconductor properties in silicon.

Parameter	Temperature Depencence Equation
Carrier Lifetime	$\tau_{HL} = 5 \cdot 10^{-7} \left(\dfrac{T}{300}\right)^{1.5}$
Electron Mobility	$\mu_n = 1400 \left(\dfrac{300}{T}\right)^{2.5}$
Hole Mobility	$\mu_p = 450 \left(\dfrac{300}{T}\right)^{2.5}$

Since both the electron and hole mobility decreases with temperature, the forward voltage drop will increase as the temperature increases for a given forward current. This prevents thermal runaway in a diode and is accounted for in the Simplorer model by temperature coefficients of N and IS in (4.1). The result is a diode model with iv-characteristics that adapts well to the component temperature. This is illustrated in Figure 4.39 that shows a comparison of simulation results from the Simplorer model with temperature compensation and measurements for two different temperatures and two different diodes.
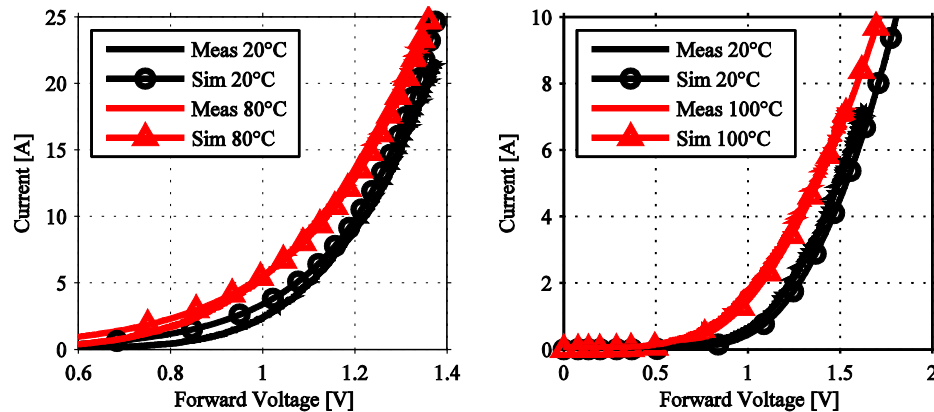
Fig. 4.39:   Comparison of Simplorer simulations and measurements. V_F vs. I_F for different temperatures. Left: 20ETS12. Right: FFPF10UP60S.

The diode junction capacitance is also affected by the temperature since and one of the reasons it that it is inversely proportional to the depletion region width which in turn is affected by the strongly temperature dependent carrier density in the semiconductor. Since the carrier density increases with temperature, less width is required to store the required charge and hence will the depletion region

decrease and consequently will the junction capacitance increase [103]. This is accounted for by a capacitance temperature exponent in Simplorer which gives a model that also takes changes in junction into account, see Figure 4.40.
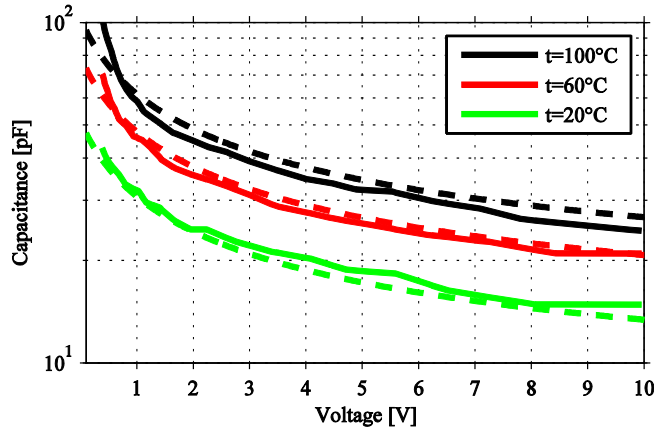
Fig. 4.40:   Diode capacitance in FFPF10UP60S as a function of reverse voltage for different temperatures. Dashed line: Simplorer capacitance from (4.2) plus temperature coefficients. Solid line: datasheet values.

The change in junction capacitance in combination with increased carrier lifetime due to increased temperature also affects the dynamic performance of the diode. Since it takes longer time for the charges to recombine during the reverse recovery process, the sweep out time will take longer which gives a greater reverse recovery current, see Figure 4.41.
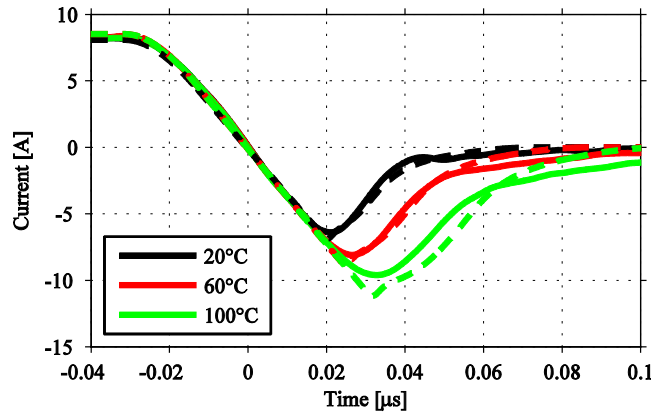
Fig. 4.41:   Reverse recovery in FFPF10UP60S for different temperatures, constant current $I_F = 8A$. Dashed line: Simplorer simulation. Solid line: measurement.

Also, due to the increased carrier life time, the shape of the tailing recovery current can change, this factor is much more difficult to take into account in the model, but the general change in recovery due to temperature is still accounted for in a satisfactory way.

4.3   MOSFET

4.3.1   Nodal Analysis vs. State Variable Approach

In most electric circuit simulator, nodal analysis is used where a consistent set of simultaneous equations is obtained by invoking Kirchhoff's current law for each node in the circuit. This gives an equation system that is simple to solve, eay to implement in a graphical interface and has low computational time. However, the focus of the model proposed in this thesis is aimed at investigating the stability of the system by using transfer functions and developing suitable controller structures. These properties make state space representation more suitable rather than nodal analysis and is therefore used for the forthcoming investigation. The general state-space equations can be expressed as

$$
\begin{aligned}
\dot{x}(t) &= f\big(x(t), u(t)\big) \\
y(t) &= g\big(x(t), u(t)\big)
\end{aligned}
\tag{4.4}
$$

where $x(t)$ is the states, $u(t)$ is the input to the system and $y(t)$ is the output of the system. If (4.4) is applied to a linear system, it can be rewritten as

$$
\begin{aligned}
\dot{x}(t) &= \mathbb{A}x(t) + \mathbb{B}u(t) \\
y(t) &= \mathbb{C}x(t) + \mathbb{D}u(t)
\end{aligned}
\tag{4.5}
$$

where $\mathbb{A}$, $\mathbb{B}$, $\mathbb{C}$ and $\mathbb{D}$ are matrixes. The use of the state space representation is not limited to systems with linear components and zero initial conditions which makes it suitable for the analysis performed in this thesis.

4.3.2   A Novel Model Based on Circuit Analysis

The proposed MOSFET model is depicted in Figure 4.42. The main elements are the current generator, I_{DS}, determining the drain-source current, and the capacitors C_{GS}, C_{GD} and C_{DS} that emulates the charge accumulations in the semiconductor. All external connectors have a resistance, R_S, R_D and R_G, that simulates the built in ohmic losses in each terminal. In addition to the resistance in each terminal, a parasitic series inductance, L_S, L_D and L_G, is introduced.

The drain-source current (I_{DS}) is determined as a function of the applied gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) by equations that are taken directly from SPICE [60]. When V_{GS} exceeds V_{th} and the MOSFET is operating in the linear/ohmic region ($V_{GS} - V_{th} \geq V_{DS}$), the drain source current is described as
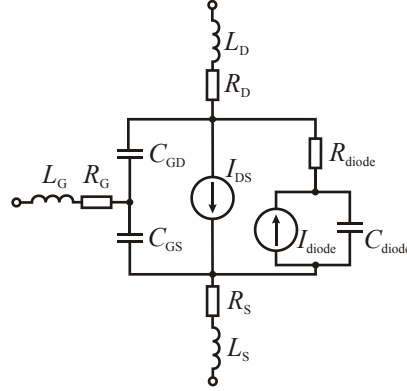
Fig. 4.42: Circuit diagram for the proposed MOSFET model

$$I_{DS(linear)} = \frac{\mu W_{eff} C_{ox}}{L_{eff}} \left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS}) \qquad (4.6)$$

where several constants (μ, W_{eff}, C_{ox}, L_{eff}) scale the current to a suitable level. The SPICE constant λ that models the channel length of the MOSFET is also introduced. Usually λ has a very low value and causes only a small slope on the output characteristics, mostly in the active region. In the active/saturated region ($V_{GS} - V_{th} < V_{DS}$), the drain-source current can be described as

$$I_{DS(saturation)} = \frac{\mu W_{eff} C_{ox}}{2 L_{eff}} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \qquad (4.7)$$

where the channel length modulation parameter λ once again is present. As described in Section 2.3.4, a feature of the VDMOS is the internal body-diode which is modeled by a current source (I_{diode}), an internal series resistor (R_{diode}), and a junction capacitor (C_{diode}). This model can be compared with the SPICE model for regular *pn*-junction diodes [60] and can also be found in SPICE models for power MOSFET's provided by manufacturers.

Figure 4.42 contain six energy storing elements whose voltage or current are selected to form the state matrix

$$x(t) = \begin{bmatrix} v_{CGS} \\ v_{CGD} \\ v_{Cdiode} \\ i_G \\ i_D \\ i_S \end{bmatrix} \qquad (4.8)$$

where the current through an inductor or the voltage over a capacitor will

constitute a state. For a functional circuit, the MOSFET model is implemented in a circuit together with appropriate external elements. The inputs $(u(t))$ and the outputs $(y(t))$ to the system are selected in an appropriate way to form a state-space model of the total system.

4.3.3 Parameter Extraction for a Power MOSFET

To be able to simulate the performance of the component, parameter extraction needs to be performed. The procedure suggested in this thesis is based on three different sources of information; datasheets provided by the manufacturer, SPICE models provided by the manufacturer and component measurements. A flowchart of how the suggested procedure can be performed is found in Figure 4.43.

The value of the parasitic inductor in each terminal (L_S, L_D and L_G,) is not investigated in detail in this thesis; instead are typical values used. This inductance is strongly dependent on the package type and can according to [104, 105] be approximated to 5-15nH for a regular TO-247 package and more than 30nH for larger IGBT power module packages [106]. For all coming simulations where nothing else is specified from the manufacturer, the terminal inductance is set to 5nH since this thesis mainly deals with low power components. In addition to information about inductances, the datasheet also contains information about the voltage dependent capacitors C_{GS}, C_{GD} and C_{DS}. This information is however only valid for one specific operating point and is hence not suitable for the operating range that will appear during a switching event. However can C_{GS} be considered constant [59] and therefore extracted from the datasheet.
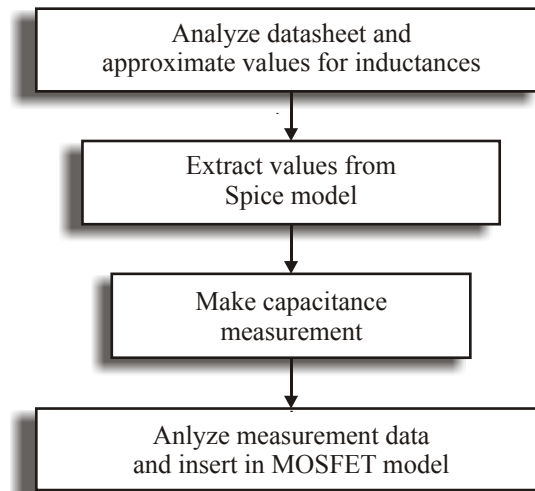

Fig. 4.43: Procedure for extracting model parameters.

Once the parasitic inductances and C_{GS} are extracted from the datasheet, the SPICE model provided by the manufacturer is used for parameter extraction.

Since the proposed model uses the same equations to calculate the I_{DS} as SPICE, the parameters found in the manufacturer SPICE model can be reused. Also, data for the parasitic body diode and terminal resistances can usually be found in the manufacturer SPICE model. The main difference between the SPICE model and the proposed MOSFET model is the voltage dependent capacitor C_{GD}. The data for this capacitor needs to be measured by an impedance analyzer. Once the measurements are done, data is extracted in order to make C_{GD} dependent on both the gate-source and drain-source voltage, $C_{GD}(v_{GS}, v_{DS})$.

To test the parameter extraction procedure, the HEXFET power MOSFET IRF520N was chosen. The reason to select this component is a suitable voltage and current rating in combination with a detailed SPICE model and datasheet provided from the manufacturer. Table 4.2 shows the most common parameter values for the selected MOSFET. For reasons of simplicity, the parameter extraction procedure is based on typical values and measurements on an individual component in room temperature.

Table 4.2   Parameter values for IRF520N

Parameter	Source	Value
C_{GS}	Datasheet	$C_{GD}(v_{DS})$
C_{GD}	Measurements	$C_{GD}(v_{GS}, v_{DS})$
C_{DS}	SPICE	$C_{GD}(v_{DS})$
L_G	Approximation	$5nH$
L_D	Datasheet	$4.5nH$
L_S	Datasheet	$7.5nH$
R_G	SPICE	2.49Ω
R_D	SPICE	98Ω
R_S	SPICE	$439\mu\Omega$
R_{diode}	SPICE	$11.2m\Omega$
I_{diode}	SPICE	See (2.8)
i_{DS}	SPICE	See (4.6) and (4.7)

4.3.4   MOSFET Model under Static Conditions

The verification of the proposed model can be divided into two parts; static and dynamic behavior. For the static behavior, the experimental set up in Section 3.2 is used. If the states in (4.8) are applied to the system for static testing, the derivatives can be expressed as

$$\dot{x}(t) = \mathbb{A}x(t) + \mathbb{B}u(t) + \mathbb{B}_2 \begin{bmatrix} i_{DS} \\ i_{diode} \end{bmatrix} \qquad (4.9)$$

$$\mathbb{A} = \begin{bmatrix} \dfrac{-1}{C_{GS}RS} & \dfrac{1}{C_{GS}RS} & \dfrac{1}{C_{GS}RS} & \dfrac{1}{C_{GS}} & \dfrac{1}{C_{GS}} & 0 \\[2mm] \dfrac{1}{C_{GD}RS} & \dfrac{-1}{C_{GD}RS} & \dfrac{-1}{C_{GD}RS} & 0 & \dfrac{1}{C_{GD}} & 0 \\[2mm] \dfrac{-1}{C_{diode}RS} & \dfrac{1}{C_{diode}RS} & \dfrac{1}{C_{diode}RS} & 0 & 0 & 0 \\[2mm] \dfrac{-L_D}{L_{sum}} & \dfrac{-L_S}{L_{sum}} & 0 & \dfrac{-L_S R_D - L_D R_G - L_S R_G}{L_{sum}} & 0 & \dfrac{L_S R_D - L_D R_S}{L_{sum}} \\[2mm] \dfrac{-L_G}{L_{sum}} & \dfrac{L_G + L_S}{L_{sum}} & 0 & \dfrac{L_S R_G - L_G R_S}{L_{sum}} & \dfrac{-L_G R_D - L_S R_D - L_G R_S}{L_{sum}} & 0 \\[2mm] \dfrac{-L_D - L_G}{L_{sum}} & \dfrac{L_G}{L_{sum}} & 0 & \dfrac{L_G R_D - L_D R_G}{L_{sum}} & 0 & \dfrac{-L_G R_D - L_D R_S - L_G R_S}{L_{sum}} \end{bmatrix} \tag{4.10}$$

$$\mathbb{B} = \begin{bmatrix} 0 & 0 \\[1mm] 0 & 0 \\[1mm] 0 & 0 \\[1mm] \dfrac{L_D + L_S}{L_{sum}} & \dfrac{-L_S}{L_{sum}} \\[2mm] \dfrac{-L_S}{L_{sum}} & \dfrac{L_G + L_S}{L_{sum}} \\[2mm] \dfrac{L_D}{L_{sum}} & \dfrac{L_G}{L_{sum}} \end{bmatrix} \tag{4.11}$$

$$u(t) = \begin{bmatrix} v_G \\ v_{ramp.} \end{bmatrix} \tag{4.12}$$

$$\mathbb{B}_2 = \begin{bmatrix} \dfrac{-1}{C_{GS}} & 0 \\[2mm] \dfrac{-1}{C_{GD}} & 0 \\[2mm] 0 & \dfrac{-1}{C_{diode}} \\[2mm] 0 & 0 \\[1mm] 0 & 0 \\[1mm] 0 & 0 \end{bmatrix} \tag{4.13}$$

where

$$L_{sum} = L_D L_G + L_D L_S + L_G L_S \tag{4.14}$$

Since no external components are applied to the MOSFET, the only part that limits i_{DS} is the MOSFET itself. The elements that determine the transient characteristics (i.e. C_{GS}, C_{GD} and C_{DS}) become negligible since the voltage ramp applied to the drain-source terminals has a low derivative. This makes it possible to set the normally voltage dependent capacitors to a fixed approximate value during the static simulations. The static characteristic of the model is instead determined by the internal resistances (R_S and R_D) in the MOSFET and the drain-source current which in turn is described as a function of the applied terminal voltages. The equations that govern the static behavior can be found in (4.6) and (4.7) with parameter values taken from the SPICE model, see Table 4.3.

Table 4.3   SPICE parameters for IRF520N, static behavior

Parameter	Source	Value	Unit
VTO	SPICE	2.7908	V
λ	SPICE	0	V^{-1}
L	SPICE	$100 \cdot 10^{-6}$	m
W	SPICE	$100 \cdot 10^{-6}$	m
LD	SPICE	0	m
KP	SPICE	0	A/V^2
CGS0	SPICE	$2.79 \cdot 10^{-6}$	F
CGD0	SPICE	$1 \cdot 10^{-11}$	F

The manufacturer specifies a certain output characteristics in the datasheet, and it is of interest to verify both the SPICE model and the proposed MOSFET against this data, see Figures 4.44 and 4.45.

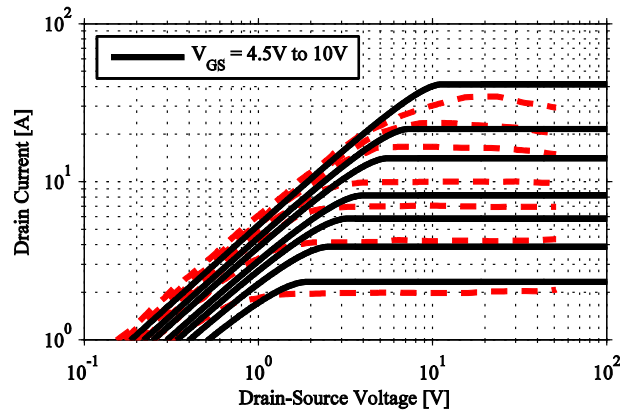

Fig. 4.44:   IRF520N output characteristics. Comparison between SPICE model (solid line) and datasheet (dashed line).
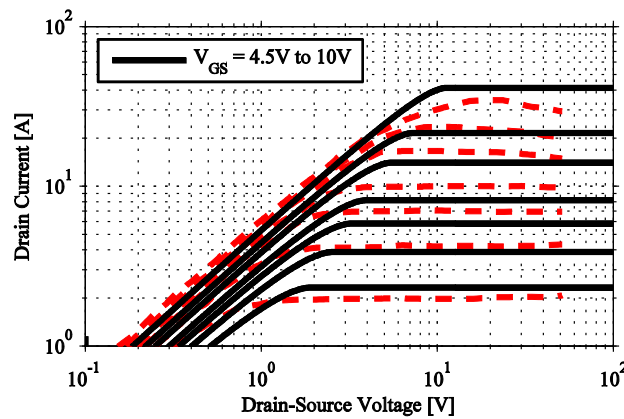

Fig. 4.45:   IRF520N output characteristics. Comparison between proposed model (solid line) and datasheet (dashed line).

The output characteristics correspond quite well both for the SPICE model and the proposed model. The results from both models correspond to each other since they are based on the same equations and use the same input data taken from the SPICE model provided by the manufacturer.

If the investigated MOSFET is tested with the test circuit described in Section 3.2, the output characteristics in Figure 4.46 are obtained. It is concluded that the output characteristics deviate from the data specified by the manufacturer, mainly due to deviations in threshold level (V_{th}). The difference in threshold level can on component level be deduced to variation in process parameters such as oxide thickness, doping levels, but it also shows a temperature dependence [102].
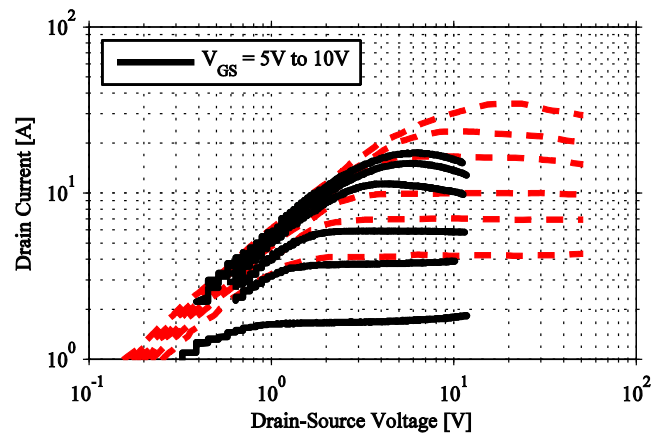
Fig. 4.46: IRF520N output characteristics, comparison between measurements (solid line) and datasheet (dashed line).

The conclusion drawn from the simulations is that the output characteristics are strongly dependent on the individual component. In the datasheet, the span in which the threshold voltage varies can be rather large; for the selected MOSFET, IRF520N, the threshold voltage may vary between $V_{th} = 2V$ and $V_{th} = 4V$. The individual component that was selected most likely has a slightly higher threshold voltage ($V_{th} \approx 3.6V$) than the typical value specified in the datasheet.

To investigate the temperature affects the output characteristics, two measurements were made at two different temperatures, see Figure 4.47. The temperature of the component was selected to 25ºC and 80ºC and was carefully monitored throughout the test in order to keep it as constant as possible. But it is not only the temperature dependency of the threshold voltage that will cause a difference between measurements and simulations. Other parameters such as increased electron mobility with temperature also contribute to deviancies. All together, these dependencies are difficult to take into account due to the complexity of the ingoing parameters; this thesis do not focus on correct modeling of doping levels but rather on simplicity and usability. Due to this, the

temperature is assumed to be 25°C and the threshold voltage to a fixed value for all upcoming analysis with the proposed MOSFET model.
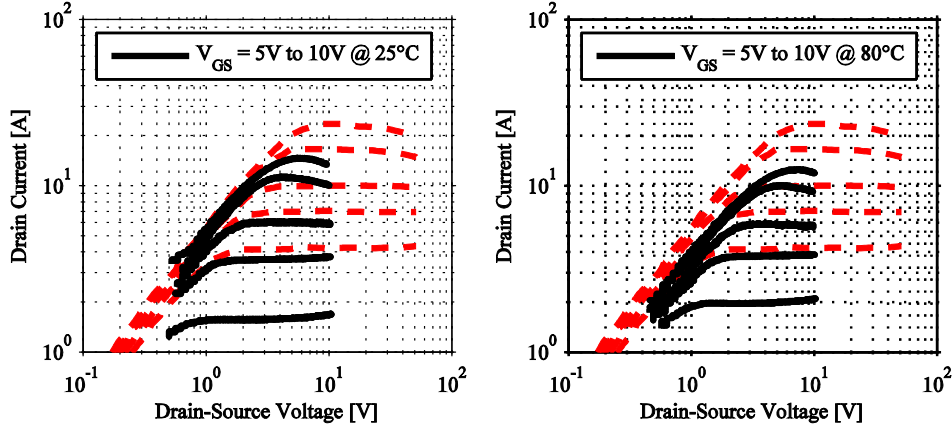
Fig. 4.47: IRF520N output characteristics. Left: 25°C. Right: 80°C.

4.3.5 MOSFET Model under Dynamic Conditions

To describe the total switching characteristics, the capacitors in the model must be given a characteristic that makes them nonlinearly voltage dependent. If a linear capacitor is considered, it can be defined as a component whose charge is a function of voltage. The capacitance is defined as the derivative of charge with respect to voltage according to

$$C(t) = \frac{dq(v_c)}{dv_c} \tag{4.15}$$

where v_C is the voltage applied over the capacitor. The current through a capacitor can then be expressed as the time-derivative of the charge

$$i(t) = \frac{dq(v_c(t))}{dt} \tag{4.16}$$

which in turn can be expanded to

$$i(t) = \frac{dq(v_c(t))}{dv_c(t)} \frac{dv_c(t)}{dt} = C(v_c(t)) \frac{dv_c(t)}{dt}. \tag{4.17}$$

This methodology to model non-linear voltage dependent capacitors are described in [107, 108] and [109, 110]. Some would argue that the current through the capacitor can be described as

$$i(t) = C(v_c(t)) \frac{dv_c(t)}{dt} + v_c(t) \frac{dC(v_c(t))}{dt}. \tag{4.18}$$

but this is wrong as shown in [109]. The error lies in the interpretation of charge; the charge stored in the capacitor equals the capacitance times the voltage change of the capacitor, not the static voltage.

The datasheet provided by the semiconductor manufacturer only presents the internal capacitances, (C_{GS}, C_{GD} and C_{DS}), as a function of the applied voltage for one operating point, see Figure 4.48 where C_{iss}, C_{oss} and C_{rss} refers to the input capacitance, output capacitance and reverse transfer capacitance respectively. Hence, the capacitors must be thoroughly investigated in order to get a more comprehensive description of the switching procedure.
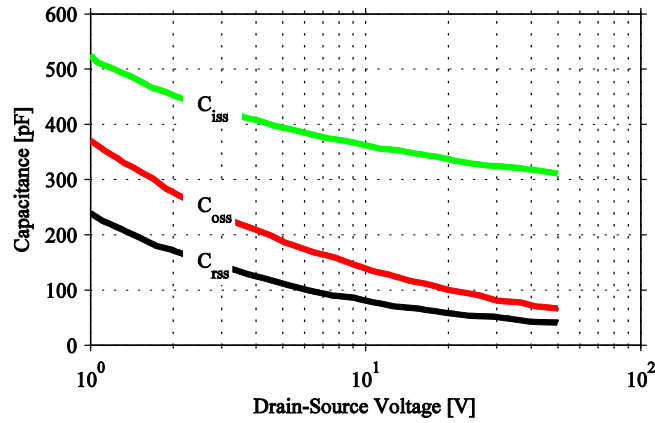
Fig. 4.48: Datasheet values of the capacitances in the MOSFET IRF520N.

One significant difference between the datasheet and the capacitors in the proposed model is how the capacitance is expressed. In Figure 4.48, the capacitors are expressed as

$$\begin{aligned} C_{iss} &= C_{GS} + C_{GD} \quad (C_{DS} \text{ shorted}) \\ C_{rss} &= C_{GD} \\ C_{oss} &= C_{DS} + C_{GD} \end{aligned} \tag{4.19}$$

where C_{iss}, C_{oss} and C_{rss} refers to the input capacitance, output capacitance and reverse transfer capacitance respectively. From these quantities, the capacitances included in the proposed MOSFET model can be calculated as

$$\begin{aligned} C_{GD} &= C_{rss} \\ C_{GS} &= C_{iss} - C_{rss} \\ C_{DS} &= C_{oss} - C_{rss} \end{aligned} \tag{4.20}$$

As seen, it is of great importance that the gate-drain capacitance is measured correctly; with help of this parameter, it is possible to extract information about the other two components. The standard procedure of how to measure these capacitances is described in [111]. This method however lacks some information since the measurements are usually only performed around one operating point. Lembeye et al. [112, 113] suggests a slightly different method to characterize all internal capacitances as a function of the applied voltage with the help of an impedance analyzer. If the suggested method in [112, 113] is performed on the object of investigation (IRF520N) with a HP4395 impedance analyzer, the results shown in Figures 4.49, 4.50 and 4.51 are obtained. These figures show a comparison between measurement and data taken from the datasheet of the capacitance as a function of the applied drain-source voltage.
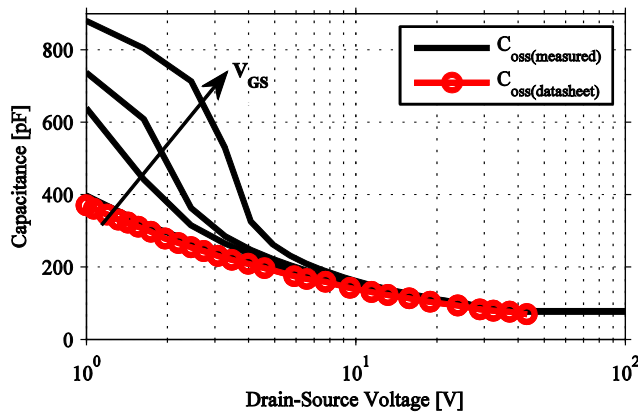

Fig. 4.49: Output capacitance as a function of applied drain-source voltage. v_{GS} is varied between 0V and 3V
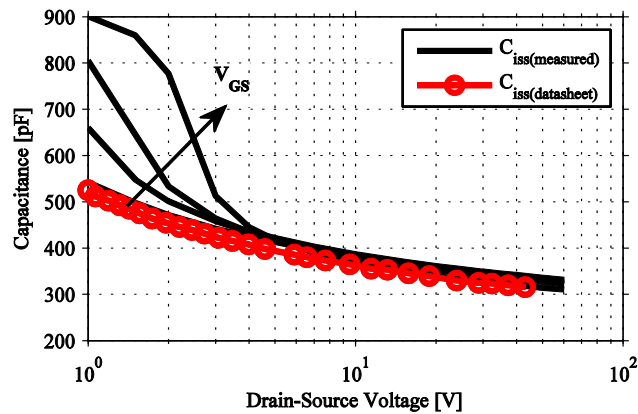
Fig. 4.50: Input capacitance as a function of applied drain-source voltage. v_{GS} is varied between 0V and 2V.

Still, Lembeye [112, 113] takes no consideration of how the gate-drain
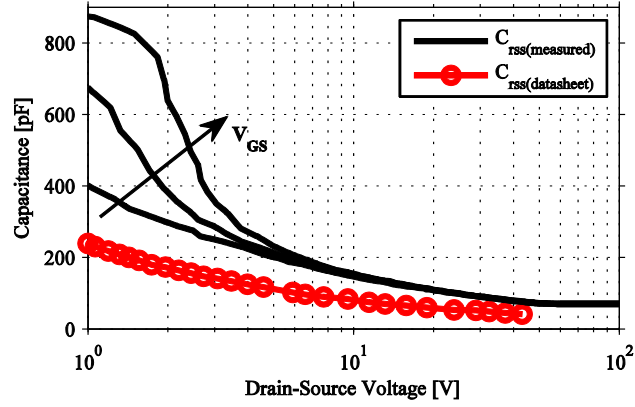
Fig. 4.51: Reverse transfer capacitance as a function of applied drain-source voltage. v_{GS} is varied between 0V and 2V.

capacitance can be represented when the MOSFET is conducting. This phenomenon is described in [114, 115] where it is suggested that the gate-drain capacitance, which is the most crucial component for correct switching behavior, diminishes as the gate-source voltage decreases. The approach used in this thesis is to measure the gate-drain capacitance at the highest possible gate-source voltage before the MOSFET enters the ohmic region and after this point approximate its value based on previous measurements. The final function of how the gate-drain capacitance depends on the applied voltages $\left(C_{GD}(v_{GS}, v_{DS}) \right)$ is depicted in Figure 4.52. If a switching event is analyzed in detail, the operating points found during the course of events can be plotted in the same graph as the gate-drain capacitance, see Figure 4.53.
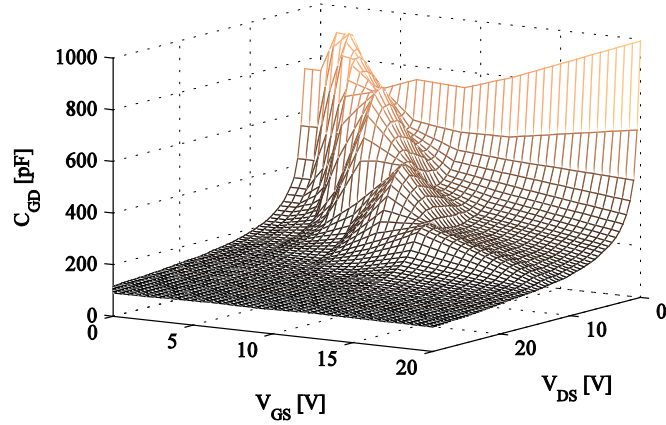
Fig. 4.52: Gate-drain capacitance as a function of v_{GS} and v_{DS}.

The main reason for incorporating the gate-drain capacitor as a function of both v_{GS} and v_{DS} comes from the fact that a switching event is a fairly complex
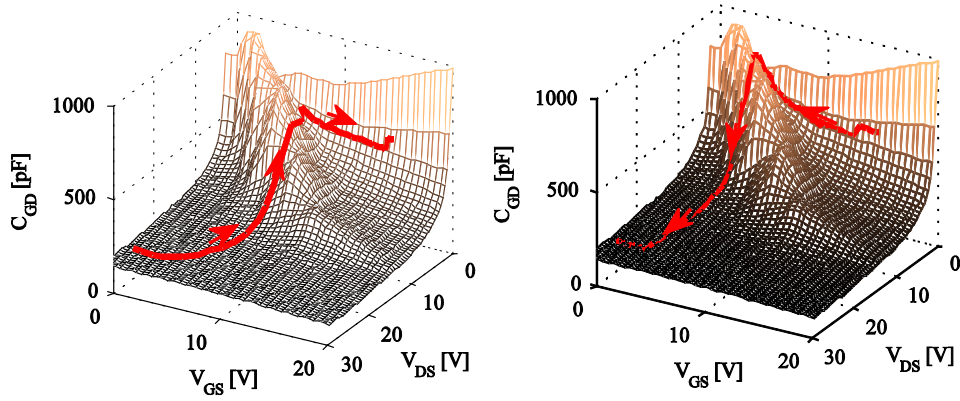
Fig. 4.53: Gate-drain capacitance as a function of applied drain-source and gate-source voltages. Left: Turn-on event marked as a line. Right: Turn-off event marked as a line.

procedure that covers all of the operating areas of a power MOSFET. Figure 4.53 visualizes the fact that as the gate-source voltage increases and reaches the miller-region, an increase of the gate-drain capacitance will occur. Figure 4.54 shows a simulation results from the MATLAB model where C_{GD} is only dependent on v_{DS} as suggested in the datasheet. A small deviance can be seen in all voltages and currents during the switching event. This discrepancy is minimized if the gate-drain capacitance is made dependent on both v_{GS} and v_{DS}, i.e. $C_{GD} = f(v_{GS}, v_{DS})$, see Figure 4.55. Both simulations are compared with the SPICE model which is proven to show good agreement to real measurements.
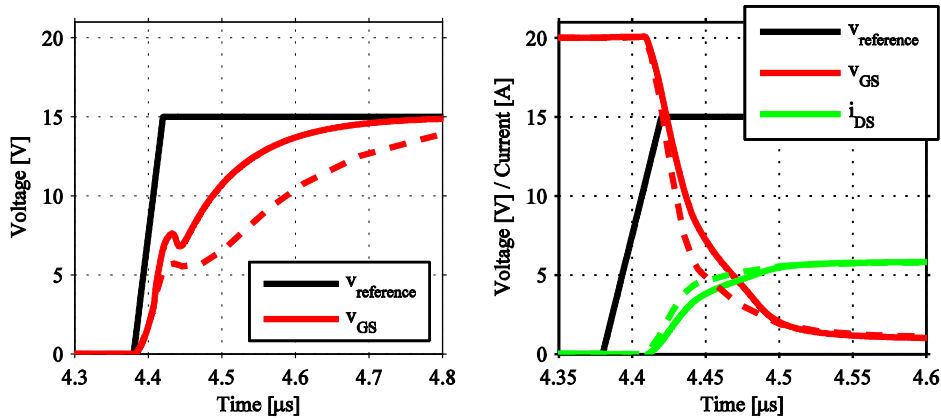
Fig. 4.54: Simulation of switching event where C_{GD} is a function of only v_{DS} according to the datasheet. MATLAB simulations: Solid line. SPICE simulations: Dashed line.
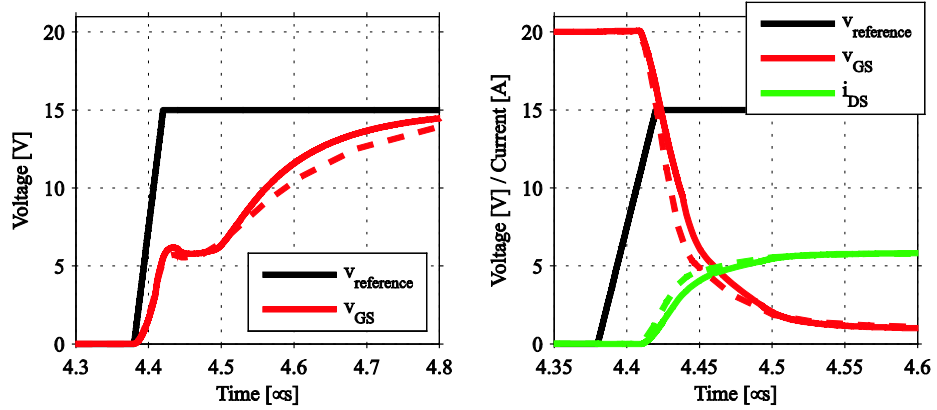
Fig. 4.55: Gate-drain capacitance as a function of v_{GS} and v_{DS}.

As previously mentioned, the gate-source capacitance can be considered almost constant [59] since it mainly consists of the parallel plate capacitor formed by the gate electrode, the substrate and the gate-oxide as a dielectric in between. Since the model proposed in this thesis only deal with positive voltage applied on the gate-terminal, the gate-source capacitance value is chosen to be extracted from the datasheet. The datasheet capacitance can be expressed as

$$C_{GS} = 2.84 \cdot 10^{-9} \exp(-0.0011 \cdot V_{DS}) + 3.55 \cdot 10^{-14} \exp(-0.0056 \cdot V_{DS}) \tag{4.21}$$

if an exponential function is used. The coefficients are calculated using a curve-fitting procedure.
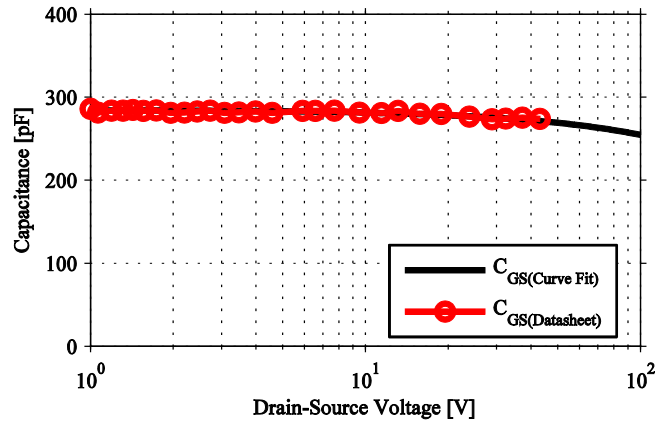
Fig. 4.56: Gate-source capacitance as a function of v_{DS}. Exponential curve fit (solid line) and datasheet values (circles).

The last capacitor that needs to be extracted is C_{DS} which show similar behavior as the capacitance in the pn-junction; it is therefore chosen to obtain the cv-characteristics from the SPICE model where a body diode is present. The parameter values in the capacitance representation are taken from the SPICE model delivered by the manufacturer and can be found in Table 4.4. The diode capacitance, C_{diode}, as a function of applied drain-source voltage can be seen in Figure 4.57. Also, the curve fit taken from SPICE is compared with datasheet values which show good agreement.

Table 4.4   Parameter values for the internal body diode

Parameter	Source	Value	Unit
IS	SPICE	$8.70123 \cdot 10^{-6}$	A
N	SPICE	1.1841	
BV	SPICE	100	V
ISR	SPICE	$IS/2$	A
CJ0	SPICE	$1.909 \cdot 10^{-10}$	F
VJ	SPICE	0.5	V
M	SPICE	0.395	
FC	SPICE	0.1	
TT	SPICE	$1 \cdot 10^{-7}$	s
$V_{thermal}$	SPICE	$25.8 \cdot 10^{-3}$	V
NR	SPICE	2	
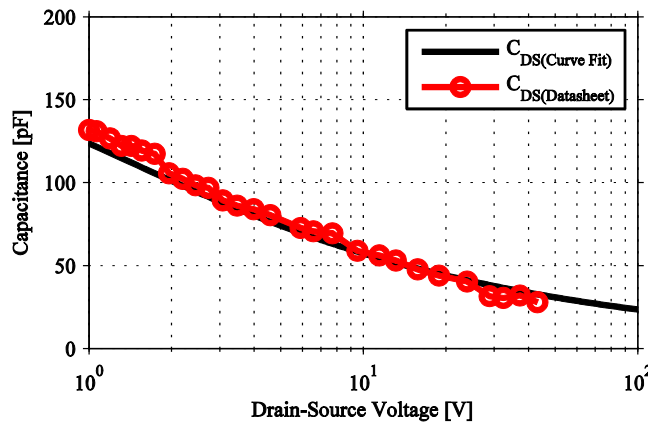
Fig. 4.57:   Drain-source capacitance as a function of v_{DS}. SPICE equations (solid line) and datasheet values (circles).

4.3.6   Switching With Resistive Load

Switching of the MOSFET when the load is purely resistive, e.g. a heating element can be considered the simplest case of switching and is selected as a test circuit for further analysis, see Section 3.4 for test setup. In order to verify the

validity of both the SPICE model and the proposed MOSFET model, results from simulations needs to be compared with measurements. By doing this, it can be seen that the black-box SPICE model provided by the manufacturer shows a switching behavior that corresponds rather well with the measurements, see Figures 4.58 and 4.59.
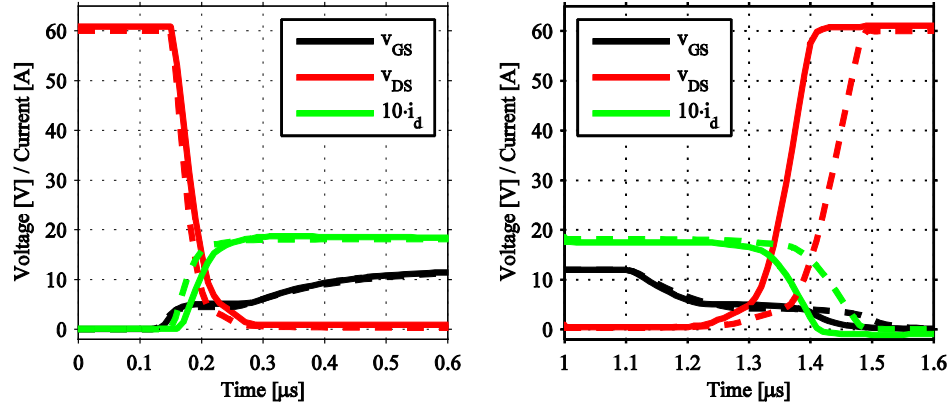
Fig. 4.58: Switching circuit with IRF520N ($R_G = 110\Omega$, $R_{load} = 33\Omega$, $V_{in} = 60V$, $V_G = 12V$). Measurements: solid line. SPICE model: dashed line.
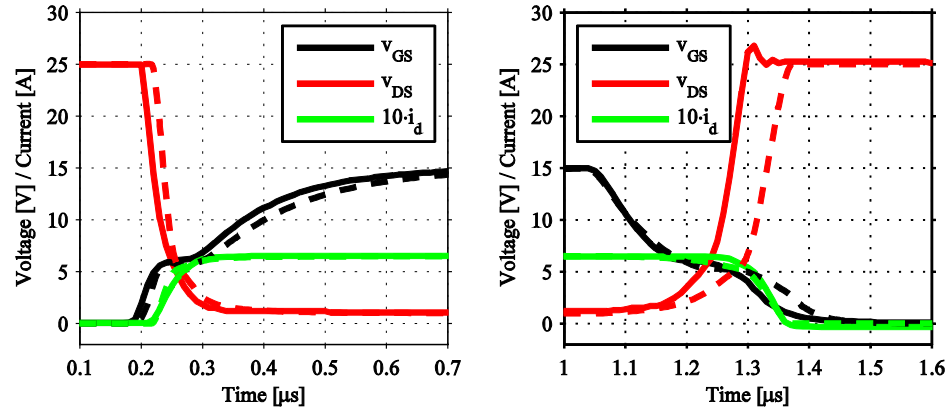
Fig. 4.59: Switching circuit with IRF520N ($R_G = 110\Omega$, $R_{load} = 3.7\Omega$, $V_{in} = 25V$, $V_G = 15V$). Measurements: solid line. SPICE model: dashed line.

The most noticeable difference comes from the turn-off procedure. As the gate-source voltage reaches the miller-region and levels out, the drain-source voltage starts to fall. In the measurement, this event takes much shorter time which might be caused by a difference in the gate-drain capacitance as the MOSFET turns off. Figure 4.60 and 4.61 shows a comparison between measurements and simulations with the proposed MOSFET model.
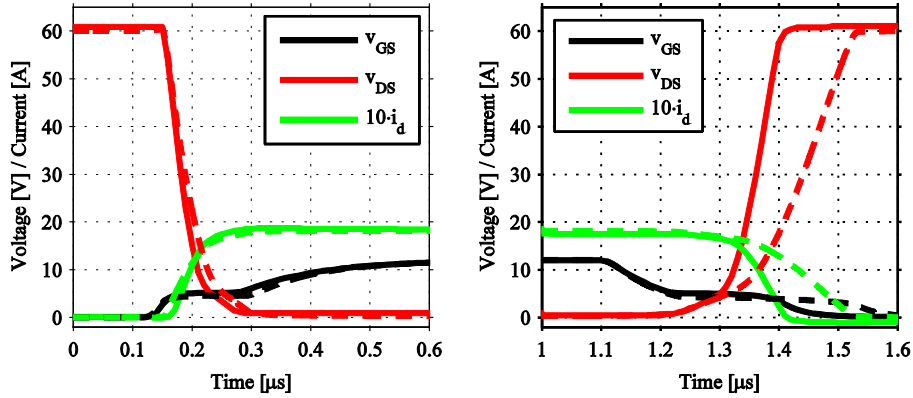
Fig. 4.60: Switching circuit with IRF520N ($R_G = 110\Omega$, $R_{load} = 33\Omega$, $V_{in} = 60V$, $V_G = 12V$). Measurements: solid line. Proposed model: dashed line.
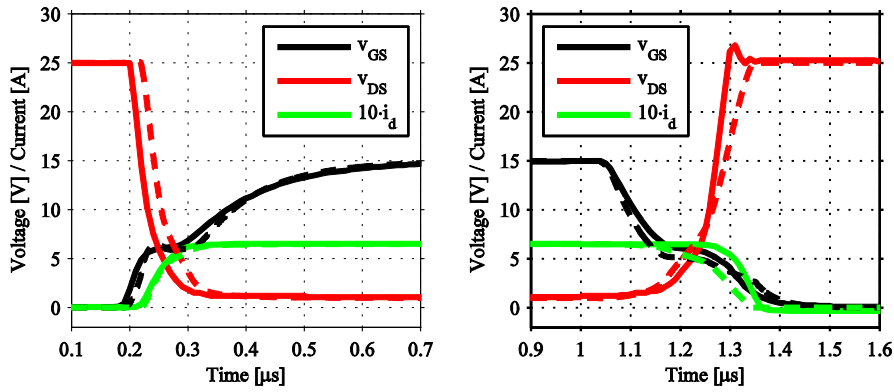
Fig. 4.61: Switching circuit with IRF520N ($R_G = 110\Omega$, $R_{load} = 3.7\Omega$, $V_{in} = 25V$, $V_G = 15V$). Measurements: solid line. Proposed model: dashed line.

The conclusion drawn from the measurements is that the internal capacitances, mostly C_{GD}, is of great importance when it comes to characterizing a MOSFET model adapted for a switching event. The proposed model is valid for the entire operating range of the component, even though the value of C_{GD} to some extent is based on extrapolations of measurement data. This in combination with the fact that the model is going to be used for deriving a suitable controller makes is sufficiently good for this application.

4.3.7   Validity for Different Components

To verify the previously determined statements regarding the validity of the models and the capacitance behavior, different components were analyzed. Regarding the static behavior, it is concluded that the SPICE model provided by the manufacturers is well matched to the datasheet values but due to component

and temperature variations, the model shows slight differences compared to the measurements, see Figure 4.62.
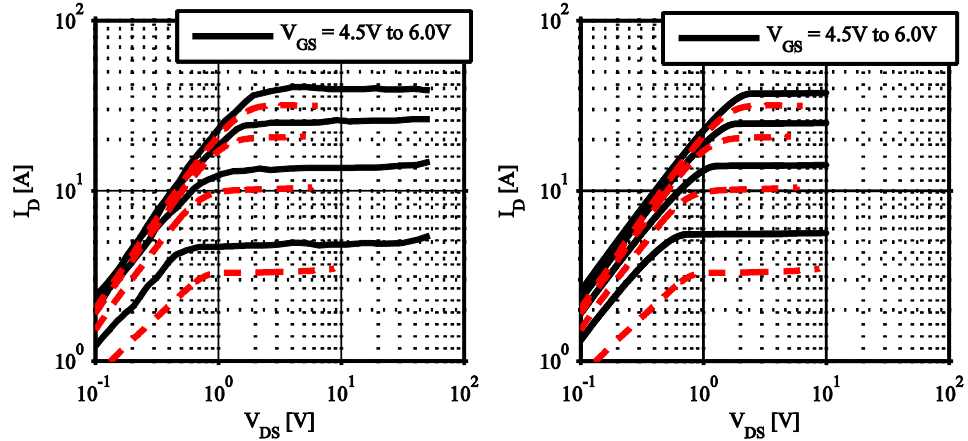
Fig. 4.62: Output characteristics for IRFP150N at 25°C. Left: Comparison of datasheet (solid line) and measured (dashed line) values. Right: Comparison of simulated (solid line) and measured (dashed line) values.

The capacitances show a similar behavior for all measured components, see Figure 4.63 that shows measurement of the reverse transfer capacitance (C_{RSS}) for the MOSFET IRF7403. The general conclusion is that the MOSFET model in SPICE gives satisfactory results for all analyzed components which make it suitable for switching applications.
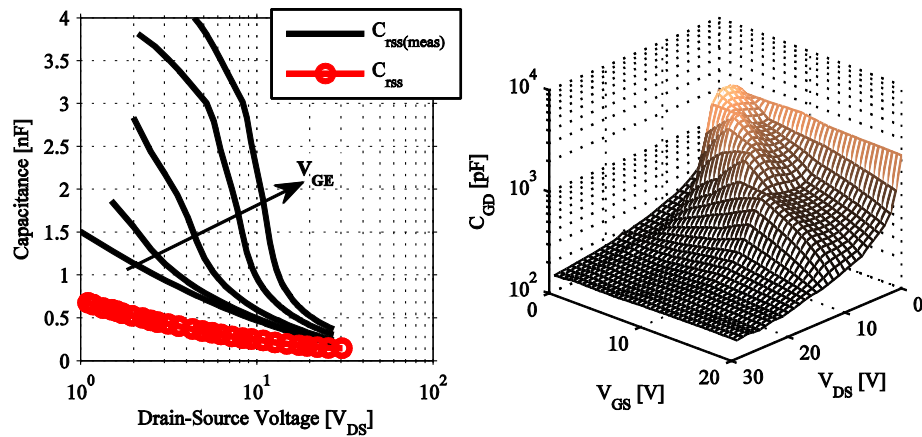
Fig. 4.63: Simulated IGBT output characteristics. Comparison between Simplorer model (solid line) and datasheet (dashed line).

4.4 IGBT

No simulation model of the IGBT provided by manufacturers with sufficient

usability was found as this thesis was written. Many models have been proposed as described in Section 2.5.4, but none of the investigated models have been simple enough to perform a parameter extraction procedure on and implement in an electric circuit simulator. All focus in this section is aimed on the IGBT model in Ansoft Simplorer.

4.4.1 The IGBT Model under Static Conditions

The manufacturer specifies a certain output characteristics in the datasheet which in contrast to the earlier analyzed MOSFETs correspond very well to measurements, see Figure 4.64. The gate threshold voltage is specified in a relatively large span according to the datasheet ($3.5V \leq V_{GE(th)} \leq 5.5V$) and the analyzed component has a threshold voltage according to the typical value ($V_{GE(th)} \approx 3.5V$). The parameter extractor in Simplorer uses the output characteristics to fit the parameters that determine the static behavior of the IGBT model which make the datasheet curves suitable to use as input data.
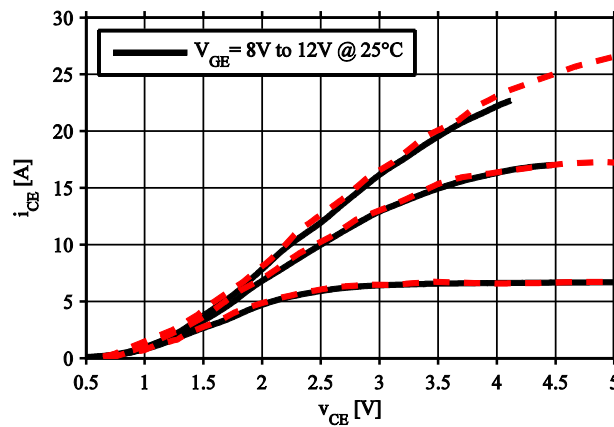
Fig. 4.64: IGBT output characteristics at 25ºC. Comparison between measurements (solid line) and datasheet (dashed line).

If the static behavior of the fitted IGBT model is simulated, the output characteristic is very well fitted to the datasheet values after some fine tuning of the automatically derived values. Figure 4.65 shows a comparison between Simplorer simulations and datasheet values. Since the analyzed component is rated for $10A$, the obtained static characteristics from the fitted model is considered to be sufficiently good.

4.4.2 Dynamic Properties of the IGBT Model

As for the MOSFET, the switching characteristics are strongly determined by the internal capacitances of the IGBT. Their origin is, as explained in Section 2.5.1, to a large extent similar to the one found in the MOSFET, e.g. the MOS-interface

and the inversion layer beneath it. The measurement procedure is the same as for the MOSFET, see Section 4.3.5, and the results correspond well to the datasheet values, see Figure 4.66.
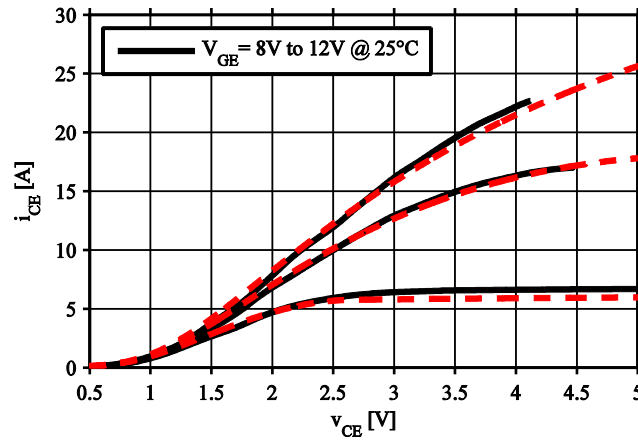
Fig. 4.65:   IGBT output characteristics at 25ºC. Comparison between measurements (solid line) and Simplorer model (dashed line).
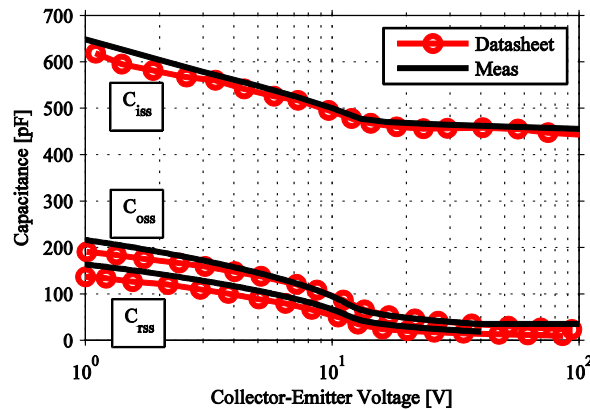
Fig. 4.66:   Internal capacitances of the IGBT IRGB8B60K as a function of V_{CE}. Comparison between measurements (solid line) and datasheet (circled line).

As for the MOSFET, the gate-emitter capacitance origins from the parallel plates formed by the gate oxide on the gate of the IGBT which makes it almost constant independent of the applied voltage. The gate-collector capacitance (also known as C_{RSS}) is strongly dependent on the applied voltages and shows the same behavior as the MOSFET, see Figure 4.67, left picture. The collector-emitter capacitance is much more complex in the IGBT compared with the MOSFET and does not show a simple exponential behavior, see Figure 4.67, left picture for C_{CE} plotted as a function of v_{CE}. The complexity origins from the fact that it is made up of charge accumulations in both the bipolar region and in MOS-region; their location is not obvious as in the reverse biased *pn*-junction within the power MOSFET.
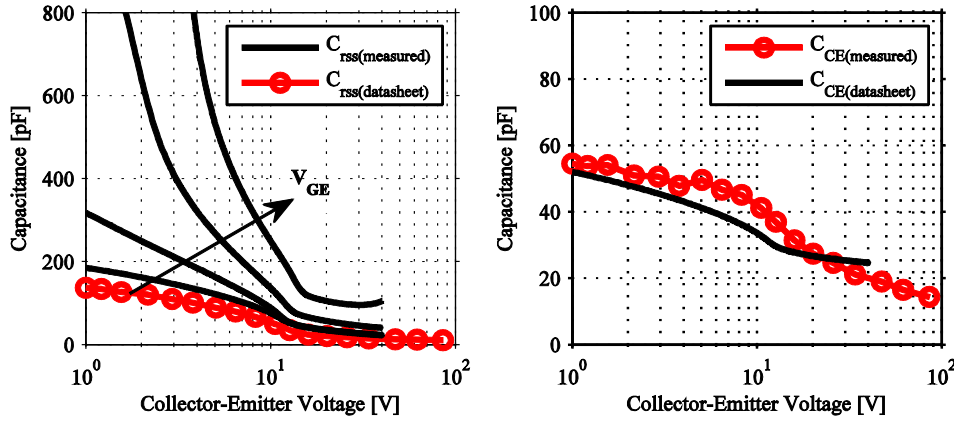
Fig. 4.67: Measured gate-emitter capacitance as a function of V_{CE} for different V_{GE}. Comparison between measurements (solid line) and datasheet (circled line).

The model in Simplorer accounts for the internal capacitances by several internal parameters which do not have any physical representation but can fitted against a switching event. The input capacitances are indirectly controlled by the switching times that are specified in the datasheet and not vice versa as for the proposed MOSFET model in Section 4.3.5. Once the model is fully fitted to the switching events, a frequency sweep can be performed in Simplorer to obtain the actual capacitance values, see Figure 4.68. The difference in simulated capacitance compared with datasheet values is noticeable which can be explained with the causality of the capacitances and switching behavior.
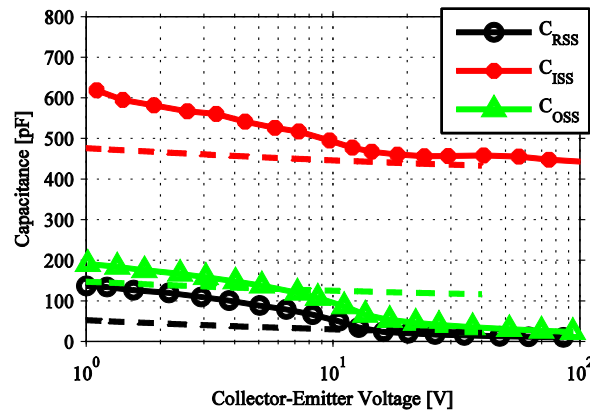
Fig. 4.68: Internal capacitances of the IGBT IRGB8B60K as a function of V_{CE}. Comparison between Simplorer simulations (dashed line) and datasheet values (solid line with marker).

4.4.3   Switching with Purely Resistive Load

To verify the model against real behavior, the switching circuit in section 3.4 was implemented in Simplorer together with the IGBT model obtained by the

parameter extraction tool. It was quickly found that the automatically generated model does not represent the switching behavior in a satisfactory way. However, the switching losses are well matched which makes it more suitable for efficiency calculations. If the complexity of the model is increased and extensive manual fitting of the more than 100 ingoing parameters that determine the switching behavior in the Simplorer Advanced Dynamic IGBT model, significantly better results are obtained. The results are seen in Figure 4.69 that compares simulations and measurements. The advanced dynamic IGBT model with manually fitted dynamic parameters show satisfactory switching behavior and adapts itself well to different operating conditions, see Figure 4.70. It can be noted that the simulated tail current has an appearance that corresponds well to the measurements due to the carrier lifetime modeling within the IGBT model.
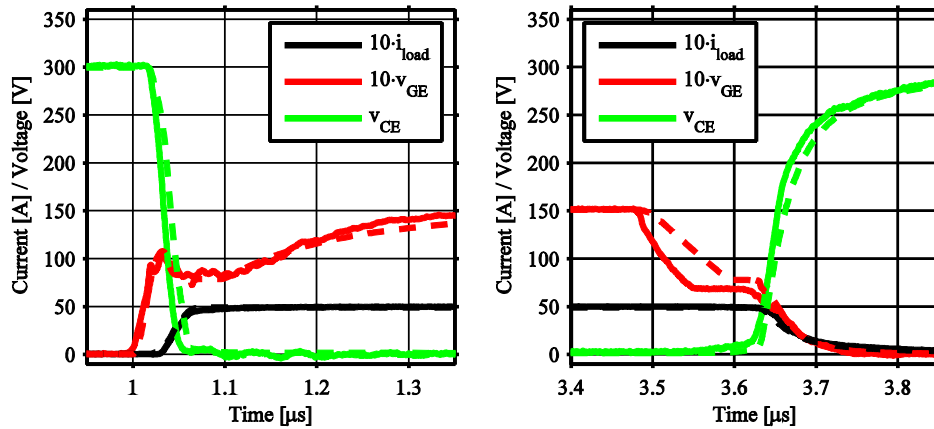
Fig. 4.69: Switching circuit with resistive load. ($V_{DC} = 300V$, $R_G = 50\Omega$, $R_{load} = 61\Omega$, $V_G = 15V$). Solid line: measurements. Dashed: Simplorer model.
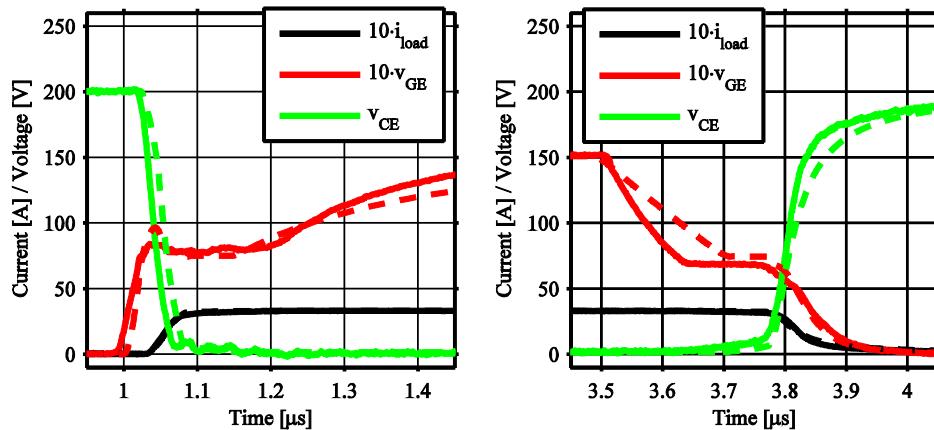
Fig. 4.70: Switching circuit with resistive load. ($V_{DC} = 200V$, $R_G = 100\Omega$, $R_{load} = 61\Omega$, $V_G = 15V$). Solid line: measurements. Dashed: Simplorer model.

4.4.4   Temperature Effects in the IGBT

As for the diode and the MOSFET, the temperature has strong influence on the static performance of an IGBT. Since both electron and hole mobility will decrease with temperature (see Table 4.1) the forward voltage drop will increase as the temperature increases for a given forward current. This is reflected in the output characteristics as a flattening out of the curves; see Figure 4.71 that shows a comparison of the measured output characteristics with datasheet values. This is also accounted for in the Simplorer model by several parameters, e.g. *ALPHA_M_BJT* which compensate for the temperature changes in the BJT ideality coefficient within the IGBT model. The result is an IGBT model that adapts itself to the temperature in a satisfactory way, see Figure 4.72 that show a comparison of the output characteristics for the fitted Simplorer model and datasheet values. The temperature effects are taken into account by the parameter extraction tool, but to get the best result extensive manual curve fitting is needed.
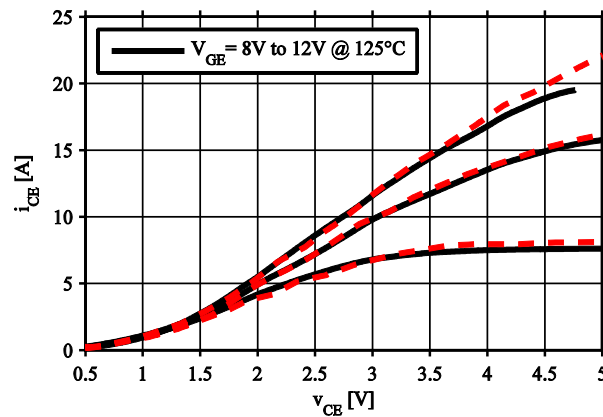
Fig. 4.71:   Measured (solid) and datasheet (dashed) IGBT output characteristics.
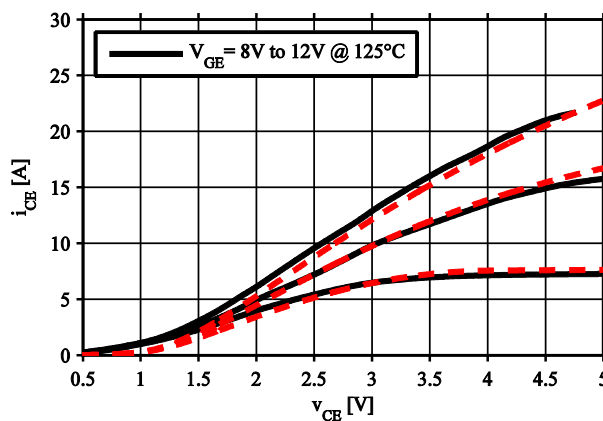
Fig. 4.72:   Measured (solid) and Simplorer (dashed) IGBT output characteristics..

The most obvious temperature effect in an IGBT is the increase in tail current due to longer carrier lifetime. The carriers in the BJT region of the IGBT needs to be swept out or recombine, and since the carrier lifetime increase with approximately the temperature to the power of 1.5, see Table 4.1, the tail current that consist of carriers that are swept out becomes extended, see Figure 4.73, left picture that depicts measurements of IGBT tail currents at two temperatures. Once again, this is taken into account by the IGBT model in Simplorer where the durations of the tail current becomes prolonged as the temperature increase, see Figure 4.73, right picture. However, the effect is not as distinguished as for the measurements and the model might need further fitting of the temperature parameters to obtain even better results.
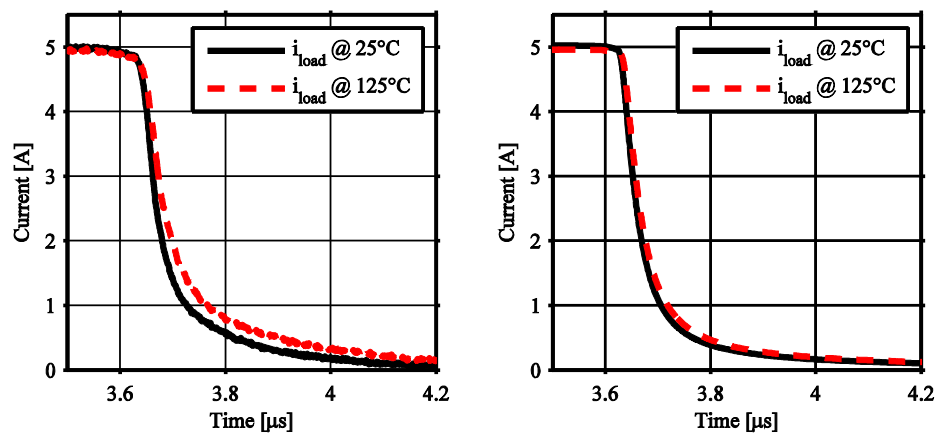
Fig. 4.73: IGBT output characteristics at 125ºC. Comparison between measurements (solid line) and datasheet (dashed line).

Chapter 5

Active Gate Control

5.1 Active Gate Control - Theoretical Derivation

In this section, a new way of controlling the EMI from a switched DC/DC converter by active gate control is proposed. The operation principle is that the gate voltage is controlled in such a way that the harmonic content in the desired output, either v_{DS} or i_D, is reduced. This is achieved by reducing the sharp transitions in the output and shall not be mixed up with the traditional method of increasing the gate resistance. Figure 5.1 presents a schematic time function, $f(t)$, of the desired voltage waveforms with linear and sinusoidal transitions.
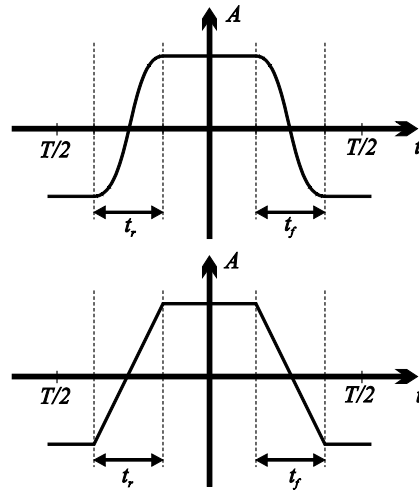
Fig. 5.1:   PWM pulse with sinusoidal and trapezoidal transitions.

Instead of using a trapezoidal shaped (can be seen as a square wave voltage with a finite rise time) gate voltage to switch the semiconductor, it is possible to control the desired output in a more curved way by applying a corresponding gate voltage. The desired output can take several shapes, e.g. a sinusoidal transition or a third degree approximation. The main purpose of this transition and what all

applied waveforms should have in common is the low harmonic content mainly due to rounding off sharp edges. In this thesis, only the sinusoidal transition is considered. Figure 5.2 shows a comparison between a sinusoidal and a trapezoidal transition in both time and frequency domain.
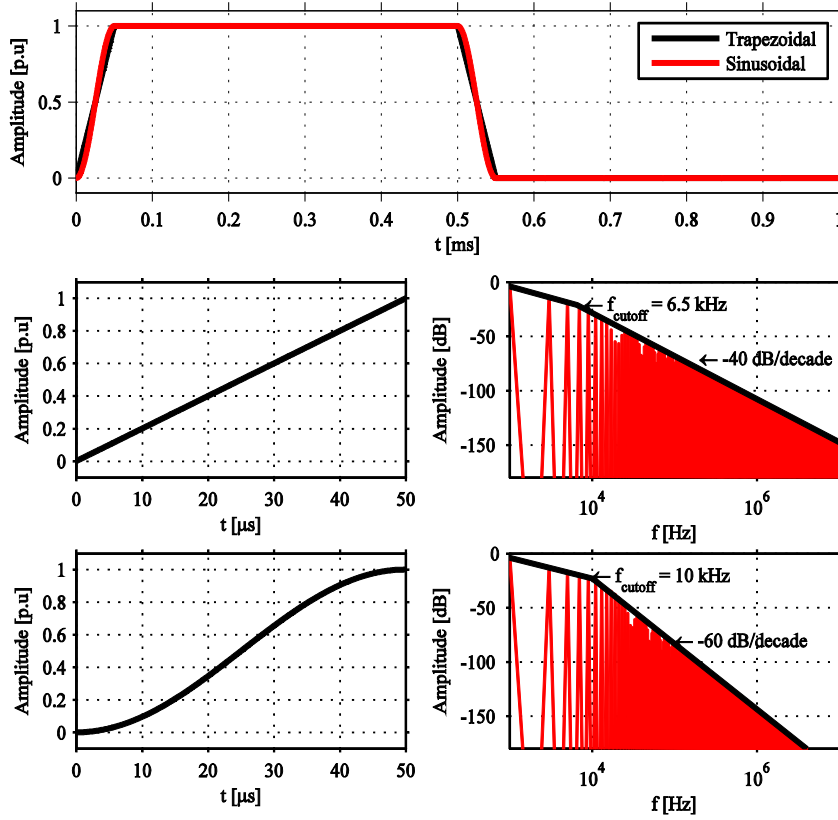
Fig. 5.2: FFT comparison of pulses with sinusoidal and trapezoidal transitions.

Assume the rise time to be t_r the duty cycle to be D, and the total period time T. One period of the function with sinusoidal transition can be written as

$$f_{\text{sine}}(t) = \begin{cases} -1 & -\dfrac{T}{2} \leq t \leq t_1 \\[2mm] f_1 = \cos\left[\dfrac{\pi t}{t_r T} + \dfrac{\pi}{2}\left(\dfrac{D}{t_r} - 1\right)\right] & t_1 \leq t \leq t_2 \\[2mm] 1 & t_2 \leq t \leq t_3 \\[2mm] f_2 = \cos\left[\dfrac{\pi t}{t_r T} - \dfrac{\pi}{2}\left(\dfrac{D}{t_r} - 1\right)\right] & t_3 \leq t \leq t_4 \\[2mm] -1 & t_4 \leq t \leq \dfrac{T}{2} \end{cases} \qquad (5.1)$$

and for the trapezoidal pulse as

$$f_{\text{trap}}(t) = \begin{cases} -1 & -\dfrac{T}{2} \le t \le t_1 \\[2mm] f_1 = \dfrac{2t}{t_r T} + \dfrac{D}{t_r} & t_1 \le t \le t_2 \\[2mm] 1 & t_2 \le t \le t_3 \\[2mm] f_2 = -\dfrac{2t}{t_r T} + \dfrac{D}{t_r} & t_3 \le t \le t_4 \\[2mm] -1 & t_4 \le t \le \dfrac{T}{2} \end{cases} \tag{5.2}$$

where

$$t_1 = (-D - t_r)\frac{T}{2}, \quad t_2 = (-D + t_r)\frac{T}{2}$$
$$t_3 = (D - t_r)\frac{T}{2}, \quad t_4 = (D + t_r)\frac{T}{2} \tag{5.3}$$

The Fourier series expansion for an even function is

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\Omega t) \tag{5.4}$$

where a_n is determined by

$$a_n = \frac{4}{T}\int_0^{t_3} \cos(n\Omega t)\, dt + \frac{4}{T}\int_{t_3}^{t_4} f_2 \cdot \cos(n\Omega t)\, dt + \frac{4}{T}\int_{t_4}^{T/2} -\cos(n\Omega t)\, dt \tag{5.5}$$

After solving and simplifying the expression a_n can be written as, for the trapezoidal case

$$a_n = \frac{4}{\pi} \cdot \frac{1}{n^2 \pi t_r} \cdot \sin(n\pi t_r) \cdot \sin(n\pi D). \tag{5.6}$$

a_n will decrease as n^{-2} which equals to $-40 dB/decade$. For the sinusoidal transition function the Fourier component will be given as

$$a_n = \frac{-4}{\pi} \cdot \frac{1}{n((2t_r n)^2 - 1)} \cdot \cos(n\pi t_r) \cdot \sin(n\pi D). \tag{5.7}$$

Obviously, a_n will decrease as n^{-3} for large n. The suspected singularity at

$(2t_r n)^2 = 1$ can be investigated as follows. Consider that

$$\cos(n\pi t_r) = -\sin\left(n\pi t_r - \frac{\pi}{2}\right) = -\sin\left(\frac{\pi}{2}(2nt_r - 1)\right) \qquad (5.8)$$

and that

$$[(2nt_r)^2 - 1] = (2nt_r + 1)(2nt_r - 1). \qquad (5.9)$$

Insertion (5.8) and (5.9) in (5.7) gives

$$a_n = \frac{4}{\pi} \cdot \frac{1}{n} \frac{1}{(2t_r n + 1)} \cdot \frac{\pi}{2} \cdot \frac{\sin\left(\pi/2\right) \cdot (2t_r n - 1)}{\pi/2 \,(2t_r n - 1)} \cdot \sin(n\pi D). \qquad (5.10)$$

Since

$$\lim_{2t_r n - 1 \to 0} \frac{\sin\left(\pi/2\right) \cdot (2t_r n - 1)}{\pi/2 \,(2t_r n - 1)} = 1 \qquad (5.11)$$

a_n is defined for every value of n. This results in a theoretical proof of the statement that a sinusoidal transition reduces the harmonic content with -60dB/decade.

5.2   Controller Design

In order to develop a controller that satisfies the demands set by the principle of active gate control, the proposed MOSFET model can be used to derive appropriate parameters. However, the system is strongly nonlinear and one way to deal with such a system is to linearize it about an operating point. This approach gives a reasonably accurate solution for the specified output around the analyzed operating point. Consider the general nonlinear system

$$\dot{x}(t) = f\big(x(t), u(t)\big)$$
$$y(t) = g\big(x(t), u(t)\big) \qquad (5.12)$$

where $x(t)$, $u(t)$ and f are, respectively, the n-dimensional system state space vector, the r-dimensional input vector, and the n-dimensional vector function. Assume that the nominal (operating) system trajectory $x_n(t)$ is known and that the nominal system input that keeps the system on the nominal trajectory is given by $f_n(t)$. It can be assumed that the actual system dynamics in the immediate proximity of the system nominal trajectories can be approximated by the first terms of the Taylor series. That is, starting with

$$x(t) = x_n(t) + \Delta x(t)$$
$$u(t) = u_n(t) + \Delta u(t) \tag{5.13}$$

and

$$\frac{d}{dt} x_n(t) = f\big(x_n(t), u_n(t)\big) \tag{5.14}$$

we expand the right-hand side into the Taylor series as follows

$$\frac{d}{dt} x_n(t) + \frac{d}{dt} \Delta x(t) = f\big(x_n(t) + \Delta x(t), u_n(t) + \Delta u(t)\big) =$$
$$= f(x_n + u_n) + \left(\frac{\partial f}{\partial x}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta x + \left(\frac{\partial f}{\partial u}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta u + \text{higher order terms} \tag{5.15}$$

Higher-order terms contain at least quadratic quantities of Δx and Δu. Since they already are small and their squares are even smaller, the high-order terms can be neglected. Neglecting higher-order terms, an approximation is obtained

$$\frac{d}{dt} \Delta x(t) = \left(\frac{\partial f}{\partial x}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta x(t) + \left(\frac{\partial f}{\partial u}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta u(t) \tag{5.16}$$

The partial derivatives represent the Jacobian matrices given by

$$\left(\frac{\partial f}{\partial x}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} = \mathbb{A}^{n \times n} = \begin{bmatrix} \dfrac{\partial f_1}{\partial x_1} & \cdots & \dfrac{\partial f_1}{\partial x_n} \\ \vdots & & \vdots \\ \dfrac{\partial f_n}{\partial x_1} & \cdots & \dfrac{\partial f_n}{\partial x_n} \end{bmatrix}_{\substack{x_n(t) \\ u_n(t)}} \tag{5.17}$$

$$\left(\frac{\partial f}{\partial u}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} = \mathbb{B}^{n \times n} = \begin{bmatrix} \dfrac{\partial f_1}{\partial u_1} & \cdots & \dfrac{\partial f_1}{\partial u_n} \\ \vdots & & \vdots \\ \dfrac{\partial f_n}{\partial u_1} & \cdots & \dfrac{\partial f_n}{\partial u_n} \end{bmatrix}_{\substack{x_n(t) \\ u_n(t)}} \tag{5.18}$$

If the same methodology is applied to the n-dimensional vector function g that governs the outputs of the system, the expression for the how the outputs behave around an operating point can be expressed in an analogous way. If the Jacobian matrices are evaluated at the nominal points, that is, at $x_n(t)$ and $f_n(t)$, the linearized system can be expressed on the form

$$\Delta \dot{x}(t) = \mathbb{A}\Delta x(t) + \mathbb{B}\Delta u(t)$$
$$\Delta y(t) = \mathbb{C}\Delta x(t) + \mathbb{D}\Delta u(t)$$

(5.19)

If a switching event of the proposed MOSFET model is to be simulated, the model needs to be divided into three parts; turned-off region, linear region and the saturated region. Depending on which region the MOSFET operates in, the state matrix $\mathbb{A}$ will change, but the state matrix $\mathbb{B}$ will remain the same. When the MOSFET is turned off ($i_{\mathrm{DS}} = 0$), the state-matrix $\mathbb{A}$ becomes

$$\mathbb{A} = \begin{bmatrix} \dfrac{-1}{C_{\mathrm{GS}}RS} & \dfrac{1}{C_{\mathrm{GS}}RS} & \dfrac{1}{C_{\mathrm{GS}}RS} & \dfrac{1}{C_{\mathrm{GS}}} & \dfrac{1}{C_{\mathrm{GS}}} & 0 \\[2mm] \dfrac{1}{C_{\mathrm{GD}}RS} & \dfrac{-1}{C_{\mathrm{GD}}RS} & \dfrac{-1}{C_{\mathrm{GD}}RS} & 0 & \dfrac{1}{C_{\mathrm{GD}}} & 0 \\[2mm] \dfrac{-1}{C_{\mathrm{d}}RS} & \dfrac{1}{C_{\mathrm{d}}RS} & \dfrac{1}{C_{\mathrm{d}}RS} & 0 & 0 & 0 \\[2mm] \dfrac{-L_{\mathrm{D}}}{L_{\mathrm{sum}}} & \dfrac{-L_{\mathrm{S}}}{L_{\mathrm{sum}}} & 0 & \dfrac{-L_{\mathrm{S}}R_{\mathrm{D}} - L_{\mathrm{D}}R_{\mathrm{G}} - L_{\mathrm{S}}R_{\mathrm{G}}}{L_{\mathrm{sum}}} & 0 & \dfrac{L_{\mathrm{S}}R_{\mathrm{D}} - L_{\mathrm{D}}R_{\mathrm{S}}}{L_{\mathrm{sum}}} \\[2mm] \dfrac{-L_{\mathrm{G}}}{L_{\mathrm{sum}}} & \dfrac{L_{\mathrm{G}} + L_{\mathrm{S}}}{L_{\mathrm{sum}}} & 0 & \dfrac{L_{\mathrm{S}}R_{\mathrm{G}} - L_{\mathrm{G}}R_{\mathrm{S}}}{L_{\mathrm{sum}}} & \dfrac{-L_{\mathrm{G}}R_{\mathrm{D}} - L_{\mathrm{S}}R_{\mathrm{D}} - L_{\mathrm{G}}R_{\mathrm{S}}}{L_{\mathrm{sum}}} & 0 \\[2mm] \dfrac{-L_{\mathrm{D}} - L_{\mathrm{G}}}{L_{\mathrm{sum}}} & \dfrac{L_{\mathrm{G}}}{L_{\mathrm{sum}}} & 0 & \dfrac{L_{\mathrm{G}}R_{\mathrm{D}} - L_{\mathrm{D}}R_{\mathrm{G}}}{L_{\mathrm{sum}}} & 0 & \dfrac{-L_{\mathrm{G}}R_{\mathrm{D}} - L_{\mathrm{D}}R_{\mathrm{S}} - L_{\mathrm{G}}R_{\mathrm{S}}}{L_{\mathrm{sum}}} \end{bmatrix}$$

(5.20)

$$\mathbb{B} = \begin{bmatrix} 0 & 0 \\[2mm] 0 & 0 \\[2mm] 0 & 0 \\[2mm] \dfrac{L_D + L_S}{L_{sum}} & \dfrac{-L_S}{L_{sum}} \\[2mm] \dfrac{-L_S}{L_{sum}} & \dfrac{L_G + L_S}{L_{sum}} \\[2mm] \dfrac{L_D}{L_{sum}} & \dfrac{L_G}{L_{sum}} \end{bmatrix}$$

(5.21)

where

$$L_{\mathrm{sum}} = L_{\mathrm{D}}L_{\mathrm{G}} + L_{\mathrm{D}}L_{\mathrm{S}} + L_{\mathrm{G}}L_{\mathrm{S}}.$$

(5.22)

For the active and linear region respectively, the state matrix A becomes

$$\mathbb{A}_{\text{active}} = \begin{bmatrix} \dfrac{-1 - 2KP \cdot RS \cdot V_{CGS(0)} - 2KP \cdot \lambda \cdot RS \cdot V_{Cd(0)} \cdot V_{CGS(0)} + 2KP \cdot RS \cdot V_{th(0)} + 2KP \cdot \lambda \cdot RS \cdot V_{Cd(0)} \cdot V_{th(0)}}{C_{GS}RS} & \dfrac{1}{C_{GS}RS} \cdots \\[2mm] \dfrac{1 + 2KP \cdot RS \cdot V_{CGS(0)} + 2KP \cdot \lambda \cdot RS \cdot V_{Cd(0)} \cdot V_{CGS(0)} - 2KP \cdot RS \cdot V_{th(0)} - 2KP \cdot \lambda \cdot RS \cdot V_{Cd(0)} \cdot V_{th(0)}}{C_{GD}RS} & \dfrac{-1}{C_{GD}RS} \cdots \\[2mm] \dfrac{-1}{C_d RS} & \dfrac{1}{C_d RS} \cdots \\[2mm] \dfrac{-L_D}{L_{sum}} & \dfrac{-L_S}{L_{sum}} \cdots \\[2mm] \dfrac{-L_G}{L_{sum}} & \dfrac{L_G + L_S}{L_{sum}} \cdots \\[2mm] \dfrac{-L_D - L_G}{L_{sum}} & \dfrac{L_G}{L_{sum}} \cdots \end{bmatrix}$$

$$\begin{matrix} \cdots & \dfrac{-1 - KP \cdot \lambda \cdot RS(V_{CGS(0)} - V_{th(0)})^2}{C_{GS}RS} & \dfrac{1}{C_{GS}} & \dfrac{1}{C_{GS}} & 0 \\[2mm] \cdots & \dfrac{1 + KP \cdot \lambda \cdot RS(V_{CGS(0)} - V_{th(0)})^2}{C_{GD}RS} & 0 & \dfrac{-1}{C_{GD}} & 0 \\[2mm] \cdots & \dfrac{-R_{rev} - RS}{C_d R_{rev} RS} & 0 & 0 & 0 \\[2mm] \cdots & 0 & \dfrac{-L_S R_D - L_D R_G - L_S R_G}{L_{sum}} & 0 & \dfrac{L_S R_D - L_D R_S}{L_{sum}} \\[2mm] \cdots & 0 & \dfrac{L_S R_G - L_G R_S}{L_{sum}} & \dfrac{-L_G R_D - L_S R_D - L_G R_S}{L_{sum}} & 0 \\[2mm] \cdots & 0 & \dfrac{L_G R_D - L_D R_G}{L_{sum}} & 0 & \dfrac{-L_G R_D - L_D R_S - L_G R_S}{L_{sum}} \end{matrix} \quad (5.23)$$

$$\mathbb{A}_{\text{lin}} = \begin{bmatrix} \dfrac{-1 + KP \cdot RS \cdot V_{Cd(0)} + KP \cdot \lambda \cdot RS \cdot V_{Cd(0)}^2}{C_{GS}RS} & \dfrac{1}{C_{GS}RS} & \dfrac{-2 + KP \cdot RS\left(3\lambda V_{Cd(0)}^2 + 2(V_{CGS(0)} - V_{th(0)}) - V_{Cd(0)}(2 + 4\lambda V_{CGS(0)} - 4\lambda V_{th(0)})\right)}{C_{GS}RS} \cdots \\[2mm] \dfrac{1 - KP \cdot RS \cdot V_{Cd(0)} - KP \cdot \lambda \cdot RS \cdot V_{Cd(0)}^2}{C_{GD}RS} & \dfrac{-1}{C_{GD}RS} & \dfrac{2 - KP \cdot RS\left(3\lambda V_{Cd(0)}^2 + 2(V_{CGS(0)} - V_{th(0)}) - V_{Cd(0)}(2 + 4\lambda V_{CGS(0)} - 4\lambda V_{th(0)})\right)}{C_{GS}RS} \cdots \\[2mm] \dfrac{-1}{C_d RS} & \dfrac{1}{C_d RS} & \dfrac{-R_{rev} - RS}{C_d R_{rev} RS} \cdots \\[2mm] \dfrac{-L_D}{L_{sum}} & \dfrac{-L_S}{L_{sum}} & 0 \cdots \\[2mm] \dfrac{-L_G}{L_{sum}} & \dfrac{L_G + L_S}{L_{sum}} & 0 \cdots \\[2mm] \dfrac{-L_D - L_G}{L_{sum}} & \dfrac{L_G}{L_{sum}} & 0 \cdots \end{bmatrix}$$

$$\begin{matrix} \cdots & \dfrac{1}{C_{GS}} & \dfrac{1}{C_{GS}} & 0 \\[2mm] \cdots & 0 & \dfrac{-1}{C_{GD}} & 0 \\[2mm] \cdots & 0 & 0 & 0 \\[2mm] \cdots & \dfrac{-L_S R_D - L_D R_G - L_S R_G}{L_{sum}} & 0 & \dfrac{L_S R_D - L_D R_S}{L_{sum}} \\[2mm] \cdots & \dfrac{L_S R_G - L_G R_S}{L_{sum}} & \dfrac{-L_G R_D - L_S R_D - L_G R_S}{L_{sum}} & 0 \\[2mm] \cdots & \dfrac{L_G R_D - L_D R_G}{L_{sum}} & 0 & \dfrac{-L_G R_D - L_D R_S - L_G R_S}{L_{sum}} \end{matrix} \quad (5.24)$$

The step response of the proposed linearized model can be seen in Figure 5.3. The results from SPICE simulations and the proposed MOSFET model show good agreement both for v_{GS} and i_D. Several different operating points were analyzed and the conclusion is that the linearized model shows good agreement with the SPICE model when it comes to small signal analysis. If the linearized model and the SPICE model are verified against real measurements, significantly larger discrepancies can be noticed. Figure 5.3 shows a comparison of measurements and SPICE simulations of the small signal response in the active region. The difference can mainly be explained due to deviations in static behavior between simulation models and real components. Due to practical reasons such as internal heating of the component, simulation results are hard to verify with a practical measurement for higher currents.
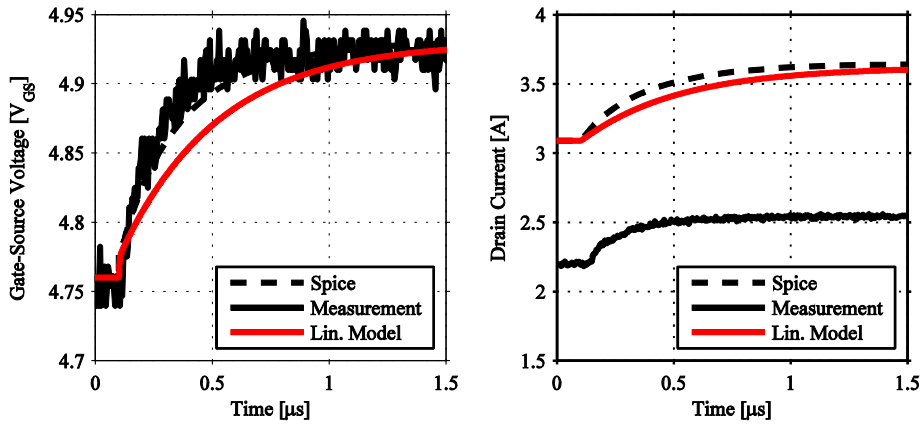
Fig. 5.3:   Measured and simulated step response. Left: v_{GS} Right: i_D.

Since this thesis deals with switching procedures, the system will operate in all of the preceding states. The selected switching needs to be analyzed and broken down into discrete operating points where the first task is to identify which area the model is operating in. Note that the proposed methodology only gives a rule of thumb when designing the controller, when designing a controller that is fully valid over the entire operating range, other methods such as exact linearization should be used instead [116, 117].

5.3   Selecting the Output of the System

Once the state matrixes $\mathbb{A}$ and $\mathbb{B}$ are known for all operating points of the system, the matrixes that determine the outputs of the system, matrixes $\mathbb{C}$ and $\mathbb{D}$, must be defined. These matrixes do not vary depending on the operating point but will differ depending on the desired output. Basically there are two different signals that can be of interest; the component drain-source voltage and the drain-current. Depending on the output, the state-matrixes $\mathbb{C}$ and $\mathbb{D}$ can be defined as

$$\mathbb{C}_{\text{Vds}} = \begin{bmatrix} 0 & 0 & 0 & 0 & -1 & R_{D(ext)} \end{bmatrix} \qquad (5.25)$$

$$\mathbb{D}_{\text{Vds}} = \begin{bmatrix} 0 & 0 \end{bmatrix} \qquad (5.26)$$

$$\mathbb{C}_{\text{Vds}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \qquad (5.27)$$

$$\mathbb{D}_{\text{Id}} = \begin{bmatrix} 0 & 0 \end{bmatrix} \qquad (5.28)$$

When the MOSFET is turned off ($i_{DS} = 0$), a small change in the gate-source voltage will not affect the desired output in a significant way. Since it is desired to boost v_{GS} to a level just beneath the threshold voltage before the switching event, the subthreshold region is of lower importance when the controller is designed.

Since the MOSFET are operating under a dynamic procedure, the operating points that the system experiences during the switching transient cannot be considered as steady state solutions. Several operating points in the vicinity of the switching event depicted in Figure 4.61 were selected and analyzed. It is clear that the gain of the system depends on the output (v_{DS} or i_D) which needs to be taken into consideration when designing a suitable controller. In order to implement a suitable controller, the system needs to be evaluated in both the ohmic and the active region. The problem that inevitably occurs by this transition via the previously defined stationary points is that the system will enter undefined operating points; the previously analyzed switching event is broken down into some discrete operating points for which the system is defined, but for the area between these points the system will still be undefined. Another property of the system is that the ingoing constants in the state matrixes $\mathbb{A}$, $\mathbb{B}$, $\mathbb{C}$ and $\mathbb{D}$ changes as the switching event progresses which results in a system with varying properties. In order to get a controller that is suitable for the entire operating range, other methods such as exact linearization should be used. However, the purpose of this approach is solely to investigate if there is a potential to design a controller on a basis of the obtained parameters and if an adaptive controller gives better performance.

The bode plot of the system resembles the bode plot of a first order system; hence can a reasonable approximation be made by translating the low frequency properties of the system into a first order system. The transfer function of the total system, G_{sys}, can be written as

$$\frac{-4.8e7 \cdot s^5 - 1.4e20 \cdot s^4 - 1.7e30 \cdot s^3 - 7.2e38 \cdot s^2 + 2.9e48 \cdot s + 1.2e57}{s^6 + 2.9e12 \cdot s^5 + 7.9e22 \cdot s^4 + 5.6e32 \cdot s^3 + 4.0e41 \cdot s^2 + 7.7e49 \cdot s + 2.2e56} \qquad (5.29)$$

which equals a sixth order system. However, the dominant poles of this system can be found at a low frequency which gives a system that can be approximated as

$$G_{sys} = \frac{\alpha_e}{s + \alpha_e}. \tag{5.30}$$

The transfer function in (5.29) can now be expressed as

$$G_{sys} = \frac{1.47 \cdot 10^7}{s + 2.88 \cdot 10^6}. \tag{5.31}$$

which is a suitable form for designing a controller. Figure 5.4 shows a bode plot comparison where the difference between the total and the simplified system is shown. By expressing the system as a first order system, the controller design can be made with loop shaping which is a special case of the Internal Model Control (IMC) design procedure [118].
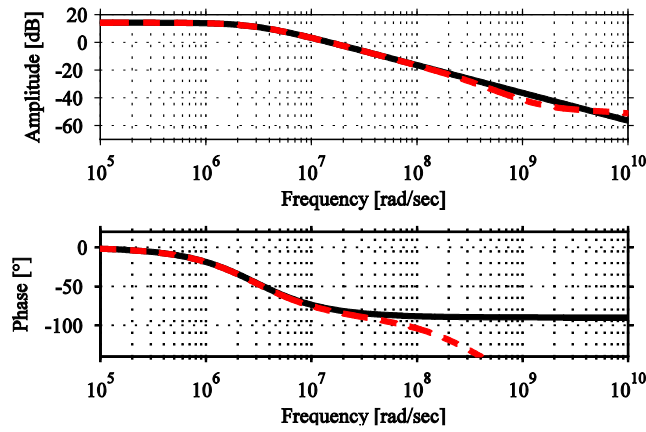
Fig. 5.4: Comparison of total and simplified transfer function from V_{GS} to I_D. $V_{GS} = 4.4V$ and $V_{DS} = 25V$.

The basic operating principle of the complete closed loop system including a controller is depicted in Figure 5.5 where a block diagrams is presented for both the drain current and the drain-source voltage selected as the controlled quantity.
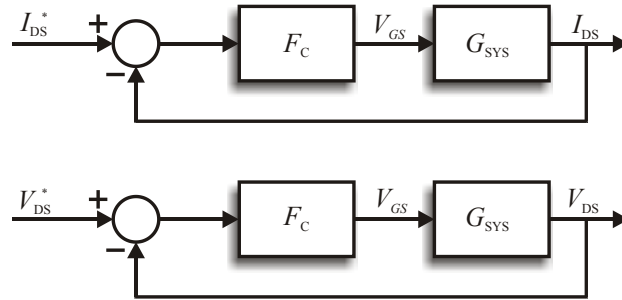
Fig. 5.5: Block diagram of the two different controller schemes.

Since the transfer function G_{sys} can be approximated with a transfer function of order one, the controller, F_c, can be selected as a simple PI-controller; the order of

the controller does not need to be higher than that of the controlled process. The idea is to specify the desired rise time (10% - 90%) of the closed loop system. If G_{sys} is known, it is apparent that the closed loop transfer function of the total closed loop system depicted in Figure 5.5 can be obtained according as

$$G_{cl} = \frac{F_c(s)G_{sys}(s)}{1 + F_c(s)G_{sys}(s)}. \tag{5.32}$$

where $G_{cl}(s)$ is the closed-loop transfer function and $F_c(s)$ is the transfer function of the controller. In Figure 5.6 the step response of the open loop system from a unity step applied to the input (V_{GS}) is seen as a solid line. The step response of the system if a unity step is applied results in a large remaining error; an error that can be eliminated by applying a well designed controller.
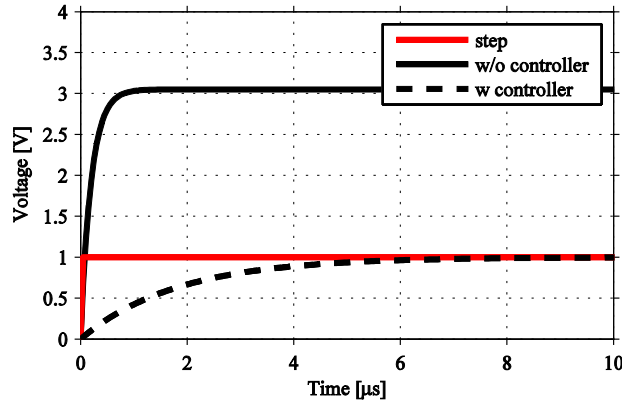

Fig. 5.6:   Step response of the transfer function from v_{GS} to v_{DS}. Solid Line: Without controller. Dashed Line: Closed loop system with controller.

By using the IMC-method, a controller can be designed that is valid around a specified operating point. In order to obtain the closed loop transfer function in (5.32), the controller $F_c(s)$ must be designed according to

$$F_c(s) = \frac{\alpha_e}{s} G_{sys}^{-1}(s). \tag{5.33}$$

where α_e is the desired bandwidth of the total system. A suitable controller for the system in (5.31) can then be expressed as

$$F_c(s) = \frac{\alpha_e}{s}\left(\frac{1.47 \cdot 10^7}{s + 2.88 \cdot 10^6}\right). \tag{5.34}$$

where the bandwidth is determined by α_e. To verify the method, the step response of the system can be studied. The dashed line in Figure 5.6 shows how the system $G_{cl}(s)$ taken from (5.31) behaves when a controller circuit with rise time 10µs is implemented. The method proposed by IMC works and gives the desired results

applied to the system. However, one concern still remains and that is how the changes in system parameters will influence the controller design.

5.4   Implementation of Active Gate Control

In order to realize a control circuit for active gate control, the control strategies derived in the previous section are now implemented. A principal schematic of the realized controller structure is shown in Figure 5.7 where the magnitude of the error depends on which output quantity (V_{DS} or I_D) that is desired to control.
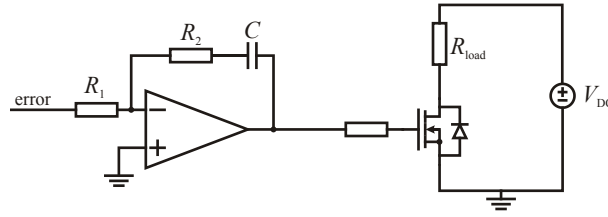
Fig. 5.7:   Principal schematic of the implemented controller circuit.

A suitable controller would consist of a proportional and an integral part with the transfer function

$$F_c(s) = K_p + \frac{K_i}{s}. \qquad (5.35)$$

This controller can be realized with help of operational amplifiers according to the circuit depicted in Figure 5.7. The proportional gain is determined by

$$K_p = \frac{R_2}{R_1} \qquad (5.36)$$

and the integral gain is determined by

$$K_i = \frac{1}{R_1 C}. \qquad (5.37)$$

Note that the circuit in Figure 5.7 produces a negative voltage, hence, an inverting voltage follower or summer must be attached between the controller circuit and the MOSFET in order to obtain a functioning circuit. One other important aspect of the controller design is to guarantee that the output of the operational amplifier can deliver sufficient current.

An FPGA is used to generate the sinusoidal shaped reference waveform [119], but due to limitations in the FPGA-circuit, the investigated rise times and switching frequencies are limited to a certain number of discrete steps in order to avoid jitter, see Table 5.1.

Table 5.1   Switching frequency and rise-times of the reference waveform.

Frequency	Rise Time [%]	Rise Time [μs]
2464Hz	10%	40.6μs
	1%	4.0μs
493Hz	10%	203μs
	1%	20μs

The design of the controller circuit can be made according to IMC which requires a small signal analysis around an operating point. The approach analyzed in this thesis is based on discretization of the switching event where each operating point is analyzed individually to give controller parameters that will vary during the switch event. The analyzed points during the turn-on event are shown as circles in Figure 5.8 where $V_{DC} = 25V$, $V_{gate} = 15V$ and $R_{load} = 3.7\Omega$ which in total gives 16 points excluding the subthreshold region. In all forthcoming reasoning, the discussed operating points refer to this figure.
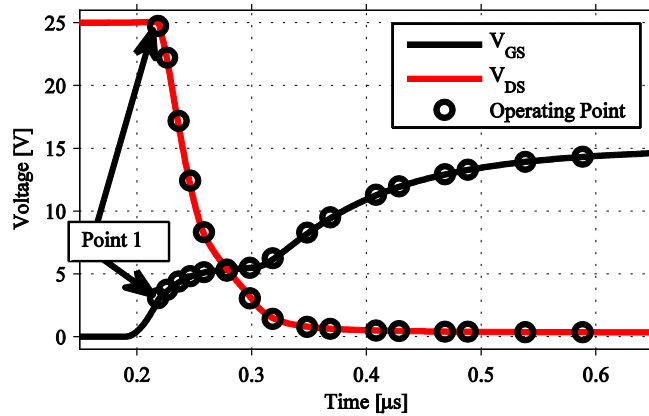
Fig. 5.8:   Selected operating points for analysis during a turn on-event.

5.4.1   Step Response of the System

In order to evaluate the closed loop system, the step response for each operating point of the system is evaluated separately. Figure 5.9 and 5.10 shows all analyzed operating points for the switching system during turn-on. The variations in both the proportional gain (K_p) and integral gain (K_i) for the analyzed switching event with a resulting rise-time of $4\mu s$ are shown on the right axis. A similar analysis was also performed to the turn-off event.

Based on measurements and simulations for the current operating case and for all rise times specified in Table 5.1, it can be concluded that the most suitable controller with fixed parameters is always the one derived from the beginning of the turn-on event (point 1 in Figure 5.9). If controllers from the following

Fig. 5.9: Proportional and integral gain variations for a controller with $t_{rise} = 4\mu s$ during a switching event, i_{DS} selected as output.

Fig. 5.10: Proportional and integral gain variations for a controller with $t_{rise} = 4\mu s$ during a switching event, v_{DS} selected as output.

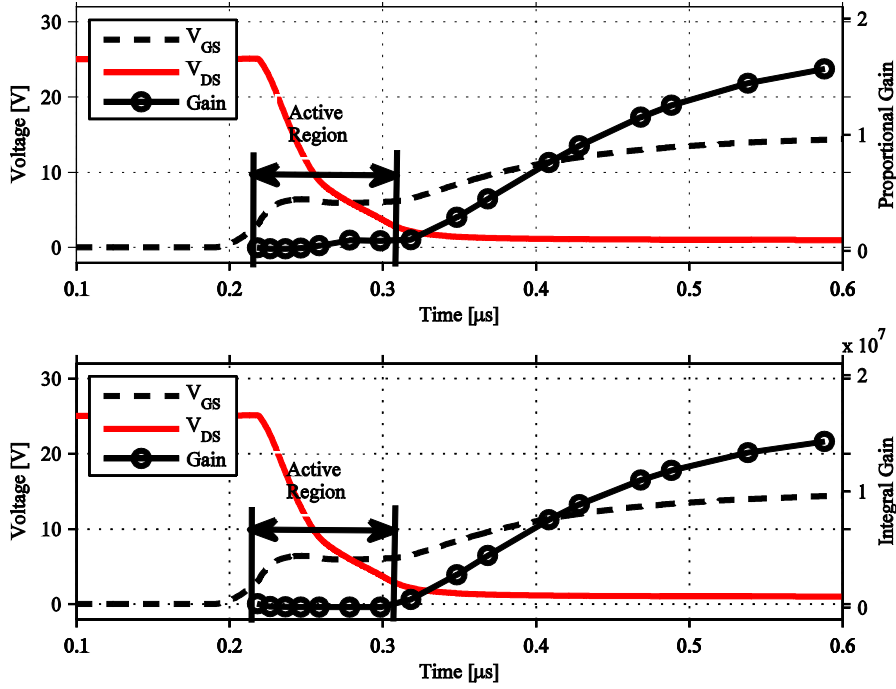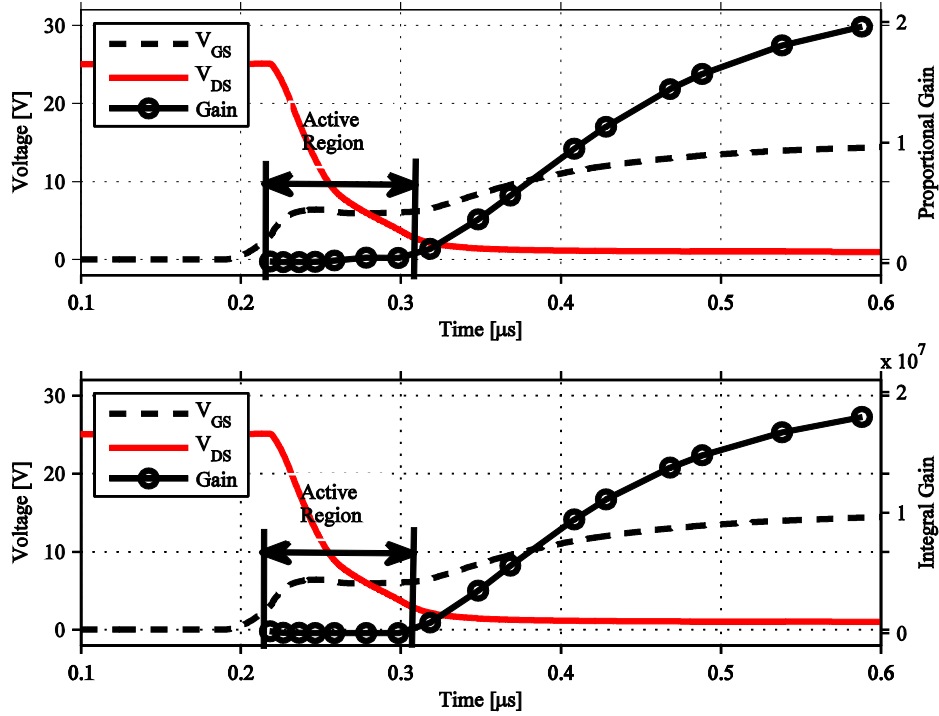operating points are used (i.e. points 2 and up in Figure 5.9), the step response becomes highly distorted. The most probable explanation of this relationship is that the integral gain of the controller becomes too large in order to initialize the switching event. This is illustrated in Figure 5.11 where the step response for the system including a mathematically derived controller for the first operating points in the active region is shown. The simulation results from the SPICE model and the proposed Simulink model show good agreement.

Also worth noticing in Figure 5.11 is the difference between the real rise time ($\approx 1.5\mu s$) which is significantly faster than the desired rise time ($4\mu s$). This discrepancy is seen for all analyzed rise times and is most likely explained by the change in the ingoing parameters as the switching event proceeds; a controller derived for the initiation of the switching event is not suitable any longer at the end of the switching event due to changes in the system parameters such as C_{GD}.
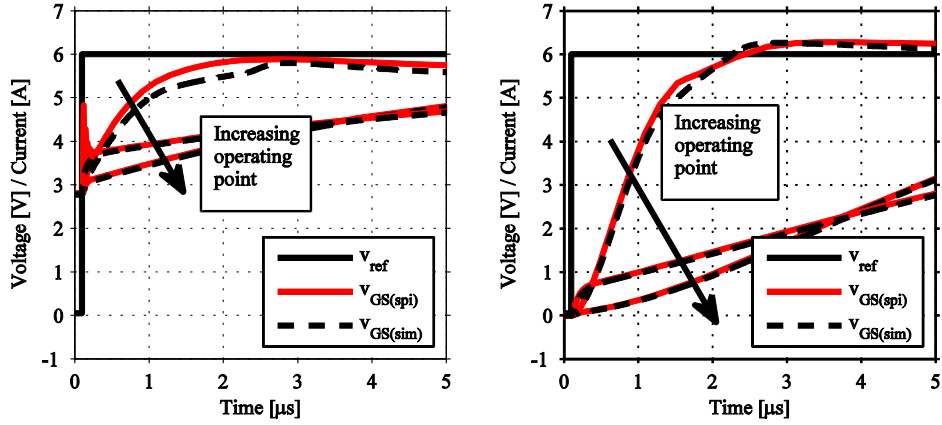
Fig. 5.11: Simulated step response with controller. i_{DS} as output, step from $0A$ to $6A$, $4\mu s$ rise time. Note that the dashed line is not visible due to overlapping.

The previously derived simulation results are also valid for real measurements, see Figure 5.12. Once again, the difference in static behavior between the simulation models and the measurements can be noted. Here is it foremost seen as a difference in threshold voltage which results in a slightly higher v_{GS} in the measurements ($V_{th} \approx 3.5V$) compared with the simulations ($V_{th} \approx 2.8V$) to reach the same current level. Once the switching event is initiated, at $t \approx 0.2\mu s$, the measured dynamic behavior show good agreement with the simulation results.

The mathematically derived controller can be compared with a controller derived with Ziegler-Nichols method as described in [120]. The critical gain of the system is found to be approximately 20 times ($K_c \approx 20V$) and the self oscillation period (T_c) to be $170ns$ ($\sim 5.9MHz$) around the current operating point. According to Ziegler-Nichols a suitable proportional gain can be found by
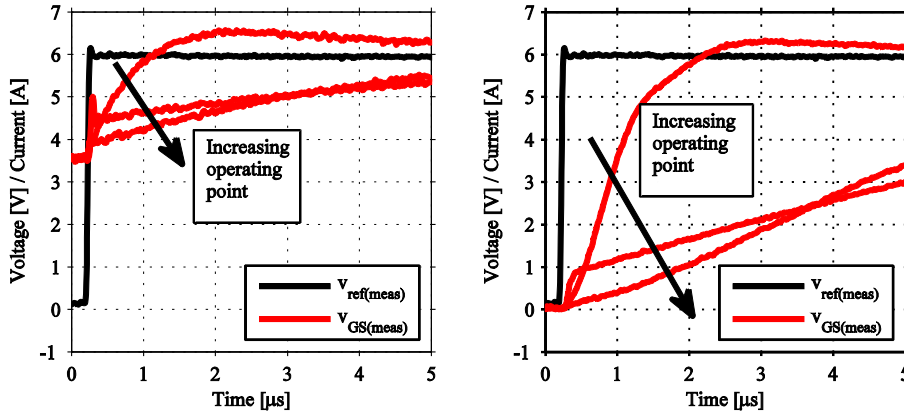
Fig. 5.12: Measured step response with controller. i_{DS} as output, step from $0A$ to $6A$, $4\mu s$ rise time.

$$K_p = 0.45 K_c. \tag{5.38}$$

and a suitable integral gain as

$$K_i = \frac{1.2 K_p}{T_c}. \tag{5.39}$$

which in this operating case gives $K_p = 9$ and $K_i = 6.35 \cdot 10^7$. If these parameters are applied to the controller structure in Figure 5.7, the results become slightly better than the one obtained by the mathematical derivation, see Figure 5.13. This method gives a fast controller with a small overshoot of the controlled quantity. The rise time is not controllable in the same sense as with the previous controller structure, it is rather determined by the system and controller properties, e.g. the ability of the controller to deliver sufficiently high voltage without saturating and the amount of current that the driver circuit can deliver.
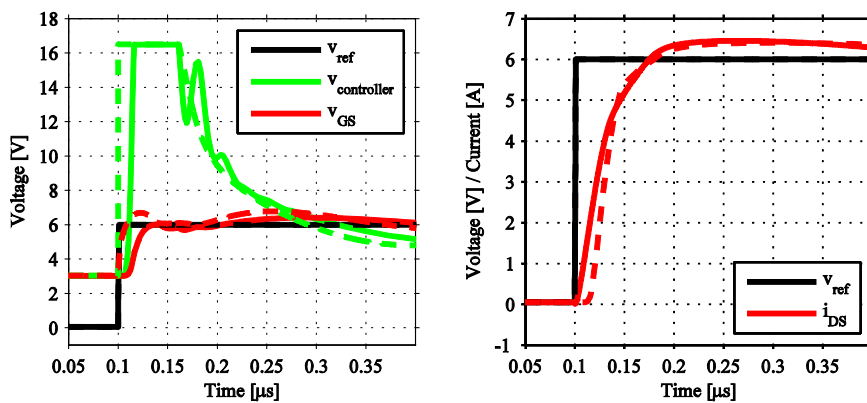
Fig. 5.13: Simulated step response with controller structure according to Ziegler-Nichols. i_{DS} as output, step from $0A$ to $6A$, $4\mu s$ rise time.

Another difference between the two simulation models that is worth noticing is the difference in performance of the controller system. In the Matlab model, the controller structure consists of a plain transfer function which gives an ideal performance on the basis of the derived parameters. In SPICE, the controller circuit consists of a model of the operational amplifier provided by the manufacturer (high speed operational amplifier LM6171 from National Instruments Inc. is used as controller and driver circuit) which in turn contains other parasitic elements that will cause a certain delay.

If v_{DS} is selected as output, the same conclusions still apply; the most suitable controller is always the one derived from the beginning of the switching event. This can clearly be seen if the step response for the system including a mathematically derived controller for the first operating points in the active region are compared, see Figure 5.14. Note that since v_{DS} increases when the MOSFET turns off, the parameter extraction is based on the turn-off event.

Once again, the simulation results from SPICE and the proposed Simulink model are very well corresponding. If measurements are compared to the simulation results, the most significant discrepancy that can be seen is the threshold level in v_{GS}, see Figure 5.14. Note that the simulations and measurements are very dependent on the specific shape of the reference waveform; e.g. offset voltage. If the controller cannot lower the voltage sufficiently due to conduction resistance of the component, the controller will saturate and it will inevitably take longer time to lower v_{DS}. In order to minimize conduction losses it is also of great interest that the MOSFET is fully turned on or off, respectively, which contradicts that the output shall be tracked along a trajectory for an entire switching period; it may be more advantageous to just track the switching event and once it is finished, make sure that the component is fully turned on or off by an external circuitry.
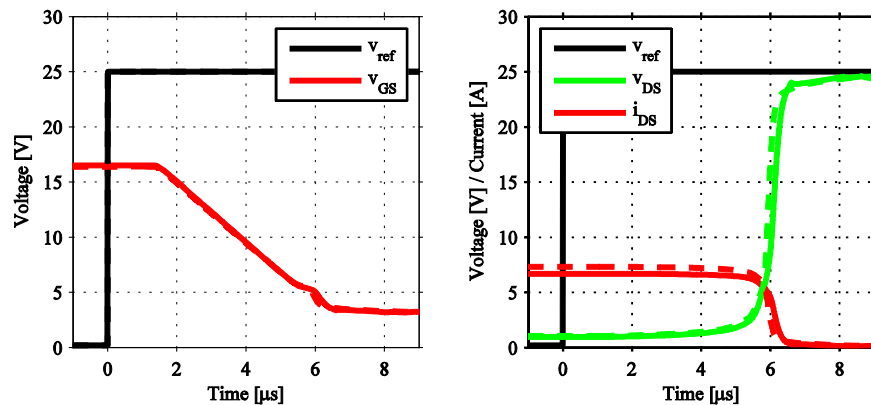

Fig. 5.14: Simulated step response with derived controller structures. v_{DS} output, step from $20mV$ to $25V$, $4\mu s$ rise time. Solid line: SPICE simulations. Dashed line: Matlab simulations (not visible due to overlapping).

Another problem that will appear when v_{DS} is selected as output is the delay that occurs before the voltage start to rise. This delay originates from the delay in the controller circuit and the time it takes for the controller to lower v_{GS} to reach the Miller region. Measurements show the same results and verify the simulations, see Figure 5.15. One way to minimize the problem is to slow down the controller, but simulations shows that the delay will always cause some delay in the circuit before the v_{DS} starts to rise.
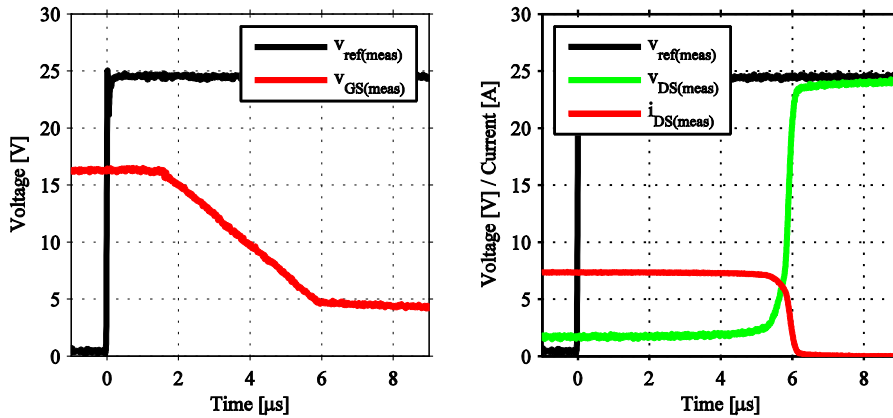

Fig. 5.15: Measured step response with derived controller structures. v_{DS} output, step from $20mV$ to $25V$, $4\mu s$ rise time.

5.4.2 Sinusoidal Step Response of the System

In order to implement active gate control, the behavior when a applying a sinusoidal reference waveform also needs to be analyzed. Figure 5.16 shows the simulated response of the system with i_{DS} selected as output when a sinusoidal reference with 4μs rise time is applied. It can be concluded that the SPICE model gives more accurate results compared with measurements due to the delay in the controller. The Simulink model gives a similar step response but slightly faster due to the lack of delay. The SPICE model shows good accuracy if a sinusoidal step is applied as reference voltage, see Figure 5.17. If a controller with parameters derived by the Ziegler Nichols method is simulated, a slightly better result is obtained, see Figure 5.18.

If the sinusoidal step response with v_{DS} selected as output, the previously mentioned delay becomes even more significant, see Figure 5.19 for simulation results and Figure 5.20 for measurements. In this case, the internal delay in the controller circuit has a minor effect compared to the time it takes for the controller to respond and lower the gate-source voltage to a suitable level. This delay was also observed in [121], their approach was to implement an external circuitry that pre-charges (or pre-discharges) the gate-source voltage just before the moment of transition. Also, a rather big discrepancy can be seen between the SPICE results
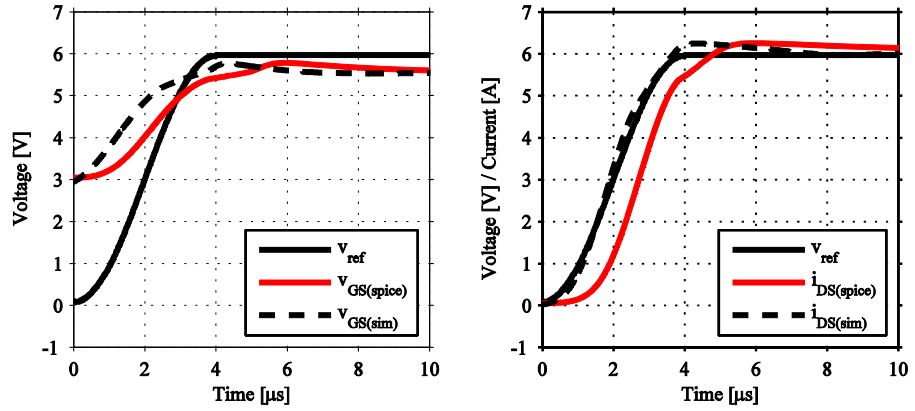
Fig. 5.16: Simulation results with sinusoidal reference. i_{DS} as output, $t_{rise} = 4\mu s$.
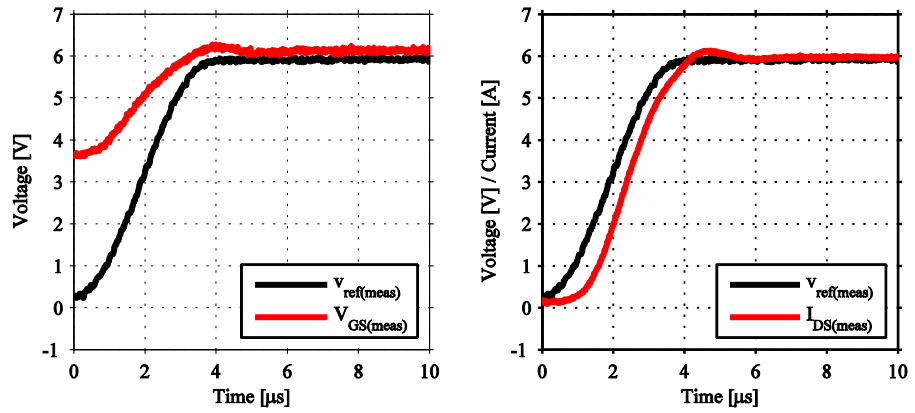
Fig. 5.17: Measurement results with sinusoidal reference. i_{DS} as output, $4\mu s$ rise time.
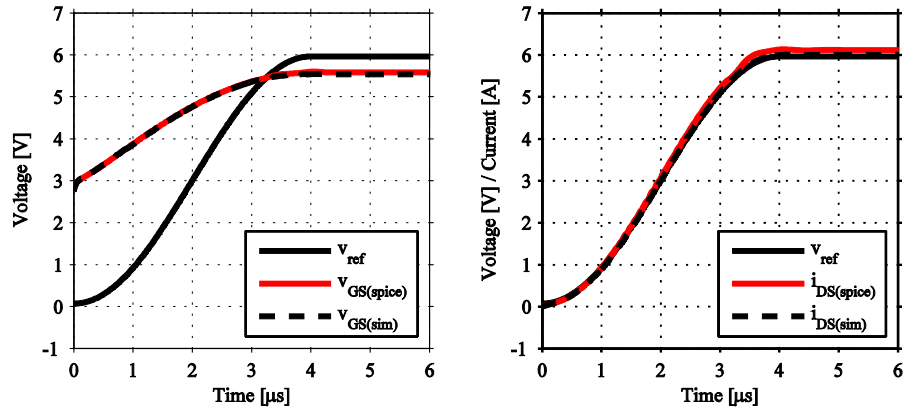
Fig. 5.18: Simulation results with sinusoidal reference, Ziegler-Nichols controller. i_{DS} as output, $4\mu s$ rise time.

and the results obtained by the Matlab model. This deviance most likely originates from an inadequate description of C_{GD} for the off transition.
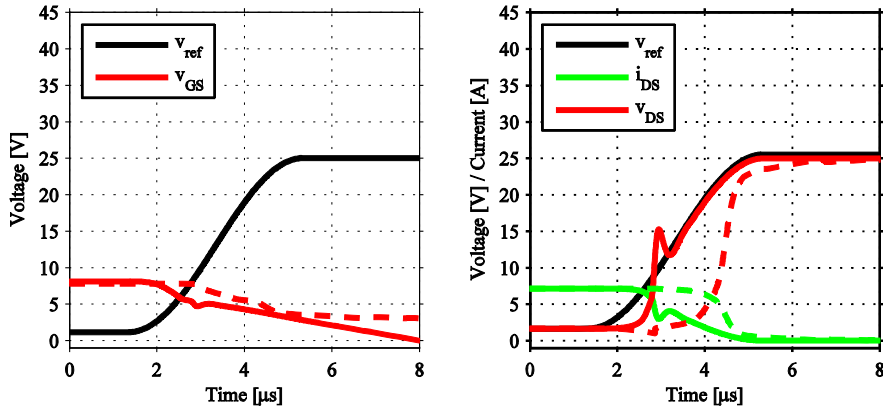
Fig. 5.19: Measured step response with derived controller structures. v_{DS} output, step from $20mV$ to $25V$, $4\mu s$ rise time. Solid line: SPICE simulations. Dashed line: Matlab simulations.

The results presented in [121, 122] showed that a slight improvement is possible by precharging the gate of the MOSFET. The external precharging circuitry increased the cost and the complexity of the circuit and made it rather sensitive to changes in operating conditions, e.g. supply voltage and reference voltage variations. All in all, the technique of external precharging was considered not worth investigating further due to these disadvantages.
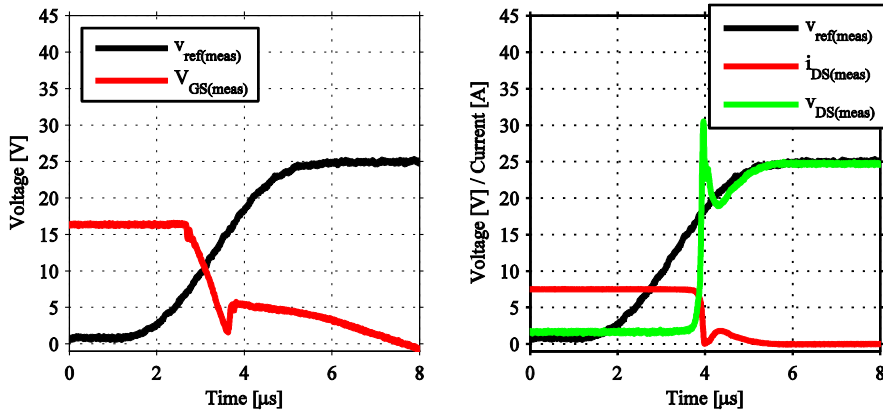
Fig. 5.20: Measured step response with derived controller structures. v_{DS} output, step from $20mV$ to $25V$, $4\mu s$ rise time.

Although an external precharging was found to be too complex, the idea can still be adapted to modern technology such as digital control. In order to make precharging more versatile and suitable for this type of system it can be of interest to completely implement the precharging circuitry within a digital controller. By doing this, the gate control is entirely embedded in a digital environment which

facilitates both adaptive control and removes the need for external circuitry that increases/decreases the v_{GS} once the transition has been passed. However, this kind of digital control is out of scope of this thesis and can be considered to be an interesting subject for further investigations.

Based on simulations and measurements it is concluded that the drain-source voltage is hard to control due to several reasons. The foremost disadvantage when controlling the v_{DS} is to adjust the reference voltage to the current operating conditions. This means that when the MOSFET is fully conducting, the voltage drop that becomes present over the component must be accounted for when comparing the measured voltage with the reference voltage. If these two voltages does not correspond, i.e. the reference voltage is lower than the measured voltage, the controller will saturate. The forward voltage drop over the MOSFET depends on several factors where v_{GS} is one of them. Also, in addition to finding the low level of the reference voltage, the high level also needs to be adjusted depending on the operating conditions (i.e. supply voltage). Parts of this reasoning are of course also valid when controlling the drain current; the main difference is that when the MOSFET is turned off, the drain current also goes to zero which gives no need for adjusting the reference voltage level during this time. Hence, all further investigations focused on controlling the drain current.

5.4.3 Controller Design with Varying Parameters

The controller designed with the proposed method must be valid over the entire operating range of the MOSFET, all parameter (e.g. C_{GD}) variations included. The reasoning in previous sections has shown that the parameter variations are too big for the controller to handle. This gives the need for adaptive design of the controller parameters; i.e. the controller parameters shall be adapted during the switching transition itself in order to better suit the system. This section is entirely based on theoretical reasoning and simulations due to practical complications. Variable controller design can be implemented in several different ways but since digital controller design has become more widespread during the last years, it may be one of the most flexible methods for implementation.

Once the method of adjusting the control parameters is decided, the actual controller parameters values must be determined. As indicated in previous sections in this thesis, the controller parameter extraction can be based on a linearized model of the entire system. Although this method is not completely stringent from a control theory point of view, it might result in approximate controller parameters suitable for this type of application. The control parameter variation can be based on three scenarios; $K_p, K_i = f(v_{GS})$, $K_p, K_i = f(v_{DS})$ or $K_p, K_i = f(v_{GS}, v_{DS})$. If the parameters are based on only one variable, a simple one dimensional curve fit can be made in order to extract the parameters, see

Figures 5.21 and 5.22 where the proportional and integral gain are plotted as functions of v_{GS} and v_{DS} respectively.
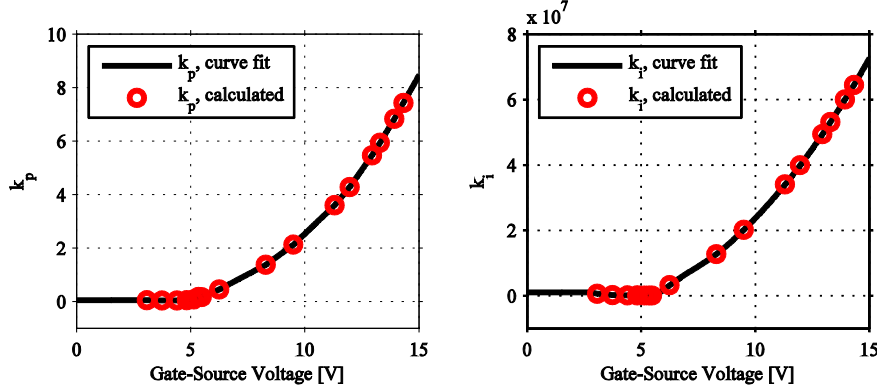
Fig. 5.21: K_p and K_i as a function of v_{GS} during a switching event.
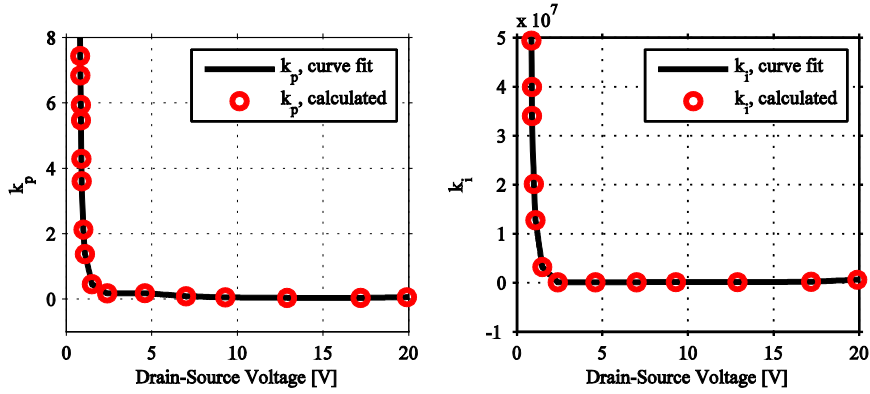
Fig. 5.22: K_p and K_i as a function of v_{DS} during a switching event.

Since the entire system, including the MOSFET, is implemented in Matlab, it is rather simple to implement a variable controller. The simulation results for a system including controller with a total rise-time of 4µs are presented in Figure 5.23 where the dashed line represents the step response of the system with controller parameters determined by only the drain-source voltage ($K_p, K_i = f(v_{DS})$) and the solid line represents the step response if the controller parameters are determined by the gate-source voltage ($K_p, K_i = f(v_{GS})$).

It can be noticed that the rise time for the system is approximately $9\mu s$ which is longer than the desired rise time ($4\mu s$). Also, the step response of the system is controlled with no overshoot. If results from simulations with adaptive control are compared with results from simulations with fixed parameters, see e.g. Figure 5.11, it can be concluded that adaptive control gives a more suitable step response with no overshoot, yet slightly slower than the desired rise-time.
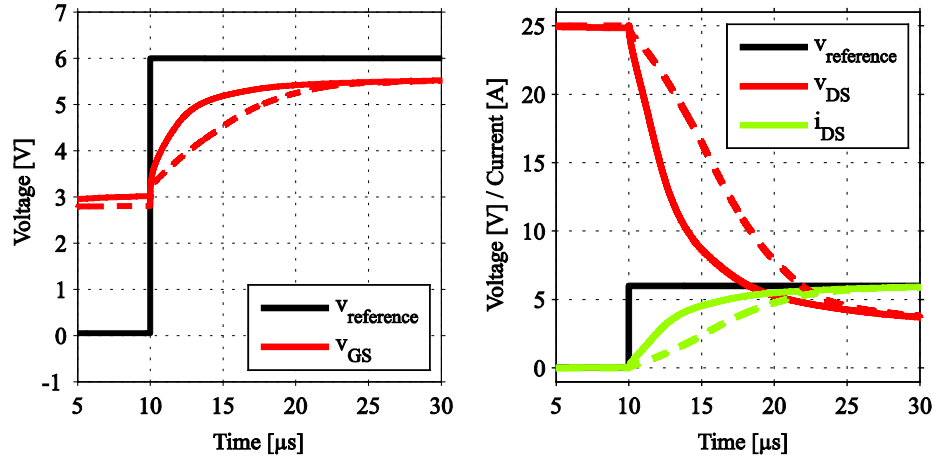
Fig. 5.23: Step response with variable controller structures. Id selected as output, step from $0A$ to $6A$ $4\mu s$ desired rise time. Dashed line: $K_p, K_i = f(v_{DS})$. Solid line: $K_p, K_i = f(v_{GS})$

One reason for the prolonged rise time of the step response might be the simplifications made to the transfer function of the system. This simplification implies that the derived controller parameters are approximations to actual parameters that suit the system. Another contributor to the error is the deviance in operating points; since the trajectory experienced by the system during the step response most likely will not fit the exact trajectory during the linearization process, the obtained control parameters can be inadequate. This divergence is a well known shortcoming with the proposed methodology.

In order to minimize the problem with finding suitable controller parameters when the proportional and integral gain changes during a switching event, the two controller parameters can be made dependent on two variables, $K_p, K_i = f(v_{GS}, v_{DS})$. In Figure 5.24, three different switching trajectories are shown as a function of v_{DS} and v_{GS}. Each switching trajectory are valid for the investigated system with different external voltages applied, i.e. the supply voltage v_{DS} and the peak value of v_{GS} is changed.

Based on these three switching trajectories obtained by simulations of the system without controller, the proportional and integral gain can be calculated in several discrete operating points in the vicinity of the trajectory. This is exactly the same methodology as described in Figure 5.8, but adapted for three different operating conditions. Based on these trajectories, an approximate surface can be created from which the approximate gain can be interpolated for all operating points that the system may experience, see Figure 5.25 for K_p-surface and 5.26 for K_i-surface. It shall be noted that this methodology is not completely stringent from a control theory point of view; the obtained gains shall rather be seen as a rule of thumb.
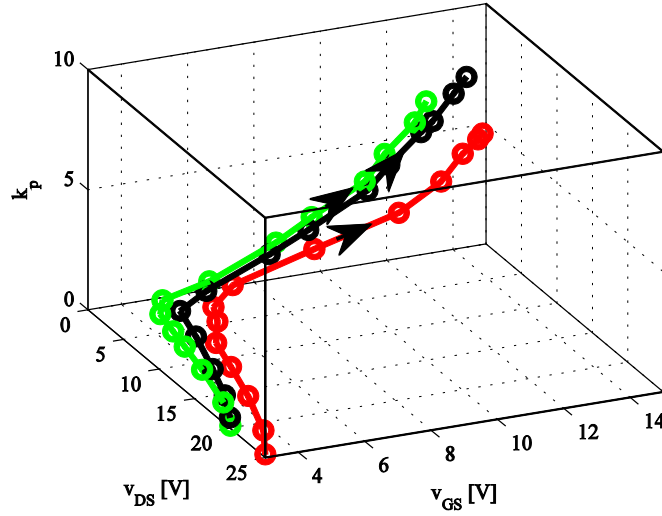
Fig. 5.24: K_p as a function of both drain-source and gate-source voltage during a turn-on event. Three different switching trajectories.
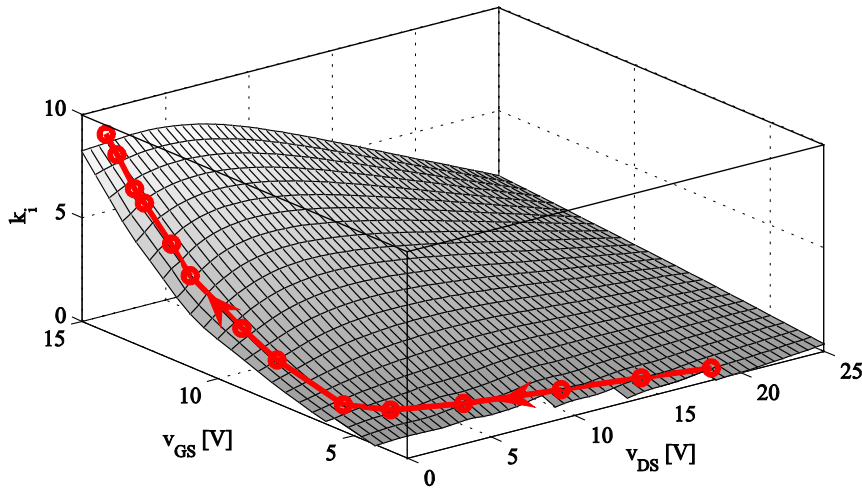
Fig. 5.25: Interpolated surface for K_p as a function of both drain-source and gate-source voltage during a turn-on event.

The main conclusion drawn from the variable gain is that the response of the system is strongly determined by the controller parameters. Since the fitted surfaces have high derivatives (e.g. $\partial K_p/\partial v_{DS}$ and $\partial K_p/\partial v_{GS}$) and large variations in parameter values around the trajectories (K_p vary with almost a factor of 200 and K_i vary with approximately a factor of 100), the system becomes sensitive to small changes in voltage. If incorrect controller parameters are chosen, the system will become unstable which gives that the fitted surface must be chosen very carefully in order to avoid instabilities in the system.
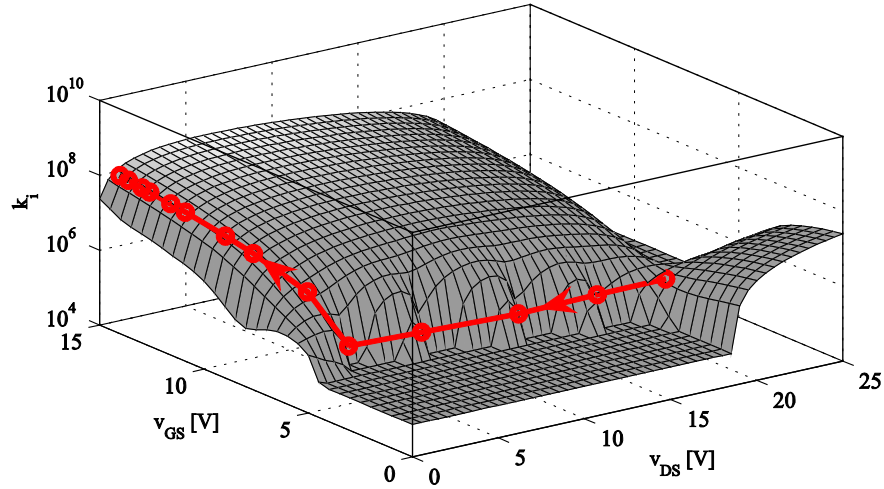
Fig. 5.26:   Interpolated surface for K_i as a function of both drain-source and gate-source voltage during a turn-on event.

By carefully fitting the surface to the calculated gain, a slightly better step response can be obtained from the closed loop system including controller compared to a system without adaptive control, see Figure 5.27. Yet, the step response is still not ideal; some fluctuations can still be observed and the shape is not ideally exponential, but the rise time is close to the desired $4\mu s$.
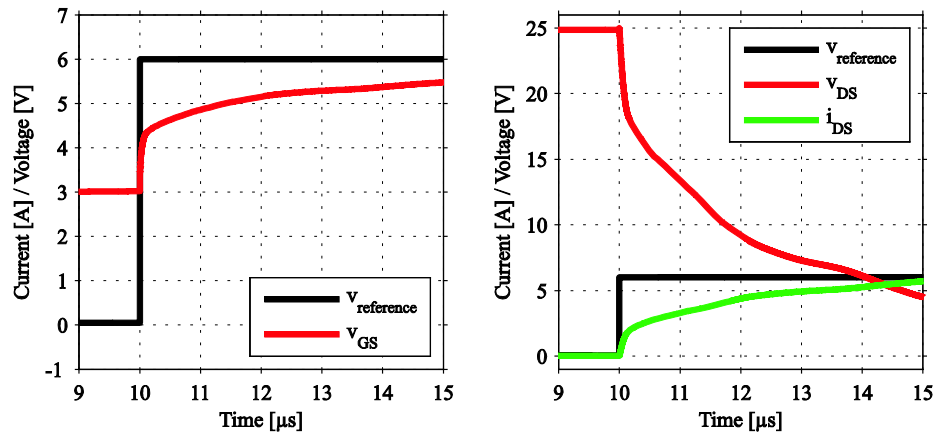
Fig. 5.27:   Simulation results of step response with adaptive control, $K_p, K_i = f(v_{GS}, v_{DS})$, $t_{rise} = 4\mu s$ and i_{DS} selected as output.

Since this system is intended for switching with sinusoidal transitions, the validity of the system was tested thoroughly with sinusoidal reference voltages, see Figure 5.28 for an example waveform with $t_{rise} = 4\mu s$. Based these simulations is can be concluded that the previously established reasoning holds true; when the controller parameters are solely determined by v_{DS} or v_{GS} the system response is

not adequate due to a mismatch between the controller parameters and the current operating point.

An example of this deviance can be seen Figure 5.28, left picture, where a sinusoidal reference voltage with $t_{\mathrm{rise}} = 4\mu s$ is applied to a system with $K_{\mathrm{p}}, K_{\mathrm{i}} = f(v_{\mathrm{GS}})$. By making the controller parameters dependent on both v_{DS} or v_{GS}, the system response gets slightly better, see Figure 5.28, right picture, where $K_{\mathrm{p}}, K_{\mathrm{i}} = f(v_{\mathrm{GS}}, v_{\mathrm{DS}})$. Once again, the controller parameters from the fitted surface do not entirely match the analytically obtained values for the current trajectory which can be seen as a small superimposed oscillation on i_{DS}.
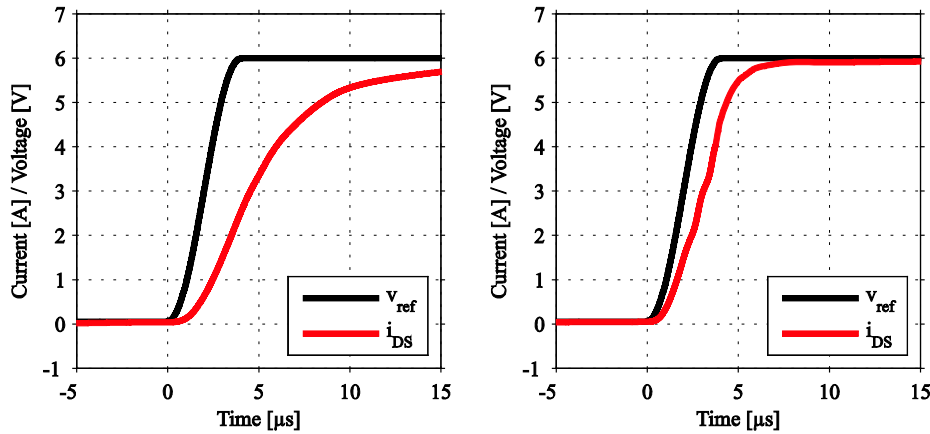
Fig. 5.28: Simulation results of sinusoidal transition and adaptive control. Left: $K_{\mathrm{p}}, K_{\mathrm{i}} = f(v_{\mathrm{GS}})$. Right: $K_{\mathrm{p}}, K_{\mathrm{i}} = f(v_{\mathrm{GS}}, v_{\mathrm{DS}})$.

5.4.4 Robustness of the Circuit

In order to evaluate the system stability and usefulness it is important to verify the circuit in different operating conditions. Until now, only one operating case has been evaluated; this section deals with problems that may arise when the operating conditions are changed and discussions regarding the system versatility. As previously discussed, it if found more advantageous to control the drain current than the drain-source voltage. By doing this, only one voltage level of the waveform has to be varied if the supply voltage changes. This is illustrated in Figure 5.29 where three different simulations with varying supply voltage are presented. As seen, only one of these voltages (25V) results in a correct shape of the controlled quantity. For the other two cases, 17V and 22V, the reference voltage is no longer adapted to the maximum drain current which causes the controller to saturate and the controlled quantity be distorted. For reasons of simplicity and the illustrative purpose of the figure, the simulations were made with fixed controller parameters.
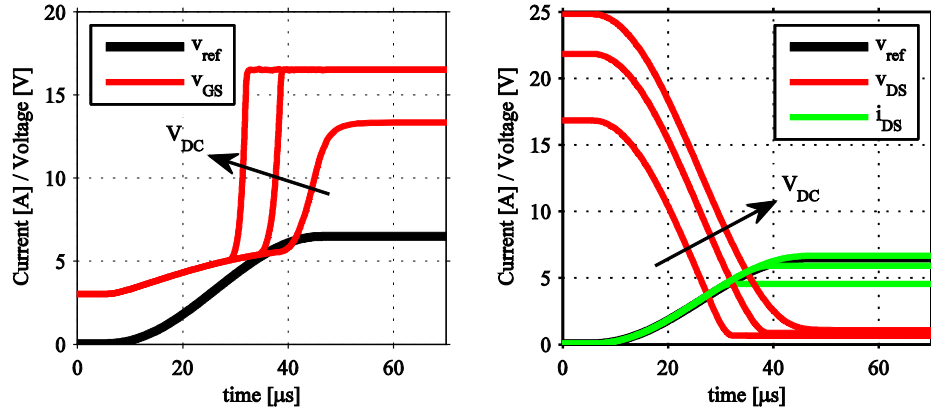
Fig. 5.29: Simulation results with sinusoidal transition and different DC-voltages. $v_{\mathrm{DC}} = 17V, 22V, 25V$

The same conditions also apply when the voltage level of the reference waveform is altered, see Figure 5.30 where three simulations with varying reference voltages are presented. For the case where $V_{ref} = 6.0V$, the MOSFET is not completely turned on which causes high conduction losses. On the other hand, if $V_{ref} = 7.0V$, the actual value of the current will never reach the reference voltage ($\sim 7A$) which causes the controller to saturate. This saturation leads to a distorted drain current during the turn-off event (not seen in the figure). The best performance is achieved when $V_{ref} = 6.5V$, hence, some kind of adaptation of the reference waveform is needed if changes in supply voltage are to be handled in a suitable way.
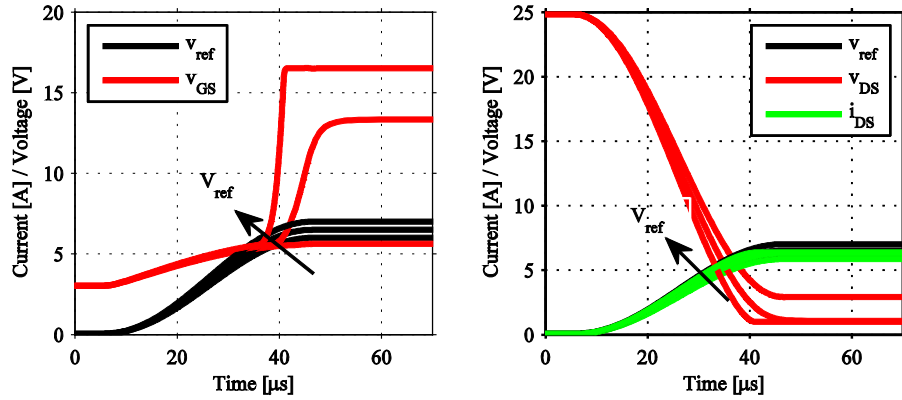
Fig. 5.30: Simulation results with sinusoidal transition and different reference voltages. $v_{\mathrm{ref}} = 6.0V, 6.5V, 7.0V$

5.4.5   Switching Losses with Active Gate Control

By implementing active gate control, the switching losses can be reduced with up

to 25% [122]. This is based on an assumption that the transition is purely trapezoidal as seen in Figure 5.31 where the simulated switching losses are shown for a sinusoidal and a trapezoidal transition with $t_{\text{rise}} = 20\mu s$. The switching losses (shaded area in Figure 5.31) for the sinusoidal transition and trapezoidal transition are approximately $0.60mJ$ and $0.52mJ$, respectively.
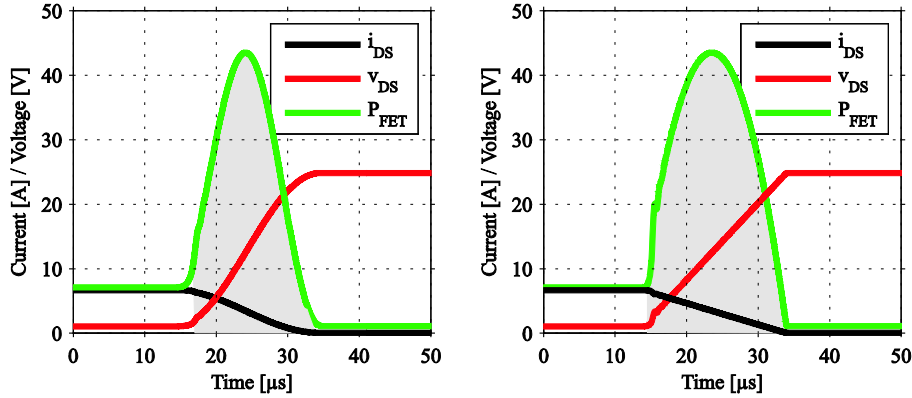
Fig. 5.31: Comparison between simulated switching losses in the MOSFET for $t_{\text{rise}} = 20\mu s$. Left: Sinusoidal transition. Right: Trapezoidal transition.

However, in some cases the transition is not really trapezoidal as suggested in Figure 5.31. For an inductive load with freewheeling diode the typical shapes of the voltage and current waveform can be seen Figures 2.19 and 2.20. If a simulation is made for this case where the current is not controlled during the switching event, i.e. a regular hard-switched converter, the results in Figure 5.32 are obtained. The switching losses are now slightly lower than those obtained with a sinusoidal transition; $0.42mJ$ for the hard-switched case and $0.52mJ$ for the previous sinusoidal case.
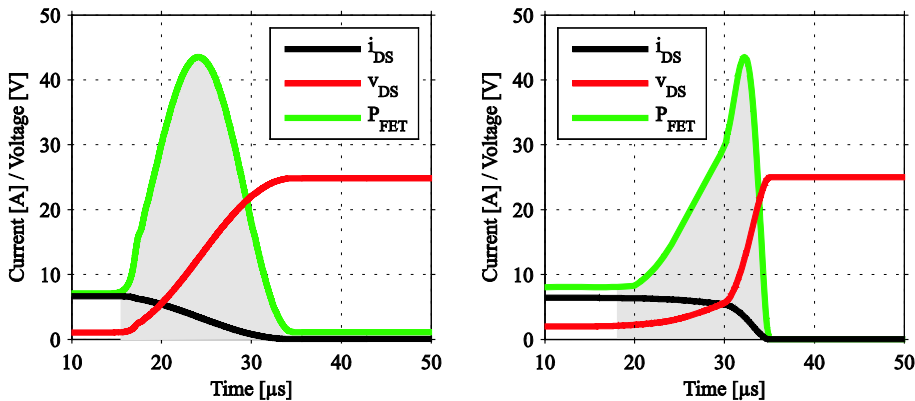
Fig. 5.32: Comparison between simulated switching losses in the MOSFET for $t_{\text{rise}} = 20\mu s$. Left: Sinusoidal transition. Right: Hard switched transition with freewheeling diode.

Note that caution has to be taken if the sinusoidal switching transition is made too long. In Figure 5.33 the transition for two different transition times are depicted; $t_{\text{rise}} = 4\mu s$ and $t_{\text{rise}} = 40\mu s$. For the case where $t_{\text{rise}} = 4\mu s$, the energy dissipated in the component during one switching event is approximately $0.09mJ$ and for $t_{\text{rise}} = 40\mu s$, the energy dissipation is approximately $1.0mJ$. From this simulation it can be concluded that if sinusoidal transitions are to be implemented, the energy dissipation in the component during the switching event has to be thoroughly investigated. For the current switching frequency $2464Hz$, the switching losses can be calculated to approximately $4.7W$ which can be considered too high for this type of application. However, under special circumstances there might be an application for this type of switching, e.g. for high voltage DC/DC converters operating with IGBT's where the switching frequency is rather low.
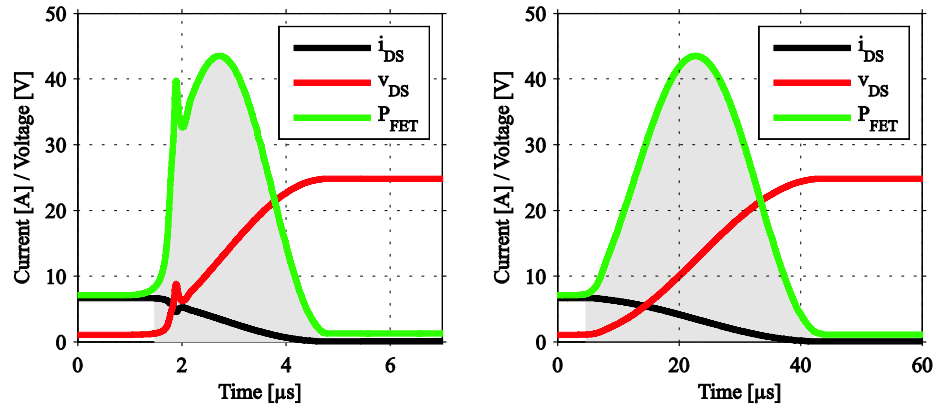
Fig. 5.33: Comparison between simulated switching losses in the MOSFET. Left: $t_{\text{rise}} = 4\mu s$. Right: $t_{\text{rise}} = 40\mu s$.

Chapter 6

Implementation into Converters

In this chapter, all the individual elements that were analyzed in the previous sections are put together into a complete system and evaluated from an EMI perspective. To do this, several parameters such as mutual coupling filter performance needs to be taken into account. The total system performance was simulated and verified by two different converters; a 60W buck converter with the possibility to apply both diode and synchronous rectification and a commercial 15W flyback converter.

6.1   Switching Circuit Modeling

Even a basic switching circuit sets high demands on the included models when correct EMI behavior is to be predicted. This is illustrated in Figure 6.1 that depicts a comparison between SPICE simulations and measurements of a switching circuit with resistive load (Figure 3.3). The circuit consists of many undefined stray elements, e.g. long component leads and a wire wound load resistor. The values of the stray elements can to a limited extent be determined if the analyzed circuit is not too complex and if the circuit is built in a controlled way [93]. A controlled way means e.g. that the characteristics of the ingoing components are well specified and that the circuit layout is well known in order to calculate the stray capacitances. Due to the long component leads and highly inductive resistors and capacitors, it becomes virtually impossible to determine the stray elements with sufficient accuracy. All of these stray elements contribute to the resonance circuits that are formed in the circuit; the voltage overshoot or resonance frequency as the MOSFET turns off becomes virtually impossible to calculate due to the many unknown parameters.

If instead a circuit that utilize surface mounted components including low inductive load resistors mounted on a PCB with advantageous layout, the results become significantly different, see Figure 6.1. The manufacturer MOSFET model (IRF7403) gives satisfactory switching behavior as previously concluded and the overshoots are minimized due to low inductive components. However, there are

still many unknown parasitic elements that are not accounted for in the simulation. This is acceptable in this case since the overall complexity of the circuit is low, but if a more complicated circuit is to be analyzed, as many elements stray elements as possible needs to be accounted for.
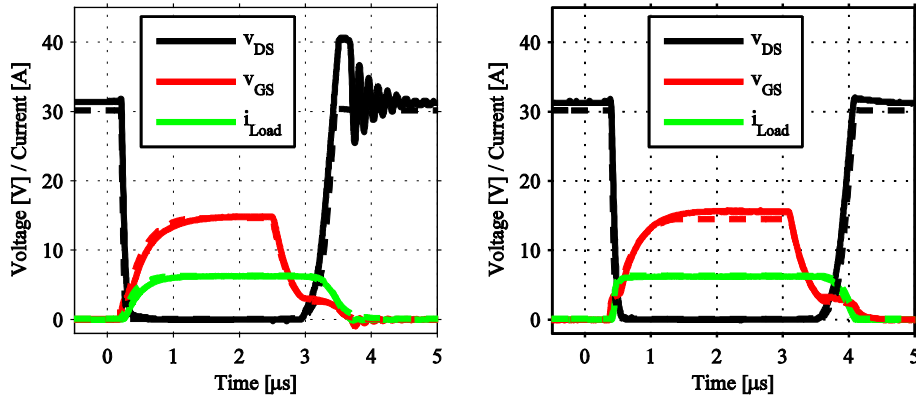
Fig. 6.1:   Comparison of measurements (solid line) and SPICE simulations (dashed line). Left: Switching circuit with hardwired layout and wire-wound load resistor. Right: Switching circuit with advantageous circuit layout and low inductive load resistor

6.2   Mutual Couplings and Filter Performance

6.2.1   Mutual Inductive Couplings

Each component in a circuit is affected by mutual couplings as described in Chapter 2.1.5 and to investigate how these couplings affect the performance of a filter, the π-filter in Figure 6.2 ($C_1 = C_2 = 1\mu F$ and $L = 2.2mH$) is investigated. The filter is analyzed both with measurements and by implementation in the FEM software Maxwell from Ansoft Inc. to establish values of the mutual couplings.
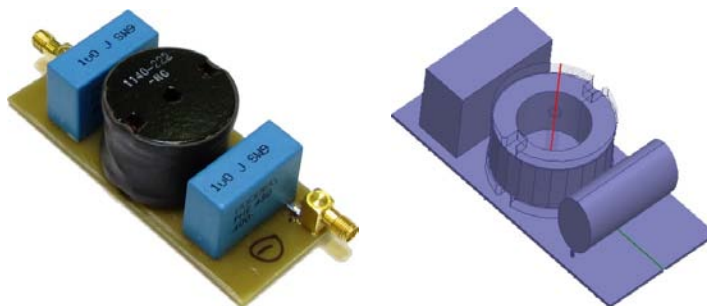
Fig. 6.2:   Analyzed input filter. Real filer and Maxwell implementation with cylindrical representation of the lower capacitor.

The implementation in Maxwell is only aimed at investigating the mutual inductive couplings between the ingoing elements in the circuit at low

frequencies, hence are no frequency effects (skin effect and ferrite properties) and capacitive effects taken into account. It is found that the most accurate modeling of the inherent inductance in a plastic film capacitor is achieved by approximating the metallic film roll with a cylindrical solid metal cylinder [123] as seen in Figure 6.2. left picture. The most important mutual couplings in the input filter are presented in Figure 6.3 and account for inductive coupling between inductor and capacitors (M_1 and M_2), inductive coupling between the inductor and trace loops (M_4 and M_5), inductive coupling between the two capacitors (M_3) and inductive coupling between input and output ground trace loops (M_6).
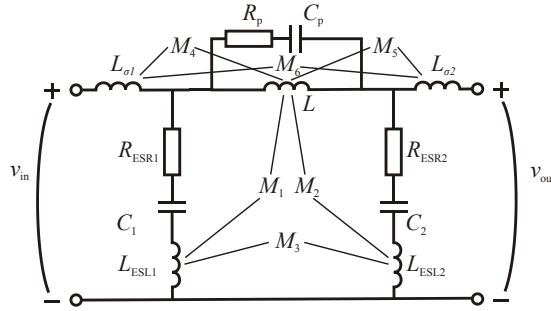
Fig. 6.3:   Equivalent circuit of the input filter including parasitic elements and mutual inductances.

The impedance of the ingoing inductor is characterized according to the previously described procedure with an impedance analyzer and the interwinding capacitance was found to be relatively large due to the large number of turns ($R_L = 494m\Omega$, $C_p = 70pF$ and $R_p = 7\Omega$). The stray parameters (L_{ESL} and L_σ) are calculated with both Maxwell and Q3d and compared to measurements where possible. Note that Ansoft Q3d only considers the PCB which only makes it possible to calculate the input and output trace inductances. All calculated inductances and mutual couplings are specified in Table 6.1. The measured L_{ESL} of the capacitors corresponds well to the measured values which verify that the cylindrical model of the capacitor is a good approximation of the current loop formed by a plastic film capacitor.

Table 6.1   Calculated and measured values of the stray elements and dominating mutual inductive couplings for the filter in Figure 6.2.

	L	L_{ESL}	R_{ESL}	$L_{\sigma 1}$	$L_{\sigma 2}$	M_1	M_2	M_3
Maxwell	$2.22mH$	$19nH$	N/A	$27nH$	$33nH$	$-795nH$	$795nH$	$0.32nH$
Q3D	N/A	N/A	N/A	$29nH$	$31nH$	N/A	N/A	N/A
Measured	$2.21mH$	$17nH$	$30m\Omega$	N/A	N/A	N/A	N/A	N/A

If the attenuation of the filter is analyzed according to the equivalent circuit in Figure 6.3, the difference between measurements and a filter with only parasitic

inductances becomes very significant, see Figure 6.4, left picture. However, if all calculated mutual coupling coefficients are implemented in the simulation model, the attenuation become comparable to the measurements (also presented in Figure 6.4, left picture). The most significant couplings were found to be M_1, M_2 and M_3 which all contribute to the total filter performance. The three remaining coefficients are relatively large ($M_5 = 243nH$, $M_4 = -194nH$ and $M_6 \leq 1pH$) but can in comparison with the dominating coupling factors be neglected. There is a discrepancy between the simulations and the measurements mainly at higher frequencies ($> 10MHz$) mainly due to the omission of capacitive couplings within e.g. connectors and an underestimation of the intrawinding capacitance (C_p). The Ansoft Maxwell model is considerably simplified compared with the real PCB and several factors such as frequency dependence and skin effects are left out for reasons of simplicity. Still, the results are satisfactory and point out that the magnitudes of the inductive coupling coefficients can be determined with relative simple measures.

As a comparison, a simulation where the PCB stray elements are calculated with Q3d is performed. By just adding the PCB stray elements via Q3d, a slight underestimation of the filter attenuation is obtained; see Figure 6.4, right picture. Such a configuration does not include any mutual coupling between external components, and by adding the dominating mutual inductive couplings (M_1, M_2 and M_3), the result will match the measurements slightly better, see Figure 6.4, right picture. Still, there is a slight overestimation of the mutual couplings which points out the difficulty to consider the influence of PCB stray elements, inductive couplings and capacitive effects at the same time.
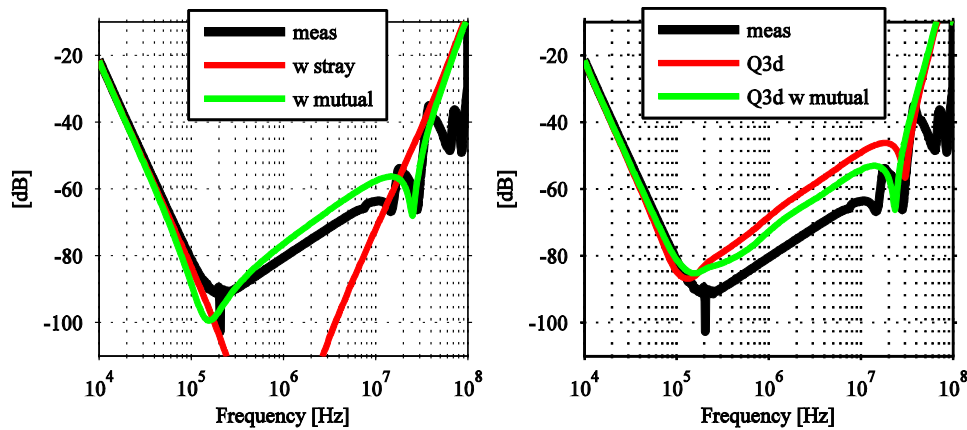

Fig. 6.4: Attenuation of the filter in Figure 6.2. Left: comparison of measurements and equivalent circuit in Figure 6.3. Right: comparison of measurements and co-simulation with Simplorer and Q3d.

6.2.2 Component Placement

It is well known that the inductive mutual couplings will be reduced if the orientation of the components is changed [124] and to illustrate this, the filter in Figure 6.5 is investigated. The components have same values as those used in the filter in Figure 6.2; the main difference is the orientation of the capacitors that is perpendicular to the inductor.
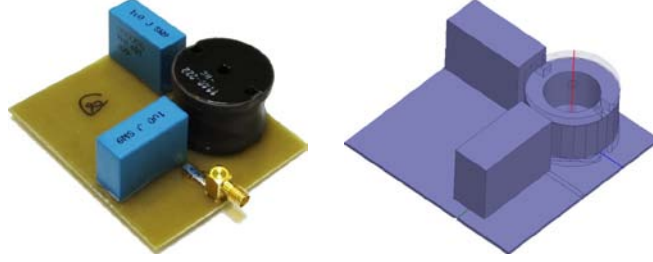
Fig. 6.5:   Analyzed input filter with perpendicular capacitors.
Real filter and Maxwell implementation.

The calculated and measured coupling parameters are presented in Table 6.2 where the inductances in the capacitors (L_{ESL}) are similar to the previously analyzed filter. The trace inductances are changed due to different lengths of the input and output traces and the inductive coupling coefficients between the inductor and the capacitors (M_1 and M_2) are drastically reduced. The three remaining coefficients are relatively large ($M_4 = -28nH$, $M_5 = 162nH$ and $M_6 \leq 1pF$) but can in comparison with the dominating coupling factors be neglected.

Table 6.2   Calculated and measured values of the stray elements and dominating mutual inductive couplings for the filter in Figure 6.5.

	L	L_{ESL}	R_{ESL}	$L_{\sigma 1}$	$L_{\sigma 1}$	M_1	M_2	M_3
Maxwell	$2.22mH$	$19nH$	N/A	$13nH$	$29nH$	$-0.29nH$	$0.64nH$	$0.29nH$
Q3D	N/A	N/A	N/A	$15nH$	$36nH$	N/A	N/A	N/A
Measured	$2.21mH$	$17nH$	$30m\Omega$	N/A	N/A	N/A	N/A	N/A

A similar analysis is performed for the filter with perpendicular capacitors as for the filter with parallel capacitors and the same tendencies can be seen. It is not sufficient to account for just stray elements (L_{ESL}, R_{ESL} and C_p) which is clearly seen if the attenuation of the filter is analyzed, see Figure 6.6, left picture. Since M_1 and M_2 are almost eliminated due to the perpendicular orientation, the dominating coupling factor was found to be the one between the input and output capacitors (M_3). If accounted for, the simulated attenuation becomes more similar to the measurements, but the resonance peaks in the measured attenuation around $0.1MHz$ and $5MHz$ are not captured in the simulations. The low frequencies suggest that the elements that cause the resonance are relatively large but their

origin is still unidentified. Note that the attenuation of the filter is improved due to the component orientation; the highest attenuation is now more than $90dB$ in the frequency range $0.1 - 1MHz$. As for the previously analyzed filter, a slight underestimation of the filter attenuation is obtained by co-simulating the PCB stray elements in Q3d, see Figure 6.6, right picture. An addition of the dominating mutual inductive couplings (mainly M_3) will give a simulation result that matches the measurements slightly better, see Figure 6.6, right picture.
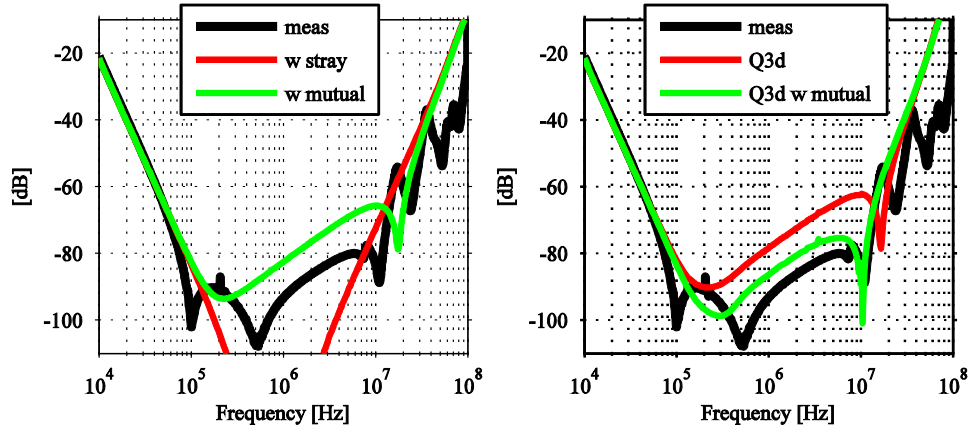
Fig. 6.6: Attenuation of the filter in Figure 6.5. Left: comparison of measurements and equivalent circuit in Figure 6.3. Right: comparison of measurements and co-simulation with Simplorer and Q3d.

Not just the orientation of the components contributes to the reduced mutual inductive couplings; the distance between the components also plays a dominant role. The π-filter in Figure 6.7 was designed to investigate the influence and consists of a $10\mu H$ inductor and two $68nF$ plastic film capacitors where the distance between the capacitors and the inductor can be changed in 4 steps of $2.5mm$.
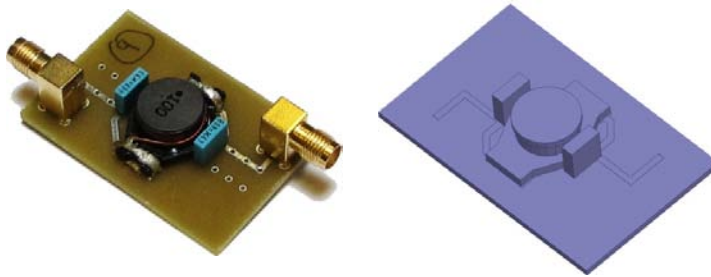
Fig. 6.7: Analyzed input filter, parallel capacitors with possibility to change the distance. Real filter and Maxwell implementation.

If the capacitor is located as close to the inductor as possible (position 1) the parasitic elements and mutual couplings in Table 6.3 are obtained. It is found sufficient to only consider the mutual couplings between the components (M_1, M_2

and M_3) since the remaining do not contribute to the overall performance in a significant way.

The measured and simulated attenuation of the filter is shown in Figure 6.8; both for the closest position to the inductor (left) and with varying distance (right). The discrepancy between the simulations and measurements are mainly two; the main resonance peak at $3MHz$ shows a slight deviation and the high frequency ($> 10MHz$) attenuation is slightly overestimated due to omission of parasitic effects. The shift in resonance peak at $3MHz$ has to do with the fact that the inductance decreases with frequency (see also Table 6.3) due to a decline in the permeability in the ferrite material.

Table 6.3   Calculated and measured values of the stray elements and dominating mutual inductive couplings for the filter in Figure 6.7.

|	L	L_{ESL}	R_{ESL}	$L_{\sigma1}$	$L_{\sigma1}$	M_1	M_2	M_3
Maxwell	$10.8\mu H$	$8.5nH$	N/A	$31nH$	$31nH$	$1.25nH$	$1.27nH$	$2pH$
Measured	$9.5\mu H$	$9nH$	$10m\Omega$	N/A	N/A	N/A	N/A	N/A
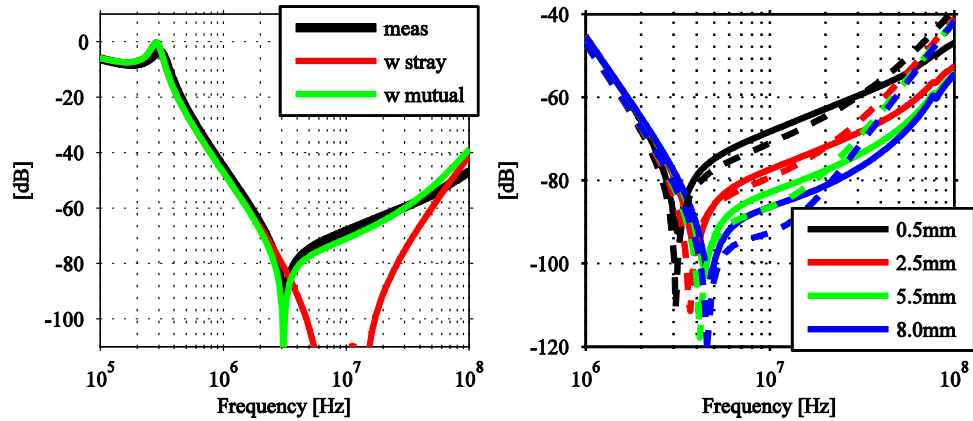
Fig. 6.8:   Attenuation of the filter in Figure 6.7, comparison of measurements and equivalent circuit in Figure 6.3. Left: capacitor positioned closest to the inductor (0.5mm). Right: measurements (solid) and simulations (dashed) of attenuation with varying distance from the inductor.

If the $68nF$ capacitors are placed perpendicular to the inductor, see Figure 6.9, the coupling is drastically reduced. The filter performance is significantly improved, (see Figure 6.10, left picture) and attenuation well below $100dB$ for a wide frequency range is obtained. Even though the coupling coefficients are small ($M_1 = 1.27nH$, $M_2 = 1.25nH$ and $M_3 = 2.5pH$), they still contribute to the overall performance and the simulation becomes sufficiently accurate.

How the coupling coefficients vary as a function of the distance from the inductor is illustrated in Figure 6.10, right picture. Its also worth noting that the angular deviation of the capacitors contribute to the magnitude of the coupling coefficient; the lowest value will be obtained if the capacitor is oriented exactly 90° radial from the inductor.
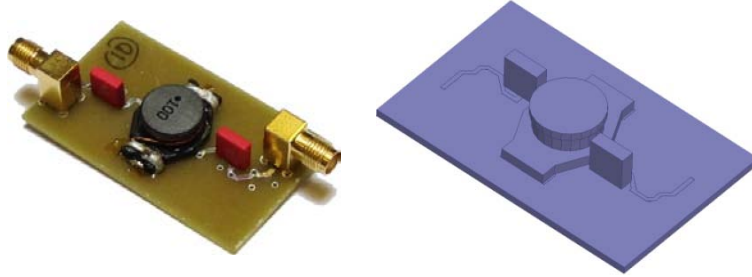
Fig. 6.9: Analyzed input filter, perpendicular capacitors with possibility to change the distance. Real filter and Maxwell implementation.

Fig. 6.10: Left: Idealized reverse recovery current waveform. Right: harmonic content of the ideal reverse recovery waveforms.

6.3 The Influence of Reverse Recovery on EMI

As described in previous chapters, every pn-diode will show some kind of reverse recovery; since this event is a fast transition of the current it contains high amounts of harmonics and will inevitably affect the conducted emissions as shown later. The harmonic content in the reverse recovery can be described mathematically according to [125]. This is illustrated in Figure 6.11 where an idealized current waveform including reverse recovery is depicted. The idealized curve form includes a finite rise and fall time (t_r and t_f) and an current overshoot caused by the reverse recovery (I_{RM}). The derivatives are assumed to be constant for all current rises and falls for reasons of simplicity.

Fig. 6.11:   Idealized reverse recovery current waveform.

For an ideal pulsed waveform with trapezoidal rise and fall times, the harmonics will decrease with $20dB/decade$ until a cut off frequency $(1/\pi/t_r)$ that is determined by the derivative of the rise and fall times. At higher frequencies, the harmonics will decrease with $40dB/decade$. However, if a recovery phenomenon is included, the current peak gives rise to an increase in the harmonics at the same frequency range as the cut off frequency due to the rise and fall time of the current. In Figure 6.12, left picture, two currents ($I_F = 8A$, $f = 200kHz$, $D = 0.3$) with recovery current peaks at 100% and 200% of the forward current, respectively, are presented. The resulting harmonic content is seen in Figure 6.12, right picture. A large recovery current will give rise to increased harmonic levels at frequencies slightly lower than the cut-off frequency, in the investigated current derivatives the increase will be approximately $8dB\mu A$ at $\sim 5MHz$ compared with a waveform without reverse recovery. A lower recovery will give rise to increased harmonic levels at a higher frequency, in this case $4dB\mu A$ at $\sim 13MHz$. Note that since the curve form is ideal, oscillations due to parasitic elements are not accounted for.
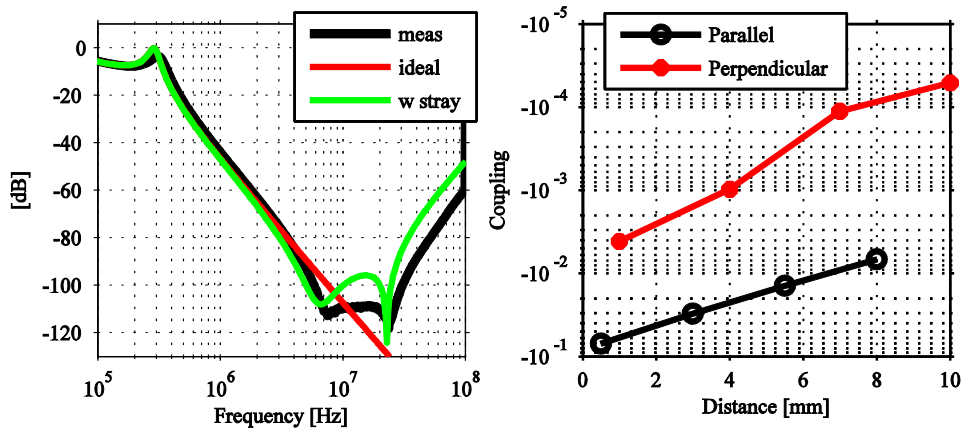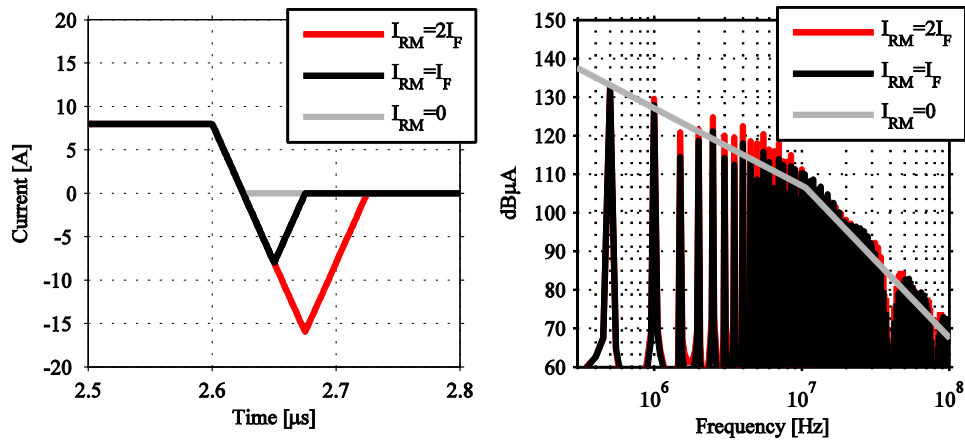

Fig. 6.12:   Left: Idealized reverse recovery current waveform. Right: harmonic content of the ideal reverse recovery waveforms.

The harmonic content in the recovery waveform depends on the shape of the recovery current which gives that the previous reasoning is only valid for recovery currents with equal derivatives. If instead a more real resembling recovery current curve form is analyzed, the shift in harmonics becomes less distinctive, see Figure

6.13. A current with soft recovery will in this case result in increased harmonics at $\sim 4MHz$ which is the same as for a current with greater recovery peak current and shorter recovery time. From this analysis it can be concluded that at hard recovery of the diode recovery will increase the harmonic content at higher frequencies; for the analyzed waveform the increase will be most pronounced at $5 - 30MHz$.
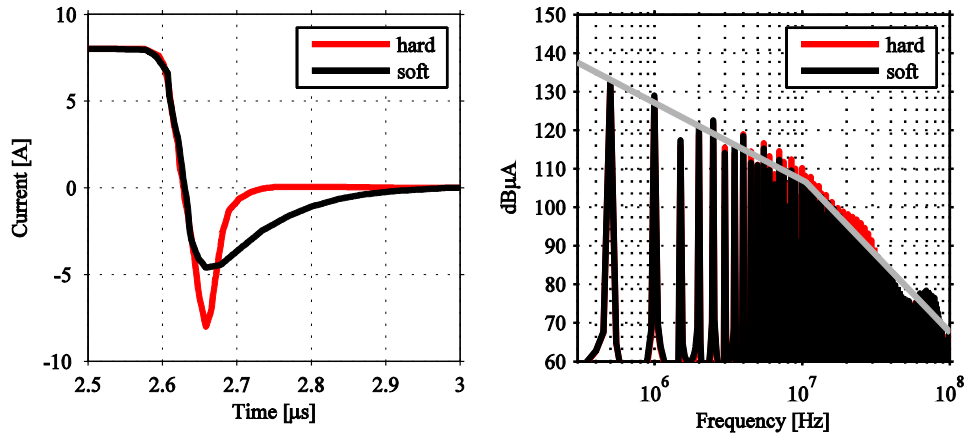
Fig. 6.13: Left: Representation of realistic reverse recovery current waveforms. Right: harmonic content of the realistic reverse recovery waveforms.

6.4 Implementation into a Flyback Converter and Influence of Reverse Recovery

The details and operating conditions for the investigated flyback is presented in Chapter 3.7.1. The simulation model of the converter consists of passive components that are characterized over a broad frequency range by impedance measurements as described in Chapter 4.1. For this investigation, the parasitic elements in the PCB interconnectors are characterized by approximations (e.g. stray inductance $5nH/cm$ for a PCB connector) due to reasons of simplicity.

The transformer consists of a ferrite core (EFD12/6/3.5-3F3 with $160\mu m$ air gap, $N_1 = 21$, $N_2 = 6$) which frequency dependent impedance was characterized using an impedance analyzer (HP4395A). The impedances were measured in four steps; from primary to secondary side with the secondary side open and shorted, respectively, and from secondary to primary side with the primary side open and shorted respectively. By such a thorough measurement procedure, each parasitic element (e.g. leakage inductances and interwinding capacitances) on both sides of the transformer can be identified. The parameters were fitted to the equivalent circuit shown in Figure 6.14, which show a clear resemblance to the earlier investigated model in Figure 4.27. The major difference is that due to reasons of simplicity and software compatibility, the Jiles-Atherton model in Chapter 4.1.5 is

replaced with simple inductor models and mutual couplings.
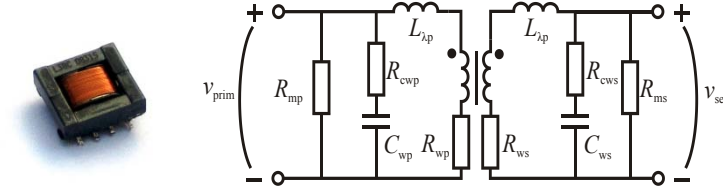
Fig. 6.14:   Photo of the analyzed Flyback transformer and equivalent electric circuit that accounts for parasitic elements.

The primary inductance of the transformer was determined to $L_p = 43.4uH$ with a coupling coefficient $k = 0.28$ to simulate the turns ratio. Each stray element was identified to $C_{wp} = 2.3pF$, $C_{ws} = 1.1pF$, $L_{\lambda p} = 150nH$, $L_{\lambda s} = 17nH$, $R_{cwp} = 120\Omega$, $R_{cws} = 80\Omega$, $R_{ws} = 5m\Omega$ and $R_{wp} = 33m\Omega$. The parameter identification procedure results in a transformer model that matches the measurements well up to $100MHz$; see Figure 6.15 that shows a comparison of the simulated and measured impedance as function of frequency for all possible measurement cases.
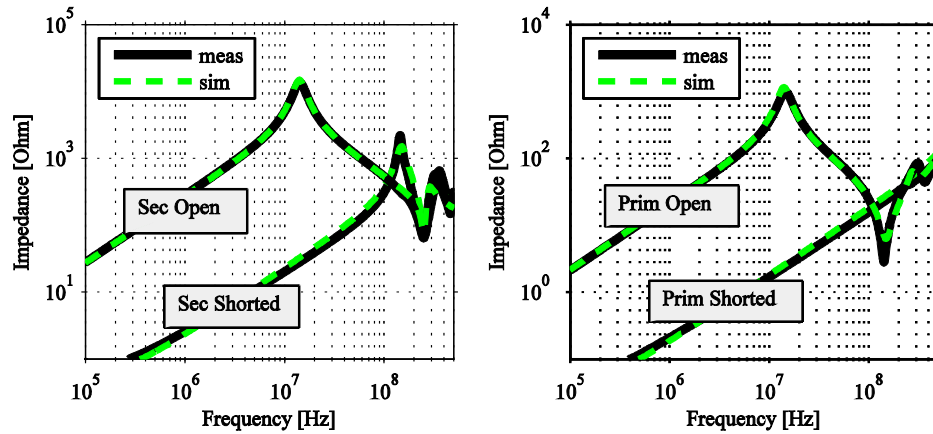
Fig. 6.15:   Impedance as function of frequency for the analyzed flyback transformer. Solid line: measurements. Dashed line: Simulated equivalent circuit including parasitic elements according to Figure 6.14.

To evaluate how the reverse recovery event of a diode affects the conducted emissions, two pn-diodes with different reverse recovery was chosen for the investigation. The diodes were selected so that the other stray elements (e.g. junction capacitance and package parasitics) are as similar as possible, see Table 6.4. I addition to the pn-diodes, two Schottky diodes were also investigated to evaluate how the lack of reverse recovery in combination with a larger junction capacitance affects the emission levels, see Table 6.5 for Schottky diode specifications. Each diode was modeled with SABER® Power Diode Tool® with datasheet values and graphs used as input.

Table 6.4   Specifications of the evaluated pn-diodes.

Diode	I_F	V_R	$V_F@I_F$	t_{RR}	$C_{tot@50V}$	L_S
8ETH06	$8A$	$600V$	$2.0V@8A$	$18ns$	$24pF$	$5nH$
8ETU04	$8A$	$400V$	$1.2V@8A$	$60ns$	$30pF$	$5nH$

Table 6.5   Specifications of the evaluated Schottky diodes.

Diode	I_F	V_R	$V_F@I_F$	$I_{R@25C}$	$C_{tot@20V}$
MBRS540T3	$5A$	$40V$	$0.42V@3A$	$0.3mA$	$140pF$
30BQ100	$3A$	$100V$	$0.65V@3A$	$0.5mA$	$60pF$

6.4.1   The Input and Output Filters

For the investigated Flyback converter, the input filter consists of two $1\mu F$ ceramic capacitors from Kemet (C1210C105KRAC) and a $10\mu H$ open core inductor in a π-configuration similar to the one investigated in Figure 6.3.

The inductor is modeled with a main inductor ($L = 10.5\mu H$) with a parallel capacitance ($C_p = 9pF$) to model the interwinding capacitance and a resistor ($R_p = 5\Omega$) to dampen the resonance peak. The validity of the model is discussed in Chapter 4.1.5 but with the difference that the Jiles-Atherton model is replaced with an ideal inductance. The capacitors are modeled with discrete SPICE models provided by the manufacturer which have been proven to be valid also for high frequencies since they include parasitic elements such as equivalent series inductance (ESL) and resistance (ESR). The ideal filter shows a significant resonance at $67kHz$ and higher frequencies are shunted by the input and output capacitors, see Figure 6.16, left picture. If the parasitic elements in the circuit are accounted for, the resonance frequency is slightly shifted ($71kHz$) and higher frequencies are attenuated due to stray inductances, also depicted in Figure 6.16, left picture.

The last parameters that must be accounted for in the input filter are the mutual couplings between inductive components and other current loops. If the mutual couplings are accounted for in the input filter, the impedance is not affected in a significant way, see Figure 6.16, right picture.

If the transmission characteristics of the filter (the ratio between an ideally transmitted voltage and the voltage applied across the filter), the influence of the
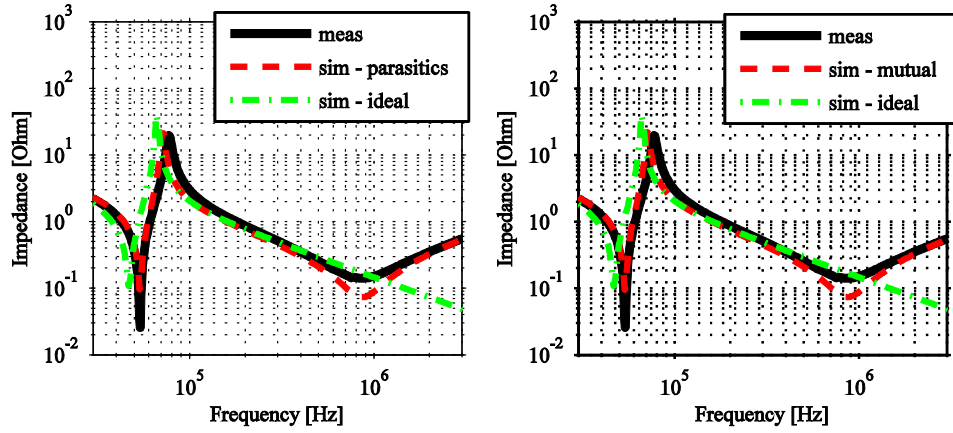
Fig. 6.16: Flyback input filter impedance including only stray elements (left picture) and stray elements with added mutual inductances (right picture).

mutual couplings becomes observable. If only parasitic inductances and capacitances are included, the filter will still attenuate high frequencies rather well; see Figure 6.17, left picture. The two resonant peaks caused by the capacitor series inductance ($2MHz$) and the inductor intrawinding capacitance ($1.6MHz$) can also be observed. If mutual inductive couplings are accounted for, the filter performance can be matched to the measurements, see Figure 6.17, right picture.
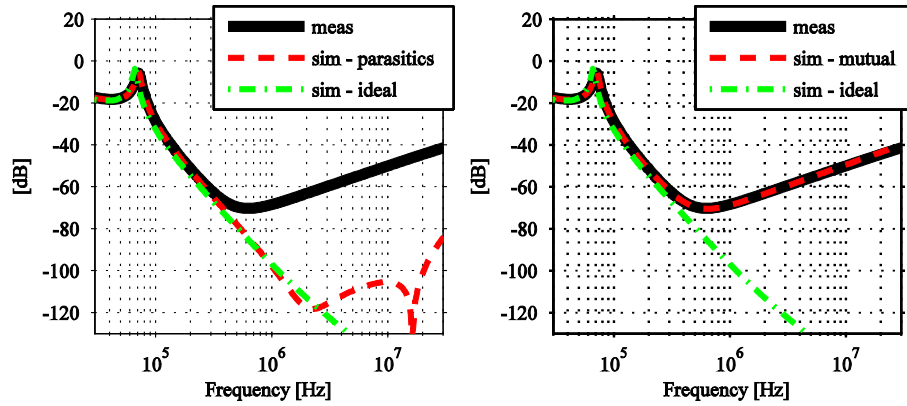
Fig. 6.17: Flyback input filter attenuation including only stray elements (left picture) and stray elements with added mutual inductances (right picture).

All six coupling coefficients contribute to the overall high frequency performance of the filter, but the most important coupling coefficients were found to be the coupling between the main inductor and the input and output trace loops ($M_4 = 14nH$ and $M_5 = 25nH$). Figure 6.18 shows a photo of the input filter that aim to facilitate the origin the interpretation of the mutual inductances.
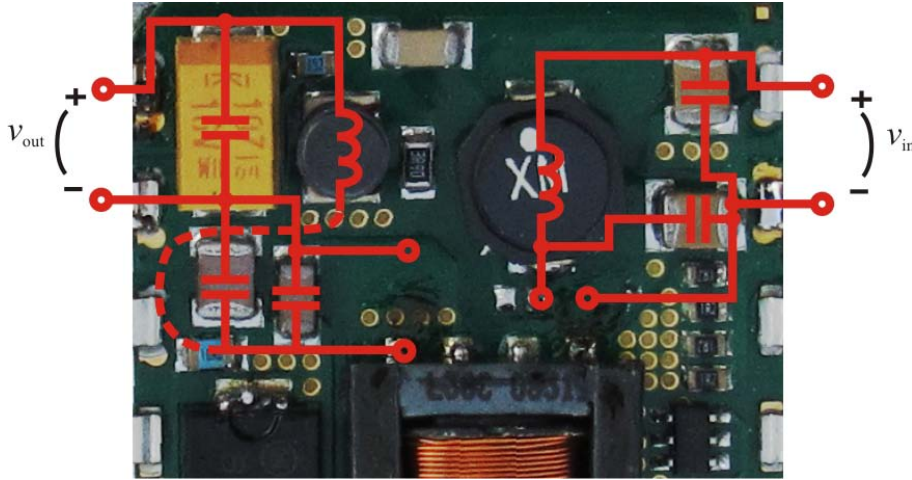
Fig. 6.18:   Photo of the component placement in the input and output filter of the Flyback converter.

A part of this coupling may be related to the measurement equipment, but the measurement procedure (short probe leads, small loops and thorough calibration of the impedance analyzer) aims to ensure that the measurement results actually reflect the inductive couplings from the passive components and not from probe interconnectors. The main inductor also couples to both capacitors, but the coupling to C_2 is significantly smaller compared to the coupling to C_1. This difference most likely originates from the orientation between the components; since C_2 is oriented perpendicular to L, the coupling will be reduced compared with C_1 that is oriented parallel with L. The coupling between the input and output trace loops is relatively small ($M_6 = 0.3nH$) and the coupling between the capacitors is also reduced due to the perpendicular orientation between themselves.

The output filter is also configured as a low-pass filter in a π-configuration, see Figure 6.19. As for the input filter, the capacitor models are provided by Kemet ($C_1 = 2.2\mu F$ and $C_2 = 4.7\mu F$ ceramics and $C_3 = 100\mu F/16V$ tantalum) which are encircled by a dashed box in Figure 6.19. The inductor ($L = 1\mu H$) is built on an open core with measured winding parasitics $C_p = 7.2pF$ and $R_p = 53\Omega$.
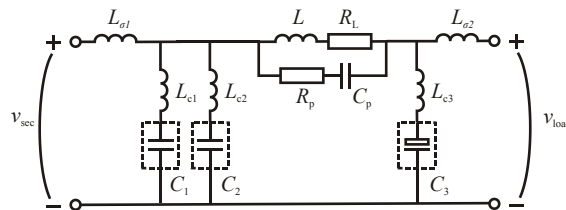
Fig. 6.19:   Equivalent circuit of the output filter including parasitic elements

The impedance seen by the transformer (v_{sec}) is determined by the characteristics of the ceramic capacitors and their interconnectors and is satisfactory estimated by the simulation model, see Figure 6.20, left picture. On the other hand, the impedance seen by the load is strongly determined by the frequency characteristic of the output tantalum capacitor (C_3), see Figure 6.20, right picture which shows some discrepancies at lower frequencies ($< 1MHz$).
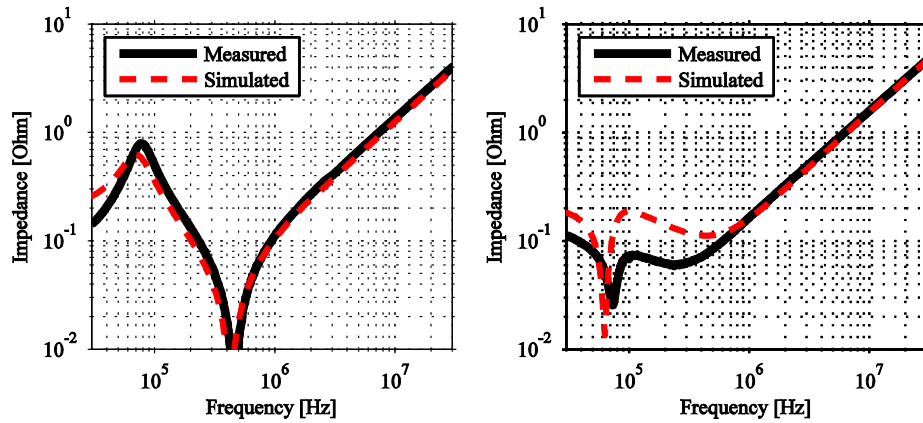
Fig. 6.20: Impedance of the output filter. Solid line represents measurements and the dashed line represents simulations. Left: impedance from v_{sec} to v_{load}. Right: impedance from v_{load} to v_{sec}.

The divergence in impedance from v_{load} to v_{sec} most likely originates from the simulation model of the tantalum capacitor (Kemet T494X107M016AT) which results in the deviations at lower frequencies ($< 1MHz$). At frequencies higher than $1MHz$, the series inductance of both the output terminals ($L_{\sigma 2} = 19nH$) and the interconnector to the capacitor ($L_{C3} = 3nH$) starts to dominate.

6.4.2   Oscillations in the Circuit

The overall conformity of the reverse recovery current is very satisfactory in SABER® since it incorporates a more adequate diode model, see Figure 6.21, right picture, that show a comparison of simulations and measurements for the pn-diode 8ETU04. What is worth noting is once again that if a similar diode is implemented in SPICE, a significant discrepancy in recovery behavior can be seen. The simulation models gives a slightly steeper derivative (440A/μs) compared with the simulations (400A/μs) most likely due to a slight underestimation of the parasitic inductances within the PCB and component interconnectors. Note that the possibility to measure currents requires some kind of current sensor to be implemented in the circuit which is difficult due to the surface mounted component. The increased current loop will inevitably implicate increased stray inductance which may result in misleading results for the final converter.
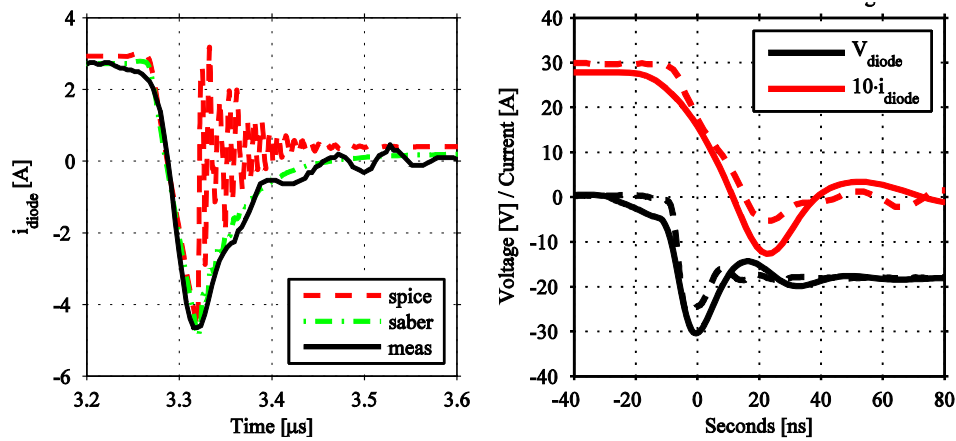
Fig. 6.21:   Left: Diode current for diode 8ETU04. $v_{in} = 48V, i_{out} = 3A$. Right: Diode current and voltage for Schottky diode MBRS5540T3 ($v_{in} = 48V, i_{out} = 3A$). Comparison of measurements (dashed line) and SABER® simulations (solid line).

If a Schottky diode is analyzed during turn off, no real reverse recovery is present, but the switching behavior still resemble a recovery event due to the oscillations in the current, see Figure 6.21, right picture. The overall conformity in the diode current is satisfactory, but a slight difference in current overshoot and oscillation frequency can be noted. Once again, the discrepancy originates from inadequately represented parasitic elements in, mostly within the diode and in the PCB. The parasitic elements also cause a discrepancy both in the voltage overshoot and in the voltage oscillation frequency between the simulations ($31MHz$) and in the measurements ($\sim 50MHz$).

6.4.3   Conducted Emissions with pn-diodes

The reverse recovery event in a standard *pn*-diode will not just contribute to increased losses, but it will also affect the conducted emissions. From the simulations, the peak recovery current for the diode 8ETH04 was found to be approximately 40% greater than for the diode 8ETH06 ($I_{RR(8ETH06)} = 2.0A$ compared with $I_{RR(8ETU04)} = 2.8A$). The current derivative was constant for the two diodes ($100A/\mu s$) since they had same packaging (TO220) and consequently also stray elements with similar magnitude. The increase in recovery current results in an increase in the simulated harmonic content at approximately $10MHz$, see Figure 6.22, left picture.

The same tendency is also observed in the measurements where the high frequency harmonics (>30MHz) are increased while mid frequency harmonics ($10MHz - 30MHz$) are decreased if a diode with lower reverse recovery is implemented, see Figure 6.22, right picture that shows the measured harmonics.
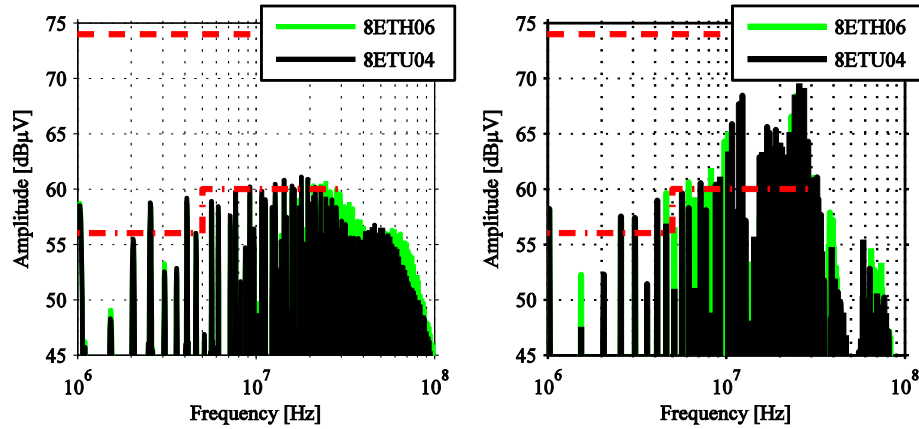
Fig. 6.22:   Comparison of conducted emission levels for two *pn*-diodes with different reverse recovery (8ETU04 and 8ETH06). $P_{out} = 15W$. Left: Simulations from SABER®. Right: Measurements.

This shift in harmonics is also predicted by the mathematical analysis of the diode current. If diode current from the simulation that serves as base for the harmonic analysis in Figure 6.22, left picture, is analyzed, it can be seen that diode 8ETH06 gives a slightly sharper reverse recovery, see Figure 6.23, left picture. The harmonic analysis (Figure 6.23, right picture) shows that the diode with lower reverse recovery (8ETH06) results in higher harmonic content at frequencies $> 50MHz$. The diode with greater reverse recovery (8ETU04) gives a significant increase in harmonics compared with an ideal trapezoidal curveform; at most $10dB\mu A$ at $50MHz$. Note the similarity to Figure 6.13 that shows a mathematical analysis of a theoretical reverse recovery event.

The conducted emissions from a converter are strongly dependent on the load current; higher currents within the circuit results in higher induced voltages in e.g. stray inductances. For a regular *pn*-diode, the reverse recovery current will show different behavior depending on the load; as the current increases, the peak recovery current will also increase. This result not only in higher conducted emissions as previously discussed, but also in a shift in peak harmonic content as previously discussed. If the output current is increased from $I_{load} = 1A$ to $I_{load} = 3A$, the recovery current peak in diode 8ETU04 will according to the simulations increase from $I_{RR(1A)} = 1.2A$ to $I_{RR(1A)} = 2.8A$. This is reflected in the both simulated and measured conducted emission levels, see Figure 6.24, left picture, and Figure 6.24, right picture, respectively. For the investigated case, a lowered reverse recovery once again gives increased harmonic levels at high frequencies ($> 50MHz$).
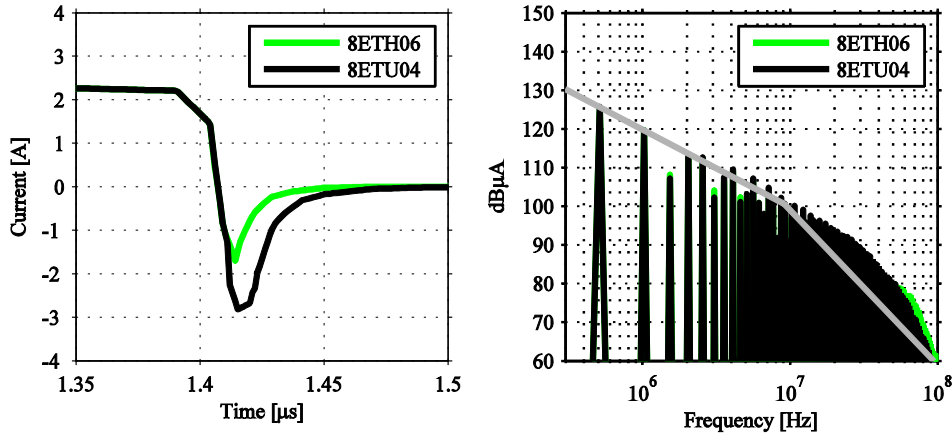
Fig. 6.23: Left: Simulated diode reverse recovery current for two different diodes ($P_{out} = 15W$). Right: harmonic content of the simulated reverse recovery waveforms..

6.4.4 Emissions with Schottky diodes

Since the inherent capacitance of the investigated Schottky diodes is significantly larger than the one found in the investigated pn-diodes, oscillations with higher amplitude are more likely to occur. The fact that the package inductance is slightly lower (SMC for the Schottky diodes and TO-220 for the pn-diodes) also contribute to the oscillations in the circuit due to a slight increased current derivative during current commutation from the diode. The voltage over the diode (v_{diode}) shows a strong oscillation with different frequencies depending on the type of diode, see Figure 6.25.
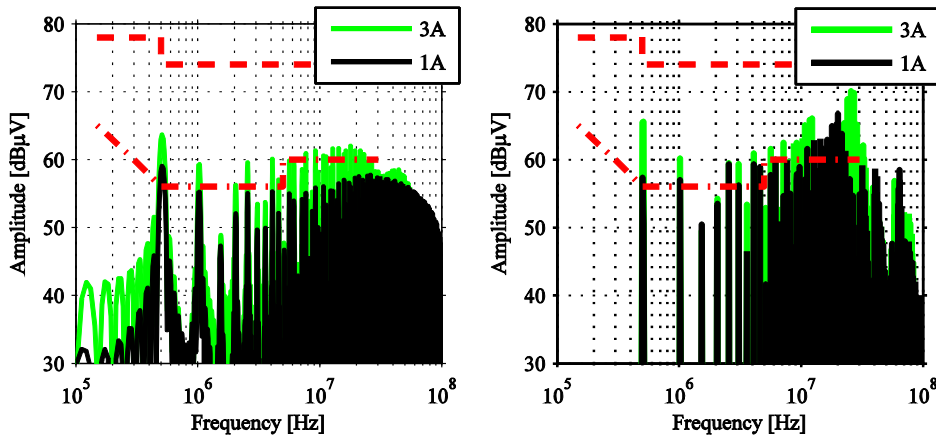
Fig. 6.24: Comparison of conducted emission levels for two different load cases ($P_{out} = 5W\ and\ P_{out} = 15W$), 8ETU04 as diode. Left: Simulations from SABER®. Right: Measurements.

Fig. 6.25:   Comparison of measured v_{DS} for two Schottky diodes with different junction capacitance (MBRS540T3 and 30BQ100). $P_{out} = 10W$.

The diode MBRS540T3 has a larger inherent capacitance which results in a lower frequency ($\sim 90MHz$) compared with diode 30BQ100 ($130MHz$). The resonance frequency can be approximated with

$$f_{\text{resonance}} = \frac{1}{2\pi\sqrt{L_{\text{stray}}C_{\text{diode}}}} \tag{6.1}$$

which in combination with $f_{\text{resonance}} = 130MHz$ and $C_{30BQ100@18V} = 63pF$ gives the stray inductance $L_{\text{stray}} = 24nH$. This is a reasonable approximation of the total secondary inductance since the output leakage inductance of the transformer was estimated to $L_{\sigma 2} = 17nH$ and a reasonable package inductance lies in the range of $3 - 4nH$ according to component datasheeet. If the measured harmonic content is analyzed, the oscillation with the diode MBRS540T3 is found in the frequency spectrum at $\sim 90MHz$, see Figure 6.26, right picture. The simulation model gives a satisfactory prediction of the harmonic content up to approximately $10MHz$, see Figure 6.26. The predicted oscillation for diode MBRS540T3 is slightly lower than the one found in the measurements, but for diode 30BQ100, the high frequency oscillations are not captured adequately. The discrepancy in the levels of the simulated and measured high frequency harmonics are caused by a combination of inadequately characterized LISN devices and parasitic elements in the simulation model.

6.5   Step Down Converter and the Effect of Synchronous Rectification

The step down converter is described in Chapter 3.7.2 and is in this chapter analyzed with several different rectifying options. This investigation is aimed at
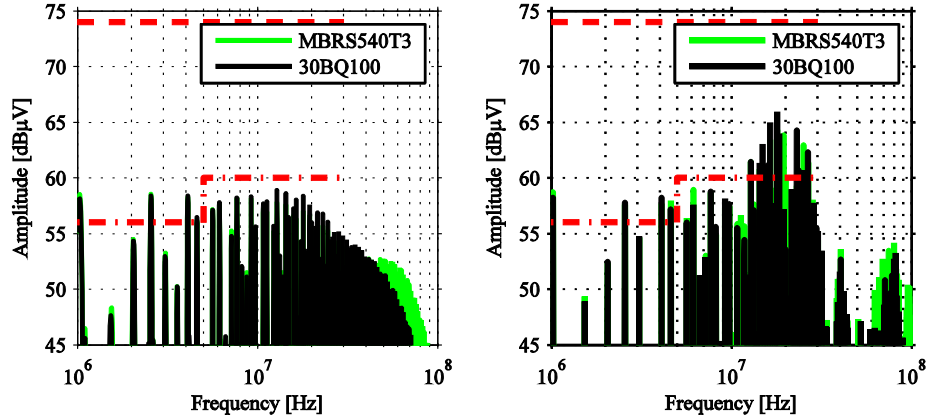
Fig. 6.26: Comparison of conducted emission levels for two Schottky diodes with different junction capacitance (MBRS540T3 and 30BQ100). $P_{out} = 10W$. Left: Simulations from SABER®. Right: Measurements.

two different objectives; to evaluate the validity of the Ansoft Q3D parasitics extraction tool and to evaluate how different rectification options affect the conducted emissions.

6.5.1 The Step-Down Input Filter

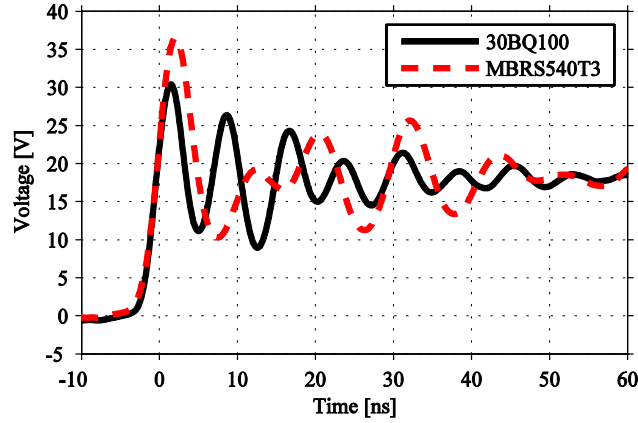The input filter of the step-down converter consists of an iron powder inductor (Micrometals T106-26, $N = 21$) in combination with two $10\mu F$ tantalum electrolytic capacitors in series (T495A105M035), one electrolytic (Jamicon $33\mu F/63V$) capacitor as energy storage and one $1\mu F$ ceramic capacitor (C1812F105K1RAC), see Figure 6.27. Each type of capacitor serve different purposes and the aim is to in combination form a satisfactory EMI filter.
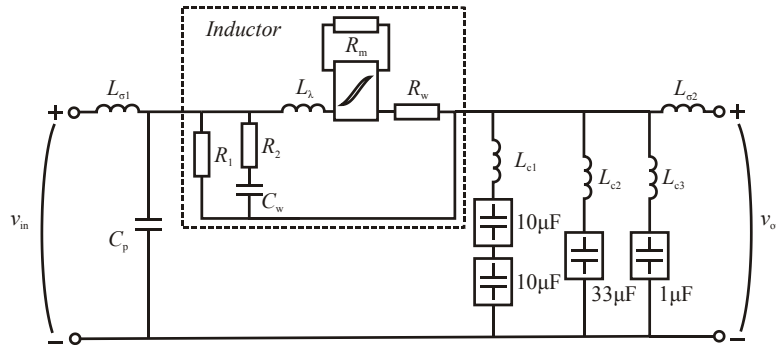
Fig. 6.27: Equivalent circuit of the input filter including parasitic elements

The input inductor is modeled with the Jiles-Atherton model found in Simplorer which provides a previously defined BH-loop for the chosen iron powder material from Micrometals (T106-26). The material was chosen for both the input and output inductor due to its high saturation flux density. Figure 6.27 shows the

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inductor (dashed box) represented as a part of the total input filter and include stray elements that model intrawinding capacitance (C_w) and leakage inductance (L_λ). The reluctance of the core is calculated from the core geometry ($A_m = 0.659cm^2$, $l_m = 6.59cm$, $R_m = 10.6 \cdot 10^6 At/Wb$) and the high frequency behavior (mainly determined by the intrawinding capacitance, C_w) of the standalone inductor is identified using an impedance analyzer (HP4395A), see Figure 6.28, left picture, for resulting impedance as a function of frequency.
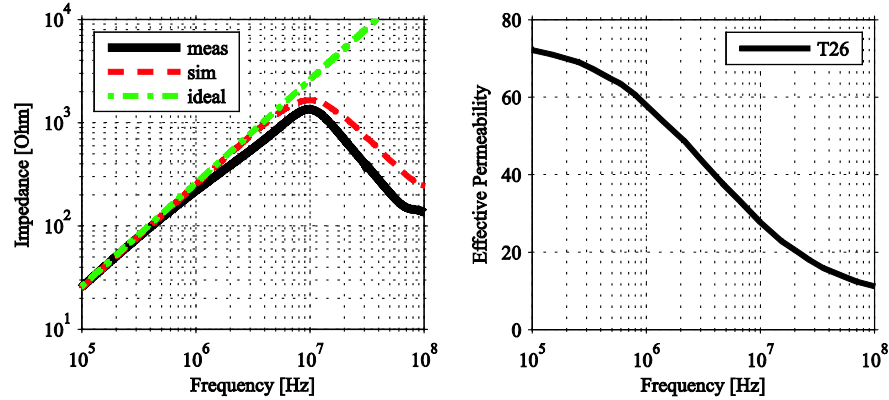
Fig. 6.28:   Left: Comparison of measured and simulated impedance of the input inductor standalone. Right: Datasheet values for the effective permeability as a function of frequency for Micrometals T26.

The intrawinding capacitance for the toroidal core T106-26 with 21 turns was calculated to approximately $C_w = 6pF$ ($R_1 = 1400\Omega$, $R_2 = 200\Omega$) which gives an input inductor that behaves inductively for frequencies up to $10MHz$. After this, the parasitic capacitances become dominant and the performance of the input filter will deteriorate significantly. It is also that noted the inductance decreases with frequency; at $5MHz$ the inductance has been reduced to $26\mu H$ (33% decrease) compared with its low frequency behavior. This is explained by the decrease in effective permeability for the specific iron powder material, see Figure 6.28, right picture. Note that the decrease in inductance is not accounted for in the simulation model.

The overall performance of the filter is to a large extent affected by the inherent parasitics. For this investigation, the parasitics are determined by measurements of the total input filter and the results are matched with simulations of the total input filter including interconnection parasitics. One of the dominating parasitic components in the investigated circuit was found to be the parasitic capacitance formed between the PCB and the inductor itself ($C_{stray} \approx 10pF$). This parasitic capacitor deteriorates the performance of the input filter so that it becomes capacitive for frequencies higher than $6MHz$, see Figure 6.29, right picture.
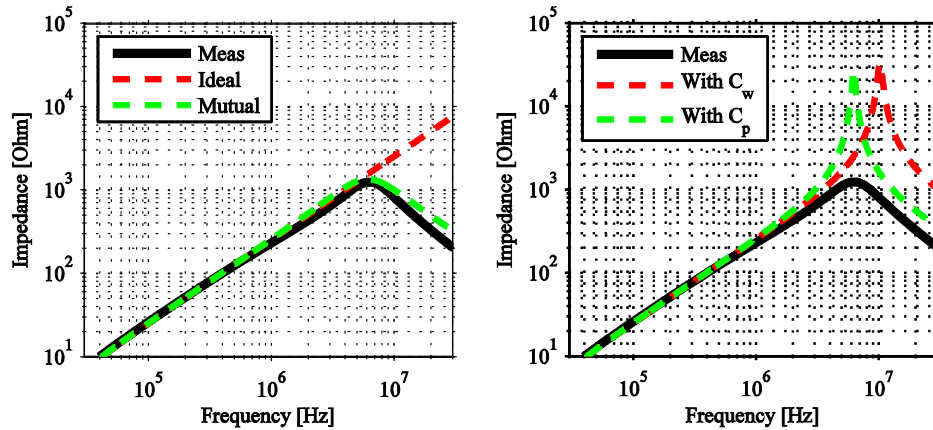
Fig. 6.29:   Comparison of measured and simulated impedances of the input filter with different configurations of the parasitic elements.

It becomes clear that it is not sufficient to only account for the intrawinding capacitance, since C_{stray} becomes dominating at higher frequencies. The origin of this capacitor is rather obvious since the toroidal input inductor is mounted directly over a grounded reference plane. If all parasitic elements from the interconnectors are taken into account, the simulated impedance matches the measured one rather well except for the decreased inductance, see Figure 6.29, left picture.

The total filter performance is not only affected by the parasitics in each component but also the mutual couplings. But since the investigated filter is large and the components are oriented in a favorable way (see Figure 6.30), mutual couplings becomes of minor importance which also is seen if the attenuation of the filter is analyzed; see Figure 6.31. The characteristics of the input filter is strongly dependent on the characteristics of the capacitor with best high frequency performance which in this case is the ceramic capacitor C_3.
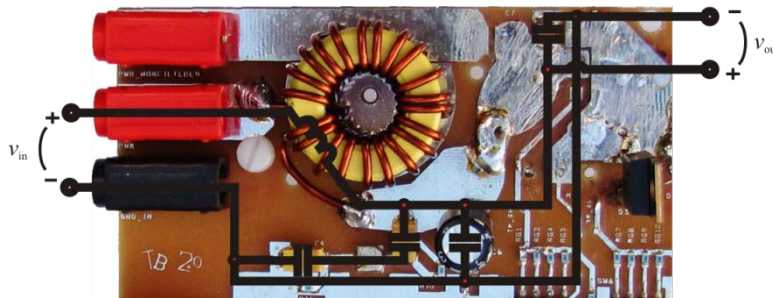
Fig. 6.30:   Photo of the component placement in the input filter of the step-down converter.
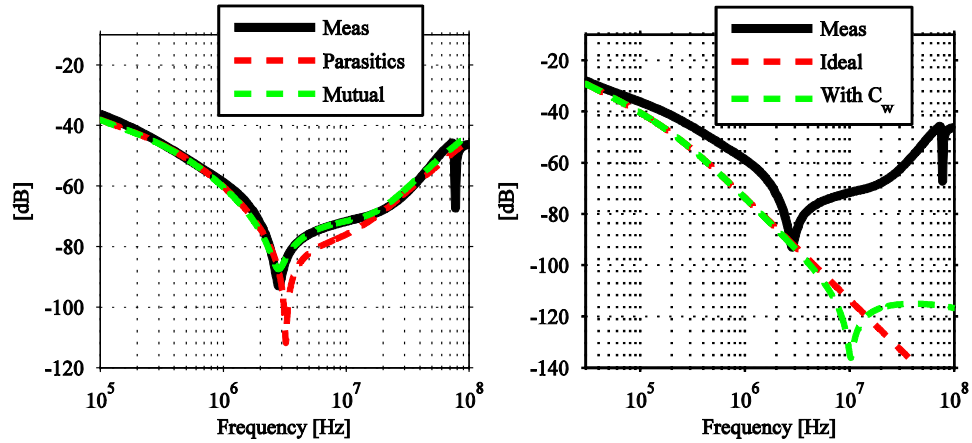
Fig. 6.31:   Step-down converter input filter attenuation including stray elements with added mutual inductances (left picture) and ideal filter compared with inductor with added intrawinding capacitance (right picture).

6.5.2   Stray Elements within the PCB

The parasitic elements within the PCB result in both interconnection inductances and capacitances that can be determined with Ansoft Q3D. The program gives a matrix with capacitive and inductive couplings between each element within the PCB which consequently can be implemented into Simplorer that co-simulates it simultaneously with the electrical circuit. The original PCB is simplified so that only the traces and planes that carry high currents are implemented in the simulation model, see Figure 6.32. Auxiliary circuitry such as clock, drive circuit, feedback loop and additional power regulators are omitted for reasons of simplicity. The circuit board is of standard fabrication and consists of $35\mu m$ copper on a $1.6mm$ FR4 epoxy laminate. All geometries and associated properties such as dielectric constant and conductivity are accounted for in Ansoft Q3D.
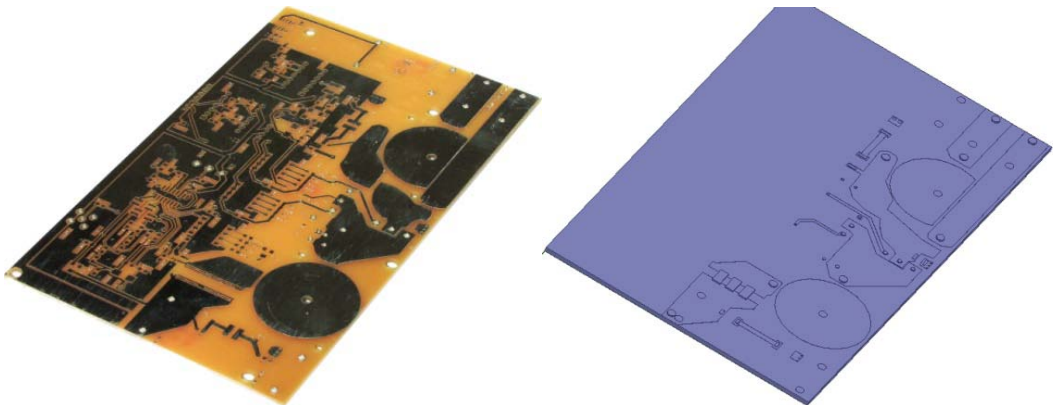
Fig. 6.32:   Comparison of the actual PCB and the Ansoft Q3D model.

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The result from Ansoft Q3d is a very large matrix that accounts for all couplings between each node. Due to the vast complexity of the Q3D simulation model, only a small selection of the most relevant couplings in the output filter of the converter are presented is Figure 6.33. However, by performing a co-simulation with Simplorer, all stray parameters within the PCB, including their frequency dependence, are taken into account.
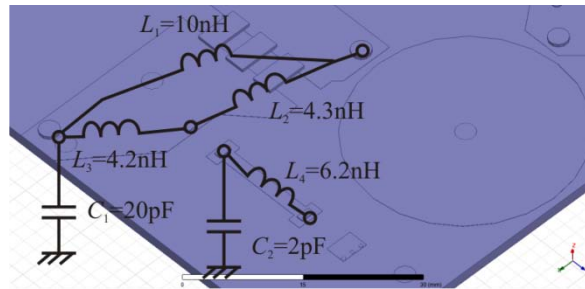
Fig. 6.33: A selection of stray elements in the output filter calculated by the Ansoft Q3D model.

6.5.3 Oscillations in the Circuit

If the diode current is analyzed, the reverse recovery process is well characterized in Simplorer due to the extended diode model. A slight underestimation of the reverse recovery charge can be noted for the 8ETU04 model, but the results are in general satisfactory and correspond well to the measurements, see Figure 6.34, left picture. The simulation model gives a current derivative ($\sim440A/\mu s$) that correspond well to the simulations ($\sim400A/\mu s$). This points out that the parasitic inductances within the PCB are calculated with good accuracy in Ansoft Q3D and that the parasitic inductances in the component interconnectors are well represented in the datasheet. Note that the possibility to measure currents requires some kind of current sensor to be implemented in the circuit; the increased current loop will inevitably cause increased stray inductance which may result in misleading results for the final converter.

Due to the representation of the parasitic elements in the circuit, the transition of the drain source voltage is also well represented, see Figure 6.34, right picture. Even though the amplitude of the voltage overshoot is slightly underestimated in the simulations, the main oscillation frequency was consistent between simulations ($1.6MHz$) and measurements ($1.8MHz$).

6.5.4 Diode Rectification

Diode rectification is the simplest form of rectification, but it also has some drawbacks, e.g. higher losses compared with synchronous rectification due to the reverse recovery and the forward voltage drop. Depending on the specifications of
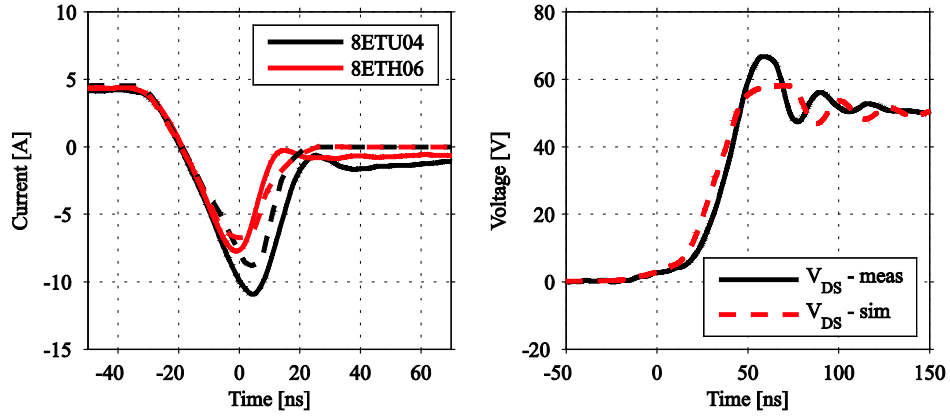
Fig. 6.34: Left: Measurements (solid line) and Simplorer simulations (dashed line) of the diode current (I_D) during reverse recovery for two diodes with different recovery characteristics. Right: Measurements (solid line) and Simplorer simulations (dashed line) of v_{DS} with diode 8ETU04 used as rectifier.

the selected diode, not only the reverse recovery parameters will differ, but also the inherent capacitance and forward voltage, see Table 6.6. All parameters will affect the EMI performance on the converter and as comparison; a Schottky diode is also evaluated to determine how the lack of reverse recovery affect the circuit performance. The aim is to analyze how the diode reverse recovery and the comparably large Schottky diode capacitance affects the conducted emissions.

Table 6.6   Specifications of the evaluated diodes.

Diode	I_F	V_R	$V_F @ I_F$	t_{RR}	$C_{tot@50V}$	L_S
8ETH06	8A	600V	2.0V@8A	18ns	24pF	5nH
8ETU04	8A	400V	1.2V@8A	60ns	30pF	5nH
43CTQ100	8A	100V	0.7V@20A	N/A	430pF	8nH

The simulation model of the characterized passive components in combination with the quantification of the PCB parasitics gives a simulation model that corresponds well to the measurements up to approximately 10MHz, see Figure 6.35. As previously discussed, a diode with greater reverse recovery (8ETU04) will result in higher levels of the conducted emissions which are seen in both measurements and simulations. However, the mathematically derived statement that a diode with sharper recovery gives higher harmonic content at higher frequencies is obvious in neither simulations nor measurements. The input filter effectively attenuates higher frequency harmonics and for frequencies over $10MHz$, the levels are as low as $50dB\mu V$ (which corresponds to $100\mu V$); this are extremely low voltages which makes the error tolerance high. A slight difference in emission levels are seen at higher frequencies (>10MHz) which amongst other factors originate from miscalculated mutual couplings in the input filter and LISN.
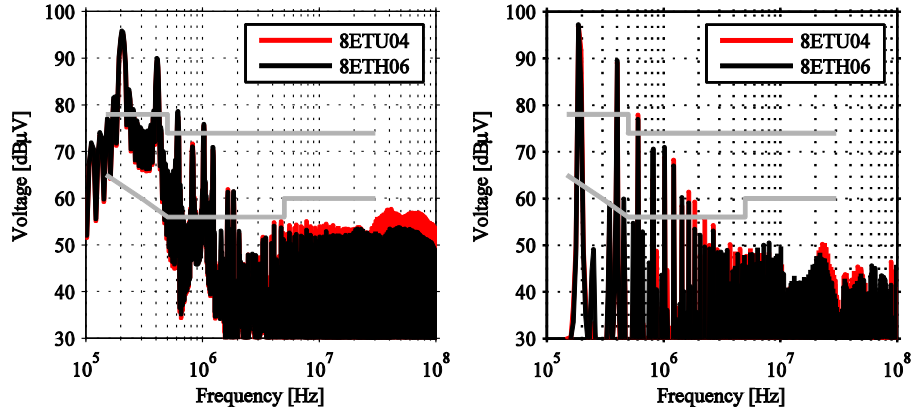
Fig. 6.35:   Conducted emissions of for a buck converter ($V_{in} = 24V$, $V_{out} = 5V$, $I_{out} = 4.5A$), pn-diode rectification with different reverse recovery. Left: Simplorer Simulation. Right: Measurements.

Implementation of a Schottky diode gives a slight increase of the oscillations in the circuit, especially in the diode current during turn off. However, high frequency oscillations are rather well damped and therefore are the emission levels also noticeably reduced at higher frequencies ($> 4MHz$), see Figure 6.36. The same tendency is seen in both simulations and measurements and the conclusion drawn is that for the investigated case, the presence of a high recovery current peak in a regular pn-diode is dominant over the larger capacitance within a Schottky diode; the stray elements are not sufficiently large to create oscillations in the step-down converters. The most noticeable high frequency oscillation in the measurements with a Schottky diode is the presence of a harmonic peak at approximately $60MHz$. This oscillation frequency is also seen in the drain-source voltage (v_{DS}) which most likely is reflected in the measured emissions.
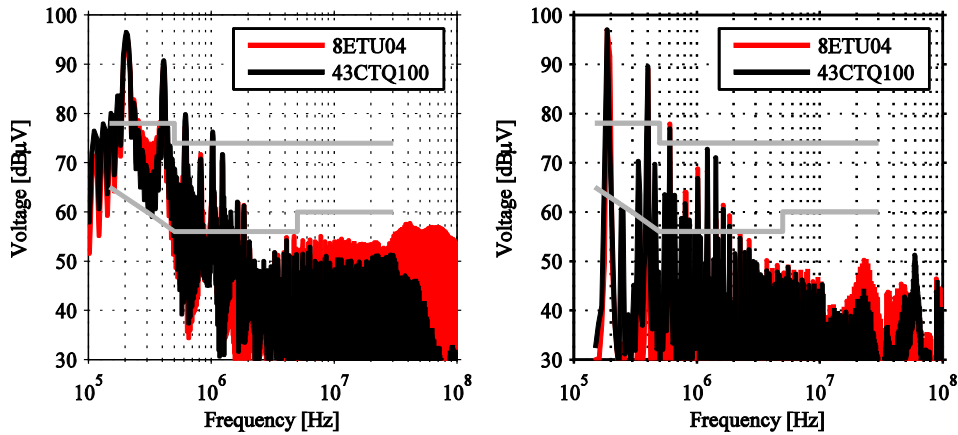
Fig. 6.36:   Conducted emissions of for a buck converter ($V_{in} = 24V$, $V_{out} = 5V$, $I_{out} = 4.5A$), comparison of Schottky (43CTQ100) and pn-diode (8ETU04). Left: Simplorer Simulation. Right: Measurements.

6.5.5 Synchronous Rectification

To reduce the effects of diode reverse recovery even further, synchronous rectification can be applied. The purpose is to evaluate different types of synchronous rectifiers with and how the switching characteristics affect the EMI performance. The specifications of the evaluated low-side switches are presented in Table 6.7.

Table 6.7   Datasheet specifications of the evaluated synchronous rectifiers.

MOSFET	I_D	V_{DS}	t_{on}	t_{off}	Q_G	C_{RSS}	V_{SD}	t_{rr}	Q_{RR}
IRFP150N	$42A$	$100V$	$67ns$	$95ns^1$	$110nC$	$230pF$	$1.3V$	$180ns$	$1.2\mu C$
IRL1004	130ι	$40V$	$226ns$	$39ns^1$	$100nC$	$320pF$	$1.3V$	$78ns$	$180n\iota$
FDFS6N548	$7A$	$30V$	$8ns$	$16ns$	$9nC$	$65pF$	$0.9V$	N/A	N/A

     1)   The measured and simulated turn-off times indicate an inverse relationship between the two MOSFETS at the investigated operating point.

The switching performance and the emission levels from the converter are strongly dependent on which type of low-side rectifier that is used; both the turn off time and the diode performance contribute to the switching performance. By changing the low-side switch, not just one property will change but rather the entire performance of the switch will be changed and consequently also the switching performance. For this investigation, the blanking times were kept constant and since the current is forced to freewheel through the body diode of the synchronous low-side switch during the blanking time, the performance of this diode still contribute to the EMI behavior of the circuit, see Figure 6.37.
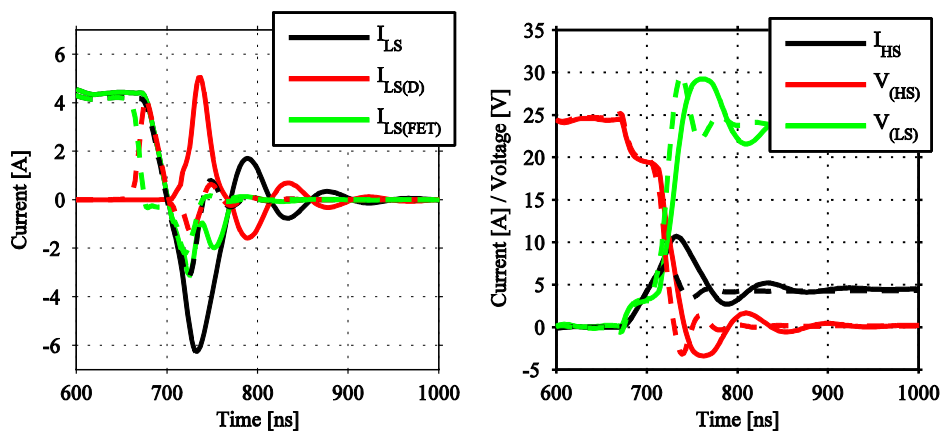
Fig. 6.37:   Simulated currents and voltages with synchronous rectification. ($V_{in} = 24V$, $V_{out} = 5V$, $I_{out} = 4.5A$). Solid line: IRL1004 as low-side switch. Dashed line: IRFP150N as low-side switch.

As footnote 1 in Table 6.7 suggests, the specified values of turn-off times in the datasheet does not correspond to the simulated results. The exact path of the current flow is impossible to determine with measurements since the two components are located in the same package. The increased current peak in IRL1004 seen in the simulations is also observed in the measurements which indicate that the simulation results are valid. This disqualify the original intent with the study (reverse recovery during the blanking time), but instead is the turn-off event put in focus. It can be concluded that a diode with faster switching time and higher stray elements (IRL1004) gives higher emission levels at lower frequencies $(3 - 6MHz)$ both in the simulations and in the measurements, see Figure 6.38. This increase can be deduced to the increased current peak during turn-off of the low-side switch. On the other hand, a low-side switch with smaller stray elements (IRF150N) will give rise to oscillations with higher frequencies which can be seen in both the drain-source voltage (Figure 6.37, right picture) and in the conducted emissions (Figure 6.38).
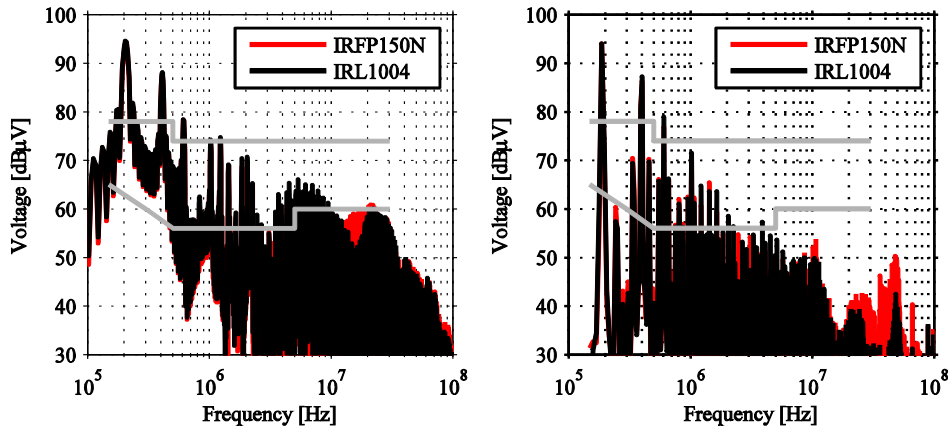
Fig. 6.38: Conducted emissions of for a buck converter with synchronous rectification and different low-side switches ($V_{in} = 24V$, $V_{out} = 5V$, $I_{out} = 4.5A$). Left: Simplorer Simulation. Right: Measurements.

An extra measure that can be taken to reduce the emission levels even further is to implement a low-side switch with an integrated Schottky diode (FDFS6N548), this ensures that the body diode does not have to conduct at all, not even during the blanking time. By adding a diode with shorter turn-off time, the body-diode (or Schottky diode) will conduct the entire load current during the blanking time. The fast turn off-time of the low-side switch also gives low reverse transfer capacitance ($65pF$) and stray inductances which e.g. gives a low overshoot in the drain-source voltage, see Figure 6.39 that show a comparison of the simulated currents and voltages with and without the Schottky diode.

The shift in conducted emission levels is very small when the co-packaged Schottky diode is enabled, see Figure 6.40. The most noticeable difference in both

simulations and measurements is seen at frequencies above $20MHz$ where the configuration with Schottky diode gives a slightly reduced levels ($\sim 2dB$ at $4.5MHz$). However, a significant difference is noted if the measured emission levels with a fast low-side switch (Figure 6.40, right picture) is compared to the levels from a slower low-side switch (e.g. IRL1004 in Figure 6.38, right picture); a decrease with $\sim 9dB$ at $4MHz$ that most likely originate from the lack of reverse recovery and other current overshoots.
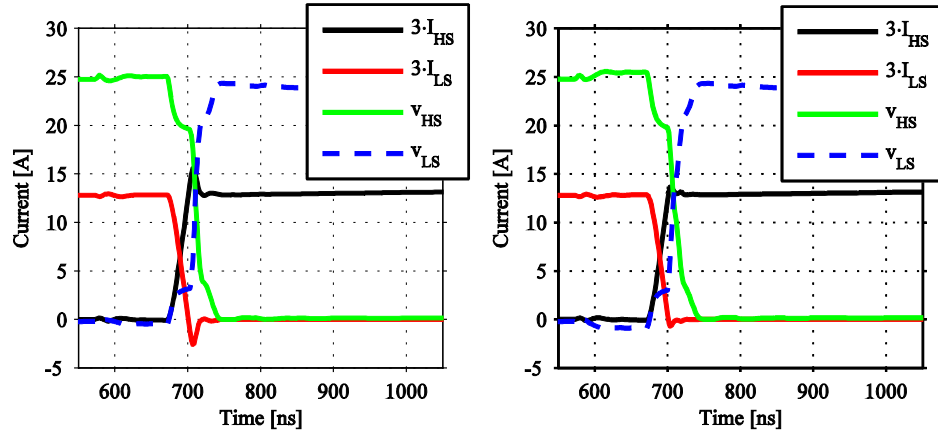
Fig. 6.39: Simulated currents and voltages with synchronous rectification (FDFS6N548 as low-side switch). ($V_{in} = 24V$, $V_{out} = 5V$, $I_{out} = 4.5A$). Left: without internal Schottky diode. Right: with internal Schottky diode.
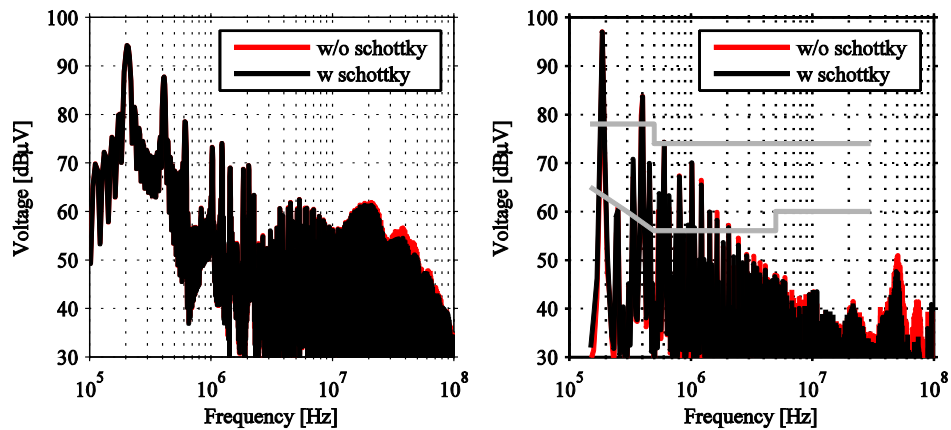
Fig. 6.40: Conducted emissions of for a buck converter, synchronous rectification (FDFS6N548 as low-side switch) with and without integrated Schottky diode ($V_{in} = 24V$, $V_{out} = 5V$, $I_{out} = 4.5A$). Left: Simplorer Simulation. Right: Measurements.

Chapter 6 - Implementation into Converters

Chapter 7

Concluding Remarks

7.1   Conclusions

In this thesis, the conducted EMI from switched power converters has been analyzed using various existing and own-derived models. The established theories of the relationship between EMI-generating mechanisms in a converter and conducted emission levels were initially verified mathematically and by simulations. The simulations were then verified with measurements that to a large extent verified the earlier stated theories even though the differences might not be as distinct due to the impact of stray elements not accounted for in the simulations. To simulate a converter with sufficient accuracy, each component in the converter, both passive and active, were thoroughly characterized and the existing component models were verified to ensure that all necessary high frequency properties such as stray inductances, capacitances and mutual inductive couplings were accounted for. In addition to the analysis of the conducted emissions, a new method to reduce the EMI directly at the source in a switched converter was analyzed. The principle is referred to as active gate control and aims at reducing the high frequency content in the otherwise sharp voltage and current transitions. The functionality is verified both theoretically and by measurements that establish the operation principle.

7.1.1   Component Modeling

The ingoing components in a switching converter must be modeled with respect to their high frequency behavior since it to a large extent affects the conducted EMI. At first, each component must be verified as a standalone unit; i.e. the high frequency behavior of all passive components must be accounted for. In some cases, the manufacturer (e.g. the capacitor manufacturer Kemet) provides high frequency models of the components, but for many other components this is not the case. For most types of components, it has been shown that the capacitive and inductive parasitic properties can be modeled sufficiently well with simple equivalent circuits. Other effects that may occur in passive components at higher

frequencies, such as inductance decrease due to reduced effective permeability, was not found possible to model in a simple way.

Furthermore, the modeling of the dynamic properties of diodes (i.e. mainly the reverse recovery phenomenon) was shown to be rarely accurately predicted by the simulation programs used. The diode model in both Simplorer and SABER$^{®}$ accounts for this and makes it possible to simulate dynamic events correctly in contrast to the diode model in SPICE that shows a snappy recovery behavior.

The simulation models for power MOSFETs provided by the manufacturers are often sufficiently accurate and adapted to switching applications. The gate-drain capacitance was shown to have great influence on the switching behavior of a MOSFET since it varies strongly with the applied voltages. In contrast to what often is stated in the datasheet, it not only shows voltage dependence on the drain source-voltage (v_{DS}) but also on the applied gate-source voltage (v_{GS}).

The most suitable IGBT model found in this thesis was the Simplorer model that, but even though a parameter extraction tool is provided, a full covering component model requires manual additions and modifications. By using datasheets and measurements, it is possible to characterize an IGBT so that sufficient switching performance is achieved. The IGBT model in Simplorer will also account for temperature effects such as extended tail current.

7.1.2 Active Gate Control

The proposed MOSFET model was used to show that it is possible to achieve better controllability of a system comprising of varying parameters with an adaptive control algorithm. Regarding the output of the system, the controllability is significantly better for a system where the drain current is selected as an output compared to a system where the drain-source voltage is selected as an output. Nevertheless, certain problems still exist where the greatest problem to overcome is how the reference voltage shall be adapted to the present operating conditions.

The suggested procedure for extracting parameters, although not completely correct from a control theory point of view, gives the possibility to approximate suitable values already at the simulation stage of the development work. It is shown that a single operating point is not sufficient when the controller parameters are to be determined. The total system is a complex entity with many non-linear variables and a procedure for finding the adaptive control parameters is presented in this thesis.

The principle of active gate control is found to be working sufficiently well for slower switching transitions ($> 20\mu s$). For faster transitions, the derived controller structures still work, but disturbances can be noticed due to saturation

of the controller.

The switching losses can in some cases be lowered if active gate control is applied. This statement holds true for the fastest switching transitions ($4\mu s$) investigated in this thesis.

7.1.3   System Modeling

The first and perhaps most important remark when it comes to system modeling is that EMI-modeling is a very complex subject and even though each component is well characterized, the predicted emission levels from a complete converter might not be predicted correctly. It shall be kept in mind that the analyzed voltage levels in the conducted emission often are very low; the lowest limit in the CISPR 22 class B standard is $56dB\mu V$ which corresponds to $0.63mV$. Even a small error in e.g. the input filter characterization of a converter will therefore inevitably result in incorrect emission levels.

The need for a diode model with correct reverse recovery behavior was shown to be essential since the reverse recovery event affects the conducted EMI in the frequency region of $5 - 30MHz$. The connection between reverse recovery and emission levels has been verified in simulations and measurements for two different types of converter topologies. A sharp recovery current will most likely result in higher levels of harmonics.

It has been shown both experimentally and in simulations that the conducted emission levels are strongly determined by the mutual couplings in the input filter. Depending on the type of filter and the orientation of the filter components, the mutual couplings can be of more or less importance. For the compact input filter with open core inductors on the investigated flyback converter, the mutual couplings are more dominant than for the filter on the synchronous step-down converter. This is explained by the fact that the buck filter is spaciously designed and that a toroidal inductor is used which minimizes the stray inductances.

Regarding synchronous rectification, the body diode and the turn-off time in the low-side MOSFET was shown to influence the conducted emissions in a negative way. A slow MOSFET results in longer switching transitions which in turn result in a longer blanking time; a time interval in which the body diode must conduct. By implementing a low-side switch with integrated Schottky diode, the emission levels will most likely be lowered since the Schottky diode reduces the conduction time of the slow body diode.

7.2   Future Work

Many of the studies performed in this thesis have been performed with user

friendliness and the everyday engineer in mind. This made the work relatively broad so that all essential ingoing subsystems within in a switched converter were covered. However, the broadness also highlighted several new problems that were encountered and other issues worth investigating also emerged. Based on the investigations performed in this thesis, some ideas for further research in this and related fields are outlined below.

- More detailed modeling of magnetic components such as inductors and transformers. Even though a simple equivalent circuit often is sufficient to characterize the high frequency behavior of an inductive component, some mechanisms such as decreased inductance due to reduced effective permeability, is not accounted for in the proposed models.

- More thorough FEM modeling of the input filters in order to characterize and quantify the mutual couplings in a better way. Also, it is of great interest to further analyze the possibility to co-simulate FEM-calculations of the input filter together with Ansoft Simplorer so that even mutual couplings can be accounted for in the electric circuit simulation.

- Analyze how the control of the converter affects the EMI performance. Due to reasons of simplicity, all simulations have been performed at steady state adapted to the current operating point. Therefore, it would be of interest to investigate how the control circuit and fluctuations in control voltage affect the EMI performance.

- Deeper analysis with Ansoft Q3D. How do the parasitic elements in the PCB affect the switching behavior and is it possible to model even more complex structures? If only surface mounted components are considered, it might even be possible to simulate the mounted components including e.g. bond wires.

- Digital implementation of the active gate control algorithm, including the proposed pre-charging. By digital control, the control parameters of the system can be totally configurable and encountered problems such as adaptation of the reference voltage to the current operating conditions can be solved. It might even be possible to alter the controller parameters during a switching event in a digital environment.

- Develop a better algorithm for determining the proportional and integral gain when adaptive control is used. The trajectory which the system takes during a switching interval is strongly determined by the controller parameters which can be more clearly defined.

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