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International Journal of Electrical Engineering Education (ISSN: 0020-7209)

Citation for the published paper:

Larsson-Edefors, P. (2010) "Teaching Bachelors Electronic Circuits with Electronic Systems Design in Mind". International Journal of Electrical Engineering Education, vol. 47(3), pp. 263-276.

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Teaching Bachelors electronic circuits with electronic system design in mind

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Abstract This paper presents the development of Electronic Circuits, an elective course in the final year of computer and digital system engineering Bachelor programmes at Chalmers University of Technology. Serving as a bridge between the traditional circuits perspective of junior-level courses and the electronic system perspective of senior-level courses, the course was developed to lay a foundation for contemporary electronic system design in a manner that spurs student motivation. The course adopts an integrated view of analog circuits, digital circuits, and wires, and this necessitates a new pedagogical flow, including an extensive set of design-oriented exercises.

Keywords analog circuits; CMOS integrated circuits, digital circuits, electrical interconnects; electronic system design

The subject area of electronic circuits appears to have a declining appeal to engineering students in Sweden, and the trend seems to be the same in many other countries across Western Europe and in the US. Unless we change the way we present and teach electronics, the trend toward *embedded* electronics may lead to a lost generation of electronics designers: Students need to get under the hood of embedded systems to make their interests gravitate toward electronics.

The educational challenge of the electronics area is that it takes considerable patience on the part of the students to attain the level of understanding that makes them productive as designers. In contrast, software is easier to understand and quicker to apply in the design of useful systems. We who have been teaching electronics within a traditional five-year bottom-up curriculum notice that the reward of basic training seems sometimes not large enough to make students endure a string of basic non-applied courses in physics, electric circuits, transforms etc. Could it be that there is no lack of talent among students, but that it is rather a question of motivation to study complex, non-applied subjects? Could it be that the Bachelor-level electronics curriculum needs to be changed so that training of circuits fundamentals is accompanied by motivating electronic system applications, using real design and analysis environments?

We have tried to address the above questions in the context of Bachelor programmes with a profile of computer and digital system design engineering. Here the trend is that many talented students choose to study software design, rather than intricate electronics design. Studying software is not a bad career choice, as the industry certainly has a large need for software-oriented designers. However, the electronics industry *depends critically* on the universities' ability to shape a new breed of electronic system designers that have a combination of skills in software, hardware architecture and circuits. Computer and digital system design engineering

students generally have a very suitable background for electronic system design and, if motivated, they indeed perform well in their electronic system design studies. This paper will describe our experiences in teaching such Bachelors electronic circuits with electronic system design in mind.

Background

Chalmers University of Technology recently adopted the two-tier Bachelor/Masters system of the Bologna declaration. In 2006 we hence started to develop the curriculum of an Integrated Electronic System Design (IESD) Masters programme. The curriculum of this programme emphasises digital systems and architectures; however, it is the conviction of the teaching team that a thorough understanding of circuit issues is necessary to make wise design decisions also at higher levels of design abstraction.

One of the early issues in developing the IESD programme was that of prerequisite courses in the Bachelor programmes: What knowledge and what skills should be expected from students admitted to our Masters programme and, consequently, what should be the technical content of the prerequisite courses? How do we help instil an interest and engagement in impatient Bachelor students that have grown somewhat tired of bottom-up teaching and fundamental courses that lack fun applications? The challenge is to create prerequisite courses that not only efficiently bridge the subject matter of the Bachelor-level and the Masters-level courses, but also have a pedagogical format that motivates students to work hard.

This paper gives an account of the work spent on EDA351 Electronic Circuits,² a prerequisite course to IESD for Bachelor students in computer and digital system engineering. A constraint for the implementation of this course is that the students have previous experience of neither electromagnetic nor semiconductor technology. In fact, they have taken only one basic course addressing basic circuit analysis and signals, and one basic course addressing transforms, control theory, etc.

Conventional Bachelor-level electronics training

Conventionally, Bachelor programmes associated with electrical engineering start their electronics training with an introduction to electric circuits, emphasizing basic circuit analysis. In Sweden at least, areas other than electronics (telecomms, automatic control, and device engineering to name just a few) are competing for electrical engineering students. Thus, the electrical engineering Bachelor programmes at Chalmers as well as the other major Swedish technical universities, in Lund, Linköping, and Stockholm, have only one other circuits-centric electronics course, in year 2 or 3, which focuses on analog circuits.

Considering that software and architectural aspects also need to be covered, the electronics course package in the area of computer and digital system engineering has of necessity to focus on higher levels of design abstraction. Again, basic electric circuits are introduced in the first year, but this turns out to be the only circuits-centric electronics course of the entire Bachelor programme. At least this is the case in the Bachelor programmes throughout Sweden, with the exception of Chalmers,

for which the tailor-made EDA351 Electronic Circuits is an elective course for third-year students.

The new course and its content

As the second circuits-centric electronics course in computer and digital system engineering oriented programmes, EDA351 Electronic Circuits² aims to bridge, already at the Bachelor level, the gap between the circuit perspective of junior-level courses and the system perspective of senior-level courses. To match the course content to the student background, the IESD Masters programme focus and the industry needs, the course has a relatively large emphasis on the digital aspects of circuit design, which is a novel approach judging by the composition of the major textbooks in the field (see the next section). The course content represents rudimentary skills of an electronic system designer and consists of an unconventional mix of subject matter: analog circuits, digital circuits, and wires.

Especially the third component, wires, stands out in the context of Bachelor-level courses. Wires are becoming increasingly important in electronic system design, ranging from boards to integrated circuits, so circuit-centric courses at the Bachelor level could generally benefit from including wire aspects, if possible. The problem in programmes with a digital orientation is that the students may lack, partially or completely, an understanding of electromagnetics. On the other hand, because wires are so important in electronic systems, it is not a question of *if* wires should be treated in a digitally-oriented electronics programme, but *when*. We view the early inclusion of wires as a way to enhance the connection to system aspects, rather than getting one more complex issue to study.

Some design considerations of this course traditionally belong to the Masters level, for example, dissipation of power and energy in digital circuits, performance and power impact of transistor capacitances on logic gates, and modeling of both lossy and lossless wires. Again, we chose to include such details to be able to give a fuller picture of circuits in the context of electronic systems, to increase student motivation. At the same time, the expansion into digital aspects forces us to shorten the treatment of analog circuits. However, by limiting the training of skills in the analog area to

- integrated circuit platforms (no discrete circuits);
- MOSFETs (no bipolar transistors);
- a minimum of transistor circuit topologies, such as only common-source amplifying stages (no common-gate nor common-drain stages);
- high-frequency amplification aspects (no low-frequency aspects),

we still are able to reach all the way to the design of a simple operational amplifier, in the form of a demonstration.

The problem of matching content to textbook

A practical problem resulting from the chosen course content is that there exists no single textbook that covers the area. Among textbooks on electronic circuit design that find widespread use in final-year Bachelor-level courses, we especially note

Sedra and Smith,³ Jaeger and Blalock⁴ and Spencer and Ghausi.⁵ All these textbooks focus heavily on analog circuit design and pay relatively little attention to digital circuit design. Worse yet, the treatment of wires is negligible:

- Sedra and Smith briefly discuss wire issues in 11.7.6. Speed of operation and signal transmission, which amounts to one page out of 1283 (or 0.08% of the entire textbook);
- Jaeger and Blalock do not discuss wires at all;
- Spencer and Ghausi devote a small portion of the book to lossless wires: 14.4. Reflections on transmission lines uses four pages out of 1081 (or 0.37% of the entire textbook);

Today, wire issues become a first-class citizen only when the students reach Masters level. Commonly used VLSI-oriented textbooks, such as Refs 6 and 7, approach circuit design with a combined view of transistors and wires, but generally the level of those books is too advanced for Bachelors that only have studied the fundamentals of electric circuits.

Course organization and language

EDA351 Electronic Circuits is given over a seven-week time span, and its learning outcomes (see below) rest solely on the material delivered through two teaching constituents: Thirteen lectures, comprising 530 slides, and eleven design-oriented exercises, described in an 87-page lab memo. The students are still encouraged to purchase a 'reference' book³ that is good for in-depth reading, especially in the analog circuit domain. Since digital aspects, especially wires, are missing in Ref 3, a chapter on lossless wires is downloadable from the course site.

The choice of language is related to the way the course material is provided. Although virtually all Swedish students speak English fluently, the course is given in a Swedish version only, to avoid having any language barriers and to obtain as high a learning efficiency as possible (however, in subsequent Masters courses, teaching is conducted in English). An added reason for the choice of Swedish as language was that the course material potentially could lend itself also to teachers in electronics courses preparing for university. Recruitment of students to electronics programmes at university must start as early as possible.

Hands-on training

In engineering training, hands-on experiments are important as a means to corroborate an initial analysis. A successful confirmation can boost confidence, increase motivation and serve as a guide to the engineering context. Here, design-oriented exercises based on simulation are referred to as being hands-on, although the term hands-on usually defines tinkering in a lab, using physical objects. It should be noticed that the use of simulation-based exercises is not a compromise solution to learning the best design practice of industry, for which the main design activities take place in CAD-based design and verification environments.

The main pedagogical advantage of using simulation-based exercises is that the hands-on training can be scheduled in a very time-efficient manner, leading to an increased teaching pace. Selecting the right pace is a delicate trade-off: We do not want to go through the course content too fast, because the teaching will then be superficial and student attention will drop directly. At the same time we need, for the sake of student motivation, to avoid spending too much time on the basic tools in the toolbox. The first, elementary phase of the course must be followed by more complex and realistic design contexts in the final course phase. As will be shown later, the exercises in this course have shown very good results in terms of student learning outcomes.

Simulation-based exercises have been used in university courses for quite some time. However, to the best of the author's knowledge, the use of eleven consecutive exercises, which span the full content of the 7-week course, makes this course unusual.

Content of exercises

For all eleven exercises, the pedagogical flow is such that there is:

- a preparation phase, in which assignments are solved using analytical (and numerical) methods prior to the exercise hours. Some assignments cannot be prepared, but are carried out on-line during the exercise, as simulation results are gradually obtained;
- an execution phase, in which the analytical preparation is corroborated by simulations using SPICE;
- a reporting phase, when analytical and simulation results are reported to the teacher, for a pass on the exercise;
- a final exam, which forces students to revisit all exercises, for repetition.

In the following, the main features of each of the exercises are described.

Exercise 1: Circuit analysis and basic simulation

In the first exercise, the students rehearse basic circuit analysis. Furthermore, this exercise introduces circuit simulation for a few basic components (resistances, capacitances and diodes), showing the basic steps to carry out a d.c. sweep.

This exercise has three important learning objectives, all relating to *the context* in which circuit analysis techniques are used:

- By using Kirchhoff's laws, voltages and currents in a d.c. circuit can be found by way of either equation solving, graphical methods or simulation aid;
- The $j\omega$ method for stationary a.c. voltage and current allows us to administer an analysis that, in terms of methodology, corresponds to d.c. analysis. Here the students also study the resulting amplitude and phase of the output signal from the a.c.-driven circuit, focusing on the relation of phase and time delay in anticipation of the digital circuit exercises.
- The usefulness of graphical methods to solve steady-state currents and voltages for non-linear components is demonstrated, and the incompatibility between the concept of resistance and nonlinear components is highlighted. These reflections



Fig. 1 Amplifying stage of Exercise 2.

are useful in later exercises, for example when we study the small-signal resistance in analog circuits and the ON-resistance in digital circuits.

Regarding the last learning objective, it may seem like an obvious fact that non-linear components are distinguished as components having a non-linear relation of applied voltage and resulting current. However, for many of today's students a solid and intuitive interpretation of 'non-linearity' is missing.

Exercise 2: The MOSFET transistor and a basic amplifying stage

In order to maintain student interest, the second exercise – somewhat prematurely – launches the design of the simplest possible amplifying stage (Fig. 1). To allow students to simulate transistor circuits, the LEVEL 1 MOSFET model is explained. Since the students have no prerequisite knowledge of basic semiconductor technology, the teacher has to tread carefully when introducing transistor model parameters.

Here, the students study the amplifier transfer characteristic $V_{in} \rightarrow V_{out}$, as produced by SPICE. Using the MOSFET's W/L ratio as design variable, the students have two constraints to consider:

- To design the stage, such that the MOSFET is always saturated;
- To design the stage, such that it fulfils an amplification specification at the designated quiescent point.

Exercise 3: The voltage transfer characteristic of the basic amplifier

A transfer characteristic is the result of equation solving between a three-terminal MOSFET and a load resistance. In exercise 2, the transfer characteristic was 'magically' created by SPICE, while in exercise 3 the students are forced to recreate the characteristic themselves, manually: Separate load lines for the resistance and the MOSFET, respectively, are plotted, after which intersections are identified and logged.

In this exercise, the students also reflect on the fact that amplification has to do with the slope of the V_{out} (V_{in}) characteristic. In past instalments of this course, students often made the mistake of taking one point on the characteristic and calculating the ratio of V_{out} / V_{in} .

Exercise 4: High frequency aspects at the output of an amplifier

In exercise 4, the students study an amplifying stage that drives an output capacitance, that is, a loading stage. In this exercise, students have to prepare a small-signal

schematic of the output circuit, including the small-signal properties of channel resistance and transistor transconductance. Also, the corresponding analytical transfer function for V_{out} (V_{in}), in terms of amplitude and phase, is calculated prior to the exercise.

The execution stage of this exercise involves making transient simulations for a handful of frequencies and studying how well the resulting amplification agrees with the prediction of the transfer function. The a.c. sweep ability of the SPICE simulator is used to study the upper cut-off frequency and its relation to the pole of the transfer function.

Exercise 5: The CMOS inverter

To show the similarity of analog and digital circuits, the framework of transfer characteristics is preserved when the exercises on digital circuits begin. Initially exercise 5 deals with the trip point of a CMOS inverter; the students analytically derive the trip point and study its dependence on MOSFET parameter values, such as threshold voltage, W and L.

Now, when we move into the digital domain, one more opportunity to study MOSFET operating modes presents itself: The students analyse how the NMOSFET and the PMOSFET change operation modes as a toggling input signal, with finite edge rate, is applied to the inverter. Simulations corroborate that currents in the saturated devices agree well with the analytical current models.

Exercise 6: Charging gate load capacitances and gate delay

The static view of digital and analog circuits, in terms of transfer characteristics, d.c. sweeps etc., is good in that it provides simplicity. However, this view is not sufficient to explain the intricacies of charging and discharging inside logic circuits. Exercise 6 introduces the notion of time and transient simulations in the context of digital circuits: the students study a circuit in which a PMOSFET is charging an output capacitance that initially is empty.

The students use three ways to model the PMOSFET:

- A constant current source. This is a somewhat inaccurate approximation, as it only captures the saturated PMOSFET behaviour;
- An ON-resistance. This approximation captures the linear operation region of the PMOSFET, but fails to limit the current for higher channel voltages;
- The LEVEL 1 MOSFET model. This is the reference model.

The usefulness of the two first models is that they allow us to construct a simple analytical expression of the output rise time. Here, the key learning outcome is for the students to find out that the two first approximations underestimate the real delay. By studying the charging currents as function of output voltage as well as charging current over time (Fig. 2), the students are able to explain the inaccuracies of the approximative models.

Exercise 7: Power and energy dissipation in logic gates

Traditionally, Bachelor-level electronic circuits courses have their emphasis on analog features, while digital features are only treated superficially, if at all (see

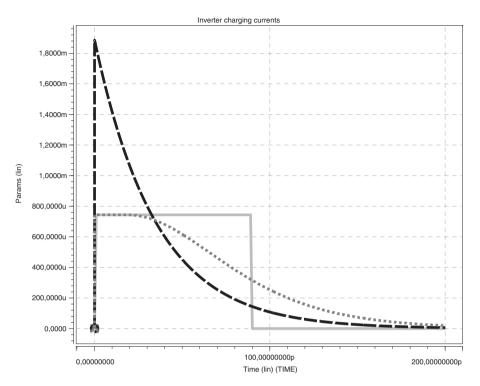


Fig. 2 Charging currents as functions of time in Exercise 6. The three different currents are: Solid line = current source, dashed line = ON-resistance, dotted line = LEVEL I PMOSFET.

earlier section on The problem of matching content to textbook). Since power and energy dissipation have become very important design parameters for digital circuits, these have been assigned their own exercise.

Exercise 7 is concerned with counting charges from the power supply, as an inverter charges its output to a logic 1. The students analyse what portion of drawn energy ends up being stored at the gate output capacitance, to recognize that power is dissipated in two distinct phases: Half in the PMOSFET- and half in the NMOSFET-network. We discuss the relation between power and energy, and discover that a gate's size only indirectly affects its power, through the potential to sustain high-speed operation and the subsequent clock rate increase.

Basic Bachelor-level courses in electric circuits tend to deal with power and energy in the framework of electric power engineering, such as reactive power etc. This framework unfortunately does not apply to electronics based on, for example, integrated circuits. Indeed the inclusion of this exercise was motivated by the lack of understanding of basic relationships for power and energy demonstrated by Masters students in past years.

Exercise 8: Capacitances in logic gates

In the exercises so far, the students are using the basic instantiation of LEVEL 1 MOSFETs, meaning that only gate oxide capacitances (Meyer models) are automatically modeled. Traditionally a Bachelor-level electronic circuits course does not deal with capacitances in detail. But the concept of parasitic properties is definitely worthwhile to introduce already at this level, since this has such a strong influence on analog and digital circuit performance.

In exercise 8, the students investigate gate oxide capacitances, to understand that CMOS logic circuit capacitance actually depends strongly on logic signal voltages (Fig. 3). They now also encounter the diffusion diodes, however, since the students have not studied semiconductor technology previously, the explanation of the physical origin of capacitances has to be very concise.

Exercise 9: Long lossy wires

In exercise 9, the students study different models for long lossy wires in the context of an inverter chain:

i) wire properties are neglected, ii) the wire is purely capacitive, iii) the wire is made up of one lumped RC segment, and finally iv) the wire is modeled as a distributed RC wire, which is the model that yields the highest accuracy, but also costs the most in terms of simulation time. To give an impression of real design challenges on integrated circuits and to illustrate the quadratic length dependence of delay, an assignment to partition a long RC-dominated wire, using repeaters, is included.

As two fundamental building blocks of digital circuits, wires and MOSFETs are quite different. But does this fact really pose a pedagogical challenge to a teacher in electronic circuits, which traditionally is lacking the wire perspective? Not really. So far, the inclusion of wires in the course is mainly a problem from a textbook point of view. This is because lossy wires easily can be related to the basic circuit analysis of low-pass filters!

Exercise 10: Methods for analyzing long lossless wires

Digital systems in general have some wires that are dominated by their LC properties and these lossless wires constitute the final part of the course. Lossless transmission

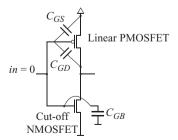


Fig. 3 The students are asked to list all gate capacitances of a CMOS inverter that has a logic 0 tied to its input.



Fig. 4 Transmission line circuit under analysis.

lines would traditionally belong to either a basic electromagnetics course or an advanced circuit design course. There are two major reasons to include lossless wires in this course:

- Lossless wire models are increasingly useful in real design situations. Such
 models are not only applicable to printed circuit boards, but also on integrated
 circuits, when fast signal edge rates and thick and wide wires in top metal layers
 are involved.
- The students of this course happen to lack basic training in electromagnetics.
 Thus, this part of the course also conveys portions of applied electromagnetics, paving the way for students to grasp issues such as electromagnetic interference (EMI).

In exercise 10, a transmission line is connected to a driver and a load. The students analyse the circuit with respect to propagation delay: Two different methods are employed to study $0 \rightarrow 1$ transients on the lossless wire.

The overall assignment of exercise 10 is to design a CMOS driver for a long lossless wire (Fig. 4), with the specification to reach a sufficiently high logic voltage level on the wire in a sufficiently short time. The students start to use a straightforward time-space diagram to log all reflections, assuming linear source and terminating load impedances.

As MOSFETs are non-linear devices, we know that we get an inaccurate result from a linear time-space analysis. Thus, in the second part of the exercise, the students need to use the Bergeron method, which is a graphical technique to solve non-linear equations, using the intersections of the load lines of source, wire and terminating load (Fig. 5). From this accurate analysis, the students find out that the specification is actually not met, and a redesign of the driver follows. Again, simulations are used to corroborate the analytical approaches (Fig. 6).

The exercise on lossless lines is quite different from the other exercises, as it involves electromagnetic considerations. On the other hand, through the use of the Bergeron methods, we once more make use of the concept of load lines and again return to the question on how to deal with non-linearity.

Exercise 11: High frequency aspects of a basic amplifying stage

In exercise 11, both the input and output circuits of an amplifying stage are studied, with and without the Miller capacitance. The first teaching block of the course was

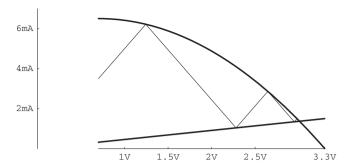


Fig. 5 Bergeron diagram for a non-linear PMOSFET driving a 3.3-V step onto a transmission line, which is terminated by a 2200 Ω resistance.

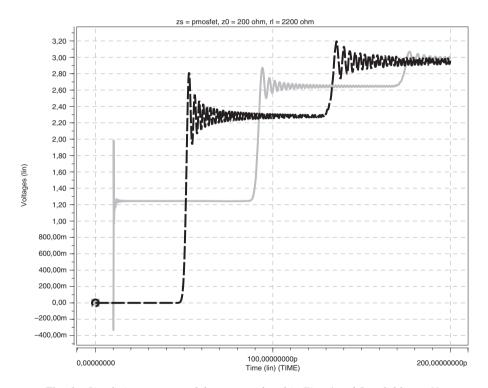


Fig. 6 Simulation outcome of the case analysed in Figs 4 and 5: solid line = V_s , dashed line = V_L .

on analog features, and it may appear better to have exercise 11 after exercise 4. However, in order to keep up student interest in the middle of the course, this final, more complex exercise is postponed. As a side effect, the students are now very proficient in handling the simulation environment, which simplifies the execution of this exercise. The first half of exercise 11 is centered around a small-signal schematic

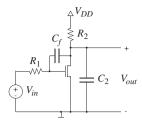


Fig. 7 The amplifying stage that acts as reference in the second half of Exercise 11.

of an amplifying stage; in one case an input-output coupling capacitance is included, in the other case it is not. The properties revealed by the analytical transfer function are compared to the simulation results. Particularly the amplitude Bode plot is interesting as a print-out allows the students to identify and compare pole frequencies. Here, the students discover that not only does the inclusion of the coupling capacitance increase transfer-function complexity, but it also gives rise to pole splitting.

In the final assignment, the students are asked to compare simulations of an amplifying stage (Fig. 7) with the corresponding small-signal schematic. After simulating the amplifying stage in Fig. 7, the students have to find the small-signal MOSFET parameters in the corresponding SPICE log file. Next they write the corresponding SPICE code for a small-signal schematic that uses the extracted parameters, using a voltage-controlled current source as replacement of the MOSFET. The simulation results (Bode plots) of the small-signal schematic hopefully agree exactly with those of the amplifying stage, again confirming the usefulness of small-signal thinking for analog circuits.

Student reactions

Student polls

All students from the course given in the period January-March 2008 were asked to take part in two polls, at the end of the course:

Exercises

Chalmers has implemented a mandatory, Internet-based poll. Beside a set of general, mandatory questions, the teacher and a small group of students that are designated 'course evaluators' can add questions pertaining to a particular course. The teacher and the course evaluators have two meetings during the course and an important part of these meetings is to identify what questions to include in the poll.

One question added to the poll asked which of the exercises the students appreciated – from a learning perspective – the most and the least, respectively. Exercise 9, 'Long lossy wires' turned out to be the favorite exercise for a third of the students, while half of the students rated exercise 7, 'Power and energy dissipation in logic gates' as the least effective one.

Altogether 80% of the students responded to this poll and they gave the course 4.5 as overall rating; where 1 = `very poor', while 5 = `excellent'.

Learning outcome	Importance	Fulfilment
Quiescent point of amplifier	4.6	4.1
Small signal operation of amplifier	4.4	3.8
Large signal behaviour in inverter	4.2	3.7
Charging behaviour of inverter with CL	4.2	4.2
First order delay and power dissipation	4.3	3.8
To distinguish lossy from lossless wires	4.5	4.2
Lossless wire analysis methods	4.2	4.0

TABLE 1 Student responses and main learning outcomes

Learning outcomes

Another (anonymous) poll was held in connection with the final lecture, regarding learning outcomes at a detailed level.² 87% of the students responded to this poll.

For each course block – analog circuits, digital circuits and wires – the main learning outcomes, together with the student responses, are listed in Table 1 below. Both student motivation ('how important is this learning outcome to me?') and learning outcome fulfilment ('how well does the course deliver on this particular learning outcome?') were measured.

Thus, the learning outcomes generally received favorable comments from the students, both in terms of importance and fulfillment.

Master programme application trends

At Chalmers there are currently more than 40 Masters programmes, among which Integrated Electronic System Design (IESD) represents electronic system design. To a large extent the students of IESD originate from the Chalmers Bachelor programmes of electrical engineering, and computer science and engineering. In terms of electronic circuits courses, the two programmes have two different courses, however, the textbook of Sedra and Smith is used in both.³ In contrast to EDA351 Electronic Circuits, the course for the electrical engineering students focuses, as outlined in the earlier section 'Conventional Bachelor-level electronics training', on analog circuit aspects. Also, the electronic circuits course for electrical engineering students is mandatory and takes place in year 2, not year 3.

In the spring of 2009, Bachelor students from Chalmers and elsewhere have applied for different Masters programmes. As for the question whether a course can help attracting students to the electronics area, the Masters programme application statistics show that less than 10% of the EE Bachelor students applied for the IESD programme. In contrast, 70% of the students that were active in EDA351 Electronic Circuits applied for the IESD programme. Here we must remember that EDA351 is elective and that the students attending this course have been filtered out from the rest of the Bachelor program.

In comparison to the application statistics of 2008, which was the second year that our Masters programme was operational, the electronics interest among

electrical engineering Bachelor students dropped in 2009, while a higher proportion of computer science and engineering students chose electronics.

Conclusions

The pedagogical ideas and the technical content of EDA351 Electronic Circuits at Chalmers University of Technology have been presented. Among the novel features of this course, we wish to highlight two: The integration of analog and digital aspects as early as possible, to spur student interest, and the comprehensive design-oriented exercises that define the content of the entire course. The course has been evaluated by the students and the results are encouraging both from the aspect of student motivation as well as student learning. Also, judging from the students that enter the succeeding electronics Masters programme, the course appears to successfully instil an interest among students in computer and digital system engineering.

References

- K. Jeppson, L. Peterson, L. Svensson, L. Bengtsson and P. Larsson-Edefors, 'A new Master's program
 in Integrated Electronic System Design', in *Proc. 7th European Workshop on Microelectronics Education*, Budapest, Hungary, May 28–30, 2008 (EDA Publishing Association, Grenoble, 2009).
- 2 http://www.ce.chalmers.se/edu/course/EDA351/, accessed July 2009.
- 3 A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 5th edn (Oxford University Press, Oxford, 2004).
- 4 R. Jaeger and T. Blalock, Microelectronic Circuit, 3rd edn (McGraw Hill, New York, 2008).
- 5 R. Spencer and M. Ghausi, *Introduction to Electronic Circuit Design* (Prentice Hall, Englewood Cliffs NJ, 2003).
- 6 J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, 2nd edn (Prentice Hall, Englewood Cliffs, 2003).
- 7 N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 3rd edn (Addison Wesley, New York, 2004).
- 8 P. J. Langlois, 'Graphical analysis of delay line waveforms: a tutorial', *IEEE Trans. Educ.*, **38**(1) (1995), 27–32.